SILICON TRANSISTORS & DIODES

1987

NEC NEC Corporation
NEC NEC HONG KONG Ltd.
NEC NEC HONG KONG Ltd.
Taipei Branch
NEC NEC SINGAPORE PTE. LTD.

AIR MAIL

ATTN: OUR CUSTOMERS

NEC Corporation

SILICON TRANSISTORS & DIODES 1987

K

SILICON TRANSISTORS & DIODES

1

NEC NEC Corporation
NEC NEC HONG KONG Ltd.
NEC NEC HONG KONG Ltd.
Taipei Branch
NEC NEC SINGAPORE PTE. LTD.

AIR MAIL

ATTN: OUR CUSTOM

NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

NEC reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

INDEX

TYPE NO. CROSS INDEX ii

QUICK REFERENCE GUIDE FOR PLASTIC MOLDED TRANSISTORS 3

NEC SEMICONDUCTORS 9

SEMICONDUCTOR STANDARDS 15

TECHNICAL SYMBOLS USED IN NEC'S SEMICONDUCTOR DEVICES 38

RELIABILITY AND QUALITY ASSURANCE SYSTEM OF NEC'S SEMICONDUCTOR DEVICES 43

PACKAGE DIMENSIONS AND STRUCTURES 71

DATA SHEETS (TRANSISTORS & DIODES) 77

TECHNICAL NOTES 1081

BLOCK DIAGRAM FOR ENTERTAINMENT EQUIPMENT 1166

APPLICATION NOTES 1178

© NEC Corporation 1980, 1987

TYPE NO. CROSS INDEX

Type No.	Use	Page
2SA639 Ⓢ	Display Tube Driver/High Voltage Amplifier	79
2SA733	Audio Frequency Amplifier	82
2SA915	Audio Frequency Amplifier	85
2SA916	Audio Frequency Amplifier	88
2SA952	Audio Frequency Amplifier	91
2SA953	Audio Frequency Amplifier	94
2SA954	Audio Frequency Amplifier	96
2SA987	Audio Frequency Amplifier	98
2SA988	Audio Frequency Amplifier	100
2SA990	Audio Frequency Low Noise Amplifier	102
2SA991	Audio Frequency Low Noise Amplifier	105
2SA992	Audio Frequency Low Noise Amplifier	108
2SA1005	FM Tuner RF Amplifier, MIX, CONV., OSC.	111
2SA1009, 1009A	High Speed, High Voltage Switching	114
2SA1142	Audio Frequency/High Frequency Power Amplifier	117
2SA1153	High Speed Switching	119
2SA1156	High Speed, High Voltage Switching	122
2SA1174	Audio Frequency Low Noise Amplifier	124
2SA1175	Audio Frequency Amplifier	127
2SA1206	High Speed Switching	130
2SA1220, 1220A	Audio Frequency/High Frequency Power Amplifier	133
2SA1376, 1376A	High Voltage Audio Frequency Amplifier	135
2SA1394	High Speed Switching	138
2SA1395	High Speed Switching	141
2SA1396	High Speed Switching	144
2SA1409	High Gain Amplifier	147
2SA1410	High Gain Amplifier	149
2SA1441	High Speed Switching	151
2SA1442	High Speed Switching	155
2SA1443	High Speed Switching	159
2SA1444	High Speed Switching	163
2SA1458	High Speed Switching	167
2SA1459	High Speed Switching	170
2SA1460	High Speed Switching(NEW DEVICE)	173
2SA1486	High Voltage High Speed Switching (NEW DEVICE)	176
2SA1544	High Voltage High Frequency Amplifier (NEW DEVICE)	179
2SA1545	High Voltage High Frequency Amplifier (NEW DEVICE)	181
2SA1546	High Voltage High Frequency Amplifier (NEW DEVICE)	183
2SB564	Audio Frequency Power Amplifier	185
2SB605	Audio Frequency Power Amplifier	188

Type No.	Use	Page
2SB731	Audio Frequency Power Amplifier, Low Speed Switching	191
2SB733	Audio Frequency Power Amplifier	193
2SB734	Audio Frequency Power Amplifier	196
2SB744, 744A	Audio Frequency Power Amplifier	199
2SB772	Audio Frequency Power Amplifier, Low Speed Switching	201
2SB794, 795	Audio Frequency Power Amplifier, Low Speed Switching	203
2SB810	Audio Frequency Amplifier	206
2SB811	Audio Frequency Amplifier	208
2SB984	Audio Frequency Power Amplifier	210
2SB1061	Audio Frequency Power Amplifier, Low Speed Switching	213
2SB1068	Audio Frequency Power Amplifier	215
2SB1093	High Gain Amplifier, Low Speed Switching	217
2SB1094	Audio Frequency Power Amplifier (NEW DEVICE)	219
2SB1095	Audio Frequency Power Amplifier (NEW DEVICE)	221
2SB1096	Audio Frequency Power Amplifier (NEW DEVICE)	223
2SB1098	Low Speed Switching	225
2SB1099	Low Speed Switching	228
2SB1100	Low Speed Switching	231
2SB1116, 1116A	General Purpose Power Amplifier	234
2SB1117	Medium Speed High Current Switching	236
2SB1149	High Gain Power Amplifier/Switching	238
2SB1150	High Gain Power Amplifier/Switching	240
2SB1151	Audio Frequency Power Amplifier	242
2SB1217	High Speed Switching, Low V_{CE} (sat) (NEW DEVICE)	244
2SC287A (B)	VHF TV Tuner Local OSC.	247
2SC288A (5.B)	UHF TV Tuner Local OSC.	250
2SC605 (B)	VHF TV Tuner MIX.	253
2SC606 (B)	VHF TV Tuner RF Amplifier	253
2SC923	Audio Frequency Amplifier	256
2SC945	Audio Frequency Amplifier	259
2SC945 Ⓛ	Audio Frequency Amplifier	262
2SC1070 (1)	UHF TV Tuner RF Amplifier	265
2SC1070 (2)	UHF TV Tuner MIX.	265
2SC1279 Ⓢ	Nixie Tube Driver/High Voltage Switching	268
2SC1280 Ⓢ	High Gain Amplifier/High Input Impedance Amplifier	270
2SC1280A Ⓢ	High Gain Amplifier/High Input Impedance Amplifier	273
2SC1393	VHF TV Tuner RF Amplifier	276
2SC1394	VHF TV Tuner MIX.	276
2SC1449	Audio Frequency/High Frequency Power Amplifier	279
2SC1674	FM Tuner RF Amplifier, MIX., CONV., OSC.	281

Type No.	Use	Page
2SC1675	AM/FM IF Amplifier, AM CONV., OSC.	285
2SC1730	VHF/UHF TV Tuner OSC., VHF MIX.	288
2SC1840	Audio Frequency Amplifier	291
2SC1841	Audio Frequency Amplifier	293
2SC1842	Audio Frequency Low Noise Amplifier	295
2SC1843	Audio Frequency Low Noise Amplifier	298
2SC1844	Audio Frequency Low Noise Amplifier	301
2SC1845	Audio Frequency Low Noise Amplifier	304
2SC1940	Audio Frequency Amplifier	307
2SC1941	Audio Frequency Amplifier	310
2SC1957	High Speed High Voltage Switching	313
2SC2000	General Purpose Amplifier	316
2SC2001	Audio Frequency Amplifier	319
2SC2002	Audio Frequency Amplifier	321
2SC2003	Audio Frequency Amplifier	323
2SC2026	High Frequency Low Noise Amplifier	325
2SC2037	High Frequency Low Noise Amplifier	328
2SC2333	High Speed High Voltage Switching	331
2SC2335	High Speed High Voltage Switching	334
2SC2352	VHF TV Tuner MIX.	337
2SC2353	VHF TV Tuner MIX.	340
2SC2368	Microwave Low Noise Amplifier	343
2SC2369	Microwave Low Noise Amplifier	345
2SC2407	High Frequency Medium Power Amplifier	347
2SC2408	High Frequency Wideband Amplifier	349
2SC2518	High Speed High Voltage Switching	351
2SC2570A	VHF/UHF Low Noise Amplifier	354
2SC2682	Audio Frequency/High Frequency Power Amplifier	357
2SC2688	Color TV Chroma Output, Video Output	359
2SC2690, 2690A	Audio Frequency/High Frequency Power Amplifier	362
2SC2720	High Speed Switching	364
2SC2749	High Speed High Current Switching	367
2SC2750	High Speed High Current Switching	370
2SC2751	High Speed High Current Switching	373
2SC2752	High Speed High Voltage Switching	376
2SC2784	Audio Frequency Low Noise Amplifier	380
2SC2785	Audio Frequency Amplifier	383
2SC2786	FM Tuner RF Amplifier, MIX., CONV., OSC.	386
2SC2787	AM/FM IF Amplifier, AM CONV., OSC.	390
2SC2901	High Speed Switching	393
2SC2908	High Speed High Current Switching	396

Type No.	Use	Page
2SC3209	High Voltage Audio Frequency Amplifier	399
2SC3355	VHF/UHF Low Noise Amplifier	402
2SC3358	VHF/UHF Low Noise Amplifier	405
2SC3434	High Voltage Ultra High Speed Switching (NEW DEVICE)	408
2SC3435	High Voltage Ultra High Speed Switching (NEW DEVICE)	412
2SC3478, 3478A	High Voltage Audio Frequency Amplifier	416
2SC3531	High Voltage High Speed Switching (NEW DEVICE)	419
2SC3533	High Voltage High Speed Switching (NEW DEVICE)	422
2SC3534	High Voltage High Speed Switching (NEW DEVICE)	426
2SC3535	High Voltage High Speed Switching (NEW DEVICE)	430
2SC3536	High Voltage High Speed Switching (NEW DEVICE)	434
2SC3544	UHF TV Tuner OSC., MIX. (NEW DEVICE)	438
2SC3566	High Speed Switching	442
2SC3567	High Speed Switching	445
2SC3568	High Speed Switching	448
2SC3569	High Speed Switching	451
2SC3570	High Speed Switching	455
2SC3571	High Speed Switching	459
2SC3572	High Speed Switching	463
2SC3573	Ultra High Speed Switching	467
2SC3574	Ultra High Speed Switching	471
2SC3615	High Gain Amplifier	475
2SC3616	High Gain Amplifier	478
2SC3622	High Gain Amplifier	481
2SC3623	High Gain Amplifier	483
2SC3691	High Speed Switching	485
2SC3692	High Speed Switching	489
2SC3693	High Speed Switching	493
2SC3694	High Speed Switching	497
2SC3731	High Speed Switching	501
2SC3732	High Speed Switching	504
2SC3733	High Speed Switching (NEW DEVICE)	507
2SC3840	High Voltage High Speed Switching (NEW DEVICE)	510
2SC3999	High Voltage High Frequency Amplifier (NEW DEVICE)	513
2SC4000	High Voltage High Frequency Amplifier (NEW DEVICE)	515
2SC4001	High Voltage High Frequency Amplifier (NEW DEVICE)	517
2SD471	Audio Frequency Power Amplifier	519
2SD571	Audio Frequency Power Amplifier	522
2SD773	Audio Frequency Power Amplifier	525
2SD774	Audio Frequency Power Amplifier	528

Type No.	Use	Page
2SD794, 794A	Audio Frequency Power Amplifier	531
2SD809 (1)	Audio Frequency Power Amplifier, Low Speed Switching	533
2SD882	Audio Frequency Power Amplifier, Low Speed Switching	535
2SD985, 986	Audio Frequency Power Amplifier, Low Speed Switching	537
2SD987	High Voltage Low Speed Switching	540
2SD1020	Audio Frequency Amplifier	543
2SD1021	Audio Frequency Amplifier	545
2SD1312	Audio Frequency Power Amplifier	547
2SD1481	High Gain Amplifier	550
2SD1491	High Gain Amplifier	552
2SD1513	Audio Frequency Power Amplifier	554
2SD1579	High Gain Amplifier, Low Speed Switching	556
2SD1581	High Gain Amplifier	558
2SD1582	High Gain Amplifier	561
2SD1585	Audio Frequency Power Amplifier (NEW DEVICE)	564
2SD1586	Audio Frequency Power Amplifier (NEW DEVICE)	566
2SD1587	Audio Frequency Power Amplifier (NEW DEVICE)	569
2SD1589	Audio Frequency Power Amplifier, Low Speed Switching	571
2SD1590	Low Speed Switching	574
2SD1591	Low Speed Switching	577
2SD1593	Audio Frequency Amplifier	580
2SD1594	Audio Frequency Amplifier	582
2SD1595	Low Speed Switching	584
2SD1616, 1616A	General Purpose Power Amplifier	587
2SD1617	Medium Speed High Current Switching	589
2SD1630	High Gain Amplifier	591
2SD1691	Audio Frequency Power Amplifier	593
2SD1692	High Gain Power Amplifier/Switching	595
2SD1693	High Gain Power Amplifier/Switching	597
2SD1694	High Gain Power Amplifier/Switching	599
2SD1697	High Gain Power Amplifier/Switching (NEW DEVICE)	601
2SD1698	High Gain Power Amplifier/Switching (NEW DEVICE)	603
2SD1700	High Gain Power Amplifier/Switching (NEW DEVICE)	605
2SD1701	High Gain Power Amplifier/Switching (NEW DEVICE)	607
2SD1779	High Gain Power Amplifier/Switching (NEW DEVICE)	609
2SD1780	High Gain Power Amplifier/Switching (NEW DEVICE)	611
2SD1818	High Speed Switching, Low V_{CE} (sat) (NEW DEVICE)	613
2SD1843	High Gain Power Amplifier/Switching (NEW DEVICE)	616
2SD1939	High Gain Power Amplifier/Switching (NEW DEVICE)	618
2SJ44	Audio Frequency Low Noise Amplifier	620

Type No.	Use	Page
2SJ45	Audio Frequency Low Noise Amplifier	622
2SK49	FM Tuner RF Amplifier	624
2SK68A	Audio Frequency Low Noise Amplifier	627
2SK104	General Purpose Amplifier	630
2SK105	General Purpose Amplifier	633
2SK162	Audio Frequency Low Noise Amplifier	636
2SK163	Audio Frequency Low Noise Amplifier	638
2SK193	FM Tuner RF Amplifier	640
2SK194	Audio Frequency Low Noise Differential Amplifier	642
2SK195	FM Tuner Low Noise Amplifier	644
2SK505	VIDEO Frequency Amplifier	646
2SK507	VIDEO Frequency Amplifier	648
2SK518	AM Tuner RF Amplifier	650
2SK519	AM Tuner RF Amplifier	652
2SK514	General Purpose Amplifier	654
2SK523	Audio Frequency Amplifier	657
2SK533	Audio Frequency Low Noise Amplifier	659
2SK540	Audio Frequency Amplifier (NEW DEVICE)	661
2SK591	Power Switching (NEW DEVICE)	663
2SK659	Power Switching (NEW DEVICE)	666
2SK679	Power Switching (NEW DEVICE)	669
2SK681	Power Switching (NEW DEVICE)	672
2SK699	Power Switching (NEW DEVICE)	675
2SK700	Power Switching (NEW DEVICE)	678
2SK701	Power Switching (NEW DEVICE)	681
2SK702	Power Switching (NEW DEVICE)	684
2SK703	Power Switching (NEW DEVICE)	687
2SK704	Power Switching (NEW DEVICE)	690
2SK705	Power Switching (NEW DEVICE)	693
2SK736	Power Switching (NEW DEVICE)	696
2SK737	Power Switching (NEW DEVICE)	699
2SK773	High Voltage Power Switching (NEW DEVICE)	702
2SK774	High Voltage Power Switching (NEW DEVICE)	705
2SK799	High Voltage Power Switching (NEW DEVICE)	708
2SK800	High Voltage Power Switching (NEW DEVICE)	711
3SK74	VHF TV Tuner RF Amplifier	714
3SK87	UHF TV Tuner RF Amplifier (DISCONTINUED)	717
3SK87A	UHF TV Tuner RF Amplifier (NEW DEVICE)	720
3SK88	UHF TV Tuner RF Amplifier (DISCONTINUED)	724

Type No.	Use	Page
3SK88A	UHF TV Tuner RF Amplifier (NEW DEVICE)	727
3SK122	VHF TV Tuner RF Amplifier	731
3SK123A	UHF TV Tuner RF Amplifier (NEW DEVICE)	734
3SK124	UHF TV Tuner RF Amplifier (NEW DEVICE)	738
3SK161A	UHF TV Tuner RF Amplifier (NEW DEVICE)	742
μPA68H	Audio Frequency Low Noise Differential Amplifier	746
μPA74HA	Audio Frequency Low Noise Differential Amplifier	748
μPA75HA	Audio Frequency Differential Amplifier	751
μPA76HA	Audio Frequency Low Noise Differential Amplifier	754
μPA77HA	Audio Frequency Differential Amplifier	756
AA1L4M	Medium Speed Switching	758
AA1F4M	Medium Speed Switching	760
AA1A4M	Medium Speed Switching	762
AA1A4P	Medium Speed Switching	764
AA1F4N	Medium Speed Switching	766
AA1L4L	Medium Speed Switching	768
AA1L3Z	Medium Speed Switching	770
AN1L4M	Medium Speed Switching	772
AN1F4M	Medium Speed Switching	774
AN1A4M	Medium Speed Switching	776
AN1A4P	Medium Speed Switching	778
AN1F4N	Medium Speed Switching	780
AN1L4L	Medium Speed Switching	782
AN1L3Z	Medium Speed Switching	784
BA1L4M	Medium Speed Switching	786
BA1F4M	Medium Speed Switching	788
BA1A4M	Medium Speed Switching	790
BA1A4P	Medium Speed Switching	792
BA1F4N	Medium Speed Switching	794
BA1L4L	Medium Speed Switching	796
BA1L3Z	Medium Speed Switching	798
BN1L4M	Medium Speed Switching	800
BN1F4M	Medium Speed Switching	802
BN1A4M	Medium Speed Switching	804
BN1A4P	Medium Speed Switching	806
BN1F4N	Medium Speed Switching	808

Type No.	Use	Page
BN1L4L	Medium Speed Switching	810
BN1L3Z	Medium Speed Switching	812
JE5400	High Voltage Audio Frequency Amplifier	814
JE5401	High Voltage Audio Frequency Amplifier	816
JE5550	High Voltage Audio Frequency Amplifier	818
JE5551	High Voltage Audio Frequency Amplifier	820
JE7001	VHF/UHF TV Tuner OSC., VHF MIX.	822
JE8050	Audio Frequency Power Amplifier	825
JE8550	Audio Frequency Power Amplifier	828
JE9011	AM/FM IF Amplifier, AM CONV., OSC.	831
JE9012	Audio Frequency Amplifier	834
JE9013	Audio Frequency Amplifier	837
JE9014	Audio Frequency Amplifier	840
JE9015	Audio Frequency Amplifier	843
JE9016	FM Tuner RF Amplifier, MIX., CONV., OSC.	846
JE9018	VHF/UHF TV Tuner OSC.	849
JE9042	High Voltage Audio Frequency Amplifier	851
JE9043	High Voltage Audio Frequency Amplifier	854
JE9092	High Voltage Audio Frequency Amplifier	856
JE9093	High Voltage Audio Frequency Amplifier	859
JE9112	Audio Frequency Power Amplifier	861
JE9113	Audio Frequency Power Amplifier	864
JE9123	High Gain Amplifier	867
JE9133	High Gain Amplifier	870
JE9143	High Gain Amplifier	873
JE9153	High Gain Amplifier	876
JE9214	Medium Speed Switching	879
JE9215	Medium Speed Switching	883
2N3903	General Purpose Amplifier/Switching	887
2N3904	General Purpose Amplifier/Switching	891
2N3905	General Purpose Amplifier/Switching	895
2N3906	General Purpose Amplifier/Switching	899
2N4123	General Purpose Amplifier/Switching	903
2N4124	General Purpose Amplifier/Switching	907
2N4125	General Purpose Amplifier/Switching	911
2N4126	General Purpose Amplifier/Switching	915
2N4400	General Purpose Amplifier/Switching	919
2N4401	General Purpose Amplifier/Switching	923
2N4402	General Purpose Amplifier/Switching	927

Type No.	Use	Page
2N4403	General Purpose Amplifier/Switching	931
NT2222	General Purpose Amplifier/High Speed Medium Power Switching	935
NT2222A	General Purpose Amplifier/High Speed Medium Power Switching	939
NT2369	High Speed Switching	943
NT2369A	High Speed Switching	946
NT2907	General Purpose Amplifier/High Speed Medium Power Switching	949
NT2907A	General Purpose Amplifier/High Speed Medium Power Switching	953
1S953	High Speed Switching	957
1S954	High Speed Switching	957
1S955	High Speed Switching	957
1S2207 (B)	VHF/UHF Band AFC	960
1S2208 (B)	UHF Band Tuning	962
1S2209 (B)	VHF Band Tuning	962
1S2222	VHF/UHF Band Electronic Tuner, VHF Band Low-High Ch., Switch	964
1SS16	UHF TV Tuner MIX.	966
1SS43	UHF Band Modulator	968
1SS53	Detector, Medium Speed Switching	970
1SS54	Detector, Medium Speed Switching	970
1SS55	Detector, Medium Speed Switching	970
1SS97	UHF Band MIX.	972
1SS98	UHF Band Detector, MIX.	974
1SS99	UHF Band Detector, MIX.	976
1SS101	UHF Band MIX.	978
1SS103	VHF/UHF Band Electronic Tuner, VHF Band Low-High Ch., Switch	980
1SS202, 202 (1)	High Speed Switching	982
1SS203	High Speed Switching	982
1SS204	High Speed Switching	982
1SS205	Detector, Medium Speed Switching	985
1SS206	Detector, Medium Speed Switching	985
1SS207	Detector, Medium Speed Switching	985
1SS229	High Speed Switching Double Diode	987
1SS230	High Speed Switching Double Diode	987
1SS231	High Speed Switching Double Diode	989
1SS232	High Speed Switching Double Diode	989
1SS233	High Speed Switching Double Diode	991
1SS234	High Speed Switching Double Diode	991
1SS235	High Speed Switching Double Diode	993
1SS236	High Speed Switching Double Diode	993
1SS237, 237 (1)	UHF Band Detector, MIX.	995

Type No.	Use	Page
1SV34	Variable Attenuator	997
1SV50, 50 (1)	FM Radio/VHF TV Tuner Tuning	1000
1SV50S	FM Radio/VHF TV Tuner Tuning	1002
1SV80	VHF/UHF TV Tuner Variable Attenuator	1004
1SV88	VHF/CATV Tuner Tuning	1006
1SV156	VHF/UHF TV Tuner Variable Attenuator	1008
1SV157	VHF/UHF TV Tuner Variable Attenuator	1010
1SV175	UHF Band Tuning (NEW DEVICE)	1012
1SV176	UHF Band Tuning (NEW DEVICE)	1014
1SV183	UHF Band Tuning (NEW DEVICE)	1016
1SV184	VHF Band Tuning (NEW DEVICE)	1018
1SV190	VHF Band Tuning (NEW DEVICE)	1020
1SV208	VHF Band Tuning (NEW DEVICE)	1022
1SZ45A	Constant Voltage	1024
1SZ46A	Constant Voltage	1024
1SZ47A	Constant Voltage	1024
1SZ47	Constant Voltage	1024
1SZ48	Constant Voltage	1024
1SZ50	Constant Voltage	1026
1SZ51	Constant Voltage	1026
1SZ52	Constant Voltage	1026
1SZ53	Constant Voltage	1026
ND487C1-3R	VHF/UHF Double Balanced Modulator	1028
ND487C2-3R	VHF/UHF Double Balanced Modulator	1030
ND487R1-3R	VHF/UHF Double Balanced Modulator	1032
ND487R2-3R	VHF/UHF Double Balanced Modulator	1034
ND587R-3R	VHF/UHF Double Balanced Mixer (NEW DEVICE)	1036
ND587T-3R	VHF/UHF Single Balanced Mixer (NEW DEVICE)	1038
RD2.0E ~RD200E	Constant Voltage, Constant Current, Clipper, Limiter, Surge Clipper	1040
RD2.0F ~RD82F	Constant Voltage, Constant Current, Clipper, Limiter, Surge Clipper	1054
RD4.7JS ~RD39JS	Constant Voltage, Constant Current, Clipper, Limiter	1061
RD2.0ES ~RD39ES	Constant Voltage, Constant Current, Limiter, Surge Clipper	1066
RD8.2EW,9.1EW	Constant Voltage, Constant Current, Limiter, Surge Clipper	1072

Type No.	Use	Page
BZY88-C2V7 ~BZY88-C33	Constant Voltage, Constant Current, Clipper, Limiter, Surge Clipper	1074
SD113	FM Radio/AFC	1078
SD115	FM Radio/AFC	1078
SD116	FM Radio/AFC	1078
SD117	FM Radio/AFC	1078

GENERAL PURPOSE INFORMATIONS

QUICK REFERENCE GUIDE FOR PLASTIC MOLDED TRANSISTORS 3

NEC SEMICONDUCTORS 9

SEMICONDUCTOR STANDARDS 15

TECHNICAL SYMBOLS USED IN NEC'S SEMICONDUCTOR DEVICES 38

RELIABILITY AND QUALITY ASSURANCE SYSTEM OF NEC'S SEMICONDUCTOR DEVICES 43

PACKAGE DIMENSIONS AND STRUCTURES 71

QUICK REFERENCE GUIDE FOR PLASTIC MOLDED TRANSISTORS

FOR PORTABLE RADIO & STEREO TUNER DEVICES

Application	SST Mold Type No.	EIAJ Standard Type No.		NEC Original Type No.	Diode
		Transistor	FET		
FM RF Amp.	2SK193 2SC2786	2SA1005 2SC1674	2SK49 2SK195	JE9016	
FM MIX., CONV.	2SC2786	2SC1674		JE9016	
FM OSC.	2SC2786 2SC2787	2SC1674 2SC1675		JE7001 JE9016 JE9018	
AM CONV., OSC.	2SC2787	2SC1675 2SC2000	2SK104	JE9011	
AM/FM IF Amp.	2SC2787	2SC1675	2SK104	JE9011	
VIDEO Amp.			2SK505 2SK507		
Tuning Di FM					1SV50(1)
Tuning Di AM					
AFC Di					1SV50S SD115 1S2207(B) SD116 SD113 SD117
AGC Di					1SV80
AF Low Noise Amp.	2SA1174 2SA1410 2SC2784	2SA990 2SA991 2SA992 2SC1842 2SC1843 2SC1844 2SC1845	2SK68A 2SK162 2SK163 2SK194 2SK523 2SJ44 2SJ45	μPA68H μPA74HA μPA75HA	
AF Amp.	2SA1175 2SC2785 2SC3623/A	2SA733 2SA987 2SA988 2SA1409 2SC923 2SC945 2SC945Ⓛ 2SC1840 2SC1841 2SC2000 2SC3622/A	2SK105 2SK514	JE9014 JE9015 JE9023 JE9033 JE9043 μPA76HA μPA77HA	
AF DRIV.	2SB810 2SB811 2SD1020 2SD1021	2SA915 2SA916 2SA952 2SA953 2SA954 2SC1940 2SC1941 2SC2001 2SC2002 2SC2003 2SC3209		JE9012 JE9013	
Power Amp.	2SB811 2SD1021	2SB564 2SB605 2SB733 2SB734 2SB984 2SD471 2SD571 2SD773 2SD774 2SD1312		JE8050 JE8550 JE9112 JE9113	

FOR TV TUNER DEVICES

APPLICATION		TYPE No.	
		EIAJ STANDARD	NEC ORIGINAL
RF AMP.	VHF	3SK74 3SK122 2SC606(B) 2SC1393	
	UHF	3SK87A 3SK88A 3SK123A 3SK124 3SK161	
MIX.	VHF	2SC605(B) 2SC1394 2SC1730 2SC2352	JE7001 JE9018
	UHF	2SC1070(1) 2SC1070(2) 2SC2353 2SC3544 1SS16 ND547R-3R ND547T-3R	
OSC.	VHF	2SC287A(B) 2SC1730	JE7001 JE9018
	UHF	2SC288A(5-B) 2SC1730	JE7001 JE9018
TUNING Di	VHF	1SV50 1SV50(1) 1S2209(B) 1SV184 1SV190 1SV208	
	UHF	1S2208(B) 1SV175 1SV176 1SV183	
AFC Di (VHF/UHF)		1SV50S 1S2207(B)	
BAND SW Di (VHF/UHF)		1S2222 1SS103	
AGC Di (VHF/UHF)		1SV80 1SV156 1SV157	

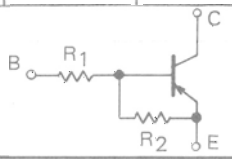
FOR SWITCHING DEVICES

APPLICATION		SWITCHING TIME (t_{rr} or t_{stg})			
		~ 3 ns	~ 13 ns	~ 100 ns	~ 225 ns
SWITCHING DIODE		1S953 1S954 1S955 1SS202 1SS202(1) 1SS203 1SS204		1SS53 1SS54 1SS55 1SS205 1SS206 1SS207	
10 mA SWITCH	PNP		2SA1206 (~ 40 ns) 2SA1459 (~ 40 ns)		2N3905 2SA1153 2N3906 2SA1458 2N4125 2N4126
	NPN		2SC2901 2SC3732 NT2369 NT2369A		2N3903 2SC2720 2N3904 2SC3731 2N4123 2N4124
150 mA SWITCH	PNP			NT2907 NT2907A	2N4402 2N4403
	NPN				NT2222 NT2222A 2N4400 2N4401
500 mA SWITCH	PNP			2SA1460	
	NPN			2SC3733	

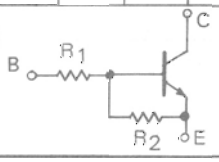
RESISTOR BUILT-IN TRANSISTORS

T0-92 (EIAJ Standard Type No.)		SST Mold Type No.		NEC Original Type No.		R_1	R_2	V_{CEO}	I_C
PNP	NPN	PNP	NPN	PNP	NPN	[kΩ]	[kΩ]	[V]	[mA]
AN1L4M	AA1L4M	BN1L4M	BA1L4M	JE9215 RANK C	JE9214 RANK C	47	47	(NPN)	(NPN)
AN1F4M	AA1F4M	BN1F4M	BA1F4M	JE9215 RANK B	JE9214 RANK B	22	22	50	100
AN1A4M	AA1A4M	BN1A4M	BA1A4M	JE9215 RANK A	JE9214 RANK A	10	10	(PNP) −50	(PNP) −100
AN1A4P	AA1A4P	BN1A4P	BA1A4P			10	47		
AN1F4N	AA1F4N	BN1F4N	BA1F4N			22	47		
AN1L4L	AA1L4L	BN1L4L	BA1L4L			47	22		
AN1L3Z	AA1L3Z	BN1L3Z	BA1L3Z			4.7	–		

(equivalent circuit) (PNP)



(NPN)

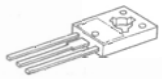
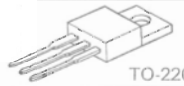
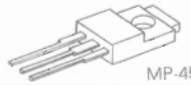
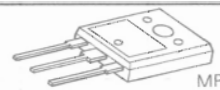


QUICK REFERENCE TABLE FOR PLASTIC MOLDED TRANSISTORS

PACKAGE / V_{CEO}, V_{DSX} (V) / I_C, I_D (A)	DISK MOLD			SST MOLD		TO-92 (EIAJ STANDARD TYPE NO.)								SP MOLD			TO-92 (NEC ORIGINAL TYPE NO.)						7Pin Sip
	15 (14)	20	30 (25)	30 (25)	60 (50)	12 (10)	15 (14)	20 (18)	30 (25)	40 (35)	50	80 (60)	160 (120)	25 (16)	50	160 (120)	20 (15)	25	30	40	45	60 (50)	80 (60)
~10 m				(20 V) 2SK193 2SK540				2SK49 2SK195															
~20 m	2SC287A(B) 2SC288A(B)		2SC605(B) 2SC606(B)	(20 V) 2SC2786	2SK514			2SC1674	2SK104 2SC1393 2SC1394		2SK68A 2SK106												
~30 m		3SK122 3SK74* 3SK87A 3SK88A 3SK123A 3SK161		2SC2787				2SC2352	2SC1675	2SJ44 2SJ45 2SA1005	2SK163 2SK523						JE9016		JE9011				μPA68H Package 7 pin SIP
~50 m	2SC2368 2SC2353			(15 V) 2SA1459	2SA1174 2SC2784 2SK507	2SC3544	2SA1206 2SC1730 2SC2026 2SC2037 2SK505			2SK162 2SK194			2SA988 2SA992 2SC1841 2SC1845 2SA639(S) 2SC1279(S)			2SA915 2SA916 2SC1940 2SC1941	JE7001 JE9018							μPA74HA μPA75HA μPA76HA μPA77HA
~80 m	3SK124					2SC2737 2SC2869																	
~0.1	(12 V) 2SC2369				2SA1175 2SC2785	2SC2670A				2SA987 2SC923 2SC1840 2SC1842	2SA733 2SA990 2SC945 2SC945Q 2SC1843 2SC2000	2SA991 2SC1844	(180 V) 2SA1376 2SC3476 (200 V) 2SA1376A 2SC3476A (250 V) 2SA1544 2SC3999			(250 V) 2SA1546 2SC4000					JE9014 JE9015		
~0.2	(12 V) 2SC3358			2SA1410 (15 V) 2SC3732	(40 V) 2SA1458 2SC3623 (40 V) 2SC3731	2SC3355	2SC2901		2SA1409		2SC3622					(300 V) 2SC3209	NT2369 NT2368A	2N4124 2N4126	2N4123 2N4125	2N3903 2N3904 2N3905 2N3906			
~0.3							2SC1280(S)*	2SC2402 2SC2408	2SC1280A(S)*			2SA953 2SA954 2SC2002 2SC2003						JE9133						
~0.5									2SK679	2SA1153 2SC2720							JE9012 JE9013							
~0.6																				NT2907 2N4400 2N4401 2N4402 2N4403		NT2907A	
~0.7				2SB810 2SD1020					2SA952 2SC2001									JE9123					
~0.8												2SD1698* 2SD1701*			(60 V) 2SD1700* 2SB605 2SD571 (80 V) 2SD1697*					NT2222	NT2222A		
~1.0				2SB811 2SD1021										2SB564 2SD471 2SK679	2SD1843* 2SB734 2SD774 2SD1582* 2SC3733								
~1.5												2SD1939						JE8050 JE8550 JE9112 JE9113					
~2.0							(16 V) 2SB1068 2SD1613							2SB733 2SD773 2SD1681	(80 V) 2SB984 2SD1312 2SB1093* 2SD1579* 2SD1779 2SD1780			JE9143					

*Darlington Transistor

QUICK REFERENCE TABLE FOR PLASTIC MOLDED POWER TRANSISTORS

V_{CEO} (V) / $I_{C(DC)}$ (A)	 TO-126 (MP-5)						 TO-220			 MP-45			 MP-80		
	~60	~120	~160	~180	~400	~600	~350	~400	800	~60	100	~400	100	400	800
~0.5				2SA1142 2SC2682	2SA1156 2SA1546 2SC2568 2SC2688 2SC2752 2SC4001										
~1.0	2SB731 2SD809(1) 2SD1630*	2SB795* 2SD986*			2SC3840	2SA1546									
~2.0	2SB794* 2SD985* 2SD1491*	2SA1220 2SC2690	2SA1220A 2SC2690A				2SA1009	2SA1009A 2SC2334			2SA1395	2SB1096 2SC3569 2SD1587			
~3.0	2SD1694 2SB744A 2SD794A 2SB772 2SD882 2SB1150* 2SD1693*	2SB1149* 2SD1692*							2SC3531	2SB1094 2SD1593 2SD1585 2SD1818	2SC3567				2SC3533
~5.0	2SB1151 2SD1691							2SC2518 2SD987		2SA1394 2SC3566 2SD1595* 2SA1441 2SC3691	2SB1098* 2SB1095 2SD1586 2SD1589*	2SC3570 2SC3573	2SC2908		2SC3534
~7.0								2SC2335		2SA1442 2SC3692	2SD1594	2SC3571 2SC3574			2SC3535
~8.0											2SB1099* 2SD1590*				2SC3536
~10										2SA1443 2SC3693	2SA1396 2SB1100* 2SC3568 2SD1591*	2SC3572		2SC2749 2SC3434	
~15										2SA1444 2SC3694			2SC2750	2SC2751 2SC3435	

* Darlington

QUICK REFERENCE TABLE FOR PLASTIC MOLDED POWER MOSFET

$I_{D(DC)}$ (A) \ V_{DSS} (V)	TO-92	SP MOLD	TO-126 (MP-5)			TO-220 (MP-25)		MP-45		MP-80	
	30	30	60	80	100	60	100	60	100	450	500
0.5	2SK679* (0.5 Ω)										
1		2SK681* (0.5 Ω)									
2			2SK701* (0.4 Ω)	2SK700* (0.6 Ω)	2SK701* (0.8 Ω)						
5						2SK704* (0.12 Ω)	2SK702* (0.2 Ω)	2SK705* (0.12 Ω)	2SK703 (0.2 Ω)		
12								2SK659* (0.05 Ω)	2SK737* (0.1 Ω)	2SK799 (0.4 Ω)	2SK773 (0.47 Ω)
15								2SK591* (0.035 Ω)	2SK736* (0.08 Ω)		
18										2SK800 (0.32 Ω)	2SK774 (0.35 Ω)
20											
25											

* : 4 V-Gate Driven Power MOSFET On-Resistance: Typical Value

NEC SEMICONDUCTORS

The development of NEC semiconductor electronic components has its beginning in the copper oxide rectifiers ventured in 1928, which were followed by the development of selenium rectifiers, microwave silicon diodes, and glass sealed mini-type diodes. And, in 1956 several types of germanium transistors were commercialized.

At this time, several high reliability types had already been established for communication and industrial use.

Since then, efforts for the advancement and improvement of semiconductors have been exerted on the following points:

(a) Improvement of high frequency characteristics.
(b) Increase of power handling capacity.
(c) Increase of reliability.
(d) Lowering of cost.

In pursuit of the above aims, from early times our company perceived the value of silicon and advanced research along this line. In 1959, our company announced the production of super-grown silicon transistors for communication and industrial use. This was followed by the manufacture of superior products by the introduction of planar and epitaxial techniques and the providing of an abundant series of products.

Though, recently, there are semiconductors which employ material of the GaAs family, nearly all of the principal products of our company employ silicon. Application in the high frequency field of these semiconductors extends to several GHz, and power transistors of 200 W power handling capacity have been commercialized.

In addition to the silicon planar process, semiconductor surface passivation and packaging techniques unique to our company have been established resulting in remarkable improvement of reliability. Ultrahigh reliability products for use in underseas cables, rocket borne equipment, electronic exchange equipment, microwave repeaters, etc. have been realized, and the techniques for making these products have been widely adopted for communication, industrial, and domestic products.

On the other hand, with the improvement and advance of characteristics, efforts have paid to rapidly lower the cost of products and progress has been made in the realization of more better products at a more lower price. What should be noted in particular is that the completion of a micro-disk transistor production line in 1963 enabled silicon transistors, which up to that time could only be produced at the price of communication or industrial use transistors, to be supplied at a price competitive with germanium transistors for use in such domestic equipment as radio and television sets. This caused the transistors used in domestic equipment to be largely changed to silicon transistors, and can be said to have formed the basis of the coming IC age.

1. KINDS OF SEMICONDUCTOR PRODUCTS MANUFACTURED BY NEC.

In order to answer to the widesread needs of our customers, our company markets an extremely numerous variety of semiconductor products. When roughly classified, these are as follows:

DIODES

* Germanium diodes (point contact type, gold bonded type).
* Silicon diodes (point contact type, Schotty barrier type, epitaxial-planar type).
* PIN diodes (for modulation and switching).
* Snap-off diodes (for switching, waveform shaping, and frequency multiplication).
* Varactor diodes (for frequency multiplication, tuning, AFC, and parametric amplification).
* Gunn diodes (for microwave oscillation).
* Impatt diodes (for microwave oscillation).
* Zener diodes.
* Varistor diodes.
* Trigger diodes (for thyristor trigger).

TRANSISTORS.

* Junction type transistors (alloy, base diffusion, planar, epitaxial-planar, mesa, epitaxial, and triple diffusion types).
* Junction type field effect transistors.
* MOS type field effect transistors.
* GaAs schottky barrier type field effect transistors.

OPTICAL APPLICATIONS

* Light emitting diodes.
* Phototransistors, photodiodes.
* Photocouplers, photointerrupters.
* Numeral display elements.
* Symbol display elements.
* Solar cells.

RECTIFIERS & THYRISTORS

* Silicon rectifying elements.
* Rectifier stacks.
* Thyristors.
* Thyristor gate elements, gate ICs.

Among the above, when the transistors are classified in more detail they become as follows:

- Signal transistors for communication and industrial use.
- Power transistors for communication and industrial use.
- Transistors for microwave use.
- High frequency high power transistors.
- Mini-mold transistors.
- Molded transistors.
- Micro-disk transistors.
- Power transistors for general domestic equipment.
- Junction type field effect transistors.
- MOS type field effect transistors.
  [N channel depletion type
  P channel enhancement type
  N channel dual gate type]
- Composite elements.
  Junction type transistors:
  [Dual, triple, and quad NPN; dual PNP.]
  MOS type transistors:
  [N channel dual; P channel dual.]

2. NOMENCLATURE OF SEMICONDUCTORS

JIS nomenclature.

Among semiconductor products, the nomenclature of transistors, diodes, rectifier elements, and thyristors is established by JIS-C-7012 of the Japanese Industrial Standards. This system if called the JIS nomenclature, but since the business of registering the name and specification of these semiconductors is handled by the Electronic Industries Association of Japan it is sometimes referred to as the EIAJ nomenclature. The JIS nomenclature is composed of the following characters and numerals, arranged in a manner so that the polarity and outline of the use of the product can be known.

1st term	2nd term	3rd term	4th term	5th term
numeral	character	character	numeral	character

The 1st Term Numeral.

0 is used for the numeral of the 1st term, for photo-transistors, photodiodes and composite elements including such diodes and transistors. In other elements, when the number of effective electrodes is n, the number n-1 is used for the numeral of the 1st term. That is to say, for a 2 electrode elements such as a diode 1, for a 3 electrode transistor 2, and for a 4 electrode transistor 3 is used. In the case of composite elements, the element with the most numerous electrodes is taken and, similarly to the above, when the number of electrodes of this element is n the numeral of the 1st term shall be n-1.

In the above case, since shield lead wires and 2 or more lead wires coming from the same electrode are not counted as effective electrodes, the number of effective electrodes and the number of lead wires may not necessarily be the same.

The 2nd Term Character.

S is employed, in order to indicate that the product is a semiconductor.

The 3rd Term Character.

This character is deleted, when the 1st term numeral is 0 or 1.

When the numeral of the 1st term is one or more, in order to make the polarity and outline characteristics of the element known, one of the following characters is used for the 3rd term.

A . . . . . High frequency PNP transistors.
B . . . . . Low frequency PNP transistors.
C . . . . . High frequency NPN transistors.
D . . . . . Low frequency NPN transistors.
E . . . . . Esaki diodes.
F . . . . . Thyristors.
G . . . . . Gunn diodes.
H . . . . . Single junction transistors.
J . . . . . P channel field effect transistors.
K . . . . . N channel field effect transistors.
M . . . . . Bidirectional thyristors.
Q . . . . . Light emitting diodes.
R . . . . . Rectifying dioces.
S . . . . . Small signal dicdes.
T . . . . . Avalanche conduction diodes.
V . . . . . Variable capac ty diodes, PIN diodes, Snap-off diodes.
Z . . . . . Zener diodes.

However, in the case of diodes some products still remain that have been registered under the old system, in which the 3rd term character is deleted and the type name is in the form of 1SOO.

The 4th Term Numeral.

A number which is attached in accordance with the order of registration, that starts at 11.

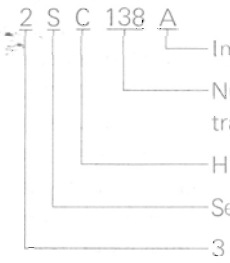
The 5th Term Character.

This character indicates improvements from the original form. This character is not attached to the original form, but is attached to improved models employing the capital letters A, B, C, D, E, F, G, H, J, K of the alphabet in the order of the improvements. In the case improvements are made, the improved model shall be compatible with the preceding model, though compatibility in the opposite direction is not necessarily

required.

In the case of diodes, when the letter M is used for the 5th term it indicates that the element is a matching couple, and when R is used that the polarity is reversed while the exterior and electrical characteristics are the same.

[Example]



In addition to the above, with no bearing on the JIS nomenclature, a character or number in ( ) is sometimes used as a 6th term to indicate that the specification is that of a specific customer.

Ⓝ . . . NHK standard type (example : 2SC594Ⓝ)
M. . . . Defense Agency Maritime General Staff approved (example : 2SC68-M)
Ⓢ. . . . One of the several Ⓢseries types established for industrial measurement (example : 2SD188Ⓢ)
(numerals) . . .Established for specific customers or applications. Attached sequentially from (1) in order of establishment. (example : 2SC653(1), 1S306(3))

JEDEC Nomenclature.

Some transistors and diodes employ the JEDEC nomenclature. This a nomenclature adopted by the EIA (Electronic Industries Association of America), and is called the JEDEC nomenclature or EIA nomenclature.

The composition of numerals and characters of the JEDEC nomenclature is approximately the same as that of the JIS nomenclature, except that the character N is used for the 2nd term and there is no classification by a 3rd term character.

Examples of JEDEC nomenclature are shown below.

Example of a transistor : 2N5762
Example of a diode : 1N23G

Semiconductors bearing JEDEC nomenclature exist because, giving consideration to interchangeability with American products, the original American manufacturer's specification and nomenclature were adopted without change when such semiconductors were first produced, or after commercialization such semiconductors became widely popular and the JEDEC nomenclature has been continued to be used.

NEC's original Nomenclature.

Some diodes and optical semiconductor elements employ a nomenclature original to NEC. This nomenclature consists of a prefix of 2 or 3 alphabet characters followed by a numeral and character. As shown in the table, the prefix indicates the use and structure of the element.

NEC Nomenclature

Prefix	Use & Structure	Product example
AD	Impatt diode	AD611
GD	Gunn diode	GD408A
GH	Germanium mixer diode	GH1D
PH	Phototransistor	PH201A
PS	Photocoupler, photointerrupter	PS2001
RD	Zener diode	RD2.0E
SD	Small signal diode	SD13
SE	Infrared light emitting diode	SE301A
SG	Green light emitting diode	SG203D
SH	Point contact type silicon diode	SH5A
SM	Schotty barrier type GaAs mixer diode	SM153
SR	Red light emitting diode	SR103D
SY	Amber color light emitting diode	SY403D
SV	Silicon varactor diode	SV87D

3. SIGNAL TRANSISTORS FOR DOMESTIC EQUIPMENT.

Signal transistors for domestic equipment have been designed for use in radios, transceivers, television sets, tape recorders, audio stereo equipment, etc., and can be classified into the following product groups according to their packaging.

* Disk-molded transistors.
* Plastic molded transistors.
* Metallic case transistors.

The product groups have been designed to meet various individual applications, and will display high performance when selected appropriately for the purpose.

Disk-Molded Transistors.

Disk-molded transistors have been developed, by fully utilizing the superior high frequency characteristics (such as low interline capacitance and lead inductance) of conventional microdisk transistors, for supplying products of low price and high quality. Furthermore, they can substitute conventional microdisk counterparts. For UHF band, types 2SC1070(B) for RF stage, 2SC2353 for mixing stage, and 2SC288A(5•B) are available. For VHF band, a dual-gate MOSFET 3SK74 of superior high gain and low noise is available for RF stage as well as other types for various uses.

Plastic Molded Transistors.

Plastic molded transistors are transistors which are sealed employing epoxy or silicone type plastics in place

of the metallic cases used formerly. Through the automation of production lines and the lowering of material costs, they are mass produced at low cost and, today, almost all domestic equipment use these transistors in large quantities.

At present, according to their manufacturing method plastic molded transistors are roughly divided into the following kinds.

* Transfer method.
* Casting method.
* E-pack method.
* Potting method.

Among the above, at first our company undertook production employing the E-pack and casting methods, however, with the aim of improving productivity and reliability, the transfer method has been adopted today. The transfer method consists of assembling the semiconductor element on a so-called lead frame, which corresponds to the stem of a metallic case, and then molding the semiconductor to shape by forcing the plastic under pressure into a metal mold. In performing this method, giving consideration to the effect that the plastic will have on the electrical characteristics, humidity resistance, flame retardancy, and other internal elements of the semiconductor, our company employs an epoxy plastic of selected quality.

In general, the failure mode of plastic molded transistors will differ as a matter of course from that of hermetic sealed transistors. The greatest difference is in humidity resistance. Humidity resistance depends greatly upon the quality of the plastic, absorption of moisture by the plastic will bring about an increase in leakage current, and when the moisture reaches the internal elements the characteristics of transistors will be degraded and in extreme cases will cause open circuits due to the melting of electrodes of the elements. In the transfer method of our company, because the plastic is injected under pressure to be molded the density of the plastic is high and, also, the hygroscopicity of the plastic itself is superior to that of other methods. However, in order to facilitate manufacture it is necessary to make the parting of the plastic and metal mold good, therefore attention must be paid to the adhesion between the leads and plastic. In regards to this point, epoxy which has superior adhesion to metal among plastics has been adopted, and humidity resistance is ascertained by performing the following tests.

(1) Pressure cooker test. (125 °C at 2 to 3 atmos.)
(2) Boiling test. (100 °C)
(3) High temperature high humidity storage. (60 °C, 95 %)

In addition, since in regards to flame retardancy a high reliability flame retardant plastic that satisfies UL standards has been adopted, these transistors may be used with reassurance.

Plastic molded signal transistors for domestic equipment are sealed in either EIAJ Form SC-43 (JEDEC Form TO-92) or semipower type packages. Product series of these transistors are provided in an abundant variety including NPN and PNP types and FETs, which cover all uses from UHF band oscillators to low frequency output (P_T = 600 ~ 800 mW) enabling kits to be made up for use in nearly all domestic equipment. In addition to the above, as a special type, ultra small size mini-mold type transistors have been commercialized. These mini-mold type transistors are unique products of our company which were first developed in Japan for use in hybrid ICs, and recently they have begun to be used in large quantities in place of transistors employing conventional chips. Product series of mini-mold transistors are provided in a complete line of NPN and PNP type transistors, FETs, and diodes for such uses as UHF – HF band amplification, switching, low frequency amplification, and output. This enables their application to a wide variety of hybrid ICs and small equipment.

Plastic Molded Power Transistors

Our high voltage, high speed switching and darlington power transistor series have been designed for use in switching regulators, DC-DC converters and power amplifiers, etc. They are sealed with epoxy resin mold are mechanically compatible with TO-220 types anc are precisely molded from top to bottom with new epoxy resin that features higher thermal conductivity. They make the mounting manhours much less by eliminating insulation sheets and washers. And they permit higher density mounting by providing superior insulation from nearby devices.

4. FIELD EFFECT TRANSISTORS. (FETs)

FETs are elements having an operating mechanism, similar to vacuum tubes, of voltage controlling the majority carrier. According to the kind of composition of the electrode (gate) exercising the voltage control, FETs are divided into junction (J FETs), Schotty barrier (SB FETs), and MOS (MOS FETs) types.

FETs have many features such as high input impedance, low noise, low distortion, good intermodulation and AGC characteristics and, in addition, since they are majority carrier elements they are basically suited as high frequency, high speed elements. MOS FETs of both N and P channel types have been commercialized, with I_{DS}–V_{GS} characteristics of either the enhancement or depletion type. Suitable combinations of these FETs perform important logical functions, and form the basic elements of MOS ICs.

According to their use, the product series of single unit FETs are compiled into those for signal, audio, and

microwave use. MOS FETs or J FETs are employed for signal or audio use, and GaAs SB FETs have been adopted for microwave use.

Signal Field Effect Transistors.

Signal FETs were first developed to provide characteristics that could not possibly be realized by bipolar transistors, such as the high input impedance and low noise characteristics desired by the instrumentation field and the wideband, low distortion and noise characteristics desired by the communication field. However, with the lowering of manufacturing costs, the features of signal FETs begun to be utilized in domestic equipment, and at present products for use in domestic equipment have became more numerous.

Communication and industrial signal FETs are of a high reliability design that employs metallic cases and, in addition to a strict quality assurance system, through the improvement of characteristics the life cycle of the products have been extended permitting long term continuous production.

The first signal FET developed for domestic use was the micro-disk 2SK37 announced in 1969. Following this, the development of products to meet various uses was continued and, recently, the recognition of the merit that due to their characteristics circuit components can be economized together with the lowering of costs has caused these FETs to be used in large quantities. Today, signal FETs of the MOS type for UHF and VHF use to junction types for audio use are being manufactured. In particular, in the case of junction type FETs the gate structure has been made into a mesh form to attain high g_m. Furthermore, through the completion of a set-up to supply these FETs at low cost by mass production, still more efforts are being made to popularize these FETs.

5. DIODES

Diodes, though being bi-terminal elements of the simplest configuration among semiconductor devices, have been diversified in use and structure and a lot of types of them are produced. Here, descriptions will be given of mass-produced diodes of conventional types other than those for special purposes. These diodes are classified by their usages as follows: switching, detecting, maintaining constant voltage or rectifying, and mixing diodes, as well as variable capacitance diodes having rather wide range of use.

Switching diode is one of types which are produced in the largest quantity. This diode can be commonly used not only for switching in logical circuits that require rather small power and in core drivers with several hundreds milliamperes but also for detecting and rectifying. Both germanium and silicon series are available, but, for economical and stability reasons, germanium diodes are regarded as types for repairment/types to be discarded and silicon diodes will be the main stream.

These silicon diodes undergo the diffusion of gold during chip processing for killing lifetime, thus they have faster switching speed, particularly for reverse recovery time (t_{rr}), by 1 or 2 orders than ordinary products and they have improved forward rise-up characteristics, too. The commonly used structure is so-called DHD (Double Heatsink Diode) which provides heat sinks on both sides of chip and sealed with glass. In spite of the small size, this structure allows large power consumption which results in a high reliability in cooperation with the stabilization processing given to the chip surface. In addition, various special switching diodes are produced, including line switcher diodes with very low series resistance and interterminal capacitance and level shifter diodes with increased forward voltage by means of stacked chips.

Mixing diode is principally used in mixer of TV UHF tuner. Since, in this use, the circuitries work frequently on direct conversion systems, the diodes are designed paying attentions to noise characteristics, strength against pulsive breakdown and conversion loss, and the inner capacitances of diode are reduced as far as possible in order to avoid any possible trouble when diodes are mounted on the tuners. Their structures may be classified into point contact and Shottky barrier types. Recently, the series of production type are the Shottky barrier types because of their advantage in noise characteristics, pulse breakdown strength and anti-shock feature.

Variable capacitance diode is used in reverse voltage application. Therefore, unlike detector diodes where forward characteristics are essential, the substantial characteristics of this diode is reverse characteristics. The important points in the design of the diode are inner capacitance variation ratio, reverse current, and reverse inner resistance when reverse voltage is applied. For consumer use, the diodes are chiefly used in TV tuners and FM tuners. Being used in tuning circuits at high frequencies, and their Q valves being of much importance, much care is taken of the mold material of the diodes. Because the necessary capacitance and capacitance variation ratio depend on the circuit that uses the diode, a variety of types are available that suit to the usages.

When the diode is used in a circuit, the reverse voltage is applied through a high resistance that also serves as a by-pass, and even a slight amount of reverse current may influence the characteristics because of the voltage drop

across the high resistance. Therefore the diodes are designed to have structure that can suppress reverse current and temporal variation as much as possible.

Zener diode is used in voltage regulator and other circuits for constant voltage, constant current, clipper, clamp and surge clipper. In the NEC, zener diode chip, the peripheral portion of the P-N junction has a double diffusion structure. One junction is main junction and the other junction is guard ring. Guard ring is diffused borde of main junciton for stabilized silicon surface. Therefore, the current-voltage characteristic of zener diode has a sharp transition potential and a flat current plateau above breakdown. The breakdown is not destructure, however, unless the power dissipation is allowed to increase the temperature to the point where local melting destroys the semiconductor.

6. CAUTION ON TREATMENT

The semiconductor devices listed in this data book were all designed under sufficiently minute scrutiny, and manufactured under perfect quality control. However, in order to preserve all the characteristics and the best use of them over a long period of time the following care should be observed upon the treatment. Also, for further details on what listed here refer to technical application notes.

ON DESIGNING

Firstly, it is important to select semiconductor devices whose rating can adequately afford great allowance for the estimated voltage, current, and temperature condition, etc. The greater the allowance the more chances of failure can be avoided when using. For components requiring higher reliability, it is advisable that industrial used devices for that purpose be used.

ON TEST AND INSPECTION

Pay attention to noise caused by inspection machines on transistors and diodes for small signal use, and on ultra-high frequency devices. In particular, the entering of voltage surge from commercial supply may result in destruction or deteriorating characteristics of devices.
Great care is also required as failure may occur on high frequency devices by applying reverse voltage.

ON TRANSPORTATION AND STORAGE

Semiconductor devices should be housed in near room temperature, dry places, if possible, as surroundings of high temperature and high humidity are not suitable for them. Field effect transistors and Schottky barrier diodes are also needed protection against static electricity. As these are carefully packed in alluminum foil, the same care should be taken in handling them prior to installing in the device.

ON MANUFACTURING PROCESS TREATMENT

It is of particular importance to preserve the reliability of semiconductor devices in treatments during the manufacturing process. In short, mechanical, thermal, electrical, and chemical stresses should not be allowed to apply to them if possible. Following are listed the major cautions.

- **Installing:** Bending or forcedly pulling transistors and diodes from the bases of their leads may result in the deprivation of airtightness or in deterioration of characteristics.
  Great care is needed when designing the lead forming and the printed-circuit board so that stress on the lead will not remain after the hermetically sealded glass package diodes have been installed.
- **Soldering:** Flux of rosinous nature is suited. Inorganic fluxes, such as zinc chloride, are considered poisonous. In general, make sure to perform the soldering over 1.5 mm distant from the base of the lead, and have it done in a shortest possible. Care is also required as warp caused by solder on the printed-circuit board may give stress to the components.
  It is under the condition that there will be no electrical leakage from the soldering iron and the soldering bath. In particular, for field effect transistors and ultra-high frequency devices, take care that perfect grounding of soldering tools is performed.
  The use of lead-cutter may also cause harmful effects on semiconductor devices.
- **Supersonic cleaning and the like:** Be sure that the printed-circuit board with semiconductor devices installed on is cleaned with well-selected solvents. The surface of plastic molded devices can be deformed by trichloroethylene or acetone. Carefully select the frequency and output in such a way that the bonding wire between components as well as the mounting parts are not affected when performing the recent widely-used supersonic cleaning method. It is also advisable that the sandblast, which is used for the same cleaning purpose, be avoided as it can damage the hermetically sealded glass package diodes.

Above is a brief description of the general cautions. It is needless to say that great attention must be paid on many other details, which have not been listed above as they are considered commonsensical, when handling semiconductor devices. Also, for further information on each individual semiconductor device, refer to technical application notes or contact us directly.

SEMICONDUCTOR STANDARDS

1. ABSOLUTE MAXIMUM RATINGS

The ratings which are applied to semiconductor products are called Absolute Maximum Ratings and are defined as "The limiting values that must not be exceeded under any usage or testing conditions, and no two or more of these values must not be applied at the same time."

Absolute maximum ratings are given for voltage, current, power, and temperature, and are specified for continuous DC conditions at a temperature of 25 °C. However, recently pulse ratings have begun to be specified.

VOLTAGE RATINGS

Voltage ratings imply the maximum reverse voltage that may be applied between two electrodes, and is specified for the following items.

1) Diodes

- Peak reverse voltage V_{RM}:

  The peak value of the inverse voltage that may be applied. It is limited by the electron avalanche breakdown voltage.

- DC reverse voltage V_R:

  The reverse voltage that may be applied continuously. Usually, the inverse leakage current is specified at this voltage.

2) Transistors

- Collector-base voltage V_{CBO}:

  The reverse voltage between the collector and base, when the emitter is kept open. Limited by the electron avalanche breakdown voltage of the collector-base junction. Electron avalanche breakdown occurs when a field of over 10^5 V/cm is applied to a PN junction. The carrier multiplication factor of the breakdown is given by the following formula.

$$M = \frac{1}{1 - (V/V_B)^m}$$

  V: Voltage applied to the PN junction.

  V_B: Electron avalanche breakdown voltage.

  m: A constant determined from experience, in regards to which the relationship shown in Table 1 has been obtained.

Table 1

Material	N* type	P* type
Ge	m=3	m=6
Si	m=4	m=8

* The type of which V_B is to be determined is taken. (The type having higher specific resistance)

- Emitter-base voltage V_{EBO}:

  The reverse voltage between the emitter and base, when the collector is kept open. Limited by the electron avalanche breakdown or zener breakdown of the emitter-base junction.

- Collector-emitter voltage V_{CEO}:

  Reverse voltage between the collector and emitter, when the base is kept open. Determined from the V_{CBO} and h_{FE}.

$$V_{CEO} = \frac{V_{CBO}}{\sqrt[m]{1 + h_{FE}}}$$

  m: Refer to the paragraph on V_{CBO}

- Collector-emitter voltage V_{CER}:

  The reverse voltage between the collector and emitter when the base and emitter are connected together with a resistor. Determined by BV_{CBO} and R_{BE}.

$$V_{CER} = V_{CBO} \sqrt[m]{1 - \frac{I_{CBO}(r_b + R_{BE})}{V_{TF}}}$$

  V_{TF}: The forward threshold voltage between the base and emitter. About 0.5 V for Si.

- Collector-emitter voltage V_{CES}:

  The reverse voltage between the collector and emitter, when the base and emitter are shorted together ($R_{BE} = 0$).

$$V_{CES} = V_{CBO} \sqrt[m]{1 - \frac{I_{CBO} \cdot r_b}{V_{TF}}} \approx V_{CBO}$$

- Collector-emitter voltage V_{CEX}:

  The reverse voltage between the collector and emitter, when the base-emitter is reverse biased through a resistor.

$$V_{CEX} = V_{CBO} \sqrt[m]{1 - \frac{I_{CBO}(r_b + R_{BE})}{V_{TF} + V_{BB}}}$$

- Collector-emitter voltage V_{CEC}:

  The reverse voltage between the collector and emitter, when the base-emitter is reverse biased ($R_{BE} = 0$).

$$V_{CEV} = V_{CB} \sqrt[m]{1 - \frac{I_{CBO} \cdot r_b}{V_{TF} + V_{BB}}} \approx V_{CBO}$$

  Generally, this is expressed as V_{CEX}.
The relationship between these ratings is, generally, $V_{CBO} \approx V_{CEV} \approx V_{CES} > V_{CER} > V_{CEO}$ and when shown as voltage-current characteristics have the relationship shown in Fig. 1.

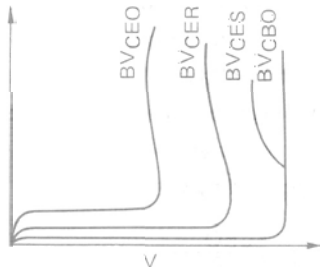


Fig. 1 Relationship of Collector Withstanding Voltages.

3) Field Effect Transistors (FETs)

- Gate-source voltage V_{GSS}:

  The voltage between the gate and source, when the drain and source are shorted. This voltage is limited by the electron avalanche breakdown in junction type FETs, and by the breakdown voltage of the gate insulating film in insulated gate type FETs. In FETs, since the gate input impedance is extremely high breakdown may occur even from static electricity, therefore great care should be exercised in their handling.

- Gate-source voltage V_{GSO}:

  The voltage between the gate and source, when the drain is kept open.

- Gate-drain voltage V_{GDS}:

  The voltage between the gate and drain, when the source and drain are shorted together. Applicable to junction type FETs only. Limited by the electron avalanche breakdown of the gate-drain junction.

- Drain-source voltage V_{DSS}:

  The voltage between the drain and source, when the gate and source are shorted together. Applicable to insulated gate type FETs only. Limited by the drain-substrate junction electron avalanche breakdown.

- Drain-source voltage V_{DSX}:

  The voltage between the drain and source, when a cutoff voltage is applied between the gate and source.

CURRENT RATINGS

Current ratings mean the maximum current that can be passed through any electrode. Current ratings are determined by either the electrical characteristics of the device, or the current carrying capacity of the internal connecting wires or the lead wires of the package.

1) Diodes

- Peak current I_{FM}:

  Limited by the power rating. Current up to this value may be repeatly passed through the device.

- Average rectified current I_O:

  The average value of the forward current, when a sine wave is rectified. DC current of this value may be passed continuously.

- Surge current $I_{F(surge)}$:

  The current that may be instantaneously passed within a specified time.

2) Transistors

- Collector current I_C:

  Hitherto, the definition of the collector current rating has been somewhat obscure. However, in the 6th Semiconductor Technical Committee of EIAJ of 1972, on the premise that the collector current should be considered from the standpoint of initial assurance of the absolute maximum ratings, a tentative opinion of the definition of the collector current was obtained as shown in Table 2. Therefore, our company specifies the collector current in accordance with this opinion.

- Base current I_B :

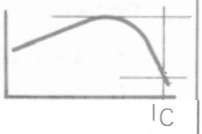
  Generally, this current is not specified (It is inevitably determined from the current amplification factor.).

  Base currents at which breakdown will not occur are as follows.

  For low power use ($I_C \leqq 1A$) . . . $I_B \leqq I_C$

  For high power use ($I_C > 1A$) . . . $I_B \leqq 1/2 \cdot I_C$

Table 2

	Interpretation	Supplementary explanation
1. DC collector current	1. Under a condition of T_j less than $T_{jMAX.}$, breakdown or degradation of characteristics shall not occur when $I_C \leqq I_CMAX.$	a) Degradation of characteristics means that the standards for breakdown voltage, h_{FE}, etc. are not satisfied when $I_C \leqq I_{C(pulse)}MAX.$ b) The time that I_C is kept at I_CMAX shall as rule be once for 5 minutes.
	2. The rating value shall be stipulated under either of the following conditions. i) In the current characteristics of h_{FE}, the current at which h_{FE} drops to 1/2 – 1/3 of its peak value. ii) A current at which normal operation is not impeded, due to dropping of the h_{FE}.	a) When the use is for switching, the current shall not be restricted to 1/2 – 1/3 of its peak value. b) The following values shall be used as rough indications for the lower limit of h_{FE}. $h_{FE} = 10$: for medium power. $h_{FE} = 3$: for high power. 
2. Pulse collector current	1. The pulse width and repetition frequency are designated according to the use, then under these conditions and the condition that T_j is less than $T_{jMAX.}$, breakdown or degradation of characteristics shall not occur when $I_C \leqq I_{C(pulse)}MAX.$	a) Characteristic degradation is the same as 1. (1) (a). b) The time that I_C is kept at $I_{C(pulse)}$ MAX shall be adequate for reading the value of the current. c) The pulse width and repetition frequency shall be designated.

3) Field Effect Transistors

- Drain current I_D :

  The current flowing through the drain. Usually, is limited by I_{DSS} in junction types (depletion mode), and by the power rating in insulated gate types. However, it shows the current at which breakdown will not occur, if current should flow due to static electricity or noise.

- Gate current I_G :

  The forward current flowing through the gate-channel junction. Usually, since reverse bias is applied I_G does not flow. However, this is the current at which breakdown will not occur, when forward biasing occurs due to static electricity or noise.

TEMPERATURE RATINGS

The temperatures of the junction region and channel region (T_j and T_{ch}) allowable under operating conditions and the temperature range (T_{stg}) allowable for storage are specified. These temperatures are mainly determined by the materials of the semiconductor and package and assure that the failure rate will be under a certain value (differs according to the manufacturer) when the devices are operated or stored at these temperatures.

POWER RATINGS

Due to the joule's heat generated in diodes or transistors, the temperature of the junction or channel region rises. The sum of this temperature rise and the

ambient temperature signifies the power dissipation reached at the power rating.

1) Diodes

In the case of diodes, generally, the power rating is not specified. Since the major portion of the power dissipated in diodes is in a forward direction, the power rating will be inevitably determined by specifying the forward current.

2) Transistors

The collector power dissipation, P_C, at an ambient temperature of 25 °C (free air), or case temperature of 25 °C (with an infinitely large heat sink), or the total power dissipation, P_T, (sum of collector and emitter power dissipation), is specified.

$$P_C = \frac{Tj - Ta}{R_{th(j\text{-}a)}} \qquad \text{(free air)}$$

$$P_T = \frac{Tj - Ta}{R_{th(j\text{-}c)}} \qquad \text{(with an infinitely large heat sink)}$$

T_a: Ambient temperature, generally taken as 25 °C.

T_C: Case temperature, generally taken as 25 °C.

$R_{th(j\text{-}a)}$: Thermal resistance from junction to surroundings.

$R_{th(j\text{-}c)}$: Thermal resistance from junction to case.

Now, when temperature is considered analogous to electric potential, and thermal resistance analogous to electric resistance, the above relationship can be expressed as shown in Fig. 2.

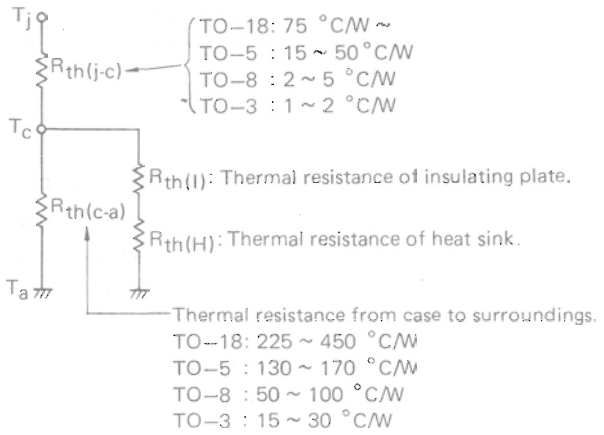


Fig. 2 (a) Relationship of Thermal Resistances.

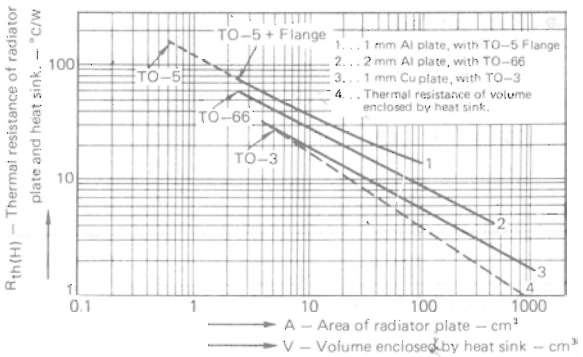


Fig. 2 (b) Relationship of Radiator Plate Area and Thermal Resistance.

3) Field Effect Transistors

The total power dissipation, P_T, is specified.

SAFE OPERATING AREA OF TRANSISTORS.

In the past, breakdown failures of power transistors occurred frequently when they were used in high power amplifiers having widely varying loads, or for the switching of inductive loads such as encountered when driving relays. Since it became known that the cause of these breakdowns was related to secondary breakdown phenomenon, it has become necessary to introduce the concept of the Safe Operating Area as the maximum rating of transistors in place of the classical idea that transistor could be safely operated in the range of $V_{CEMAX.}$, $I_{CMAX.}$, and $P_{TMAX.}$.

1) Secondary breakdown phenomenon.

As shown in Fig. 3, secondary breakdown is the phenomenon in which the voltage-current characteristics move, at a certain voltage and current, to a low impedance region with a speed of several μs or less, when the current is further increased after primary breakdown has occurred. Secondary breakdown differs in the following points from such primary breakdown phenomenon as electron avalanche breakdown.

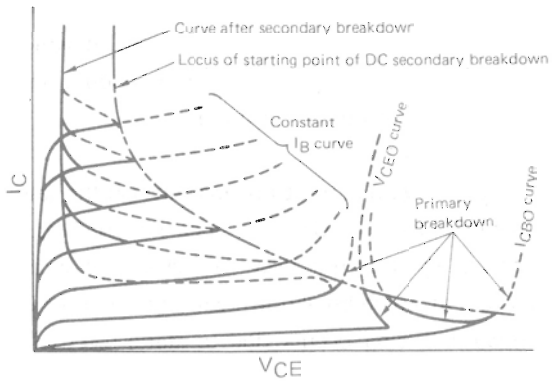
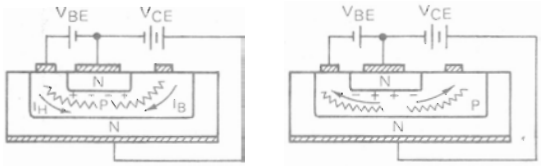


Fig. 3 Primary Breakdown and Secondary Breakdown.

(a) The secondary breakdown voltage shows an extremely low value, compared to BV_{CBO} and BV_{CEO}.

(b) The characteristic of the movement to secondary breakdown is a function of energy, and will change according to V, I, and t. But, as a primary approximation, BV_{CBO} and BV_{CEO} have no relationship with energy. The established theory is that secondary breakdown is caused by local thermal runaway brought about by concentrations of current, which are effected by pinch-in and fringing effects caused by a voltage drop in the transverse direction of the base region, or, defects of the base region, or, non-uniformity of the junction.



Current concentrated in the circumference of the emitter.
(a) Fringing effect (forward bias)

Current concentrated in the center of the emitter
(b) Pinch-in effect (reverse bias)

Fig. 4 Fringing and Pinch-in.

2) Testing method of safe operating area.

Testing methods for the safe operating area of transistors was included for the first time in the EIAJ standard "Transistor Testing Methods" (SD-71, 4th edition), published in November 25, 1969. The above standard contains such testing methods as the latching method, over-the-hill method, transient thermal resistance measuring method, etc. However, since in some testing methods there is a danger of the transistor breaking down, our company employs the transient thermal resistance measuring method. For power transistors, our company conducts 100 % inspection with a pulse width of 200 ms or 10 ms and the specified bias applied. Through this inspection thermally unbalanced transistors and those with faulty chip mounting are completely eliminated.

Next, the transient thermal resistance measuring method shall be described. This method, since secondary breakdown is caused by local thermal runaway brought about by concentration of current, utilizes the fact that when the junction temperature is kept under observation some change will appear when secondary breakdown occurs. The forward voltage of the emitter-base junction, V_{EB}, is observed as a measure of the junction temperature.

In the measuring circuit of Fig. 5, when power is applied by opening and closing SW at the specified pulse width, V_{EB} will become as shown in Fig. 6. V_{EB2} shows that the junction temperature rises due to the power applied, and V_{EB1} shows that the junction temperature drops when the power is removed. Since the temperature coefficient of V_{EB1} will vary according to the current, V_{EB1} is taken as the measure of the junction temperature.
(If the constant emitter current I_F is amply small, then the temperature coefficient of V_{EB}: $\Delta V_{EB}/T = 2$ mV/°C)

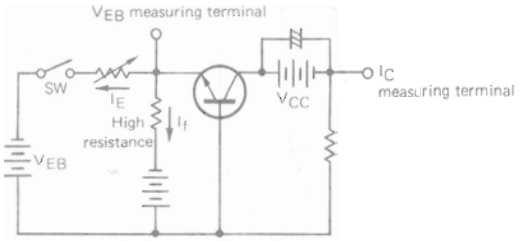


Fig. 5 Transient Thermal Resistance Measuring Circuit.

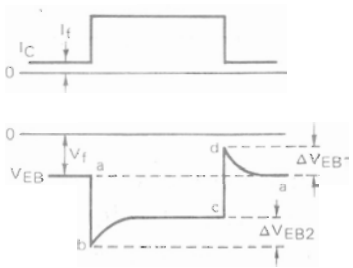


Fig. 6 I_C–V_{EB} Waveforms.

When V_{EB1} is measured, the change in junction temperature and the transient thermal resistance can be determined.

$$\Delta T_j = \frac{\Delta V_{EB1}}{\Delta V_{EB}/\Delta T} \approx \frac{\Delta V_{EB1}(mV)}{2(mV/°C)} \quad (°C)$$

$$\Delta R_{th} = \frac{\Delta T_j}{\Delta P_C} \approx \frac{1}{\Delta P_C(W)} \cdot \frac{\Delta V_{EB1}(mV)}{2\ (mV/°C)} \quad (°C/W)$$

In this method, when the collector current I_C is kept constant and the collector voltage V_{CB} is increased, ΔV_{EB1}, depend on T_j, should rise linearly. However, at high voltages hot spots appear where the junction temperature rises rapidly, as shown in Fig. 8.

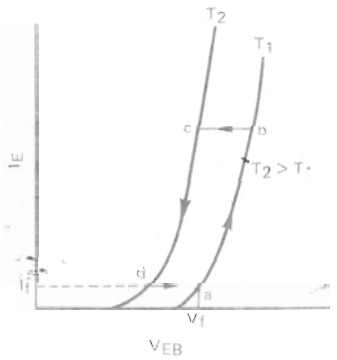


Fig. 7 Input Characteristics

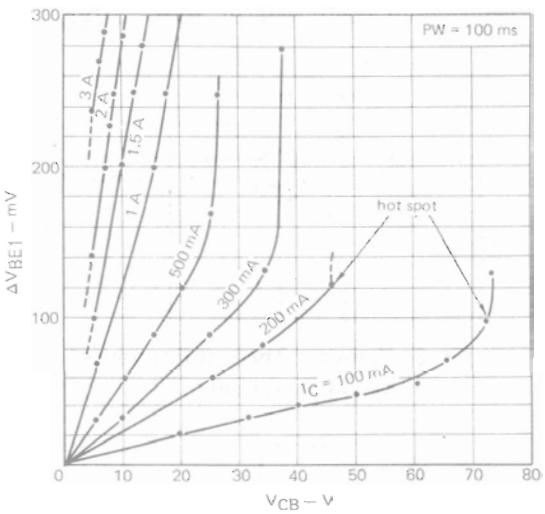


Fig. 8 Dependence of V_{EB1} on Bias.

Hot spots do not appear in low voltage regions, but since V_{EB1} = 300 mV (ΔT_j = 150 °C) corresponds to T_j = 175 °C the safe operating area can be obtained by plotting this point.

In this method, since measurement can be undertaken without making secondary breakdown to occur (hot spots appear as a forerunning phenomenon of secondary breakdown), the safe operating area can be measured without destroying the transistor. Therefore, the safe operating area obtained by this method is narrower than that obtained by the latching or over-the-hill methods.

3) Method of specifying the safe operating area.

Up to the present, our company has specified the safe operating area at the point where V_{EB1} = 300 mV (ΔT_j = 150 °C). This gave a safe operating area smaller than that given by other testing methods. Furthermore, we could not give an exact answer, when inquiries were received from customers as to how the safe operating area would be affected when the ambient temperature (case temperature) or repetition frequency was changed. Therefore, in the future our method of specifying the safe operating area shall be changed as follows.

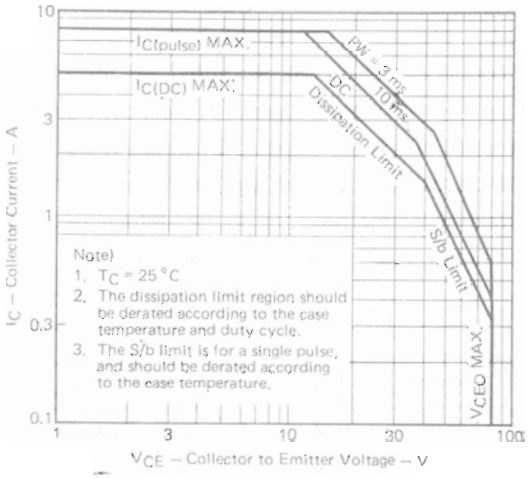


Fig. 9 Example of Safe Operating Area

The safe operating area is specified by 4 elements, as shown in Fig. 9.

* Region I

Current limit.

The region limited by the collector current rating.

* Region II

Dissipation limit.

The region limited by thermal resistance (total dissipation).

Limited by $R_{th(j-c)}$ in the case of DC, and by transient thermal resistance ΔR_{th} such as shown in Fig. 10 in the case of pulses.

Furthermore, when the pulse width is 100 ms, in the majority of packages,

$R_{th(j-c)} = \Delta R_{th(100\ ms)}$

Therefore, unless mentioned otherwise, DC means PW = 100 ms.

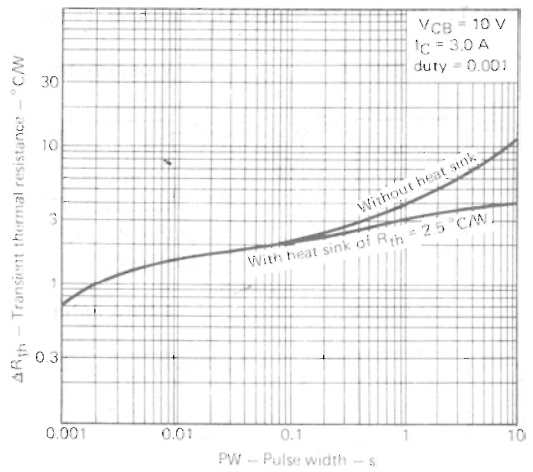


Fig. 10 Example of Transient Thermal Resistance Characteristics.

* Region III

S/b limit.

The region limited by secondary breakdown. The temperature of hot spots is said to be the temperature at which semiconductors become intrinsic (in the case of silicon: 600 °C). The breakdown of transistors is caused by the materials of the electrodes or mounting being melted by this temperature and diffusing into the semiconductor. Among these materials, the solder of the chip mounting has the lowest melting point. Therefore, the S/b limit is specified at the point where the junction reaches the melting point of the mounting solder. Specifically, these points are fixed as follows,

For devices where $T_{jMAX.}$ = 150 °C

—— the point at which V_{EB1} = 400 mV.

(∵ $T_j = \Delta T_j + T_C$ = 225 °C)

For devices where $T_{jMAX.}$ = 175 °C

—— the point at which V_{EB1} = 500 mV.

(∵ $T_j = \Delta T_j + T_C$ = 275 °C)

Furthermore, at the above temperatures the derating factor against junction temperature is taken as zero, as shown in Fig. 11.

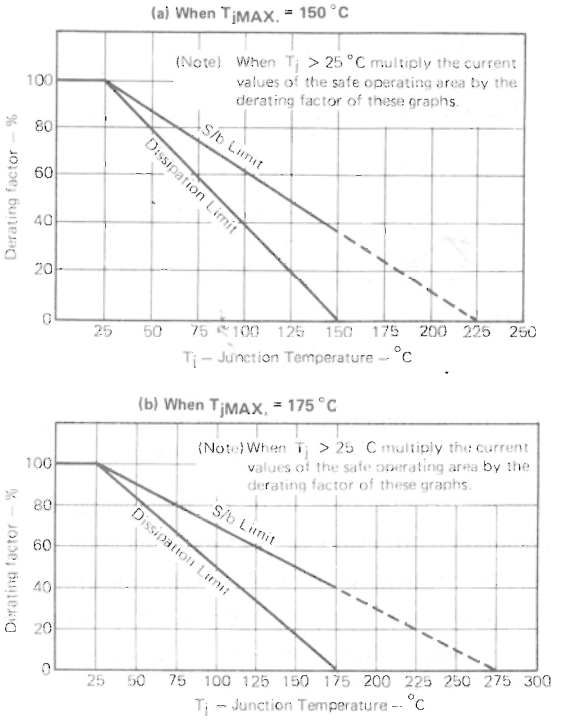


Fig. 11 Derating Curve for Safe Operating Area.

4) Method of utilizing the safe operating area.

Since the safe operating area is specified at a temperature of 25 °C, when the temperature is higher than this it is necessary to derate the safe operating area. In such case, the derating factor for the corresponding temperature is determined from Fig. 11 and the current values of the safe operating area are multiplied by this factor.

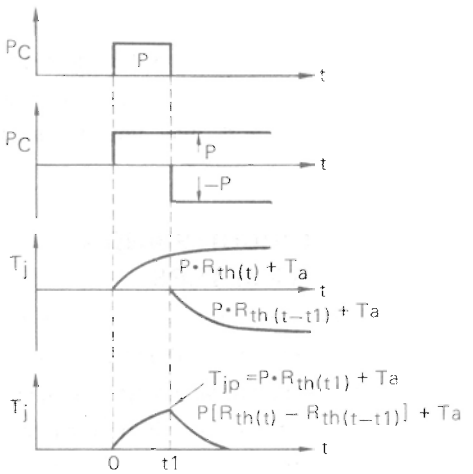
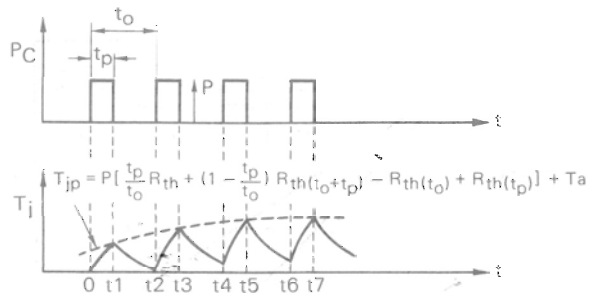


Fig. 12 Calculation of Junction Temperature When Pulse is Applied.



$T_{j(t1)} = P\, R_{th(t1)} + Ta$
$T_{j(t2)} = P\,[R_{th(t2)} - R_{th(t2-t1)}] + Ta$
$T_{j(t3)} = P\,[R_{th(t3)} - R_{th(t3-t1)} + R_{th(t3-t2)}] + Ta$

Fig. 13 Method of Determining Junction Temperature When Power is Repeatly Applied.

When the operating locus of the transistor is the dissipation limit region, surges may be repeatly applied. But, the frequency of application is determined as follows. When pulse power is applied the junction temperature will become as shown in Figs. 12 and 13, and if the peak value T_{jp} of junction temperature is less than the T_jMAX rating of the transistor, power may be repeatly applied.

In the above Figs., $R_{th}(t_1)$, $R_{th}(t_2)$ $\cdots$ $R_{th}(t_o)$, and $R_{th}(t_p)$ are transient thermal resistances determined from charts like Fig. 10.

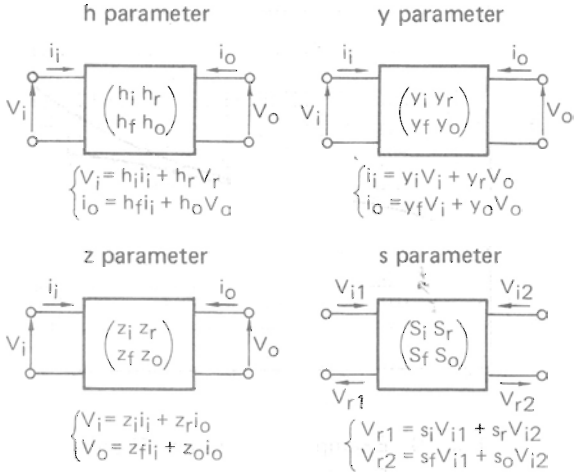
Furthermore, the S/b limit region is specified for single pulses only. Therefore, power may be applied again only after the heat generated by the applied surge has ample time to cool.

In practice, confirming experiments should be conducted with the actual circuit under the worst conditions. For this reason, adequate confirmation experiments are conducted during the development stages of the transistors, which are 100 % screened employing ΔV_{EB} tests and high voltage discharge tests pertaining to TV.

2. EQUIVALENT CIRCUITS AND 4 TERMINAL PARAMETERS

Equivalent circuits are useful for circuit design, since they closely correspond to the physical action of transistors and enable the characteristics to be grasped at a glance, however there are limitations to their application. In order to escape these limitations, the idea has been born to consider transistors as black boxes and express their characteristics as 4 terminal parameters.

DEFINITION OF 4 TERMINAL PARAMETERS



T TYPE EQUIVALENT CIRCUITS

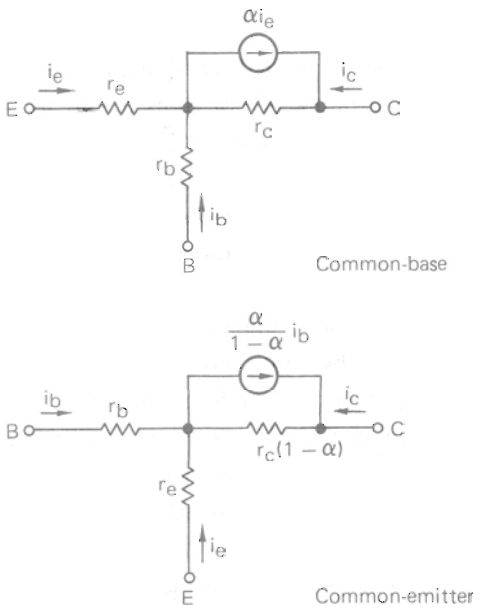


Fig. 14 T type Equivalent Circuits (low frequency)

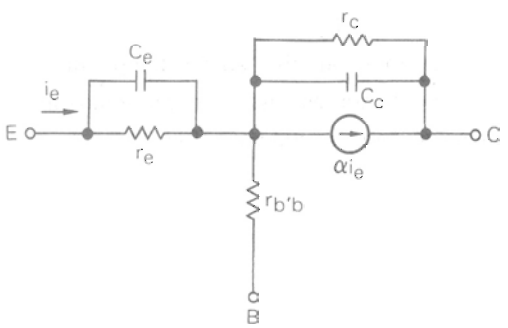
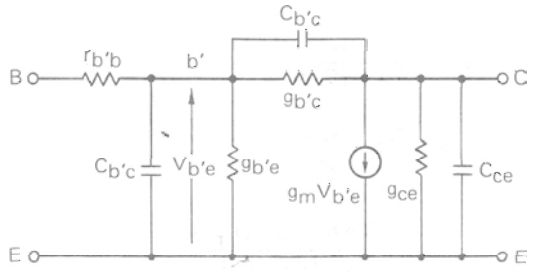


Fig. 15 T type Equivalent Circuit (high frequency)

HYBRID π TYPE EQUIVALENT CIRCUIT



$$g_m = \frac{qI_E}{kT}, \quad g_{b'e} = \frac{g_m}{B_0}$$

$$f_T = \frac{g_m}{2\pi(C_{b'c} + C_{b'e})}, \quad f_\alpha = \frac{g_{b'e}}{2\pi(C_{b'c} + C_{b'e})}$$

Fig. 16

EQUIVALENT CIRCUIT OF MICROWAVE TRANSISTORS

In transistors having a gain-bandwidth product exceeding 1 GHz, parastic elements of the container cannot be disregarded and it is necessary to considered a equivalent circuit such as shown in Fig. 17.

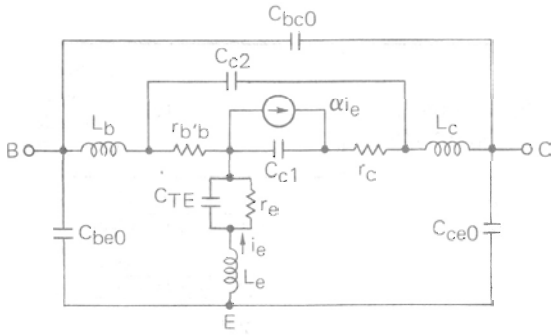


Fig. 17

h parameters

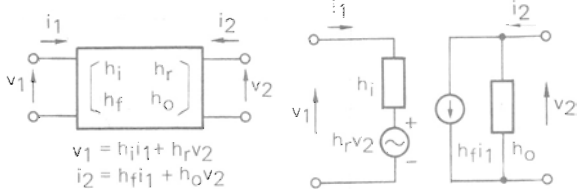


Fig. 18 Expression by h Parameters

Relationship between T type equivalent circuits. (low frequency) and h parameters.

$$\begin{cases} h_{ib} = r_e + (1-\alpha)r_b \\ h_{rb} = \dfrac{b}{r_c} \\ h_{fb} = -\alpha \\ h_{ob} = \dfrac{1}{r_c} \end{cases} \qquad \begin{cases} h_{ie} = r_b + \dfrac{r_e}{1-\alpha} \\ h_{re} = \dfrac{r_e}{(1-\alpha)r_c} \\ h_{fe} = \dfrac{\alpha}{1-\alpha} \\ h_{oe} = \dfrac{1}{(1-\alpha)r_c} \end{cases}$$

y parameters

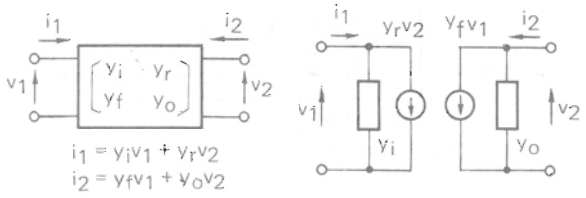


Fig. 19 Expression by y Parameters.

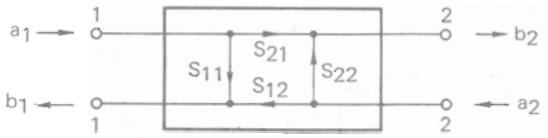
Relationship between T type equivalent circuits (high frequency) and y parameters.

$$\begin{cases} y_{ib} = \dfrac{1 + j\frac{f}{f_\alpha}}{r_e + jr_{b'b}\frac{f}{f_\alpha}} \\ y_{rb} = -2\pi f_\alpha C_c \dfrac{j\frac{f}{f_\alpha}(1 + j\frac{f}{f_\alpha})}{\frac{r_e}{r_{b'b}} + j\frac{f}{f_\alpha}} \\ y_{fb} = -\dfrac{\alpha_0}{r_e + jr_{b'b}\frac{f}{f_\alpha}} \\ y_{ob} = 2\pi f_\alpha C_c \dfrac{j\frac{f}{f_\alpha}(1 + \frac{r_e}{r_{b'b}} + j\frac{f}{f_\alpha})}{\frac{r_e}{r_{b'b}} + j\frac{f}{f_\alpha}} \end{cases}$$

$$\begin{cases} y_{ie} = \dfrac{(1-\alpha_0) + j\frac{f}{f_\alpha}}{r_e + jr_{b'b}\frac{f}{f_\alpha}} \\ y_{re} = -2\pi f_\alpha C_c \dfrac{r_e}{r_{b'b}} \cdot \dfrac{j\frac{f}{f_\alpha}}{\frac{r_e}{r_{b'b}} + j\frac{f}{f_\alpha}} \\ y_{fe} = \dfrac{\alpha_0}{r_e + jr_{b'b}\frac{f}{f_\alpha}} \\ y_{oe} = y_{ob} \end{cases}$$

S parameters

S parameters are mainly employed in microwave bands. These parameters have the advantages that measurement is easy because it is conducted with the input and output terminated with their characteristic impedance and, in addition, these parameters are convenient for the handling of the transfer and reflection of waves.



$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

Fig. 20

$$S_{11} = \frac{b_1}{a_1}/a_2 = 0 \quad : \text{Input reflection coefficient}$$

$$S_{21} = \frac{b_2}{a_1}/a_2 = 0 \quad : \text{Forward transfer coefficient}$$

$$S_{12} = \frac{b_1}{a_2}/a_1 = 0 \quad : \text{Backward transfer coefficient}$$

$$S_{22} = \frac{b_2}{a_2}/a_1 = 0 \quad : \text{Output reflection coefficient}$$

Relationship between equivalent circuit of microwave transistors and S parameters.

$$S_{11e} = \frac{Z_{in} - Z_O}{Z_{in} + Z_O}$$

$$Z_{in} \fallingdotseq (r_{b'b} + r_c + \omega'_T L_e) + j\omega\left\{(L_e + L_b) - \frac{\omega'_T r_e}{\omega^2}\right\}$$

$$\omega'_T = \frac{\omega_T}{1 + \omega_T C_c Z_O}$$

$$|S_{21e}| \fallingdotseq \frac{2Z_O}{R + Z_O}\,\frac{\omega'_T}{\omega}$$

$$R = r_b + r_e + \omega'_T L_e$$

$$|S_{12e}| \fallingdotseq \frac{2Z_O r_e\sqrt{1 + (\omega L_e/r_e)^2}}{(R_{out} + Z_O)(r_{b'b} + r_e + Z_O)}$$

$$R_{out} \fallingdotseq \omega_T/(\omega_T^2 + \omega^2)\cdot C_c$$

$$S_{22e} = \frac{Z_{out} - Z_O}{Z_{out} + Z_O}$$

$$Z_{out} \fallingdotseq \left\{\frac{\omega_T}{(\omega_T^2 + \omega^2)\,C_c} + \frac{L_e}{(r_{b'b} + Z_O)C_c} + r_c\right\} + j\omega\left\{L_e - \frac{1}{(\omega_T^2 + \omega^2)\,C_c}\right\}$$

Table 3 Mutual relationship between S, h, and y parameters.

	[S]	[h] $h_i' = h_i/Z_O$, $h_O' = h_O Z_O$	[y] $y_i' = y_i Z_O$, $y_r' = y_r Z_O$, $y_f' = y_f Z_O$, $y_O' = y_O Z_O$
[S]	S_{11} S_{12} S_{21} S_{22}	$\frac{(h_i' - 1)(1 + h'_O) - h_r h_f}{(1 + h'_i)(1 + h'_O) - h_r h_f}$ $\frac{2h_r}{(1 + h'_i)(1 + h'_O) - h_i h_f}$ $\frac{-2h_f}{(1 + h'_i)(1 + h'_O) - h_r h_f}$ $\frac{(1 + h'_i)(1 - h'_O) + h_r h_f}{(1 + h'_i)(1 + h'_O) - h_r h_f}$	$\frac{(1 - y'_i)(1 + y'_O) + y'_r y'_f}{(1 + y'_i)(1 + y'_O) - y'_r y_f'}$ $\frac{-2y'_r}{(1 + y'_i)(1 + y'_O) - y'_r y'_f}$ $\frac{-2yf'}{(1 + y'_i)(1 + y'_O) - y'_r y_f'}$ $\frac{(1 + y'_i)(1 - y'_O) + y'_r y_f'}{(1 + y'_i)(1 + y'_O) - y'_r y_f'}$
[h]	$\frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}\cdot Z_O$ $\frac{2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$ $\frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$ $\frac{(1 - S_{22})(1 - S_{11}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}/Z_O$	h_i h_r h_f h_O	$\frac{1}{y_i}$ $-\frac{y_r}{y_i}$ $\frac{y_f}{y_i}$ $\frac{y_i y_O - y_r y_f}{y_i}$
[y]	$\frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}/Z_O$ $\frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}/Z_O$ $\frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}/Z_O$ $\frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}/Z_O$	$\frac{1}{h_i}$ $-\frac{h_r}{h_i}$ $\frac{h_f}{h_i}$ $\frac{h_i h_O - h_r h_f}{h_i}$	y_i y_r y_f y_O

Table 4. Conversion of common-emitter and common-base 4 terminal parameters.

Common-base → common-emitter	Common-emitter → common-base
$h_{ie} = \frac{1}{A} \quad (h_{ib})$	$h_{ib} = \frac{1}{B} \quad (h_{ie})$
$h_{re} = \frac{1}{A} \quad (\Delta h_b - h_{rb})$	$h_{rb} = \frac{1}{B} \quad (\Delta h_e - h_{re})$
$h_{fe} = \frac{-1}{A} \quad (h_{fb} + \Delta h_b)$	$h_{fb} = \frac{-1}{B} \quad (h_{fe} + \Delta h_e)$
$h_{oe} = \frac{1}{A} \quad (h_{ob})$	$h_{ob} = \frac{1}{B} \quad (h_{oe})$
$y_{ie} = \Sigma y_b$	$y_{ib} = \Sigma y_e$
$y_{re} = -(y_{rb} + y_{ob})$	$y_{rb} = -(y_{re} + y_{oe})$
$y_{fe} = -(y_{fb} + y_{ob})$	$y_{fb} = -(y_{fe} + y_{oe})$
$y_{oe} = y_{ob}$	$y_{ob} = y_{oe}$
$A = 1 + h_{fb} - h_{rb} + \Delta h_b$	$B = 1 + h_{fe} - h_{re} + \Delta h_e$
$\Delta h_b = h_{ib}h_{ob} - h_{rb}h_{fb}$	$\Delta h_e = h_{ie}h_{oe} - h_{re}h_{fe}$
$\Sigma y_b = y_{ib} + y_{rb} + y_{fb} + y_{ob}$	$\Sigma y_e = y_{ie} + y_{re} + y_{fe} + y_{oe}$

3. SWITCHING CHARACTERISTICS

Generally, when a transistor is employed as a switching element, it assumes one of the states of ON or OFF. In order to be a ideal switch, a transistor should rapidly change the DC resistance between its collector and emitter output terminals from high resistance to low resistance, or vice versa, in response to a very small current injected into its control terminal.

Here, a simple explanation of the large amplitude operation of transistors as switches shall be given.

SWITCHING OF TRANSISTORS

When employing transistors for switching, the common-emitter connection which has large current gain is most widely used. An example of the static output characteristics of this connection is shown in Fig. 21. The operating region of a transistor can be divided into the saturation region, cutoff region and active region. Transistor switching circuits are of the saturated type which employ the two regions of saturation and cutoff, and due to their simple circuit construction and small power consumption are widely used.

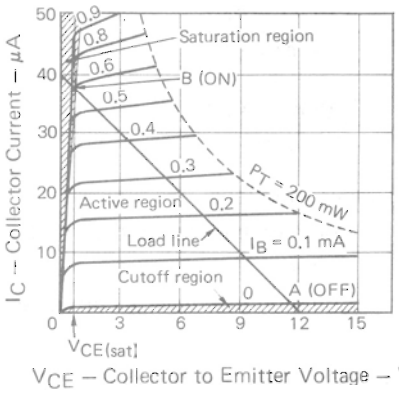


Fig. 21 Static Characteristics of Common-Emitter Output.

Fig. 22 is the basic form of a switching circuit of a common-emitter connected NPN transistor. The collector load line of this circuit is the line AB of Fig. 21. Following, based on Figs. 21 and 22 the operation of transistors in each region shall be described.

1) Cutoff Region (OFF state)

The cutoff region exists when both the emitter and collector junctions are reverse biased. In this state the operating point of the transistor rests at point A of the cutoff region in Fig. 21, the collector current takes a small value, and an extremely high

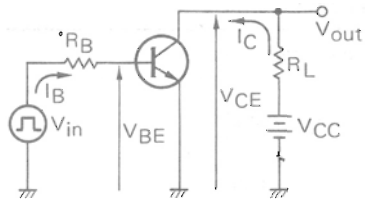


Fig. 22 Basic form of Switching Circuit

resistance is shown between the collector and emitter. That is to say, point A corresponds to a state of a transistor switch with its contacts open (OFF state). The collector current, that is the leakage current, in the OFF state poses a problem for transistor switches, however this current cannot be eliminated completely. According to Ebers' and Moll's analysis, the leakage currents flowing through the collector and emitter, when both junctions are reverse biased, can be expressed by the following formulae.

If $\alpha_I I_{CBO} = \alpha_N I_{EBO}$ is true, then

$$I_C = \frac{I_{CBO}(1-\alpha_N)}{1-\alpha_N\alpha_I}$$

$$I_E = \frac{I_{EBO}(1-\alpha_N)}{1-\alpha_I\alpha_N}$$

in the above equations,

α_N: Common-base forward current amplification factor

α_I: Common-base inverse current amplification factor

Also, the base current is shown as $I_B = I_C + I_E$

that is, $$I_B = \frac{I_{CBO}(1-\alpha_I) + I_{EBO}(1-\alpha_N)}{1-\alpha_N\alpha_I}$$

2) Active Region

The active region, in a state where the emitter junction is forward biased and the collector junction reverse biased, is put to wide general use. In Fig. 22, when the potential of the base is made positive and a base current is made to flow, the operating point of the transistor will move along the load line from point A into the active region, and the speed of transition of the operating point across the active region is determined by the gain-bandwidth product f_T.

3) Saturation region (ON state)

In Fig. 22, when the base potential is made positive and an ample base current ($I_B < I_C/h_{FE}$) is made to flow, the transistor operating point will move along the load line from the active region and reach point B of the saturation region. Then an extremely low resistance will be shown between the collector and emitter, and this corresponds to the closed state (ON state) of the switch. The value of the collector current at point B will be approximately determined by the load resistance and the power supply voltage ($I_C = V_{CC}/R_L$), but the collector-emitter voltage will not drop to zero completely and a certain saturation voltage due to the internal resistance will remain. The collector-emitter saturation voltage is an important parameter of the saturation region, and when analyzed by Ebers' and Moll's model of a transistor, as shown in Fig. 23, becomes as follows.

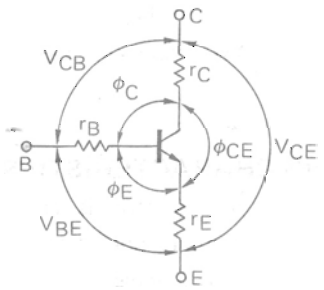


Fig. 23 Model of a Transistor.

$$V_{CE} = \phi_{CE} + r_E I_E + r_C I_C$$

$$\phi_{CE} = \frac{kT}{q} \ln\left(\frac{1}{\alpha_I}\right)\left\{\frac{1+\beta_F(1-\alpha_I)}{1-\beta_F/h_{FE}}\right\}$$

here, kT/q: 26 mV at 27 °C

β_F: Circuit current amplification factor (I_C/I_B) of saturation region.

For reference, the above for the base-emitter junction are given below.

$$V_{BE} = \phi_E + r_B I_B + r_E I_E$$

$$\phi_E = \frac{kT}{q} \ln\left(1 + \frac{I_E - \alpha_I I_C}{I_{CBO}}\right)$$

As has been described, generally, transistor can be utilized as switches by controlling the base. However, as mention they differ from ideal switches in the following points.

* A certain amount of leakage current remains in the OFF state.

* A certain amount of saturation voltage remains in the ON state.
* There is a certain delay in action in respect to the input signal.

TRANSIENT RESPONSE TIME OF TRANSISTORS

In the definition of the switching time of transistors the quantities shown in waveform (C) of Fig. 24, which appears in the output when an input waveform as shown in Fig. 24 (A) is applied to the circuit of Fig. 22, are employed. These quantities are defined as follows.

t_d : Delay time.

The time required, after the input pulse has been applied, for the output current waveform to reach 10 % of its maximum amplitude.

t_r : Rise time.

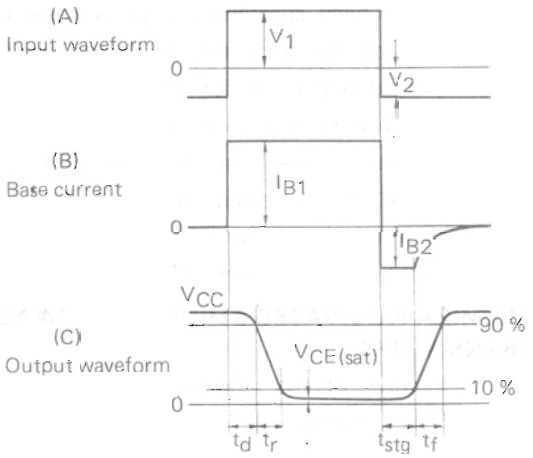
The time required for the output current waveform to increase from 10 % to 90 % of its maximum amplitude.

t_{stg} : Storage time.

The time required, after the input pulse has become zero, for the output current waveform to drop to 90 % of its maximum amplitude.

t_f : Fall time.

The time required for the output current waveform to drop from 90 % to 10 % of its maximum amplitude.



(Note) Since in the above chart the output is shown in voltage waveforms, the positions of 10 % and 90 % maximum amplitude are in inverse relationship to those mentioned in the definitions.

Fig. 24 Switching Waveforms.

Besides the above definitions, the 2 following expressions are frequently used.

t_{on}: turn-on time $t_{on} = t_d + t_r$

t_{off}: turn-off time $t_{off} = t_{stg} + t_f$

ANALYSIS OF SWITCHING TIME BY THE ELECTRON CHARGE CONTROL THEORY.

Here, the electron charge control method shall be described, in which the transistor is considered not as a current controlling element but as a electron charge controlling element and the transient response is expressed by the quantity of the electron charge contained in the base.

Simply stated, this method consists of, when a transistor changes from one state to another, finding the difference of the electron charge contained by the transistor in these two states and calculating the time required for charging this difference of charge ΔQ by current I as $t = \Delta Q/I$.

Methods for calculating the various switching times employing the electron charge control method shall be explained following.

1) Delay Time

The emitter-collector junction capacity and stray capacity of a transistor in an OFF state are charged so as to reverse bias both the collector and emitter junctions. The delay time is the time required to supply a charge to these junctions and make the emitter junction barely forward biased.

When the base current is of step form, this can be simply expressed as follows.

$$t_d = \frac{Q_{OB}}{I_{B1}}$$

here,

Q_{OB} : The electron charge stored in both the emitter and collector junctions.

I_{B1} : Turn-on base current.

$$Q_{OB} = \int_{V_{OB}}^{V_{TF}} C_{1d} dV_{BE} + \int_{V_1 + V_{OB}}^{V_1 - V_{TF}} C_{ob} dV_{CB}$$

here,

V_{OB} : Reverse voltage applied between base and emitter during OFF state.

V_{TF} : Threshold voltage between base and emitter.

V_1 : Voltage between collector and emitter during OFF state.

The voltage increment across the capacitor is ($V_{TF} - V_{OB}$). If this change is linear, the delay time can be expressed by the following formula.

$$t_d = \frac{(V_{TF} - V_{OB})(C_{ib} + C_{ob})}{I_{B1}}$$

2) Rise Time

In order to turn-on a transistor the following electron charges must be supplied: charge Q_1 for creating a carrier gradient within the base region in order to make the required collector current flow, Q_V for changing the voltage of the collector capacity from the OFF level, at which injection of the carrier starts, to the new level, and Q_R which is required for recombination.

Therefore, the equation for input current I_{B1} becomes,

$I_{B1} \cdot t_2 = Q_1 + Q_V + Q_R$

If, by amply over driving, I_C is considered to change linearly, then,

$$Q_R = \frac{t_r \cdot I_C}{2h_{FE}}$$

In addition, since Q_1 and Q_V can be expressed as follows and the rise time is defined at the 90 % point, when these are solved for t_r, t_r can be expressed as follows.

$$Q_1 = \frac{I_C}{2\pi f_T}$$

$$Q_V = C_f \cdot \Delta V_{CB}, \quad \Delta V_{CB} = C_f \cdot I_C \cdot R_C$$

$$\therefore t_r = \frac{0.9 I_C \left(\frac{1}{2\pi f_T} + C_f \cdot R_C\right)}{I_{B1} - \frac{I_C}{2h_{FE}}}$$

here, C_f: Collector-base feedback capacity.
R_C: Thevenin's equivalent load resistance.

3) Storage Time

When a transistor is in the saturation region, due to the minority carrier in the base region, an excessive charge Q_x will be created. The quantity of this charge, with τ_x as the proportional constant, is proportional to the excessive base current I_{Bx}. Furthermore, the charge which recombines is divided into two, one being charge Q_{Rx} which is due to the recombination of the excessive carrier having a lifetime of τ_x. and the other being charge Q_{Ra} that has a lifetime τ_a and is due to the recombination of the activation carrier necessary to maintain the collector current. When the reverse base current I_{B2} is stepped, then,

$$-I_{B2} \cdot t_{stg} = -Q_x + Q_{Rx} + Q_{Ra}$$

$$Q_{Ra} = \frac{t_s \cdot I_C}{h_{FE}}, \quad Q_{Rx} = \frac{I_{Bx} \cdot t_s}{2}$$

$$Q_x = I_{Bx} \cdot \tau_x, \quad I_{Bx} = I_{B1} - I_C/h_{FE}$$

$$t_{stg} = \tau_x \frac{I_{B1} - I_C/h_{FE}}{I_{B2} + \frac{I_{B1} + I_C/h_{FE}}{2}}$$

Furthermore, in recent transistors of the mesa or planar type, the minority carrier of the collector region rather than the base region becomes dominant and various modifications of the t_{stg} formula become necessary.

4) Fall Time

The fall time is calculated using the same reasoning as that followed for the rise time, and is expressed by the following formula.

$$t_f = \frac{0.9 I_C \left(\frac{1}{2\pi f_T} + R_C \cdot C_f\right)}{I_{B2} + I_C/h_{FE}}$$

4. NOISE CHARACTERISTICS

There have been spectacular improvements in the performance of low frequency low noise transistors being employed in audio equipment.

Here, the low noise bipolar transistors of alumina passivated structure and the mesh gate FETs of our company shall be explained. And, in addition, the equivalent input noise source method which is extremely effective in circuit design shall be described.

ALUMINA PASSIVATED STRUCTURE LOW NOISE TRANSISTORS.

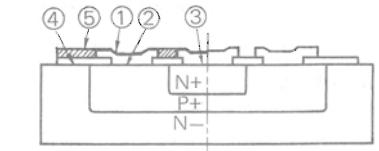
The features of the alumina passivated structure lie in the following points.

* Since the surface of the element, including the electrodes, is passivated by a stable alumina film the element will not be degraded by receiving contamination from the outside in the manufac-

turing processes coming after the electrodes have been formed.

* In NPN transistors, the low current characteristics of the h_{FE} are improved in particular and a low frequency low noise transistor of high PIV and high gain is obtained.
* The manufacture of more stable PNP transistors is possible.
* In plastic sealed type transistors, since the electrodes are passivated with a stable alumina film, the humidity resistance characteristics are improved greatly.

As described above, the adoption of the alumina passivated structure displays the features of both superior characteristics and reliability. The alumina passivated structure is as shown in Fig. 25.



Structure of alumina passivated transistor | Structure of conventional planar transistor

① Non-porous alumina. ② Aluminum base electrode.
③ Aluminum emitter electrode. ④ SiO_2
⑤ Porous alumina.

Fig. 25 Structure of an Alumina Passivated Transistor

The technique for making this alumina film is a passivation technique that consists of the adoption of an improved aluminum evaporation process together with a combination of photoresist and anode oxidizing techniques, by which portions that were formerly removed by etching are selectively replaced by a stable alumina film chemically. This alumina film, together with the gettering action of the phosphor glass layer formed on the oxide film, stabilizes the surface to produce the superior features described above.

Actual examples of the improvement of characteristics are shown in Figs. 26 and 27.

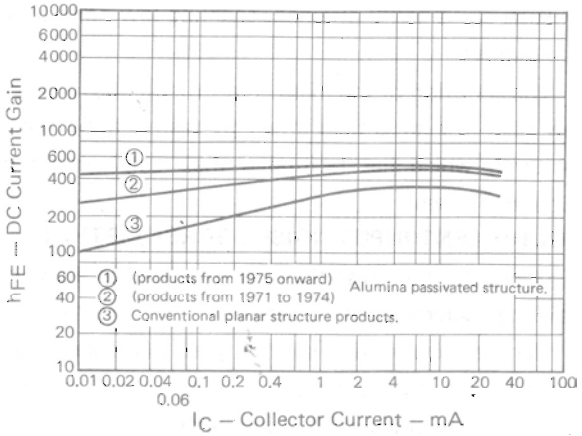


Fig. 26 h_{FE} Current Characteristics of a Bipolar Transistor (V_{CE} = 3 V)

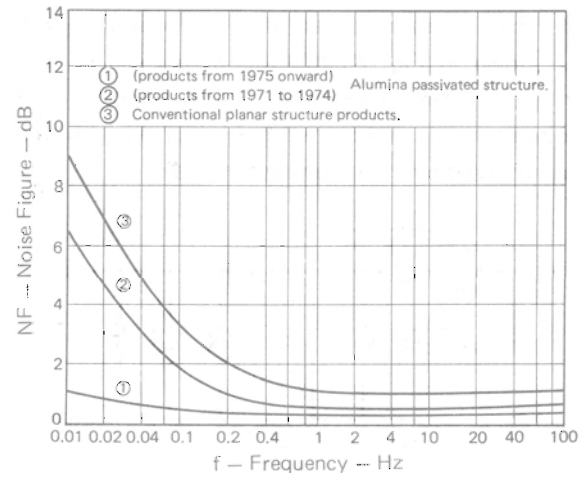


Fig. 27 Noise Figure vs. Frequency Characteristic of Bipolar Transistors. (V_{CE}=3 V, I_C=0.1 mA, R_G=10 kΩ, f=10 Hz, Δf=1 Hz)

As can be seen from the above Figs., alumina passivation technique together with the development from year to year of diffusion processes that create few crystal defects has resulted in great improvement of the h_{FE} low current and 1/f noise characteristics of transistors, compared to former products.

MESH GATE STRUCTURE, JUNCTION TYPE FIELD EFFECT TRANSISTORS.

The mesh gate structure consists of widening the channel width by shaping the gate in a mesh form, and its features lie in the following points.

* Since the degree of integration is improved, the g_m can be increased without increasing the chip area.
* The performance factor (g_m/C_{iss}) is improved.

* High g_m is easily attained, enabling low noise to be obtained.

The adoption of the mesh gate structure has enabled low cost, low noise field effect transistors to be manufactured, which has facilitated their employment in audio equipment.

EQUIVALENT INPUT NOISE SOURCE METHOD.

Generally, the noise figure is employed to show the noise characteristics of transistors.

Here, an explanation shall be given while comparing the NF and equivalent input noise source method, together with ways of thinking in the applying of the same to circuit design.

The case of bipolar transistors.

The common-emitter hybrid type equivalent circuit of a bipolar transistor can be shown as in Fig. 28 (a). As shown in Fig. 28 (b), this circuit can be drawn employing two independent noise sources, voltage noise source e_n and current noise source i_n, which can be expressed by the following formulae.

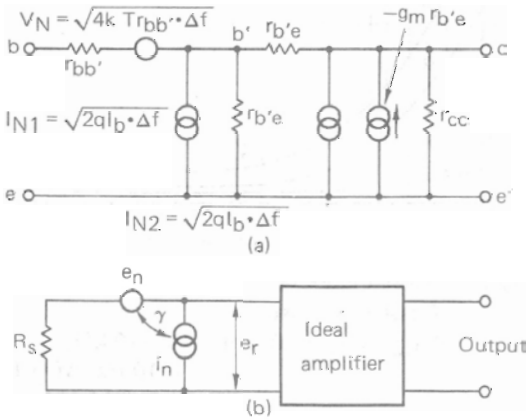


Fig. 28

When K : Boltzmann's constant.
T : Absolute temperature.
Δf : Frequency bandwidth.
g_m : Mutual conductance.
$r_{bb'}$: base resistance.
R_S : Signal source resistance.

then,

$$e_n = \sqrt{4kT(r_{bb'} + 1/2\,g_m)\cdot\Delta f}$$

$$i_n = \sqrt{\frac{4kT\cdot\Delta f}{2\beta/g_m}} = \sqrt{2qI_b\cdot\Delta f}$$

provided that,

k : Boltzmann's constant.
T : Absolute temperature.
Δf : Frequency bandwidth.
(Usually handled as $\Delta f = 1$ Hz).
g_m : Mutual conductance.

From the above equations, e_n and i_n can be equivalently related to the thermal noise in the resistors and can be expressed by the following equivalent resistances.

$$R_{Ne} = r_{bb'} + 1/2\,g_m$$
$$R_{Ni} = 2\beta/g_m$$

The case of field effect transistors.

In the case of field effect transistors, the concept is the same as that for bipolar transistors, but due to the difference in operating principle the formulae for e_n and i_n become as follows.

$$e_n = \sqrt{4KT\cdot\frac{1}{g_m}\cdot\Delta f}$$

$$i_n = \sqrt{2qI_G\cdot\Delta f}$$ I_G: Gate leakage current.

As shown in Fig. 34, the above gate leakage current I_G is that for ordinary bias and displays a voltage characteristic as shown in Fig. 29.

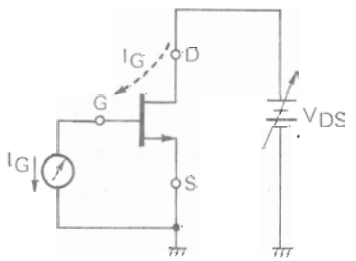


Fig. 29 Measuring Circuit for Gate Leakage Current.

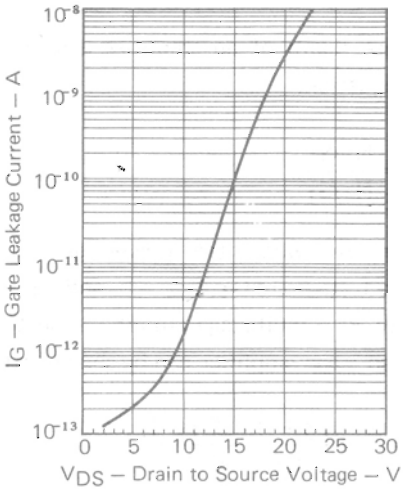


Fig. 30 Voltage Characteristic of Gate Leakage Current.

e_n, i_n and NF.

The total noise voltage at the input of the ideal amplifier of Fig. 28(b) can be expressed as the following formula.

$$e_T^2 = e_{RS}^2 + e_n^2 + i_n^2 \cdot R_S^2 + 2\gamma \cdot e_n i_n$$

provided that,

e_{RS} is the thermal noise of R_S as shown by $\sqrt{4kTR_S}$

γ: The correlation coefficient of e_n and i_n, and takes a value of $-|<\gamma<|$.

When the noise figure is shown employing the above equation, it becomes as follows.

$$NF = \frac{e_T^2}{e_{RS}^2} = 10\log_{10}\left[1 + \frac{1}{4kT}\left(\frac{e_n^2}{R_S} + i_n^2 \cdot R_S\right)\right]^* \quad (*)$$

As shown above, if the NF is determined by measuring e_n and i_n which can be measure more precisely, rather than measuring the NF directly, the e_n and i_n components contained in the NF value shown can be determined at the same time.

Fig. 31 shows the relationship between the signal source resistance R_S, total noise voltage e_T and the NF, employing e_n and i_n as the parameters.

Furthermore, from the NF equation (*) it can be seen that a optimum signal source resistance $R_S = R_{SOPt}$, which makes NF minimum, exists.

When this value of NF is put as $NF_{MIN.}$ the formula becomes as follows.

$$NF = 10\log\left[1 + \frac{e_n i_n}{2kT}\right]$$

$$= 10\log\left[1 + \sqrt{\frac{1}{\beta}\left(1 + \frac{2r_{bb'}I_C}{kT/q}\right)}\right]$$

$$R_{SOPt} = e_n/i_n$$

From the foregoing it can be seen that, in the case of bipolar transistors from a circuit standpoint it is desirable to set the bias point at a low current as possible and when R_S is large (over 10 kΩ) e_n may be disregarded and the noise will be dominated by the i_n characteristics. And, in the case of field effect transistors use at a low voltage is desirable, and when the voltage is high attention must be paid to i_n.

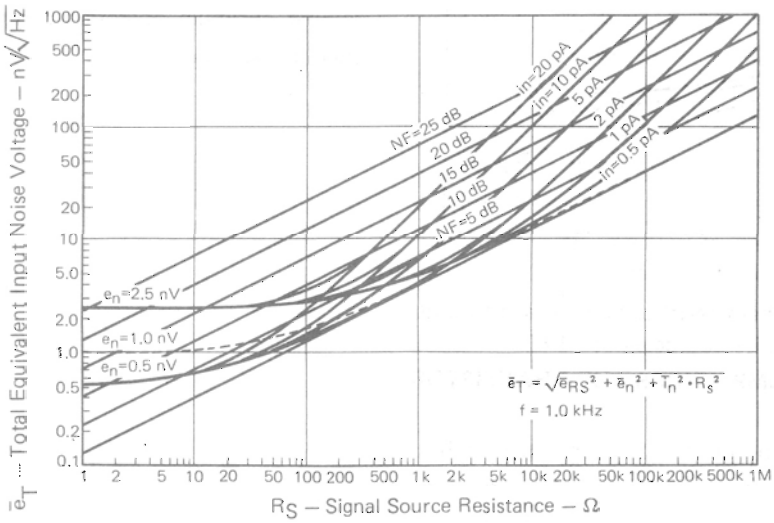


Fig. 31 Total Equivalent Input Noise Voltage vs. Signal Source Resistance R_S Characteristics.

By utilizing the equivalent input noise source method as described, a NF map can be drawn up from e_n and i_n, and from a circuit design standpoint the noise characteristics of transistors can be grasped in more diversified ways making it a very effective method.

In Fig. 32 the e_n and i_n current characteristics and the frequency characteristics of a low noise transistor are shown, and in Fig. 38 the e_n current characteristics of a low noise FET.

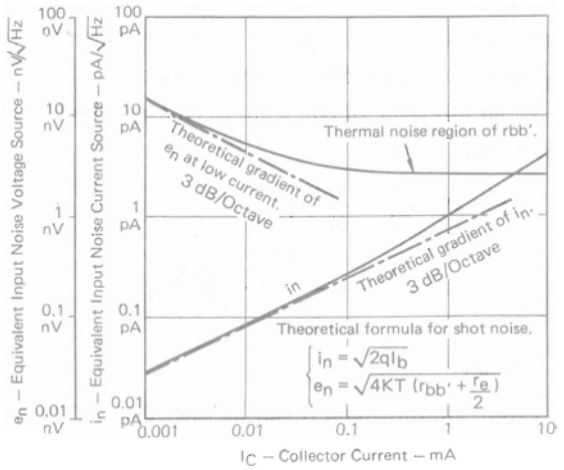


Fig. 32 e_n and i_n Current Characteristics of a Bipolar Transistor. (V_{CE} = 3 V, f = 100 Hz, Δf = 1 Hz)

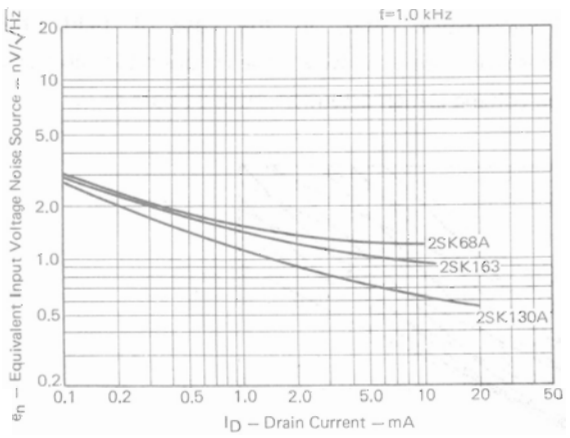


Fig. 33 Current Characteristics of Equivalent Input Voltaic Noise Source e_n of a FET.

THE SN RATIO OF AMPLIFIERS AND TRANSISTOR NOISE.

So far, the equivalent input noise source method has been explained, employing e_n, i_n and NF, in regards to the transistor alone. Here, the methods for utilizing these factors in the actual designing of circuits shall be explained.

The noise figure of an amplifier is shown by the following equation.

$$NF = \frac{N_O/S_O}{N_1/S_1}$$

Furthermore, when the power gain and noise figure of each stage are $G_1, G_2, \ldots$ and $F_1, F_2 \ldots$ respectively in a multistage amplifier, the total noise figure for an stage amplifier can be shown as follows.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_n - 1}$$

From this formula it can be seen that F_1 is determined from the noise figure of the first stage transistor and, making the gain of the first stage as large as possible will contribute towards to the improvement of the noise figure of multistage amplifiers.

Next, taking a stereo equalizing amplifier as an example of an actual circuit, the advantages of the equivalent input noise source method shall be described.

As have been described before, when low noise transistors are used, it is important to ascertain the circuit conditions and determine transistor operating conditions that will match the circuit conditions.

Fig. 34 shows a NF map. The method for determining optimum operating conditions from this map shall be explained.

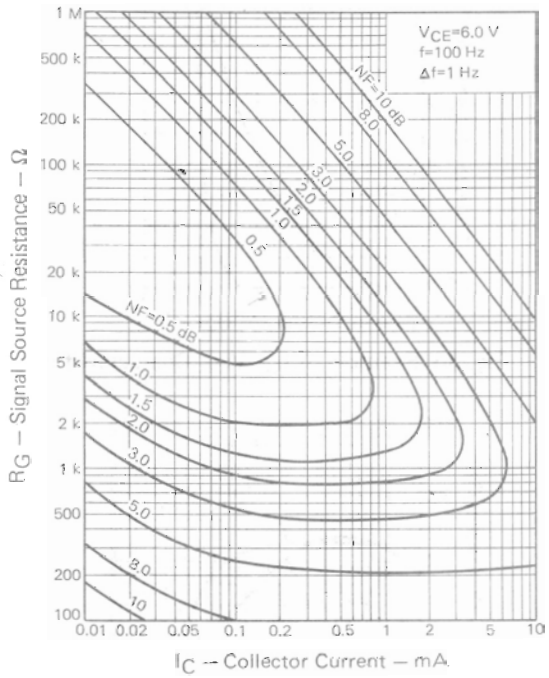


Fig. 34 NF Map.

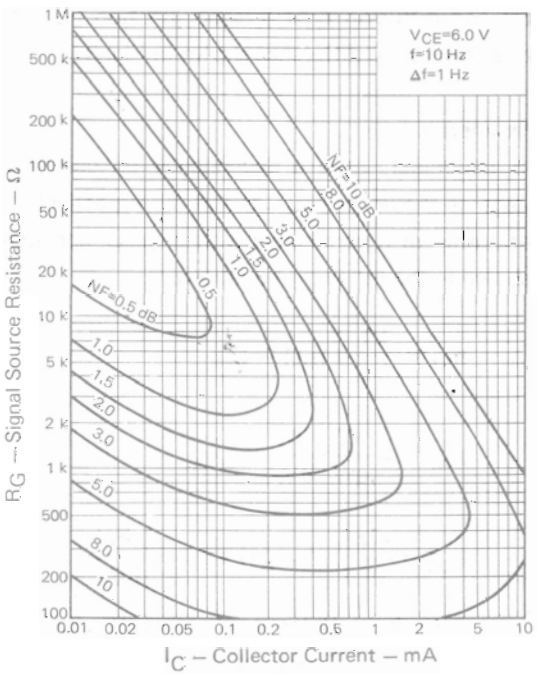


Fig. 35 NF Map.

When the signal sources of stereo equalizing amplifiers are considered to be magnetic cartridges or tape recorder heads, the majority of the signal source impedances will lie between 1 and 2 kΩ (f = 1 kHz). Also, when a frequency range of 100 Hz to 10 kHz is considered, these impedances will extend over the wide range of 500 Ω to 200 kΩ.

The I_C at which the NF will become as small as possible, within this signal source resistance range, is determined from the map. The frequency of the NF map shown in Fig. 34 is 100 Hz, however, when the frequency characteristics of a stereo equalizing amplifier is considered the gain becomes maximum at about 100 Hz, therefore this map was taken as an example. Furthermore, as reference a NF map for 10 Hz is shown in Fig. 35.

From Fig. 34 it can be judged that the collector current to be used should be selected from between several tens of μA and 100 μA.

Next, from the formula for the noise figure of multistage amplifiers it can be seen that in order to make the noise small the gain of the first stage should be made large. In order to achieve this, the collector current should be made as large as possible. Therefore, the final value of the collector current is determined through correlation of this point and the NF characteristics.

Depending on the coupling circuit with the 2nd stage, the actual gain of the first stage may be decreased. In other words, since the input resistance of the 2nd stage is the load of the first stage, the input resistance of the 2nd stage must be made large to a certain extent.

When designing low frequency low noise amplifiers as described, the NF map should be skillfully applied while giving ample consideration to the circuit conditions preceding and following each stage.

With the above, the basic way of thinking and the equivalent input noise source method and its application to NF map reading when designing low frequency low noise amplifiers have been described.

When undertaking actual designing, it is recommended that suitable use be made of specialist publications and technical journals.

5. DEPENDENCY OF PARAMETERS ON VARIOUS CONDITIONS

DC CHARACTERISTICS

Among the DC characteristics of transistors, h_{FE}, V_{BE} and $V_{CE(sat)}$ are representative. Between Ge transistors and Si transistors there is a difference in V_{BE} as shown in Fig. 36. Alloy type (step junction

type) and diffusion type (graded junction type) transistors feature the difference shown in Fig. 37.

h Parameters

h parameters have a dependency on current and voltage as shown in Figs. 38 and 39 respectively. The relationship of h parameters with physical constants is as shown in the following equations.

$$h_{ib} \approx \frac{kT}{qI_E} + r_b(1-\alpha)$$

$$h_{rb} \approx -\frac{kT}{qW}\cdot\frac{\partial W}{\partial V_C} + r_b \cdot g_c$$

$$h_{oc} \approx \frac{-I_E}{W}\left[2(1-\beta^*)+1-\gamma\right]\frac{\partial W}{\partial V_C}$$

here, k : Boltzmann's constant = 8.63×10^{-5} (eV/K)
q : Charge of electron = 1.6×10^{-5} (C)
T : Absolute temperature 273 + t (K)
W : Effective base width
g_C : Collector conductance
$\alpha = \gamma\beta^*\alpha^*$ γ : Injection efficiency
β^* : Transportation efficiency
α^* : Intrinsic current amplification factor.

Conversion of common-base h parameters to common-emitter h parameters can be performed approximately by the following formulae.

$$h_{ie} = \frac{h_{ib}}{1+h_{fb}} \qquad h_{re} = \frac{h_{ib}\cdot h_{ob}}{1+h_{fb}} = h_{rb}$$

$$h_{fe} = \frac{-h_{fb}}{1+b_{fb}} \qquad h_{oe} = \frac{h_{ob}}{1+h_{fb}}$$

The dependency of $V_{CE(sat)}$ and $V_{BE(sat)}$ on current is as shown in Fig. 40.

JUNCTION CAPACITY

Junction capacity has a dependency on voltage as shown in Fig. 41. Generally, the capacity is approximately inversely proportional to the 1/2 power of the voltage in alloy type junctions, and approximately inversely proportional to the 1/3 power of the voltage in diffusion type junctions.

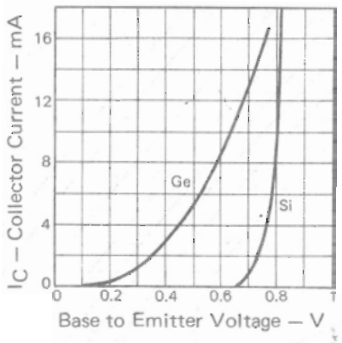


Fig. 36 Example of I_C–V_{BE} Characteristics.

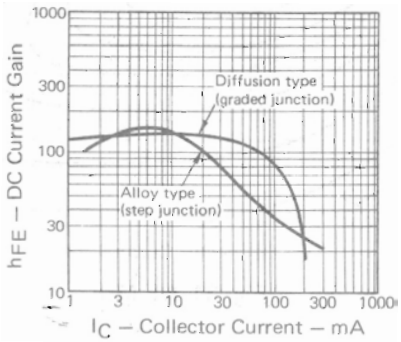


Fig. 37 Example of h_{FE}–I_C Characteristics.

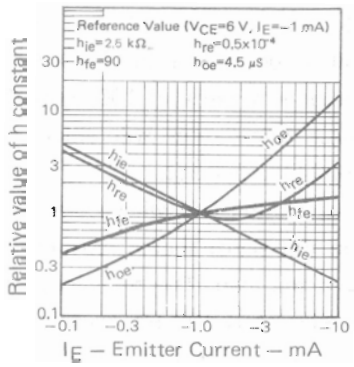


Fig. 38 Example of h Constant–I_E Chracteristics.

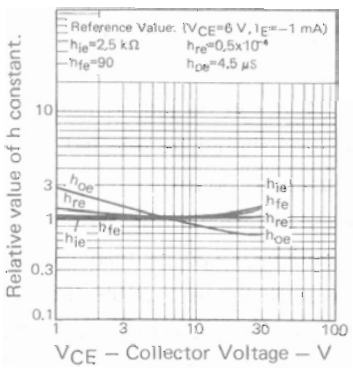


Fig. 39 Example of h Constant–V_{CE} Characteristics.

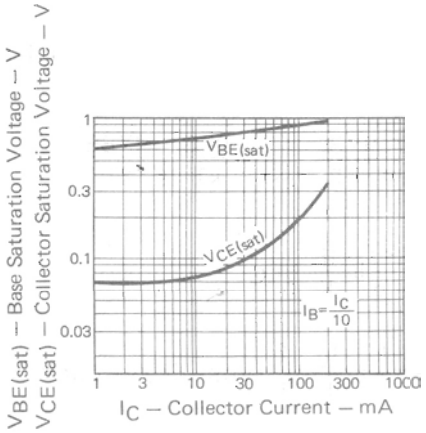


Fig. 40 Example of $V_{BE(sat)}$ and $V_{CE(sat)}$ vs. I_C Characteristics. Si Transistor

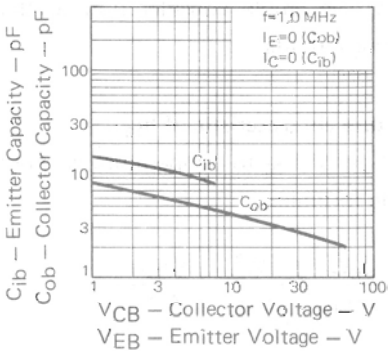


Fig. 41 Example of C_{ob}–V_{CB} and C_{ib}–V_{EB} Characteristics. Si Transistor

FREQUENCY CHARACTERISTICS

1) Frequency characteristics of current amplification factor.

The frequency characteristics of the current amplification factor are as shown in Fig. 42, and their relationship are expressed by the following formulae.

$$\alpha = \frac{\alpha_o}{1 + j\dfrac{f}{f_{\alpha b}}} \exp j\left(\frac{k-1}{k}\right)\left(\frac{f}{f_{\alpha b}}\right)$$

$$h_{fe} = \frac{\alpha_o}{1-\alpha_o} \cdot \frac{1}{1 + j\dfrac{1}{k(1-\alpha_o)} \cdot \dfrac{f}{f_{\alpha b}}} \left(\frac{f}{f_{\alpha b}} < 0.1\right)$$

$$h_{fe} = \frac{h_{feo}}{1 + j\dfrac{f}{k(1-\alpha_o) f_{\alpha b}}} \exp\left(-j\frac{1-k}{\sqrt{k}}\frac{f}{f_{\alpha b}}\right) \qquad (f < f_{\alpha b})$$

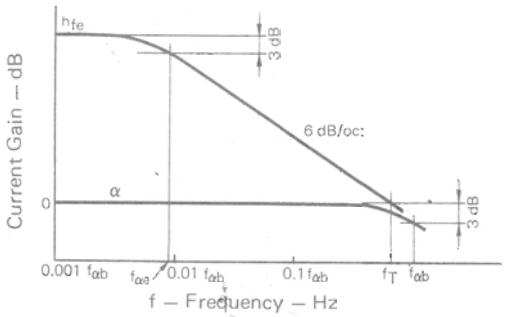


Fig. 42 Dependency of Current Amplification Factor on Frequency.

It is known that $f_{\alpha b}$, f_T and $f_{\alpha b}$ of the above formulae have the following relationship.

$$f_{\alpha e} = k\,(1-\alpha_o) f_{\alpha b}$$
$$f_T = \alpha_o k f_{\alpha b} \approx k f_{\alpha b}$$

In the above relationship, the constant k becomes 0.82 when the impurity density of the base is uniform like in alloy type junctions, and 0.5 to 0.7 when the impurity gradient is large like diffusion type junctions.

2) h parameter frequency characteristics.

The frequency characteristics of the h parameters are expressed by the following formulae.

$$h_{ie} = r_{bb'} + \frac{r_e}{1-\alpha} = r_{bb'} + \frac{r_e}{1-\alpha_o + j\omega C_e r_e}$$
$$\approx r_{bb'} + \frac{1}{j\omega C_c}$$

$$h_{re} = \frac{r_c}{r_c - (1-\alpha)} = \frac{j\omega C_e r_e}{1-\alpha_o + j\omega C_e r_e} \approx \frac{C_c}{C_e}$$

$$h_{fe} = \frac{\alpha}{1-\alpha_o + j\omega C_e r_e} \approx \frac{\alpha_o}{j\omega C_e r_e}$$

$$h_{oe} = \frac{1}{r_c(1-\alpha)} = \frac{j\omega C_c(1 + j\omega C_e r_e)}{1-\alpha_o + j\omega C_e r_e}$$
$$\approx \frac{j\omega C_c}{1-\alpha_o + j\omega C_e r_e} \approx \frac{C_c}{r_e C_e}$$

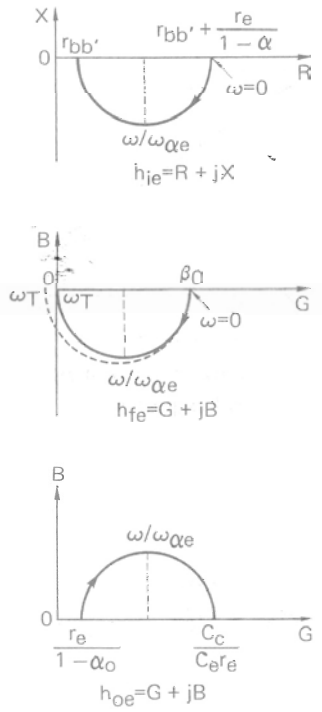


Fig. 43 Frequency Characteristics of h Parameters.

TEMPERATURE CHARACTERISTICS

Since transistors have such parameters as I_{CBO}, V_{BE} and h_{fe} which change sensitively against temperature, it is necessary to consider this point when designing circuits.

1) Temperature characteristic of I_{CBO}.

The temperature characteristic of I_{CBO} is shown by the following formula.

$$I_{CBO} = I_s \exp\left(-\frac{qE_G}{kT}\right)$$

$$\frac{\partial I_{CBO}}{\partial T} = \frac{qE_G}{kT^2} \cdot I_{CBO} \cdots\cdots \begin{cases} \text{Ge} \cdots\cdots \dfrac{\partial I_{CBO}}{\partial T} \approx 0.1\ I_{CBO} \\ \text{Si} \cdots\cdots \dfrac{\partial I_{CBO}}{\partial T} \approx 0.14\ I_{CBO} \end{cases}$$

Though the temperature coefficient of I_{CBO} is larger for Si transistors compared with Ge transistors, generally, since the absolute value of the I_{CBO} of Si transistors is amply small, in the majority of cases it may be disregarded without harm. However, in the case of Ge transistors, since the I_{CBO} is of several μA and is large, the temperature coefficient must be given consideration.

2) Temperature characteristic of V_{BE}.

The temperature characteristic of the V_{BE} is shown by the following formulae.

$$I_E = I_s e^{\frac{qV_{BE}}{kT}} = Ke^{-\frac{qE_G}{kT}} \cdot e^{\frac{qV_{BE}}{kT}}$$

$$V_{BE} = \frac{kT}{q} \ln \frac{I_E}{K} + E_G$$

$$\frac{\partial V_{BE}}{\partial T} \approx \frac{k}{q} \ln \frac{I_E}{K} = \frac{1}{T}(V_{BE} - E_G) \approx -2\ (\text{mV/°C})$$

That is to say, the temperature change of V_{BE} is about -2 mV/°C for both Ge and Si transistors. It is necessary to give ample consideration to this point, when designing circuits.

3) Temperature characteristic of h_{fe}.

The relation of h_{fe} to temperature is expressed by the following formula.

$$\frac{1}{h_{fe}} = \frac{\rho_e W}{\rho_b L_{ne}} + \frac{W^2}{2L_{pb}^2} + \frac{SA_s W}{AD_{pb}}$$

In the above formula, since the 1st term (emitter injection efficiency) and 2nd term (transportation efficiency) have a positive coefficient against temperature change and the 3rd term (surface recombination effect) has a negative coefficient it is difficult to quantitatively determine the temperature coefficient of h_{fe}. Experimentally, this coefficient has been determined to be about.

Alloy types, mesa types . . . $\dfrac{\partial h_{fe}/\partial T}{h_{fe}} \approx 0.5\ \%/°C$

Planar types . . . . . $\dfrac{\partial h_{fe}/\partial T}{h_{fe}} \approx 1\ \%/°C$

When designing circuits, consideration should be given to the decrease of h_{fe} at low temperatures.

4) Temperature characteristic of $V_{CE(sat)}$.

The temperature characteristic of $V_{CE(sat)}$ is expressed by the following formula.

$$V_{CE(sat)} = \frac{kT}{q} \ln \frac{\alpha_R \left(1 - \frac{I_C}{I_B} \cdot \frac{1-\alpha}{\alpha}\right)}{1 + \frac{I_C}{I_B}(1-\alpha_R)} + I_{Er_{SE}} \cdot I_{Cr_{SE}}$$

$V_{CE(sat)}$ has also been determined experimentally to be about.

$$\frac{\partial V_{CE(sat)}/\partial T}{V_{CE(sat)}} \approx 0.5\ \%/°C$$

TECHNICAL SYMBOLS USED IN NEC'S SEMICONDUCTOR DEVICES

(Transistors, Field Effect Transistors, Diodes)

AN ITEM COMMON TO ALL DEVICES

Symbol	Term
C	Capacitance
f	Frequency
I	DC Current
i	AC Current
L	Inductance
P	Power
R	Resistance

Symbol	Term
T	Temperature
t	Time
V	DC Voltage
v	AC Voltage
Z	Impedance
η	Efficiency
λ	Wave Length

TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Symbol	Term
SOA	Safe Operating Area
I_B	Base Current
$I_{B(DC)}$	DC Base Current
$I_{B(peak)}$	Peak Base Current
$I_{B(pulse)}$	Pulse Base Current
I_C	Collector Current
$I_{C(DC)}$	DC Collector Current
$I_{C(pulse)}$	Pulse Collector Current
I_E	Emitter Current
P_C	Collector Power Dissipation
P_T	Total Power Dissipation
R_{th}	Thermal Resistance
$R_{th(j-a)}$	Thermal Resistance (Junction to Ambient)
$R_{th(j-c)}$	Thermal Resistance (Junction to Case)
T_a	Ambient Temperature
T_c	Case Temperature
T_j	Operating Junction Temperature

Symbol	Term
T_{opt}	Operating Temperature
T_{stg}	Storage Temperature
V_{CBO}	Collector to Base Voltage
V_{CEO}	Collector to Emitter Voltage
V_{CER}	Collector to Emitter Voltage (R_{BE}=RΩ)
V_{CES}	Collector to Emitter Voltage (base emitter short circuited)
V_{CEX}	Collector to Emitter Voltage (base reverse biased)
V_{EBO}	Emitter to Base Voltage
V_{ECR}	Emitter to Collector Voltage (R_{BE}=RΩ)
V_{ECS}	Emitter to Collector Voltage (base collector short circuited)
V_{ECX}	Emitter to Collector Voltage (base reverse biased)

ELECTRICAL CHARACTERISTICS

Symbol	Term
b_{fb}	Forward Transfer Susceptance (common base)
b_{fe}	Forward Transfer Susceptance (common emitter)
b_{ib}	Input Susceptance (common base)
b_{ie}	Input Susceptance (common emitter)
b_{ob}	Output Susceptance (common base)
b_{oe}	Output Susceptance (common emitter)
b_{rb}	Reverse Transfer Susceptance (common base)
b_{re}	Reverse Transfer Susceptance (common emitter)
BV_{CBO}	Collector to Base Breakdown Voltage
BV_{CEO}	Collector to Emitter Breakdown Voltage
BV_{CER}	Collector to Emitter Breakdown Voltage (R_{BE}=RΩ)
BV_{CES}	Collector to Emitter Breakdown Voltage (base emitter short circuited)
BV_{CEX}	Collector to Emitter Breakdown Voltage (base reverse biased)
BV_{EBO}	Emitter to Base Breakdown Voltage
BV_{ECO}	Emitter to Collector Breakdown Voltage
BV_{ECR}	Emitter to Collector Breakdown Voltage (R_{BC}=RΩ)
BV_{ECS}	Emitter to Collector Breakdown Voltage (base emitter short circuited)
BV_{ECX}	Emitter to Collector Breakdown Voltage (base reverse biased)
C_{cb}	Collector Capacitance
$C_c \cdot r_{b'b}$	Collector to Base Time Constant
C_{eb}	Emitter Capacitance
C_{ib}	Input Capacitance (common base)
C_{ie}	Input Capacitance (common emitter)
C_{ob}	Output Capacitance (common base)
C_{oe}	Output Capacitance (common emitter)
C_{re}	Feedback Capacitance
$f_{\alpha b}$	α Cutoff Frequency
$f_{\alpha e}$	β Cutoff Frequency
f_{max}	Maximum Frequency of Oscillation
f_T	Gain Bandwidth Product
G_{cb}	Conversion Gain (common base)
G_{ce}	Conversion Gain (common emitter)

Symbol	Term
g_{fb}	Forward Transfer Conductance (common base)
g_{fe}	Forward Transfer Conductance (common emitter)
g_{ib}	Input Conductance (common base)
g_{ie}	Input Conductance (common emitter)
G_{max}	Maximum Unilateral Insertion Power Gain
g_{ob}	Output Conductance
g_{oe}	Output Conductance
G_{pb}	Power Gain (common base)
G_{pe}	Power Gain (common emitter)
g_{rb}	Reverse Transfer Conductance (common base)
g_{re}	Reverse Transfer Conductance (common emitter)
G_{vb}	Voltage Gain (common base)
G_{ve}	Voltage Gain (common emitter)
h_{fb}	Current Gain (common base)
h_{FC}	DC Current Gain (common collector)
h_{FE}	DC Current Gain
h_{fe}	Current Gain (common emitter)
h_{FE1}/h_{FE2}	DC Current Gain Ratio
h_{ib}	Input Impedance (common base)
h_{ie}	Input Impedance (common emitter)
h_{ob}	Output Admittance (common base)
h_{oe}	Output Admittance (common emitter)
h_{rb}	Voltage Feedback Ratio (common base)
h_{re}	Voltage Feedback Ratio (common emitter)
I_{AGC}	AGC Current
I_{CBO}	Collector Cutoff Current
I_{CEO}	Collector Cutoff Current
I_{CER}	Collector Cutoff Current (R_{BE}=RΩ)
I_{CES}	Collector Cutoff Current (base emitter short circuited)
I_{CEX}	Collector Cutoff Current (base reverse biased)
I_{EBO}	Emitter Cutoff Current
I_{ECO}	Emitter Cutoff Current
I_{ECR}	Emitter Cutoff Current (R_{BC}=RΩ)
I_{ECS}	Emitter Cutoff Current (base emitter short circuited)
I_{ECX}	Emitter Cutoff Current (base reverse biased)

Symbol	Term
KF	Distortion
KF_2	2rd Harmonic Distortion
KF_3	3rd Harmonic Distortion
LV_{CEO}	Collector to Emitter Sustaining Voltage
MAG	Maximum Available Power Gain
NF	Noise Figure
NV	Noise Voltage
P_i	Input Power
P_o	Output Power
P_{osc}	Oscillation Power
PW	Pulse Width
$r_{bb'}$	Base Spreading Resistance
$R_{e(hie)}$	Real Part of Input Impedance
R_G	Source Resistance
r_{ib}	Input Resistance (common base)
r_{ie}	Input Resistance (common emitter)
R_L	Load Resistance
r_{ob}	Output Resistance (common base)
r_{oe}	Output Resistance (common emitter)
S_{11}	Input Reflection Coefficient
S_{12}	Reverse Insertion Gain
S_{21}	Forward Insertion Gain
S_{22}	Output Reflection Coefficient
$\|S_{21}\|^2$	Forward Insertion Gain
t_d	Delay Time
t_f	Fall Time
T.H.D.	Total Harmonic Distortion
t_{off}	Turn off Time
t_{on}	Turn on Time
t_r	Rise Time
$t_{stg}(t_s)$	Storage Time
V_{AGC}	AGC Voltage
V_{BB}	Supply Voltage
V_{BE}	Base to Emitter Voltage
$V_{BE(sat)}$	Base Saturation Voltage
V_{CC}	Supply Voltage
V_{CEK}	Knee Voltage
$V_{CE(sat)}$	Collector Saturation Voltage
V_{EE}	Supply Voltage
V_{OSC}	Oscillation Voltage
y_{fb}	Forward Transfer Admittance (common base)
y_{fe}	Forward Transfer Admittance (common emitter)
Y_G	Source Admittance
y_{ib}	Input Admittance (common base)
y_{ie}	Input Admittance (common emitter)

Symbol	Term
Y_L	Load Admittance
y_{ob}	Output Admittance (common base)
y_{oe}	Output Admittance (common emitter)
y_{rb}	Reverse Transfer Admittance (common base)
y_{re}	Reverse Transfer Admittance (common emitter)
Z_G	Source Impedance
Z_{ib}	Input Impedance (common base)
Z_{ie}	Input Impedance (common emitter)
Z_L	Load Impedance
Z_o	Characteristic Impedance
Z_{ob}	Output Impedance (common base)
Z_{oe}	Output Impedance (common emitter)
η_c	Collector Efficiency
η_{osc}	Oscillation Efficiency
η_t	Total Efficiency

FIELD EFFECT TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Symbol	Term
I_D	Drain Current
I_G	Gate Current
I_S	Source Current
P_T	Total Power Dissipation
T_a	Ambient Temperature
T_{ch}	Channel Temperature
T_j	Junction Temperature
T_{stg}	Storage Temperature
V_{DSS}	Drain to Source Voltage (gate source short circuited)

Symbol	Term
V_{DSX}	Drain to Source Voltage (gate reverse biased)
V_{GDO}	Gate to Drain Voltage
V_{GDS}	Gate to Drain Voltage (drain source short circuited)
V_{GSO}	Gate to Source Voltage
V_{GSS}	Gate to Source Voltage (drain source short circuited)

ELECTRICAL CHARACTERISTICS

Symbol	Term
b_{fs}	Forward Transfer Susceptance (common source)
b_{is}	Input Susceptance (common source)
b_{os}	Output Susceptance (common source)
b_{rs}	Reverse Transfer Susceptance (common source)
BV_{DSS}	Drain to Source Breakdown Voltage
BV_{DSX}	Drain to Source Breakdown Voltage (gate reverse biased)
BV_{GSO}	Gate to Source Breakdown Voltage
BV_{GSS}	Gate to Source Breakdown Voltage (drain source short circuited)
C_{iss}	Input Capacitance
C_{oss}	Output Capacitance
C_{rss}	Feedback Capacitance
f_{max}	Maximum Frequency of Oscillation
g_{fs}	Forward Transfer Conductance
g_{is}	Input Conductance
g_{os}	Output Conductance
G_{ps}	Power Gain (common source)

Symbol	Term
g_{rs}	Reverse Conductance
I_{DSS}	Zero-Gate Voltage Drain Current
I_{DSS}	Drain Leak Current
I_{GSS}	Gate Cutoff Current
I_{GSS}	Gate Leak Current
MAG	Maximum Available Power Gain
NF	Noise Figure
NV	Noise Voltage
r_{ds}	Output Resistance
$r_{ds(on)}$	Drain to Source ON Resistance
$\|S21s\|^2$	Insertion Gain
U	Maximum Unilateral Insertion Power Gain
$V_{GS(off)}$	Gate to Source Cutoff Voltage
V_p	Pinch off Voltage
y_{fs}(or g_m)	Forward Transfer Admittance
y_{is}	Input Admittance
y_{os}	Output Admittance
y_{rs}	Reverse Transfer Admittance

DIODE

ABSOLUTE MAXIMUM RATINGS

Symbol	Term
I_{FM}	Peak Forward Current
$I_{F(surge)}$	Forward Surge Current
I_O	Average Rectified Current
P	Power Dissipation
P_{RSM}	Surge Reverse Power
R_{th}	Thermal Resistance
$R_{th(j-a)}$	Thermal Resistance (junction to ambient)
$R_{th(j-c)}$	Thermal Resistance (junction to case)
T_a	Ambient Temperature

Symbol	Term
T_C	Case Temperature
T_j	Operating Junction Temperature
T_{op}	Operating Temperature
T_{stg}	Storage Temperature
V_R	Reverse Voltage
V_{RM}	Peak Reverse Voltage
V_T	Tuning Voltage
σ_L	VSWR

ELECTRICAL CHARACTERISTICS

Symbol	Term
B_O	Burn out
C_t	Terminal Capacitance
$\Delta f/\Delta T$	Frequency Temperature Coefficient
f_c	Cutoff Frequency
Δf_e	Voltage Tuning Range
Δf_m	Mechanical Tuning Range
f_o	Center Frequency
f_{osc}	Oscillation Frequency
I_o	Rectified Current
I_{op}	Operating Current
I_p	Peak Point Current
I_p/I_v	Peak Point Current Vally Current Ratic
I_r	Reverse Recovery Current
I_v	Valley Current
L_C	Conversion Loss, Multiple Loss
L_i	Insertion Loss
N	Capacitance Ratic
NF	Noise Figure
N_{MAX}	Maximum Capacitance Ratio
P_{osc}	Oscillation Power

Symbol	Term
P_{out}	Conversion Power
Q	Figure of Merit
Q_s	Stored Charge
R_d	Differential Resistance
R_o	DC Current
R_p	RF Parallel Resistance
R_s	RF Series Resistance
t_{fr}	Forward Recovery Time
t_{rr}	Reverse Recovery Time
t_t	Transition Time
V_F	Forward Voltage
V_{op}	Operating Voltage
V_p	Peak Point Voltage
V_{pp}	Projected Peak Point Voltage
V_s	Switch Voltage
V_{th}	Threshold Voltage
V_v	Valley Voltage
V_Z	Zener Voltage
Z_Z	Dynamic Impedance
Z_{ZK}	Knee Dynamic Impedance
η_{osc}	Oscillation Efficiency
τ	Minority Carrier Lifetime
γ_Z	Zener Voltage Temperature Coefficient

RELIABILITY AND QUALITY ASSURANCE SYSTEM OF NEC'S SEMICONDUCTOR DEVICES

GENERALS

NEC has been manufacturing semiconductor devices readily adaptable to a large number of applications ranging from consumer goods up to space electronics, including communication and industrial systems. Best efforts have been made to have individual device soak up its inherent reliability and to control its quality so as to enable customers to use it with confidence.

Descriptions on the reliability and quality assurance system for NEC semiconductor devices will be made for customer's information.

1. RELIABILITY OF SEMICONDUCTOR DEVICES

1-1. Reliability Function

It is natural that equipment and components have lower performance as the longer and the more frequent use of them. This means that reliability decreases with the increase in time and frequency of use. Although reliability reduction depends greatly on the kinds of devices and the relationships between the kind and degree of stresses applied, failures modes can be roughly categorized into three modes by their natures as shown in Figure 1.

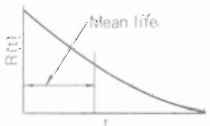
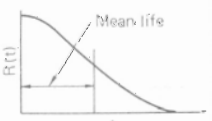
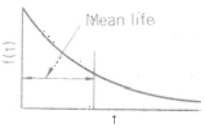
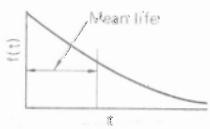
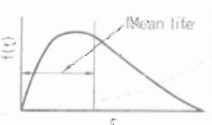
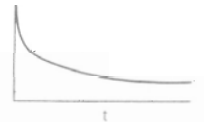
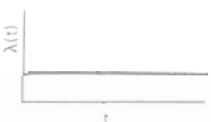
	Initial Failure	Random Failure	Wear-out Failure (Fatigue Failure)
Reliability Function (Survival Rate) R(t)			
Probable Density (Frequency Distribution) f(t)			
Failure Rate λ(t)			
Effectiveness of Periodic Repairs	Detrimental	Ineffective	Effective

Figure 1. Failure Modes

To make statistical study of these phenomena, distribution functions, such as Weibull distribution, gamma distribution, logarithmic-normal distribution, etc., are discussed. Weibull distribution, among these, is most likely discussed and seems to be the most suitable as a reliability function for semiconductor devices. The reliability of these products are expressed by the following factors in Weibull distribution.

Reliability function: $R(t) = \exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^m\right\}$

Cumulative distribution function: $F(t) = 1 - \exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^m\right\}$

Probable density function: $f(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} \exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^m\right\}$

Instantaneous failure rate: $\lambda(t) = \frac{m}{\eta^m}(t-\gamma)^{m-1}$

Mean life: $t_m = \eta \cdot \Gamma\left(1+\frac{1}{m}\right)$ note 1)

note 1)
Here, $\Gamma(\ )$ is gamma function. The relationship between m and $\Gamma(1+\frac{1}{m})$ is shown in Figure 2.

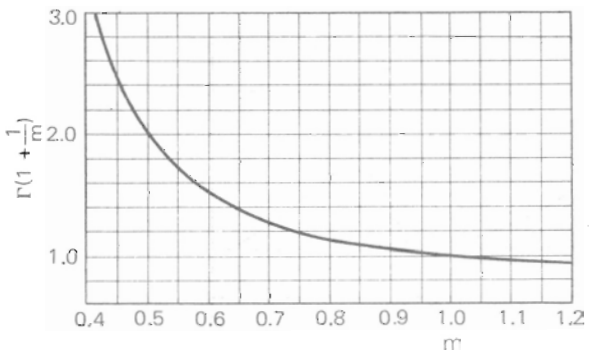


Figure 2. Relationship between Shape Parameter m and Gamma Function

This distribution function includes Location Parameter: γ, Scale Parameter: η, and Shape Parameter: m. The shape parameter can be utilized to determine the mode of each failure as follows:

$m < 1$ Initial failure

$m = 1$ Random failure (exponential distribution)

$m > 1$ Wear-out failure

In checking whether the reliability function complies with Weibull function or not and obtaining the above parameters, γ, η, m, Weibull probability paper can be utilized.

1-2. Measure to Express Reliability, Failure Rate and Reliability Index.

Failure rate is defined as "the rate that a system, equipment, devices (such as semiconductor devices), etc. which have been in operation would develop failures per unit time." If reliability function is R(t), failure rate which is also a function of time can be expressed as

$$\lambda(t) = -\frac{dR(t)}{dt} \cdot \frac{1}{R(t)}$$

In general, failure rate has two kinds: instantaneous failure rate and mean failure rate. "Failure rate" in a simple statement often refers to instantaneous failure rate. The failure rate $\lambda(t)$ in this paper also means the same.

Mean failure rate $\overline{\lambda}(t)$ can be obtained from the following formula.

$$\overline{\lambda}(t) = \frac{\text{Total number of failures in a certain period}}{\text{Total operating hours}} = \frac{n}{\sum_{j=1}^{n} t_j n_j + (n_0 - n)t}$$

Where n_j is the number of failures at time t_j, n is the number of failures in the observation period t, and n_0 is the number of devices put to testing or operation. When n_0 is sufficiently large, the mean failure rate can be expressed as follows:

$$\overline{\lambda}(t) = \frac{1-R(t)}{\int_0^t t \cdot f(t)dt + t \cdot R(t)} = \frac{1-R(t)}{\int_0^t R(t)dt}$$

where f(t) is probable density function.

However, instantaneous failure rate $\lambda(t)$ and mean failure rate $\overline{\lambda}(t)$ as defined above cannot easily be obtained from the test results or practical data.

Therefore, the following formula has been used conventionally as the measure of failure rate.

$$RI(t) = \frac{1}{R(0)} \cdot \frac{1-R(t)}{t} = \frac{n}{n_0 \times t}$$

This expression has such a practical effect that the approximate number of failures in a certain period and thus the approximate reliability can be estimated instantly. Here, RI(t) is called reliability index and should be distinguished from $\lambda(t)$ and $\overline{\lambda}(t)$.

In discussing the results of accelerated life test, all of reliability index, instantaneous failure rate, and mean failure rate use %/1000 h as a rule. In describing the value in actual operation, the unit of

FIT (failure in time) = 10^{-9} /h has been used increasingly.

If it is proved that $R(t_j)$ is 99 % in a certain period of time t_j, the mean failure rate after t_j can be estimated as shown in Figure 3(a), the reliability index after t_j as shown in Figure 3(b), and the instantaneous failure rate after t_j as shown in Figure 3(c). In the curves of Figure 3(b), the value of reliability index is not constant but varies with time even with m = 1.0. On the contrary, in the curves of Figures 3(a) and 3(c), reliability factors are always constant regardless of time if m=1.0. Also, with m other than 1.0, the relationship between reliability factor and time shows considerable difference among Figures 3(a), 3(b), and 3(c).

For this reason, the followings must be taken into account.

(1) Reliability index RI(t) may frequently be accompanied by some error when it is used as a direct mean to assume instantaneous failure rate $\lambda(t)$ and mean failure rate $\overline{\lambda}(t)$. And such error would become greater as the value of m deviates more from 1.0.

(2) If m=1.0, or reliability function is determined by exponential distribution, failure rate is said to be constant regardless of time. However, this applies only to instantaneous failure rate and mean failure rate but not to reliability index.

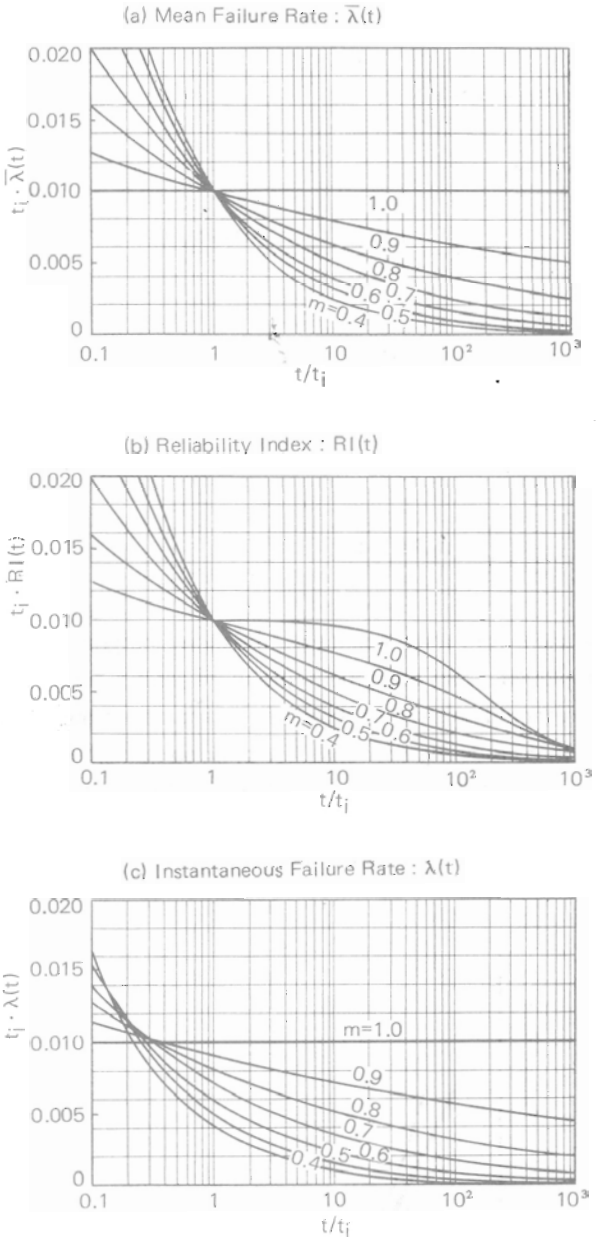


Figure 3. Reliability to be Estimated after $t=t_j$ When $R(t)=0.99$ was Recognized

1-3. Reliability of Equipment

With the recent astounding progress in electronics, electronic equipment have become larger in size and more complicated in composition, which necessitates an extremely large number of components in system or a equipment.

Suppose equipment has n_0 numbers of semiconductor devices and is used under the condition that its t-hour-later reliability will be r(t), the reliability R(t) of this device based on the failures of the devices can be ob-

tained from the following equation:

$$R(t) = \left\{ r(t) \right\}^{n_0}$$

However,

$$r(t) = \exp\left\{ -\left(\frac{t}{\eta}\right)^m \right\} = \exp\left(-\frac{\lambda(t) \cdot t}{m}\right)$$

Therefore,

$$R(t) = \left\{ \exp\left(-\frac{\lambda(t) \cdot t}{m}\right) \right\}^{n_0} = \exp\left(-\frac{n_0 \lambda(t) \cdot t}{m}\right)$$

And, furthermore, more appoximation can be attained as

$$R(t) = 1 - \frac{n_0 \lambda(t) \cdot t}{m}$$

As seen from these equations, the more components are employed in an equipment the more careful consideration should be given to the selection and use of them.

In considering the reliability of an equipment a measure called MTBF (Mean Time Between Failures) is often used. MTBF is the average of operation times between failures, and the MTBF of the above-mentioned equipment which has n_0 numbers of semiconductor devices and is used under the condition that its t-hour-later instantaneous failure rate will be $\lambda(t)$ based on the failures of its semiconductor devices is as follows:

$$MTBF = \frac{m}{n_0 \lambda(\eta)} \Gamma\left(1 + \frac{1}{m}\right)$$

2. FAILURES OF SEMICONDUCTOR DEVICES

2-1. Features of Semiconductor Device's Failure

Conventionally, the failure rates of electronic components and those of system and equipment which incorporate these components are often indicated by a bath-tub curve. Since, however, semiconductor devices may provide the shape parameter m which is smaller than 1 (i.e. 0.5 to 0.95 usually) so far as the conditions applied are not too specific, the failures of these devices will be classified into initial failure which shows a curve different from the bath-tub curve. That is, semiconductor devices would have a longer initial failure time, more than 6 months in many cases, and the changing from initial failure period to random failure period is not always distinct. These characteristics are illustrated in Figure 4.

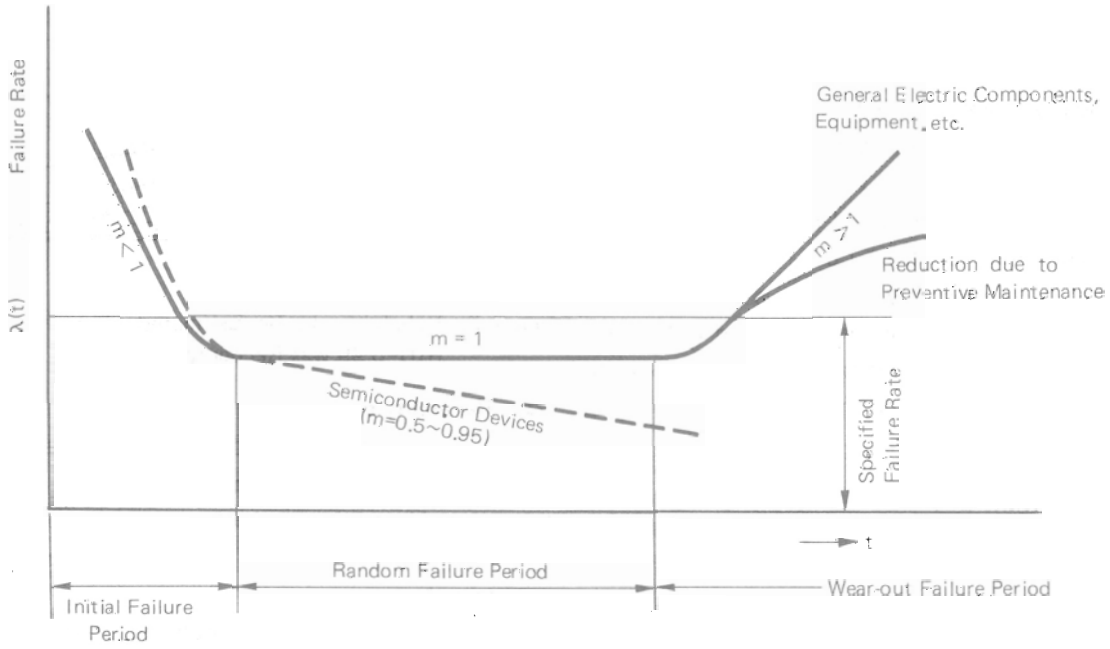


Figure 4. Failure Rate Curves (Bath-tub Curve) for Semiconductor Devices and General Electric Components and Equipment

For instance, reliability to be estimated after $t=t_j$ when $R(t_j)=99$ % was recognized according to the value from shape parameter: m, as shown in Figure 5.

This means that semiconductor devices have far longer life than other equipment belong to exponential distribution (m=1).

In other words, the semiconductor devices which can be used without failure up to the period have longer reliability after that period, so regularly replacement for maintenance will be detrimental for reliability of the equipment.

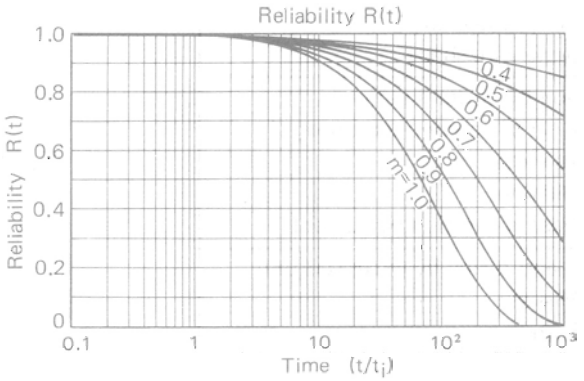


Figure 5. Reliability to be Estimated after $t=t_j$ when $R(t)=0.99$ was recognized.

2-2. Failure Analysis

Failures of semiconductor devices are attributable to their own defects or their operating or environmental conditions. Figure 6 shows a result of failure investigations in terms of classified modes of failures after inspection of the semiconductor devices that were returned in complaint of failure in the field. As indicated by the example, unexpectedly many failures can be attributed to design and use of the device, beyond expectations.

In any case, failure investigation for semiconductor devices are quite important to the improvement of reliability and quality from the viewpoint of design, manufacture and application of those products. We are always making our best to study such investigation results and feed them back to our development, design, manufacturing and sales departments so that they can be served to research and development of new devices, improvement of device, improvement of manufacturing and screening processes, study of inspection method, application technologies, etc., and thus to supply better products to every customers.

In the following description, characteristics of failures, reliability, and major failure modes of semiconductor devices are discussed.

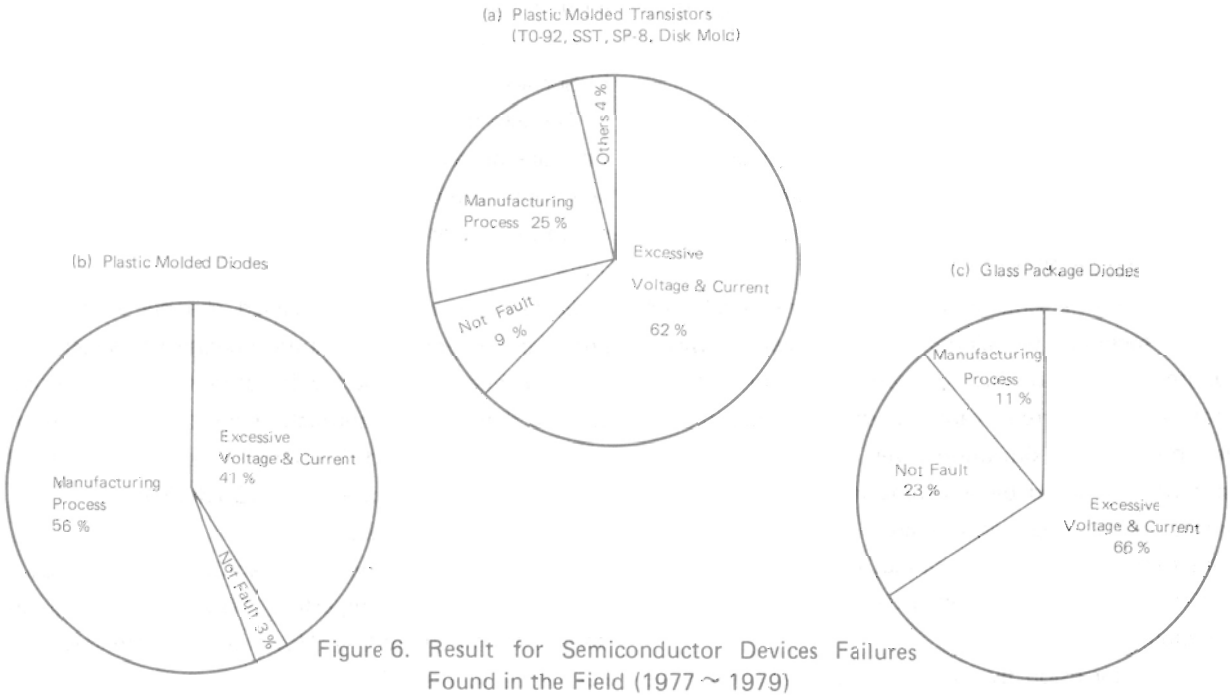


Figure 6. Result for Semiconductor Devices Failures Found in the Field (1977 ~ 1979)

2-3. Failure Mechanism

1) Connecting Portion

A package and elements are usually connected by gold wires, and this connecting portion can be the cause of failures.

The material or size of wires and bonding methods are all fully taken into account in designing and manufacturing so that they can meet the most severe of all the conditions thus assuring the quality of semiconductor devices. However, if such products are exposed to the condition exceeding the rating, there may occur failures such as open or partial open.

Some classified examples of failures in connecting portions are given in Table 1, and it is seen that similar failures may occur due to the faults in design or manufacture. And very often it is difficult to find the causes of such failures by investigating the defective devices.

Table 1. Examples of Failures in Connecting Portion and Their Causes

Failures in Connecting Portion	Mechanical causes	Excessive mechanical shock Incomplete bonding Defective pointed tools Inadequate wire shape
	Chemical causes	Corrosion by contamination Formation of compounds among Al ~ Au metals {Heating {Heat generation by current
	Electrical causes	Melting and fusing by excess current {Misuse {Surge

2) Junction Region

Junction region can be broken by the outbreak of surge or hot spot. Overvoltages applied from the outside are considered to be the major causes of those breaks.

3) Packaging

As for the failures related to packages, failure modes are remarkably different according to their structures, but any package failure may be a cause of a serious failure of semiconductor devices.

4) Metallization Wiring

Elements in a semiconductor device are usually connected together by aluminum metallization wiring. Failures related to this connection are, for example, scratches and current capacity shortage caused by a step portion of oxidization layer. Substandard devices have been removed by screening in the manufacturing process. If, however, devices are exposed to the conditions exceeding maximum rating, it cannot be avoided that the occurrence of open circuits in such weak points in metallization wiring.

As the corrosion by the humidity of aluminum electrodes is caused by the coexistence of moisture and an extremely small quantity of impurities, the use of plastic molded packages may cause troubles; especially when the humidity is extremely high, it can not be denied that plastic molded packages are inferior in reliability to hermetically sealed packages.

5) Surface Deterioration

Though the oxidized surface of semiconductor devices are protected with resin, the surface is sometimes deteriorated, and in many cases the deterioration is liable to be accelerated by the effect of voltage or temperature.

Surface deterioration — called channel — of those products sometimes causes an increase of leakage current, but heating of them will restore their characteristics. The deterioration through channel formation is often observed in forced deterioration tests, but it is hardly found in the field except for MOS devices.

6) Incomplete Manufacture

Failures due to incomplete manufacture may be caused by, for example, imperfect diffusion process or incomplete chip mounting. However, the defective devices owing to these failures are almost perfectly removed through the above-mentioned quality control acti-

vities in the manufacturing process, so practically no defective devices will be delivered to customers.

Major failure features and modes of semiconductor devices were described above, and in the following Table 2, kinds, modes, and causes of these failures are tabulated:

Table 2. Kind, Mode, Cause of Failures Related to Chips

Item	Kind of Failure	Failure Mode	Cause
Wire Bonding	Wire disconnection	Open	Incomplete manufacture or misuse
	Wire short	Short	
	Purple plague	Open, high resistance	
	Bond detaching	Open, high resistance	
	Misplaced bonding, loose contact	Open, high resistance short	Incomplete manufacture
	Improper bond shape	Open, high resistance	
	Erroneous bonding	Open, high resistance	
Junction Region	Destruction by surge	Low breakdown voltage, short, open	Incomplete manufacture or misuse
	Hot spot		
Case	Lead disconnection	Open, high resistance	Ditto
	Lead short	Short, high leakage	
Seal	Incomplete seal	Breakdown voltage deterioration, high leakage	Ditto
	Enclosed high humidity gas		
	Contamination of surface		
	Dust and dirt	Short, low breakdown voltage, large leakage	
Metallization	High current density	Open, high resistance	Misuse
	Electromigration		
	Scratch	Open, short	Incomplete manufacture
	Insufficient thickness	Open, high resistance	
	Excessive etching		
	Contamination, dust and dirt	Open, high resistance	Incomplete manufacture or misuse
	Poor wiring and element connection		
Chip Mounting	Chip crack	Open, short	Ditto
	Chip detaching	Open, short, high thermal resistance	
Oxidized Film	Pinhole, crack	Low breakdown voltage, short	Incomplete manufacture
	Insufficiently Oxidized film thickness	Low breakdown voltage	
Surface Treatment	Channel formation	Low breakdown voltage high leakage	Ditto
	Contamination		
Mask	Insufficient P.R.	Low breakdown voltage, short, open, high leakage	Ditto
	Mask misalignment		
Material and Diffusion	Improper impurity density	Ditto	Ditto

3. RELIABILITY AND QUALITY ASSURANCE SYSTEM FOR NEC SEMICONDUCTOR DEVICES

3-1. Cycle of Reliability and Quality Control System

Reliability and quality assurance of semiconductor devices can be achieved by building reliability into the devices in each process from market survey and collection of user's requirements to the development and manufacturing design, and purchase of materials and parts, and also by means of the direct quality assurance by the quality control, reliability test and examination relating to the manufacture, as well as the shipment control and after-sale service, all being performed under a consolidated system.

The system is outlined in Figure 7. Control activities for each item in the system will be described below.

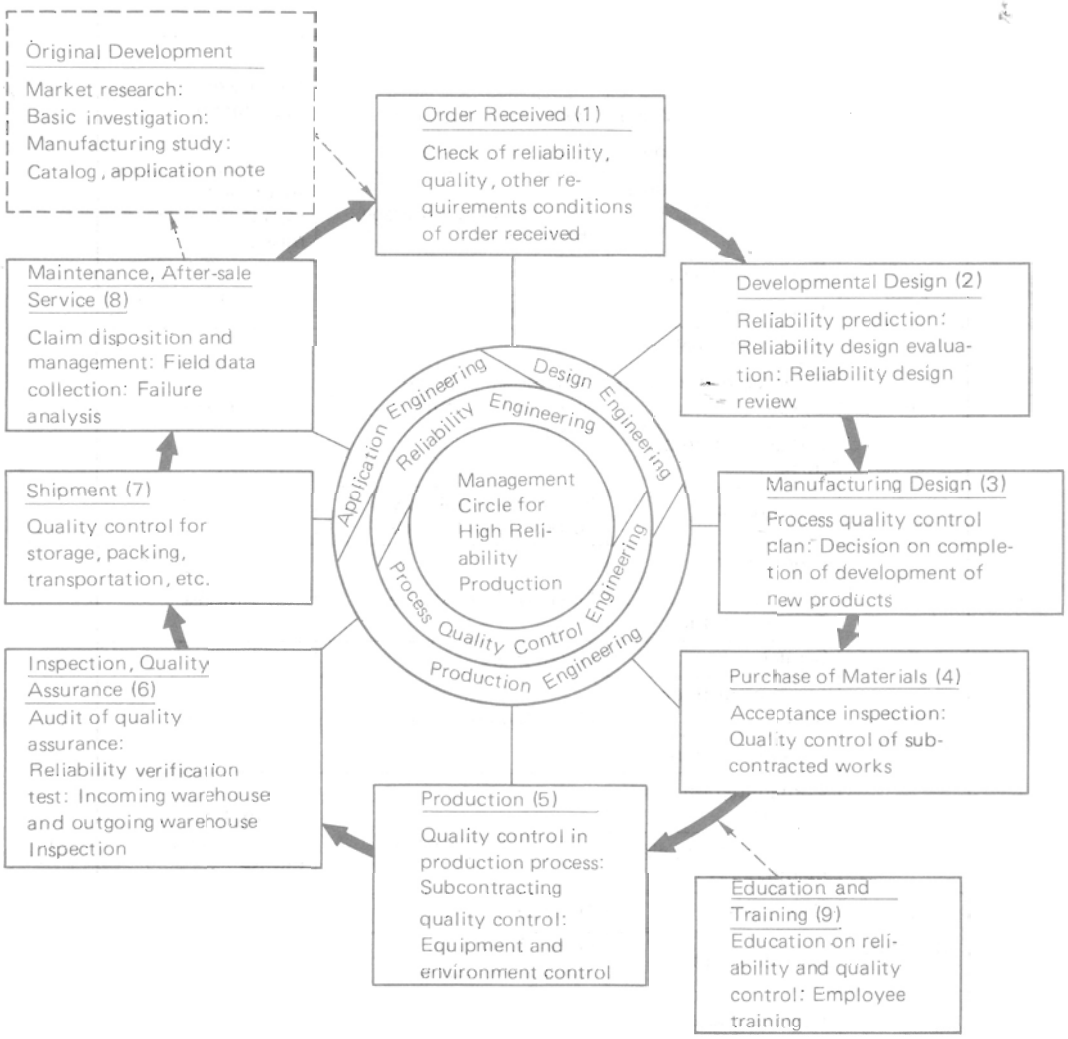


Figure 7. Cycle of Reliability and Quality Control System

3-2. Order Received

In order to manufacture and supply devices which meet the purpose of application, it is essential to build reliability and quality required or expected by the users at large into the design of the devices. Accordingly, prior to the development and order receiving kinds of equipment to be used and environmental conditions, circuit operations and so on, in addition to the performance required and allowable field failure rates must be investigated together with the price, time for delivery and quantity, and then the development plan of new products and new order receiving plan are established.

3-3. Development Design

New product development plan is determined after careful investigations performed by various departments in charge of design, manufacturing engineering reliability and quality control and so forth. According to this development plan, design, trial run and evaluation are performed. Mass production is released only when the evaluation results which are fully satisfactory have been obtained.

At the stage where the design has been completed, design review is performed to exclude defects in the design. In this review, the design is compared with the design standard, and other factors which influence the reliability and quality are examined carefully. As the result of it, if necessary, the design is partially modified or entirely redesigned.

When the design has passed the review, trial run is performed to check whether the product satisfies the required characteristics and reliability, and also to verify the stability in the manufacturing process.

When the pre-production shifts to actual mass production, various kinds of reliability and quality verification test are performed by the reliability and quality control department in accordance with the quality verification system. When it is confirmed that there is no problem in the quality, various standards for the mass production are made, and the mass production is started. Processes described above are shown in Figure 8.

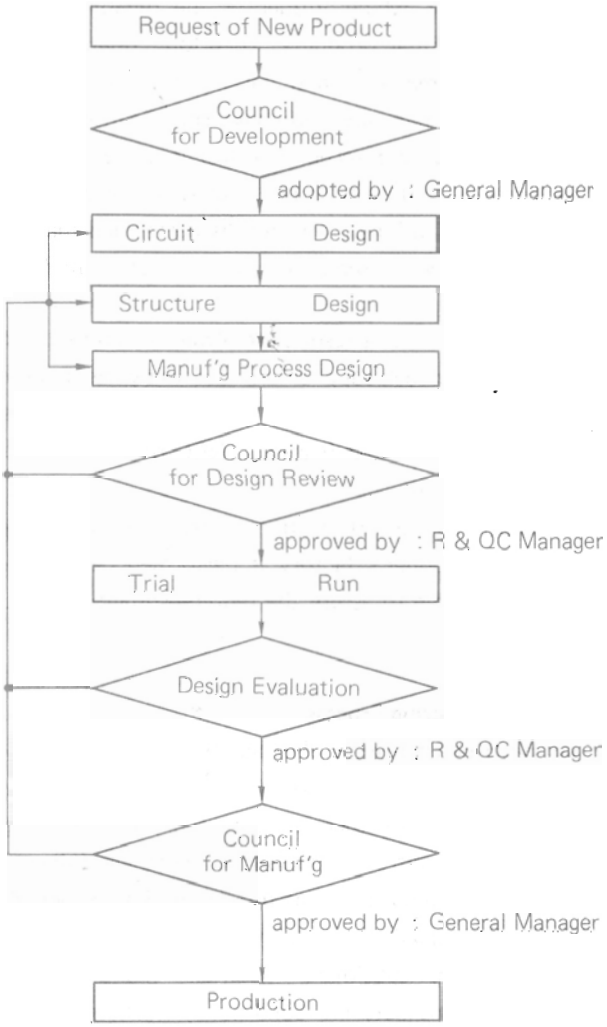


Figure 8. Flow Chart of New Product Development

3-4. Manufacturing Design

When it is confirmed that the quality required can be achieved by the quality verification system, the process shifts to the mass production based on the written mass production plan. Prior to the shift, however, the design department prepares a document for manufacturing plan including the reliability and quality control relating to the manufacturing processes, such as necessary materials, equipment, manufacturing conditions environment and so on, and thus establishes the mass production system. Even after the mass production has started, the standards for the manufacture and control are always re-examined to improve and rationalize them.

3-5. Purchase of Material

Quality of materials and parts purchased is also an

important factor which influences the reliability and quality of the final products. Therefore, quality control for those materials and parts is performed carefully and systematically. Purchase specifications have been established, and acceptance test is performed for those materials and parts to be purchased in accordance with the specifications. The test is performed mainly in accordance with sampling methods stipulated in MIL-STD-105.

The acceptance test results are always examined and accumulated for each supplier and devices by the quality control department. If any of the materials and parts does not meet the specifications, NEC does make the supplier improve it.

In addition to the utilization of test results, inspection of the supplier's factory is performed periodically or at any time to assure the required quality and to stabilize it.

3-6. Manufacturing Process

As described above, a plan has been established by which a satisfactory high quality can be expected at the stage of design. Furthermore, at the manufacturing stage, quality control is performed most carefully to maintain the quality aimed at the design. Factors which influence the quality at the manufacturing stage are main materials, subsidiary materials, manufacturing equipment, manufacturing conditions, workers, manufacturing environments and so on. These factors must be controlled at the most suitable conditions.

1) Subsidiary Materials

Subsidiary materials such as high purity gas, chemicals, and deionized water are used in the manufacturing process, and those having quality which is suitable for the purpose of use must be selected. Inert gas to be enclosed in the semiconductor package and other gases such as hydrogen and oxygen to be used in the manufacturing process are purchased from specified manufacturer in accordance with the high purity specifications especially established by NEC. Sometimes gases are directly sent to NEC factory for use through pipe lines extended from the gas manufacturer in order to maintain the purity of gas and for the economy. Chemicals and chemical materials of specific and highest purity are used according to their usage. For instance, chemicals qualified in accordance with "NEC Semiconductor Specifications" which have been specifically established by NEC are used to improve the quality of products, and this procedure has proved quite effective.

2) Manufacturing Equipment

Manufacturing equipment of high precision and stability is used not only to minimize failure rates, but also to reduce the drift in characteristics and to improve the reliability. In addition, automated equipment is used everywhere possible to prevent human errors. This method has proved to be effective especially in the manufacturing of devices and quality inspection. As the maintenance of the manufacturing equipment is essential to keep the stabilized quality, daily check, and periodical check are standarized to keep the precision and to insure normal operation of the equipment. Thus, special care is paid to keep the equipment in its best conditions.

3) Manufacturing Conditions

NEC enforces check of processing conditions everywhere in the manufacturing process in order to perform perfect control of the manufacturing conditions. This is to prevent erroneous processings and malfunctioning of the manufacturing equipment, and is effective for the speedy adjustment of the misprocessing, supported by the intermediate inspection. This check is also executed at the key points in the course of processing on the most effective items at the most effective frequency. Necessary measures are immediately taken according to the check results. The results of check and measures taken are kept in records, which are utilized as the data for the improvement of process control.

4) Manufacturing Environment

Temperature, humidity and dust are important factors influencing the quality. Semiconductor devices are sensitive to these factors, so the stringent control is applied to keep these factors within the required limits throughout the manufacturing processes. Humidity is a quite important factor, since contaminating even the least amount of water influences the quality of the semiconductor devices seriously. Some processings that require an extremely low humidity are carried out in a dry box maintaining the necessary low humidity. Small dirt and dust often affect the semiconductor devices having a minute structure seriously. Therefore, a stringent control corresponding to each grade is necessary to prevent them. In the factory, a control based on sti-

pulations of Fed-STD-209a is applied. For processings that require a specifically high cleanliness, clean room, clean bench, uniform of special make, etc. are adopted. Periodic measurement of dust and dirt in the room and over the clean bench is conducted, and if they do not meet the standards, the processings are stopped or improved.

5) Screening

As the semiconductor element devices have generally sensible structure, even if they may be made under a strict quality control and on a high grade line, some substandard devices which do not meet the quality standards would inevitably be mixed with those of standard quality due to the distribution of materials and parts and processings, as well as the inaccuracy of the manufacturing equipment and other various causes. In order to detect and remove these substandard products, screening is performed.

The screening is classified into two, i.e., an accelerated aging and characteristic selection. The accelerated aging stabilizes characteristics and at the same time detects substandard products by applying voltage, heat, mechanical shock of specified value. After the aging, a complete inspection is performed by physical or electrical measurement to remove substandard products. The screening can remove substandard products which can not be removed only by the characteristic inspection and tends to degrade the quality. Since the stability of characteristics of entire products is increased by the screening, the reliability is effectively improved by it.

3-7. Inspection and Other Quality Assurance Activities

1) Inspection and Quality Assurance Activities

In the manufacture of semiconductor devices, NEC has been making a full and continuous effort in building reliability into the products as has been described above. For this purpose, NEC performs various controls putting emphasis on the key points throughout the entire manufacturing processes, and verifies and assures the quality at the final examination. A variety of automatic measuring instruments is used for the intermediate test in the manufacturing process to obtain high efficiency and at the same time to exclude human errors. Results of the inspection are fed back to the preceeding process as an important quality information to improve the manufacturing procedures.

At the final stage of the manufacturing process, quality assurance test and warehousing inspection are performed to assure the reliability and quality of the products.

In general, the quality assurance test is roughly classified into two, i.e., initial stage characteristic test which assures external view, outline dimension, electrical characteristics and so on, and reliability test which assures life, failure rates, mechanical strength and so on. These tests are performed for almost all of the characteristics to be assured usually. However, when the distribution of characteristics sufficiently surpasses the standards or when the cost of the test is extremely high, the tests are sometimes simplified. Even in this case, verfification test is performed periodically at an appropriate interval. Inspection method and inspection item of the quality assurance test and warehousing inspection as the final inspection differ depending on the feature of the products and user's requirements. An example which is closest to the standard test method is shown in Table 3.

Table 3. Sampling Inspection Plan and Average Outgoing Quality for Initial Characteristics

Classification	Item	*Sampling Inspection Plan	Acceptance Limit	Average Outgoing Quality
Major Defect	No Marking, Wrong Configuration Open, Short, etc.	LTPD 1 %	0	AOQ 0.02 %
	Item that affect Reliability most strongly (Breakdown Voltage, Leakage Current, etc.)	LTPD 3 %	1	AOQ 0.3 %
Minor Defect	Item that affect Dynamic Characteristic most strongly, and also affect Reliability (h_{FE}, $V_{CE(sat)}$, NV, etc.)	LTPD 5 %	1	AOQ 0.5 %
	Item that not affect Reliability much, but affect Dynamic Characteristics (f_T, C_{ob}, etc.)	LTPD 7 %	1	AOQ 1 %
	Item that not affect Reliability or Dynamic Characteristic much (Appearance, etc.)	LTPD 10 %	1	AOQ 2 %

* by MIL-STD-19500 Sampling Inspection Table

2) Other Quality Assurance Activities

Quality control system for the manufacturing of semiconductor devices is as described above, and a number of other quality control activities associated with the system are performed. Of these, a few major activities will be explained below.

(a) Periodic Process Test

Manufacturing process test is performed 1~2 times a month for the purpose of checking the actual condition of standard processing and maintenance condition of the manufacturing equipment and measuring instrument. In this test, the detection and adjustment of discrepancy between the specified processing and actual processing, as well as the check of periodical maintenance and calibration of the manufacturing equipment and measuring instruments are performed. In addition, manufacturing environments such as temperature, humidity, water, gas, dust, etc. are also periodically inspected.

(b) Utilization of Work History

Work history in the manufacturing process is recorded in the work history card. The record is utilized as follows:

(i) Investigation of control condition and feed back of the results to the relevant area
(ii) Analysis of process quality drift
(iii) Analysis of manufacture total yield rate drift
(iv) Statistical investigation of process yield rate
(v) Statistical investigation of manufacture total yield rate
(vi) Lot tracing investigation of rejected devices returned from users
(vii) Statistical control of the loss.

(c) Control of Abnormality

When any abnormality occurred in any stage of incoming, manufacturing and final inspections, it is reported immediately to the reliability and quality control department and also to every other department concerned, and immediate counter-measures are taken.

Figure 9 shows abnormality reporting route. Abnormal lot determination standard is established based on the lot distribution status and reliability. Even after the establishment of the standard, it is periodically checked up with the process capability, and its appropriateness is examined.

Quality control of semiconductor devices in the

manufacturing process has been outlined above, and the quality control system is shown in Figure 10.

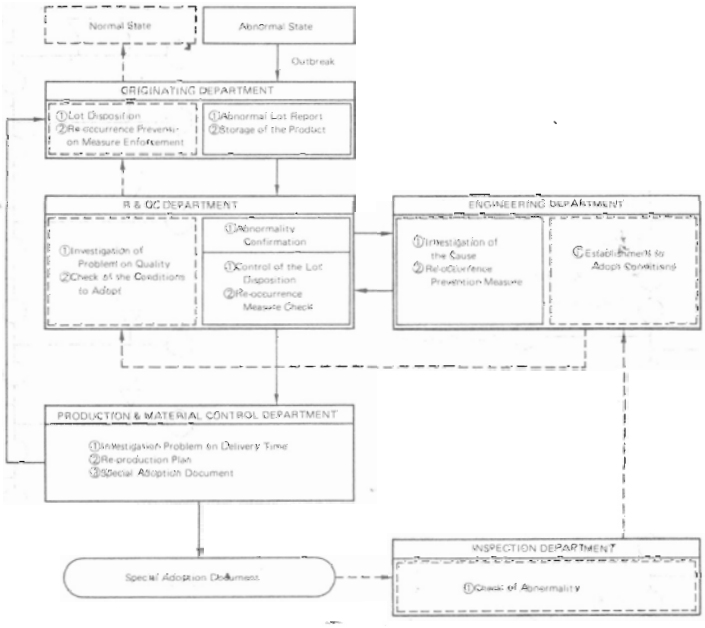


Figure 9. Abnormality Reporting Route

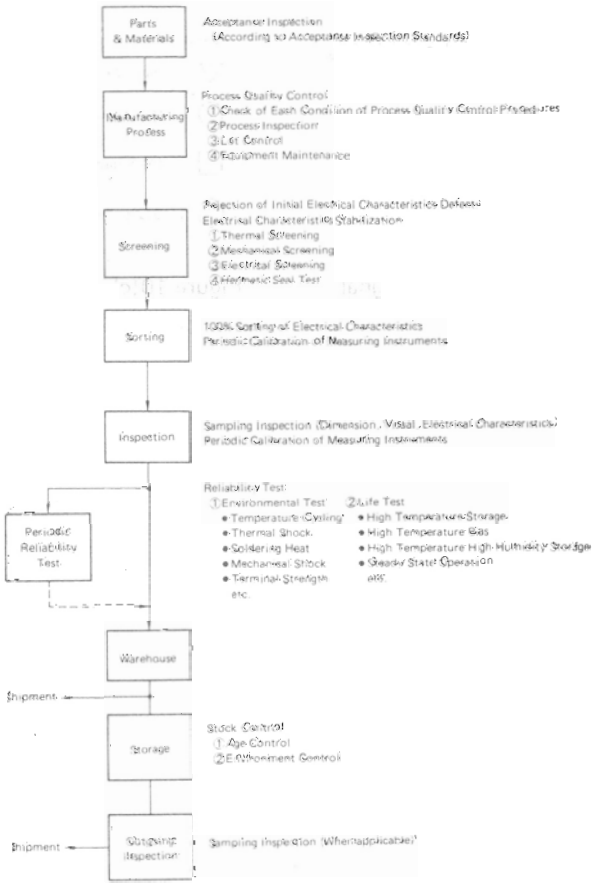


Figure 10(a) General Process Flow Chart

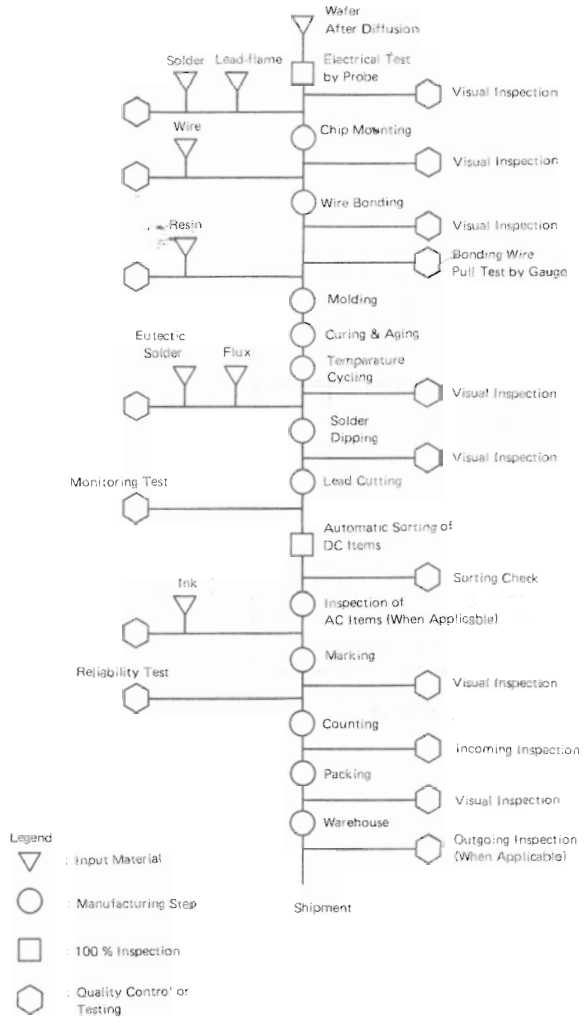


Figure 10(b) Manufacturing Process of Small Signal Transistors

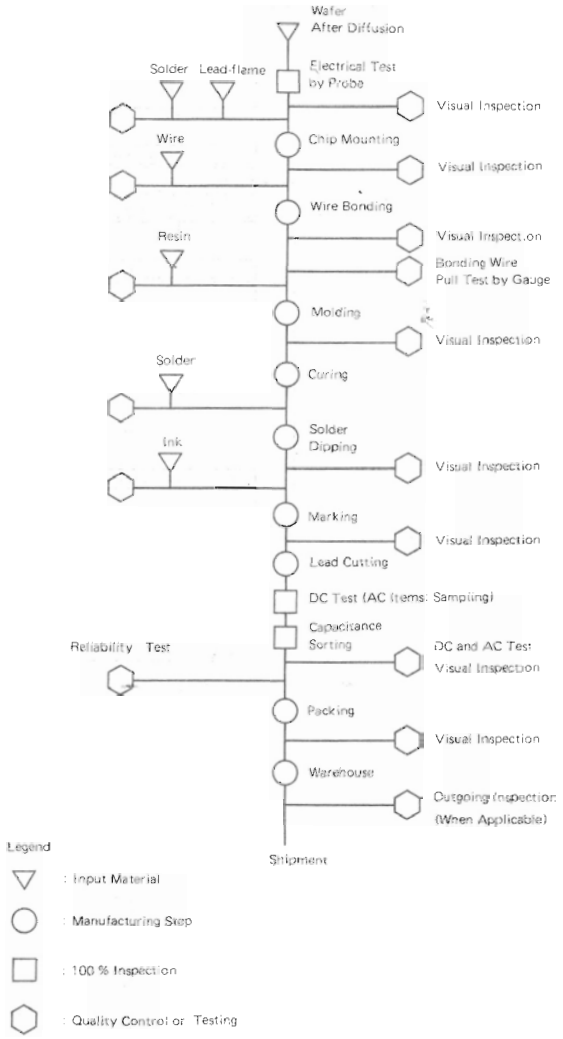


Figure 10(c) Manufacturing Process of Plastic Molded Diodes

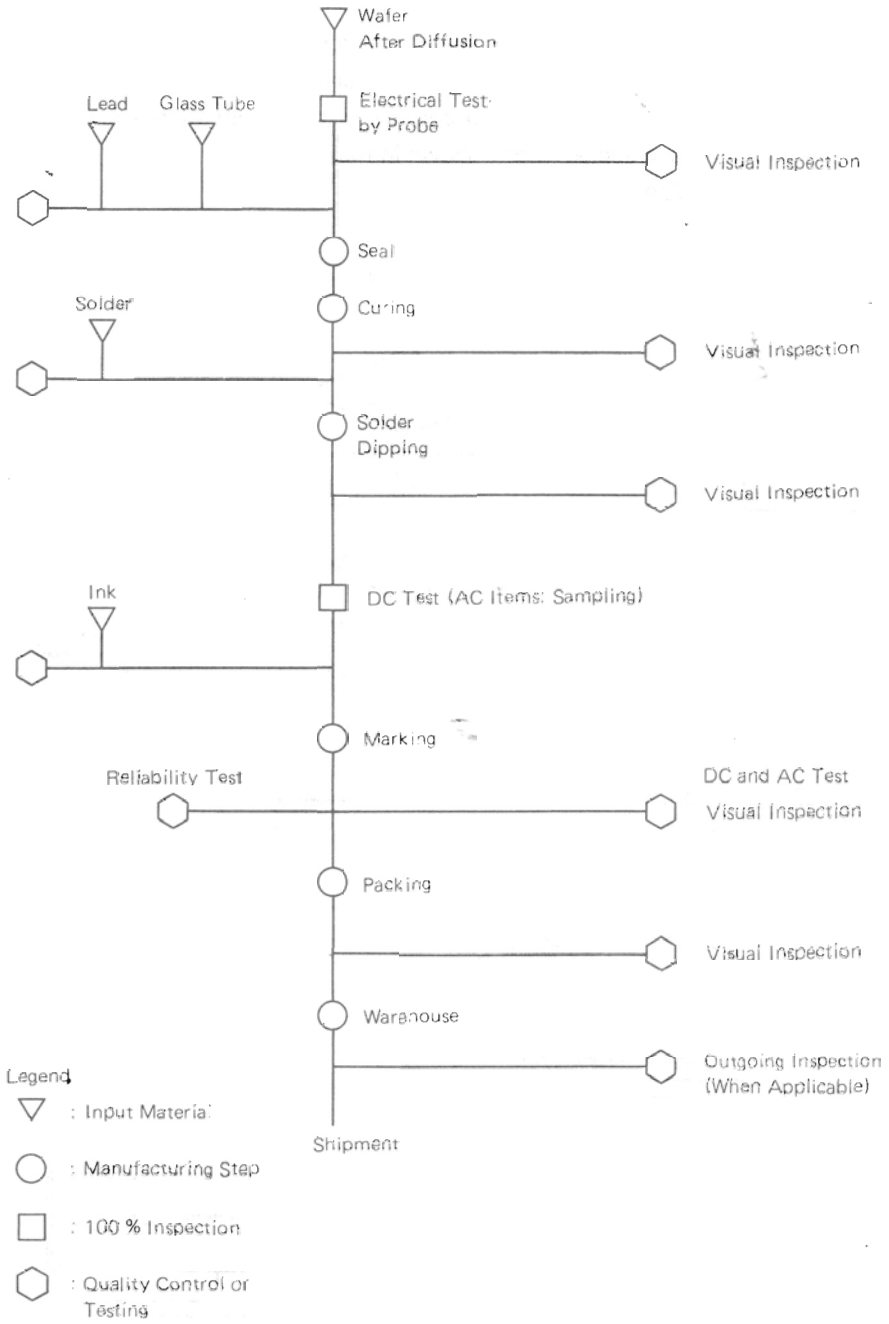


Figure 10(d) Manufacturing Process of Glass Package Diodes

(d) Control System of Engineering Changes

In order that our semiconductor devices may be used with satisfaction by our customers, needless to say stable level of reliability must always be maintained, and in addition, we deem that the improvement of reliability to keep up with the requirements of the times is also an important factor.

In order to create a stable reliability level, strict reliability and quality assurance control is exercised through the aggregation of the feed-forward and feed-back of date of the principal processes that affect the reliability of products, the adoption of improved production methods and structural materials for semiconductor devices in step with the advances of technology, and the study of field data. However, we never rest satisfied with once established standards and are constantly making ef-

forts to improve the reliability of products to meet the requirements of our customers.

When undertaking revisions of the design or manufacturing processes that are brought about by the above improvements, basically the problem is grappled with employing the same idea as when developing and mass producing new product, and thorough evaluation and starting-up control are exercised. Changes in the control system brought about by the above revisions will differ according to the extent of the revision, an example is shown in Figure 11.

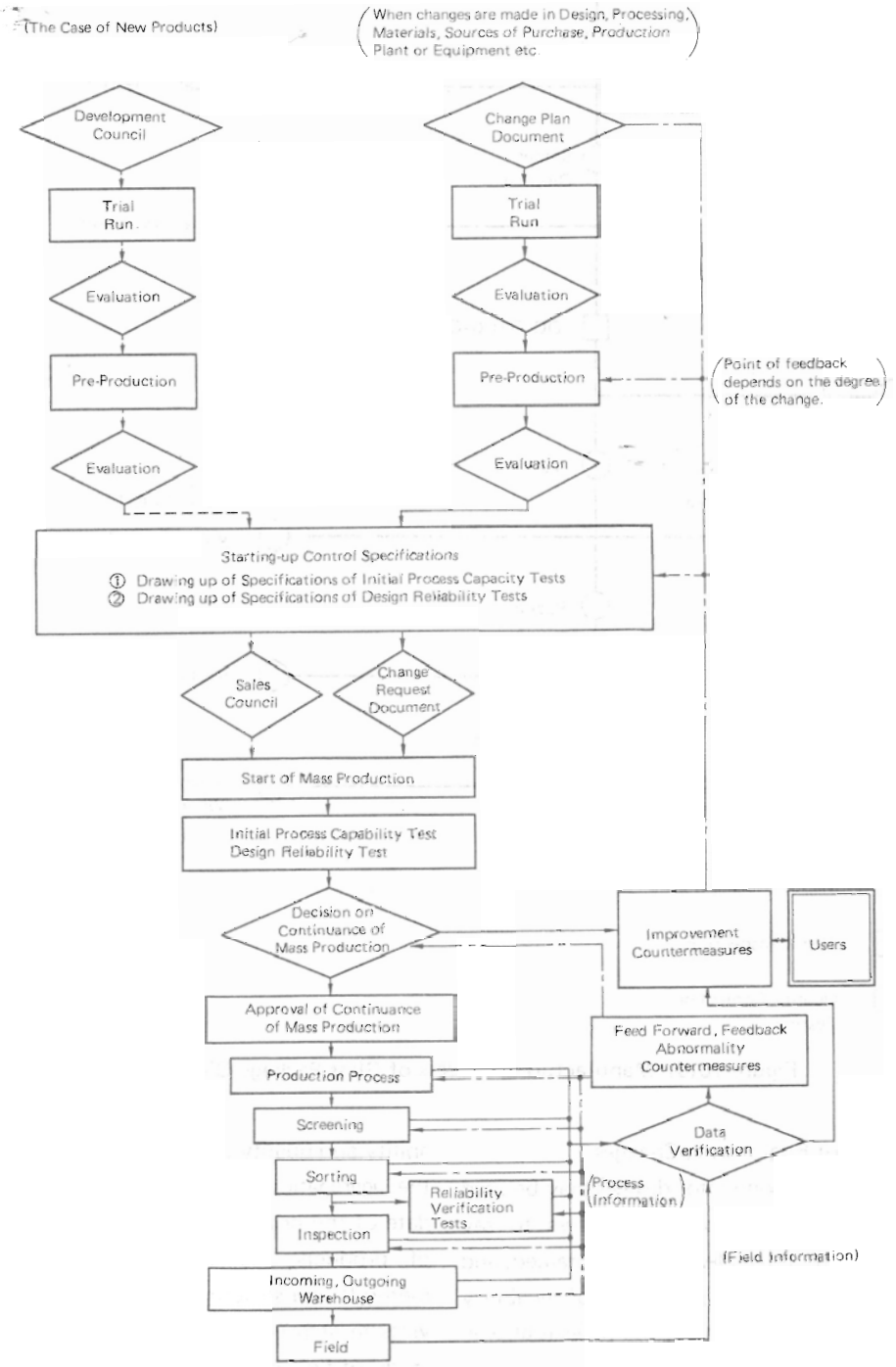


Figure 11. Control System for Engineering Changes

3-8. Shipment

Products which passed the final inspection are put in a container suitable for storage. Each container accommodates a fixed number of products and is stored in the product warehouse. These products are controlled so that they are not stored in the warehouse too long. For shipment, outgoing inspection is performed based on the specification which is set with due care for the quality degradation. Devices are packed up in due method such as individual divice packing, internal and external packing, and are transported in such a best way appropriate for delivery.

The control status of storage and shipment is checked by periodic patrol of the quality control department to find out problems and to correct them.

3-9. After-Sale Service

Field quality information after shipment is an essential factor for improvement of product quality. Especially, investigation of field failure and feed back of the investigation results are the duty and service for customers and also these data serve as direct guides to the improvement of reliability and quality. So best effort has been made on this point.

Devices which have failed after shipment are returned by user's requirement or NEC request. Sales department investigates in detail the devices used, circuit, process to the failure, and failure occurring condition, and makes failure investigation card. The card is sent to the investigation department together with the device failed.

The investigation department investigates characteristics of the returned device and its internal structure to probe into the cause of the failure. The results of the investigation are fed back to the user and departments in charge of manufacture, to obtain a user's consent and to be used for the improvement of quality. Figure 12. shows the route of these processings. Collection of information, investigation and summing up of field failures of semiconductor devices are carried out with cooperation of users, and a large amount of data have been accumulated. Correlation between these data and forced deterioration test, process quality information, inspection results and so on are studied, and good results have been obtained in improving reliability and quality of products.

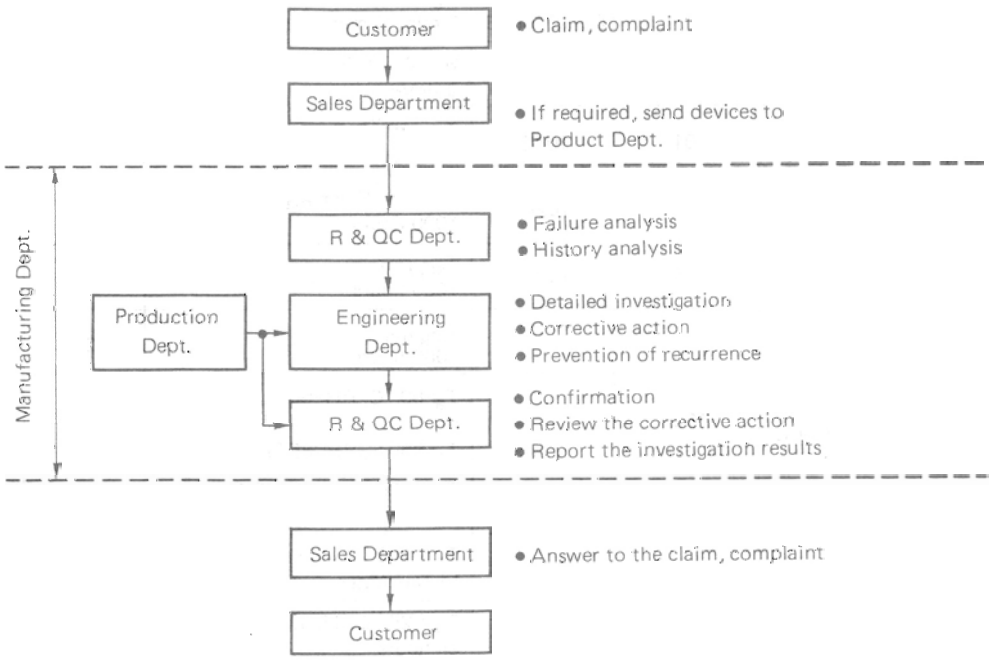


Figure 12. Procedure Route for Claim and Complaint

4. RELIABILITY OF NEC SEMICONDUCTOR DEVICES

4-1. Reliability Test

As described in preceding paragraph, NEC semiconductor devices are designed, manufactured, managed so as to maintain high reliability and quality. Method of reliability test to be performed to verify the reliability will be described below.

The reliability test of semiconductor devices is executed mainly in accordance with MIL-STD-750, MIL-STD-202, JIS C 7021, etc. Especially for the semiconductor devices, accelerated operating life test at maximum rating is performed, putting emphasis on important points. In addition, high temperature high humidity test and pressurized vapor test are applied as moisture resistance test for the plastic package of which material characteristic is rather important.

4-2. Example of Reliability Test Result

Following data show the reliability test results of NEC semiconductor devices.

These test data are evaluated as a whole together with the number of failures and check results of the characteristic drift occuring as time elapses, and are used for the estimation of field failure rates.

Table 4. Reliability Test (Small Signal Transistors)
(a) Example of Reliability Test (Small Signal Transistors)

Item	Applied Test Method JIS C 7021	Correlative Test Method		Condition	Number of Samples /Lot	Acceptance Number Ac =
		MIL-STD-202	MIL-STD-750			
Solderability	A–2	208	2026	T_{sol} = 230 °C, 5 s. Once with Flux	22	0
Soldering Heat	A–1 Condition: A	210 Condition: B	2031	T_{sol} = 260 °C, 10 s. Once without Flux	22	0
Temperature Cycling	A–4	107	1051	T_{stg} min. ~ T_{stg} max. 30 min., 30 min. 30 cycles	100	0
Thermal Shock	A–3 Method: II	–	1056 Condition: B	T_a = 100 ~ 0 °C 5 min., 5 min., 5 cycles	22	0
Terminal Strength (Lead Fatigue)	–	211 Condition: C	2036 Condition E	W = 227 g, 90 ° 3 times	11	0
Salt Spray	A–12 Condition: B	101	1042	T_a = 35 °C, 5 % 24 hours	11	0
Steady-State Operation	B–4	–	1026	T_a = 25 °C, P_T max. 1000 hours	20	0
High Temperature Storage	B–10	108	1031	T_{stg} max. 1000 hours	20	0
Low Temperature Storage	B–12	–	–	T_{stg} min. 1000 hours	20	0
High Temperature High Humidity Storage	B–11 Condition: B or C	103	–	T_a=60 °C, RH=90 %, 1000 hours or T_a=85 °C, RH=85 %, 500 hours	20	0
Pressure * Cooker	–	–	–	T_a = 125 °C, RH=100 % 2.3 atm., 24 hours	22	0
Boiling *	–	–	–	T_a = 100 °C, 24 hours In Tap Water	22	0
Bomb *	–	–	–	T_a = 25 °C, 3.5 atm. 24 hours	22	0
High Temperature* Reverse Bias	B–8	–	–	T_{stg} max., 1000 hours V_{CB} max. x 0.8	20	0

* When applicable, this test is performec.

(b) Failure Criterion (Small Signal Transistors)

Parameter	Symbol	Life End Limit		Unit
		MIN.	MAX.	
Collector Cutoff Current	I_{CBO}	–	USL x 2	μA
Emitter Cutoff Current	I_{EBO}	–	USL x 2	μA
DC Current Gain	h_{FE}	LSL x 0.8	USL x 1.2	–
h_{FE} Variation Ratio	Δh_{FE}	–25	+50	%

Note 1) USL: Upper Specification Limit
2) LSL: Lower Specification Limit
3) Δh_{FE} = Initial Value/After Test Value

(c) Environmental Test Result (Small Signal Transistors)

Item	Condition	Type No.			
		2SC945		2SA733	
		Number of Samples	Number of Failure	Number of Samples	Number of Failure
Solderability	T_{sol}=230 °C, 5 s Once with Flux	352	0	352	0
Soldering Heat	T_{sol} = 260 °C, 5 s Once without Flux	352	0	352	0
Temperature Cycling	T_{stg} = –55 ~ +125 °C 30 min., 30 min., 30 cycles	1600	0	1600	0
Thermal Shock	T_a = 0 ~ 100 °C 5 min., 5 min., 5 cycles	352	0	352	0
Terminal Strength (Lead Fatigue)	W=227 g, 90 ° 3 times	176	0	176	0
Salt Spray	T_a=35 °C, 5 % 24 hours	176	0	176	0
Pressure Cooker	T_a = 125 °C, RH = 100 % 2.3 atm., 24 hours	660	0	660	0
Boil	T_a = 100 °C, 24 hours Tap Water	1320	0	1320	0
Bomb	T_a = 25 °C, 3.5 atm. 24 hours	1320	0	1320	0

(d) Life Test Result (Small Signal Transistors)

Item	Condition **	2SC945				2SA733			
		Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)	Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)
Steady-State Operation	T_a = 25 °C, P_T = 250 mW V_{CB} = 25 V, 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
High Temperature Storage	T_a = 125 °C, 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
Low Temperature Storage	T_a = –55 °C, 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
High Temperature High Humidity Storage	T_a = 60 °C, RH = 90 % 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
High Temperature Reverse Bias	T_a = 125 °C, V_{CB} = 25 V 1000 hours	600	0.6×10^6	0	0.150	600	0.6×10^6	0	0.150

* Confidence Level : 60 %
** Negative sign for PNP type is omitted.

Table 5. Reliability Test (Power Transistor)

(a) Example of Reliability Test (Power Transistor)

Item	Applied Test Method JIS C 7021	Correlative Test Method MIL-STD-202	Correlative Test Method MIL-STD-750	Condition	Number of Samples /Lot	Acceptance Number Ac=
Solderability	A–2	208	2026	T_{sol}=230 °C, 5 s Once with Flux	22	0
Soldering Heat	A–1 Condition: A	210 Condition: B	2031	T_{sol}=260 °C, 10 s Once without Flux	22	0
Temperature Cycling	A–4	107	1051	T_{stg} min.~ T_{stg} max. 30 min., 30 min. 5 cycles	22	0
Thermal Shock	A–3 Method: 11	–	1056 Condition: B	T_a=100~0 °C 5 min., 5 min., 5 cycles	22	0
Terminal Strength (Lead Fatigue)	–	211 Condition: C	2036 Condition: E	W=227 g, 90 ° 3 times	11	0
Salt Spray	A–12 Condition: B	101	1042	T_a=35 °C, 5 % 24 hours	11	0
Steady-State Operation	B–4	–	1026	T_a=25 °C, P_T max. 1000 hours	20	0
High Temperature Storage	B–10	108	1031	T_{stg} max. 1000 hours	20	0
High Temperature High Humidity Storage	B–11 Condition: B or C	103	–	T_a=85 °C, RH=85 %, 1000 hours	20	0
Pressure Cooker	–	–	–	T_a=125 °C, RH=100 % 2.3 atm., 24 hours	22	0
High Temperature Reverse Bias	B–8	–	–	T_{stg} max., 1000 hours V_{CB} max. x 0.8	20	0

(b) Failure Criterion (Power Transistor)

Parameter	Symbol	Life End Limit MIN.	Life End Limit MAX.	Unit
Collector Cutoff Current	I_{CBO}	–	USL x 2	μA
Emitter Cutoff Current	I_{EBO}	–	USL x 2	μA
DC Current Gain	h_{FE}	LSL x 0.8	USL x 1.2	–
h_{FE} Variation Ratio	Δh_{FE}	–25	+50	%

Note 1) USL: Upper Specification Limit
2) LSL: Lower Specification Limit
3) Δh_{FE} = Initial Value/After Test Value

(c) Environmental Test Result (Power Transistor)

Item	Condition	Type No.			
		2SB1098		2SD1589	
		Number of Samples	Number of Failure	Number of Samples	Number of Failure
Solderability	T_{sol}=230 °C, 5 s Once with Flux	352	0	352	0
Soldering Heat	T_{sol}=260 °C, 5 s Once without Flux	352	0	352	0
Temperature Cycling	T_{stg}=−55~+125 °C 30 min., 30 min., 30 cycles	1600	0	1600	0
Thermal Shock	T_a=0~100 °C 5 min., 5 min., 5 cycles	352	0	352	0
Terminal Strength (Lead Fatigue)	W=227 g, 90 ° 3 times	176	0	176	0
Salt Spray	T_a=35 °C, 5 % 24 hours	176	0	176	0
Pressure Cooker	T_a=125 °C, RH=100 % 2.3 atm., 24 hours	352	0	352	0

(d) Life Test Result (Power Transistor)

Item	Condition **	2SA1220				2SC2690			
		Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)	Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)
Steady-State Operation	T_a=25 °C, P_T=1.0 W V_{CB}=70 V, 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
High Temperature Storage	T_a=150 °C, 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
High Temperature High Humidity Storage	T_a=85 °C, RH=85 % 1000 hours	1200	1.2×10^6	0	0.076	1200	1.2×10^6	0	0.076
High Temperature Reverse Bias	T_a=150 °C, V_{CB}=120 V 1000 hours	600	0.6×10^6	0	0.150	600	0.6×10^6	0	0.150

* Confidence Level: 60 %
** Negative sign for PNP type is omitted.

Table 6. Reliability Test (Plastic Molded Diodes)

(a) Example of Reliability Test (Plastic Molded Diodes)

Item	Applied Test Method JIS C 7021	Correlative Test Method		Condition	Number of Samples /Lot	Acceptance Number Ac =
		MIL-STD-202	MIL-STD-750			
Solderability	A–2	208	2026	T_{sol}=230 °C, 5 s Once with Flux	22	0
Temperature Cycling	A–4	107	1051	T_{stg} min. ~ T_{stg} max. 30 min., 30 min. 30 cycles	22	0
Thermal Shock	A–3 Method: II	–	1056 Condition: B	T_a = 100 ~ 0 °C 5 min., 5 min., 5 cycles	22	0
Mechanical Shock	A–7 Condition: F	213	2016	1500G, 0.5 ms., 3 times Each direction of X, Y and Z Axis	22	0
Vibration (Variable Frequency)	A–10 Condition: D	–	2056	100 ~ 2000 ~ 100 Hz, 20 G 4 min., 4 times, Each direction	22	0
Terminal Strength (Lead Fatigue)	–	211 Condition: C	2036 Condition: E	W = 227 g, 90 ° 3 times	11	0
Salt Spray	A–12 Condition: B	101	1041	T_a = 35 °C, 5 % 24 hours	11	0
High Temperature Storage	B–10	108	1031	T_{stg} max. 1000 hours	20	0
Low Temperature Storage	B–12	–	–	T_{stg} min. 1000 hours	20	0
High Temperature Reverse Bias	B–13	–	–	Specified V_R, T_a 1000 hours	20	0
High Temperature High Humidity Reverse Bias	–	–	–	Specified V_R, T_a, RH 1000 hours	20	0

(b) Failure Criterion (Plastic Molded Diodes)

Parameter	Symbol	Life End Limit		Unit
		MIN.	MAX.	
Reverse Current	I_R	–	USL x 2	μA
Forward Voltage	V_F	–	USL x 1.1	V

Note USL : Upper Specification Limit

(c) Environmental Test Result (Plastic Molded Diodes)

Item	Condition	1S2208 (B)	
		Number of Samples	Number of Failure
Solderability	T_{sol} = 230 °C, 5 s Once with Flux	286	0
Temperature Cycling	T_{stg} = −65 ~ +125 °C 30 min., 30 min., 5 cycles	286	0
Thermal Shock	T_a = 0 ~ 100 °C 5 min., 5 min., 5 cycles	286	0
Mechanical Shock	1500G, 0.5 ms., 3 times Each direction of X, Y and Z Axis	286	0
Vibration (Variable Frequency)	100 ~ 2000 ~ 100 Hz, 20G 4 min., 4 times Each direction of X, Y and Z Axis	286	0
Terminal Strength (Lead Fatigue)	W=227 g, 90 ° 3 times	143	0
Salt Spray	T_a = 35 °C, 5 % 24 hours	143	0

(d) Life Test Result (Plastic Molded Diodes)

Item	Condition	Type No. 1S2208 (B)			
		Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)
High Temperature Storage	T_a = 125 °C, 1000 h	260	2.6×10^5	0	0.35
Low Temperature Storage	T_a = −65 °C, 1000 h	260	2.6×10^5	0	0.35
High Temperature Reverse Bias	T_a = 125 °C, V_R = 28 V 1000 h	260	2.6×10^5	0	0.35
High Temperature High Humidity Reverse Bias	T_a = 40 °C, RH = 90 % V_R = 28 V, 1000 h	260	2.6×10^5	0	0.35

* Confidence Level : 60 %

Table 7. Reliability Test (Glass Package Diodes)
(a) Example of Reliability Test (Glass Package Diodes)

Item	Applied Test Method JIS C 7021	Correlative Test Method		Condition	Number of Samples /Lot	Acceptance Number Ac =
		MIL-STD-202	MIL-STD-750			
Soldering Heat	A–1 Condition: A	210 Condition: B	2031	T_{sol}=260 °C, 10 s Once without Flux	22	0
Temperature Cycling	A–4	107	1051	T_{stg} min. ~ T_{stg} max. 30 min., 30 min. 5 cycles	22	0
Thermal Shock	A–3 Method: II	–	1056 Condition: B	T_a = 100 ~ 0 °C 5 min., 5 min., 5 cycles	22	0
Moisture Resistance (Cyclic)	A–5 Method: I	106	1021	Specified Condition (T_a, RH), 10 cycles	22	0
Mechanical Shock	A–7 Condition: F	213	2016	1500G, 0.5 ms., 3 times Each direction of X, Y and Z Axis	22	0
Vibration (Variable Frequency)	A–10 Condition: D	–	2056	100 ~ 2000 ~ 100 Hz, 20 G 4 min., 4 times, Each direction of X, Y and Z Axis	22	0
Constant Accelation	A–9 Condition: A	212	2006	20000G, 1 min. Each direction of X, Y and Z Axis	22	0
Terminal Strength (Lead Fatigue)	–	211 Condition: C	2036 Condition: E	W = 227 g, 90 ° 3 times	11	0
Salt Spray	A–12 Condition: B	101	1041	T_a = 35 °C, 5 % 24 hours	11	0
Steady-State Operation	B–2	–	1026	T_a = 25 °C Specified I_O, V_R 1000 hours	20	0
High Temperature Storage	B–10	108	1031	T_{stg} max. 1000 hours	20	0
Low Temperature Storage	B–12	–	–	T_{stg} min. 1000 hours	20	0

(b) Failure Criterion (Glass Package Diodes)

Parameter	Symbol	Life End Limit		Unit
		MIN.	MAX.	
Reverse Current	I_R	–	USL x 2	μA
Forward Voltage	V_F	–	USL x 1.1	V

Note USL : Upper Specification Limit

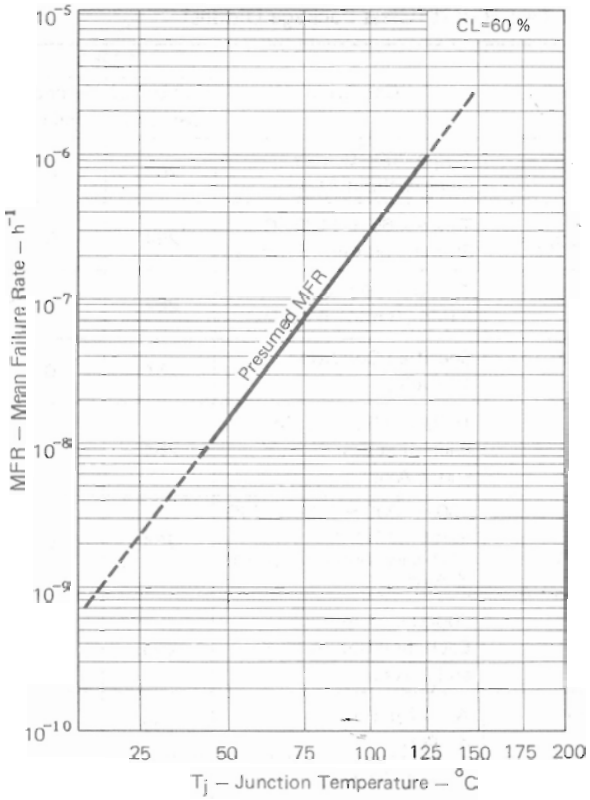
(c) Environmental Test Result (Glass Package Diodes)

Item	Condition	1S953		1SS53	
		Number of Samples	Number of Failure	Number of Samples	Number of Failure
Soldering Heat	T_{sol} = 260 °C, 10 s Once without Flux	264	0	264	0
Temperature Cycling	T_{stg} = −65 ~ +125 °C 30 min., 30 min., 5 cycles	264	0	264	0
Thermal Shock	T_a = 0 ~ 100 °C 5 min., 5 min., 5 cycles	264	0	264	0
Moisture Resistance (Cyclic)	Specified Condition 10 cycles	264	0	264	0
Mechanical Shock	1500G, 0.5 ms., 3 times Each direction of X, Y and Z Axis	264	0	264	0
Vibration (Variable Frequency)	100 ~ 2000 ~ 100 Hz, 20G 4 min., 4 times Each direction of X, Y and Z Axis	264	0	264	0
Constant Accelation	20000 G, 1 min. Each direction of X, Y and Z Axis	264	0	264	0
Terminal Strength (Lead Fatigue)	W=227 g, 90 ° 3 times	132	0	132	0
Salt Spray	T_a = 35 °C, 5 % 24 hours	132	0	132	0

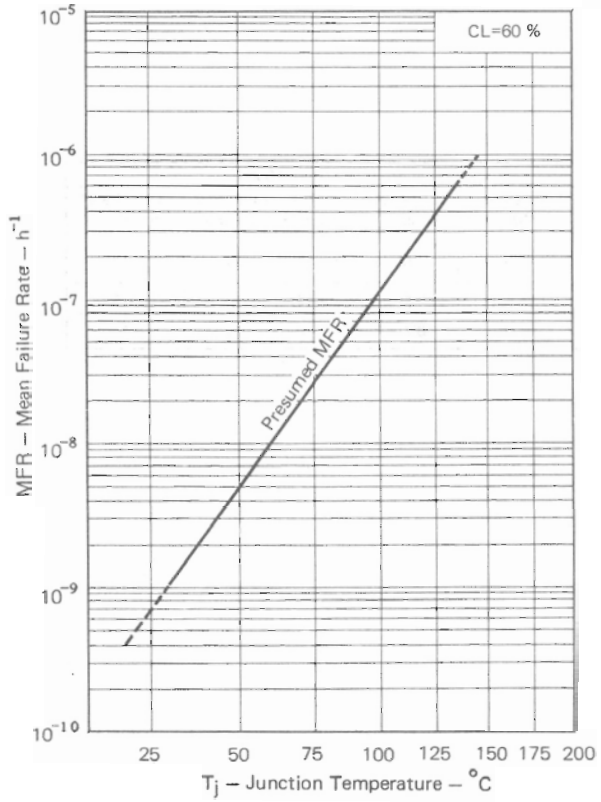
(d) Life Test Result (Glass Package Diodes)

Item	Condition	1S953				1SS53			
		Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)	Number of Samples	Total Test Time (h)	Number of Failure	Failure Rate* (%/1000 h)
Steady-State Operation	T_a = 25 °C, I_O = 100 mA V_R = 35 V, 1000 hours	560	5.6×10^5	0	0.16	880	8.8×10^5	0	0.10
High Temperature Storage	T_a = 200 °C, 1000 hours	560	5.6×10^5	0	0.16	1520	15.2×10^5	0	0.06
Low Temperature Storage	T_a = −65 °C, 1000 hours	560	5.6×10^5	0	0.16	680	6.8×10^5	0	0.13

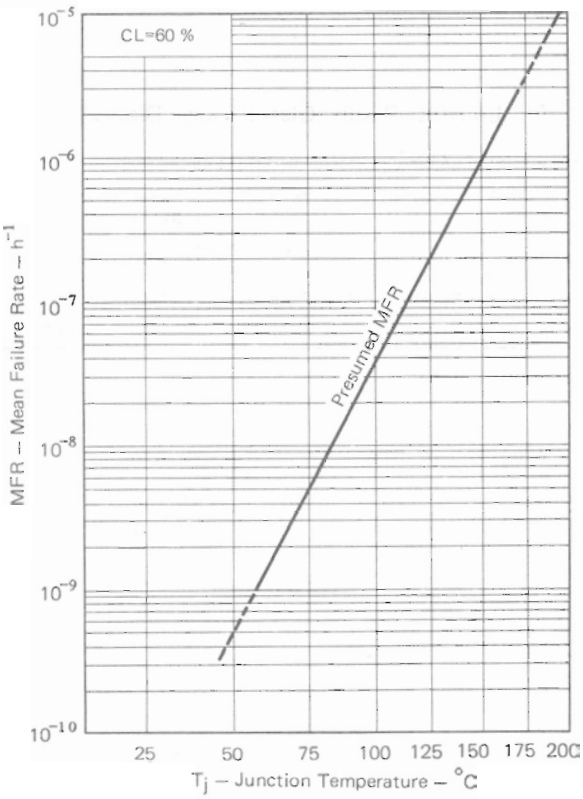
* Confidence Level : 60 %



(a) Small Signal Transistors



(b) Plastic Molded Diodes



(c) Glass Package Diodes

Figure 13. Presumed Mean Failure Rate

4-3. Procedure of Failure Analysis

We analyze the failed semiconductor devices found in manufacturing process, reliability verification test and field use by following procedure in Figure 14.

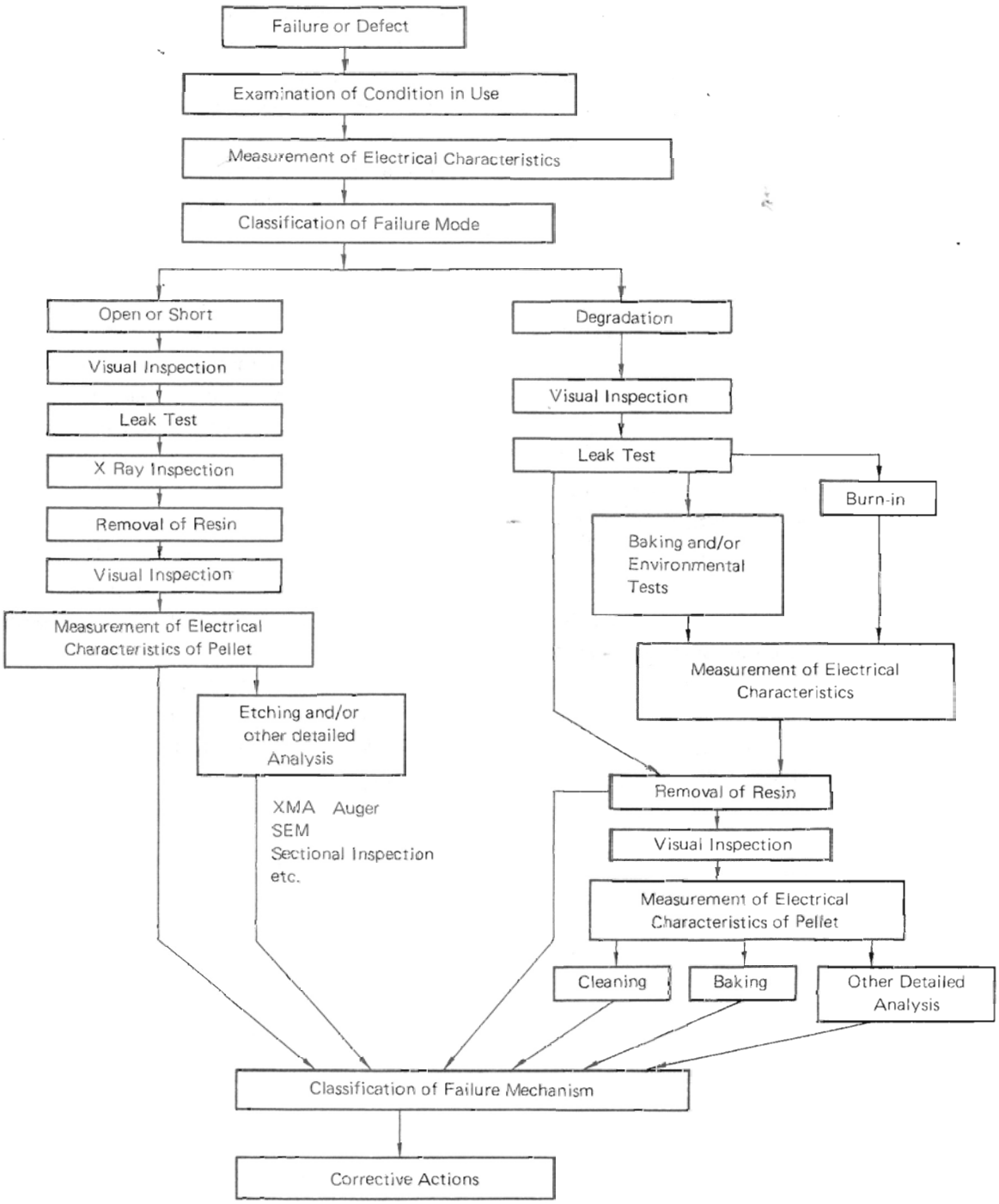


Figure 14. Procedure of Failure Analysis

5. USE OF SEMICONDUCTOR DEVICES TO MAINTAIN RELIABILITY

External factors that influence reliability of semiconductor devices are voltage, current, power, temperature, humidity, dust, gas, vibration, shock, radiation, etc. Influential factors are so varied that if the devices are used improperly, expected reliability will not come true, no matter how reliably they were designed and manufactured.

As shown in Figure 6, 1/3~2/3 of the failed semiconductor devices in use were chiefly damaged by some surge or other, and this is consipicuous among the failures. Therefore, careful attention should be given to the following points in order to use the devices, without hurting their inherent reliability.

(1) The most important factor influencing the reliability of the devices is the temperature generated at the junction region in actual applications. Therefore, for the increase of reliability, it is very effective to enhance heat dissipation capability by using radiators or to decrease temperature rise in an equipment by improving the mounting of devices.

(2) When power consumption is performed in pulses, it is necessary to see that the power or voltage does not exceed the absolute maximum ratings of the devices at the transient. In particular, when inductive loads such as relays or transformers are used, induced high voltage or surge is liable to be generated at ON-OFF operation of such devices. So it is very important to pay special attention to these points. Some devices have protection circuits to meet these conditions.

(3) When power consumption is the same, a high operating voltage usually causes a high failure rate. An example shows that when the voltage applied to a transistor was decreased to 50 % of absolute maximum rating, the failure rate reached 1/20 ~ 1/50.

(4) It is absolutely necessary to avoid bending strongly the roots of leads of semiconductor devices when assembling or checking them. It is because glass or resin is always used at the roots of these leads. If stress is given to those parts, the reliability of the devices will be deteriorated.

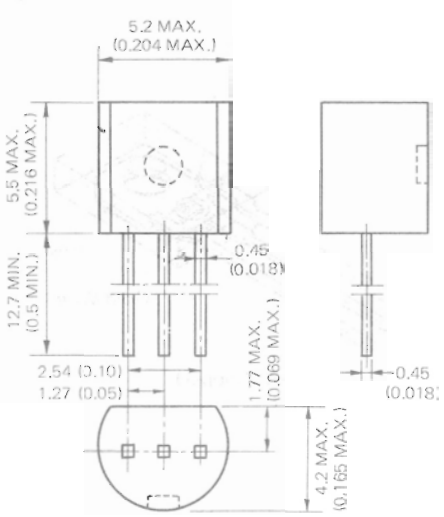
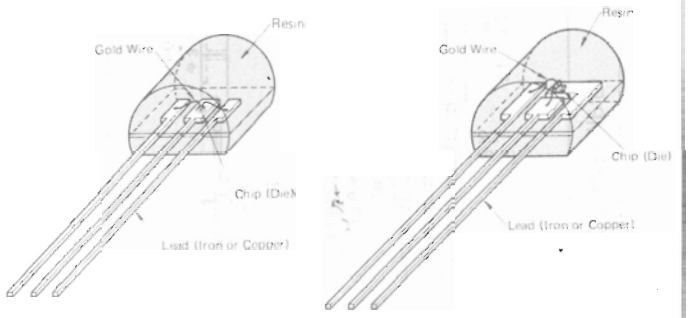
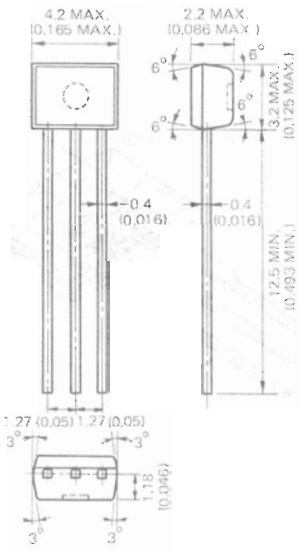
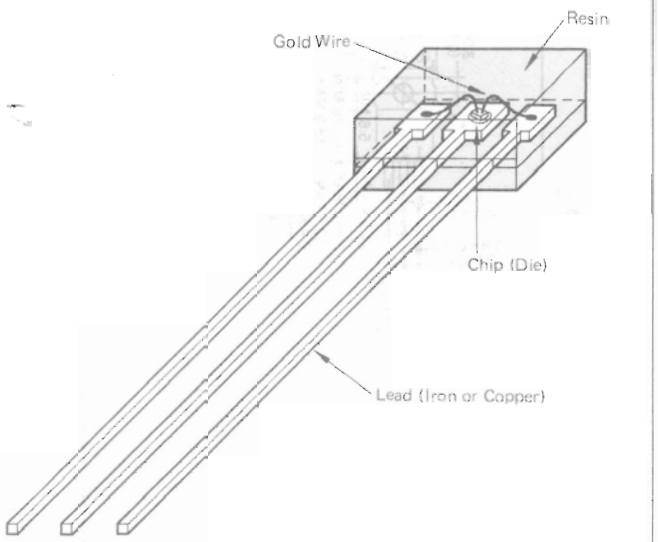
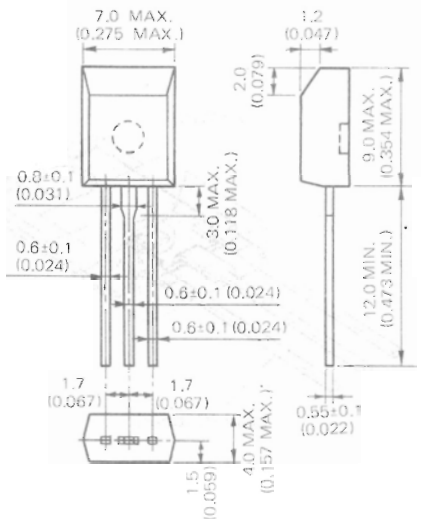
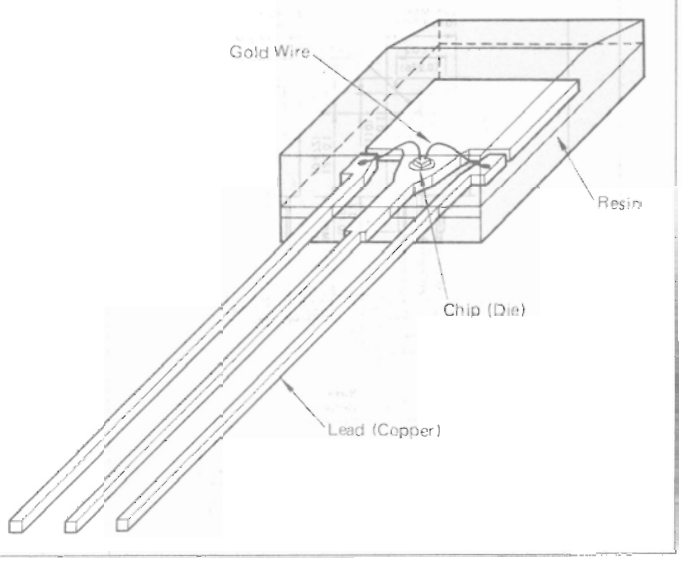
(5) In soldering, semiconductor devices must not be heated hastily at a high temperature or for a long time.

(6) For the semiconductor devices with mounting stud, the recommended torque value must be observed by using a torque wrench or other means; because too weak fastening will cause poor heat dissipation, and too strong fastening will cause semiconductor devices severe damages.

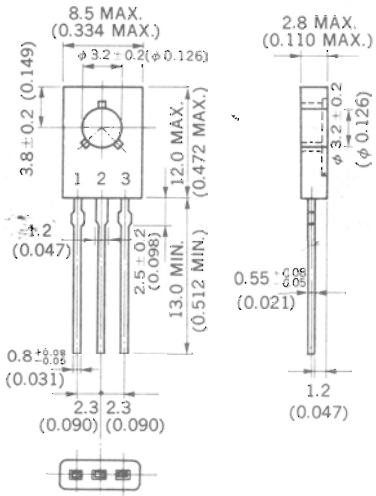
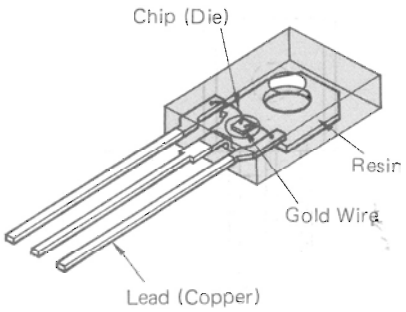
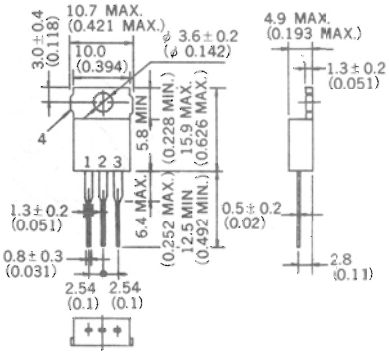
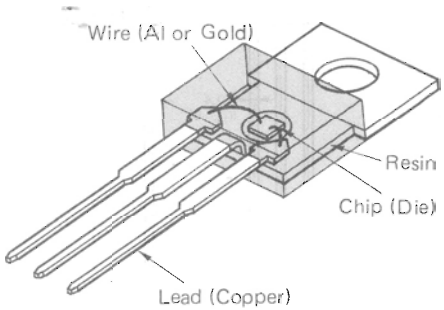
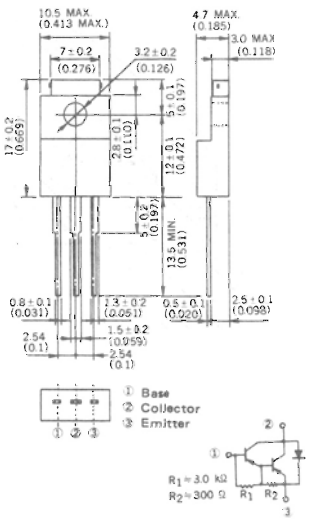
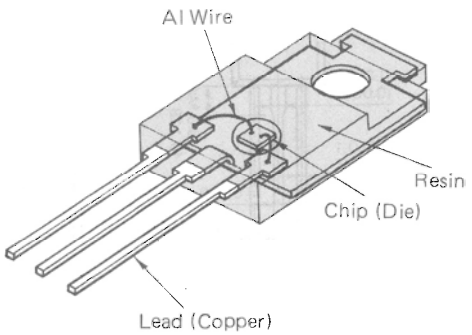
(7) A semiconductor device is an element that is extremely sensitive to humidity. Therefore, it is important to use such a device packed in an appropriate material suited for the degree of ambient humidity and expected reliability.

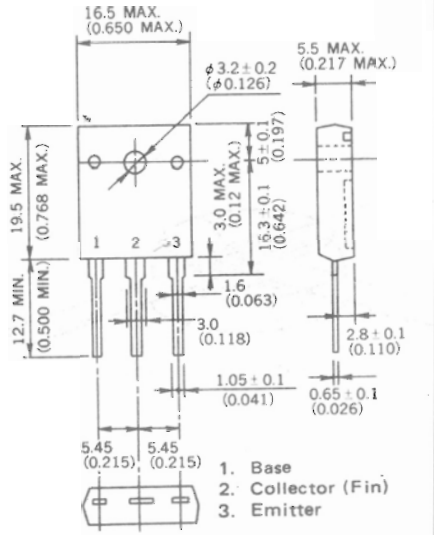
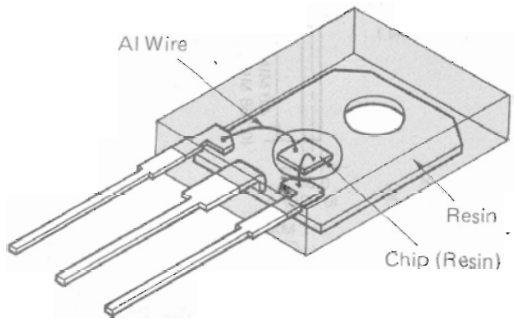
(8) The environment in which semiconductor devices are directly exposed to dust and dirt salt, or acid gas such as SO_2 gas may be usually the cause of leakage between leads and elements or rust.

PACKAGE DIMENSIONS & STRUCTURES

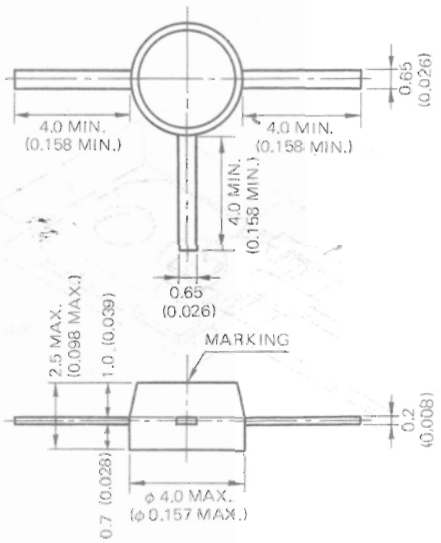
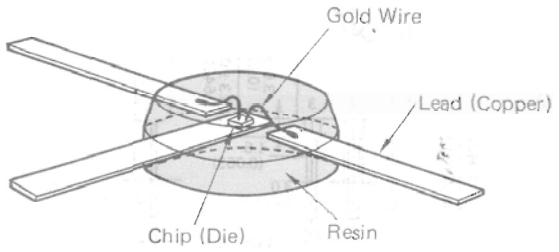
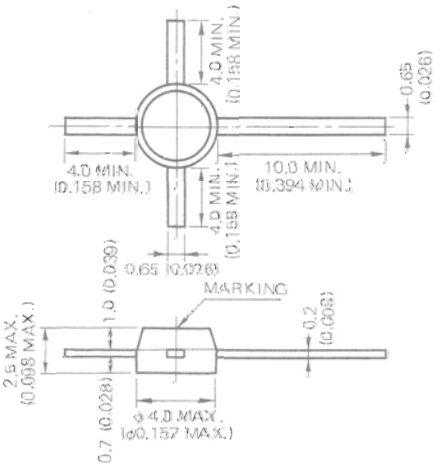
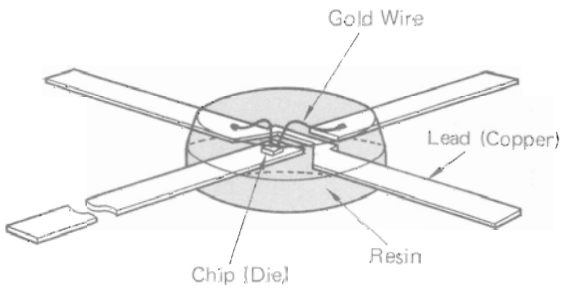
		PACKAGE DIMENSIONS in millimeters (inches)	STRUCTURES
PLASTIC MOLDED TRANSISTORS	TO-92		
	SST MOLD		
	SP MOLD		

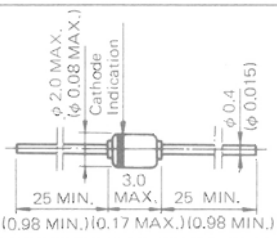
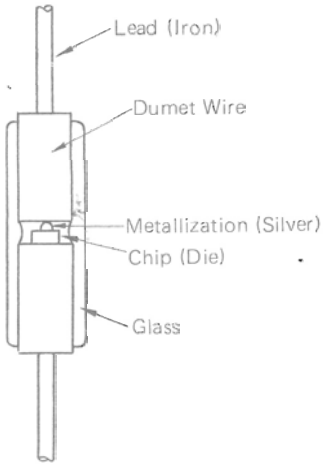
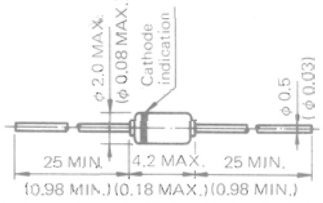
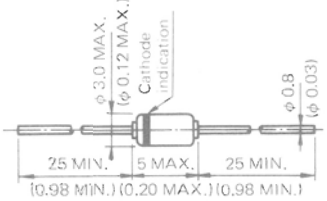
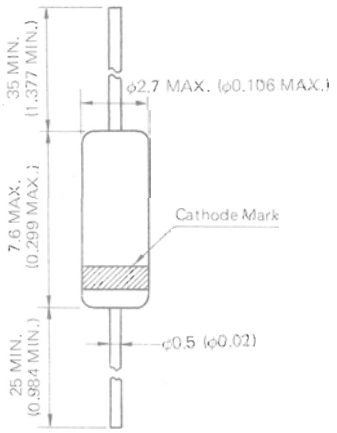
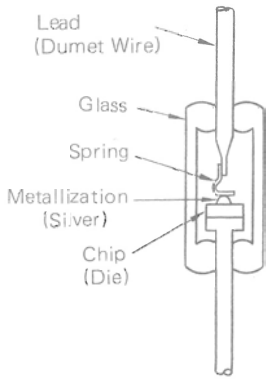
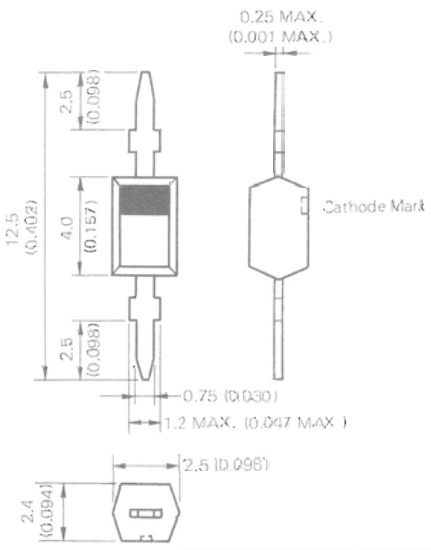
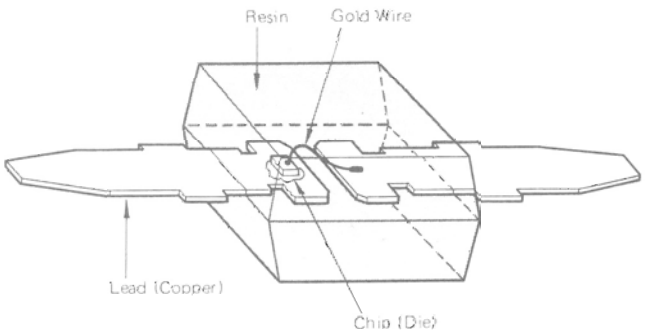
PLASTIC MOLDED POWER TRANSISTORS

	PACKAGE DIMENSIONS in millimeters (inches)	STRUCTURES
TO-126 (MP-5)		
TO-220 (MP-25)	 1. Base (B) 2. Collector (C) 3. Emitter (E) 4. Fin (Collector) JEDEC: TO-220AB	
MP-45		

		PACKAGE DIMENSIONS in millimeters (inches)	STRUCTURES
PLASTIC MOLDED POWER TRANSISTORS	MP-80		

DISK MOLD TRNASISTORS

	PACKAGE DIMENSIONS in millimeters (inches)	STRUCTURES
3-LEADS		
4-LEADS		

			PACKAGE DIMENSIONS in millimeters (inches)	STRUCTURES
GLASS PACKAGE DIODE	DOUBLE HEAT SINK	DO-34		
		DO-35		
		DO-41		
	MINI TYPE (DO-7)			
PLASTIC MOLDED DIODE				

DATA SHEETS

TRANSISTORS

2SA Type

2SB Type

2SC Type

2SD Type

2SJ Type

2SK Type

3SK Type

Twin Type

BUILT-IN RESISTORS Type

JE Series

for Switching

DIODES

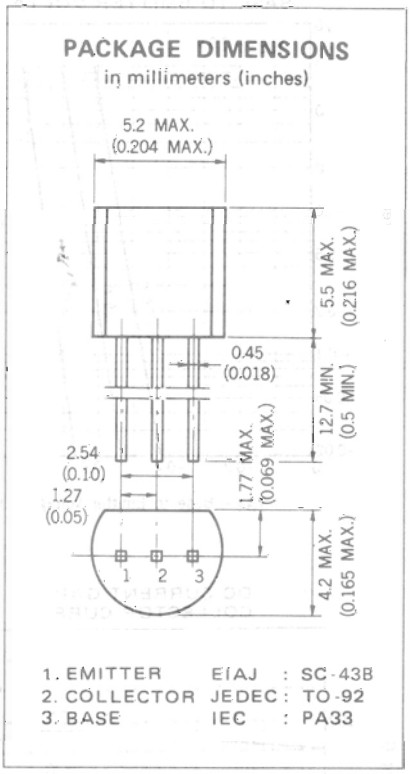
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
2SA639Ⓢ

DESCRIPTION The 2SA639Ⓢ is designed for use high voltage switching application.

FEATURES

- High breakdown voltage BV_{CER} : −180 V



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −180 V
- V_{CER} Collector to Emitter Voltage . . . . . −180 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −50 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	50	120		−	V_{CE}=−3.0 V, I_C=−1.0 mA
h_{FE2}	DC Current Gain	30	100	330	−	V_{CE}=−6.0 V, I_C=−15 mA
f_T	Gain Bandwidth Product		130		MHz	V_{CE}=−10 V, I_E=10 mA
C_{ob}	Output Capacitance		4.5		pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
BV_{CER}	Collector to Emitter Breakdown Voltage	−180	−240		V	I_C=−100 μA, R_{BE}=30 kΩ
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB}=−100 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB}=−3.0 V, I_C=0
$V_{CE(sat)}$	Collector Saturation Voltage		−0.22	−0.9	V	I_C=−10 mA, I_B=−1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.75	−1.0	V	I_C=−10 mA, I_B=−1.0 mA

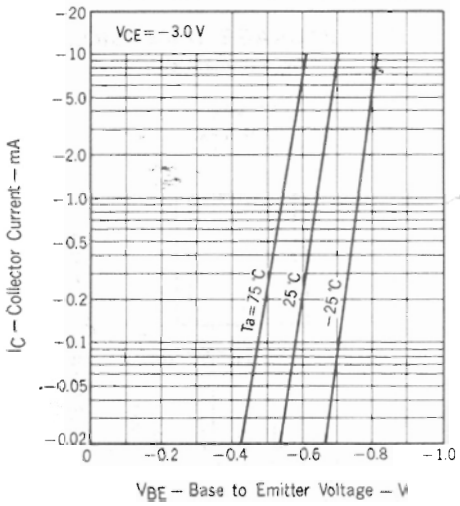
Classification of h_{FE2}

Rank	R	Q	P
Range	30 − 130	100 − 220	150 − 330

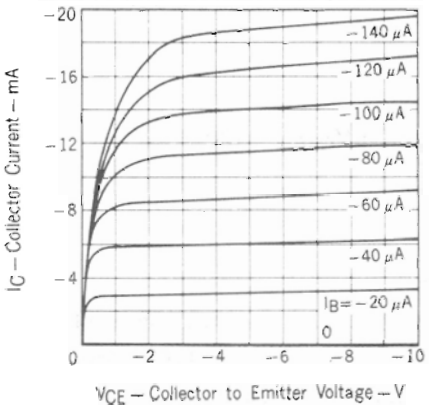
Test Conditions : V_{CE}=−6.0 V, I_C=−15 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

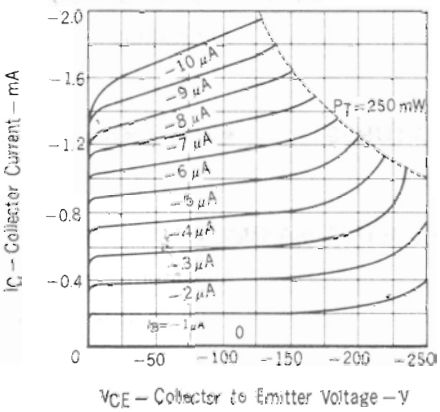
COLLECTOR CURRENT vs.
BASE TO EMITTER VOLTAGE



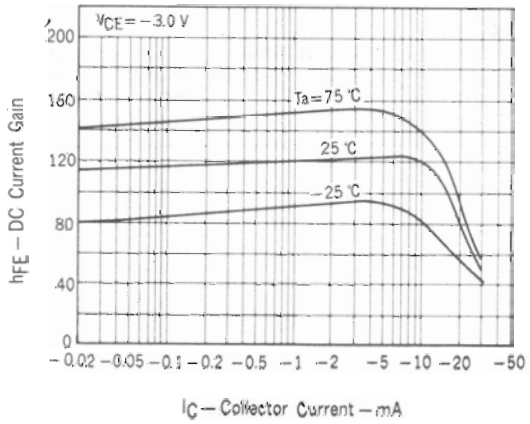
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



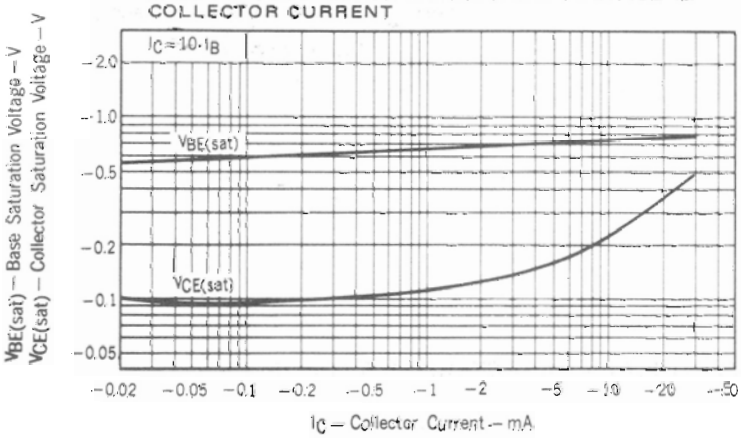
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



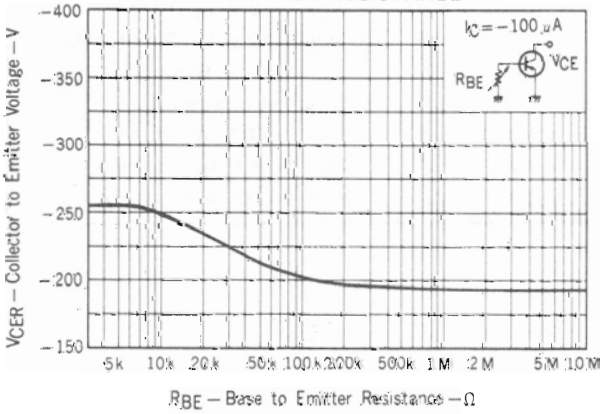
DC CURRENT GAIN vs.
COLLECTOR CURRENT



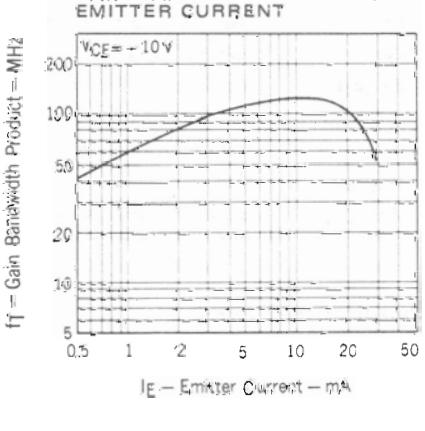
BASE AND COLLECTOR SATURATION VOLTAGE vs.
COLLECTOR CURRENT



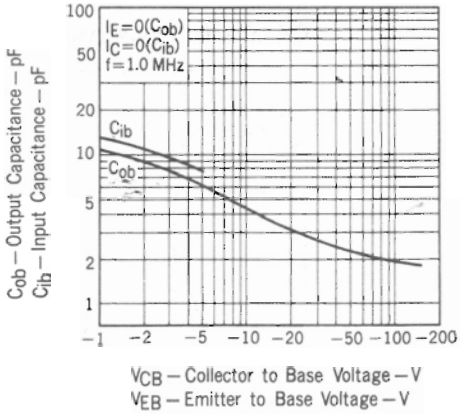
COLLECTOR TO EMITTER VOLTAGE vs.
BASE TO EMITTER RESISTANCE



GAIN BANDWIDTH PRODUCT vs.
EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

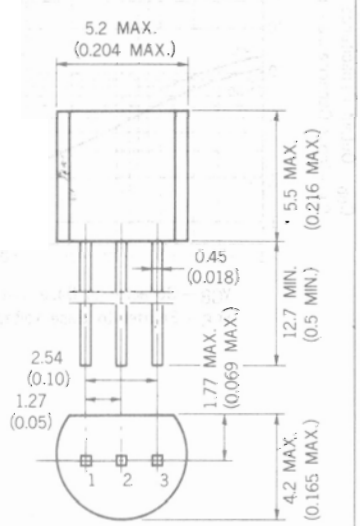
PNP SILICON TRANSISTOR
2SA733

DESCRIPTION The 2SA733 is designed for use in driver stage of AF amplifier.

FEATURES

- High h_{FE} and Excellent Linearity : 200 TYP.
  h_{FE} (V_{CE} = −6.0 V, I_C = −1.0 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −100 mA
- I_B Base Current . . . . . −20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	90	200	600		V_{CE} = −6.0 V, I_C = −1.0 mA
NF	Noise Figure		6.0	20	dB	V_{CE} = −6.0 V, I_C = −0.3 mA, R_G = 10 kΩ, f = 100 Hz
f_T	Gain Bandwidth Product	100	180		MHz	V_{CE} = −6.0 V, I_E = 10 mA
C_{ob}	Output Capacitance		4.5	6.0	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−0.55	−0.62	−0.65	V	V_{CE} = −6.0 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.3	V	I_C = −100 mA, I_B = −10 mA

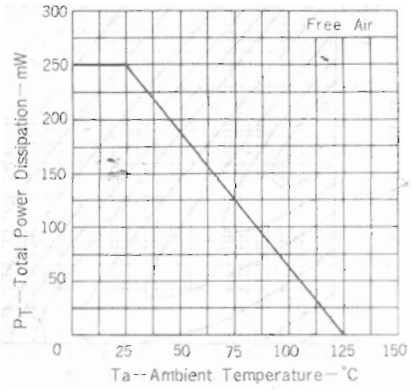
Classification of h_{FE}

Rank	R	Q	P	K
Range	90 – 180	135 – 270	200 – 400	300 – 600

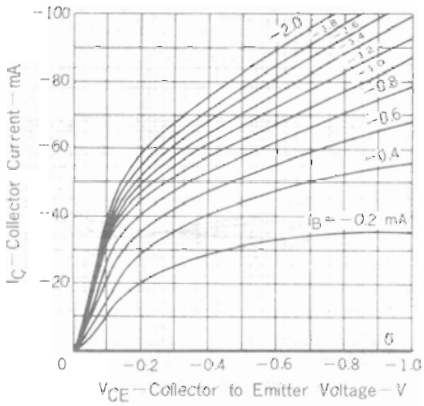
h_{FE} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

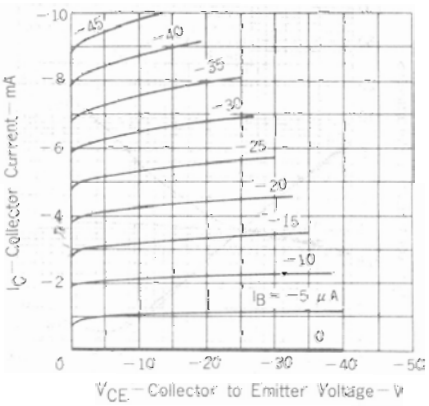
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



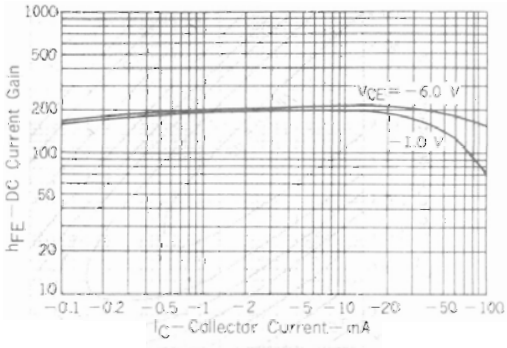
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



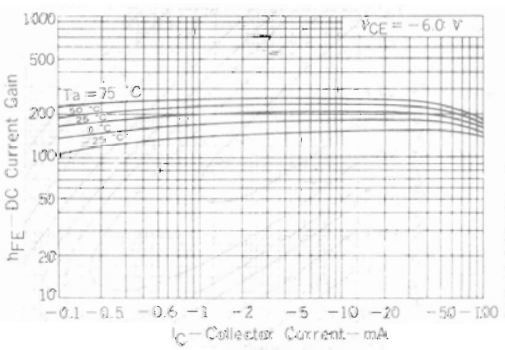
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



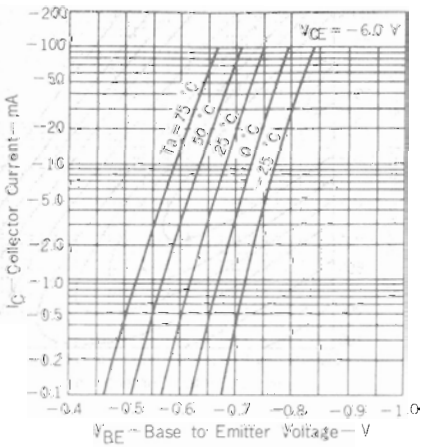
DC CURRENT GAIN vs. COLLECTOR CURRENT



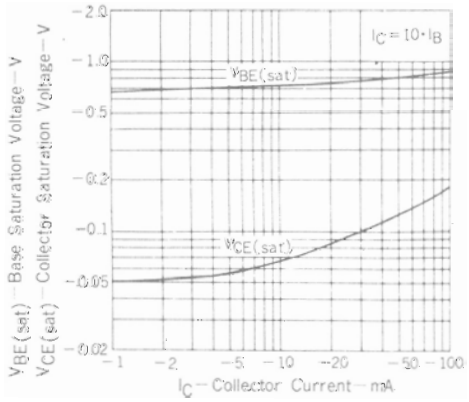
DC CURRENT GAIN vs. COLLECTOR CURRENT



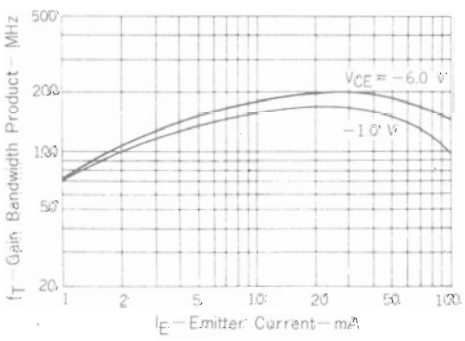
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



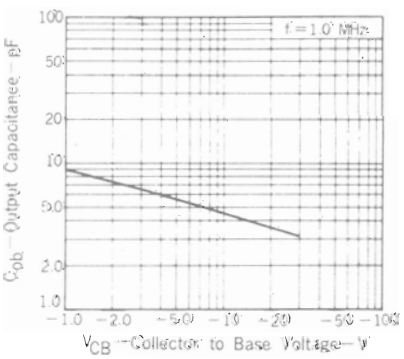
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



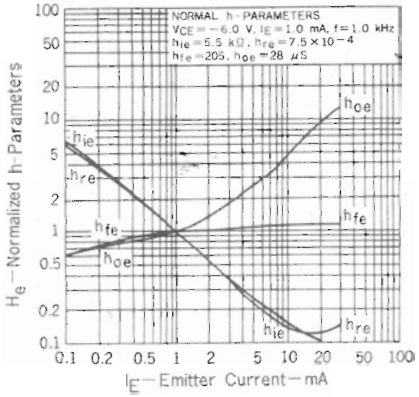
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



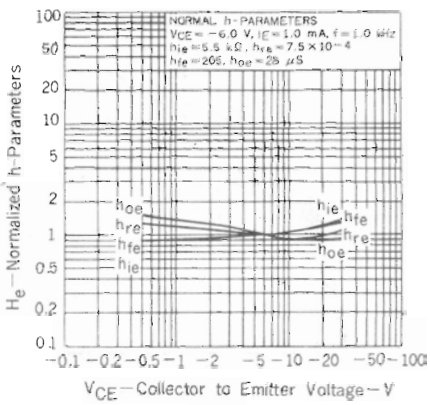
OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



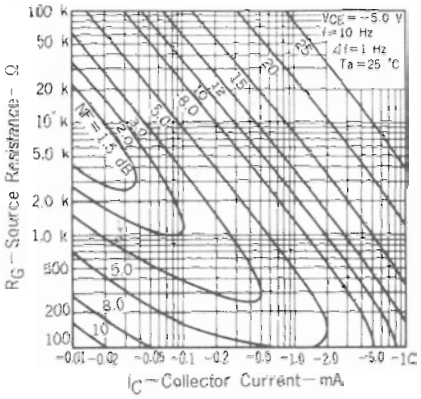
NORMALIZED h-PARAMETERS vs. EMITTER CURRENT



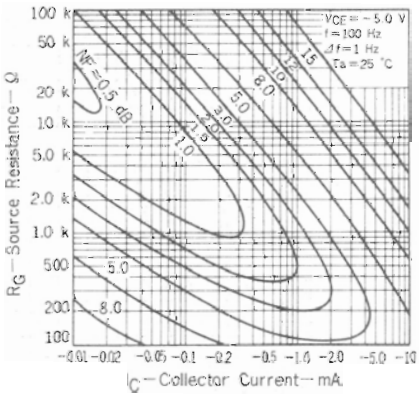
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



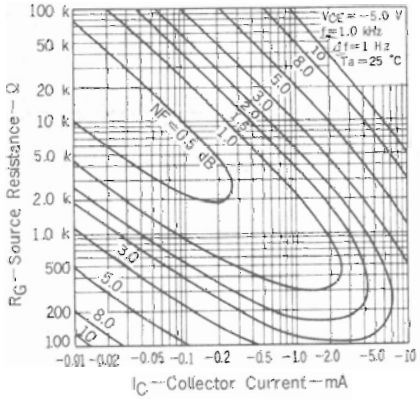
NOISE FIGURE MAP 1



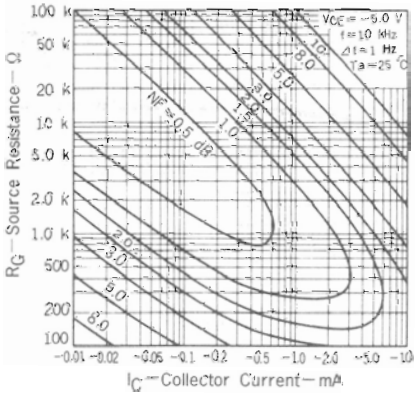
NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NOISE FIGURE MAP 4



NEC
ELECTRON DEVICE

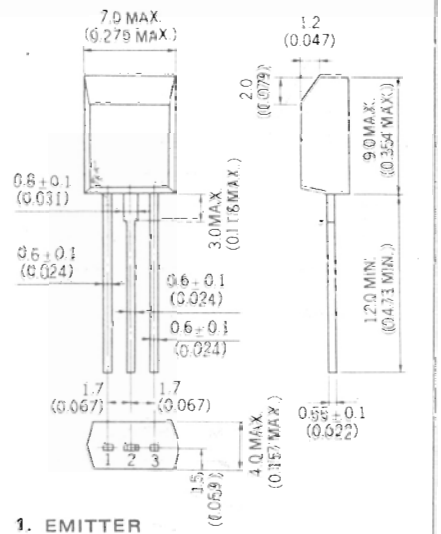
PNP SILICON TRANSISTOR
2SA915

DESCRIPTION The 2SA915 is designed for use in driver stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation and High Breakdown Voltage: 1.0 W at 25 °C Ambient Temperature/V_{CEO} = −120 V
- Complementary to the NEC 2SC1940 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 1.0 W
- Thermal Resistance (Junction to Ambient) . . . 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −120 V
- V_{CEO} Collector to Emitter Voltage . . . . . −120 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −50 mA
- I_B Base Current . . . . . −10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	−	V_{CE} = −10 V, I_C = −10 mA
h_{FE2}	DC Current Gain	50	200		−	V_{CE} = −10 V, I_C = −1.0 mA
f_T	Gain Bandwidth Product	50	80		MHz	V_{CE} = −10 V, I_E = 10 mA
C_{ob}	Output Capacitance		2.5	3.5	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−650	−695	−750	mV	V_{CE} = −10 V, I_C = −10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.6	V	I_C = −20 mA, I_B = −2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.79	−1.0	V	I_C = −20 mA, I_B = −2.0 mA

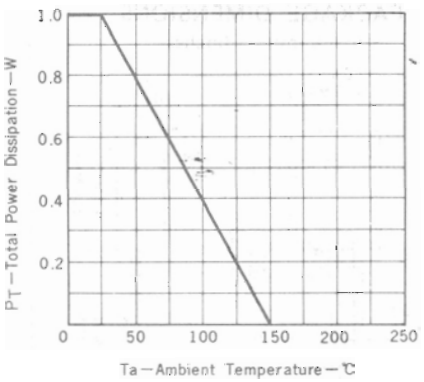
Classification of h_{FE1}

Rank	M	L	K
Range	90 − 180	135 − 270	200 − 400

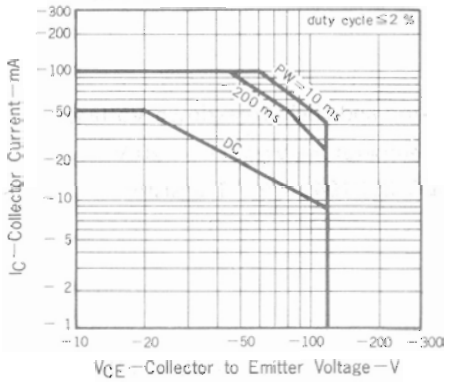
h_{FE1} Test Conditions: V_{CE} = −10 V, I_C = −10 mA

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

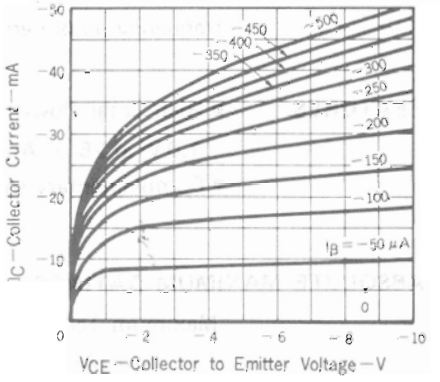
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



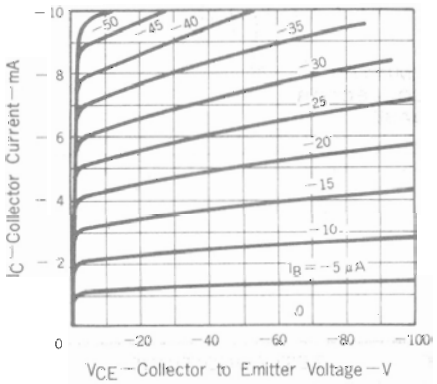
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



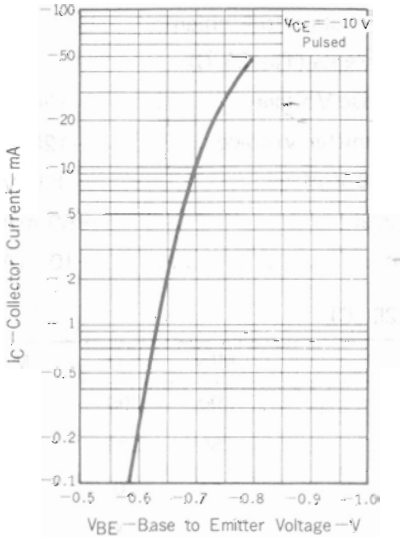
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



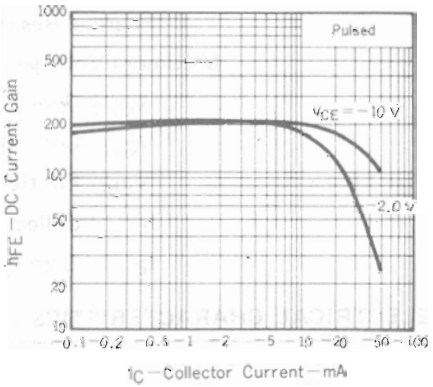
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



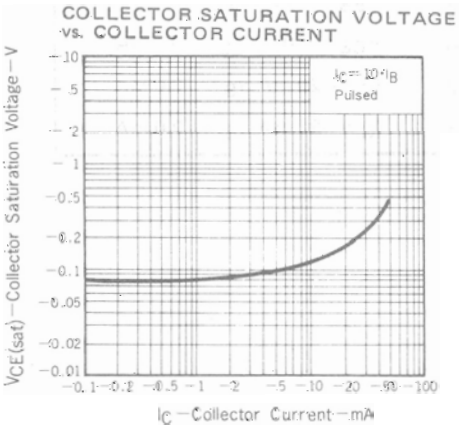
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



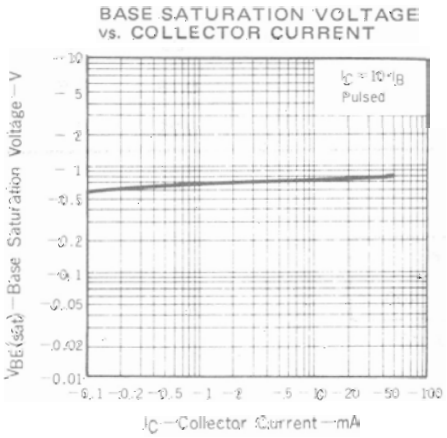
DC CURRENT GAIN vs. COLLECTOR CURRENT



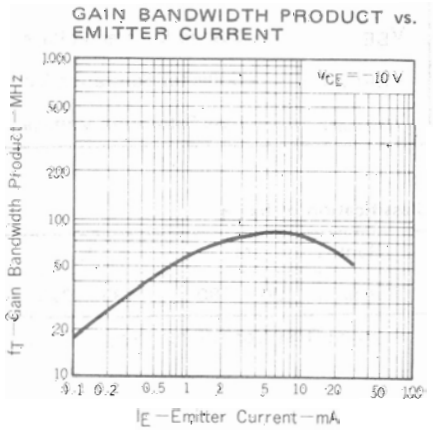
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



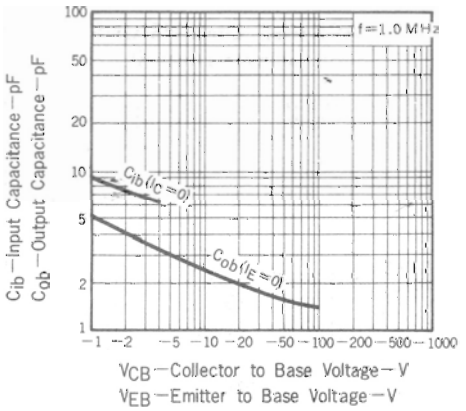
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE
vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

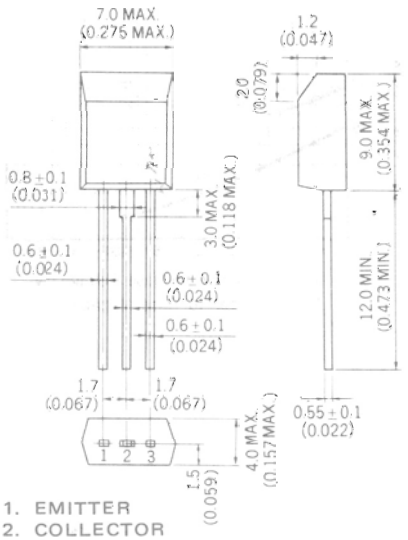
PNP SILICON TRANSISTOR
2SA916

DESCRIPTION The 2SA916 is designed for use in driver stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation and High Breakdown Voltage: 1.0 W at 25 °C Ambient Temperature /V_{CEO} = −160 V
- Complementary to the NEC 2SC1941 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 1.0 W
- Thermal Resistance (Junction to Ambient). . . 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −160 V
- V_{CEO} Collector to Emitter Voltage . . . . . −160 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −50 mA
- I_B Base Current . . . . . −10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	–	V_{CE} = −10 V, I_C = −10 mA
h_{FE2}	DC Current Gain	50	200		–	V_{CE} = −10 V, I_C = −1.0 mA
f_T	Gain Bandwidth Product	50	80		MHz	V_{CE} = −10 V, I_E = 10 mA
C_{ob}	Output Capacitance		2.5	3.5	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −160 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−650	−695	−750	mV	V_{CE} = −10 V, I_C = −10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.6	V	I_C = −20 mA, I_B = −2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.79	−1.0	V	I_C = −20 mA, I_B = −2.0 mA

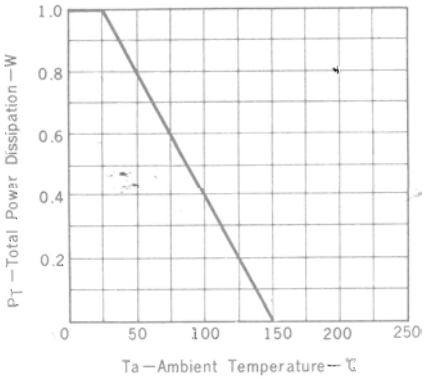
Classification of h_{FE1}

Rank	M	L	K
Range	90 − 180	135 − 270	200 − 400

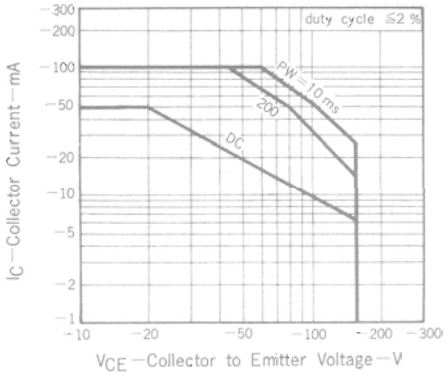
h_{FE1} Test Conditions: V_{CE} = −10 V, I_C = −10 mA

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

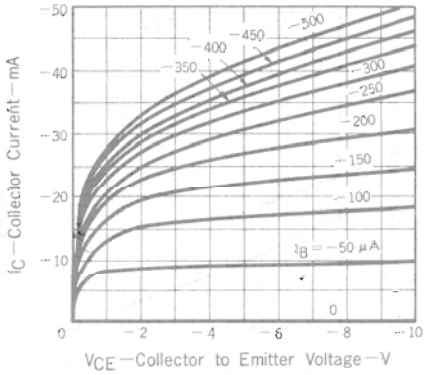
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



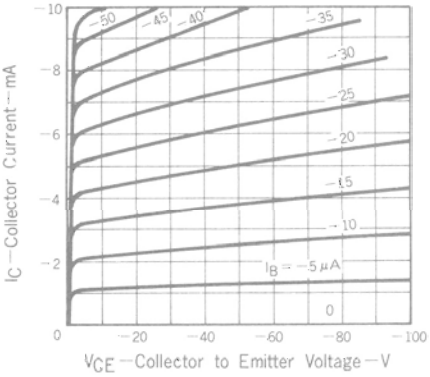
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



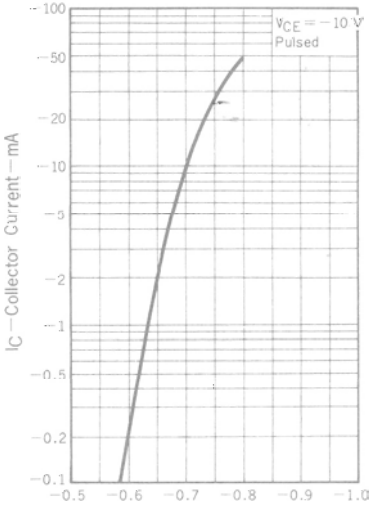
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



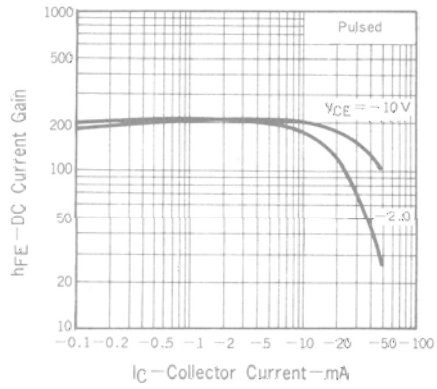
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



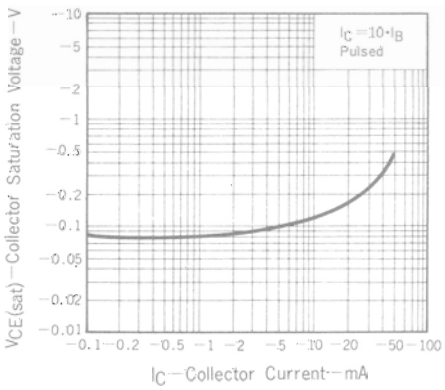
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



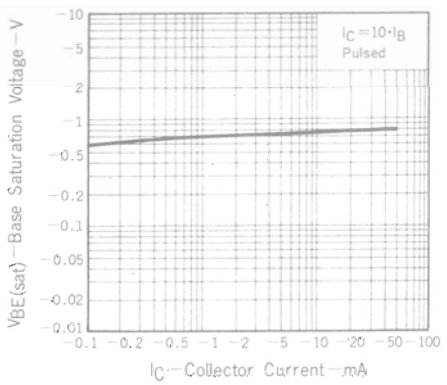
DC CURRENT GAIN vs. COLLECTOR CURRENT



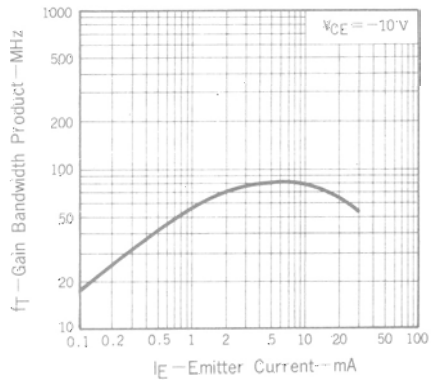
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



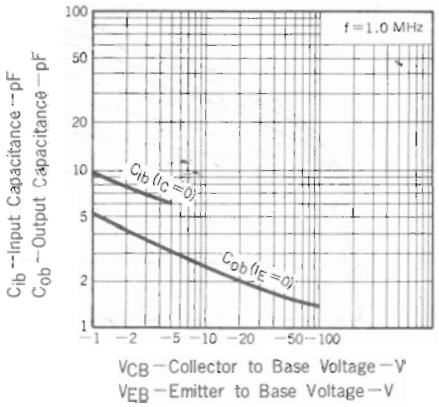
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE
vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

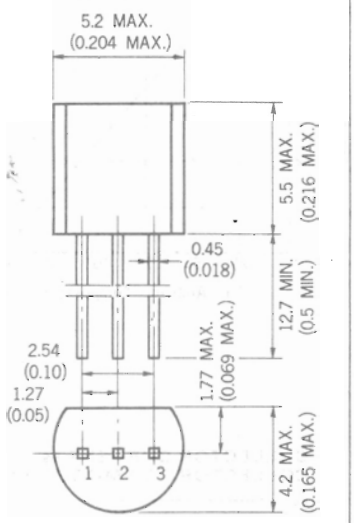
PNP SILICON TRANSISTOR
2SA952

DESCRIPTION The 2SA952 is designed for use in output stage of portable radio and cassette type tape recorder, general purpose applications.

FEATURES

- High total power dissipation.
  P_T = 600 mW
- High h_{FE} and low $V_{CE(sat)}$.
  h_{FE} (I_C = −100 mA) : 200 TYP.
  $V_{CE(sat)}$ (−700 mA) : −0.25 V TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C
Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	−30	V
V_{CEO}	Collector to Emitter Voltage	−25	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
I_C	Collector Current	−700	mA
I_B	Base Current	−150	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	90	200	400	–	V_{CE} = −1.0 V, I_C = −100 mA
h_{FE2}*	DC Current Gain	50	100		–	V_{CE} = −1.0 V, I_C = −700 mA
C_{ob}	Collector to Base Capacitance		17	40	pF	V_{CB} = −6.0 V, I_E = 0 f = 1.0 MHz
f_T	Gain Bandwidth Product	50	160		MHz	V_{CE} = −6.0 V, I_E = 10 mA
V_{BE}*	Base to Emitter Voltage	−600	−640	−700	mV	V_{CE} = −6.0 V, I_C = −10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.25	−0.6	V	I_C = −700 mA, I_B = −70 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.95	−1.2	V	I_C = −700 mA, I_B = −70 mA
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0

*Pulsed PW ≦ 350 μs, duty cycle ≦ 2.0 %

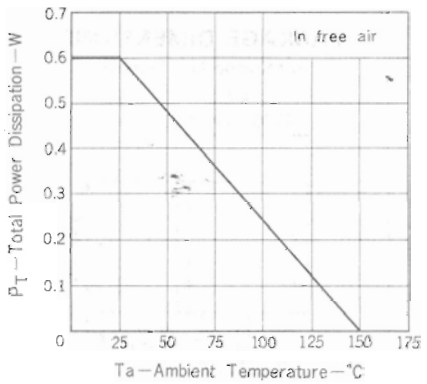
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

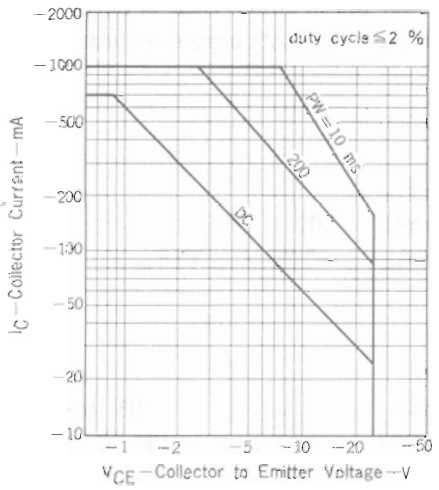
h_{FE} Test Conditions : V_{CE} = −1.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

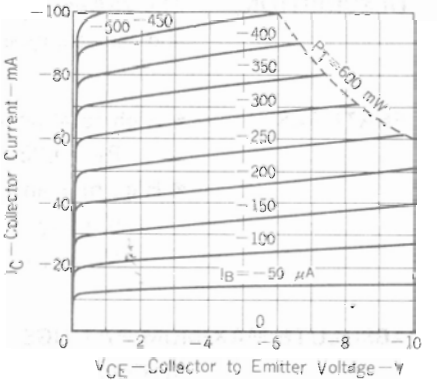
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



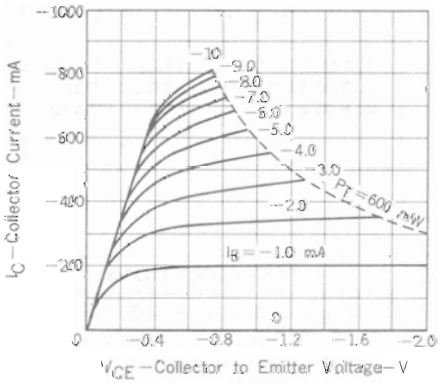
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



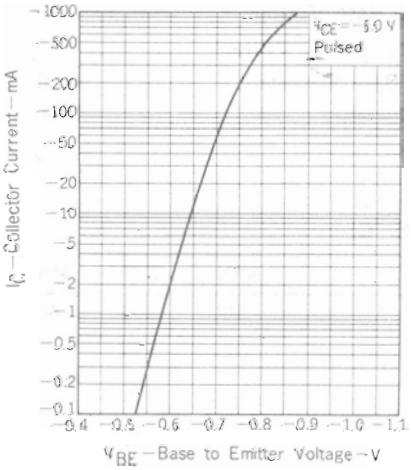
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



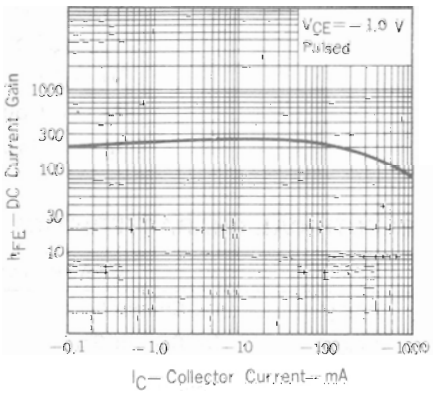
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



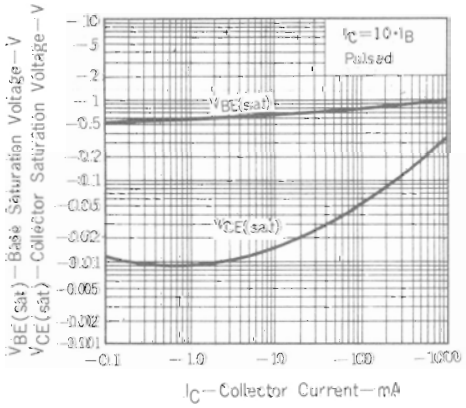
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



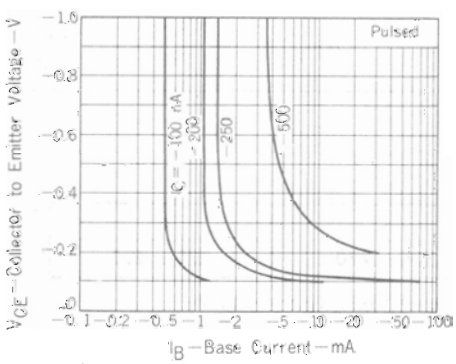
DC CURRENT GAIN vs. COLLECTOR CURRENT



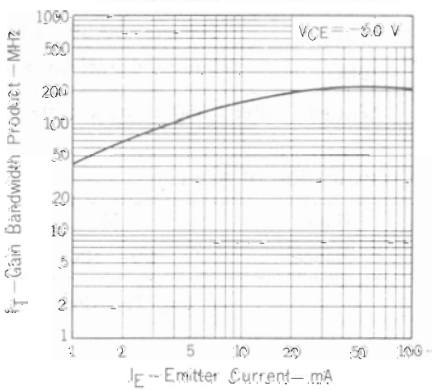
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



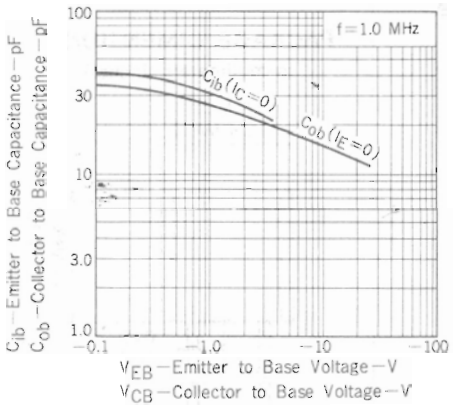
COLLECTOR TO EMITTER VOLTAGE vs. BASE CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

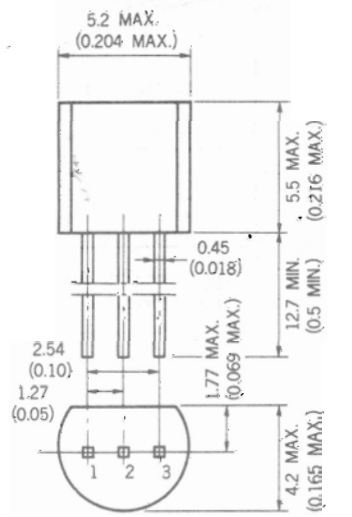
PNP SILICON TRANSISTOR
2SA953

DESCRIPTION The 2SA953 is designed for use in driver stage of high voltage audio equipment.

FEATURES

- High total power dissipation.
  P_T = 600 mW
- High h_{FE} and high voltage.
  h_{FE} (I_C = −50 mA) : 200 TYP.
  V_{CEO} : −60 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	−60	V
V_{CEO}	Collector to Emitter Voltage	−60	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
I_C	Collector Current	−300	mA
I_B	Base Current	−60	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	90	200	400	—	V_{CE} = −1.0 V, I_C = −50 mA
h_{FE2}*	DC Current Gain	30	80		—	V_{CE} = −1.0 V, I_C = −300 mA
C_{ob}	Collector to Base Capacitance		13	25	pF	V_{CB} = −6.0 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = −6.0 V, I_E = 10 mA
V_{BE}*	Base to Emitter Voltage	−600	−660	−700	mV	V_{CE} = −6.0 V, I_C = −10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.15	−0.6	V	I_C = −300 mA, I_B = −30 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.85	−1.2	V	I_C = −300 mA, I_B = −30 mA
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0

* Pulsed PW ≦ 350 μs, duty cycle ≦ 2.0 %

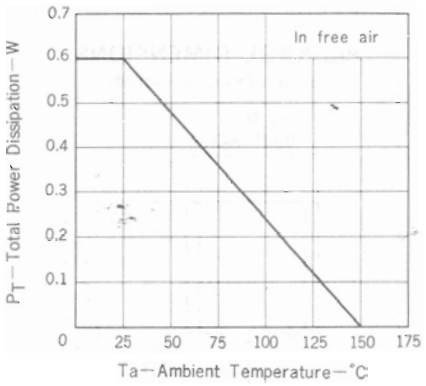
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

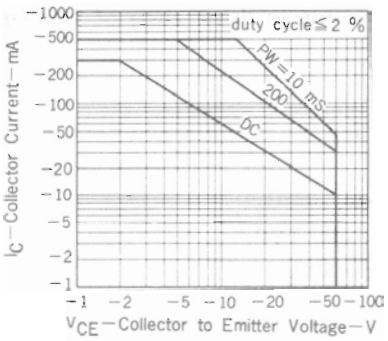
h_{FE} Test Conditions : V_{CE} = −1.0 V, I_C = −50 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

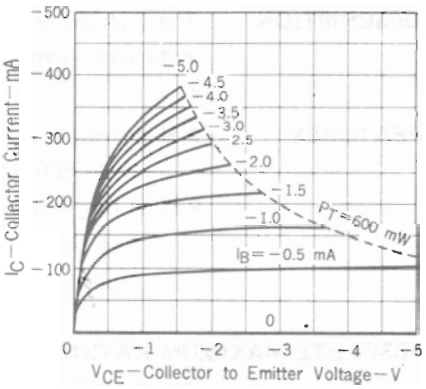
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



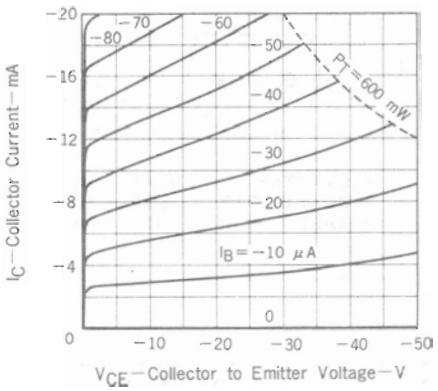
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



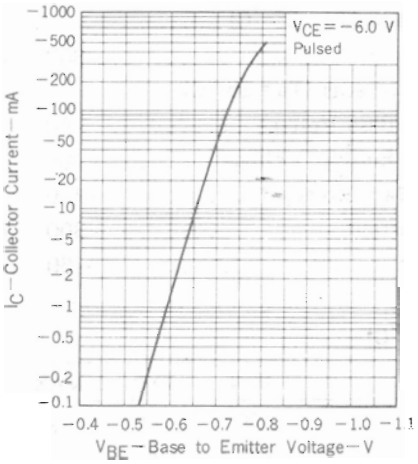
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



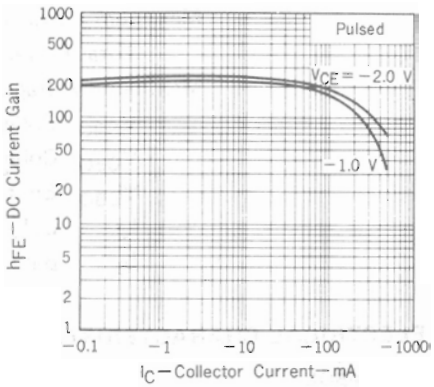
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



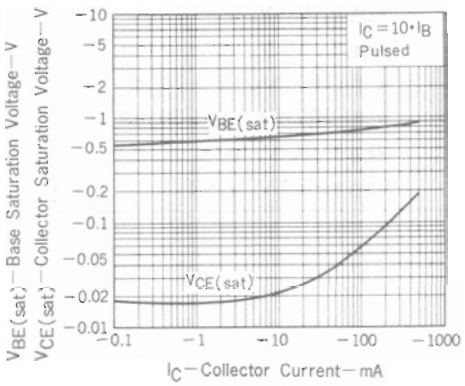
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



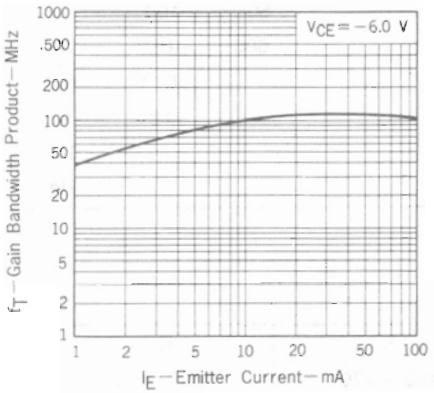
DC CURRENT GAIN vs. COLLECTOR CURRENT



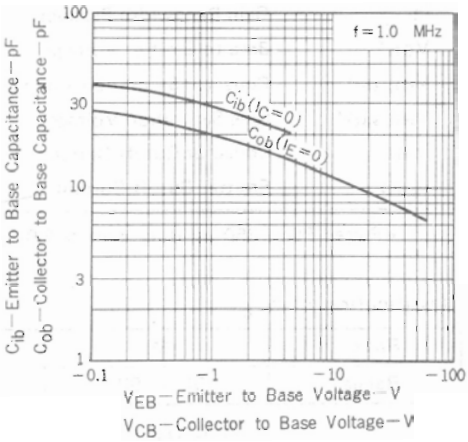
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

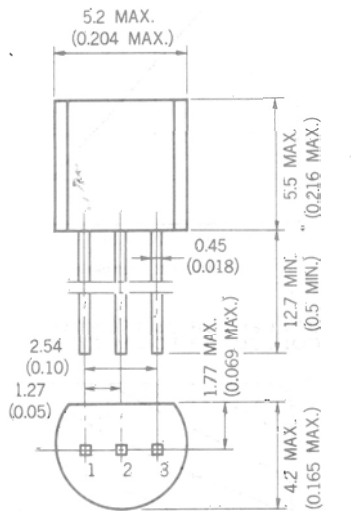
PNP SILICON TRANSISTOR
2SA954

DESCRIPTION The 2SA954 is designed for use in driver stage of high voltage audio equipment.

FEATURES

- High total power dissipation.
  P_T = 600 mW
- High h_{FE} and high voltage.
  h_{FE} (I_C = −50 mA) : 200 TYP.
  V_{CEO} : −80 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −80 V
- V_{CEO} Collector to Emitter Voltage . . . . . −80 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −300 mA
- I_B Base Current . . . . . −60 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	90	200	400	—	V_{CE} = −1.0 V, I_C = −50 mA
h_{FE2}*	DC Current Gain	30	80		—	V_{CE} = −1.0 V, I_C = −300 mA
C_{ob}	Collector to Base Capacitance		13	25	pF	V_{CB} = −6.0 V, I_E = 0 f = 1.0 MHz
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = −6.0 V, I_E = 10 mA
V_{BE}*	Base to Emitter Voltage	−600	−660	−700	mV	V_{CE} = −6.0 V, I_C = −10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.15	−0.6	V	I_C = −300 mA, I_B = −30 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.85	−1.2	V	I_C = −300 mA, I_B = −30 mA
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0

* Pulsed PW ≦ 350 μs, duty cycle ≦ 2.0 %

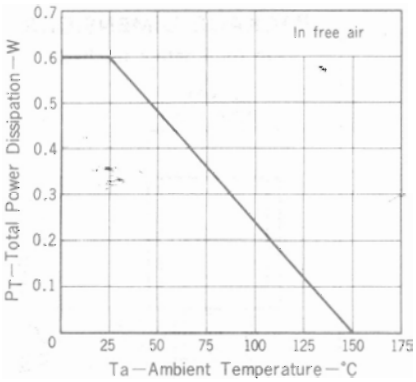
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

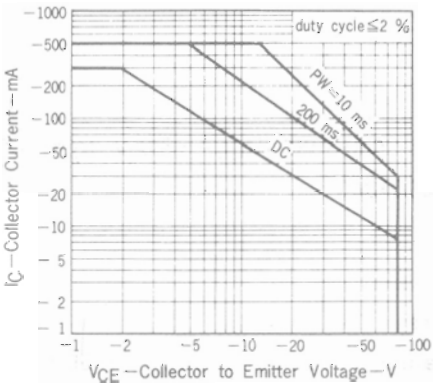
h_{FE} Test Conditions : V_{CE} = −1.0 V, I_C = −50 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

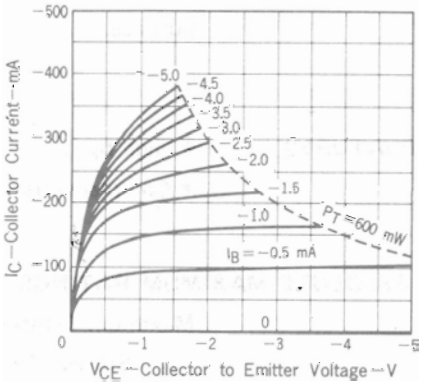
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



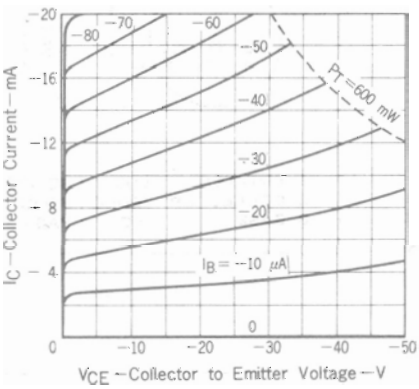
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



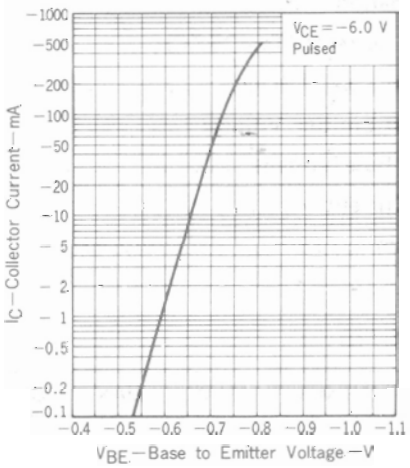
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



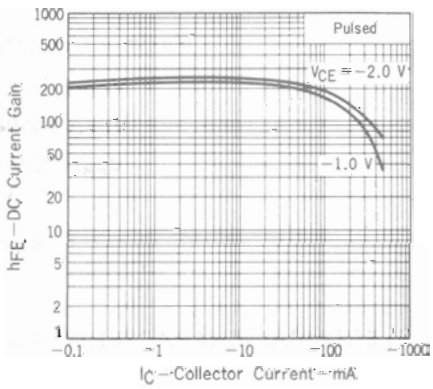
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



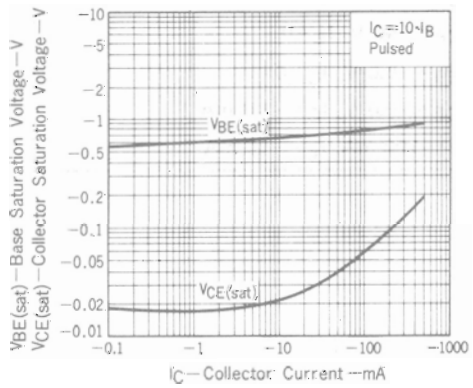
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



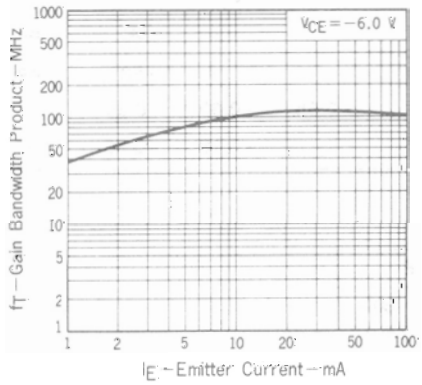
DC CURRENT GAIN vs. COLLECTOR CURRENT



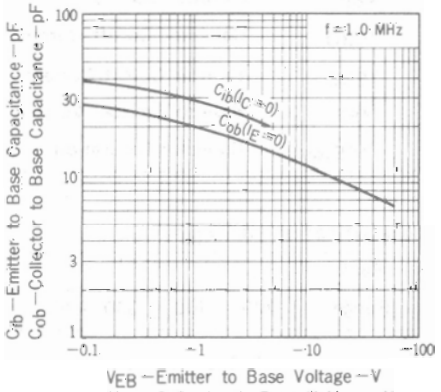
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



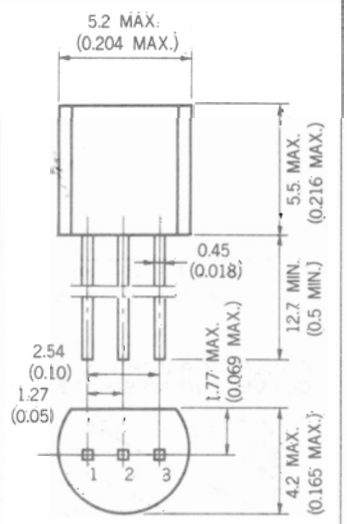
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
2SA987

DESCRIPTION The 2SA987 is designed for use in an AF amplifier and general purpose.

FEATURES
- High h_{FE}. h_{FE} : 400 TYP. (V_{CE} = −6.0 V, I_C = −1.0 mA)
- Complementary to 2SC1840.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . −40 V

V_{CEO} Collector to Emitter Voltage . . . . . −35 V

V_{EBO} Emitter to Base Voltage . . . . . −5.0 V

I_C Collector Current . . . . . −100 mA

I_B Base Current . . . . . −20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	380		–	V_{CE} = −6.0 V, I_C = −0.1 mA
h_{FE2}	DC Current Gain	200	400	800	–	V_{CE} = −6.0 V, I_C = −1.0 mA
f_T	Gain Bandwidth Product	50	90		MHz	V_{CE} = −6.0 V, I_E = 1.0 mA
C_{ob}	Output Capacitance		5.5	10	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB} = −40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−0.55	−0.60	−0.65	V	V_{CE} = −6.0 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.50	V	I_C = −100 mA, I_B = −10 mA

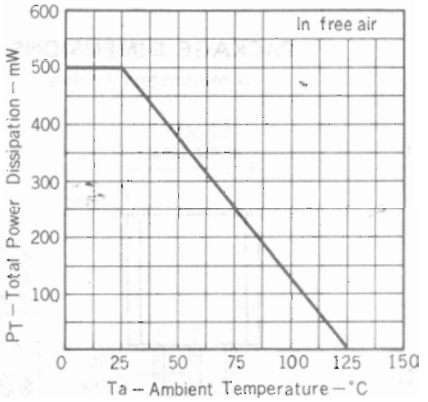
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

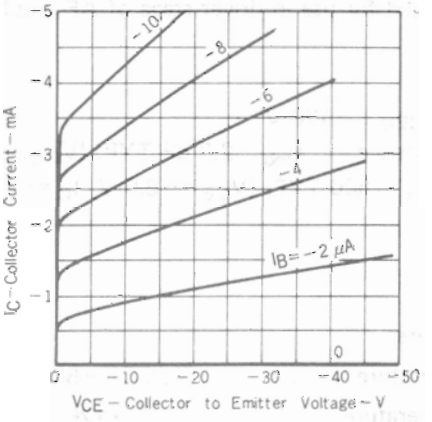
h_{FE} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

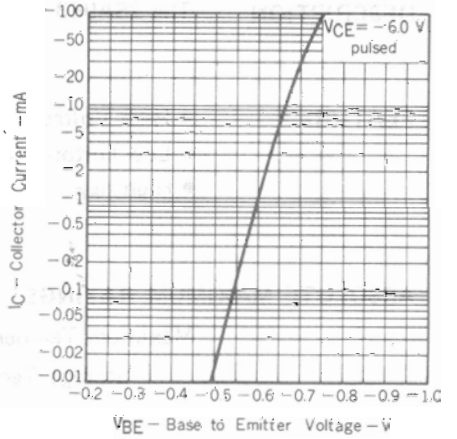
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



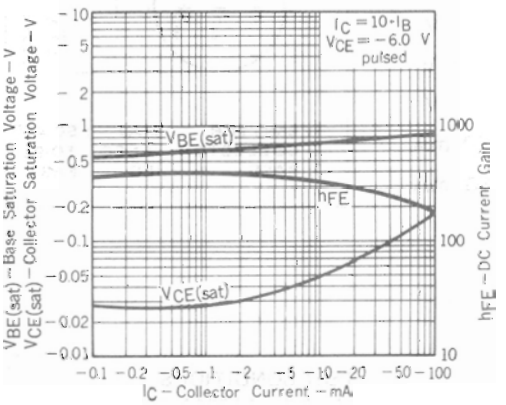
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



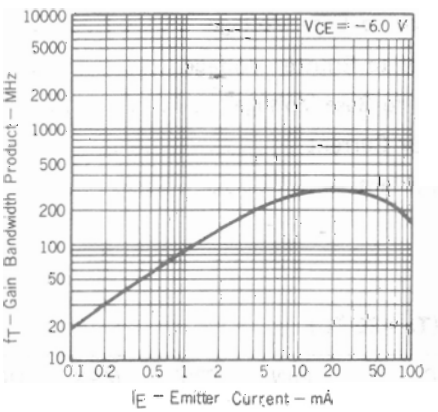
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



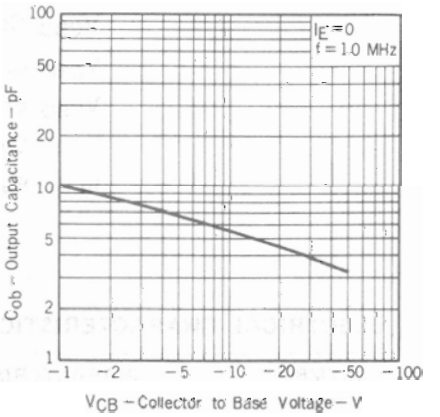
COLLECTOR AND BASE SATURATION VOLTAGE, DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

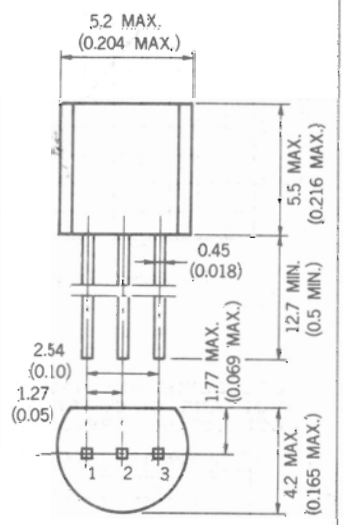
PNP SILICON TRANSISTOR
2SA988

DESCRIPTION The 2SA988 is designed for use in driver stage of AF amplifier.

FEATURES

- High Voltage. V_{CEO} : −120 V
- Low Output Capacitance. C_{ob} : 2.0 pF TYP. (V_{CB} = −30 V)
- High h_{FE}. h_{FE} : 500 TYP. (V_{CE} = −6.0 V, I_C = −1.0 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −120 V
- V_{CEO} Collector to Emitter Voltage . . . . . −120 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −50 mA
- I_B Base Current . . . . . −10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	500		−	V_{CE} = −6.0 V, I_C = −0.1 mA
h_{FE2}	DC Current Gain	200	500	800	−	V_{CE} = −6.0 V, I_C = −1.0 mA
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = −6.0 V, I_E = 1.0 mA
Cob	Output Capacitance		2.0	3.0	pF	V_{CB} = −30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB} = −120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−0.55	−0.61	−0.65	V	V_{CE} = −6.0 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.09	−0.30	V	I_C = −10 mA, I_B = −1.0 mA

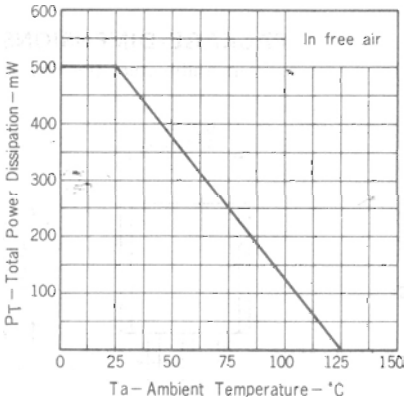
Classification of h_{FE2}

Rank	P	F	E
Range	200 − 400	300 − 600	400 − 800

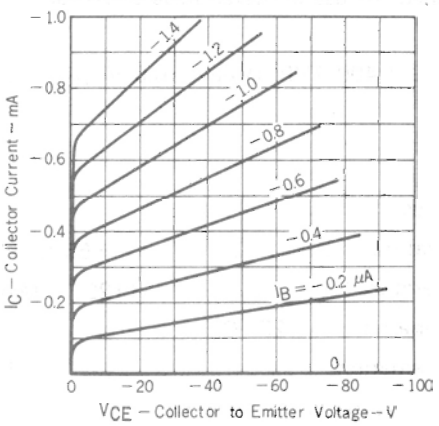
h_{FE} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

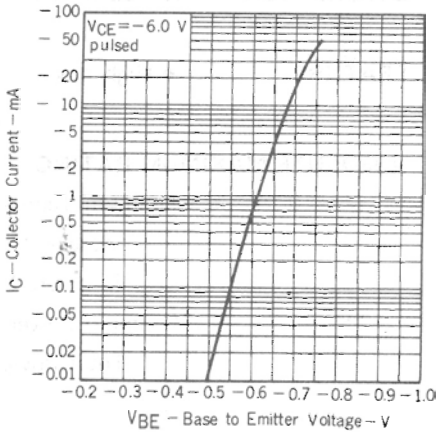
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



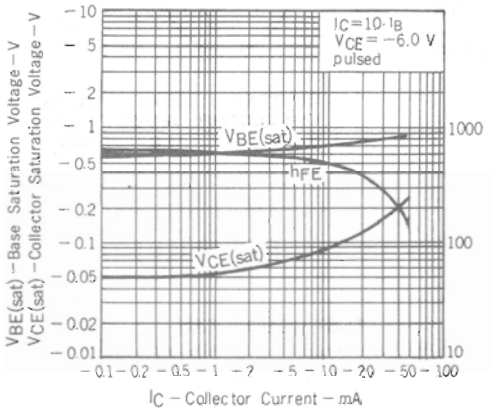
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



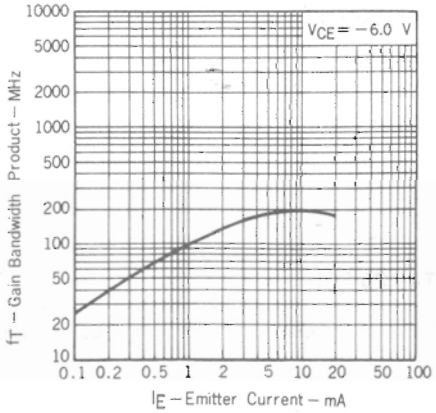
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



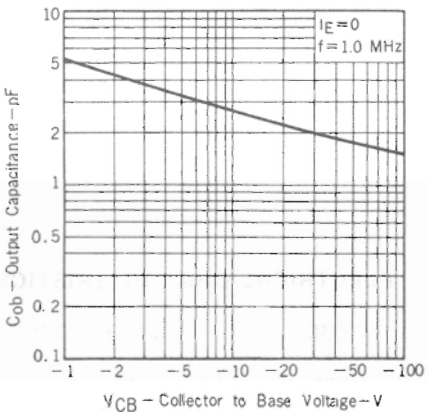
COLLECTOR AND BASE SATURATION VOLTAGE, DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



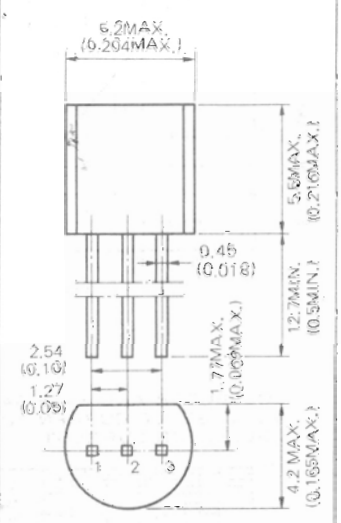
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
2SA990

DESCRIPTION The 2SA990 is designed for use in driver stage of AF amplifier.

FEATURE • High h_{FE} h_{FE} : 400 TYP. (V_{CE} = −6.0 V, I_C = −1.0 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −100 mA
- I_B Base Current . . . . . −20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	380		—	V_{CE} = −6.0 V, I_C = −0.1 mA
h_{FE2}	DC Current Gain	200	400	800	—	V_{CE} = −6.0 V, I_C = −1.0 mA
f_T	Gain Bandwidth Product	50	180		MHz	V_{CE} = −6.0 V, I_E = 1.0 mA
Cob	Output Capacitance		4.5	6.0	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
NV	Noise Voltage		25	40	mV	V_{CE} = −5.0 V, I_C = −1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = −60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−0.55	−0.62	−0.65	V	V_{CE} = −6.0 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.30	V	I_C = −100 mA, I_B = −10 mA

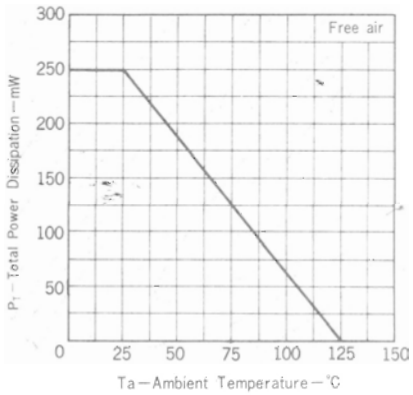
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

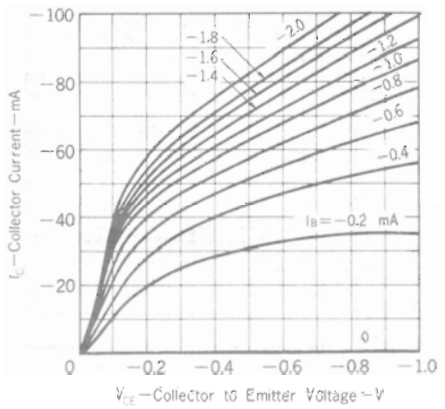
h_{FE2} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

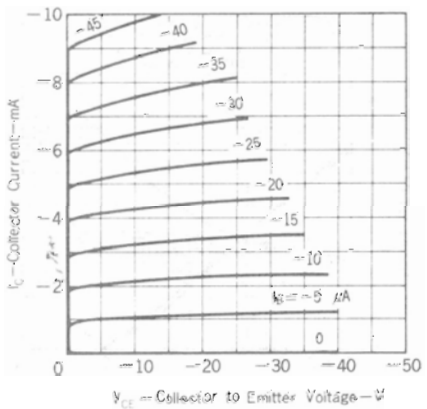
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



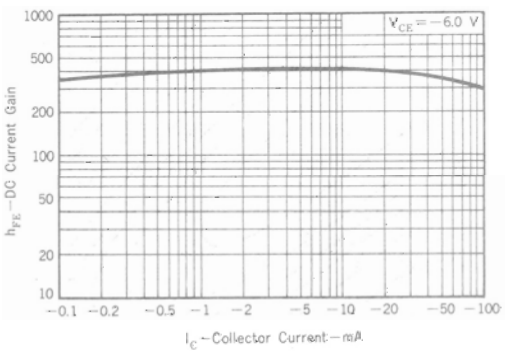
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



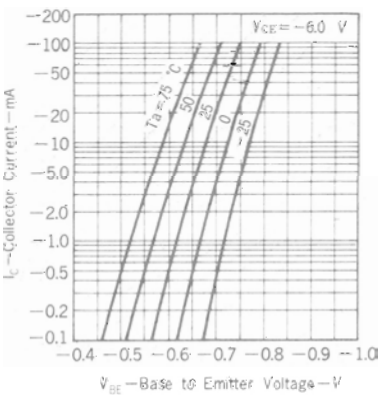
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



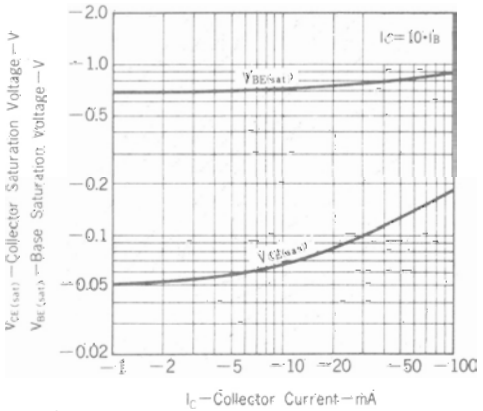
DC CURRENT GAIN vs. COLLECTOR CURRENT



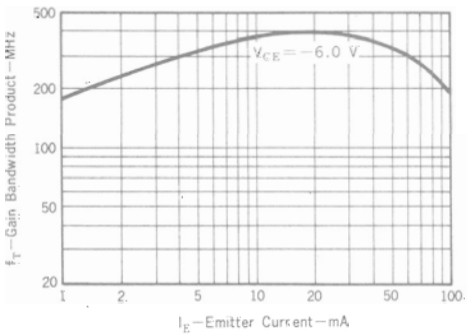
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



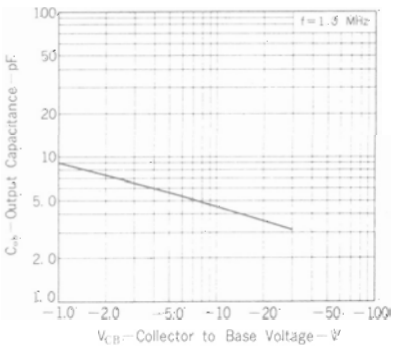
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



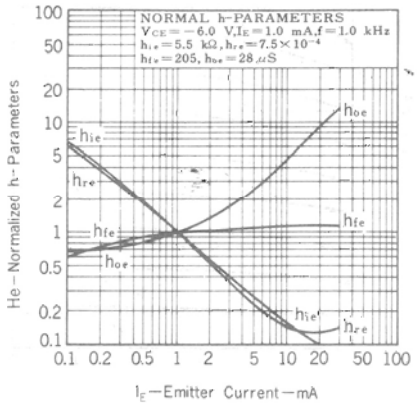
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



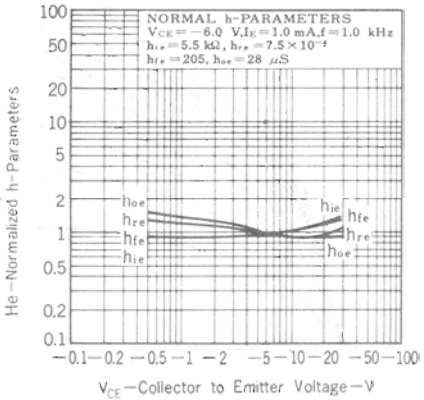
OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



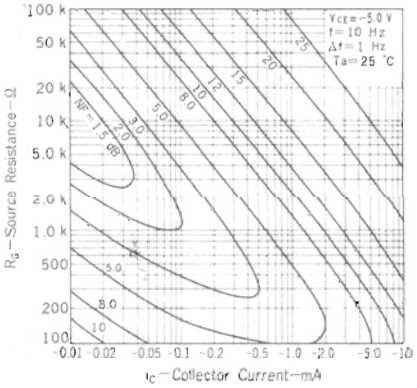
NORMALIZED h-PARAMETERS vs. EMITTER CURRENT



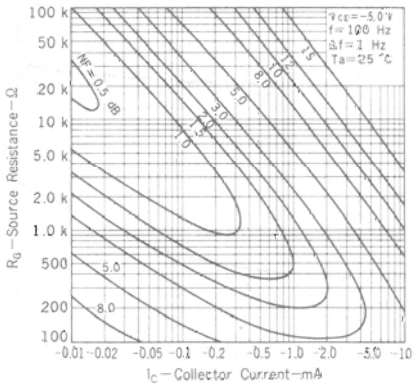
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



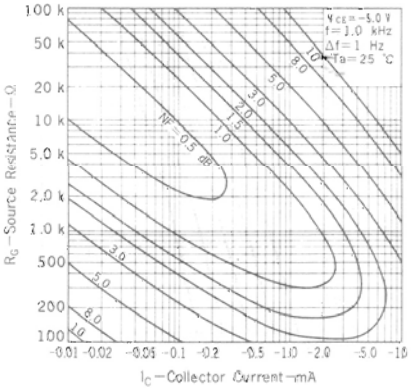
NOISE FIGURE MAP 1



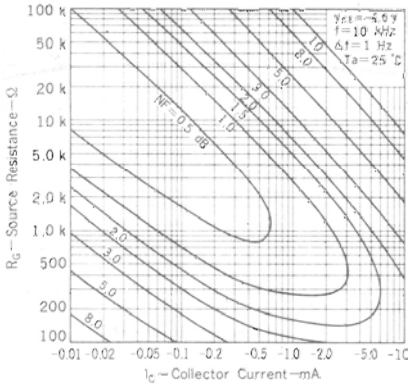
NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NOISE FIGURE MAP 4



NEC
ELECTRON DEVICE

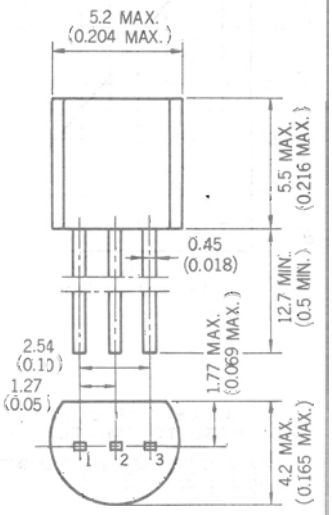
PNP SILICON TRANSISTOR
2SA991

DESCRIPTION The 2SA991 is best for the head amplifier of tape recorders, the equalizer of moving coil type record players, and etc.

FEATURES

- Super Low Noise. NV : 30 mV TYP. (See test circuit.)
- High h_{FE}. h_{FE} : 400 TYP. (V_{CE}=−6.0 V, I_C=−1.0 mA)
- Complementary to 2SC1844.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −60 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −100 mA
- I_B Base Current . . . . . −20 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	380		−	V_{CE}=−6.0 V, I_C=−0.1 mA
h_{FE2}	DC Current Gain	200	400	800	−	V_{CE}=−6.0 V, I_C=−1.0 mA
f_T	Gain Bandwidth Product	50	90		MHz	V_{CE}=−6.0 V, I_E=1.0 mA
C_{ob}	Output Capacitance		5.5	10	pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
NV	Noise Voltage		30	45	mV	V_{CE}=−5.0 V, I_C=−1.0 mA, R_G=100 kΩ G_V=80 dB, f=10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB}=−60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB}=−5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55	−0.60	−0.65	V	V_{CE}=−6.0 V, I_C=−1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.50	V	I_C=−100 mA, I_B=−10 mA

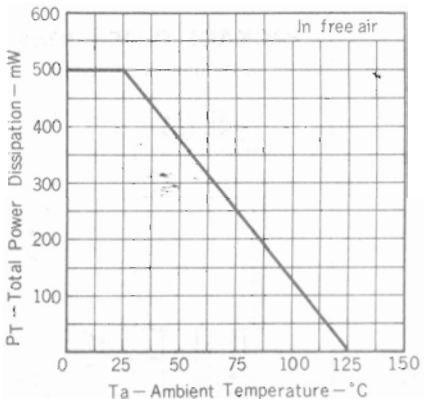
Classification of h_{FE2}

Rank	P	F	E
Range	200 − 400	300 − 600	400 − 800

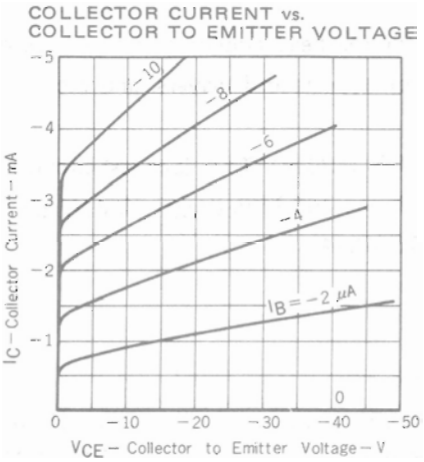
h_{FE} Test Conditions : V_{CE}=−6.0 V, I_C=−1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

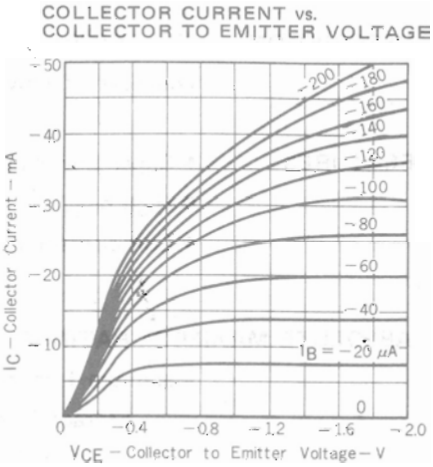
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



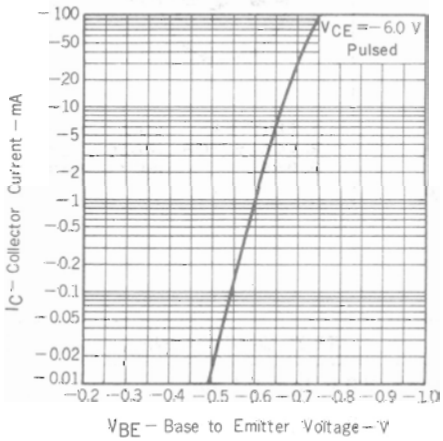
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



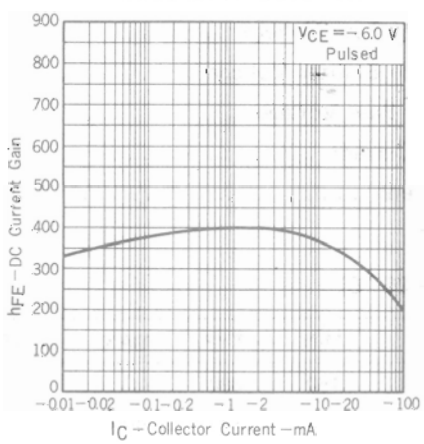
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



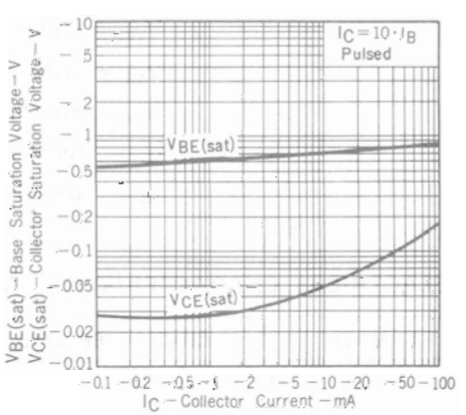
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



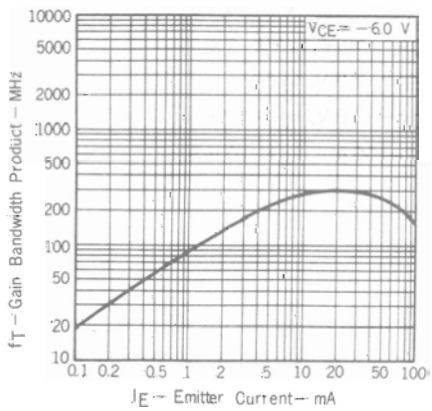
DC CURRENT GAIN vs. COLLECTOR CURRENT



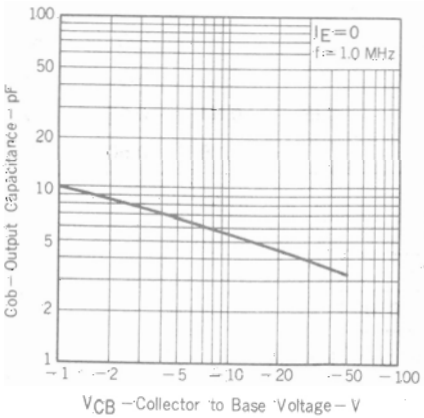
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



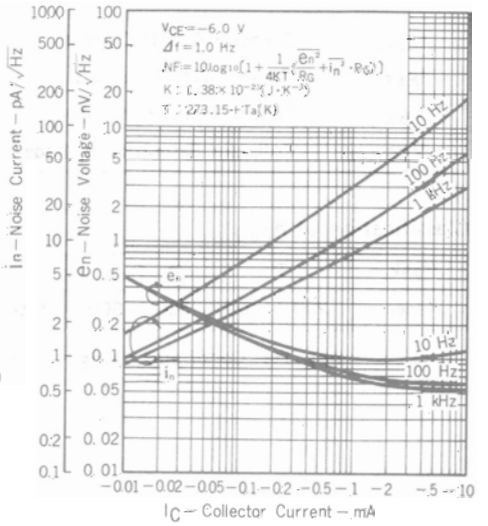
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



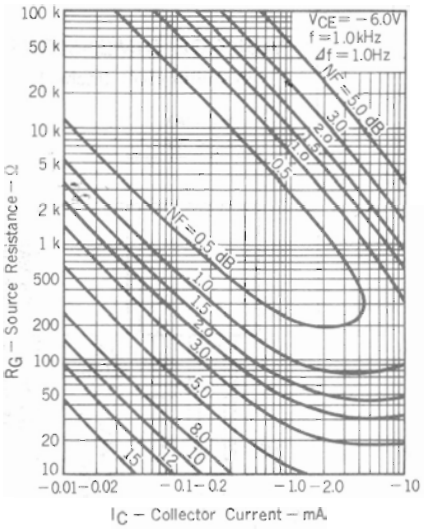
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



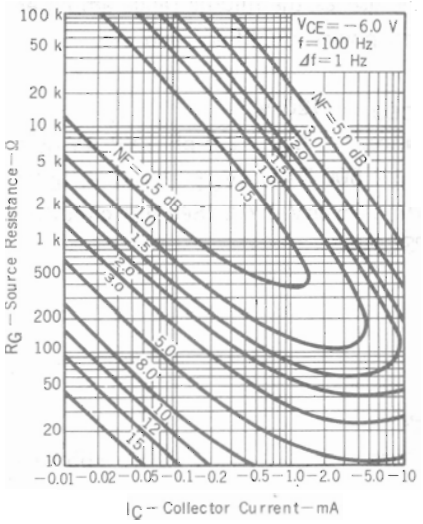
e_n AND i_n vs. COLLECTOR CURRENT



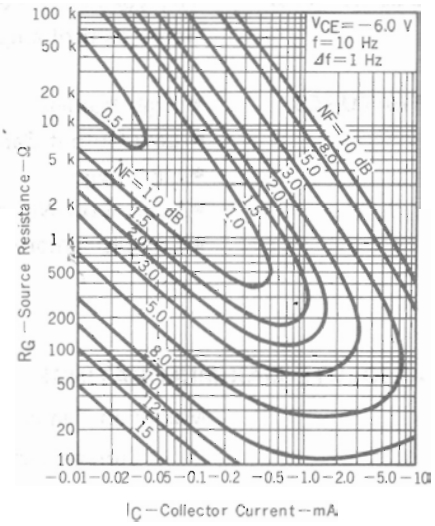
NOISE FIGURE MAP1



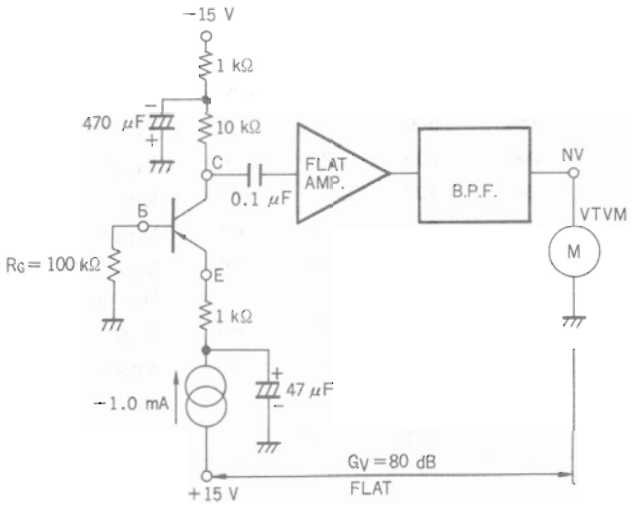
NOISE FIGURE MAP2



NOISE FIGURE MAP3



NOISE VOLTAGE TEST CIRCUIT



$V_{CE} \fallingdotseq -5$ V, $I_C = -1.0$ mA, $R_G = 100$ kΩ, $G_V = 80$ dB, FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

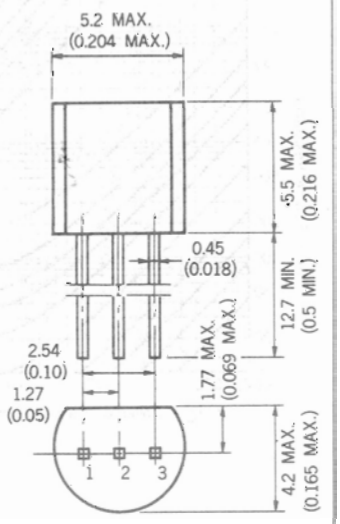
PNP SILICON TRANSISTOR
2SA992

DESCRIPTION The 2SA992 is best for use as the middle range amplifier in Hi-Fi stereo control amplifiers, power amplifiers, and etc.

FEATURES

- High Voltage. V_{CEO} : −120 V
- Low Output Capacitance. C_{ob} : 2.0 pF TYP. (V_{CB} = −30 V)
- High h_{FE}. h_{FE} : 500 TYP. (V_{CE} = −6.0 V, I_C = −1.0 mA)
- Super Low Noise. NV : 25 mV TYP. (See test circuit.)
- Complementary to 2SC1845.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −120 V
- V_{CEO} Collector to Emitter Voltage . . . . . −120 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −50 mA
- I_B Base Current . . . . . −10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	500		−	V_{CE} = −6.0 V, I_C = −0.1 mA
h_{FE2}	DC Current Gain	200	500	800	−	V_{CE} = −6.0 V, I_C = −1.0 mA
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = −6.0 V, I_E = 1.0 mA
Cob	Output Capacitance		2.0	3.0	pF	V_{CB} = −30 V, I_E = 0, f = 1.0 MHz
NV	Noise Voltage		25	40	mV	V_{CE} = −5.0 V, I_C = −1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB} = −120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−0.55	−0.61	−0.65	V	V_{CE} = −6.0 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.09	−0.30	V	I_C = −10 mA, I_B = −1.0 mA

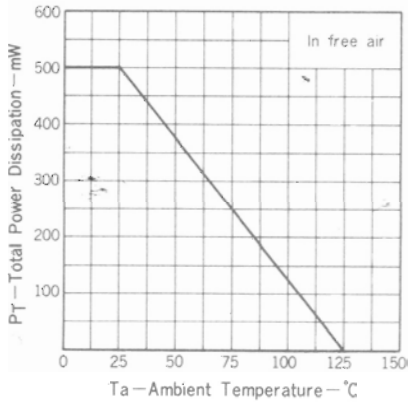
Classification of h_{FE2}

Rank	P	F	E
Range	200 − 400	300 − 600	400 − 800

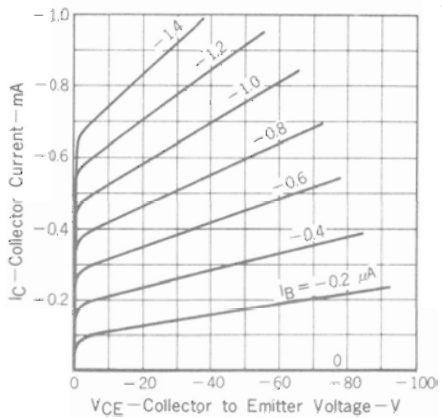
h_{FE} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

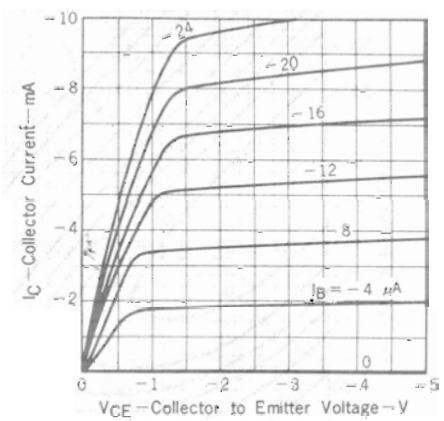
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



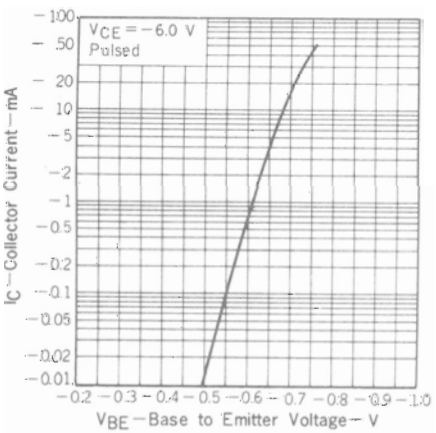
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



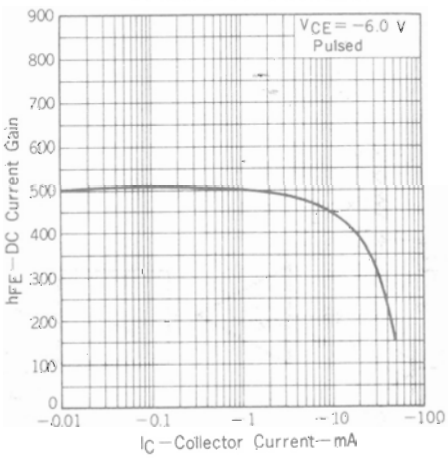
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



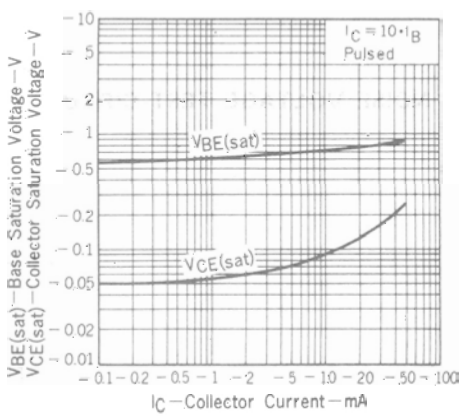
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



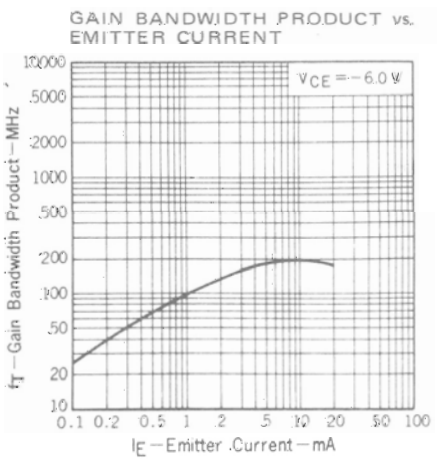
DC CURRENT GAIN vs. COLLECTOR CURRENT



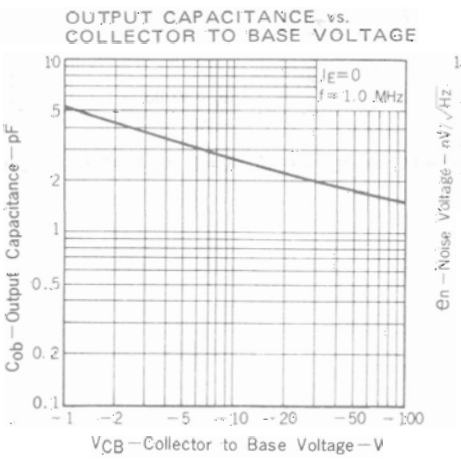
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



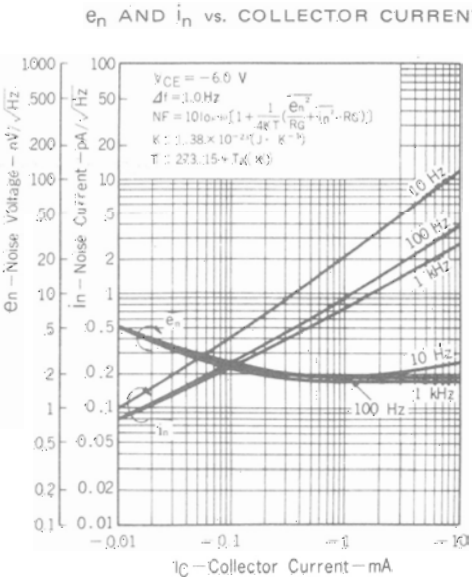
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



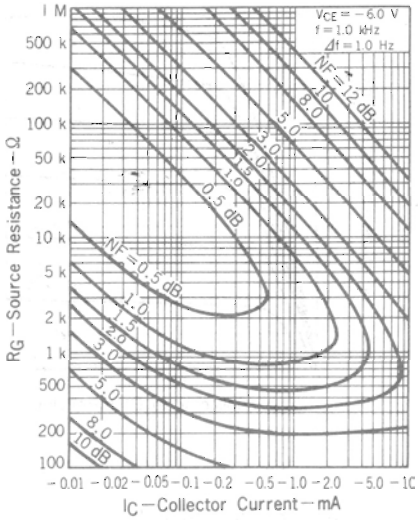
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



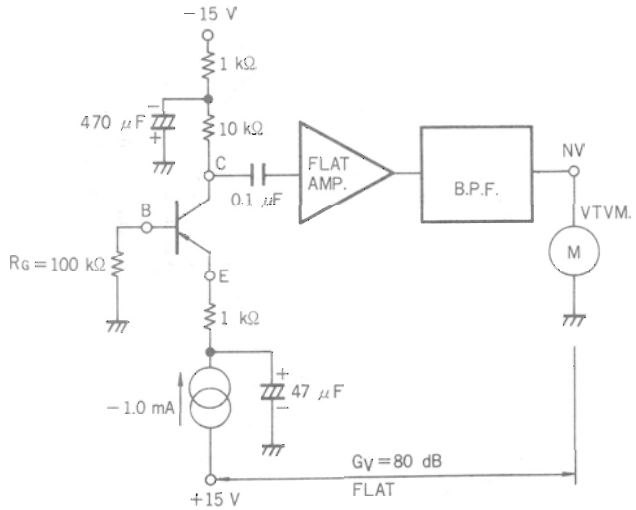
e_n AND i_n vs. COLLECTOR CURRENT



NOISE FIGURE MAP.



NOISE VOLTAGE TEST CIRCUIT



$V_{CE} \fallingdotseq -5$ V, $I_C = -1.0$ mA, $R_G = 100$ kΩ, $G_V = 80$ dB, FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

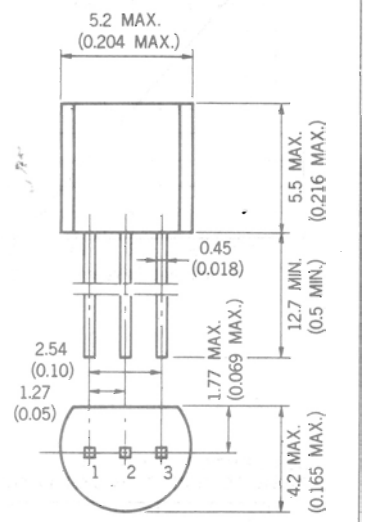
PNP SILICON TRANSISTOR
2SA1005

DESCRIPTION The 2SA1005 is designed for use in RF amplifier, conv., and oscillator of FM tuner.

FEATURES

- High gain bandwidth product: f_T = 400 MHz TYP.
  @V_{CE} = −10 V, I_E = 1.0 mA
- Small output capacitance: C_{ob} = 1.1 pF TYP.
  @V_{CB} = −10 V, f = 1.0 MHz
- Low noise figure: NF = 3.5 dB TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	−40	V
V_{CEO}	Collector to Emitter Voltage	−40	V
V_{EBO}	Emitter to Base Voltage	−4.0	V
I_C	Collector Current	−30	mA
I_B	Base Current	−10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −4.0 V, I_C = 0
h_{FE}	DC Current Gain	40	90	180	—	V_{CE} = −10 V, I_C = −1.0 mA
V_{BE}	Base to Emitter Voltage	−0.67	−0.72		V	V_{CE} = −10 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.09	−0.3	V	I_C = −10 mA, I_B = −1.0 mA
f_T	Gain Bandwidth Product	250	400		MHz	V_{CE} = −10 V, I_E = 1.0 mA
C_{ob}	Output Capacitance		1.1	2.0	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
$C_{c\cdot rb'b}$	Collector to Base Time Constant			20	ps	V_{CE} = −10 V, I_E = 1.0 mA, f = 31.9 MHz
NF	Noise Figure		3.5		dB	V_{CE} = −10 V, I_C = −1.0 mA, R_G = 500 Ω, f = 1.0 MHz

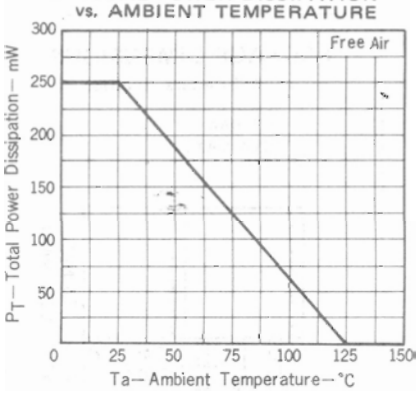
Classification of h_{FE}

Rank	M	L	K
Range	40 – 80	60 – 120	90 – 180

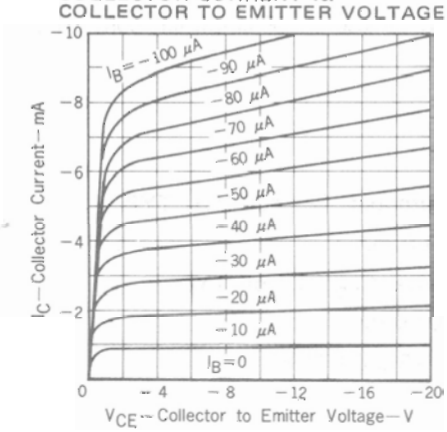
h_{FE} Test Conditions : V_{CE} = −10 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

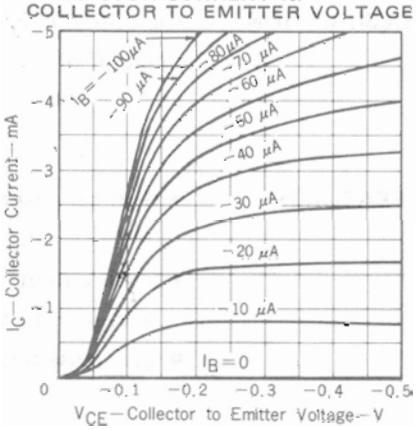
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



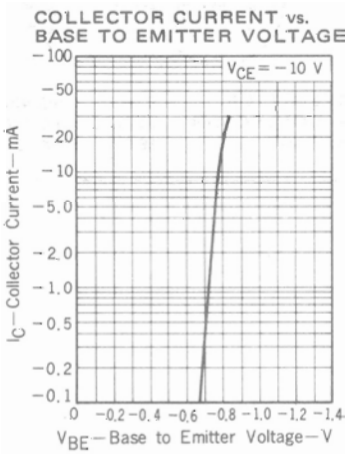
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



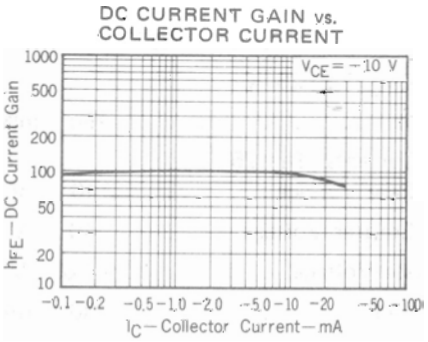
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



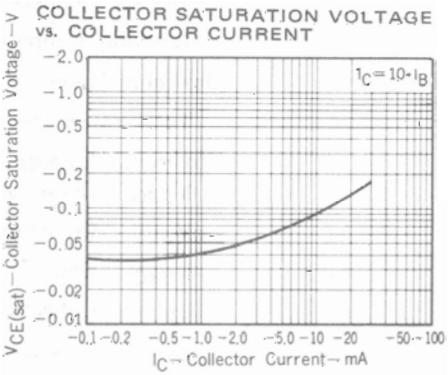
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



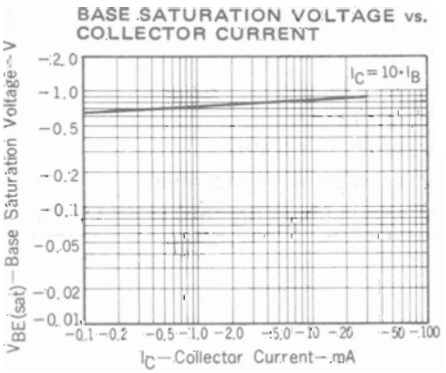
DC CURRENT GAIN vs. COLLECTOR CURRENT



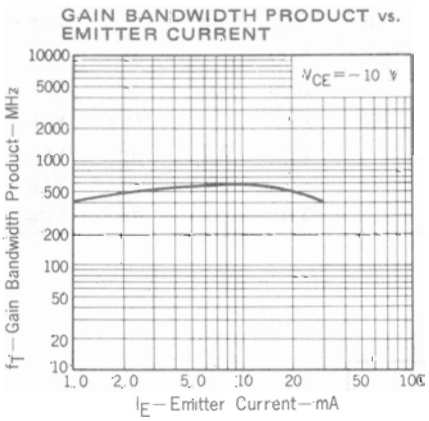
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



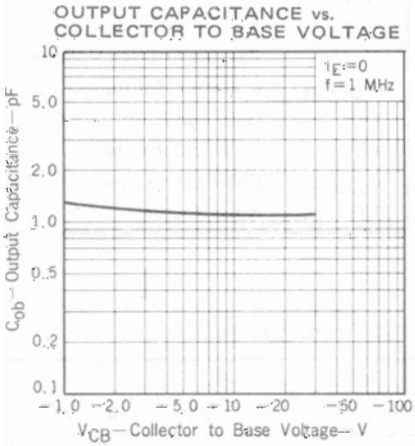
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



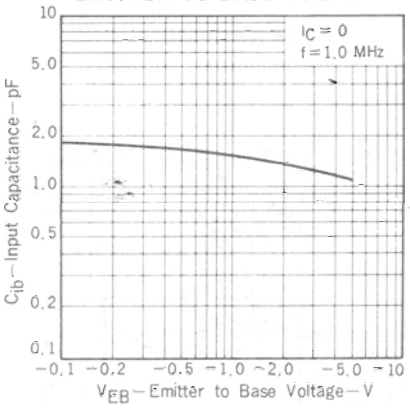
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



INPUT CAPACITANCE vs.
EMITTER TO BASE VOLTAGE



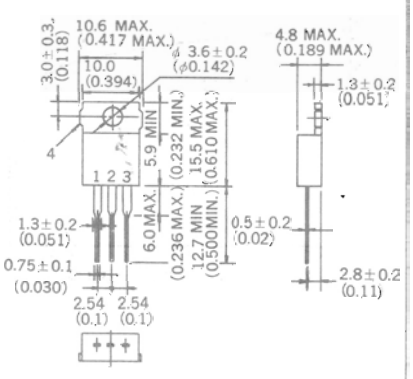
NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTORS
2SA1009,2SA1009A

DESCRIPTION The 2SA1009, 2SA1009A are PNP triple diffused transistors designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES
- Low Collector Saturation Voltage.
- High Speed Switching.
- Wide Reverse Bias Safe Operating Area.

PACAKGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

Total Power Dissipation . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SA1009/2SA1009A	
V_{CBO}	Collector to Base Voltage	−350/ −400	V
V_{CEO}	Collector to Emitter Voltage	−350/ −400	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−2.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	−4.0	A
$I_{B(DC)}$	Base Current (DC)	−1.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT.	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = −0.3 A, I_{B1} = −I_{B2} = −60 mA, R_L = 500 Ω, V_{CC} ≒ −150 V
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			1.0	μs	
h_{FE1}	DC Current Gain**	20		200	—	V_{CE} = −5.0 V, I_C = −0.1 A
h_{FE2}	DC Current Gain**	10			—	V_{CE} = −5.0 V, I_C = −0.3 A
$V_{CE(sat)}$	Collector Saturation Voltage**			−1.0	V	I_C = −0.3 A, I_B = −60 mA
$V_{BE(sat)}$	Base Saturation Voltage**			−1.2	V	I_C = −0.3 A, I_B = −60 mA
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−350/−400			V	I_C = −0.3 A, I_B = −60 mA, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	−350/−400			V	I_C = −0.3 A, I_{B1} = −I_{B2} = −60 mA, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	−350/−400			V	I_C = −0.6 A, I_{B1} = −0.2 A, −I_{B2} = 60 mA, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −350/−400 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −350/−400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −350/−400 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −350/−400 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0

**PW ≤ 350 μs, Duty Cycle ≤ 2 %

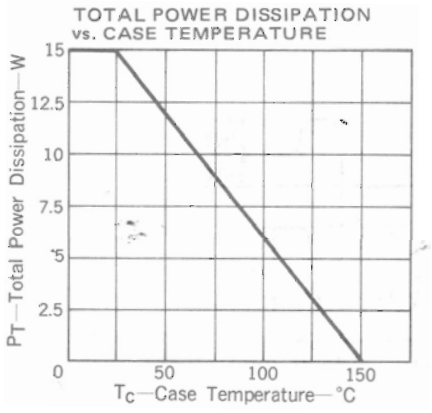
Classification of h_{FE1}

Rank	M	L	K	J	H
Range	20 to 40	30 to 60	40 to 80	60 to 120	100 to 200

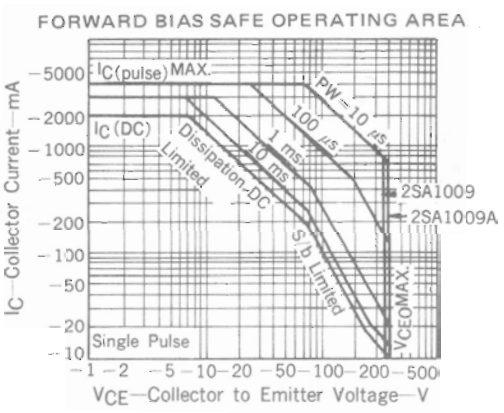
Test Conditions: V_{CE} = −5.0 V, I_C = −0.1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

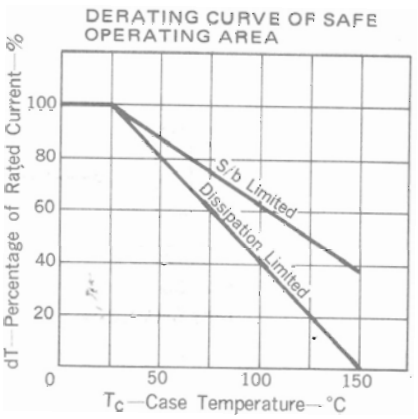
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



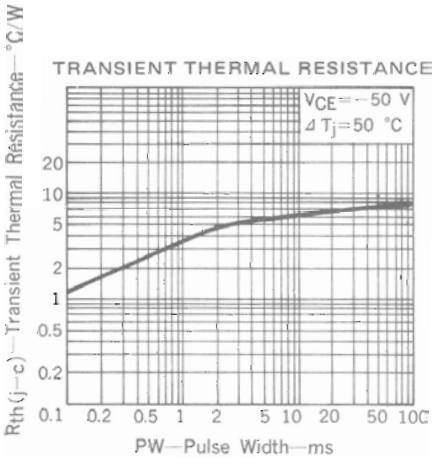
FORWARD BIAS SAFE OPERATING AREA



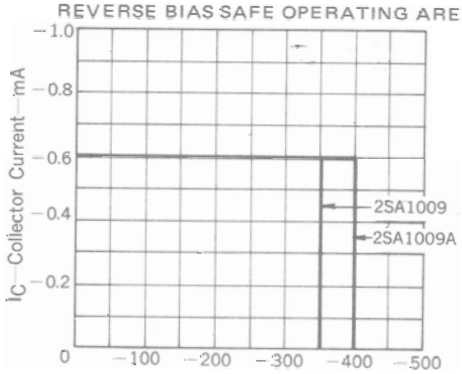
DERATING CURVE OF SAFE OPERATING AREA



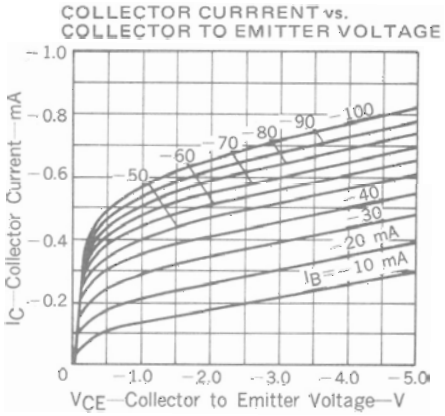
TRANSIENT THERMAL RESISTANCE



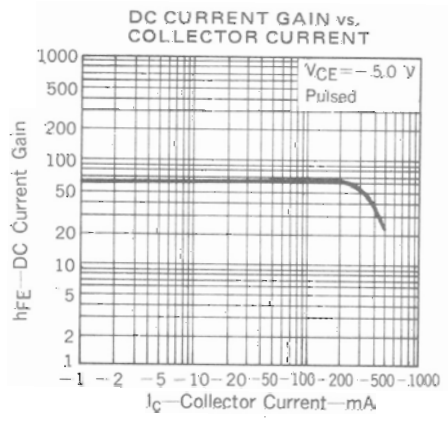
REVERSE BIAS SAFE OPERATING AREA



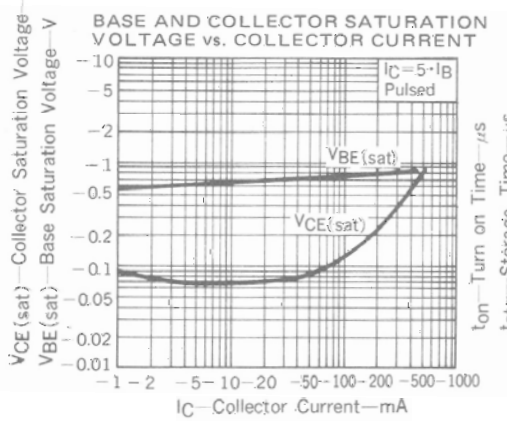
COLLECTOR CURRRENT vs. COLLECTOR TO EMITTER VOLTAGE



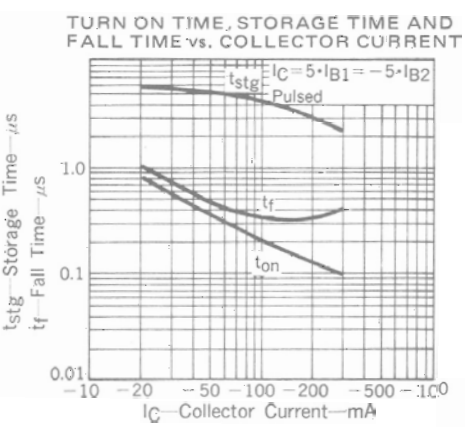
DC CURRENT GAIN vs. COLLECTOR CURRENT



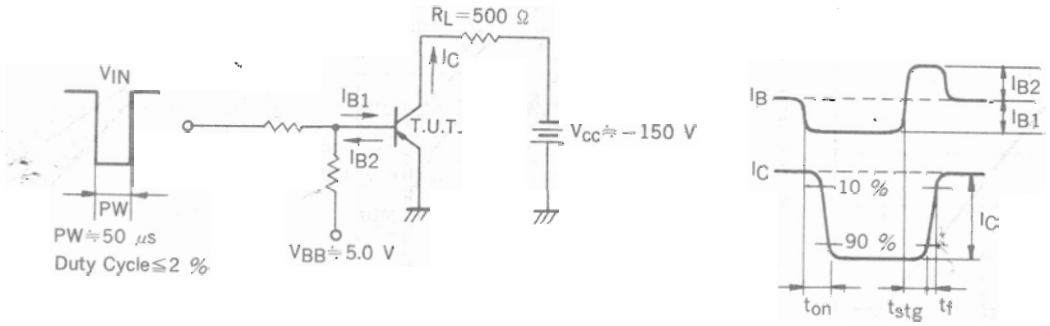
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

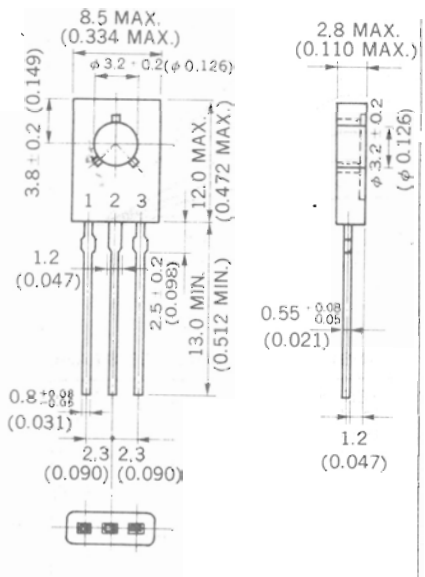
PNP SILICON POWER TRANSISTOR
2SA1142

DESCRIPTION The 2SA1142 is designed for use in Audio frequency power amplifier.

FEATURES

- High voltage. $V_{CEO} > -180$ V
- Low C_{ob}, High f_T
  f_T = 180 MHz, C_{ob} = 4.5 pF
- Complementary to the NEC 2SC2682 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations
- Total Power Dissipation (T_a = 25 °C) . . . . . 1.2 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 10 W

Maximum Voltages and Current (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −180 V
- V_{CEO} Collector to Emitter Voltage . . . . . −180 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −100 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200			V_{CE} = −5.0 V, I_C = −1.0 mA*
h_{FE2}	DC Current Gain	100	200	320		V_{CE} = −5.0 V, I_C = −10 mA*
f_T	Gain Bandwidth Product		180		MHz	V_{CE} = −10 V, I_C = −20 mA
C_{ob}	Output Capacitance		4.5	7.0	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
NF	Noise Figure		4.0		dB	V_{CE} = −10 V, I_C = −1.0 mA, R_g = 10 kΩ, f = 1.0 kHz
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB} = −180 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB} = −3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		−0.16	−0.5	V	I_C = −50 mA, I_B = −5.0 mA*
$V_{BE(sat)}$	Base Saturation Voltage		−0.8	−1.5	V	I_C = −50 mA, I_B = −5.0 mA*

*Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %

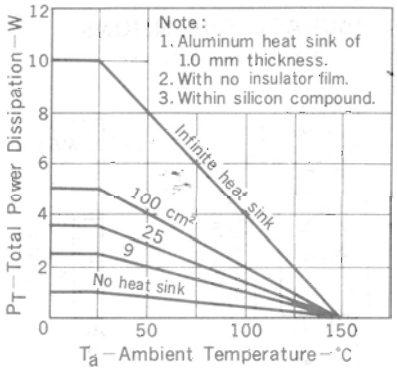
Classification of h_{FE2}

Rank	Q	P
Range	100 to 200	160 to 320

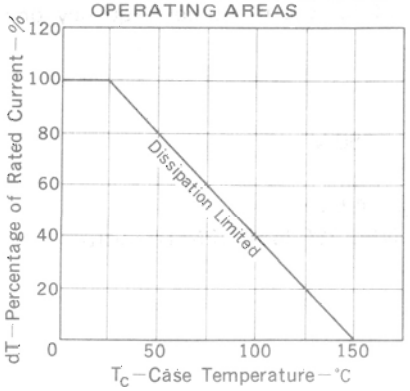
Test Conditions : V_{CE} = −5.0 V, I_C = −10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

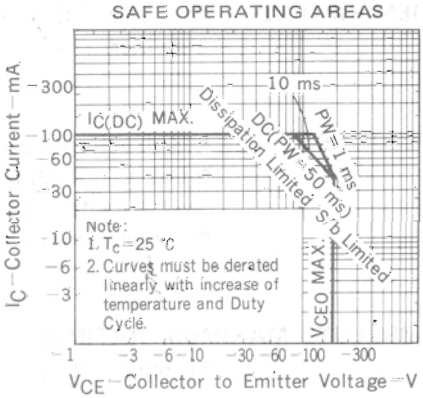
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



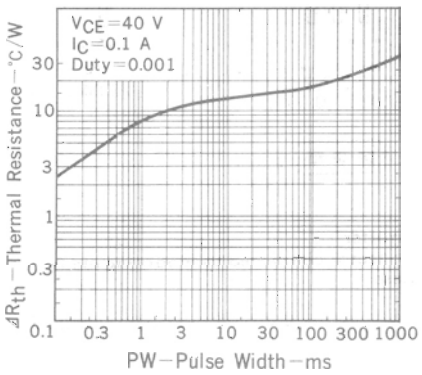
DERATING CURVE OF SAFE OPERATING AREAS



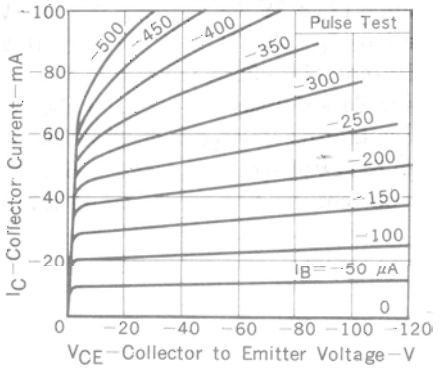
SAFE OPERATING AREAS



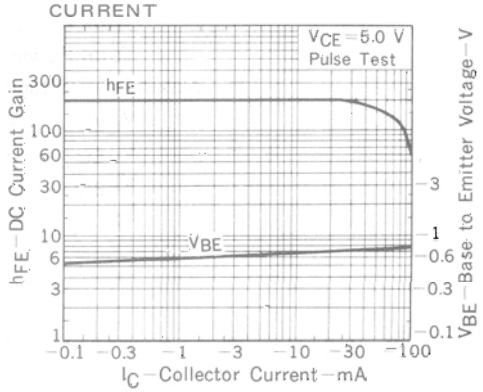
TRANSIENT THERMAL RESISTANCE



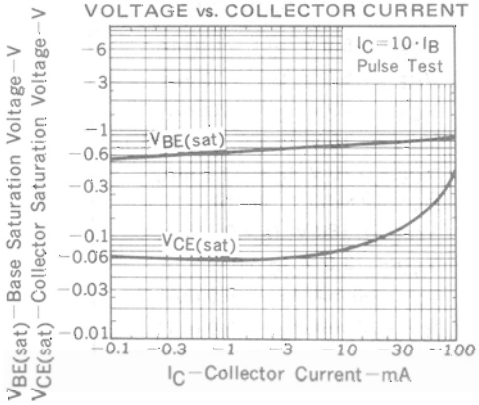
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



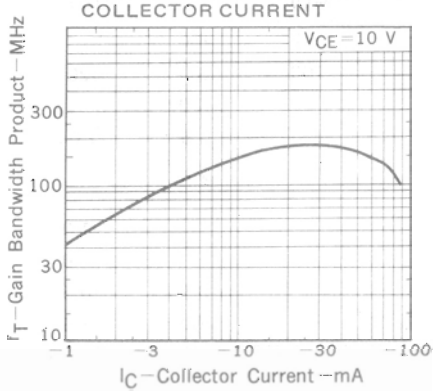
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



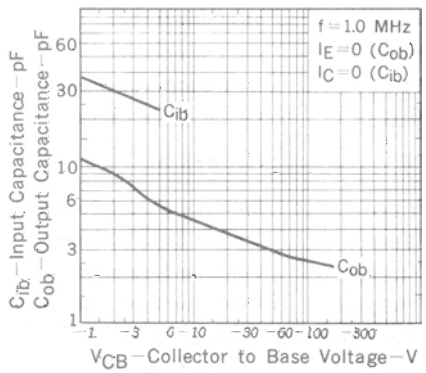
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWITH PRODUCT vs. COLLECTOR CURRENT



OUTPUT AND INPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

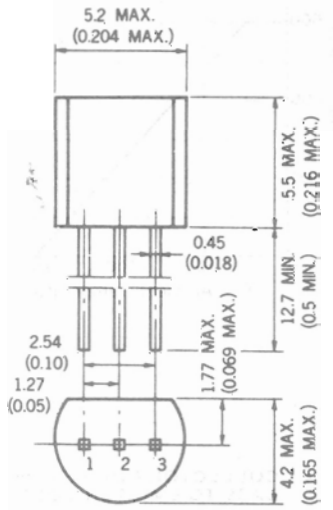
PNP SILICON TRANSISTOR
2SA1153

DESCRIPTION The 2SA1153 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.
- Low Collector Saturation Voltage.
- Complementary to the NEC 2SC2720 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Current (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −40 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current (DC) . . . . . −500 mA

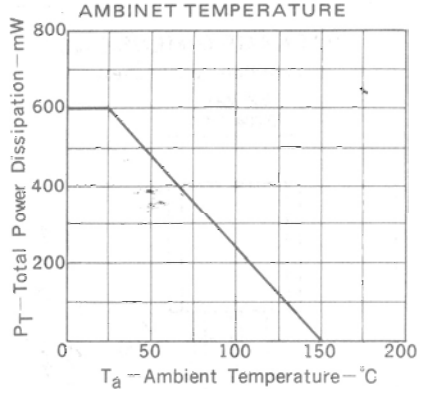
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			35	ns	See Test Circuit.
t_{off}	Turn off Time			255	ns	See Test Circuit.
t_{stg}	Storage Time			225	ns	See Test Circuit.
f_T	Gain Bandwidth Product	150	400		MHz	V_{CE} = −10 V, I_E = 20 mA
C_{ob}	Output Capacitance		5.0	8.0	pF	V_{CB} = −10 V, I_E = 0, f = 1 MHz
h_{FE1}*	DC Current Gain	50	140	300	—	V_{CE} = −2.0 V, I_C = −150 mA
h_{FE2}*	DC Current Gain	20	50		—	V_{CE} = −2.0 V, I_C = −500 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.45	−0.75	V	I_C = −500 mA, I_B = −50 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−1.0	−1.3	V	I_C = −500 mA, I_B = −50 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB} = −4.0 V, I_C = 0

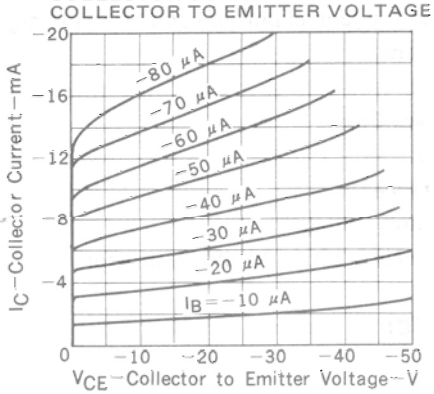
* Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

TYPICAL CHARACTERISTICS (T_a = 25 °C)

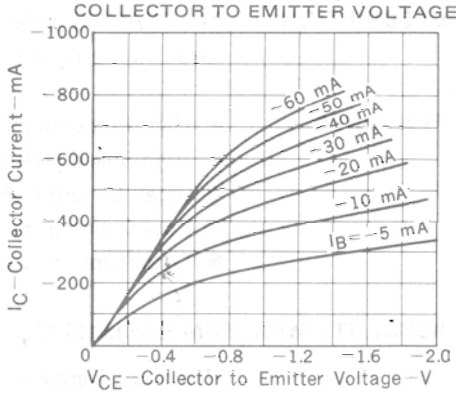
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



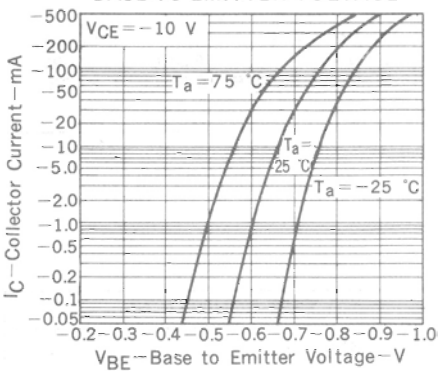
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



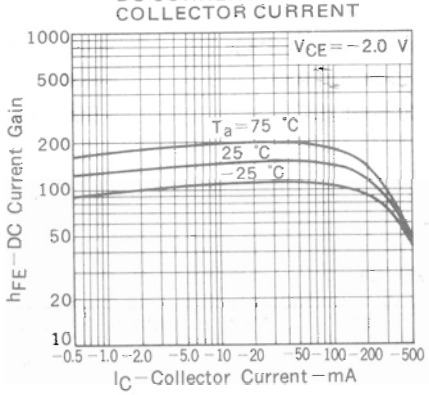
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



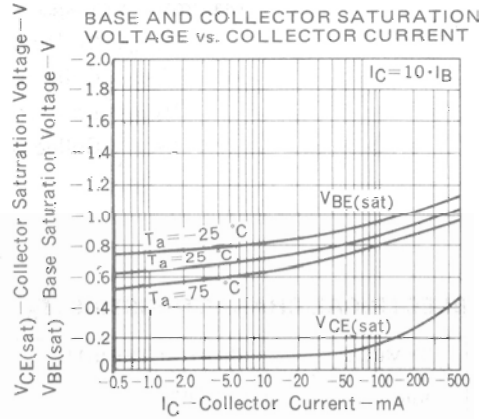
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



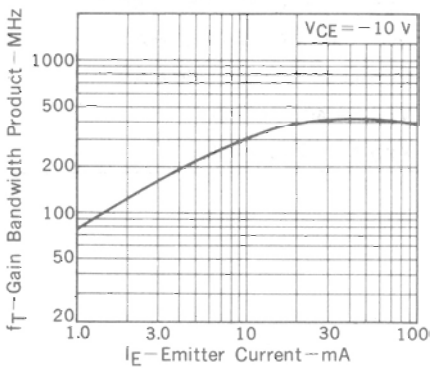
DC CURRENT GAIN vs. COLLECTOR CURRENT



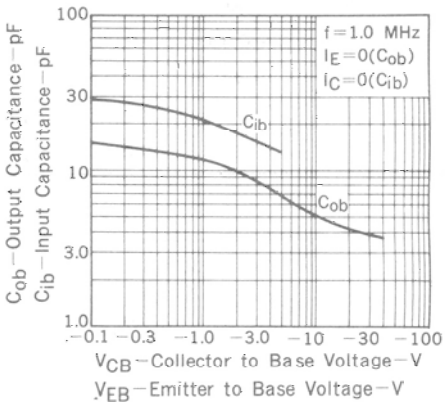
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



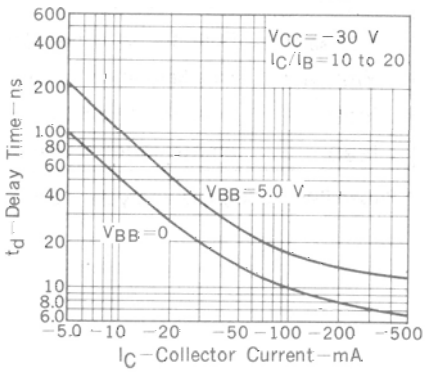
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT

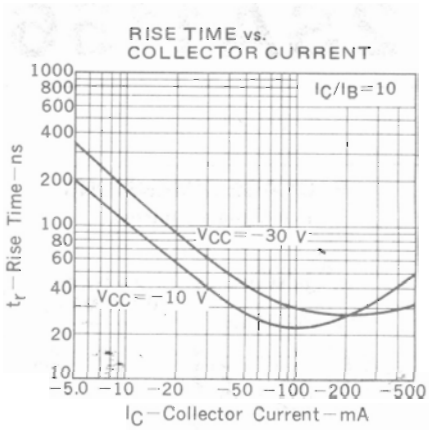


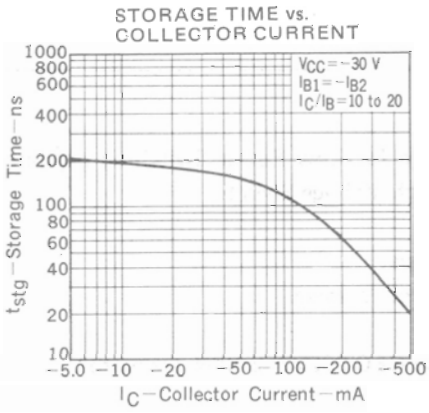
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE

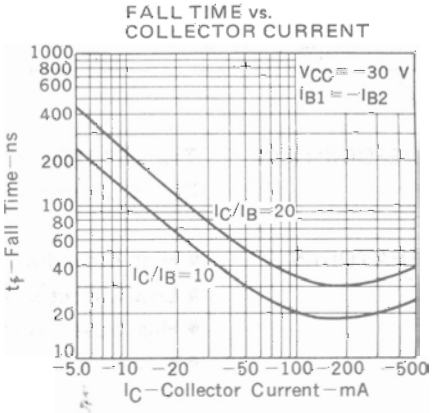


DELAY TIME vs. COLLECTOR CURRENT

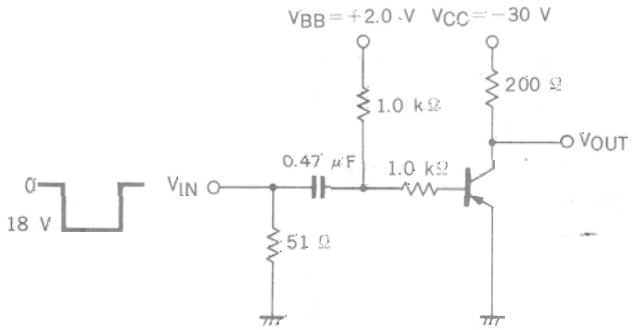






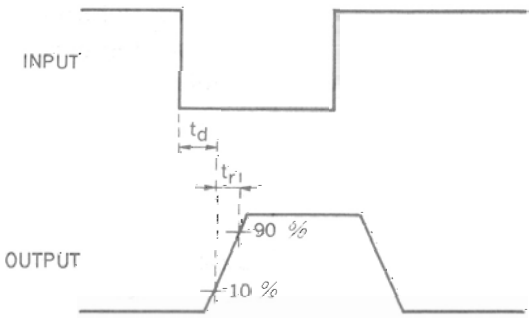


SWITCHING TIME TEST CIRCUIT

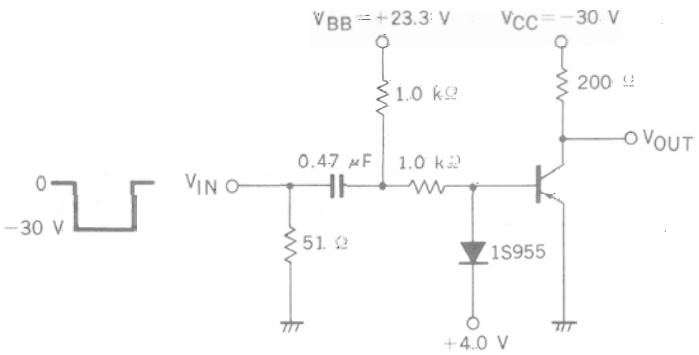


t_r<2.0 ns
PW=1.0 μs
DC=2 %

t_{on} SWITCHING

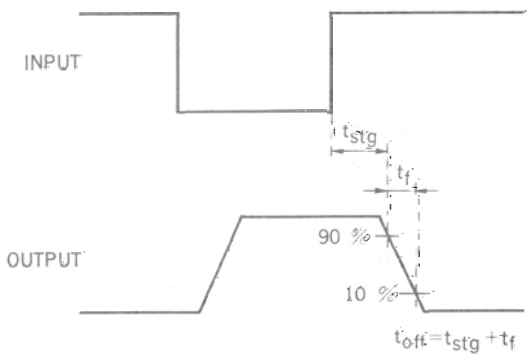


VOLTAGE WAVEFORMS



t_r≪2.0 ns
PW≫1.0 μs
DC=2 %

t_{off} SWITCHING



VOLTAGE WAVEFORMS

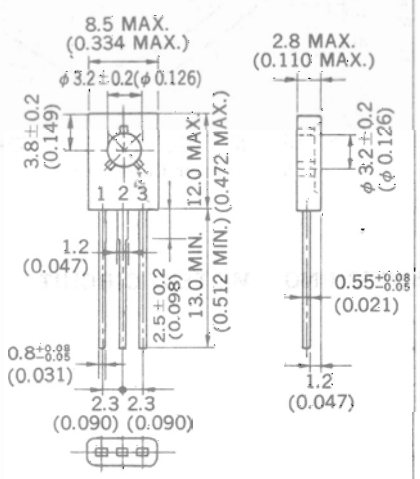
NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SA1156

DESCRIPTION The 2SA1156 is suitable for Low Power Switching regulator, DC-DC converter and High Voltage Switch.

FEATURES
- High Breakdown Voltage.
- Low Collector Saturation Voltage.
- High Speed Switching.
- Complementary to the NEC 2SC2752 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−400 V
V_{CEO}	Collector to Emitter Voltage	−400 V
V_{EBO}	Emitter to Base Voltage	−7.0 V
$I_{C(DC)}$	Collector Current	−0.5 A
$I_{C(pulse)}$*	Collector Current	−1.0 A
$I_{B(DC)}$	Base Current	−0.25 A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE} **	DC Current Gain	30		200	—	V_{CE} = −5.0 V, I_C = −100 mA
t_{on}	Turn On Time			1.0	μs	I_C = −100 mA, R_L = 1.5 kΩ
t_{stg}	Storage Time			4.0	μs	I_{B1} = −10 mA, I_{B2} = 20 mA, V_{CC} ≒ −150 V
t_f	Fall Time			1.0	μs	PW = 50 μs, Duty Cycle ≦ 2 %
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−400			V	I_C = −100 mA, I_B = −10 mA, L = 20 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	−400			V	I_C = −200 mA, I_{B1} = −I_{B2} = −20 mA $V_{BE(OFF)}$ = 5.0 V, L = 10 mH, Clamped.
I_{CBO}	Collector Cutoff Current			−100	μA	V_{CB} = −400 V, I_E = 0
I_{CEX1}	Collector Cutoff Current			−100	μA	V_{CE} = −400 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −400 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage			−1.0	V	I_C = −100 mA, I_B = −10 mA
$V_{BE(sat)}$**	Base Saturation Voltage			−1.2	V	I_C = −100 mA, I_B = −10 mA

** Pulsed / PW ≦ 350 μs, Duty Cycle ≦ 2 %

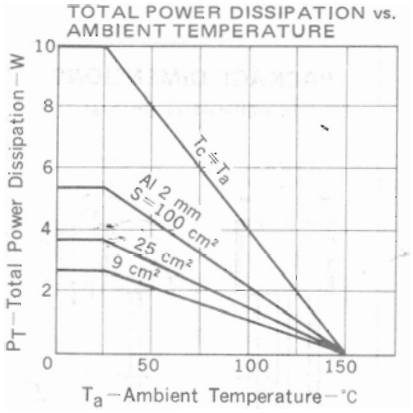
Classification of h_{FE}

Rank	N	M	L	K
Range	30 to 60	40 to 80	60 to 120	100 to 200

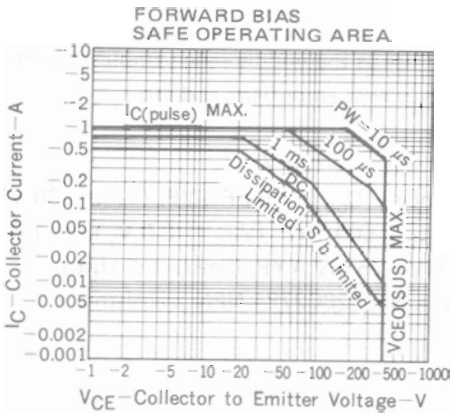
Test Conditions: V_{CE} = −5.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

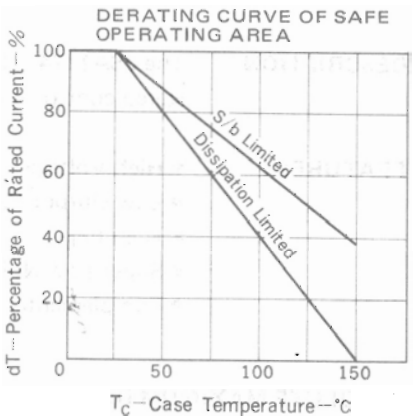
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



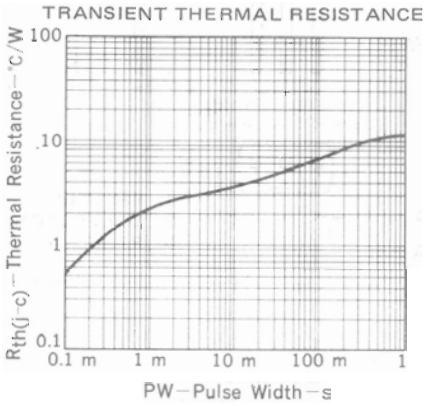
FORWARD BIAS SAFE OPERATING AREA



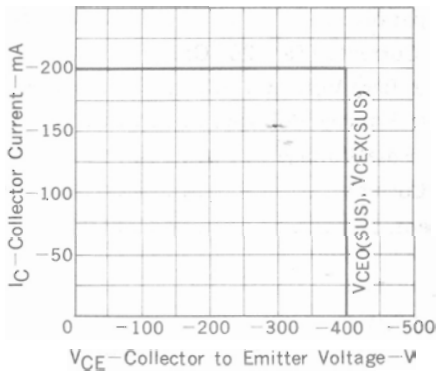
DERATING CURVE OF SAFE OPERATING AREA



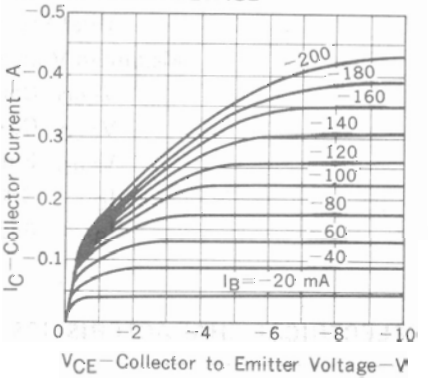
TRANSIENT THERMAL RESISTANCE



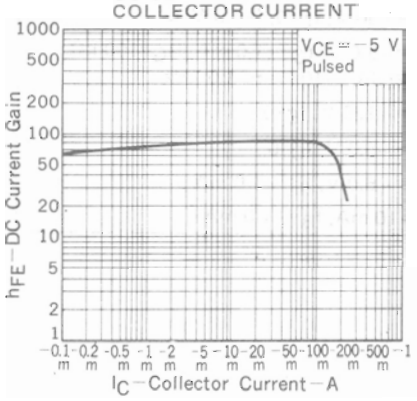
REVERSE BIAS SAFE OPERATING AREA



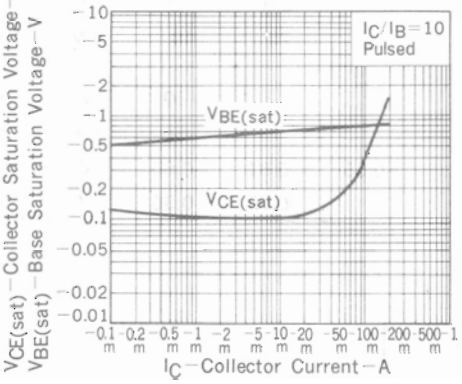
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



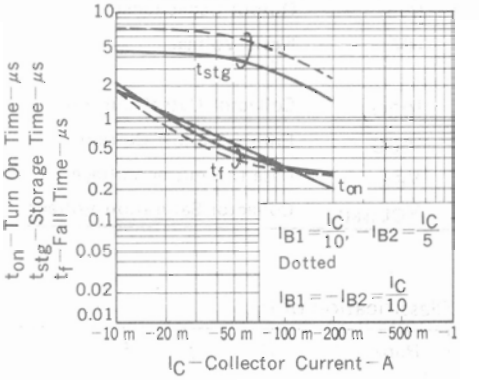
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

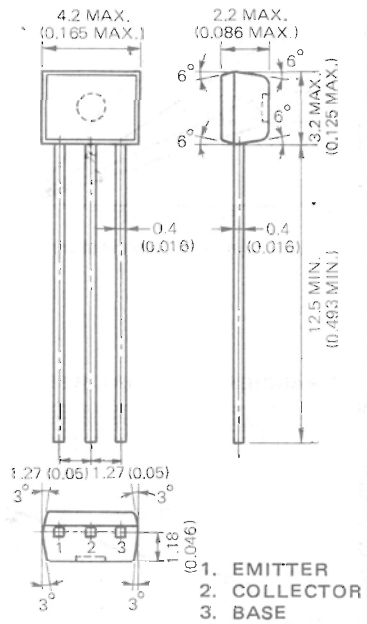
PNP SILICON TRANSISTOR
2SA1174

DESCRIPTION The 2SA1174 is best for use as the middle range amplifier in Hi-Fi stereo control amplifiers, power amplifiers, and etc.

FEATURES

- High Voltage. V_{CEO} : −120 V
- Low Output Capacitance. C_{ob} : 2.0 pF TYP. (V_{CB}=−30 V)
- High h_{FE}. h_{FE} : 500 TYP. (V_{CE}=−6.0 V, I_C=−1.0 mA)
- Super Low Noise. NV : 25 mV TYP. (See test circuit.)
- Complementary to the NEC 2SC2784 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −120 V
- V_{CEO} Collector to Emitter Voltage . . . . . −120 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −50 mA
- I_B Base Current. . . . . −10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	500		−	V_{CE}=−6.0 V, I_C=−0.1 mA
h_{FE2}	DC Current Gain	200	500	800	−	V_{CE}=−6.0 V, I_C=−1.0 mA
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE}=−6.0 V, I_E=−1.0 mA
Cob	Output Capacitance		2.0	3.0	pF	V_{CB}=−30 V, I_E=0, f=1.0 MHz
NV	Noise Voltage		25	40	mV	V_{CE}=−5.0 V, I_C=−1.0 mA, R_G=100 kΩ Gv=80 dB, f=10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB}=−120 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB}=−5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55	−0.61	−0.65	V	V_{CE}=−6.0 V, I_C=−1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.09	−0.30	V	I_C=−10 mA, I_B=−1.0 mA

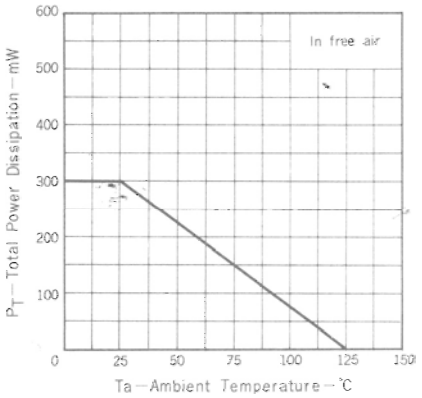
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

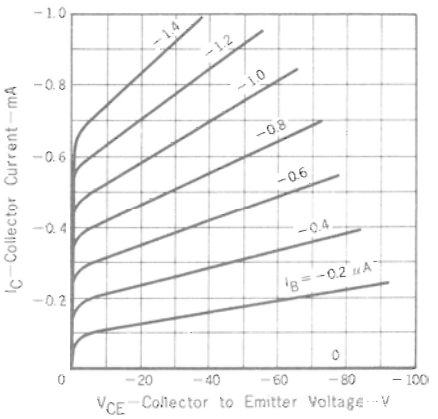
h_{FE2} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

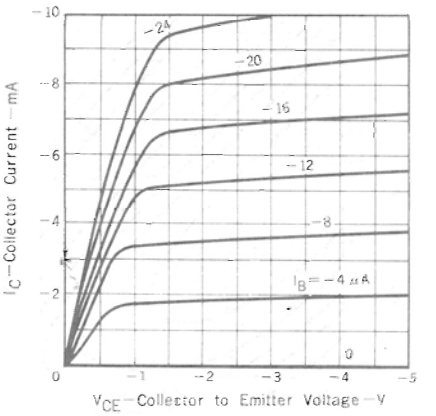
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



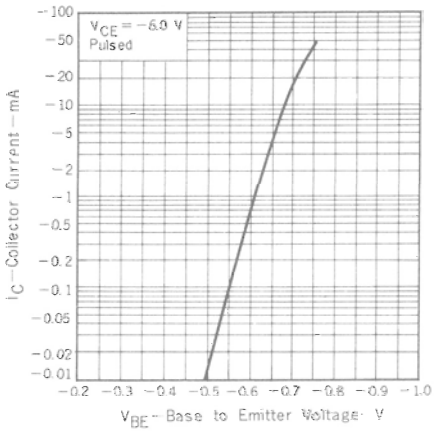
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



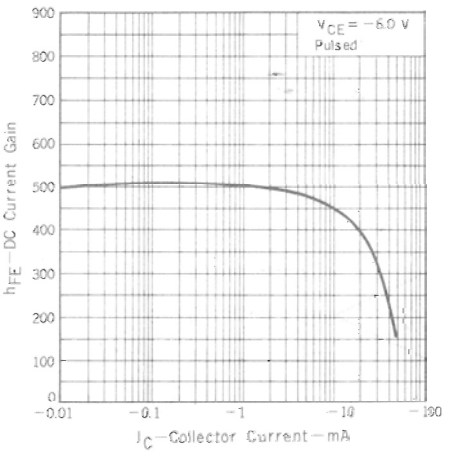
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



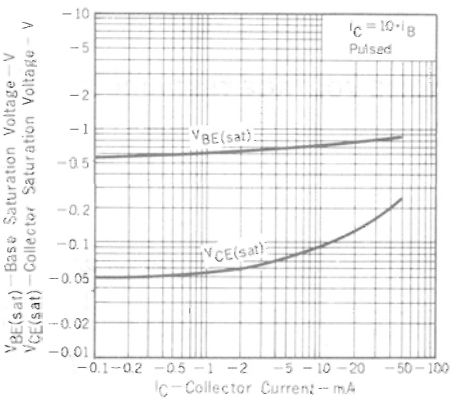
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



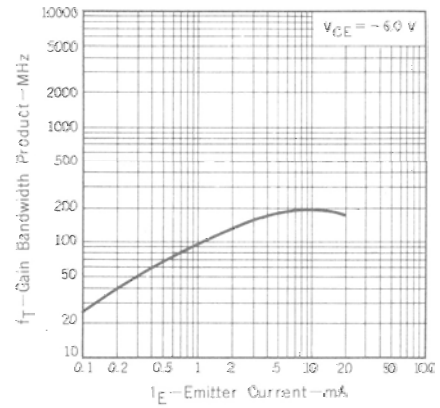
DC CURRENT GAIN vs. COLLECTOR CURRENT



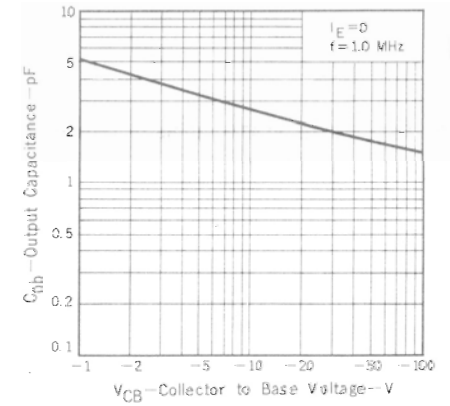
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



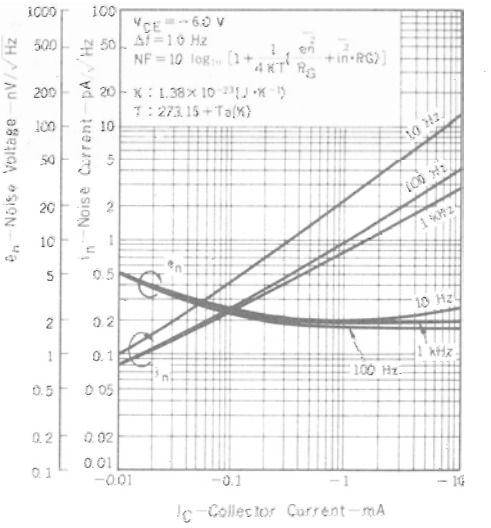
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



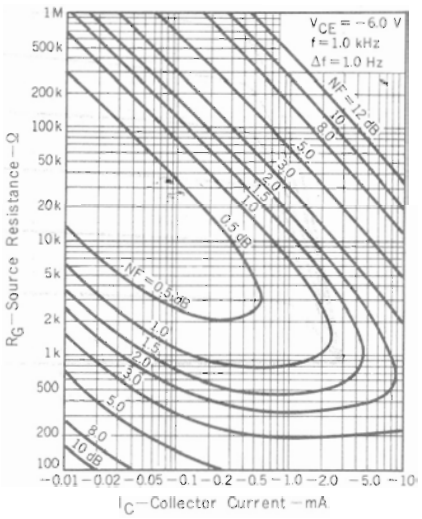
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



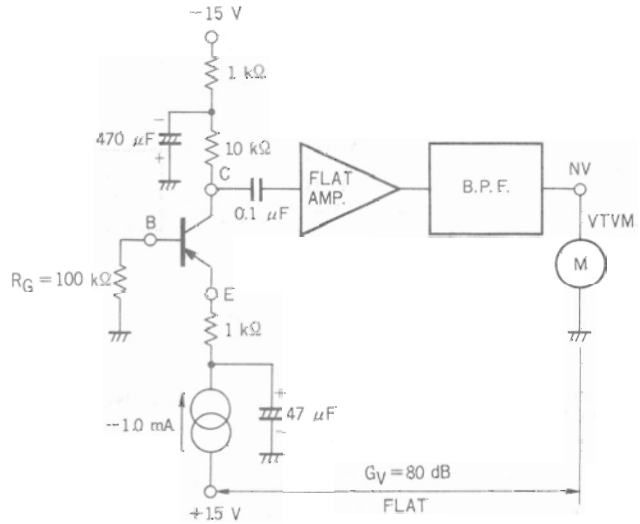
e_n AND i_n vs. COLLECTOR CURRENT



NOISE FIGURE MAP



NOISE VOLTAGE TEST CIRCUIT



V_{CE} = −5 V, I_C = −1.0 mA, R_G = 100 kΩ, G_V = 80 dB, FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

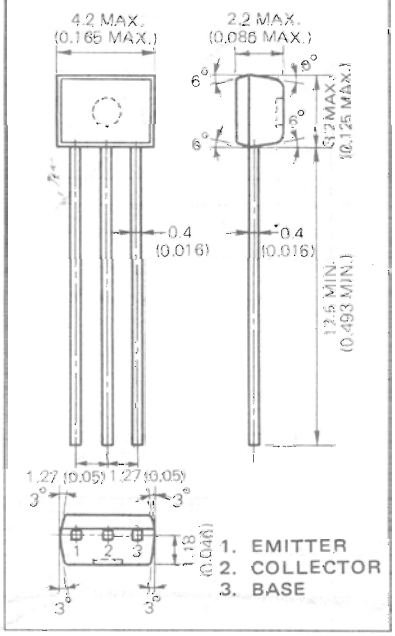
PNP SILICON TRANSISTOR
2SA1175

DESCRIPTION The 2SA1175 is designed for use in driver stage of AF amplifier.

FEATURES

- High h_{FE} and excellent linearity : 200 TYP.
  h_{FE} (I_C = −1.0 mA)
- Complementary to the NEC 2SC2785 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −100 mA
- I_B Base Current . . . . . −20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	110	200	600	–	V_{CE}=−6.0 V, I_C=−1.0 mA
NF	Noise Figure		6.0	20	dB	V_{CE}=−6.0 V, I_C=−0.3 mA, R_G=10 kΩ, f=100 Hz
f_T	Gain Bandwidth Product	50	180		MHz	V_{CE}=−6.0 V, I_E=−1.0 mA
C_{ob}	Output Capacitance		4.5	6.0	pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB}=−60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB}=−5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55	−0.62	−0.65	V	V_{CE}=−6.0 V, I_C=−1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.3	V	I_C=−100 mA, I_B=−10 mA

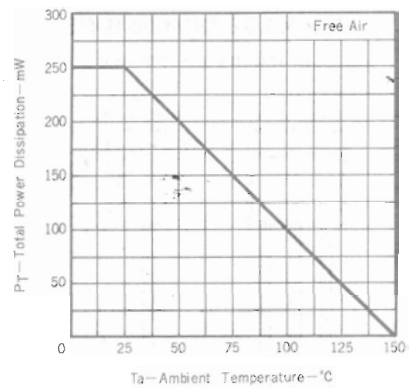
Classification of h_{FE}

Rank	RF	JF	HF	FF	EF	KF
Range	110 – 180	135 – 220	170 – 270	200 – 320	250 – 400	300 – 600

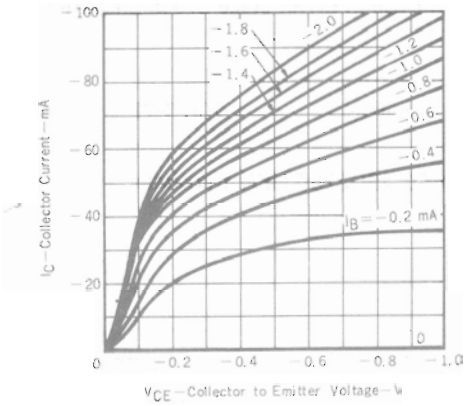
h_{FE} Test Conditions : V_{CE}=−6.0 V, I_C=−1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

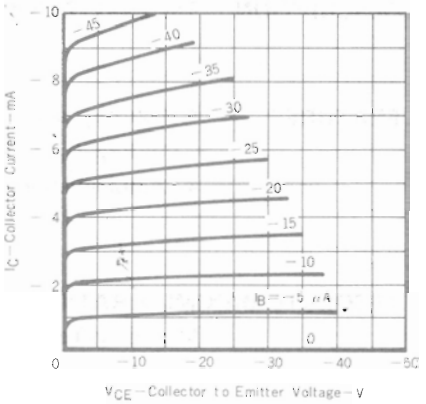
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



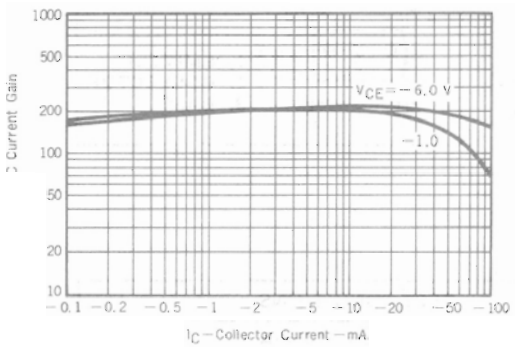
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



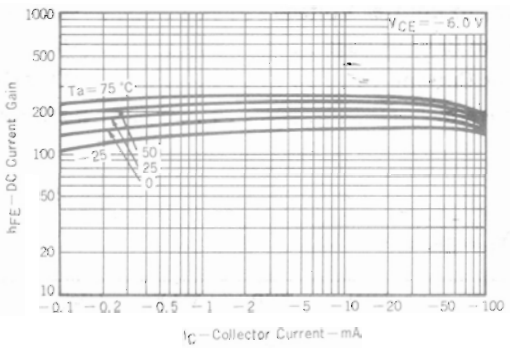
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



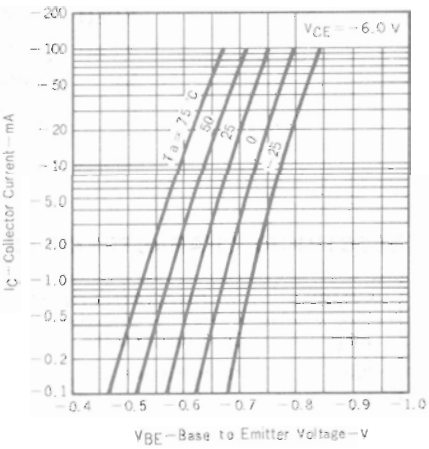
DC CURRENT GAIN vs. COLLECTOR CURRENT



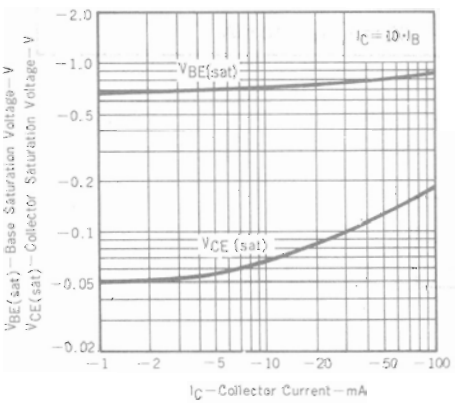
DC CURRENT GAIN vs. COLLECTOR CURRENT



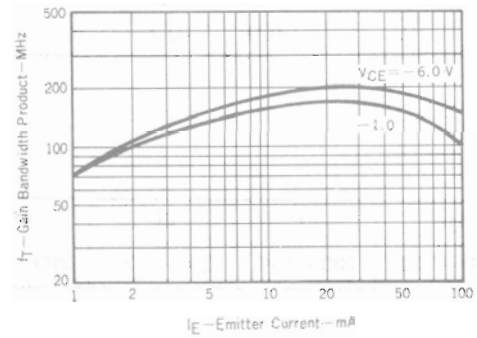
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



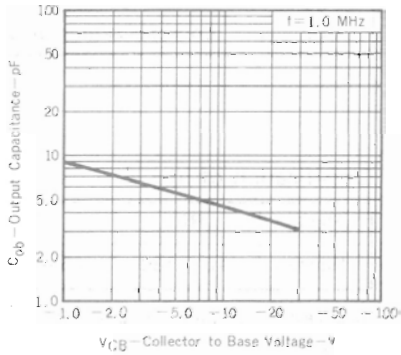
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



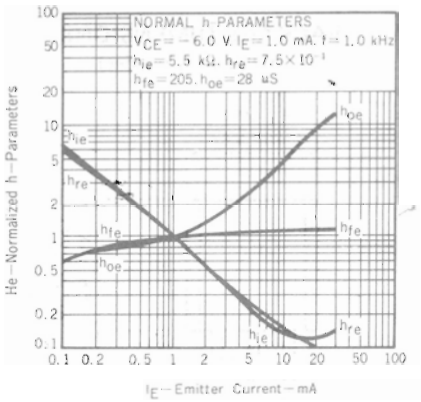
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



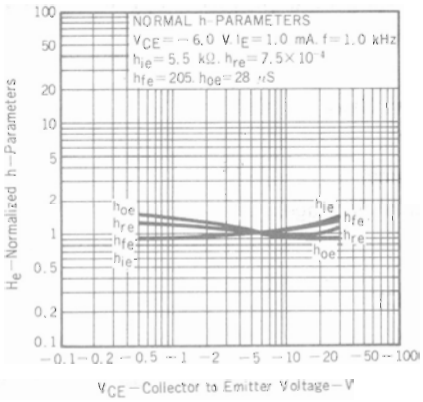
OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



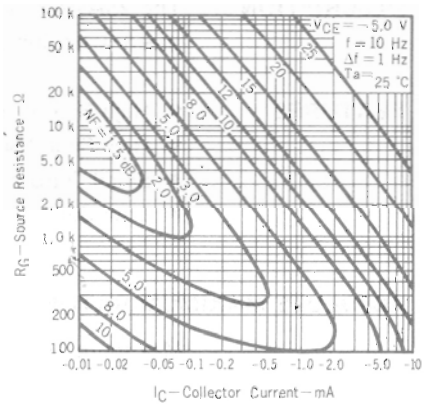
NORMALIZED h-PARAMETERS vs. EMITTER CURRENT



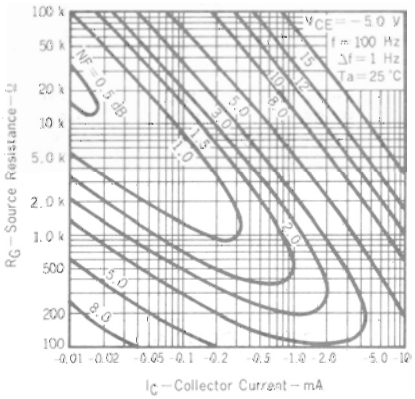
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



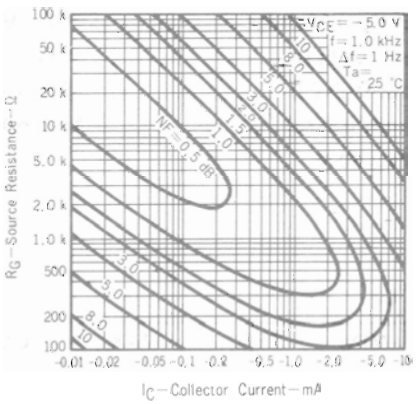
NOISE FIGURE MAP 1



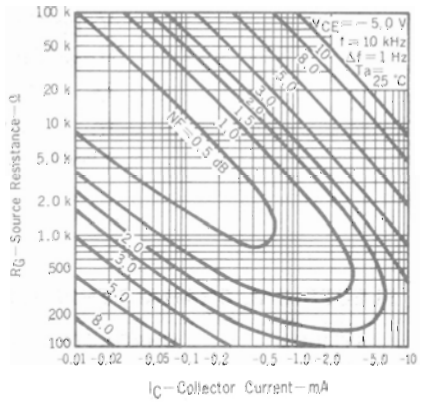
NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NOISE FIGURE MAP 4



NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR

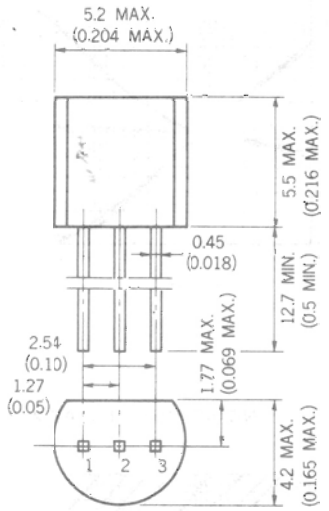
2SA1206

DESCRIPTION The 2SA1206 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Currents (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −15 V
- V_{CEO} Collector to Emitter Voltage . . . . . −15 V
- V_{EBO} Emitter to Base Voltage . . . . . −4.5 V
- I_C Collector Current (D.C.) . . . . . −50 mA
- I_C Collector Current (pulse) * . . . . . −100 mA

* PW ≦ 2 ms, duty cycle ≦ 50 %

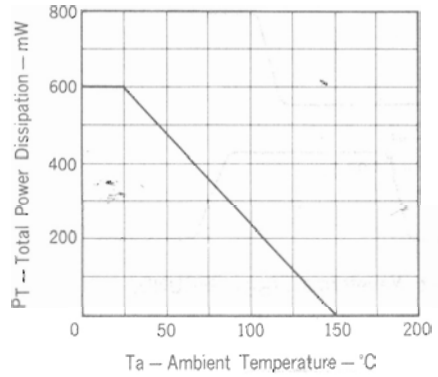
ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time		9.0	20	ns	See test circuit.
t_{off}	Turn-off Time		19	40	ns	See test circuit.
t_{stg}	Storage Time		16	40	ns	See test circuit.
f_T	Gain Bandwidth Product	800	1800		MHz	V_{CE}=−10 V, I_E=10 mA, f=100 MHz
C_{ob}	Output Capacitance		2.0	3.0	pF	V_{CB}=−5.0 V, I_E=0, f=1 MHz
h_{FE1}*	DC Current Gain	50	80	150	–	V_{CE}=−1.0 V, I_C=−10 mA
h_{FE2}*	DC Current Gain	30	70		–	V_{CE}=−1.0 V, I_C=−1.0 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.09	−0.20	V	I_C=−10 mA, I_B=−1.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.80	−0.95	V	I_C=−10 mA, I_B=−1.0 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB}=−8.0 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB}=−3.0 V, I_C=0

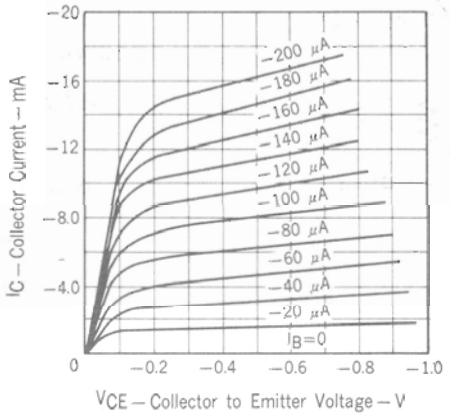
* Pulsed PW ≦ 350 μs, duty cycle ≦ 2 %

TYPICAL CHARACTERISTICS (Ta = 25 °C)

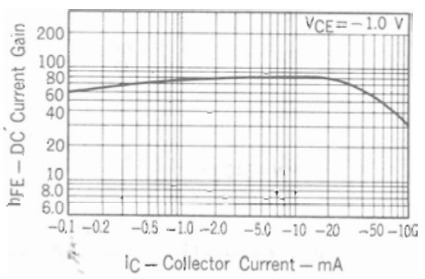
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



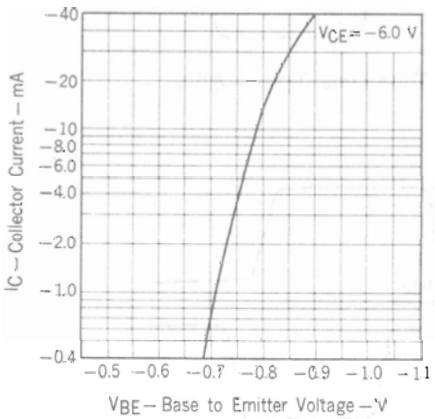
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



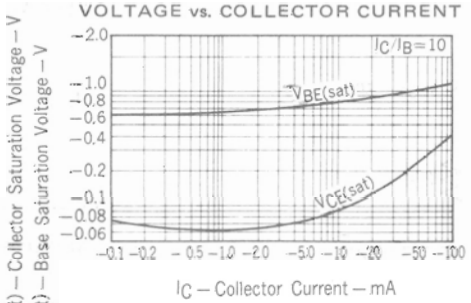
DC CURRENT GAIN vs. COLLECTOR CURRENT



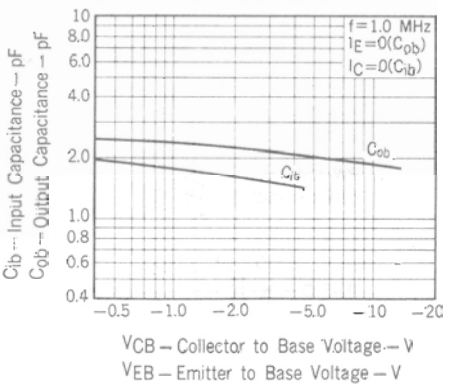
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



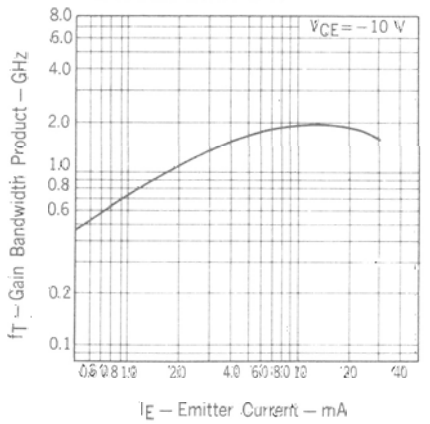
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



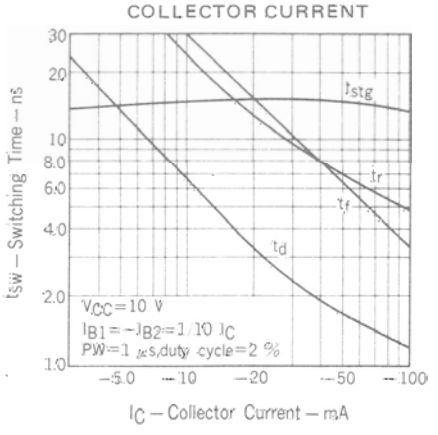
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



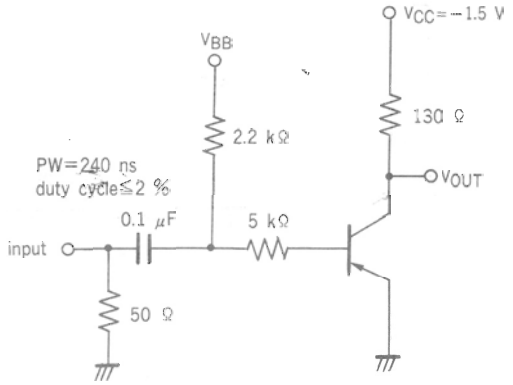
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



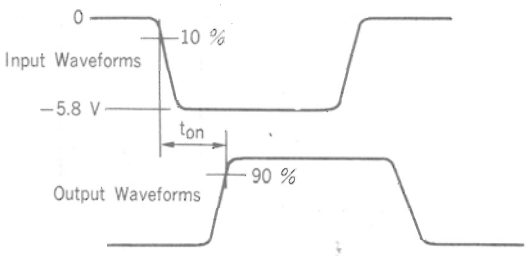
SWITCHING TIME vs. COLLECTOR CURRENT



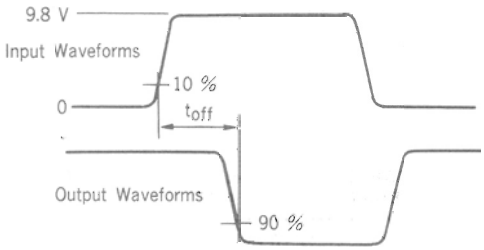
SWITCHING TIME TEST CIRCUIT



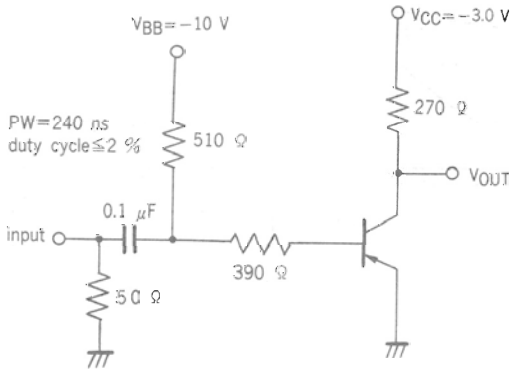
t_{on}, t_{off} Test Circuit



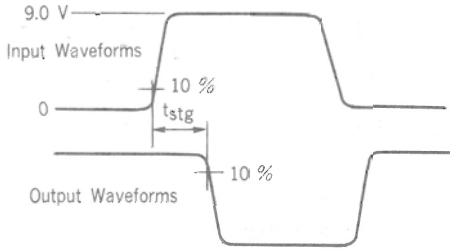
t_{on} Test Waveforms (V_{BB}=GROUND)



t_{off} Test Waveforms (V_{BB}=−8.0 V)



t_{stg} Test Circuit



t_{stg} Test Waveforms

NEC
ELECTRON DEVICE

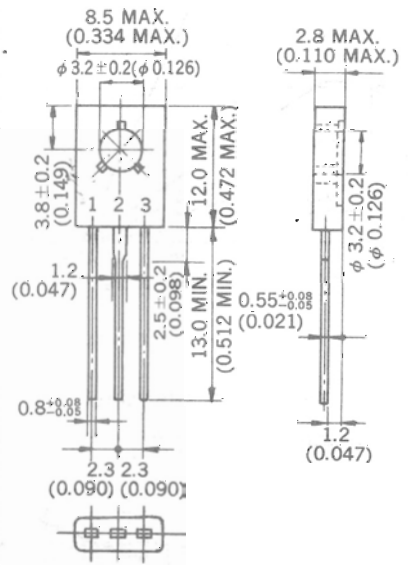
PNP SILICON POWER TRANSISTORS
2SA1220, 2SA1220A

DESCRIPTION The 2SA1220, 2SA1220A are general purpose transistors designed for use in audio and radio frequency power amplifiers.

FEATURES

- Suitable for use in driver stage of 50 to 100 W audio amplifiers and output stage of TV vertical deflection circuit.
- High Voltage and High f_T
  V_{CEO} = −120 V/−160 V (2SA1220, 2SA1220A)
  f_T = 105 MHz TYP. (@V_{CE} = −5.0 V, I_C = −0.2 A)
- Complementary to the NEC 2SC2690, 2SC2690A NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation
- Total Power Dissipation (T_a = 25 °C) . . . . . 1.2 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SA1220	2SA1220A	
V_{CBO}	Collector to Base Voltage	−120	−160	V
V_{CEO}	Collector to Emitter Voltage	−120	−160	V
V_{EBO}	Emitter to Base Voltage	−5.0		V
$I_{C(DC)}$	Collector Current	−1.2		A
$I_{C(pulse)}$ *	Collector Current	−2.5		A
$I_{B(DC)}$	Base Current	−0.3		A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	35	105		−	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2} **	DC Current Gain	60	140	320	−	V_{CE} = −5.0 V, I_C = −0.3 A
f_T	Gain Bandwidth Product		105		MHz	V_{CE} = −5.0 V, I_C = −0.2 A
C_{ob}	Output Capacitance		19		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB} = −120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB} = −3.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage		−0.4	−0.7	V	I_C = −1.0 A, I_B = −0.2 A
$V_{BE(sat)}$ **	Base Saturation Voltage		−1.0	−1.3	V	I_C = −1.0 A, I_B = −0.2 A

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

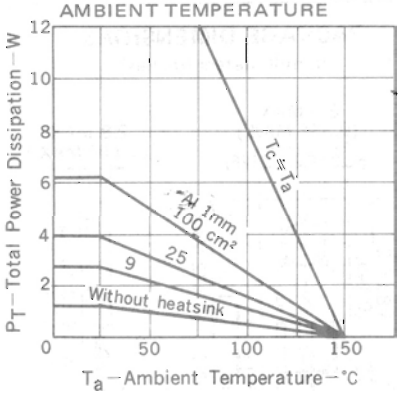
Classification of h_{FE2}

Rank	R	Q	P
Range	60 to 120	100 to 200	160 to 320

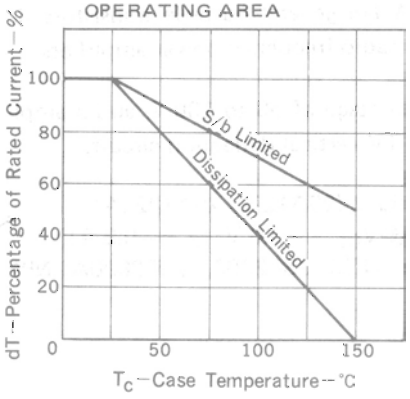
Test Conditions: V_{CE} = −5.0 V, I_C = −0.3 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

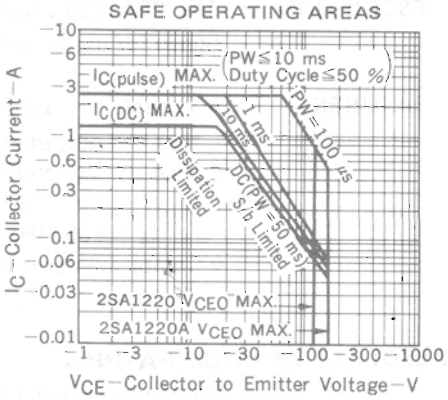
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



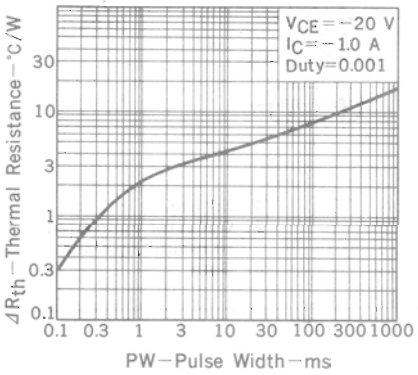
DERATING CURVE OF SAFE OPERATING AREA



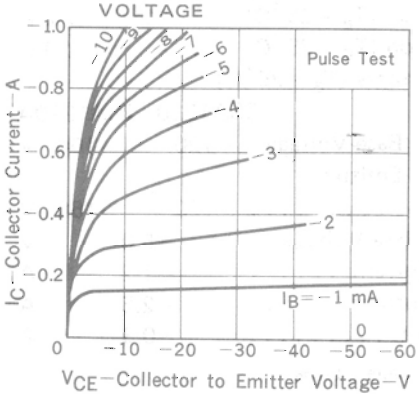
SAFE OPERATING AREAS



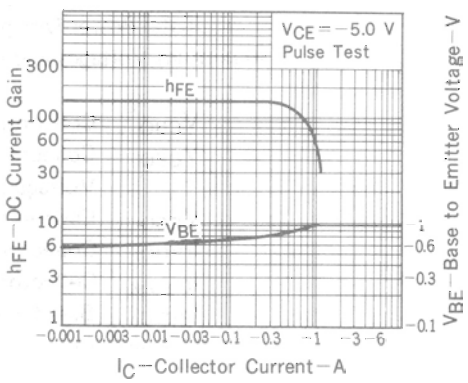
TRANSIENT THERMAL RESISTANCE



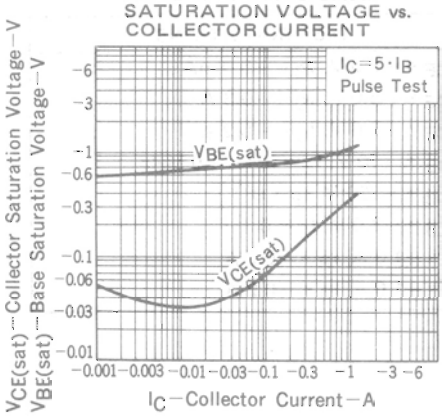
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



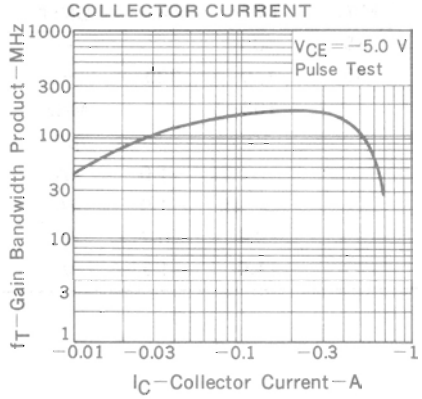
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



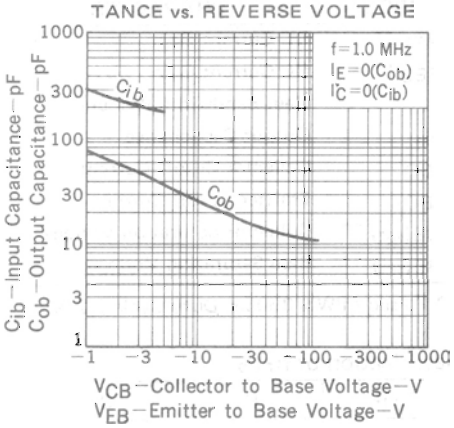
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT AND INPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

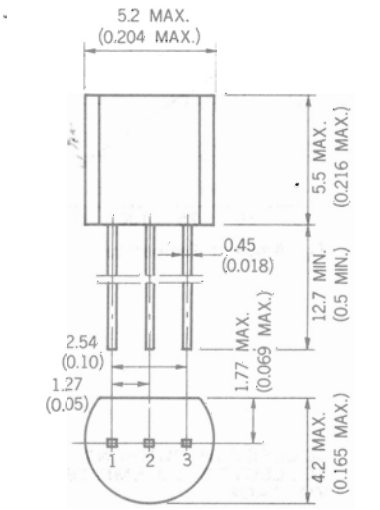
PNP SILICON TRANSISTORS
2SA1376,2SA1376A

DESCRIPTION The 2SA1376/2SA1376A is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Breakdown Voltage.
  V_{CEO} = −180 V/−200 V (2SA1376/2SA1376A)
- Good h_{FE} linearity.
- A Complementary pair with 2SC3478/2SC3478A.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Toltal Power Dissipation. . . . . 750 mW

Maximum Voltages and Currents (T_a = 25 °C)

		2SA1376/2SA1376A	
V_{CBO}	Collector to Base Voltage . .	−200	V
V_{CEO}	Collector to Emitter Voltage	−180/−200	V
V_{EBO}	Emitter to Base Voltage . . .	−5.0	V
I_C	Collector Current (DC). . . .	−100	mA
I_C	Collector Current (pulse)*. .	−200	mA
I_B	Base Current (DC)	−20	mA

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	2SA1376/2SA1376A MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	135		400/600	−	V_{CE} = −10 V, I_C = −10 mA
t_{on}	Turn-on Time		0.16		μs	I_C = −10 mA
t_{off}	Turn-off Time		1.5		μs	I_{B1} = −I_{B2} = −1 mA, V_{CC} = −10 V
f_T	Gain Bandwidth Product	80	120		MHz	V_{CE} = −10 V, I_E = 10 mA
C_{ob}	Output Capacitance		3.5	4.0	pF	V_{CB} = −30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −4.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−600	−650	−700	mV	V_{CE} = −10 V, I_C = −10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.2	−0.3	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.8	−1.2	V	I_C = −50 mA, I_B = −5.0 mA

Classification of h_{FE}

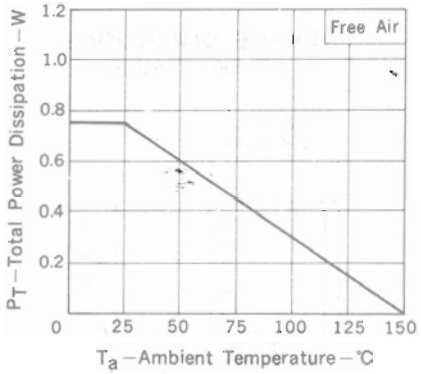
Rank	L	K	U**
Range	135 − 270	200 − 400	300 − 600

Test Conditions: V_{CE} = −10 V, I_C = −10 mA

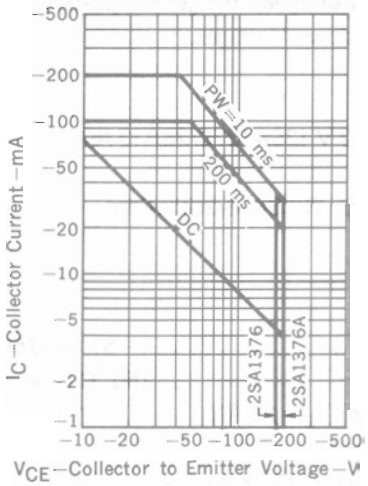
** 2SA1376A has no U rank.

TYPICAL CHARACTERISTICS (T_a = 25 °C)

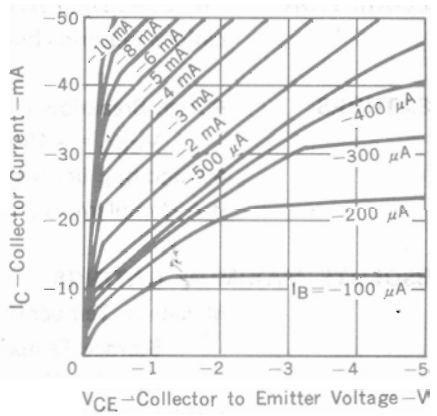
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



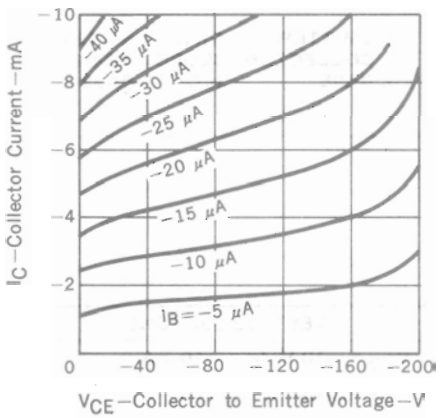
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



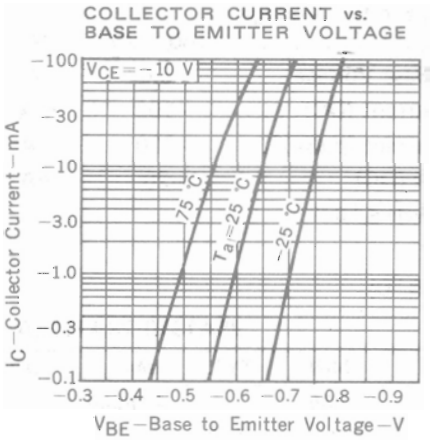
COLLECTOR CURRENT vs. COLLECTOR TO MITTER VOLTAGE



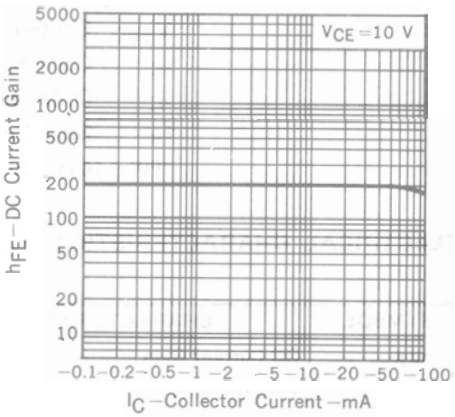
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



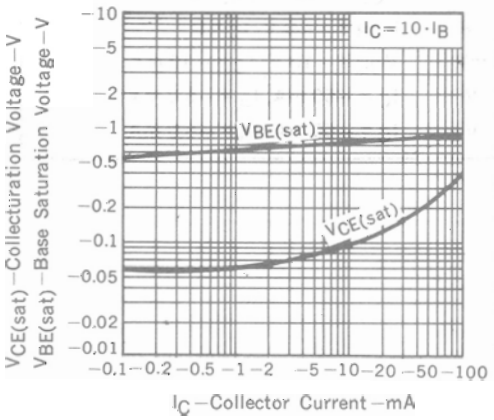
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



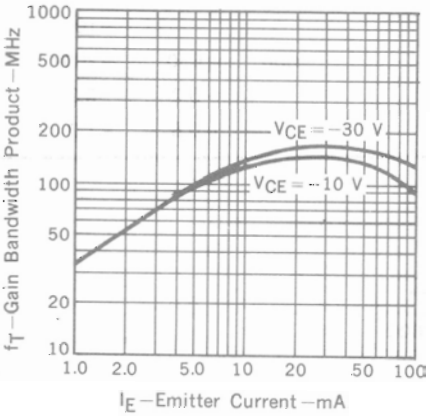
DC CURRENT GAIN vs. COLLECTOR CURRENT



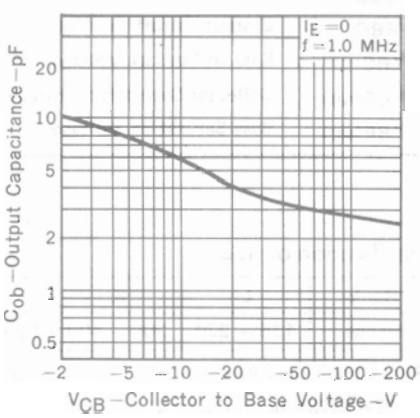
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



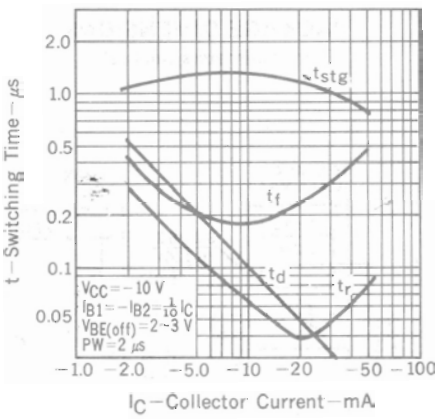
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

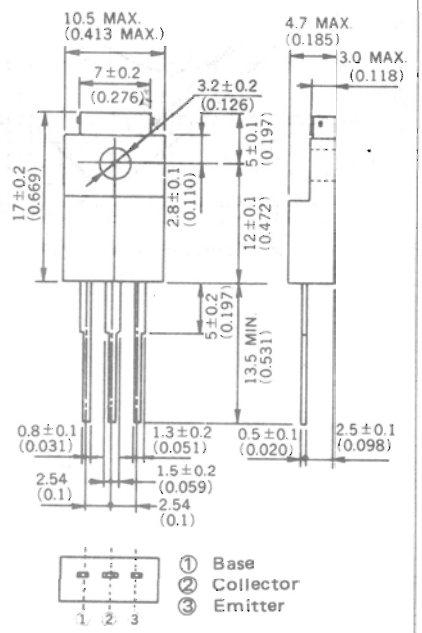
PNP SILICON POWER TRANSISTOR
2SA1394

DESCRIPTION The 2SA1394 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3566.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150	°C Maximum

Maximum Power Dissipation (T_a = 25 °C)

	Total Power Dissipation	25	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−80	V
V_{CEO}	Collector to Emitter Voltage	−60	V
V_{EBO}	Emitter to Base Voltage	−12	V
$I_{C(DC)}$	Collector Current (DC)	−5	A
$I_{C(pulse)}$	Collector Current (pulse)*	−10	A
$I_{B(DC)}$	Base Current (DC)	−2.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = −3.0 A, I_{B1} = −I_{B2} = −0.3 A, R_L = 17 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}	DC Current Gain*	40			—	V_{CE} = −5.0 V, I_C = −0.3 A
h_{FE2}	DC Current Gain*	40		200	—	V_{CE} = −5.0 V, I_C = −3.0 A
$V_{CE(sat)}$	Collector Saturation Voltage*			−0.6	V	I_C = −3.0 A, I_B = −0.3 A
$V_{BE(sat)}$	Base Saturation Voltage*			−1.5	V	I_C = −3.0 A, I_B = −0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −3.0 A, I_B = −0.3 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −3.0 A, I_{B1} = −I_{B2} = −0.3 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −6.0 A, I_{B1} = −0.6 A, −I_{B2} = 0.3 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −10 V, I_C = 0

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

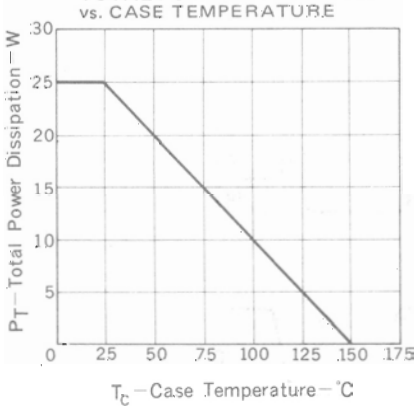
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

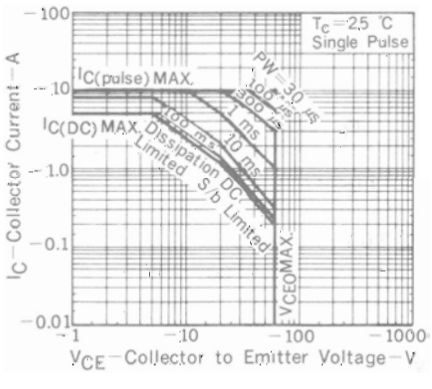
Test Conditions: V_{CE} = −5.0 V, I_C = −3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

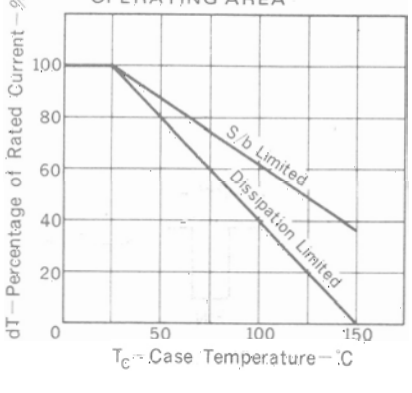
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



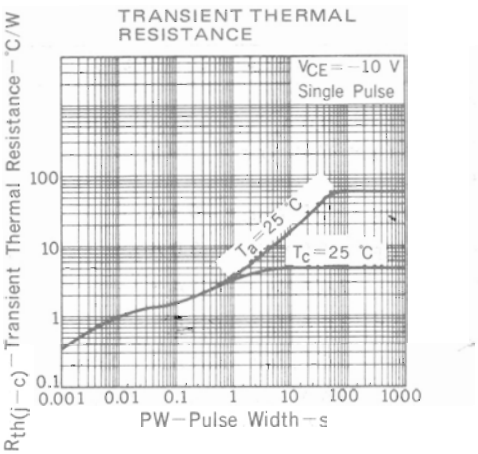
FORWARD BIAS SAFE OPERATING AREA



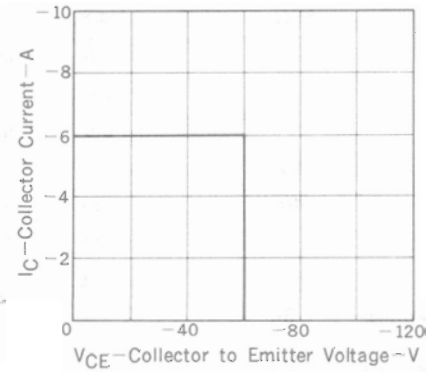
DERATING CURVE OF SAFE OPERATING AREA



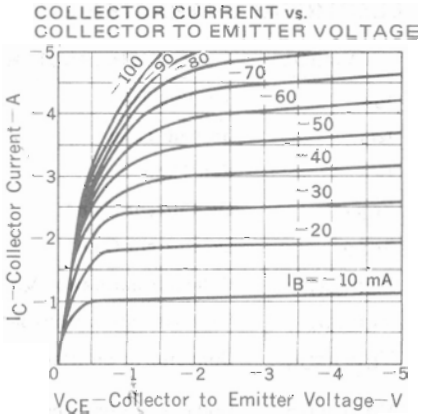
TRANSIENT THERMAL RESISTANCE



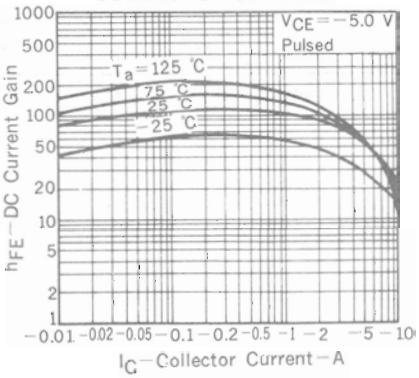
REVERSE BIAS SAFE OPERATING AREA



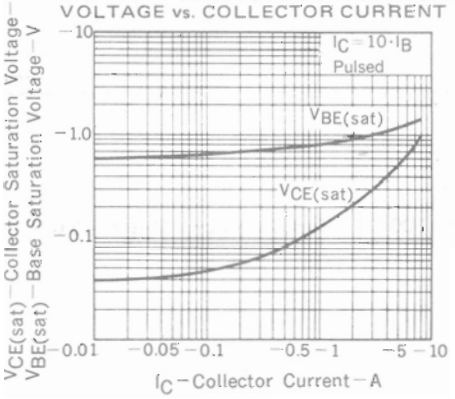
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



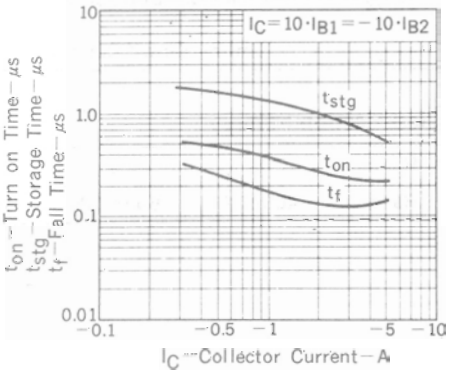
DC CURRENT GAIN vs. COLLECTOR CURRENT



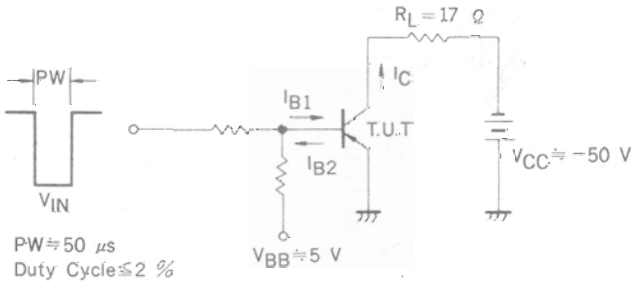
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

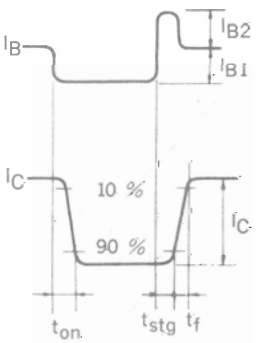


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





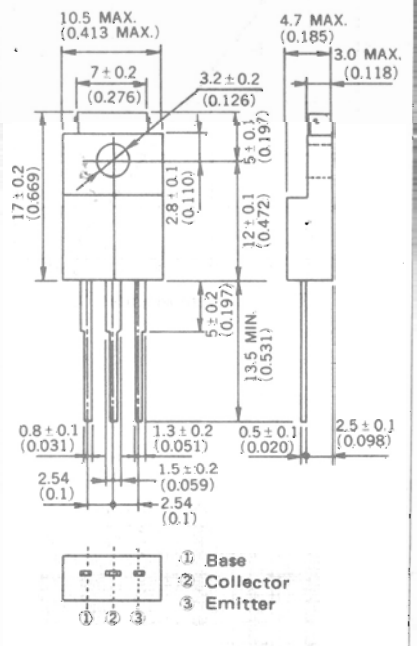
NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SA1395

DESCRIPTION The 2SA1395 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES
- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3567.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100	V
V_{CEO}	Collector to Emitter Voltage	−100	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−2.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	−4.0	A
$I_{B(DC)}$	Base Current (DC)	−1.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT.	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = −1.0 A, I_{B1} = −I_{B2} = −0.1 A, R_L = 50 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}	DC Current Gain**	40			—	V_{CE} = −5.0 V, I_C = −0.1 A
h_{FE2}	DC Current Gain**	40		200	—	V_{CE} = −5.0 V, I_C = −1.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			−0.6	V	I_C = −1.0 A, I_B = −0.1 A
$V_{BE(sat)}$	Base Saturation Voltage**			−1.5	V	I_C = −1.0 A, I_B = −0.1 A
$V_{CEO\ (SUS)}$	Collector to Emitter Sustaining Voltage	−100			V	I_C = −1.0 A, I_B = −0.1 A, L = 1 mH
$V_{CEX\ (SUS)1}$	Collector to Emitter Sustaining Voltage	−100			V	I_C = −1.0 A, I_{B1} = −I_{B2} = −0.1 A, L = 180 μH, Clamped
$V_{CEX\ (SUS)2}$	Collector to Emitter Sustaining Voltage	−100			V	I_C = −2.0 A, I_{B1} = −0.2 A, −I_{B2} = 0.1 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −100 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −100 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −100 V, $V_{BE(OFF)}$ = 5.0 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −100 V, $V_{BE(OFF)}$ = 5.0 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

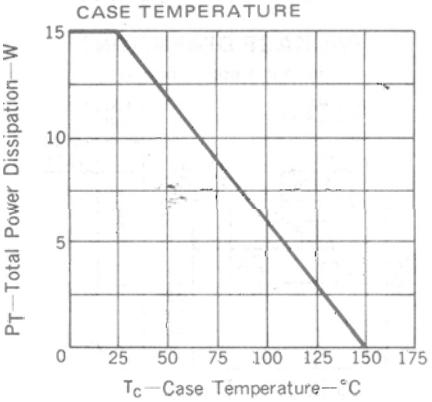
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

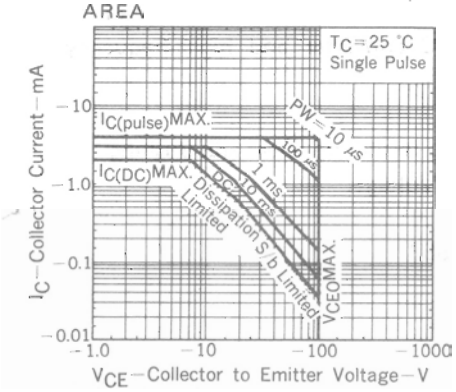
Test Conditions: V_{CE} = −5.0 V, I_C = −1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

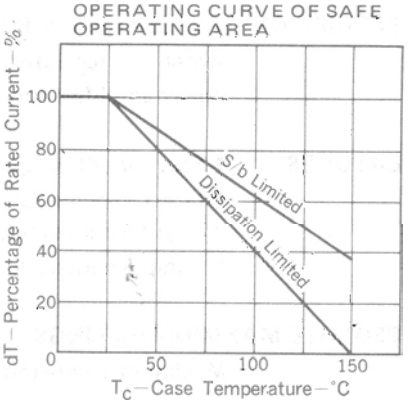
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



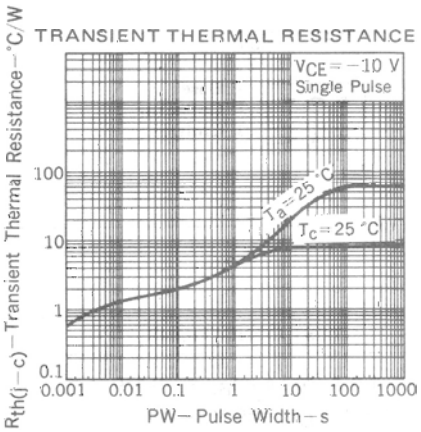
FORWARD BIAS SAFE OPERATING AREA



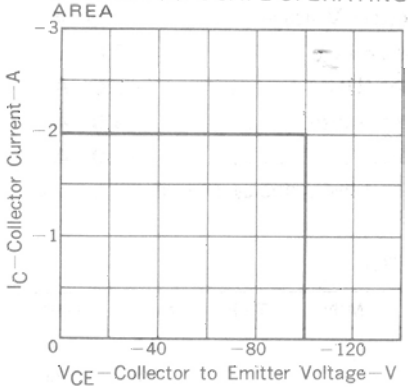
OPERATING CURVE OF SAFE OPERATING AREA



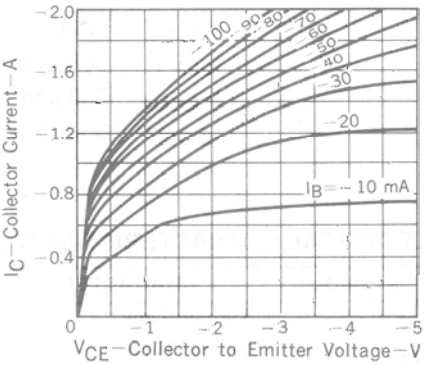
TRANSIENT THERMAL RESISTANCE



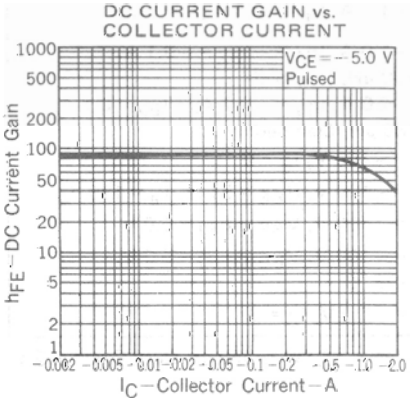
REVERSE BIAS SAFE OPERATING AREA



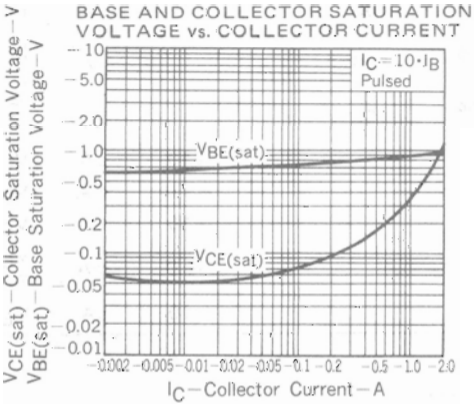
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



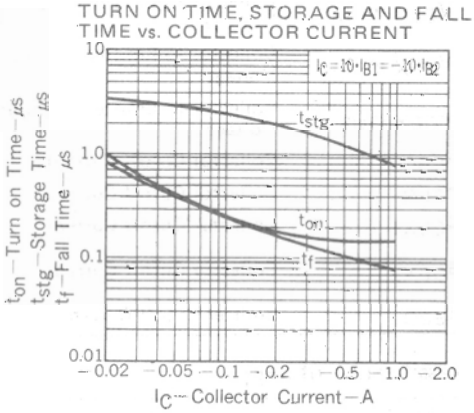
DC CURRENT GAIN vs. COLLECTOR CURRENT



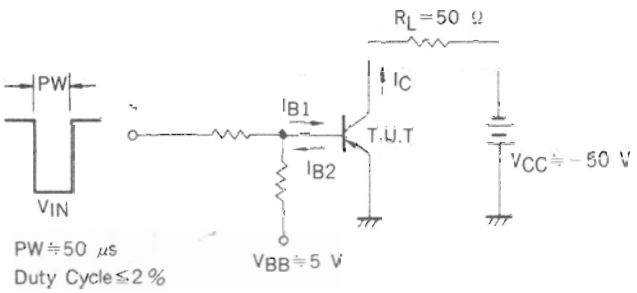
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

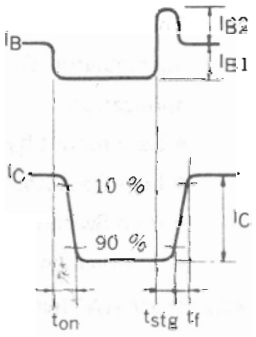


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

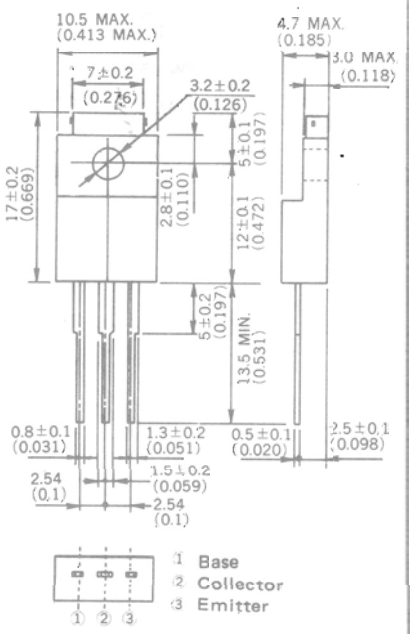
PNP SILICON POWER TRANSISTOR
2SA1396

DESCRIPTION The 2SA1396 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3568.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100 V
V_{CEO}	Collector to Emitter Voltage	−100 V
V_{EBO}	Emitter to Base Voltage	−7.0 V
$I_{C(DC)}$	Collector Current (DC)	−10 A
$I_{C(pulse)}$	Collector Current (pulse)*	−20 A
$I_{B(DC)}$	Base Current (DC)	−5.0 A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = −5.0 A, I_{B1} = −I_{B2} = −0.5 A R_L = 10 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}	DC Current Gain**	40		200	—	V_{CE} = −5.0 V, I_C = −0.5 A
h_{FE2}	DC Current Gain**	40		200	—	V_{CE} = −5.0 V, I_C = −3.0 A
h_{FE3}	DC Current Gain**	20			—	V_{CE} = −5.0 V, I_C = −5.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			−0.6	V	I_C = −5.0 A, I_B = −0.5 A
$V_{BE(sat)}$	Base Saturation Voltage**			−1.5	V	I_C = −5.0 A, I_B = −0.5 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−100			V	I_C = −5.0 A, I_B = −0.5 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	−100			V	I_C = −5.0 A, I_{B1} = −I_{B2} = −0.5 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	−100			V	I_C = −10 A, I_{B1} = −1.0 A, −I_{B2} = 0.5 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −100 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −100 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −100 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −100 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0

**PW ≦ 350 μs, Duty Cycle ≦ 2 %

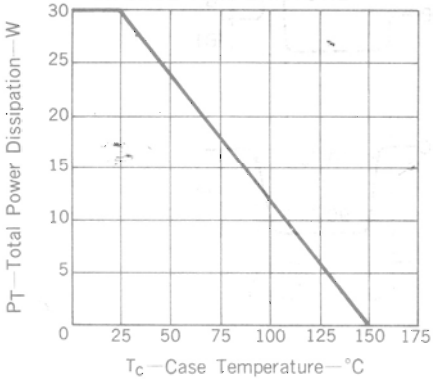
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

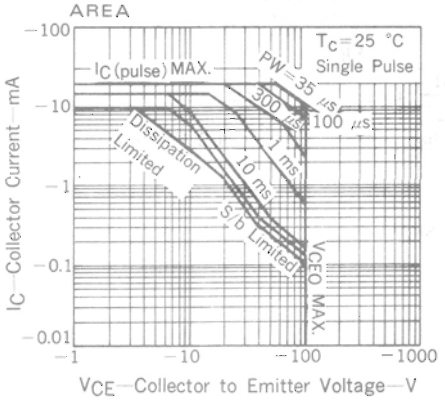
Test Conditions: V_{CE} = −5.0 V, I_C = −3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

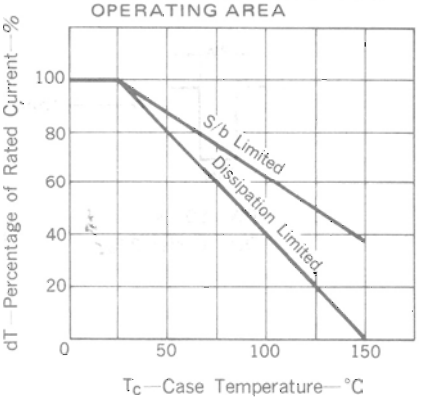
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



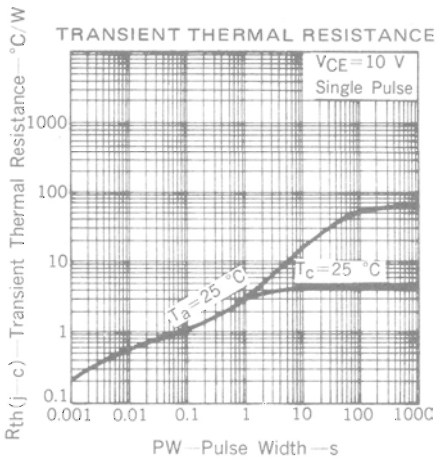
FORWARD BIAS SAFE OPERATING AREA



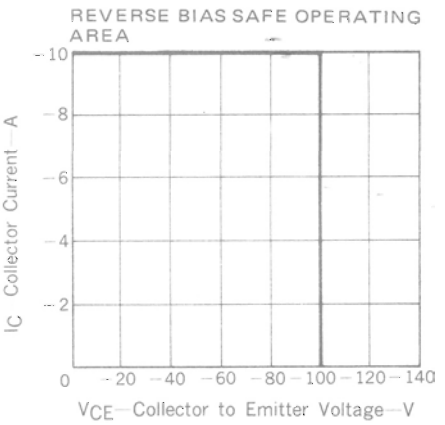
DERATING CURVE OF SAFE OPERATING AREA



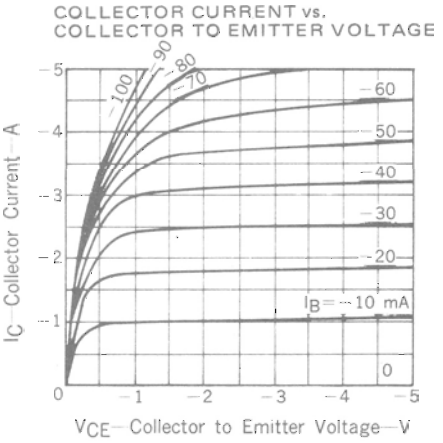
TRANSIENT THERMAL RESISTANCE



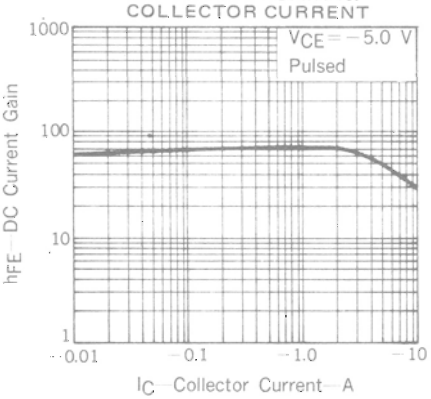
REVERSE BIAS SAFE OPERATING AREA



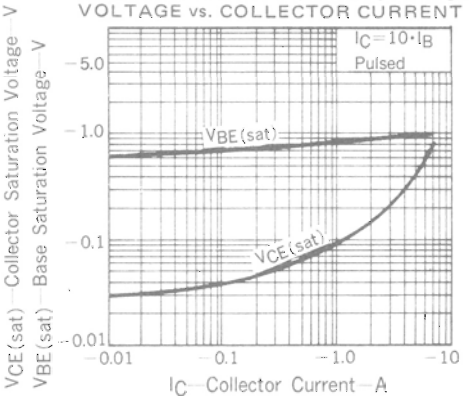
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



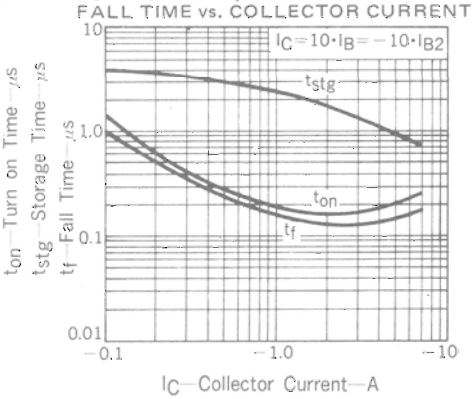
DC CURRENT GAIN vs. COLLECTOR CURRENT



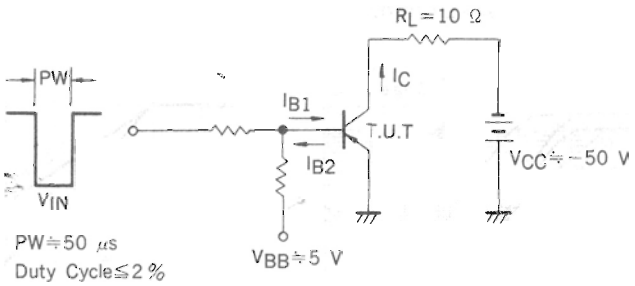
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

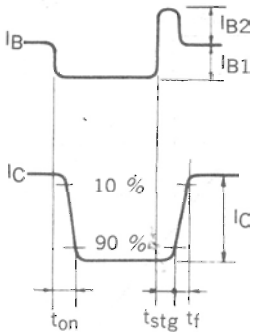


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

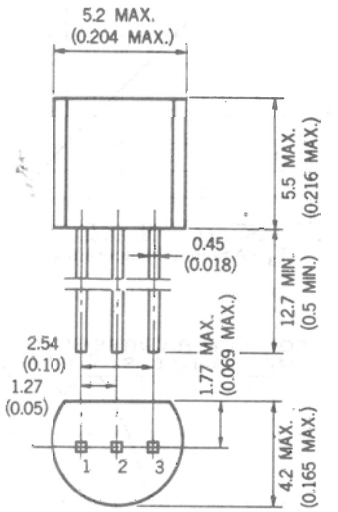
PNP SILICON TRANSISTOR
2SA1409

DESCRIPTION The 2SA1409 is designed for general-purpose applications requiring High DC Current Gain.

FEATURES

- High DC Current Gain.
  h_{FE} = 500 to 1600 (@ V_{CE} = −5.0 V, I_C = −1.0 mA)
- High V_{EBO} : V_{EBO} > −10 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER EIAJ : SC-43B
2. COLLECTOR JEDEC : TO-92
3. BASE IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −25 V
- V_{CEO} Collector to Emitter Voltage . . . . . −25 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- I_C Collector Current . . . . . −150 mA
- I_B Base Current. . . . . −10 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	500	1000	1600	—	V_{CE} = −5.0 V, I_C = −1.0 mA
h_{FE2}*	DC Current Gain	200	400		—	V_{CE} = −5.0 V, I_C = −100 mA
f_T	Gain Bandwidth Product		200		MHz	V_{CE} = −5.0 V, I_E = 10 mA
C_{ob}	Output Capacitance		4.6		pF	V_{CB} = −5.0 V, I_E = 0, f = 1.0 MHz
t_{on}	Turn-on Time		0.12		μs	V_{CC} = −10 V, $V_{BE(off)}$ = 2.7 V
t_f	Storage Time		0.58		μs	I_C = −50 mA
t_{off}	Turn-off Time		0.75		μs	I_{B1} = −I_{B2} = −1.0 mA
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −25 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −7.0 V, I_C = 0
V_{BE}*	Base to Emitter Voltage		−580		mV	V_{CE} = −5.0 V, I_C = −1.0 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.15	−0.30	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.8	−1.2	V	I_C = −50 mA, I_B = −5.0 mA

*Marked items are Pulse Test : PW 350 μs, Duty Cycle ≤ 2 %

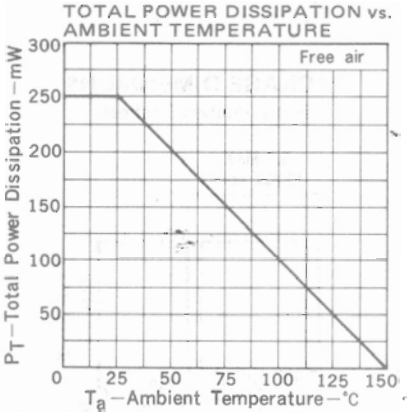
Classification of h_{FE1}

Rank	L	K
Range	500 to 1000	800 to 1600

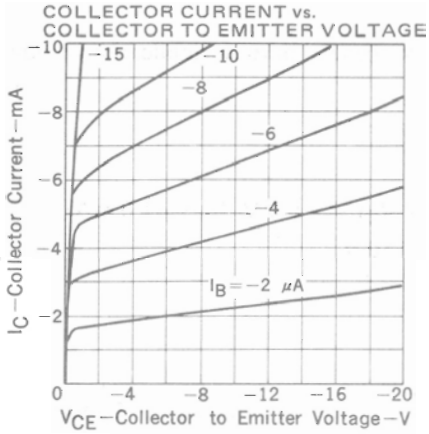
Test Conditions: V_{CE} = −5.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

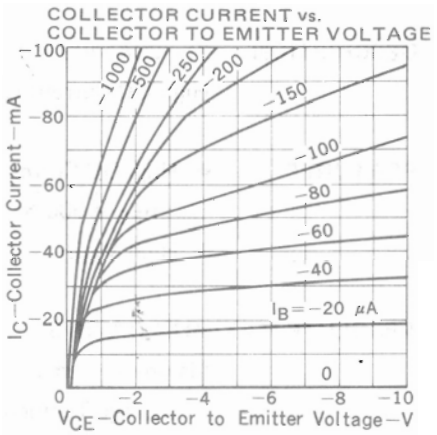
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



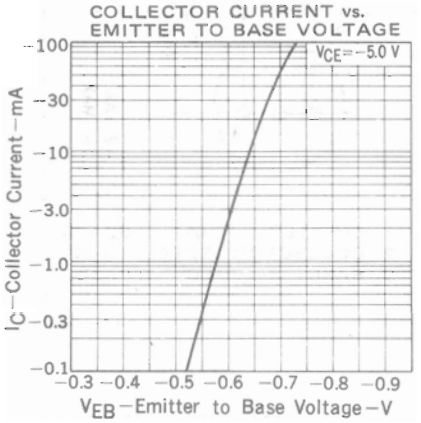
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



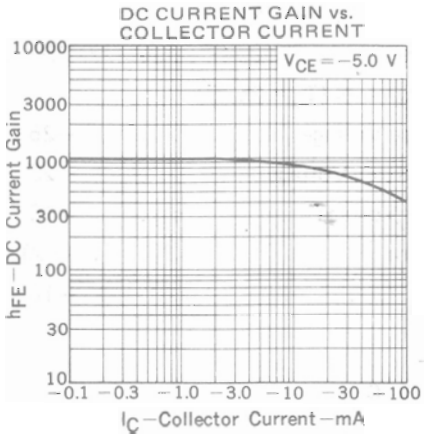
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



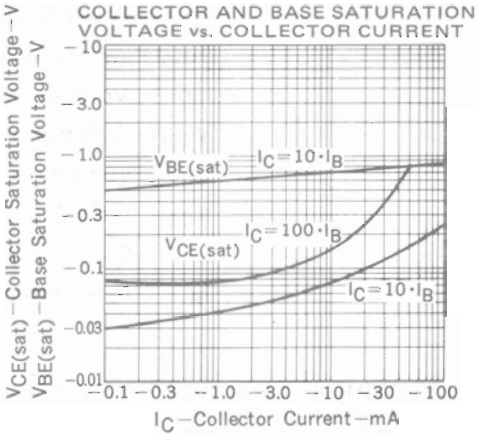
COLLECTOR CURRENT vs. EMITTER TO BASE VOLTAGE



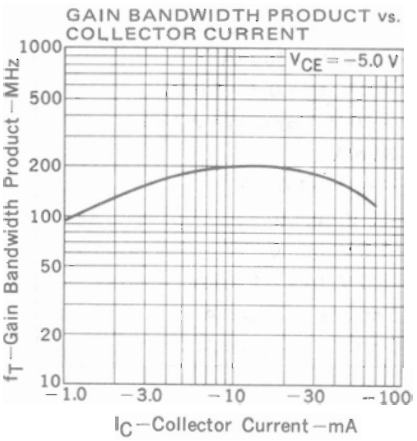
DC CURRENT GAIN vs. COLLECTOR CURRENT



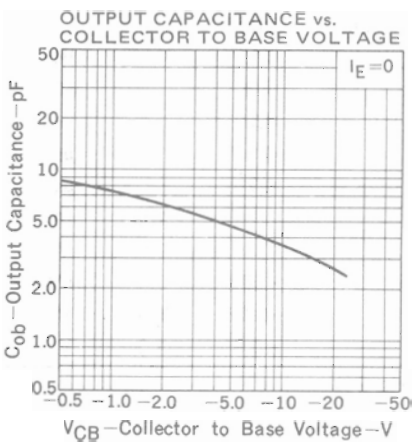
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



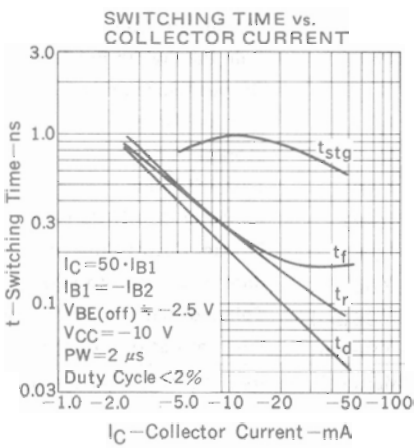
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

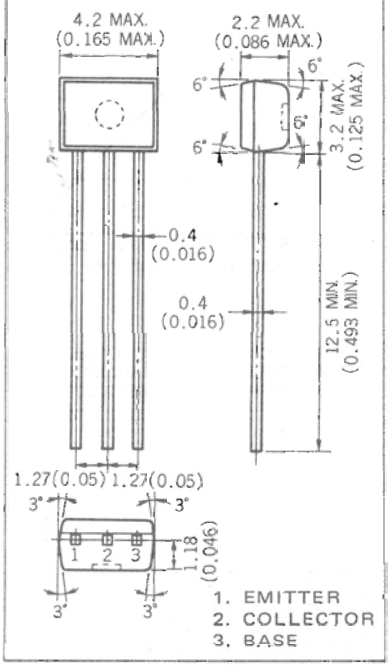
PNP SILICON TRANSISTOR
2SA1410

DESCRIPTION The 2SA1410 is designed for general-purpose applications requiring High DC Current Gain.

FEATURES

- High DC Current Gain.
  h_{FE} = 500 to 1600 (@ V_{CE} = −5.0 V, I_C = −1.0 mA)
- High V_{EBO} : V_{EBO} > −10 V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −25 V
- V_{CEO} Collector to Emitter Voltage . . . . . −25 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- I_C Collector Current . . . . . −150 mA
- I_B Base Current. . . . . −10 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	500	1000	1600	–	V_{CE} = −5.0 V, I_C = −1.0 mA
h_{FE2}*	DC Current Gain	200	400		–	V_{CE} = −5.0 V, I_C = −100 mA
f_T	Gain Bandwidth Product		200		MHz	V_{CE} = −5.0 V, I_C = 10 mA
C_{ob}	Output Capacitance		4.6		pF	V_{CB} = −5.0 V, I_E = 0, f = 1.0 MHz
t_{on}	Turn-on Time		0.12		μs	V_{CC} = −10 V, $V_{BE(off)}$ = 2.7 V
t_f	Storage Time		0.58		μs	I_C = −50 mA
t_{off}	Turn-off Time		0.75		μs	I_{B1} = −I_{B2} = −1.0 mA
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −25 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −7.0 V, I_C = 0
V_{BE}*	Base to Emitter Voltage		−580		mV	V_{CE} = −5.0 V, I_C = −1.0 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.15	−0.30	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.8	−1.2	V	I_C = −50 mA, I_B = −5.0 mA

*Marked items are Pulse Test : PW 350 μs
Duty Cycle ≦ 2 %

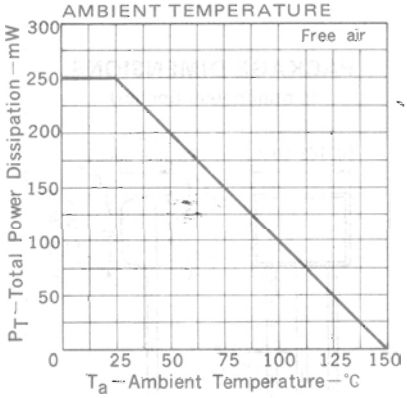
Classification of h_{FE1}

Rank	L	K
Range	500 to 1000	800 to 1600

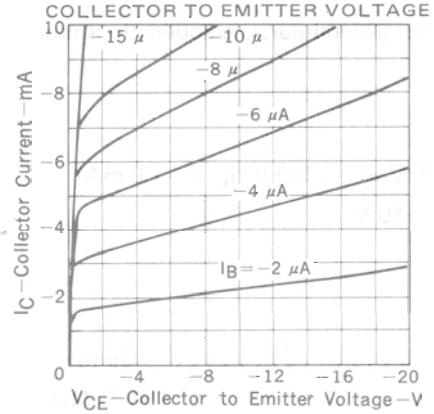
Test Conditions: V_{CE} = −5.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

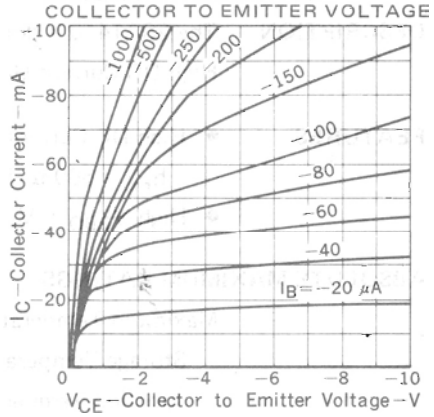
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



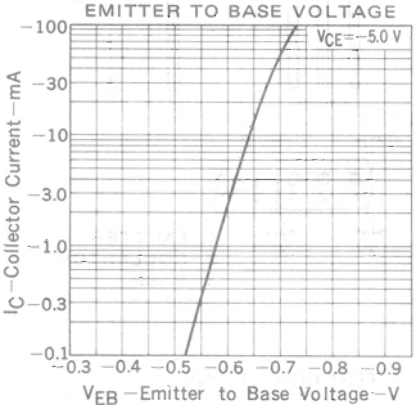
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



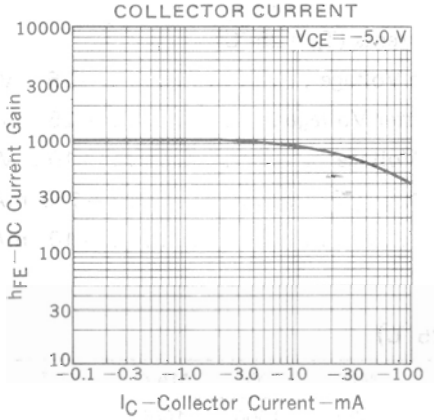
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



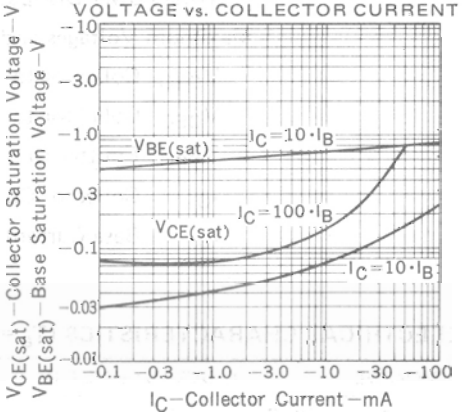
COLLECTOR CURRENT vs. EMITTER TO BASE VOLTAGE



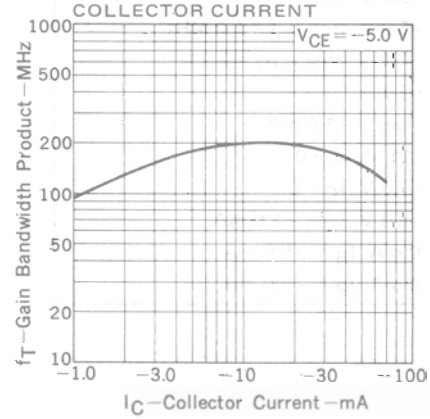
DC CURRENT GAIN vs. COLLECTOR CURRENT



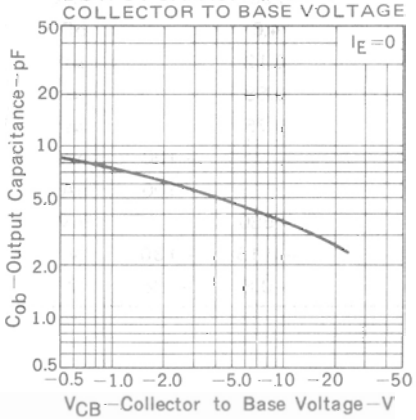
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



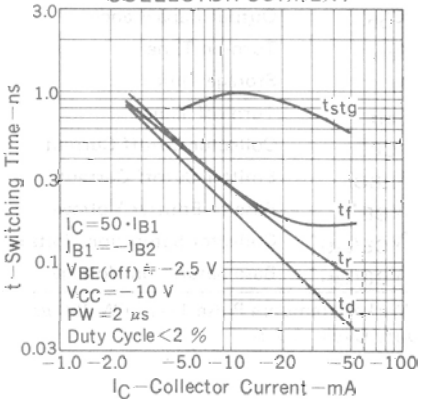
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

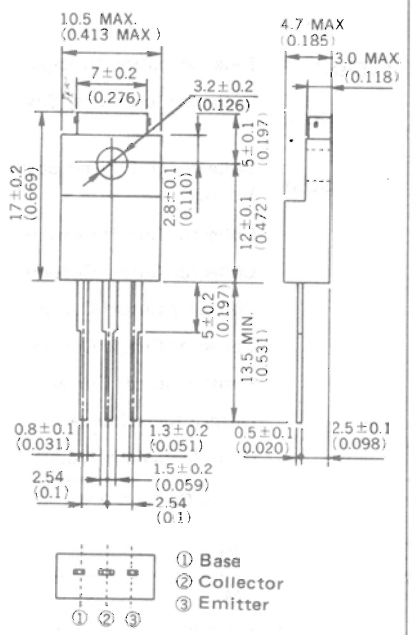
PNP SILICON POWER TRANSISTOR
2SA1441

DESCRIPTION The 2SA1441 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3691.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100 V
V_{CEO}	Collector to Emitter Voltage	−60 V
V_{EBO}	Emitter to Base Voltage	−7.0 V
$I_{C(DC)}$	Collector Current (DC)	−5.0 A
$I_{C(pulse)}$	Collector Current (pulse)*	−10 A
$I_{B(DC)}$	Base Current (DC)	−2.5 A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = −3.0 A, I_{B1} = −I_{B2} = −0.15 A, R_L = 17 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = −2.0 V, I_C = −0.5 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = −2.0 V, I_C = −1.0 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = −2.0 V, I_C = −3.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			−0.3	V	I_C = −3.0 A, I_B = −0.15 A
$V_{BE(sat)}$*	Base Saturation Voltage			−1.2	V	I_C = −3.0 A, I_B = −0.15 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −3.0 A, I_B = −0.3 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −3.0 A, I_{B1} = −I_{B2} = −0.3 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0
C_{ob}	Output Capacitance		130		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		80		MHz	V_{CE} = −10 V, I_C = −0.5 A

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

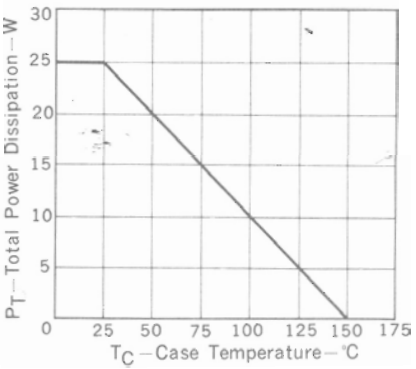
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

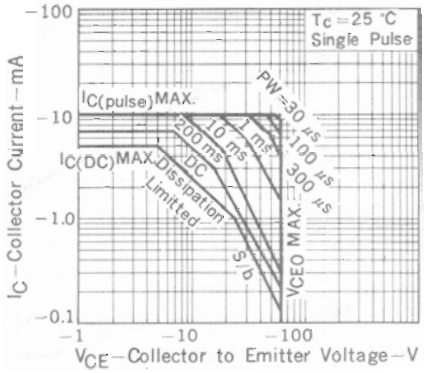
Test Conditions: V_{CE} = −2.0 V, I_C = −1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

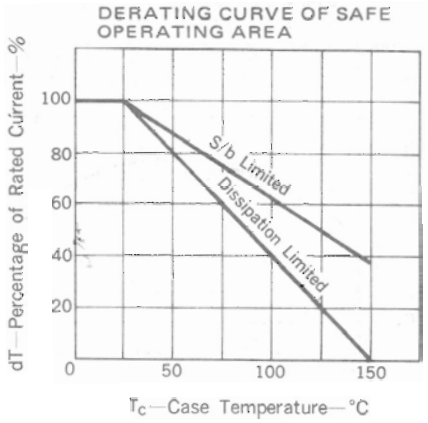
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



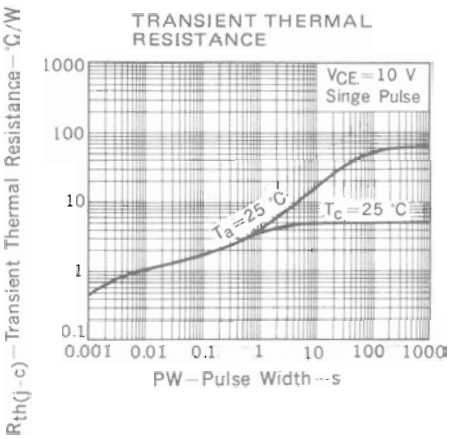
FORWARD BIAS SAFE OPERATING AREA



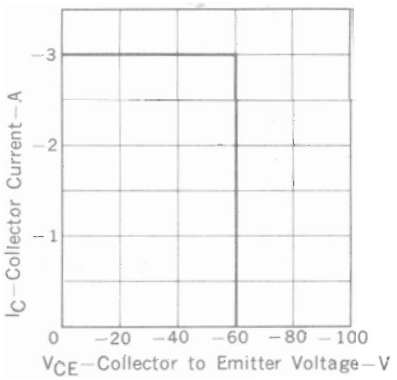
DERATING CURVE OF SAFE OPERATING AREA



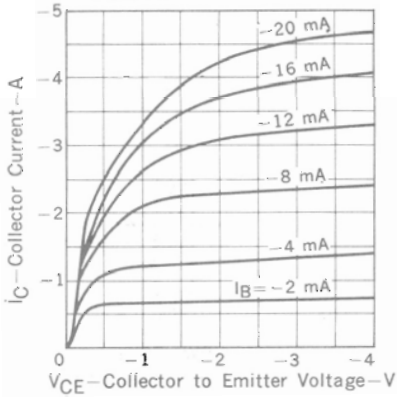
TRANSIENT THERMAL RESISTANCE



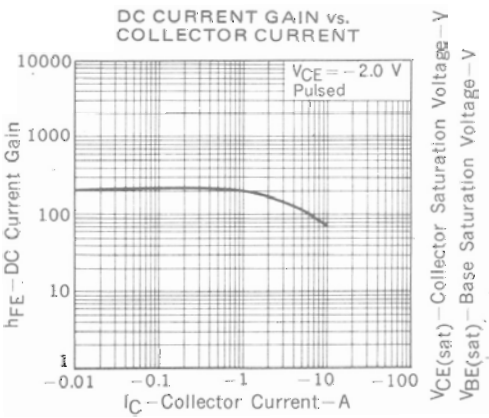
REVERSE BIAS OPERATING AREA



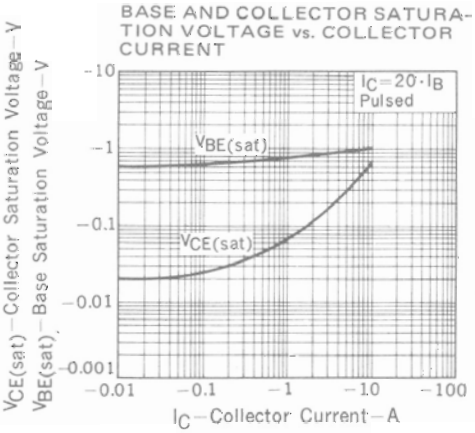
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



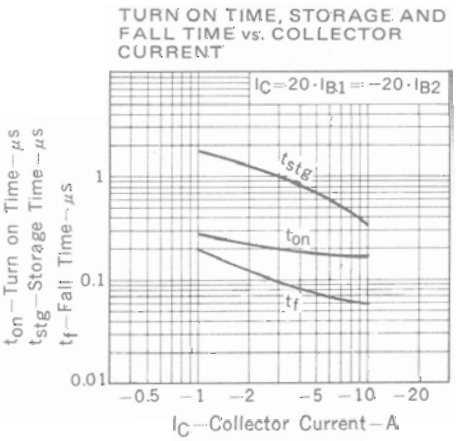
DC CURRENT GAIN vs. COLLECTOR CURRENT



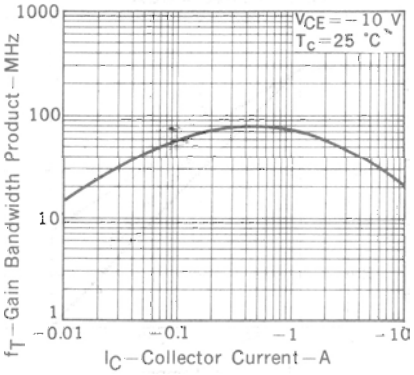
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



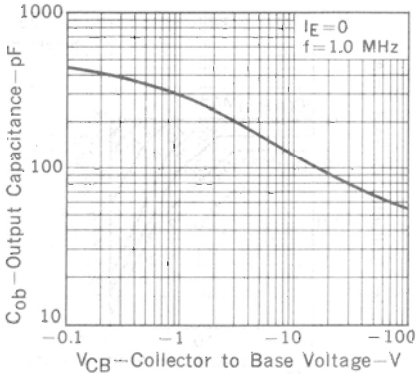
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



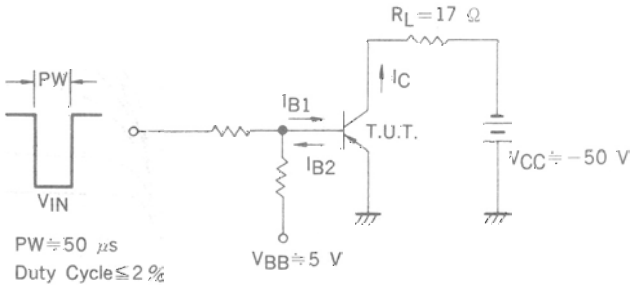
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

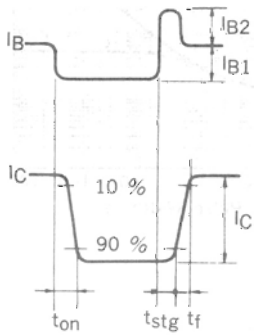


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

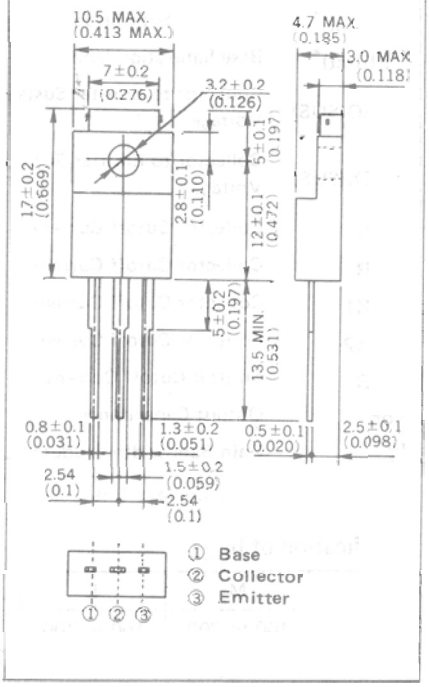
PNP SILICON POWER TRANSISTOR
2SA1442

DESCRIPTION The 2SA1442 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3692.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100	V
V_{CEO}	Collector to Emitter Voltage	−60	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−7.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	−14	A
$I_{B(DC)}$	Base Current (DC)	−3.5	A

* PW ≤ 300 μs, Duty Cycle ≤10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = −4.0 A, I_{B1} = −I_{B2} = −0.2 A R_L = 12.5 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = −2.0 V, I_C = −0.7 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = −2.0 V, I_C = −1.5 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = −2.0 V, I_C = −4.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			−0.3	V	I_C = −4.0 A, I_B = −0.2 A
$V_{BE(sat)}$*	Base Saturation Voltage			−1.2	V	I_C = −4.0 A, I_B = −0.2 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −4.0 A, I_B = −0.4 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −4.0 A, I_{B1} = −I_{B2} = −0.4 A, T_a = 125 °C L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0
C_{ob}	Output Capacitance		180		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		40		MHz	V_{CE} = −10 V, I_C = −1.0 A

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

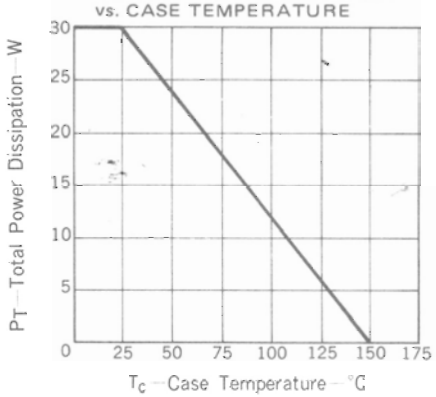
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

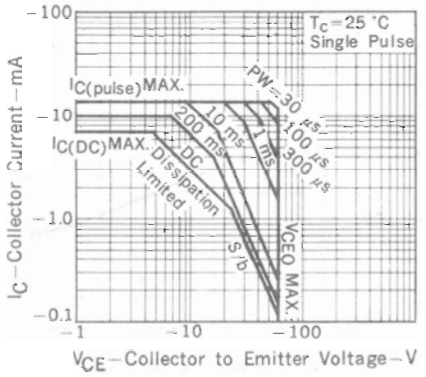
Test Conditions: V_{CE} = −2.0 V, I_C = −1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

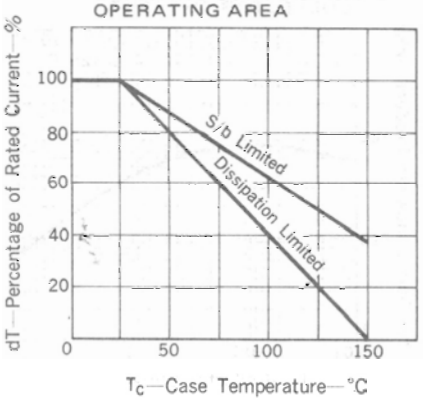
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



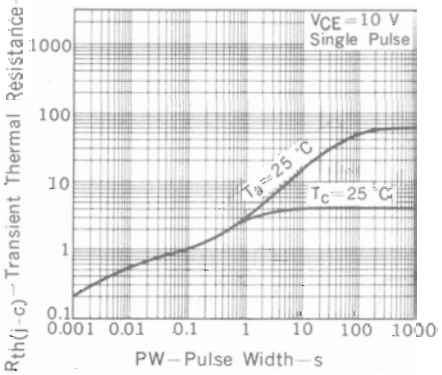
FORWARD BIAS SAFE OPERATING AREA



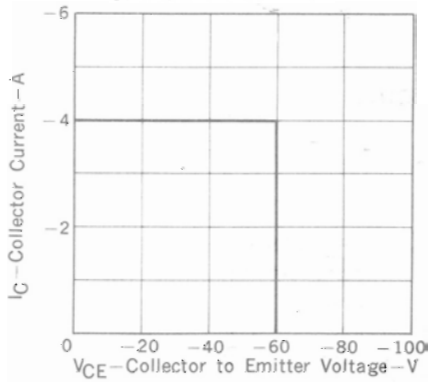
DERATING CURVE OF SAFE OPERATING AREA



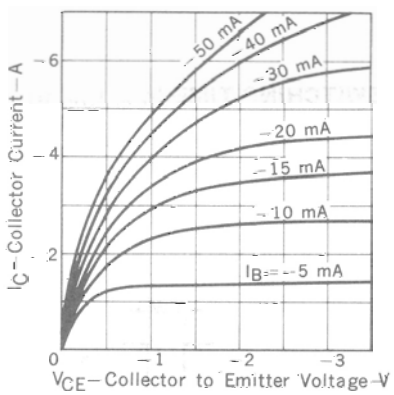
TRANSIENT THERMAL RESISTANCE



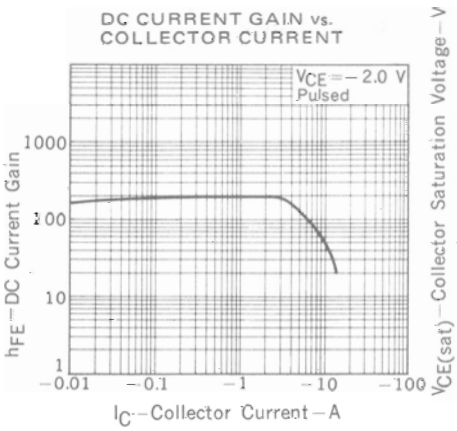
REVERSE BIAS SAFE OPERATING AREA



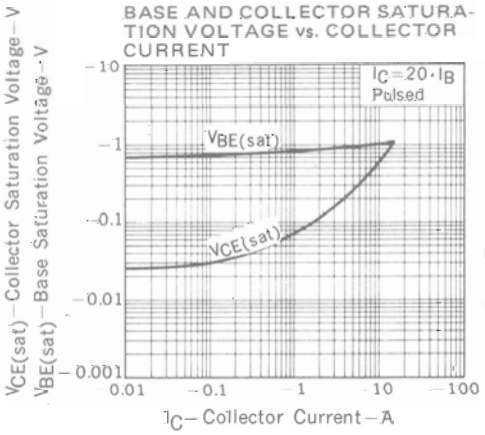
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



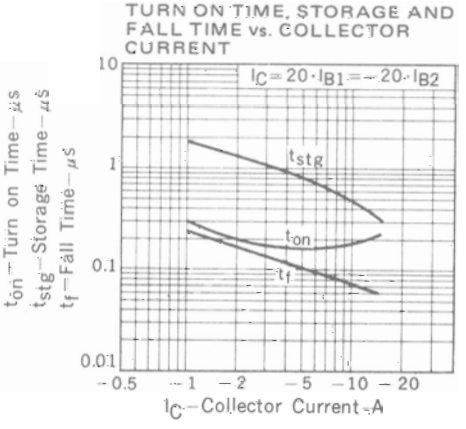
DC CURRENT GAIN vs. COLLECTOR CURRENT



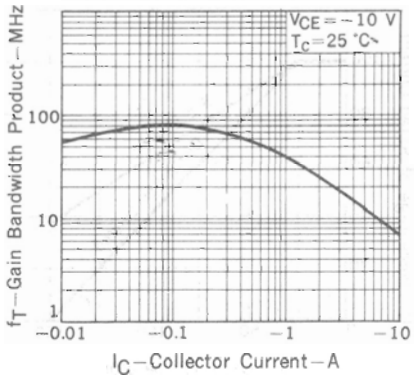
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



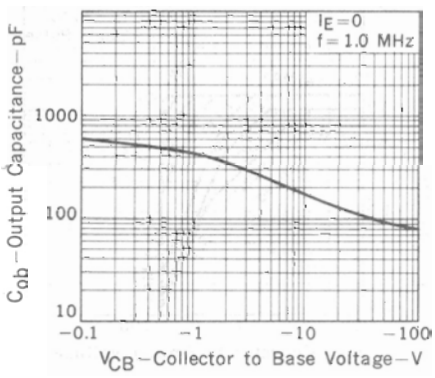
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



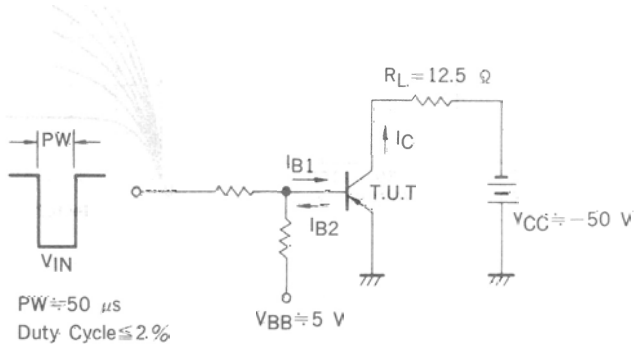
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

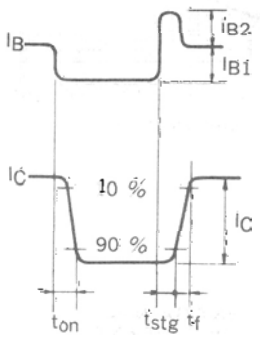


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

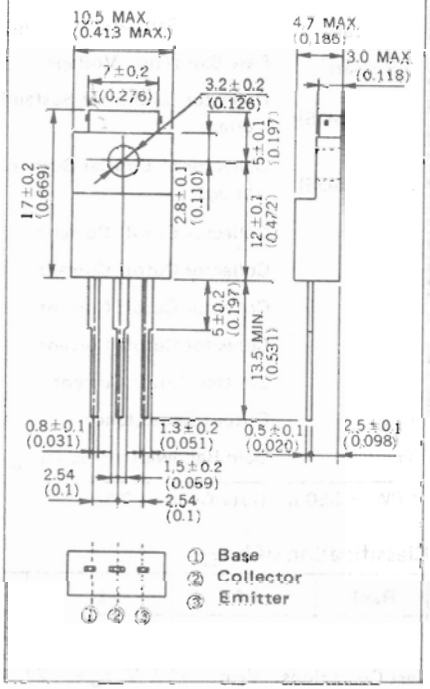
PNP SILICON POWER TRANSISTOR
2SA1443

DESCRIPTION The 2SA1443 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3693.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100	V
V_{CEO}	Collector to Emitter Voltage	−60	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−10	A
$I_{C(pulse)}$	Collector Current (pulse)*	−20	A
$I_{B(DC)}$	Base Current (DC)	−5.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = −6.0 A, I_{B1} = −I_{B2} ≒ −0.3 A R_L ≒ 8.3 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = −2.0 V, I_C = −1.0 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = −2.0 V, I_C = −2.0 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = −2.0 V, I_C = −6.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			−0.3	V	I_C = −6.0 A, I_B = −0.3 A
$V_{BE(sat)}$*	Base Saturation Voltage			−1.2	V	I_C = −6.0 A, I_B = −0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −6.0 A, I_B = −0.6 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −6.0 A, I_{B1} = −I_{B2} = −0.6 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0
C_{ob}	Output Capacitance		230		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		80		MHz	V_{CE} = −10 V, I_C = −1.0 A

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

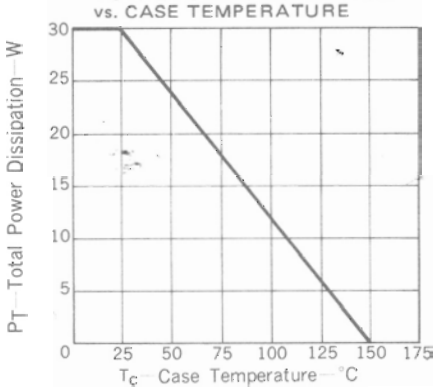
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

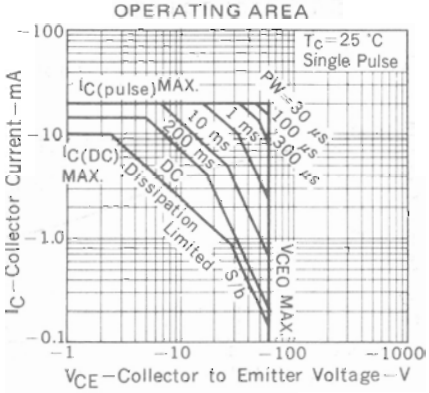
Test Conditions: V_{CE} = −2.0 V, I_C = −2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

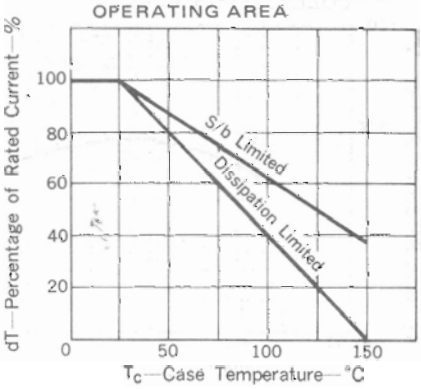
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



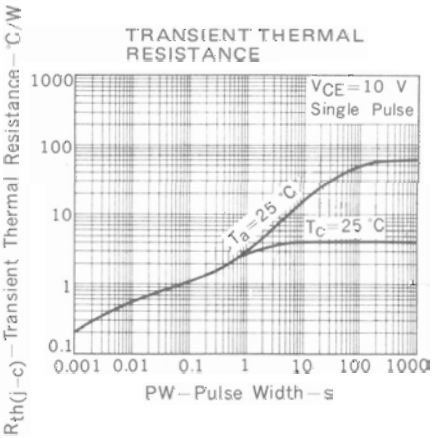
FORWARD BIAS SAFE OPERATING AREA



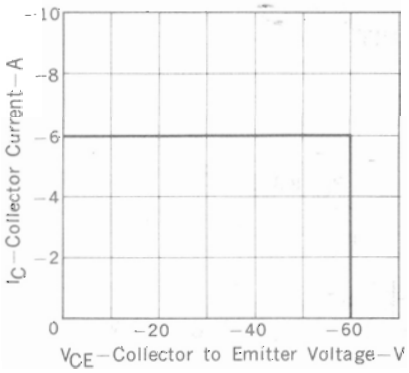
DERATING CURVE OF SAFE OPERATING AREA



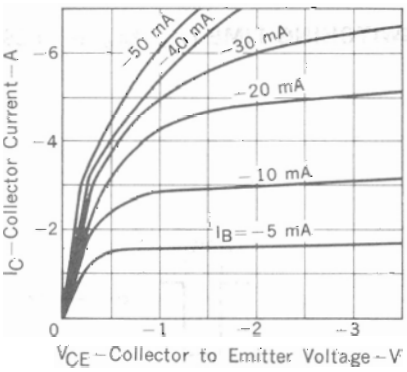
TRANSIENT THERMAL RESISTANCE



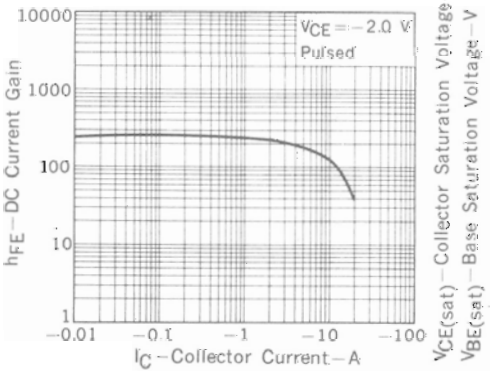
REVERSE BIAS SAFE OPERATING AREA



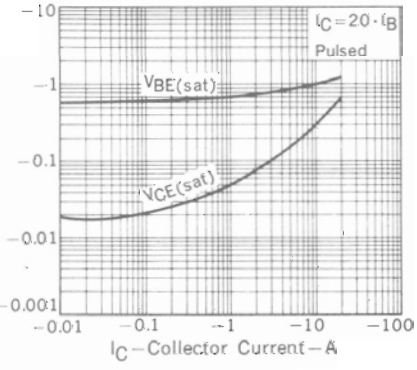
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



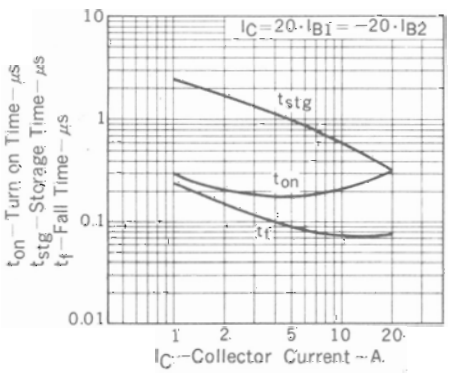
DC CURRENT GAIN vs. COLLECTOR CURRENT



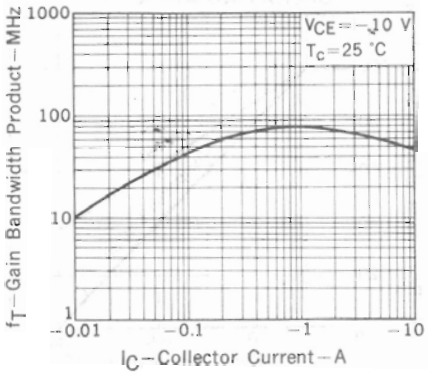
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



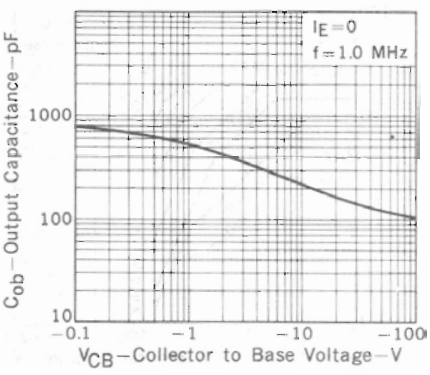
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



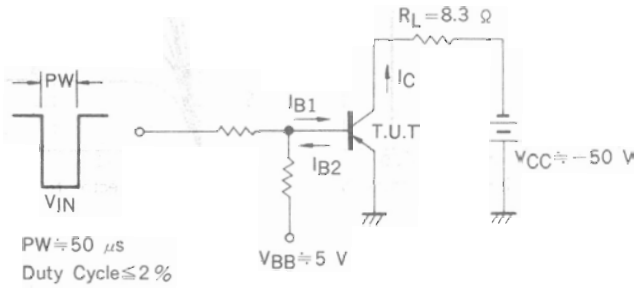
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

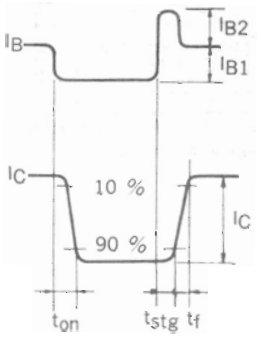


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

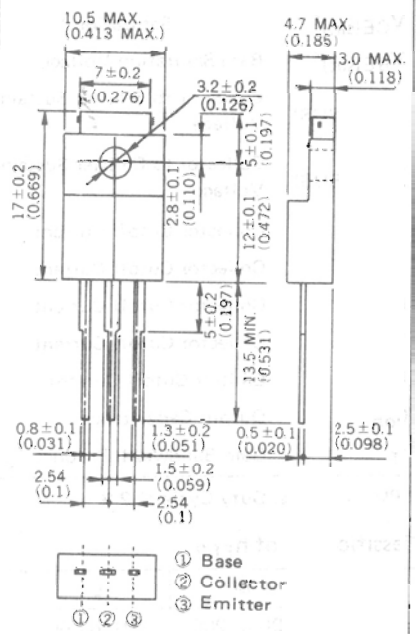
PNP SILICON POWER TRANSISTOR
2SA1444

DESCRIPTION The 2SA1444 is PNP silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SC3694.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100	V
V_{CEO}	Collector to Emitter Voltage	−60	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−15	A
$I_{C(pulse)}$	Collector Current (pulse)*	−30	A
$I_{B(DC)}$	Base Current (DC)	−7.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = −8.0 A, I_{B1} = −I_{B2} = −0.4 A R_L = 6.3 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = −2.0 V, I_C = −1.5 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = −2.0 V, I_C = −3.0 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = −2.0 V, I_C = −8.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			−0.3	V	I_C = −8.0 A, I_B = −0.4 A
$V_{BE(sat)}$*	Base Saturation Voltage			−1.2	V	I_C = −8.0 A, I_B = −0.4 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −8.0 A, I_B = −0.8 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	−60			V	I_C = −8.0 A, I_{B1} = −I_{B2} = −0.8 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −60 V, $V_{BE(OFF)}$ = 1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −5.0 V, I_C = 0
C_{ob}	Output Capacitance		300		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		80		MHz	V_{CE} = −10 V, I_C = −1.5 A

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

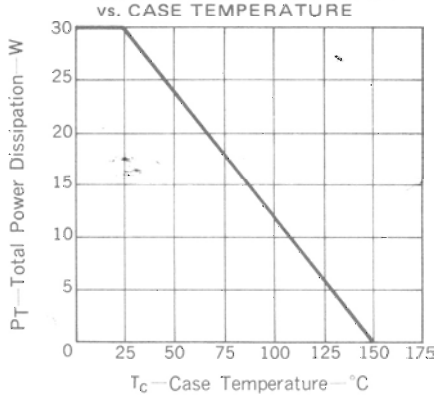
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

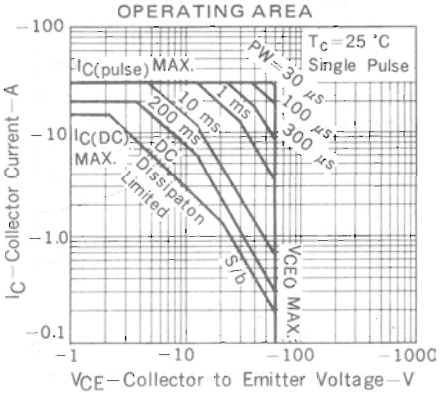
Test Conditions: V_{CE} = −2.0 V, I_C = −3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

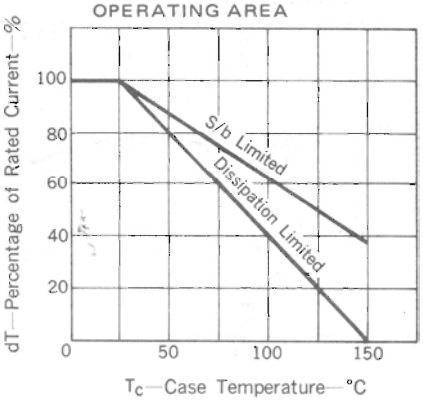
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



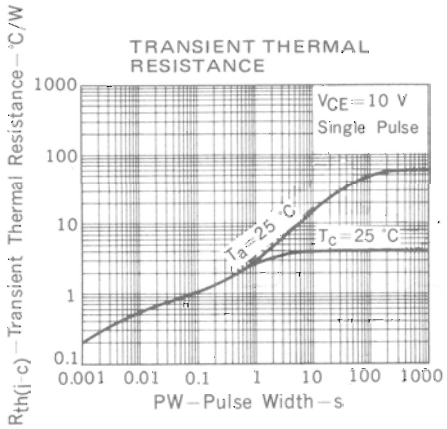
FORWARD BIAS SAFE OPERATING AREA



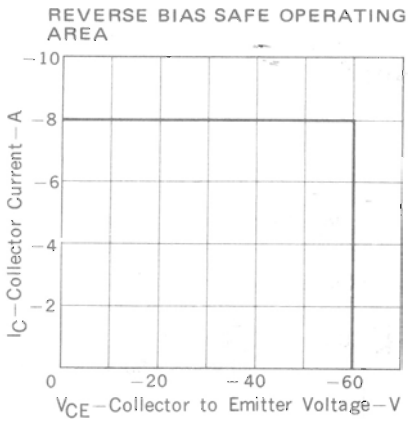
DERATING CURVE OF SAFE OPERATING AREA



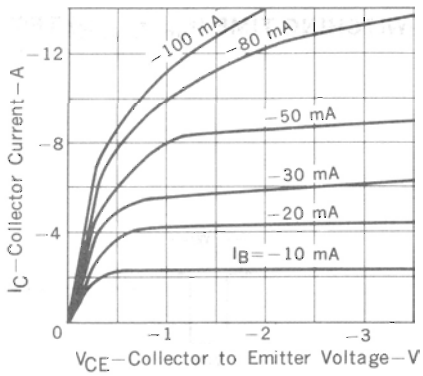
TRANSIENT THERMAL RESISTANCE



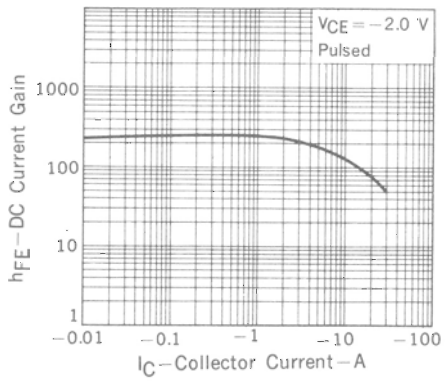
REVERSE BIAS SAFE OPERATING AREA



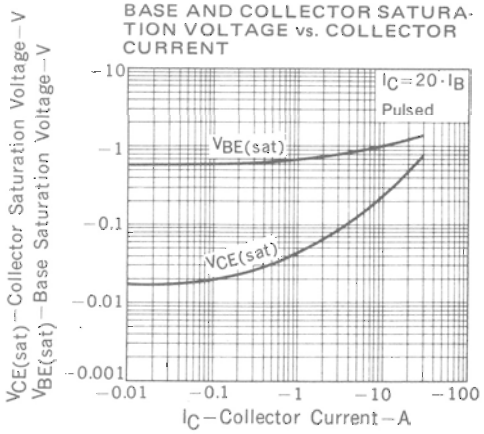
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



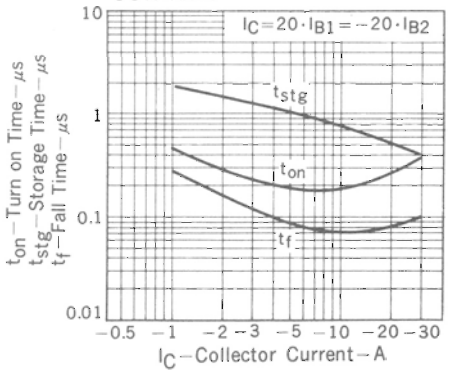
DC CURRENT GAIN vs. COLLECTOR CURRENT



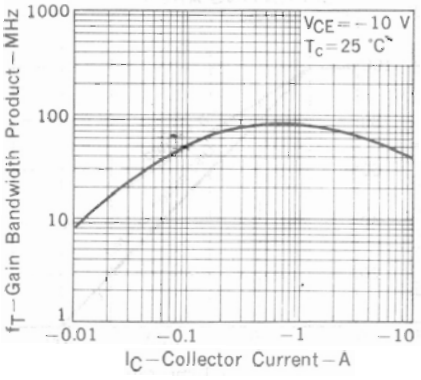
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



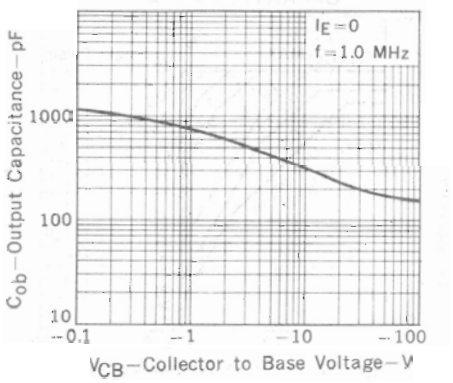
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



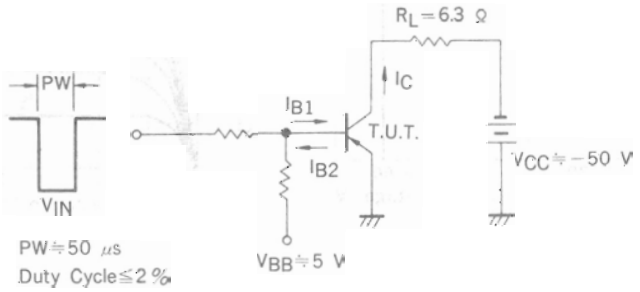
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

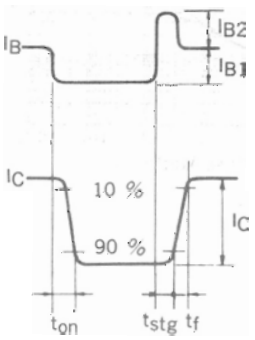


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

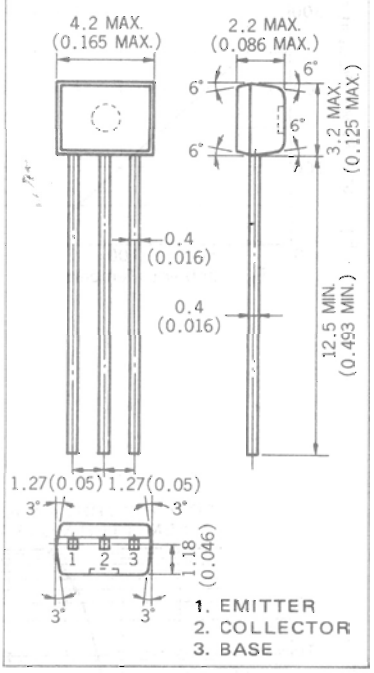
PNP SILICON TRANSISTOR
2SA1458

DESCRIPTION The 2SA1458 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.
- Low Collector Saturation Voltage.
- Complementary to the NEC 2SC3731 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −40 V
- V_{CEO} Collector to Emitter Voltage . . . . . −40 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current (DC) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			70	ns	See Test Circuit.
t_{stg}	Storage Time		110	225	ns	See Test Circuit.
t_{off}	Turn-off Time			300	ns	See Test Circuit.
f_T	Gain Bandwidth Product	200	510		MHz	V_{CE} = −20 V, I_E = 10 mA, f = 100 MHz
C_{ob}	Output Capacitance		2.5	4.5	pF	V_{CB} = −5.0 V, I_E = 0, f = 1 MHz
h_{FE1}*	DC Current Gain	75	180	300	—	V_{CE} = −1.0 V, I_C = −100 mA
h_{FE2}*	DC Current Gain	25	100		—	V_{CE} = −1.0 V, I_C = −1.0 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.1	−0.4	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.80	−0.95	V	I_C = −50 mA, I_B = −5.0 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB} = −3.0 V, I_C = 0

* Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

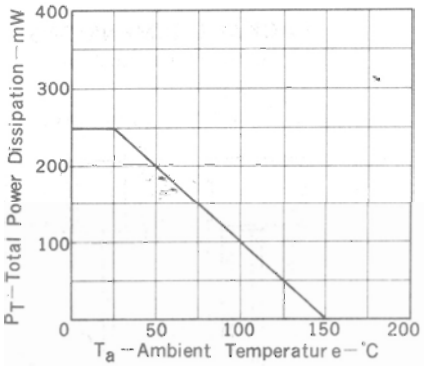
Classification of h_{FE1}

Rank	M	L	K
Range	75 to 150	100 to 200	150 to 300

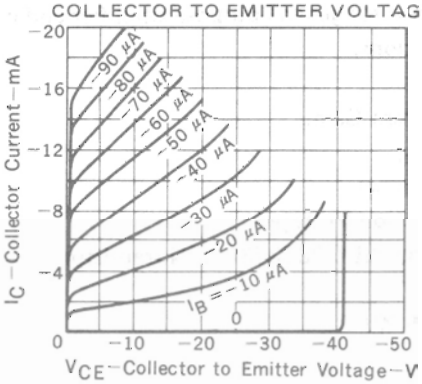
h_{FE1} Test Conditions : V_{CE} = −1.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

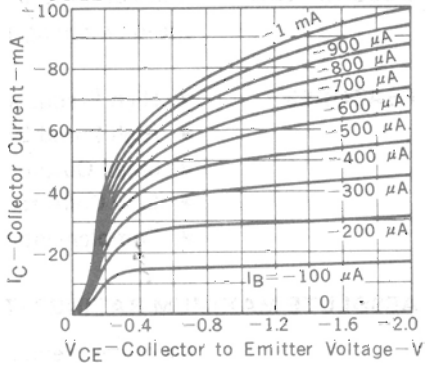
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



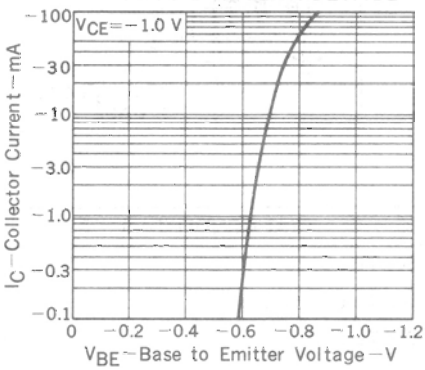
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



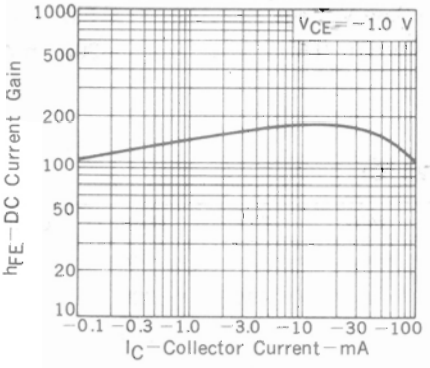
COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE



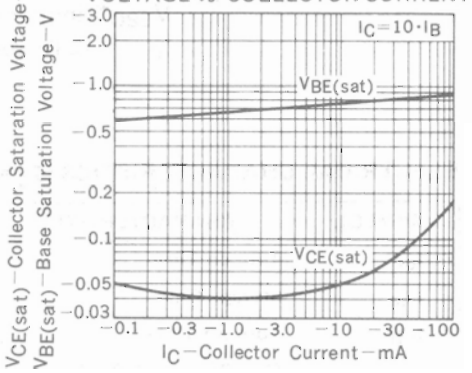
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



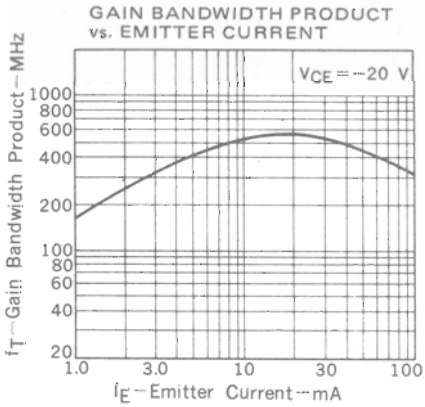
DC CURRENT GAIN vs. COLLECTOR CURRENT



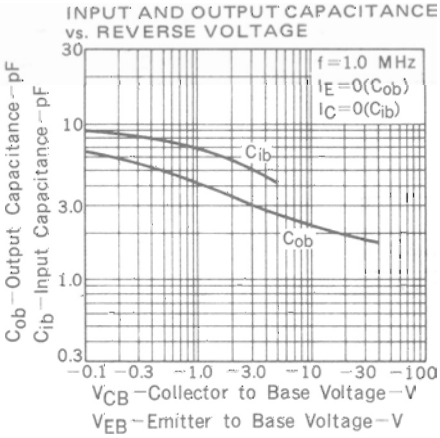
BASE AND COLLECTOR SATURATION VOLTAGE vs COLLECTOR CURRENT



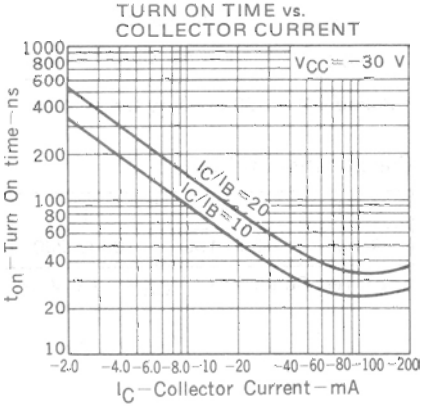
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



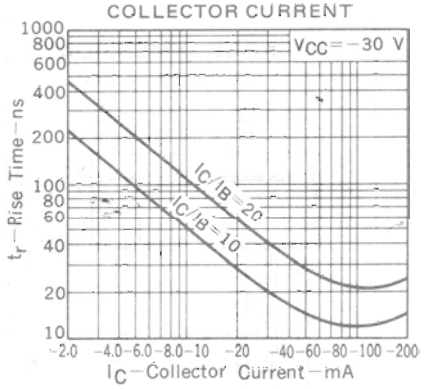
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



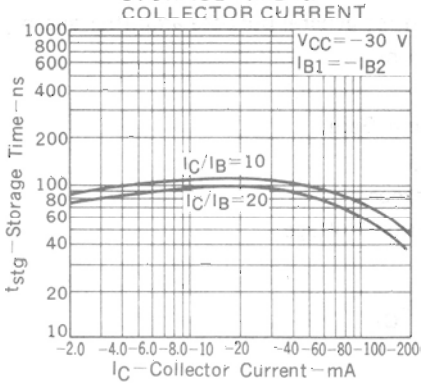
TURN ON TIME vs. COLLECTOR CURRENT



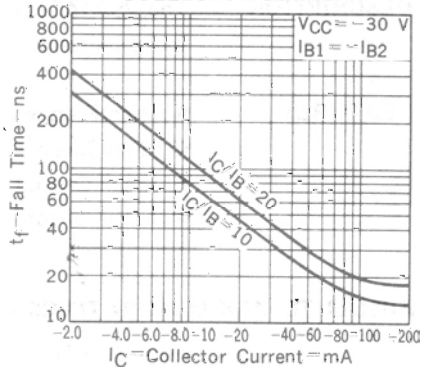
RISE TIME vs. COLLECTOR CURRENT



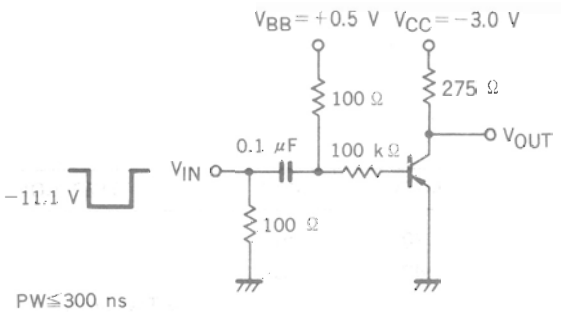
STORAGE TIME vs. COLLECTOR CURRENT



FALL TIME vs. COLLECTOR CURRENT

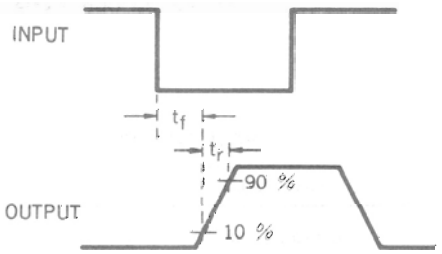


SWITCHING TIME TEST CIRCUIT

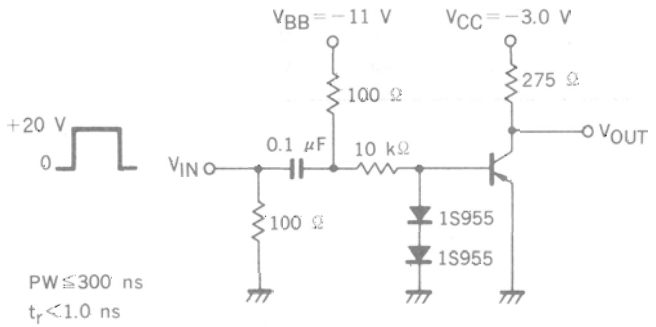


PW≦300 ns
t_r<1.0 ns
Z_{IN}=50 Ω
Duty Cycle=2 %

t_{on} SWITCHING

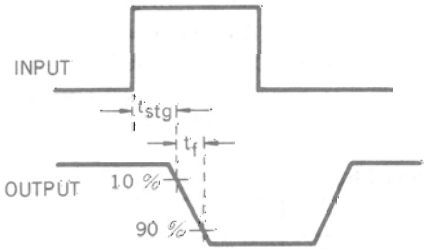


$t_{on} = t_f + t_r$



PW≦300 ns
t_r<1.0 ns
Duty Cycle=2 %

t_{off} SWITCHING



$t_{off} = t_{stg} + t_f$

NEC
ELECTRON DEVICE

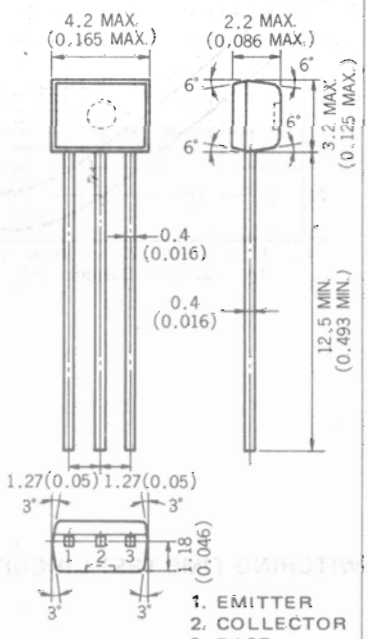
PNP SILICON TRANSISTOR
2SA1459

DESCRIPTION The 2SA1459 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −15 V
- V_{CEO} Collector to Emitter Voltage . . . . . −15 V
- V_{EBO} Emitter to Base Voltage . . . . . −4.5 V
- I_C Collector Current (DC) . . . . . −50 mA
- I_C Collector Current (Pulse)* . . . . . −100 mA

* PW ≤ 2 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time		9.0	20	ns	See Test Circuit.
t_{off}	Turn-off Time		19	40	ns	See Test Circuit.
t_{stg}	Storage Time		16	40	ns	See Test Circuit.
f_T	Gain Bandwidth Product	800	1800		MHz	V_{CE} = −10 V, I_E = 10 mA, f = 100 MHz
C_{ob}	Output Capacitance		2.0	3.0	pF	V_{CB} = −5.0 V, I_E = 0, f = 1 MHz
h_{FE1}**	DC Current Gain	50	80	150	—	V_{CE} = −1.0 V, I_C = −10 mA
h_{FE2}**	DC Current Gain	30	70		—	V_{CE} = −1.0 V, I_C = −1.0 mA
$V_{CE(sat)}$**	Collector Saturation Voltage		−0.09	−0.20	V	I_C = −10 mA, I_B = −1.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		−0.80	−0.95	V	I_C = −10 mA, I_B = −1.0 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −8.0 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB} = −3.0 V, I_C = 0

** Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

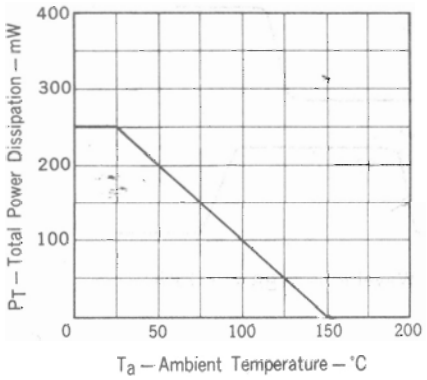
Classification of h_{FE1}

Rank	L	K
Range	50 to 100	75 to 150

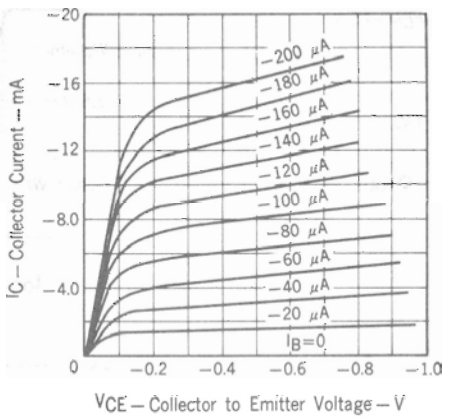
h_{FE2} Test Conditions: V_{CE} = −1.0 V, I_C = −10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

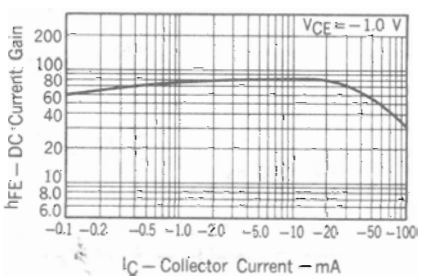
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



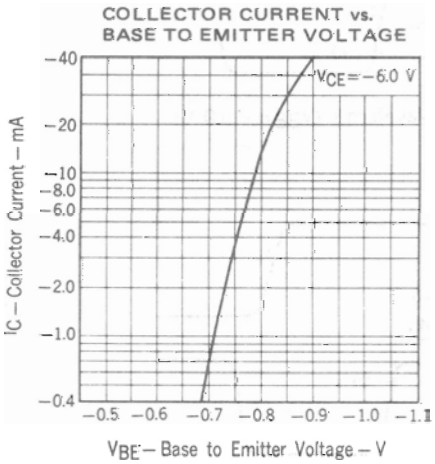
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



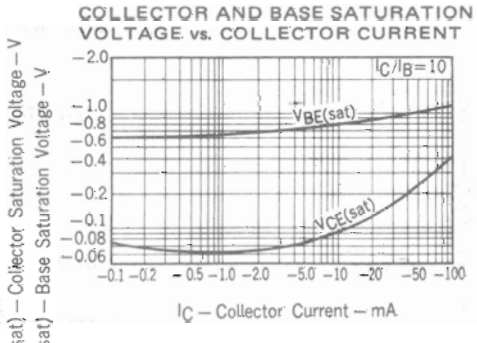
DC CURRENT GAIN vs. COLLECTOR CURRENT



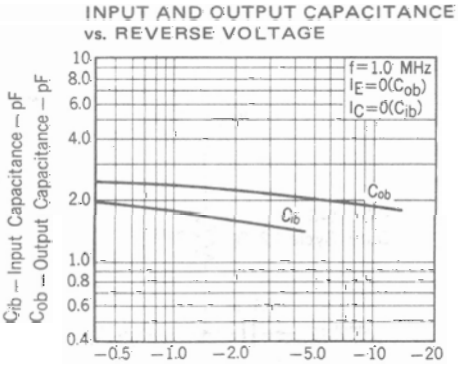
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



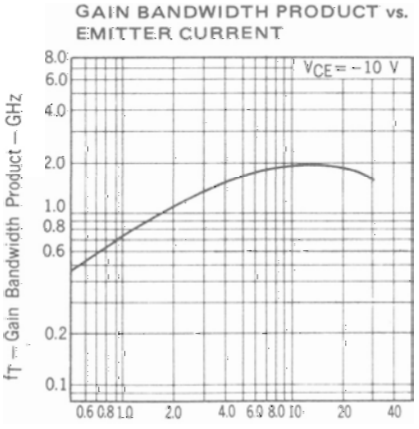
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



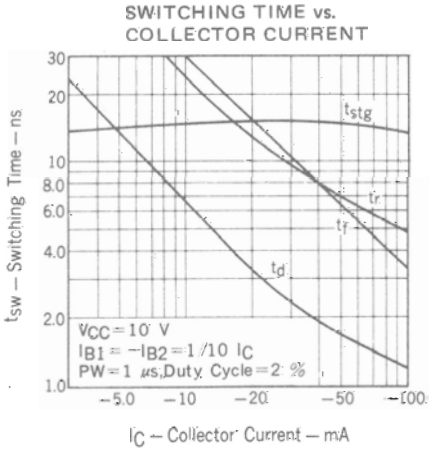
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



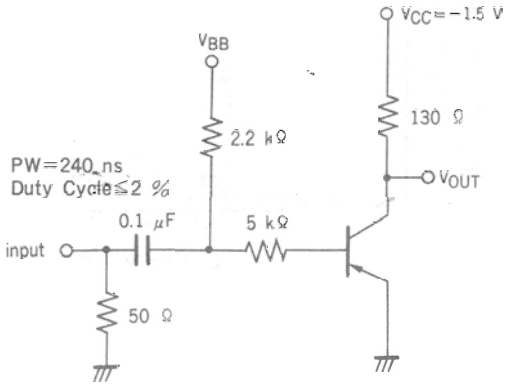
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



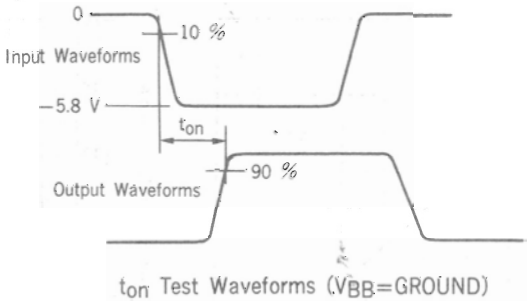
SWITCHING TIME vs. COLLECTOR CURRENT



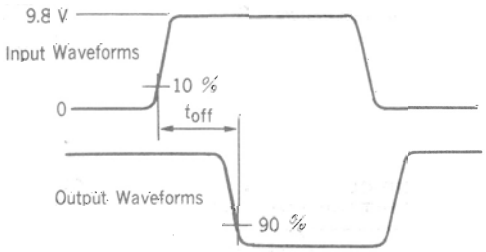
SWITCHING TIME TEST CIRCUIT



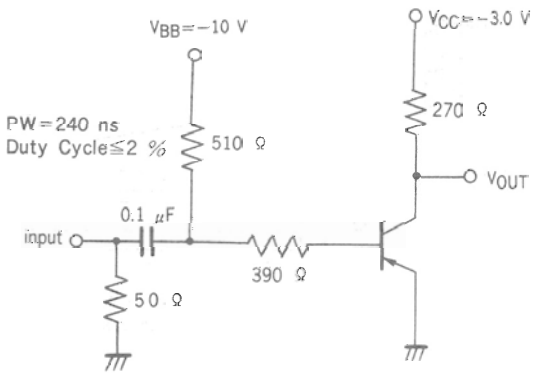
t_{on}, t_{off} Test Circuit



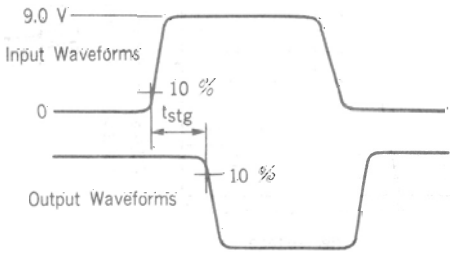
t_{on} Test Waveforms (V_{BB}=GROUND)



t_{off} Test Waveforms (V_{BB}=−8.0 V)



t_{stg} Test Circuit



t_{stg} Test Waveforms

NEC
ELECTRON DEVICE

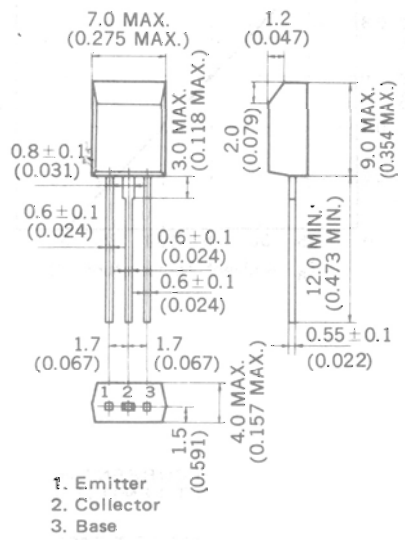
PNP SILICON TRANSISTOR
2SA1460

DESCRIPTION The 2SA1460 is designed for power amplifier and high speed switching applications.

FEATURES

- High speed, high voltage switching.
- Low Collector Saturation Voltage.
- Complementary to the NEC 2SC3733 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−60	V
V_{CEO}	Collector to Emitter Voltage	−45	V
V_{EBO}	Emitter Base Voltage	−5.0	V
$I_{C(DC)}$	Collector Current (DC)	−1.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	−2.0	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time		25	40	ns	V_{CC} = −10 V, I_C = −500 mA, $I_{B1} = -I_{B2}$ = −50 mA
t_{stg}	Storage Time		46	70	ns	
t_{off}	Turn-off Time		62	100	ns	
f_T	Gain Bandwidth Product	300	400		MHz	V_{CE} = −10 V, I_E = 100 mA
C_{ob}	Output Capacitance		11	25	pF	V_{CB} = −10 V, I_E = 0, f = 1 MHz
h_{FE1}*	DC Current Gain	60	120	200	–	V_{CE} = −10 V, I_C = −50 mA
h_{FE2}*	DC Current Gain	60	150		–	V_{CE} = −10 V, I_C = −500 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.26	−0.60	V	I_C = −500 mA, I_B = −50 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.98	−1.20	V	I_C = −500 mA, I_B = −50 mA
I_{CES}	Collector Cutoff Current			−0.5	μA	V_{CB} = −45 V, R_{BE} = 0
I_{EBO}	Emitter Cutoff Current			−0.5	μA	V_{EB} = −4.0 V, I_C = 0

* Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE1}

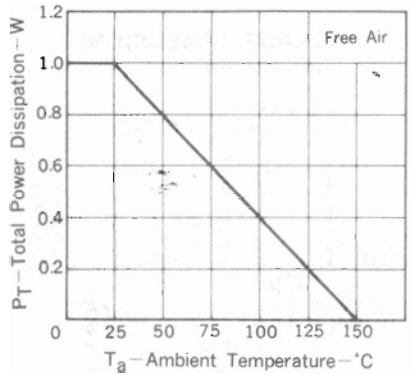
Rank	L	K
Range	60 to 120	100 to 200

h_{FE1} Test Conditions: V_{CE} = −10 V, I_C = −50 mA

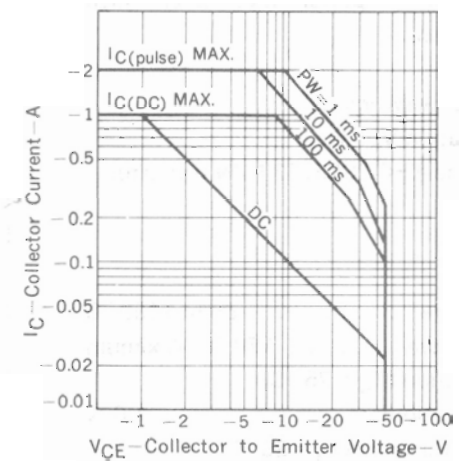
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

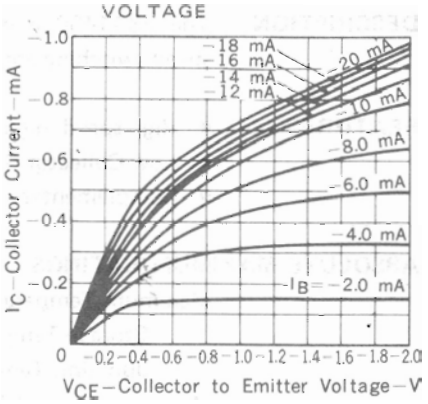
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



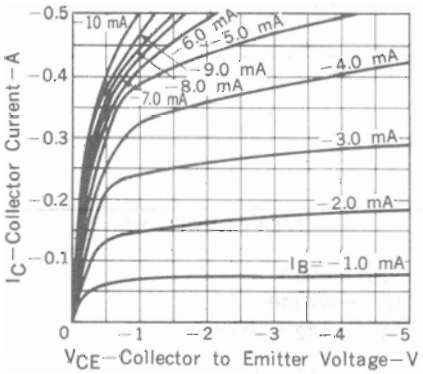
SAFE OPERATING AREA (TRANSIENT THERMAL RESISTANCE METHOD)



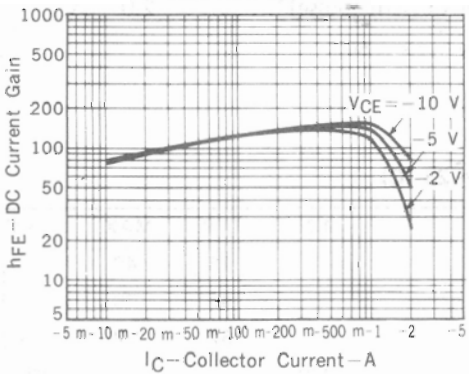
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



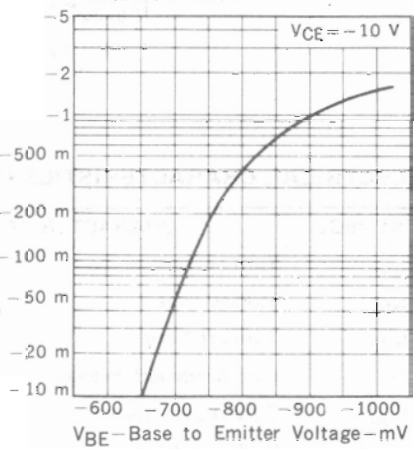
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



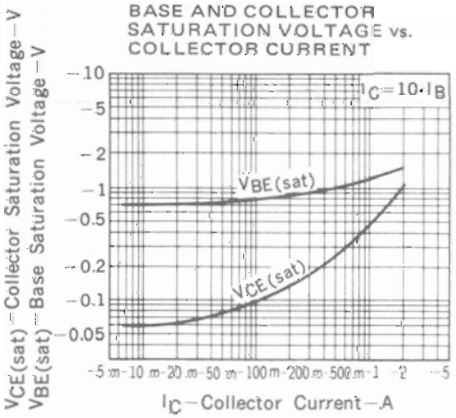
DC CURRENT GAIN vs. COLLECTOR CURRENT



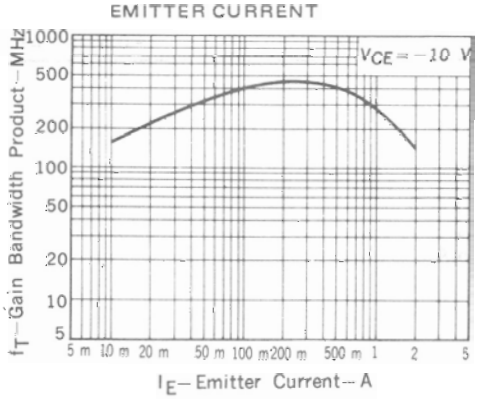
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



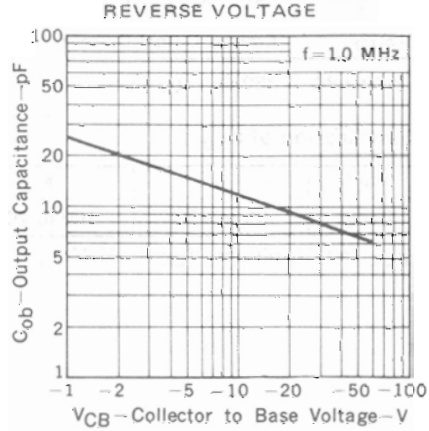
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



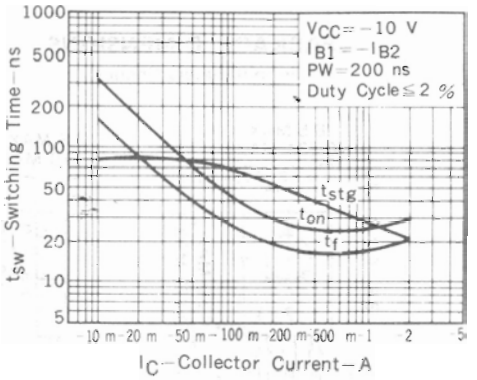
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



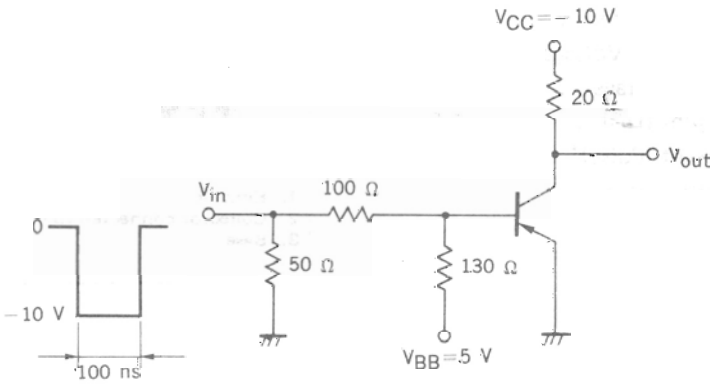
OUTPUT CAPACITANCE vs. REVERSE VOLTAGE

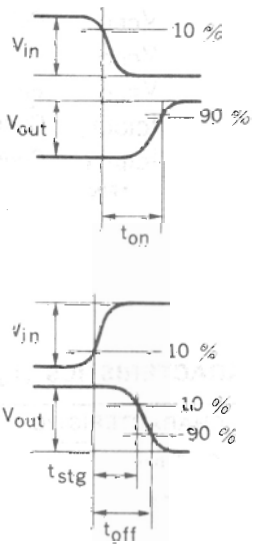


SWITCHING TIME vs.
COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

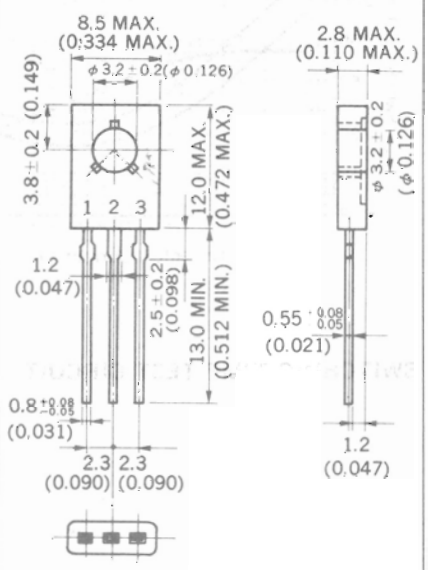
PNP SILICON POWER TRANSISTOR
2SA1486

NEW DEVICE

DESCRIPTION The 2SA1486 is designed for use in high speed and high voltage switching.
It is suitable for switching regulators, DC-DC converters and ultrasonic appliance applications.

FEATURES
- High speed switching
- High Voltage

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)
- Total Power Dissipation . . . . . 15 W

Maximum Voltage and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−600	V
V_{CEO}	Collector to Emitter Voltage . .	−600	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−1.0	A
$I_{C(pulse)}$	Collector Current (Pulse)* . . .	−2.0	A

*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time		0.1	0.5	μs	I_C = −0.5 A, I_{B1} = −I_{B2} = −0.1 A R_L = 500 Ω, V_{CC} ≒ −250 V
t_{stg}	Storage Time		3.5	5.0	μs	
t_f	Fall Time		0.08	0.5	μs	
h_{FE1}**	DC Current Gain	30		120	—	V_{CE} = −5.0 V, I_C = −0.1 A
h_{FE2}**	DC Current Gain	5			—	V_{CE} = −5.0 V, I_C = −0.5 A
$V_{CE(sat)}$**	Collector Saturation Voltage			−1.0	V	I_C = −0.3 A, I_B = −0.06 A
$V_{BE(sat)}$**	Base Saturation Voltage			−1.2	V	I_C = −0.3 A, I_B = −0.06 A
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −600 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB} = −7.0 V, I_C = 0

** Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

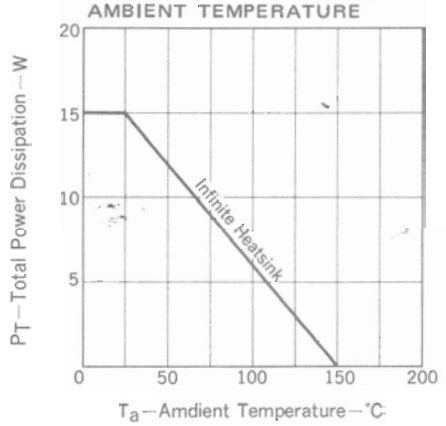
Classification of h_{FE1}

Rank	M	L	K
Range	30 to 60	40 to 80	60 to 120

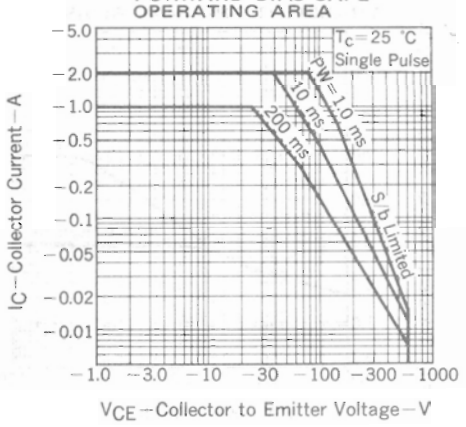
Test Conditions: V_{CE} = −5.0 V, I_C = −0.1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

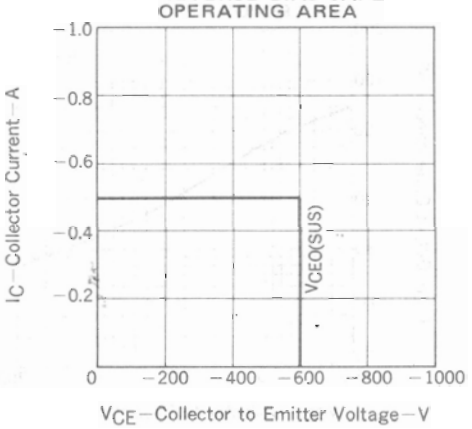
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



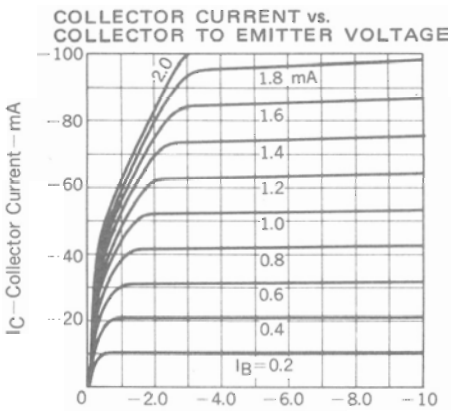
FORWARD BIAS SAFE OPERATING AREA



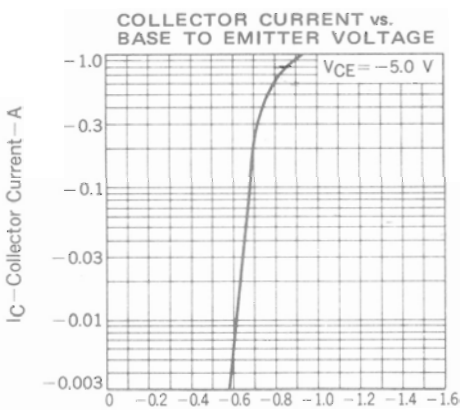
REVERSE BIAS SAFE OPERATING AREA



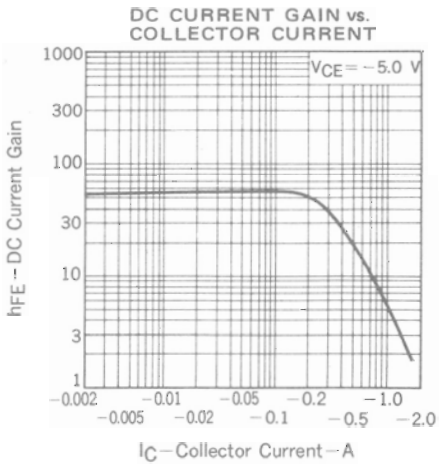
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



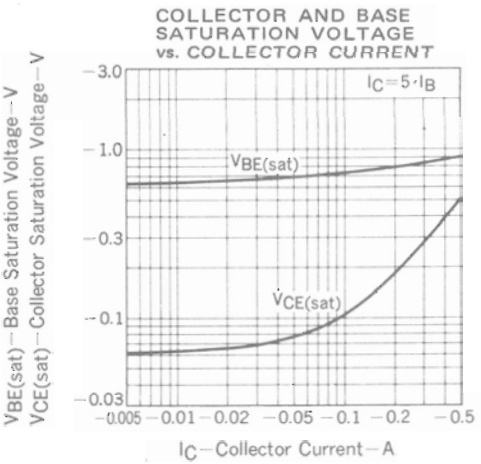
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



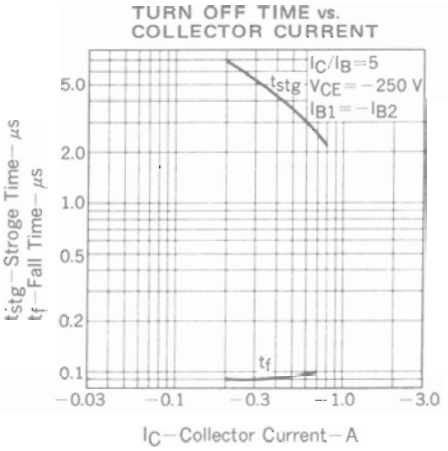
DC CURRENT GAIN vs. COLLECTOR CURRENT



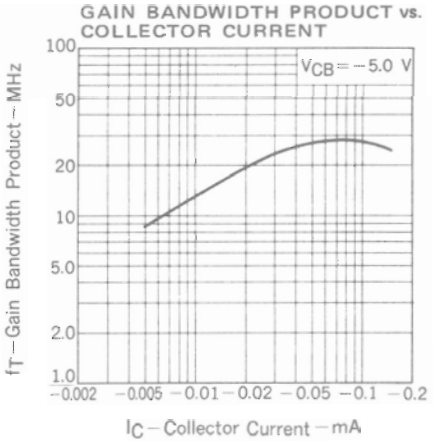
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



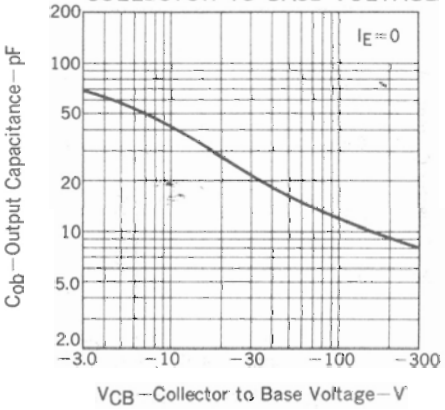
TURN OFF TIME vs. COLLECTOR CURRENT



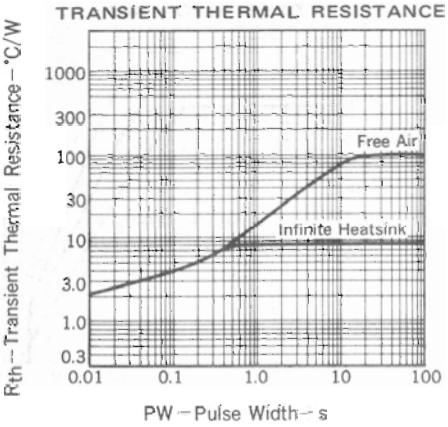
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



TRANSIENT THERMAL RESISTANCE



NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
2SA1544

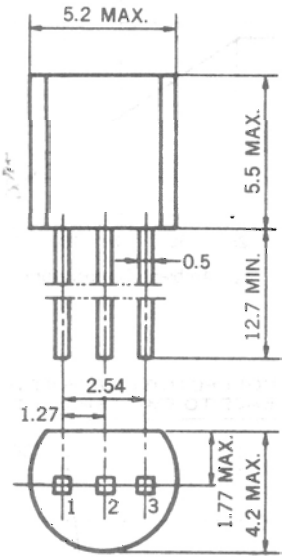
NEW DEVICE

DESCRIPTION The 2SA1544 is designed for uses of high-resolution monitor TV applications. This makes it possible to raise the video band of high-resolution monitor TVs to 50 MHz.

FEATURES

- High f_T: f_T = 300 MHz TYP. (@V_{CE} = –30 V, I_E = 30 mA)
- Low C_{ob}: C_{ob} = 3.3 pF (@V_{CB} = –30 V)
- High Voltage: V_{CBO} = V_{CEO} = –250 V
- High Total Power Dissipation: P_T = 0.75 W
- Complementary to 2SC3999

PACKAGE DIMENSIONS
in millimeters



1. Emitter
2. Collector
3. Base

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . –55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 750 mW

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	–250	V
V_{CEO}	Collector to Emitter Voltage	–250	V
V_{EBO}	Emitter to Base Voltage	–5.0	V
I_C	Collector Current	–100	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	150	320	–	V_{CE} = –10 V, I_C = –10 mA
f_T	Gain Bandwidth Product	200	300		MHz	V_{CE} = –30 V, I_E = 30 mA
C_{ob}	Output Capacitance		3.3	3.7	pF	V_{CB} = –30 V, I_E = 0, f = 1 MHz
I_{CBO}	Collector Cutoff Current			–100	nA	V_{CB} = –200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			–100	nA	V_{EB} = –3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		–0.12	–0.3	V	I_C = –10 mA, I_B = –1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		–0.73	–1.2	V	I_C = –10 mA, I_B = –1.0 mA
V_{ESDR}	Electrostatic Discharge-Resistant		800		V	C = 1 000 pF, E-B Reverse Bias

* Pulsed PW < 350 μs, Duty Cycle < 2 %

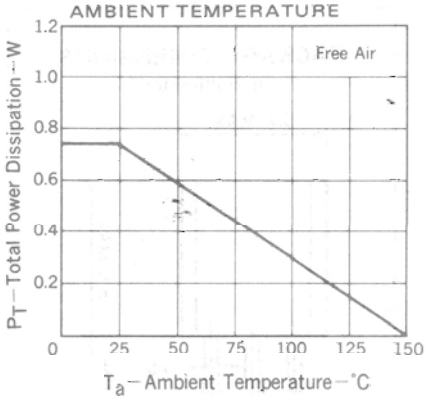
Classification of h_{FE}

Rank	M	L	K
Range	60 to 120	100 to 200	160 to 320

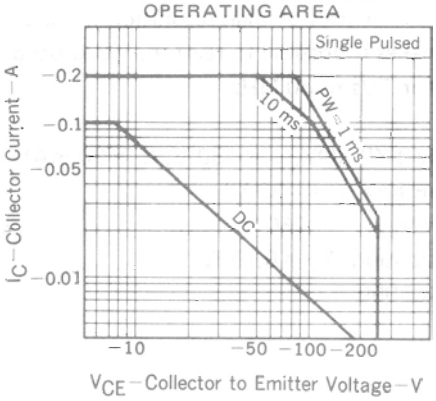
Test Conditions: V_{CE} = –10 V, I_C = –10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

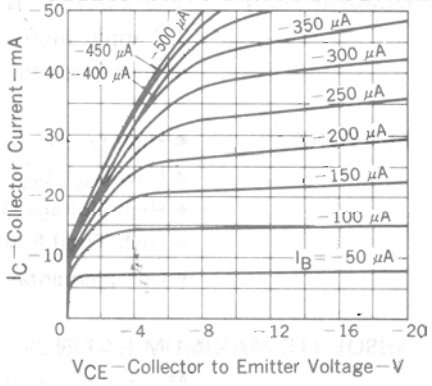
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



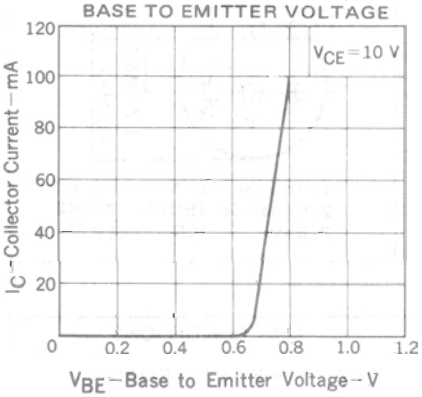
FORWARD BIAS SAFE OPERATING AREA



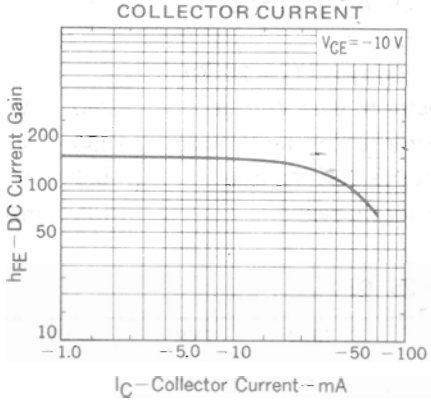
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



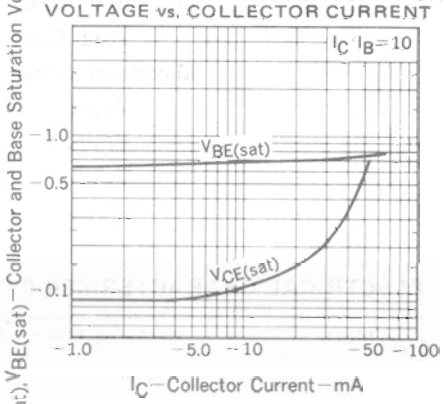
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



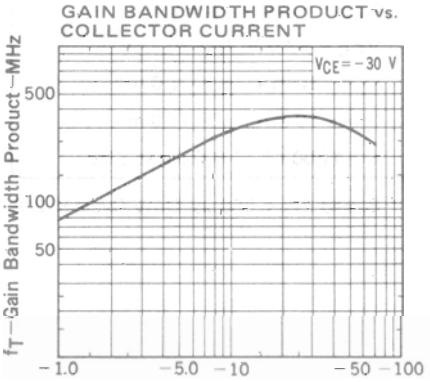
DC CURRENT GAIN vs. COLLECTOR CURRENT



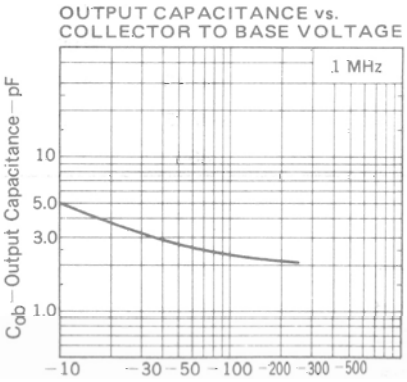
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

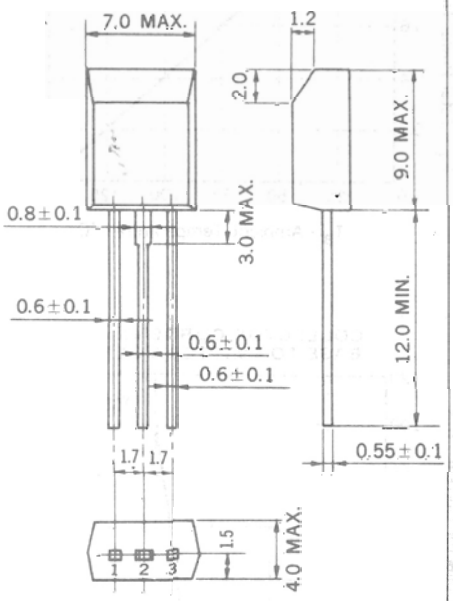
PNP SILICON TRANSISTOR
2SA1545

DESCRIPTION The 2SA1545 is designed for uses of high-resolution monitor TV applications. This makes it possible to raise the video band of high-resolution monitor TVs to 50 MHz.

FEATURES

- High f_T: f_T = 300 MHz TYP. (@V_{CE} = −30 V, I_E = 30 mA)
- Low C_{ob}: C_{ob} = 3.3 pF (@V_{CB} = −30 V)
- High Voltage: V_{CBO} = V_{CEO} = −250 V
- High Total Power Dissipation: P_T = 1.0 W
- Complementary to 2SC4000

PACKAGE DIMENSIONS
in millimeters



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−250	V
V_{CEO}	Collector to Emitter Voltage	−250	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
I_C	Collector Current	−100	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	150	320	−	V_{CE} = −10 V, I_C = −10 mA
f_T	Gain Bandwidth Product	200	300		MHz	V_{CE} = −30 V, I_E = 30 mA
C_{ob}	Output Capacitance		3.3	3.7	pF	V_{CB} = −30 V, I_E = 0, f = 1 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = −200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = −3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		−0.12	−0.3	V	I_C = −10 mA, I_B = −1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.73	−1.2	V	I_C = −10 mA, I_B = −1.0 mA
V_{ESDR}	Electrostatic Discharge-Resistant		800		V	C = 1 000 pF, E-B Reverse Bias

* Pulsed PW < 350 μs, Duty Cycle < 2 %

Classification of h_{FE}

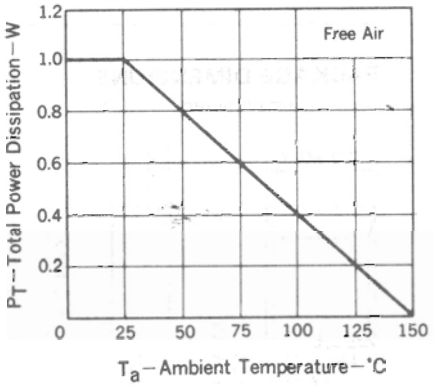
Rank	M	L	K
Range	60 to 120	100 to 200	160 to 320

Test Conditions: V_{CE} = −10 V, I_C = −10 mA

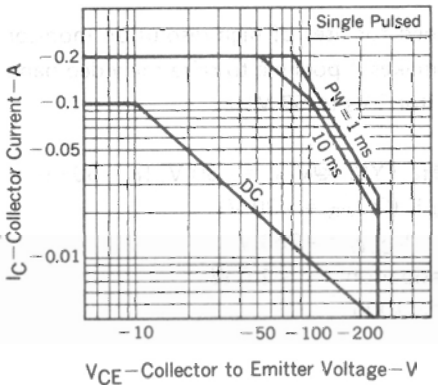
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

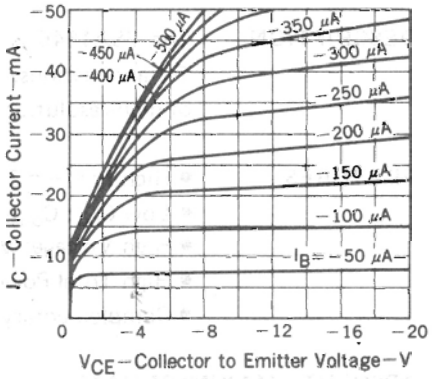
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



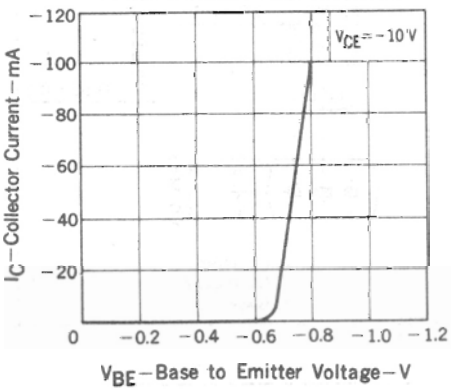
FORWARD BIAS SAFE OPERATING AREA



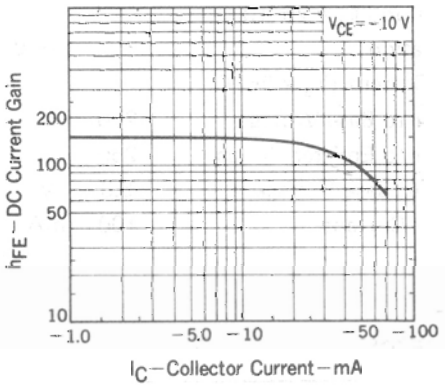
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



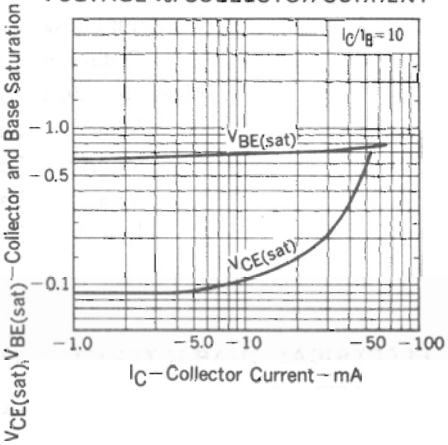
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



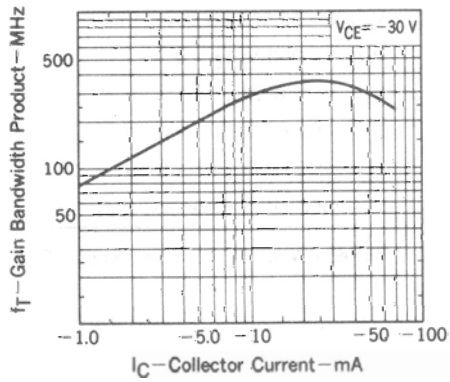
DC CURRENT GAIN vs. COLLECTOR CURRENT



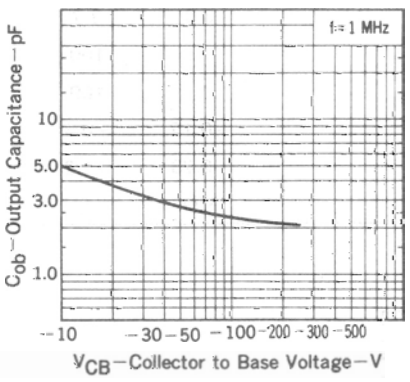
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SA1546

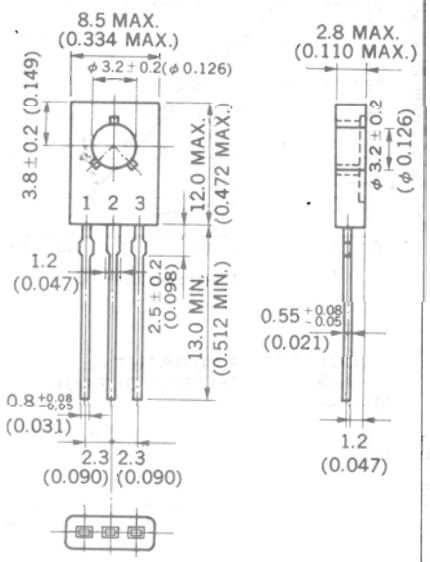
DESCRIPTION

The 2SA1546 is designed for uses of high-resolution monitor TV applications. This makes it possible to raise the video band of high-resolution monitor TVs to 50 MHz.

FEATURES

- High f_T: f_T = 300 MHz TYP. (@V_{CE} = –30 V, I_E = 30 mA)
- Low C_{ob}: C_{ob} = 3.3 pF (@V_{CB} = –30 V)
- High Voltage: V_{CBO} = V_{CEO} = –250 V
- High Total Power Dissipation:
  P_T (T_a/T_c = 25 °C) = 1.3 W/7 W
- Complementary to 2SC4001

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 7 W

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	–250	V
V_{CEO}	Collector to Emitter Voltage	–250	V
V_{EBO}	Emitter to Base Voltage	–5.0	V
I_C	Collector Current	–100	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

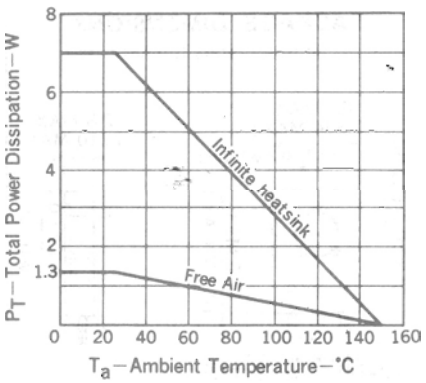
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	150	320	–	V_{CE} = –10 V, I_C = –10 mA
f_T	Gain Bandwidth Product	200	300		MHz	V_{CE} = –30 V, I_E = 30 mA
C_{ob}	Output Capacitance		3.3	3.7	pF	V_{CB} = –30 V, I_E = 0, f = 1 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = –200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = –3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		–0.12	–0.3	V	I_C = –10 mA, I_B = –1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		–0 73	–1.2	V	I_C = –10 mA, I_B = –1.0 mA
V_{ESDR}	Electrostatic Discharge-Resistant		800		V	C = 1 000 pF, E-B Reverse Bias

* Pulsed PW < 350 μs, Duty Cycle < 2 %

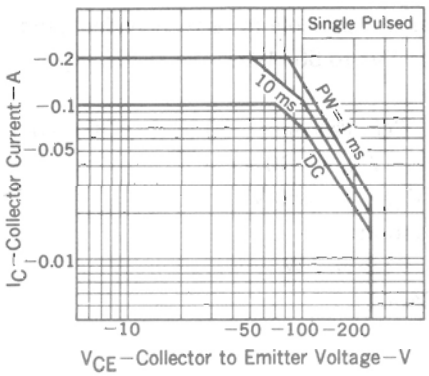
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

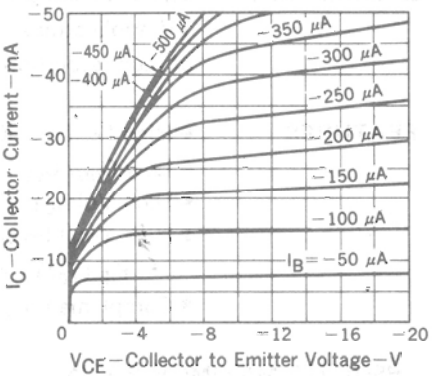
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



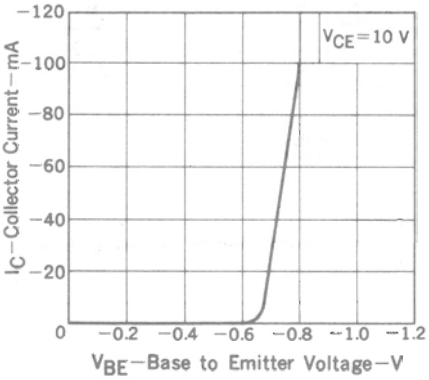
FORWARD BIAS SAFE OPERATING AREA



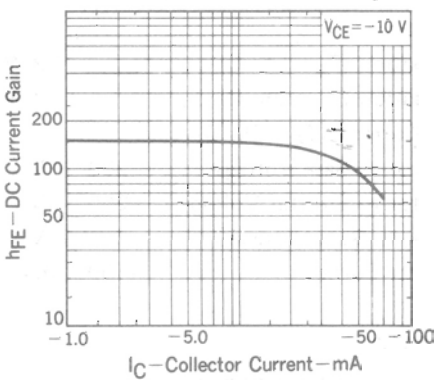
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



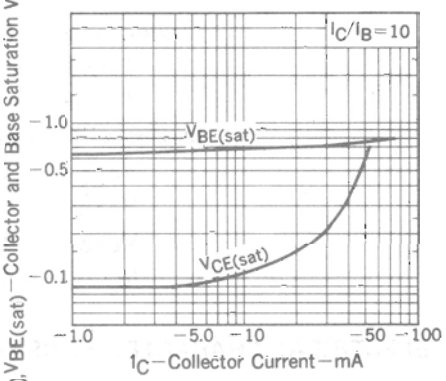
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



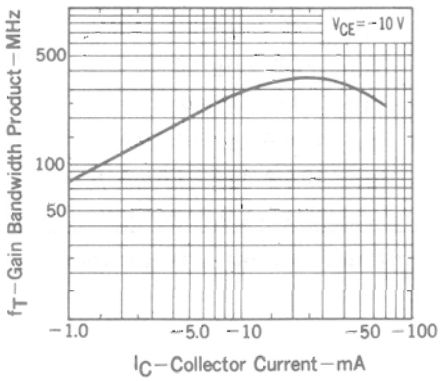
DC CURRENT GAIN vs. COLLECTOR CURRENT



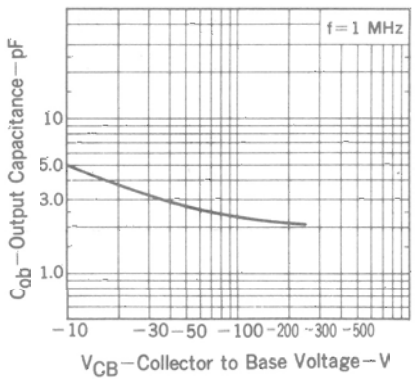
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

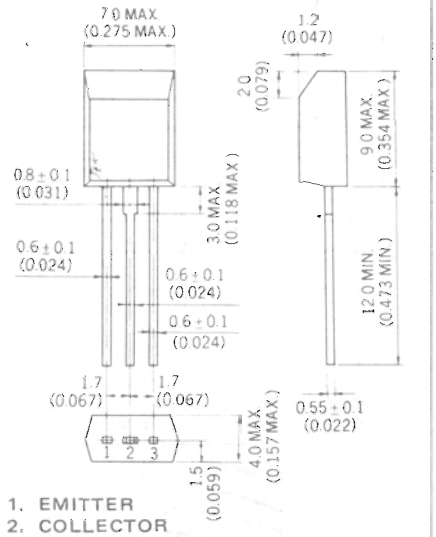
PNP SILICON TRANSISTOR
2SB564

DESCRIPTION The 2SB564 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation:
  1.0 W at 25 °C Ambient Temperature.
- Complementary to the NEC 2SD471 Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 1.0 W
- Thermal Resistance(Junction to Ambient) . . 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −30 V
- V_{CEO} Collector to Emitter Voltage . . . . . −25 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −1.0 A
- I_B Base Current . . . . . −0.1 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	—	V_{CE}=−1.0 V, I_C=−0.1 A
h_{FE2}	DC Current Gain	50	100		—	V_{CE}=−1.0 V, I_C=−1.0 A
f_T	Gain Bandwidth Product		110		MHz	V_{CE}=−6.0 V, I_E=−10 mA
C_{ob}	Collector to Base Capacitance		36		pF	V_{CB}=−6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB}=−30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB}=−5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−600	−640	−700	mV	V_{CE}=−6.0 V, I_C=−10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.25	−0.35	V	I_C=−1.0 A, I_B=−0.1 A
$V_{BE(sat)}$	Base Saturation Voltage		−1.0	−1.2	V	I_C=−1.0 A, I_B=−0.1 A

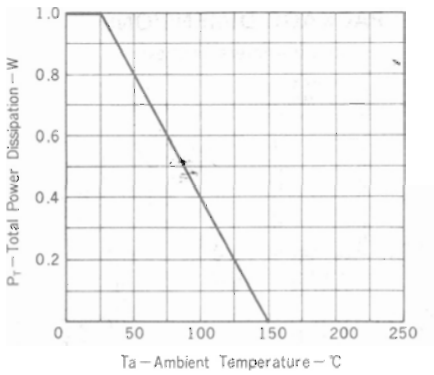
Classification of h_{FE1}

Rank	M	L	K
Range	90 − 180	135 − 270	200 − 400

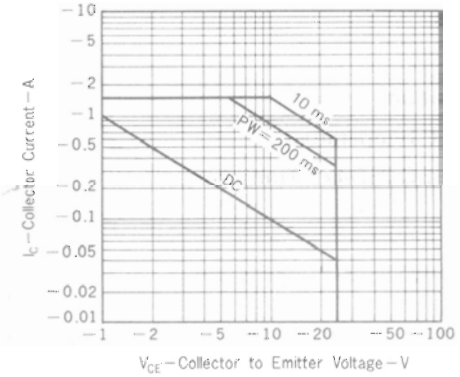
h_{FE1} Test Conditions: V_{CE}=−1.0 V, I_C=−0.1 A

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

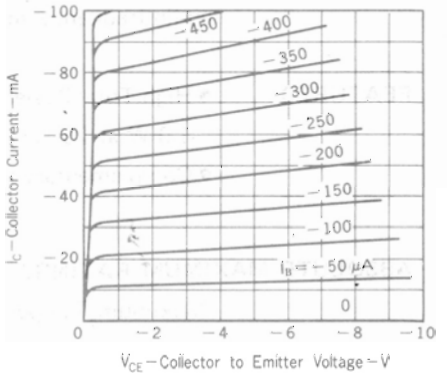
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



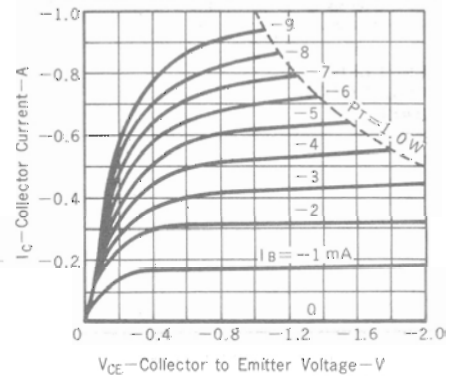
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



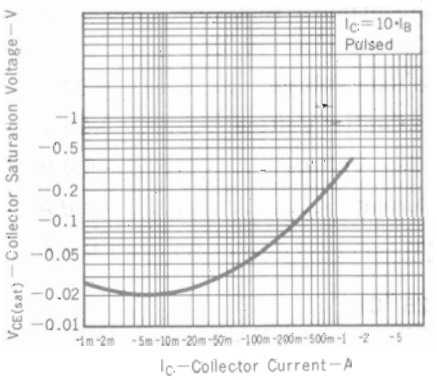
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



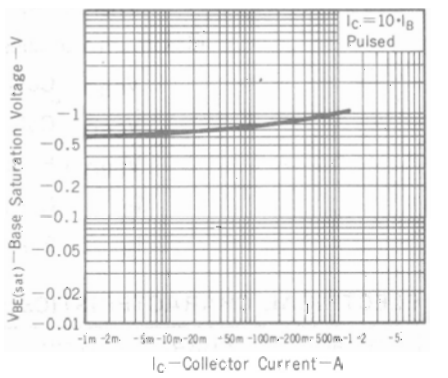
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



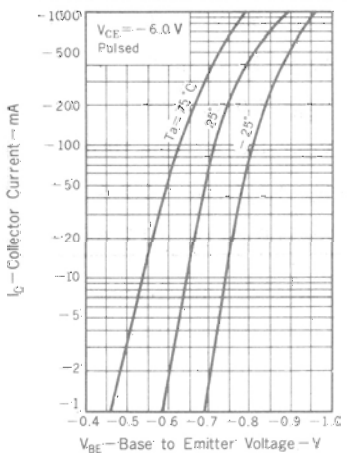
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



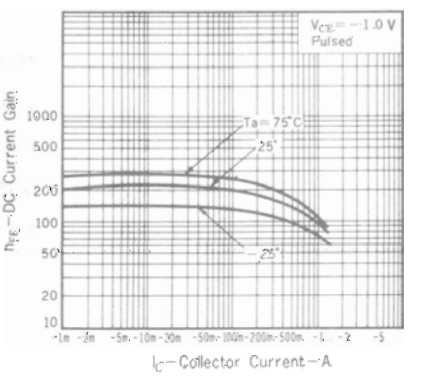
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



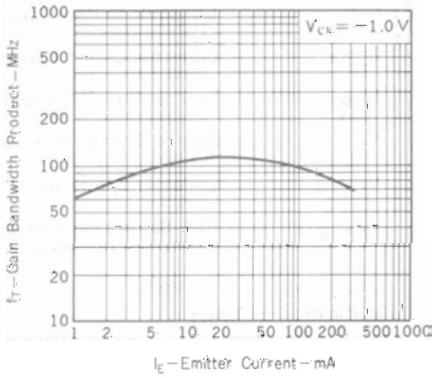
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



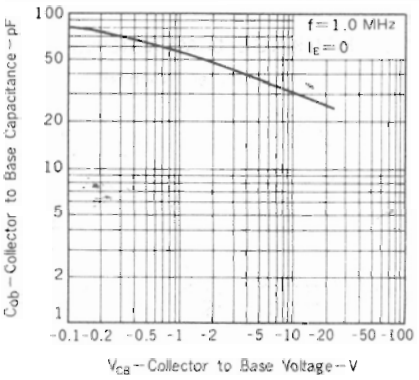
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



COLLECTOR TO BASE CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

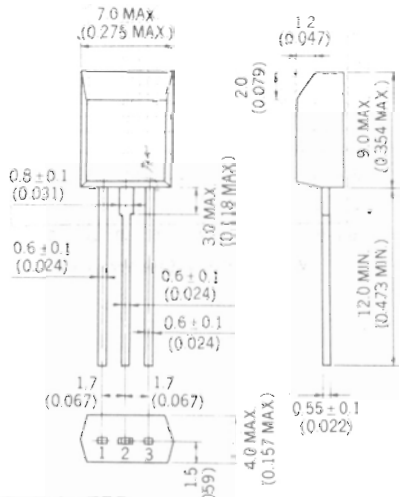
PNP SILICON TRANSISTOR
2SB605

DESCRIPTION The 2SB605 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation and High Breakdown Voltage: 1.0 W at 25 °C Ambient Temperature/V_{CEO} = –50 V
- Complementary to the NEC 2SD571 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 1.0 W
- Thermal Resistance(Junction to Ambient) . . 125 °C/W

Maximum Voltages and Currents (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . –60 V
- V_{CEO} Collector to Emitter Voltage . . . . . –50 V
- V_{EBO} Emitter to Base Voltage . . . . . –5.0 V
- I_C Collector Current . . . . . –0.7 A
- I_B Base Current . . . . . –0.1 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	–	V_{CE}=–1.0 V, I_C=–0.1 A
h_{FE2}	DC Current Gain	50	120		–	V_{CE}=–1.0 V, I_C=–0.5 A
f_T	Gain Bandwidth Product		120		MHz	V_{CE}=–6.0 V, I_E=–10 mA
C_{ob}	Collector to Base Capacitance		25		pF	V_{CB}=–6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			–100	nA	V_{CB}=–60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			–100	nA	V_{EB}=–5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	–600	–630	–700	mV	V_{CE}=–6.0 V, I_C=–10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		–0.16	–0.35	V	I_C=–0.5 A, I_B=–0.05 A
$V_{BE(sat)}$	Base Saturation Voltage		–0.90	–1.2	V	I_C=–0.5 A, I_B=–0.05 A

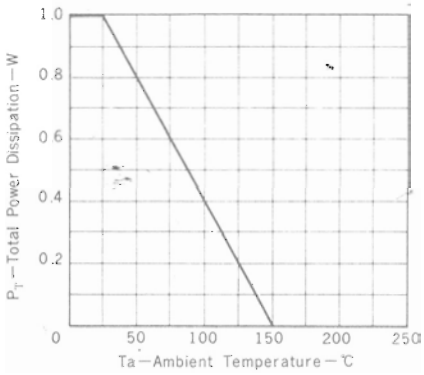
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

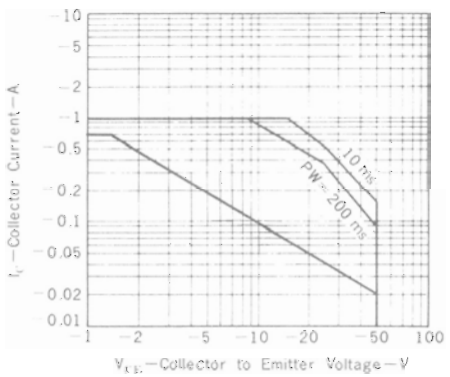
h_{FE1} Test Conditions: V_{CE}=–1.0 V, I_C=–0.1 A

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

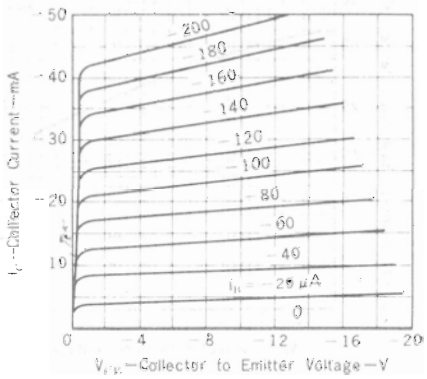
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



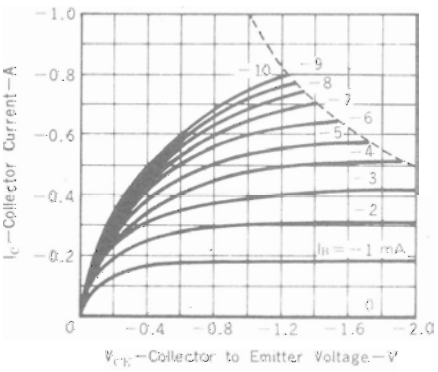
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



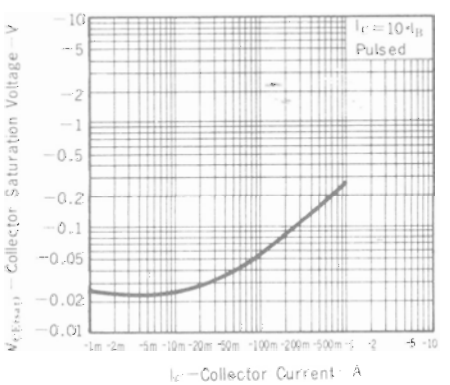
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



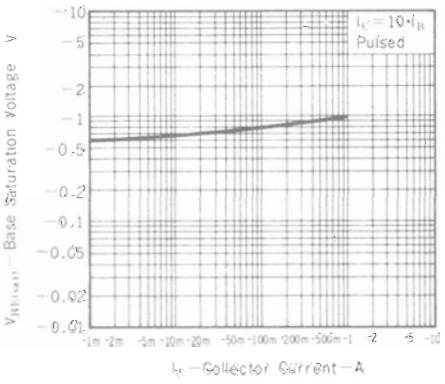
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



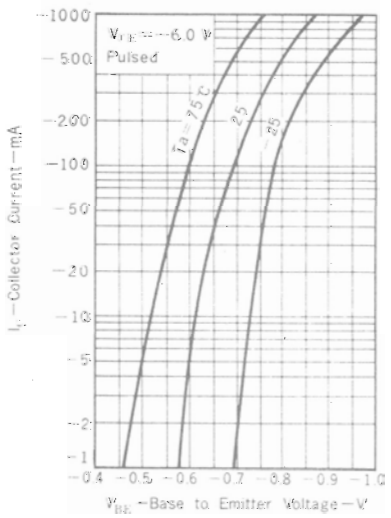
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



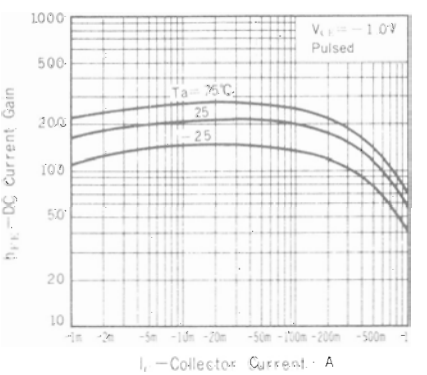
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



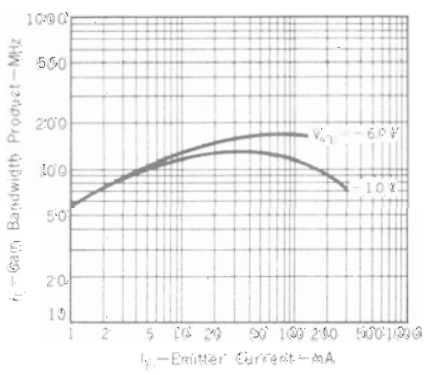
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



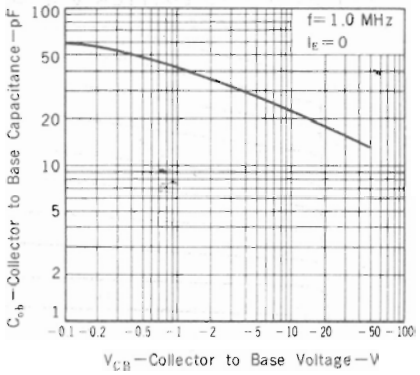
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



COLLECTOR TO BASE CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

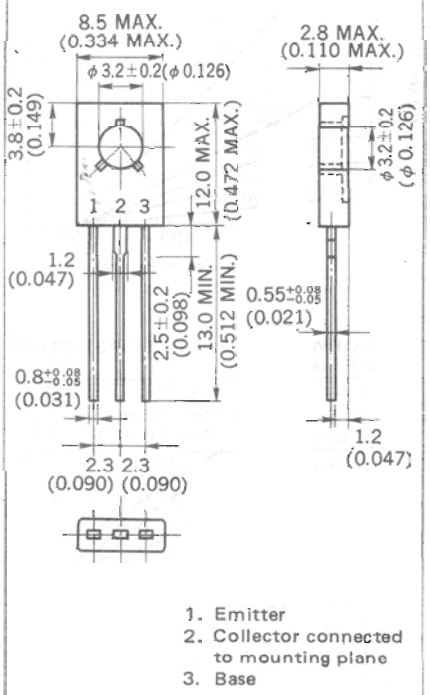
PNP SILICON POWER TRANSISTOR
2SB731

DESCRIPTION The 2SB731 is designed for use in driver and output stages of audio frequency amplifier, and low speed switching.

FEATURES

- Suitable for general driving use, such as lamp, relay or motor.
- Low Collector Saturation Voltage.
- High h_{FE} and Excellent h_{FE} Linearity.
- Complementary to the NEC 2SD809(1) NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- $I_{C(DC)}$ Collector Current . . . . . −1.0 A
- $I_{C(pulse)}$* Collector Current . . . . . −2.0 A
- $I_{B(DC)}$ Base Current . . . . . −5.0 A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	135	250	600	–	V_{CE} = −2.0 V, I_C = −0.1 A
h_{FE2} **	DC Current Gain	40			–	V_{CE} = −1.0 V, I_C = −1.0 A
f_T	Gain Bandwidth Product		75		MHz	V_{CE} = −2.0 V, I_C = −10 mA
C_{ob}	Output Capacitance		25		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB} = −6.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage		−0.5	−0.6	V	I_C = −1.0 A, I_B = −50 mA
$V_{BE(sat)}$ **	Base Saturation Voltage		−1.0	−1.2	V	I_C = −1.0 A, I_B = −50 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

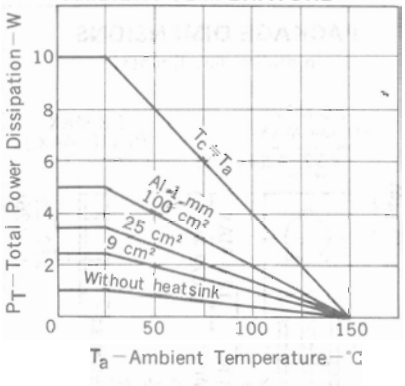
Classification of h_{FE1}

Rank	L	K	F	E
Range	135 to 270	200 to 400	300 to 480	360 to 600

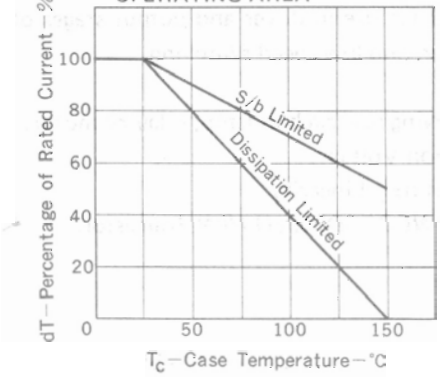
Test Conditions: V_{CE} = −2.0 V, I_C = −0.1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

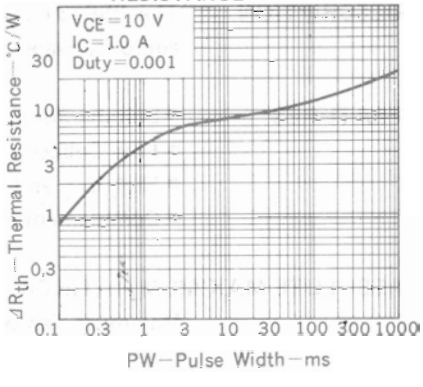
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



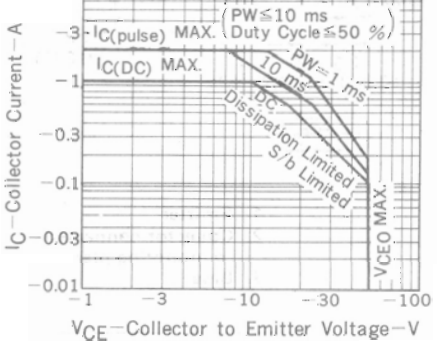
DERATING CURVE OF SAFE OPERATING AREA



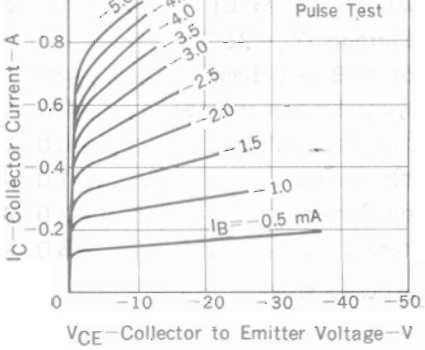
TRANSIENT THERMAL RESISTANCE



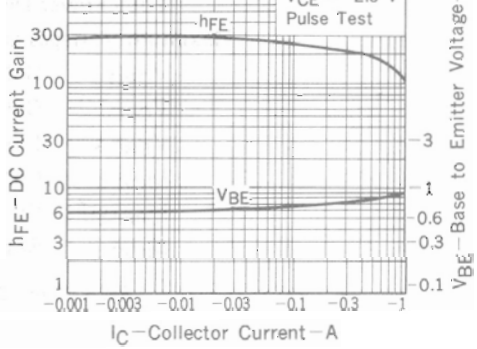
FORWARD BIAS SAFE OPERATING AREA



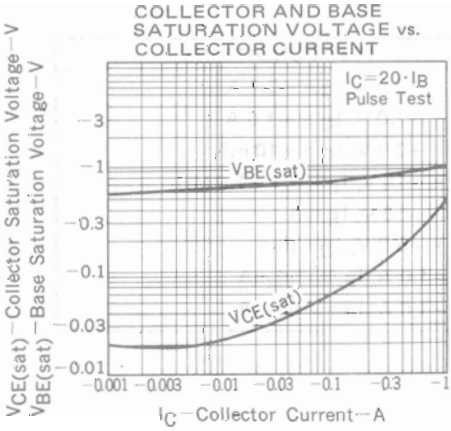
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



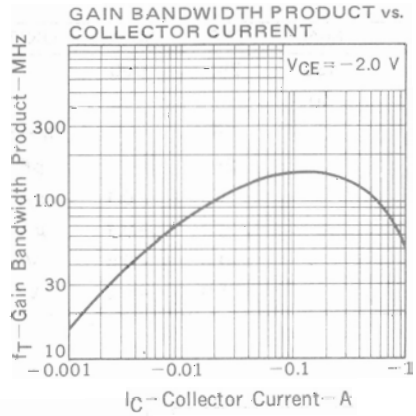
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



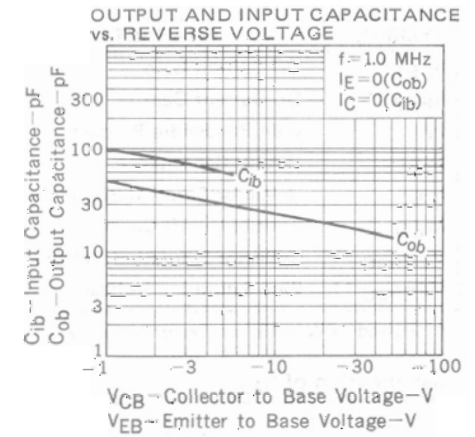
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT AND INPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

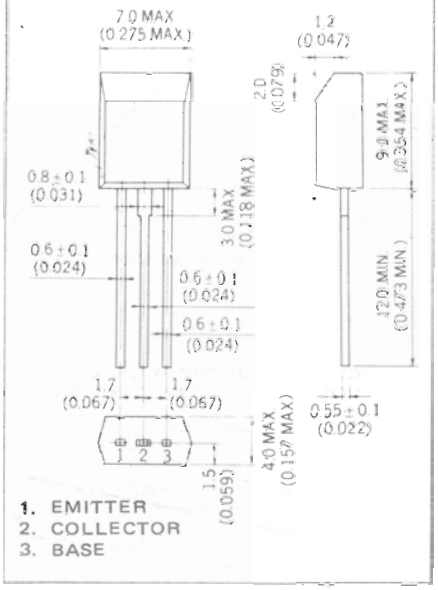
PNP SILICON TRANSISTOR
2SB733

DESCRIPTION The 2SB733 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation P_T : 1.0 W (Ta=25 °C)
- High D.C. Current Gain h_{FE} : 300 TYP. (I_C=−100 mA)
- Low Collector Saturation Voltage
  $V_{CE(sat)}$: −0.27 V TYP. (I_C=−1.0 A)
- Complementary to the NEC 2SD773 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −20 V
- V_{CEO} Collector to Emitter Voltage . . . . . −16 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current . . . . . −1.0 A

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135	300	600	–	V_{CE}=−2.0 V, I_C=−100 mA
h_{FE2}	DC Current Gain	100			–	V_{CE}=−1.0 V, I_C=−1.0 A
f_T	Gain Bandwidth Product	50			MHz	V_{CE}=−2.0 V, I_E=10 mA
C_{ob}	Output Capacitance		27	60	pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB}=−16 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB}=−6.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55	−0.60	−0.65	V	V_{CE}=−6.0 V, I_C=−5.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.27	−0.40	V	I_C=−1.0 A, I_B=−50 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.94	−1.20	V	I_C=−1.0 A, I_B=−50 mA

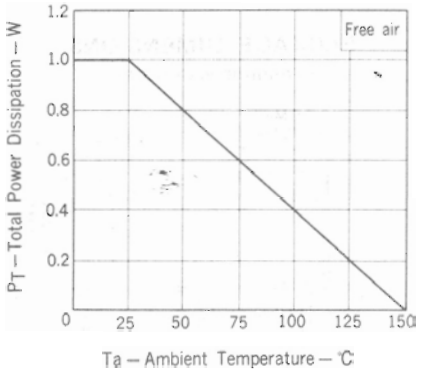
Classification of h_{FE1}

Rank	L_2	K_3	K_4	U_4	U_5
Range	135 – 270	200 – 320	250 – 400	300 – 480	360 – 600

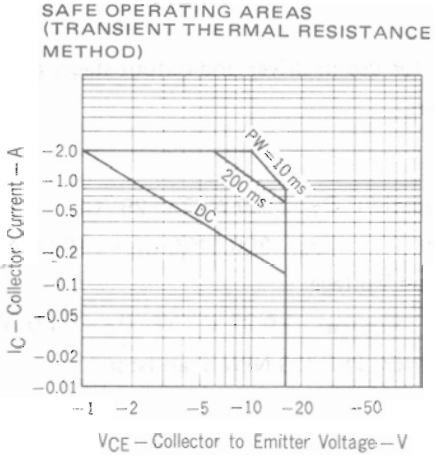
Test Conditions : V_{CE}=−2.0 V, I_C=−100 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

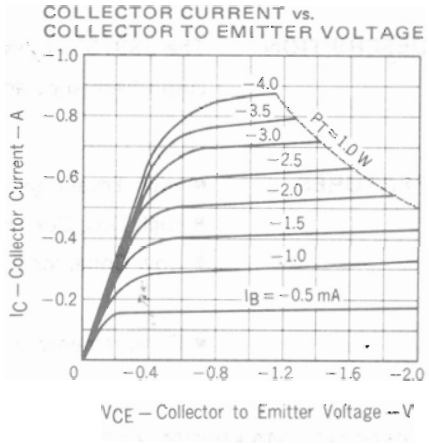
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



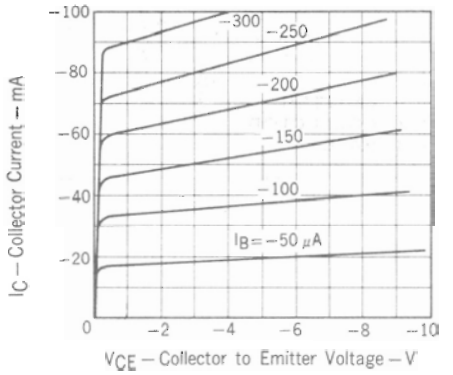
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



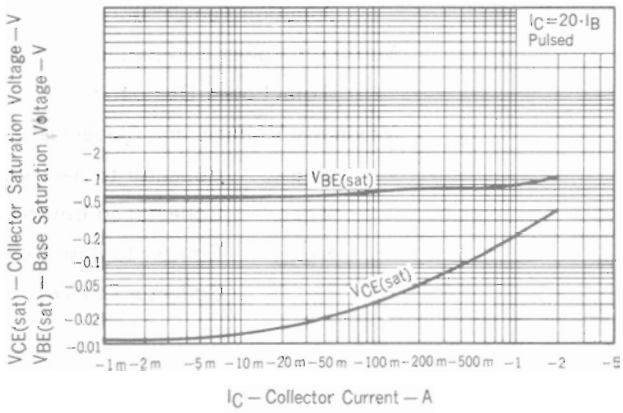
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



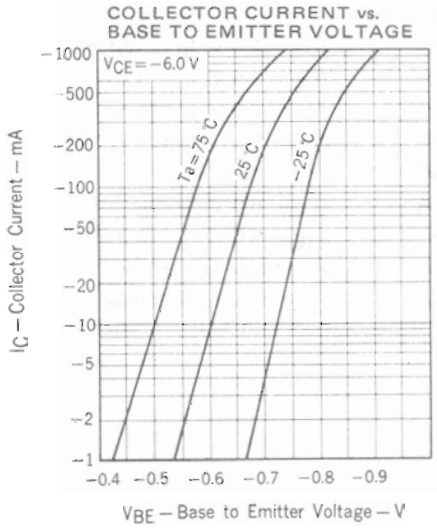
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



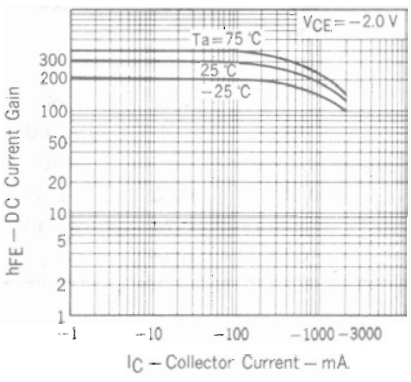
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



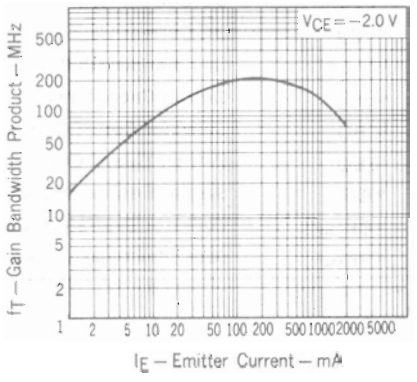
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



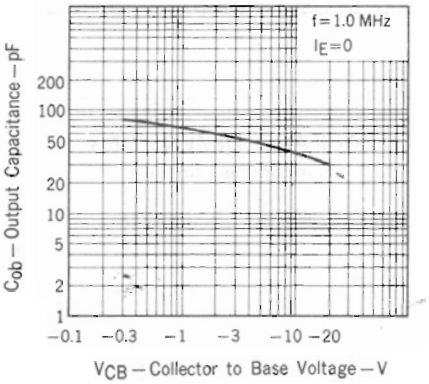
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

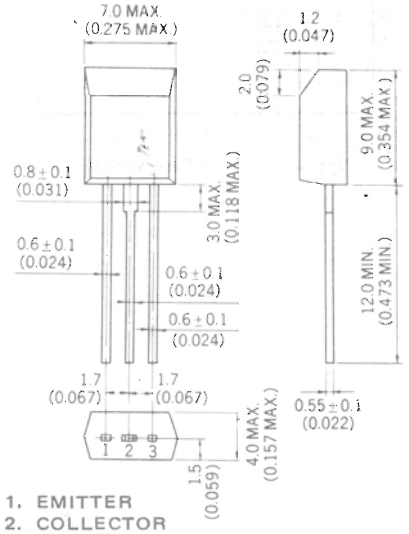
PNP SILICON TRANSISTOR
2SB734

DESCRIPTION The 2SB734 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation P_T : 1.0 W (Ta=25 °C)
- High Voltage V_{CEO} : −50 V MIN.
- Complementary to the NEC 2SD774 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current . . . . . −1.0 A

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135	250	600	—	V_{CE}=−2.0 V, I_C=−100 mA
h_{FE2}	DC Current Gain	40			—	V_{CE}=−1.0 V, I_C=−1.0 A
f_T	Gain Bandwidth Product	50	80		MHz	V_{CE}=−2.0 V, I_E=10 mA
C_{ob}	Output Capacitance		23	50	pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB}=−50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB}=−6.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55	−0.60	−0.65	V	V_{CE}=−6.0 V, I_C=−50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.35	−0.60	V	I_C=−1.0 A, I_B=−50 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.94	−1.20	V	I_C=−1.0 A, I_B=−50 mA

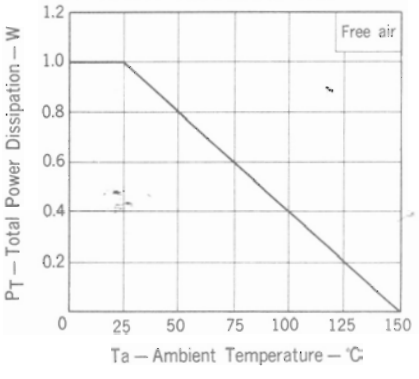
Classification of h_{FE1}

Rank	L_2	K_3	K_4	U_4	U_5
Range	135 – 270	200 – 320	250 – 400	300 – 480	360 – 600

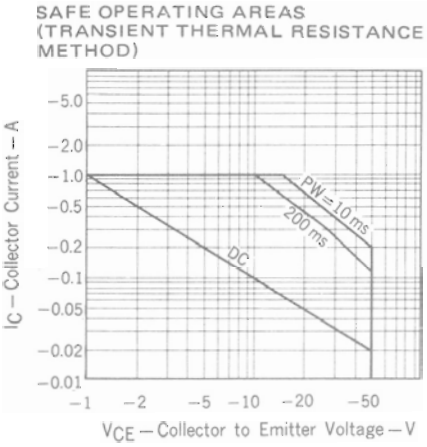
Test Conditions : V_{CE}=−2.0 V, I_C=−100 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

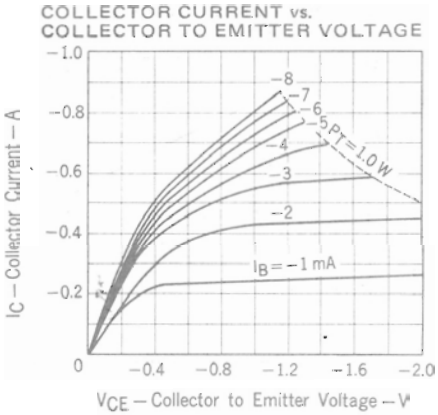
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



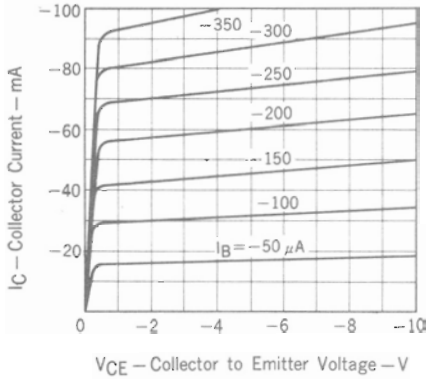
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



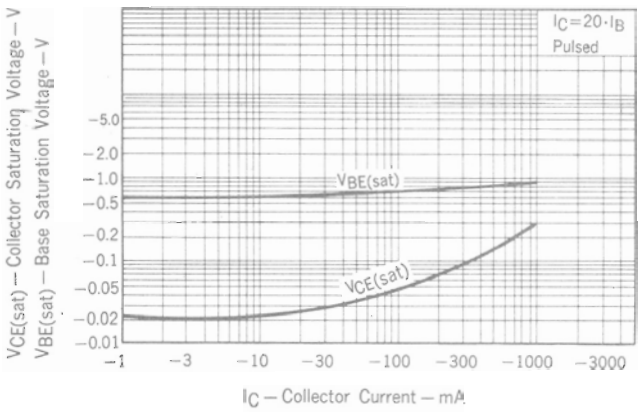
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



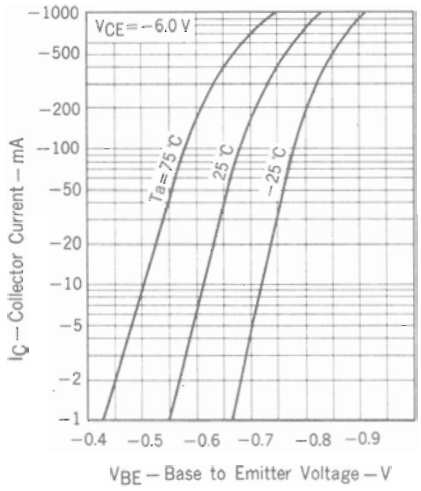
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



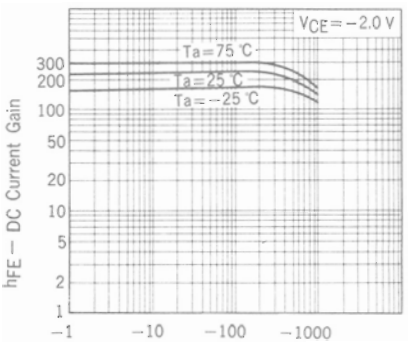
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



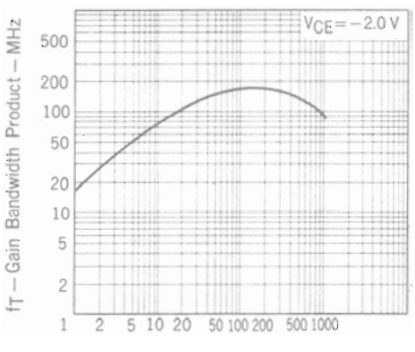
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



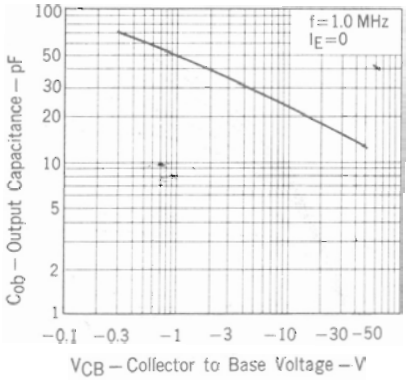
DC CURRENT GAIN vs. COLLECTOR CURRNET



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

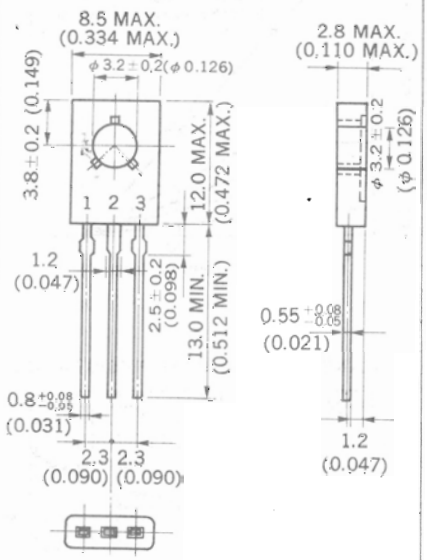
NPN SILICON POWER TRANSISTORS
2SB744,2SB744A

DESCRIPTION The 2SB744, 2SB744A are PNP general purpose transistors designed for use in audio and radio frequency power amplifiers.

FEATURE

- Complementary to the NEC 2SD794, 2SD794A.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SB744	2SB744A	
V_{CBO}	Collector to Base Voltage	−70	−70	V
V_{CEO}	Collector to Emitter Voltage	−45	−60	V
V_{EBO}	Emitter to Base Voltage	−5.0	−5.0	A
$I_{C(DC)}$	Collector Current (DC)	−3.0	−3.0	A
$I_{C(pulse)}$	Collector Current (pulse)	−5.0	−5.0	A

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	30	120			V_{CE} = −5.0 V, I_C = −20 mA*
h_{FE2}	DC Current Gain	60	100	320		V_{CE} = −5.0 V, I_C = −0.5 A*
f_T	Gain Bandwidth Product		45		MHz	V_{CE} = −5.0 V, I_C = −0.1 A
C_{ob}	Output Capacitance		60		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB} = −45 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB} = −3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		−0.5	−2.0	V	I_C = −1.5 A, I_B = −0.15 A
$V_{BE(sat)}$	Base Saturation Voltage		−0.8	−2.0	V	I_C = −1.5 A, I_B = −0.15 A

*Pulse Test PW ≦ 350 μs, Duty Cycle ≦ 2 %

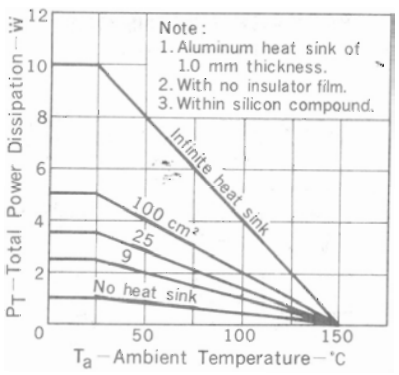
Classification of h_{FE2}

Rank	R	Q	P
Range	60 to 120	100 to 200	160 to 320

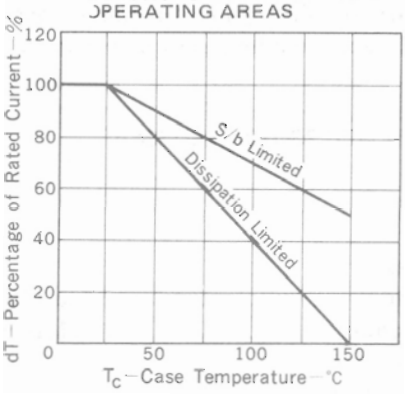
Test Conditions : V_{CE} = −5.0 V, I_C = −0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

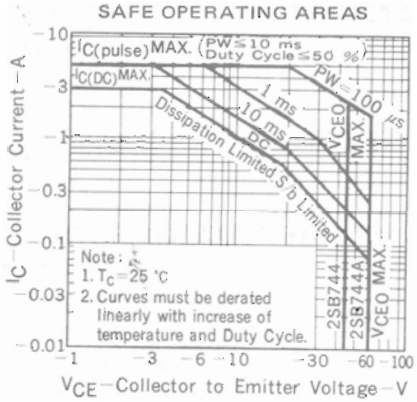
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



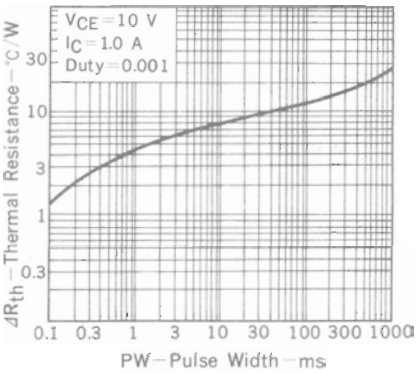
DERATING CURVE OF SAFE OPERATING AREAS



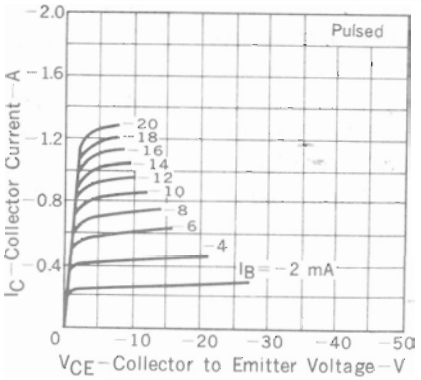
SAFE OPERATING AREAS



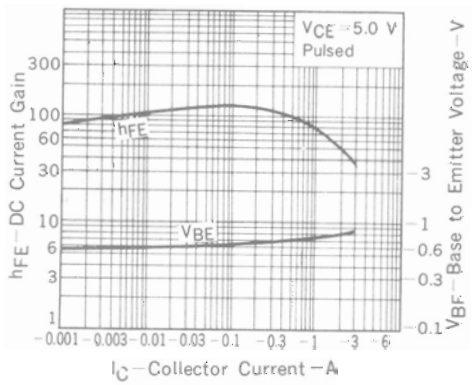
TRANSIENT THERMAL RESISTANCE



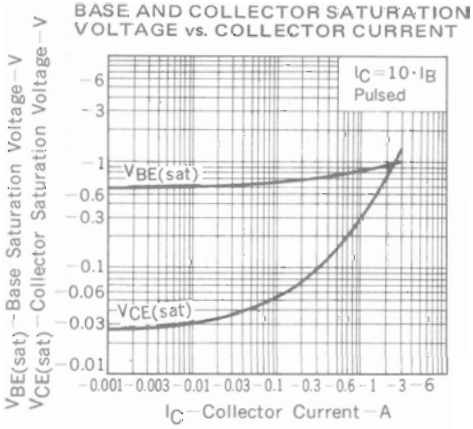
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



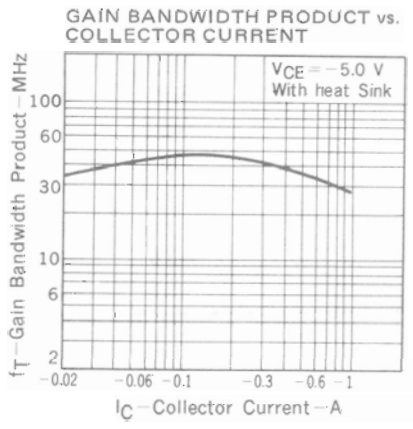
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



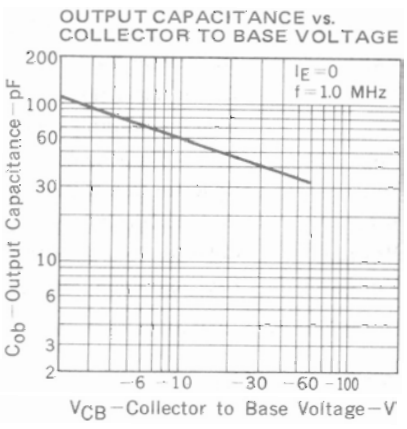
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

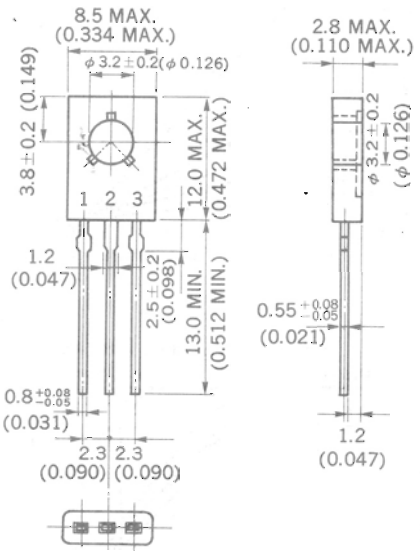
PNP SILICON POWER TRANSISTOR
2SB772

DESCRIPTION The 2SB772 is PNP silicon transistor suited for the output stage of 3 watts audio amplifier, voltage regulator, DC-DC converter and relay driver.

FEATURES

- Low saturation voltage.
  $V_{CE(sat)} \leqq -0.5$ V (@ $I_C = -2$ A, $I_B = -0.2$ A)
- Excellent h_{FE} linearity and high h_{FE}.
  h_{FE} : 60 to 400 (@ $V_{CE} = -2$ V, $I_C = -1$ A)
- Less cramping space required due to small and thin package and reducing the trouble for attachment to a radiator.
  No insulator bushing required.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−40	V
V_{CEO}	Collector to Emitter Voltage	−30	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
$I_{C(DC)}$	Collector Current (DC)	−3.0	A
$I_{C(pulse)}$*	Collector Current (pulse)	−7.0	A

*Pulse Test PW ≦ 350 μs, Duty Cycle ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	30	220			$V_{CE} = -2.0$ V, $I_C = -20$ mA**
h_{FE2}	DC Current Gain	60	160	400		$V_{CE} = -2.0$ V, $I_C = -1.0$ A**
f_T	Gain Bandwidth Product		80		MHz	$V_{CE} = -5.0$ V, $I_C = -0.1$ A
C_{ob}	Output Capacitance		55		pF	$V_{CB} = -10$ V, $I_E = 0$, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−1.0	μA	$V_{CB} = -30$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			−1.0	μA	$V_{EB} = -3.0$ V, $I_C = 0$
$V_{CE(sat)}$	Collector Saturation Voltage		−0.3	−0.5	V	$I_C = -2.0$ A, $I_B = -0.2$ A**
$V_{BE(sat)}$	Base Saturation Voltage		−1.0	−2.0	V	$I_C = -2.0$ A, $I_B = -0.2$ A**

**Pulse Test : PW ≦ 350 μs, Duty Cycle ≦ 2 %

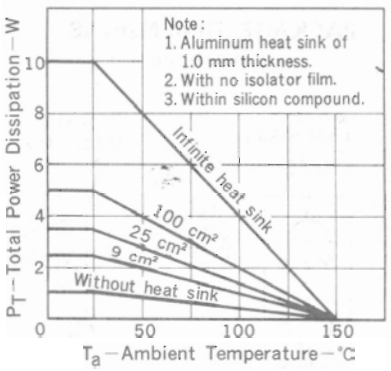
Classification of h_{FE}

Rank	R	Q	P	E
Range	60 to 120	100 to 200	160 to 320	200 to 400

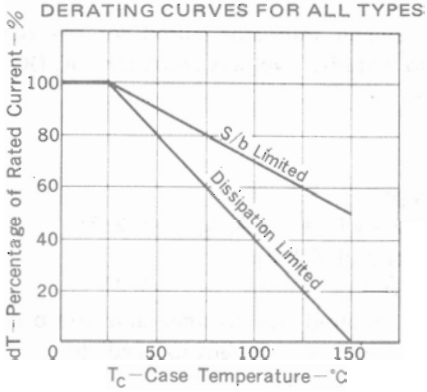
Test Conditions : $V_{CE} = -2.0$ V, $I_C = -1.0$ A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

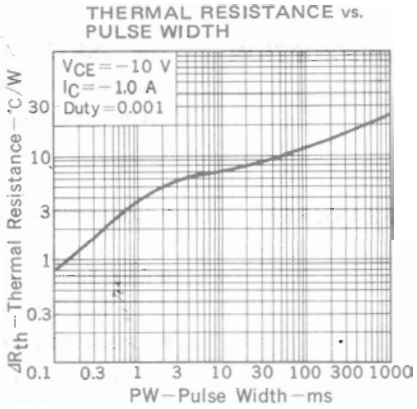
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



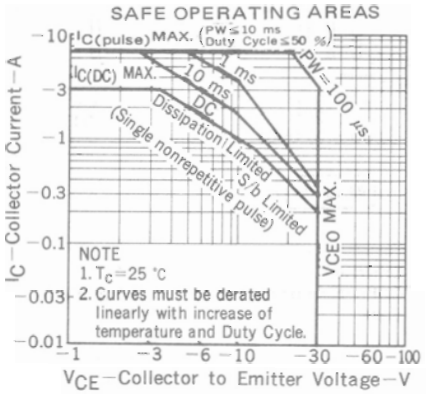
DERATING CURVES FOR ALL TYPES



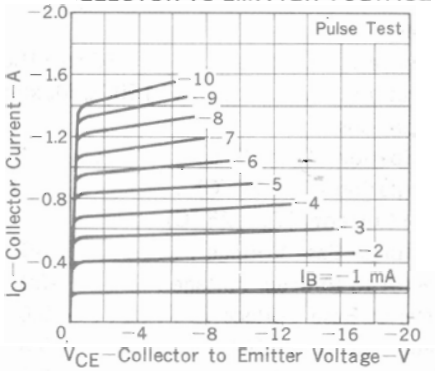
THERMAL RESISTANCE vs. PULSE WIDTH



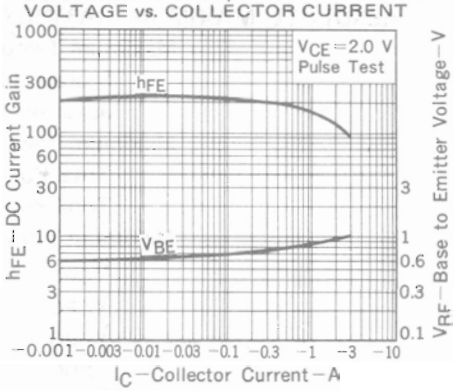
SAFE OPERATING AREAS



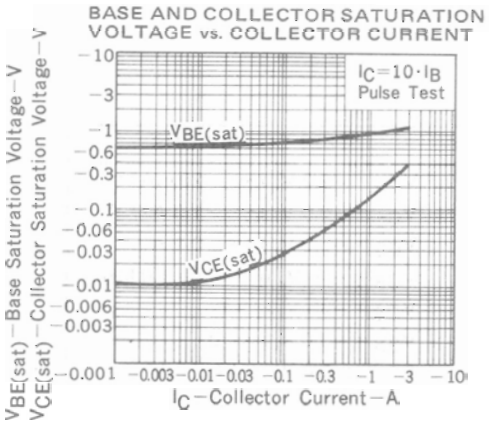
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



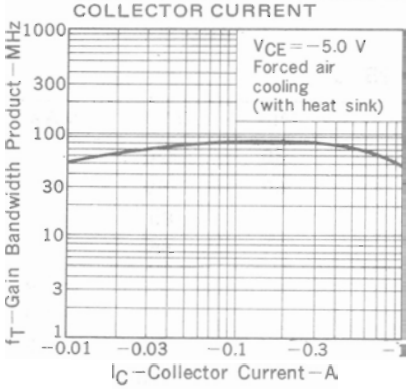
DC CURRENT GAIN, BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



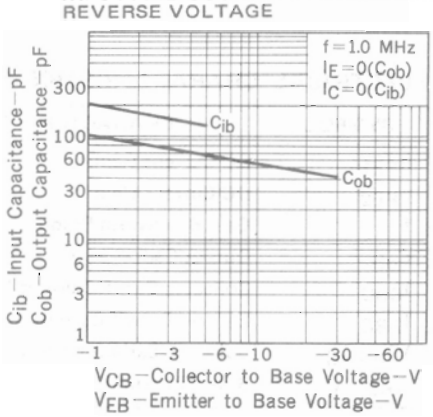
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

PNP SILICON DARLINGTON POWER TRANSISTORS
2SB794,2SB795

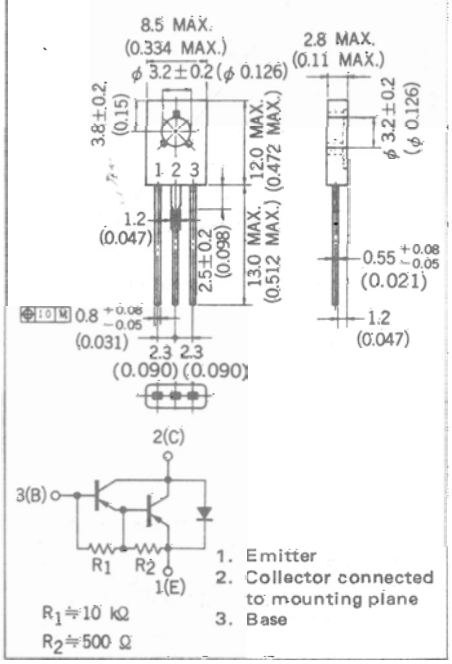
DESCRIPTION

The 2SB794, 2SB795 are darlington transistors built-in dumper diodes at C-E.
They are suitable for use operating from IC without predriver, such as hammer driver.

FEATURES

- High DC Current Gain.
- Low Collector Saturation Voltage.
- Built-in a dumper diode at C-E.
- Complementary to the NEC 2SD985, 2SD986 NPN Transistors.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations
- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SB794	2SB795	
V_{CBO}	Collector to Base Voltage. . . .	−60	−80	V
V_{CEO}	Collector to Emitter Voltage. .	−60	−80	V
V_{EBO}	Emitter to Base Voltage.	−8.0		V
$I_{C(DC)}$	Collector Current.	∓1.5		A
$I_{C(pulse)}$ *	Collector Current.	∓3.0		A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	1000			—	V_{CE} = −2.0 V, I_C = −0.5 A
h_{FE2}	DC Current Gain	2000		30000	—	V_{CE} = −2.0 V, I_C = −1.0 A
t_{on}	Turn On Time		0.5		μs	I_C = −1.0 A, R_L = 50 Ω
t_{stg}	Storage Time		1.0		μs	I_{B1} = −I_{B2} = −1.0 mA, V_{CC} = −50 V
t_f	Fall Time		1.0		μs	See Test Circuit.
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB} = −60/−80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	mA	V_{EB} = −5.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			−1.5	V	I_C = −1.0 A, I_B = −1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage			−2.0	V	I_C = −1.0 A, I_B = −1.0 mA

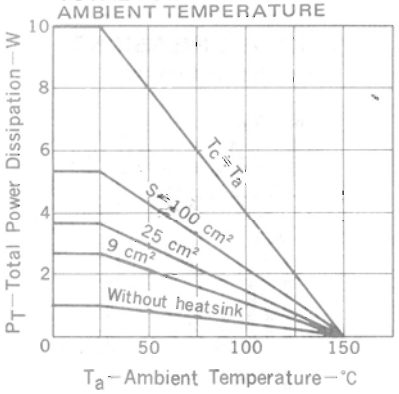
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 30000

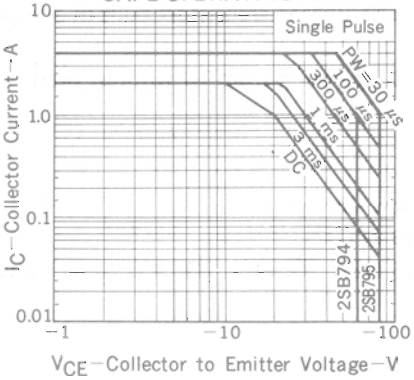
Test Conditions: V_{CE} = −2.0 V, I_C = −1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

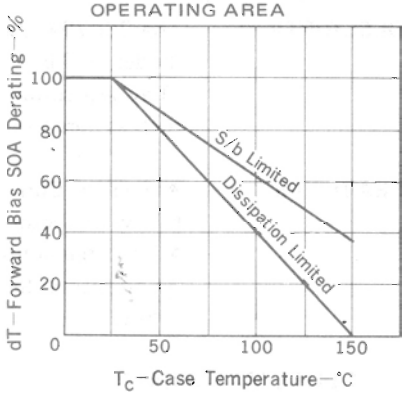
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



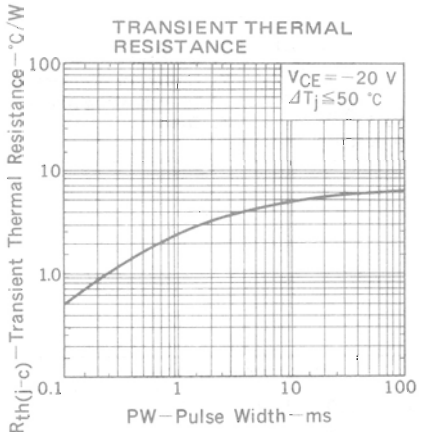
SAFE OPERATING AREA



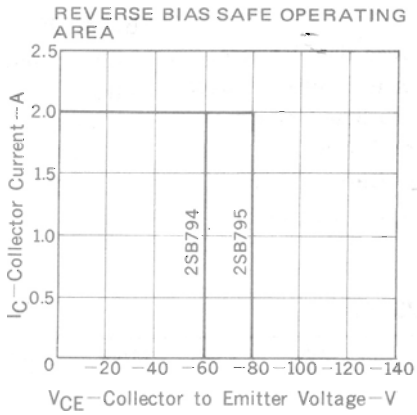
DERATING CURVE OF SAFE OPERATING AREA



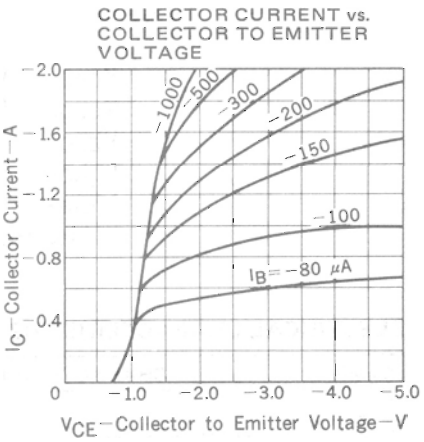
TRANSIENT THERMAL RESISTANCE



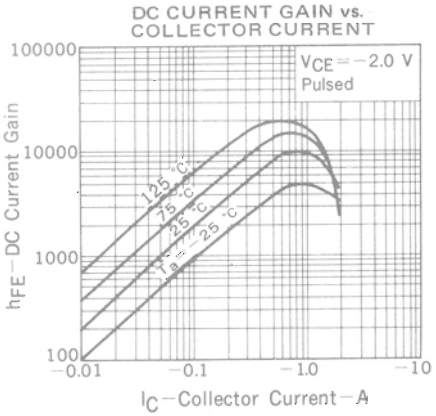
REVERSE BIAS SAFE OPERATING AREA



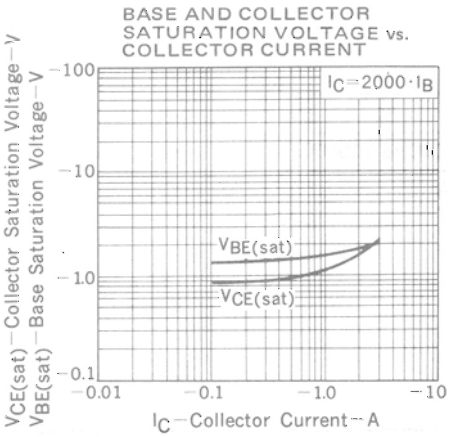
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



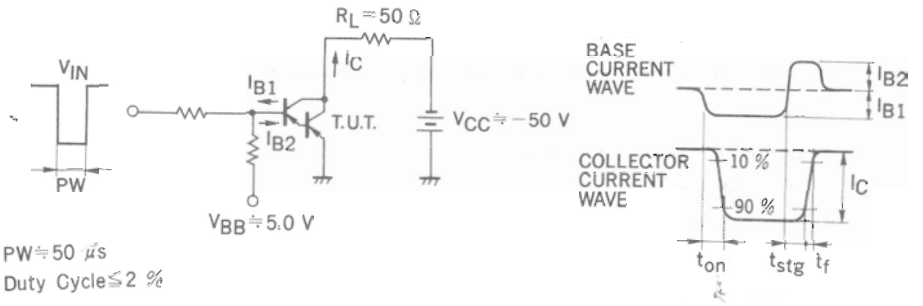
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



PW ≒ 50 μs
Duty Cycle ≦ 2 %

NEC
ELECTRON DEVICE

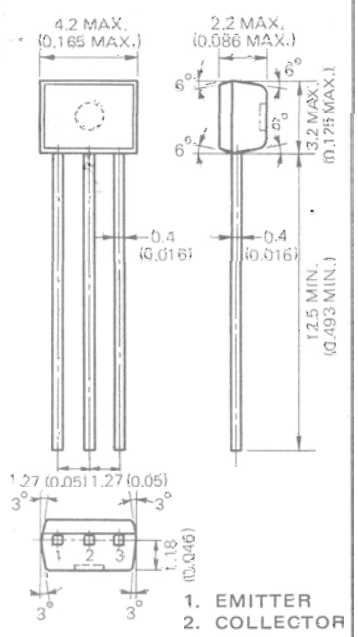
PNP SILICON TRANSISTOR
2SB810

DESCRIPTION The 2SB810 is designed for use in output stage of portable radio and cassette type tape recorder, general purpose applications.

FEATURES

- High total power dissipation.
  P_T = 350 mW
- High h_{FE} and low $V_{CE(sat)}$.
  h_{FE} (I_C=−100 mA) : 200 TYP.
  $V_{CE(sat)}$ (−700 mA) : −0.25 V TYP.
- Complementary to the NEC 2SD1020 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 350 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −30 V
- V_{CEO} Collector to Emitter Voltage . . . . . −25 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −700 mA
- I_B Base Current. . . . . −150 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	110	200	400	—	V_{CE}=−1.0 V, I_C=−100 mA
h_{FE2}*	DC Current Gain	50	100		—	V_{CE}=−1.0 V, I_C=−700 mA
C_{ob}	Collector to Base Capacitance		17	40	pF	V_{CB}=−6.0 V, I_E=0, f=1.0 MHz
f_T	Gain Bandwidth Product	50	160		MHz	V_{CE}=−6.0 V, I_E=−10 mA
V_{BE}*	Base to Emitter Voltage	−600	−640	−700	mV	V_{CE}=−6.0 V, I_C=−10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.25	−0.4	V	I_C=−700 mA, I_B=−70 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.95	−1.2	V	I_C=−700 mA, I_B=−70 mA
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB}=−30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB}=−5.0 V, I_C=0

* Pulsed PW ≤ 350 μs, duty cycle ≤ 2.0 %

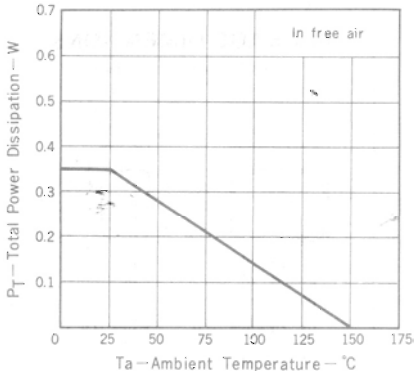
Classification of h_{FE1}

Rank	M	J	H	F	E
Range	110 – 180	135 – 220	170 – 270	200 – 320	250 – 400

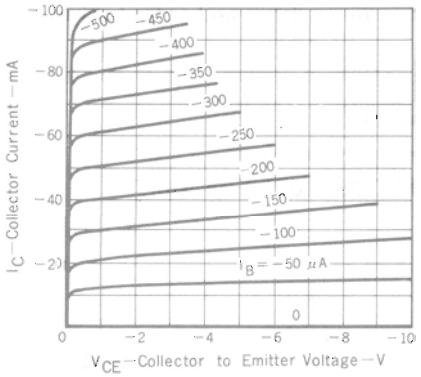
h_{FE1} Test Conditions : V_{CE} = −1.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

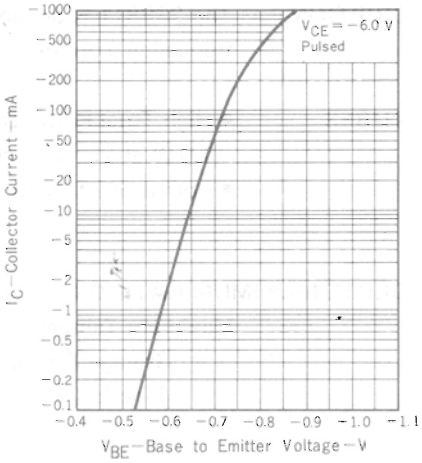
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



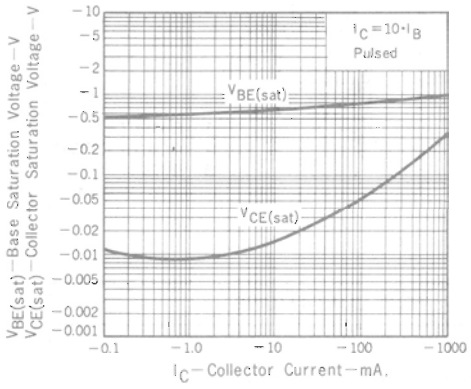
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



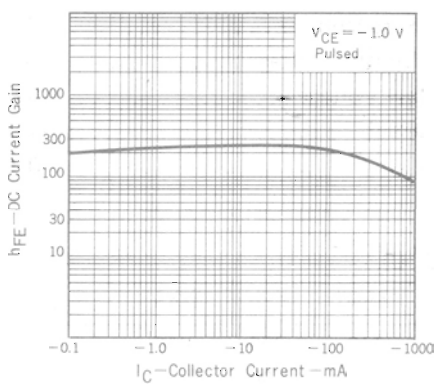
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



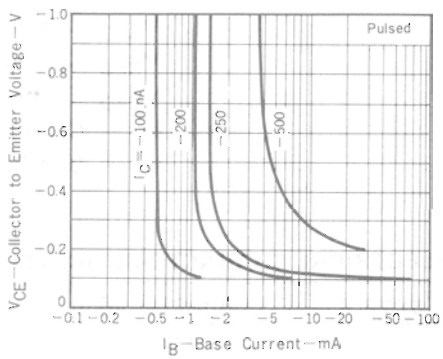
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



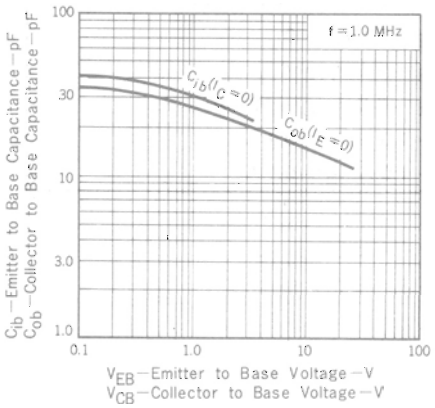
DC CURRENT GAIN vs. COLLECTOR CURRENT



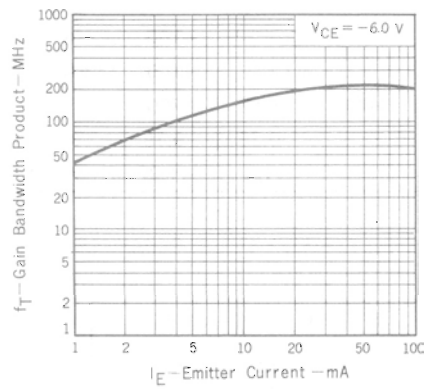
COLLECTOR TO EMITTER VOLTAGE vs. BASE CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



NEC
ELECTRON DEVICE

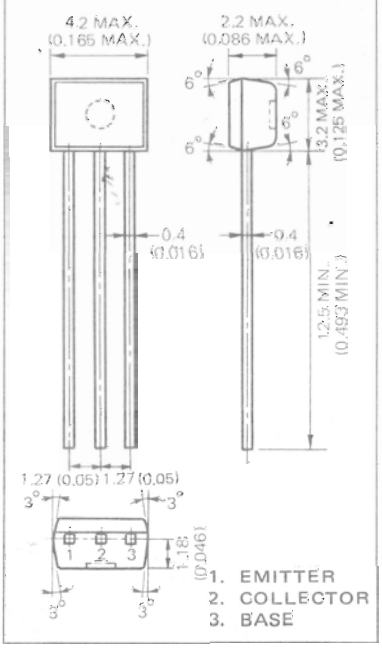
PNP SILICON TRANSISTOR
2SB811

DESCRIPTION The 2SB811 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation:
  1.0 W at 25 °C Ambient Temperature.
- Complementary to the NEC 2SD1021 Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 350 mW
- Thermal Resistance (Junction to Ambient) ..... 429 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... −30 V
- V_{CEO} Collector to Emitter Voltage ..... −25 V
- V_{EBO} Emitter to Base Voltage ..... −5.0 V
- I_C Collector Current ..... −1.0 A
- I_B Base Current ..... −0.1 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	110	200	400	–	V_{CE}=−1.0 V, I_C=−0.1 A
h_{FE2}	DC Current Gain	50	100		–	V_{CE}=−1.0 V, I_C=−1.0 A
f_T	Gain Bandwidth Product		110		MHz	V_{CE}=−6.0 V, I_E=−10 mA
C_{ob}	Collector to Base Capacitance		36		pF	V_{CB}=−6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB}=−30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB}=−5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−600	−640	−700	mV	V_{CE}=−6.0 V, I_C=−10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.25	−0.35	V	I_C=−1.0 A, I_B=−0.1 A
$V_{BE(sat)}$	Base Saturation Voltage		−1.0	−1.2	V	I_C=−1.0 A, I_B=−0.1 A

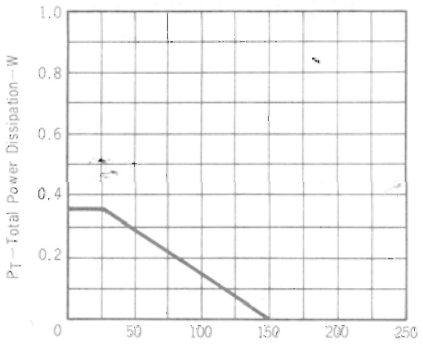
Classification of h_{FE1}

Rank	M	J	H	F	E
Range	110 – 180	135 – 220	170 – 270	200 – 320	250 – 400

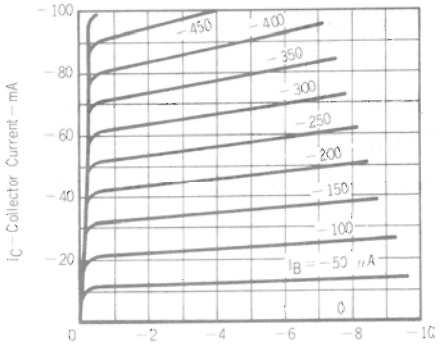
h_{FE1} Test Conditions: V_{CE}=−1.0 V, I_C=−0.1 A

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

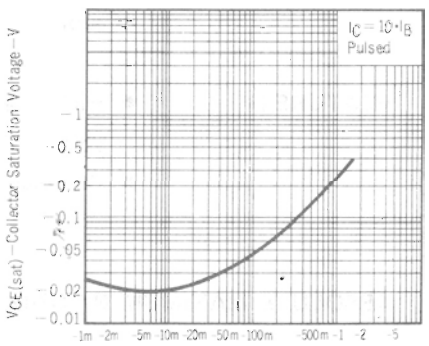
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



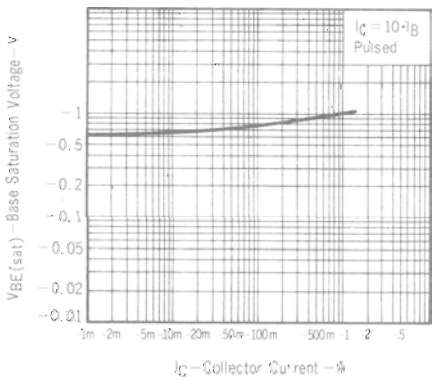
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



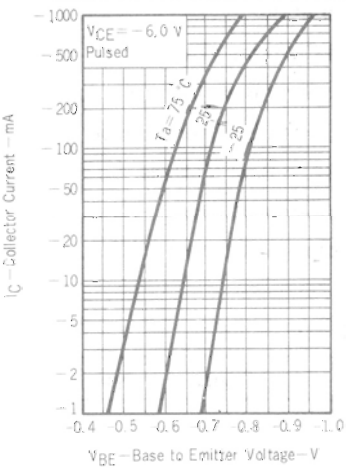
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



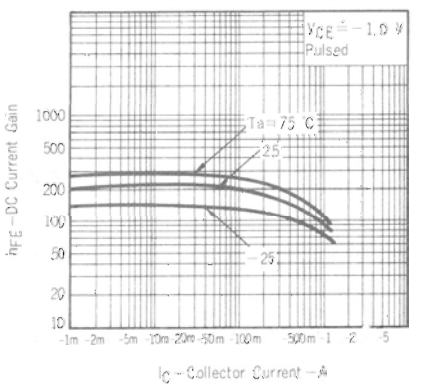
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



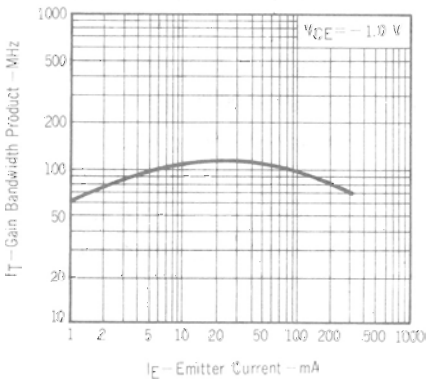
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



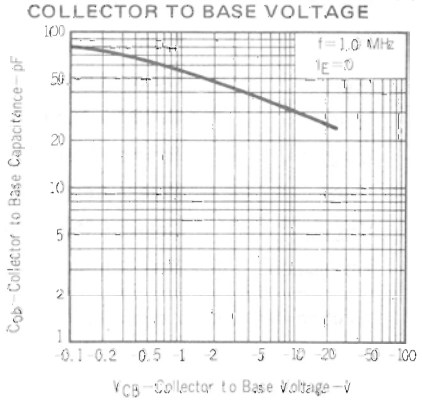
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



COLLECTOR TO BASE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

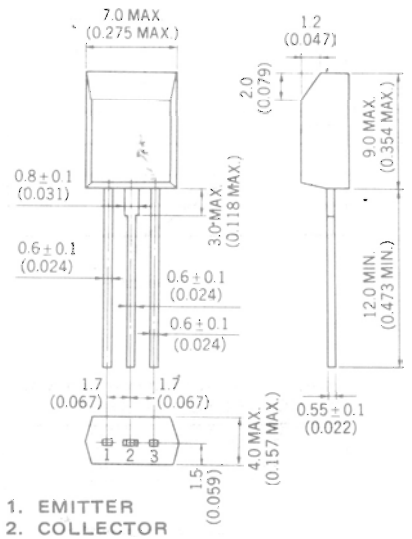
PNP SILICON TRANSISTOR
2SB984

DESCRIPTION The 2SB984 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High total power dissipation and high break-down voltage : P_T = 1.0 W (T_a = 25 °C), V_{CEO} = −80 V
- Complementary to the NEC 2SC1312 NPN transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −120 V
- V_{CEO} Collector to Emitter Voltage . . . . −80 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- $I_{C\ (DC)}$ DC Collector Current . . . . . −1.0 A
- $I_{C\ (pulse)}$ AC Collector Current . . . . . −2.0 A

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	135		400		V_{CE} = −1.0 V, I_C = −200 mA
h_{FE2}*	DC Current Gain	40				V_{CE} = −1.0 V, I_C = −500 mA
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = −6.0 V, I_E = 200 mA
C_{ob}	Output Capacitance		20	50	pF	V_{CB} = −10 V, I_E = 0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −5.0 V, I_C = 0
V_{BE}*	Base to Emitter Voltage	−550	−600	−650	mV	V_{CE} = −6.0 V, I_C = −10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.5	−1.0	V	I_C = −1.0 A, I_B = −100 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−1.0	−1.2	V	I_C = −1.0 A, I_B = −100 mA

* Pulsed PW≦300 μs, duty cycle≦2 %

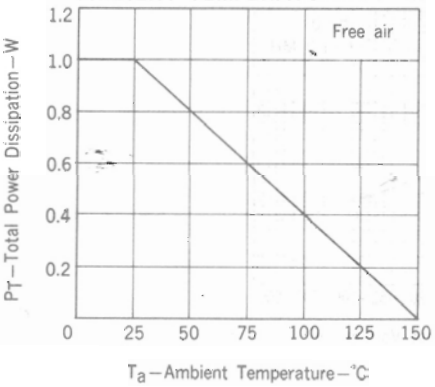
Classified of h_{FE1}

Rank	L	K
Range	135 – 270	200 – 400

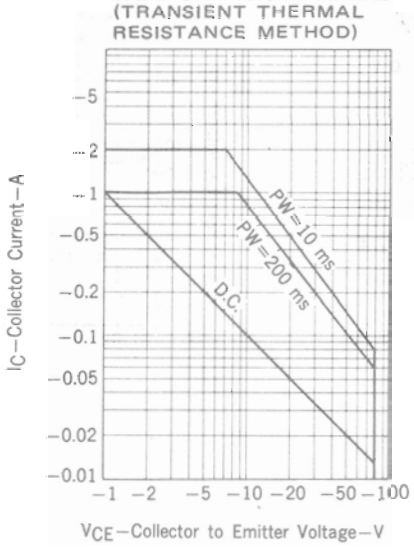
Test Conditions: V_{CE} = −1.0 V, I_C = −200 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

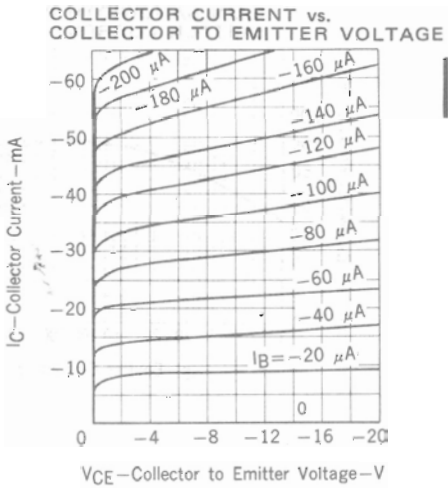
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



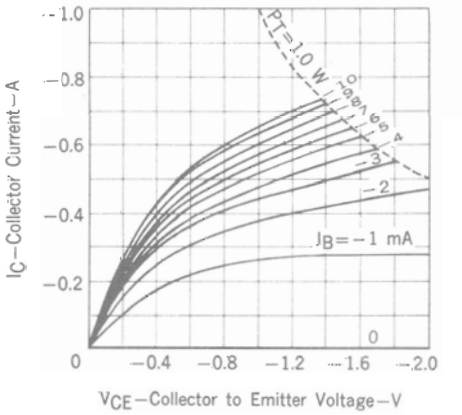
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



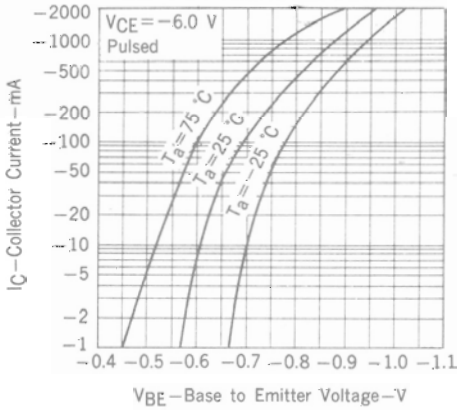
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



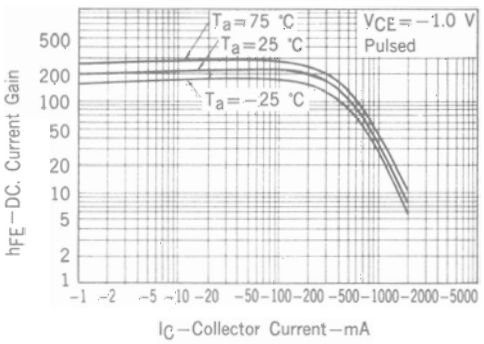
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



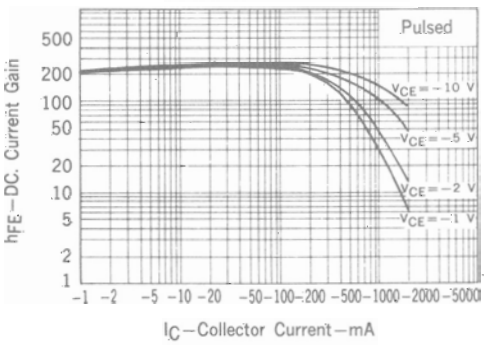
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



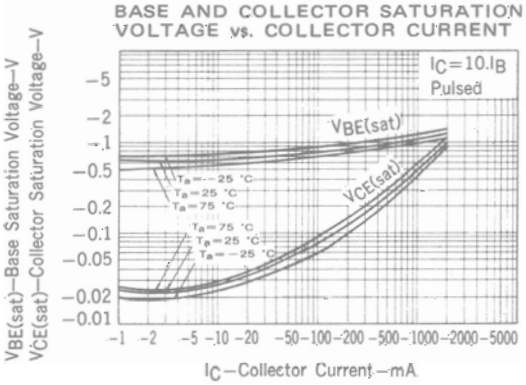
DC CURRENT GAIN vs. COLLECTOR CURRENT



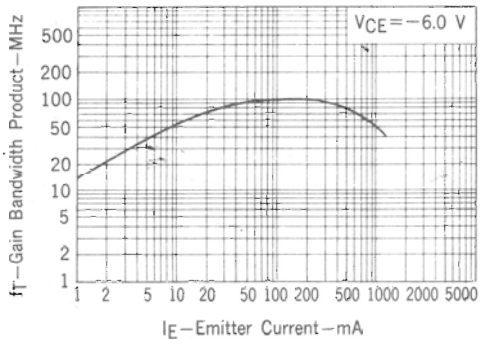
DC CURRENT GAIN vs. COLLECTOR CURRENT



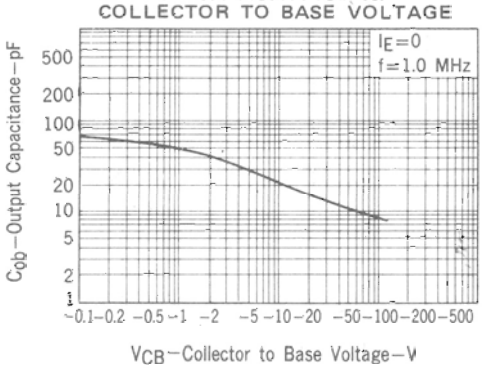
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs.
EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



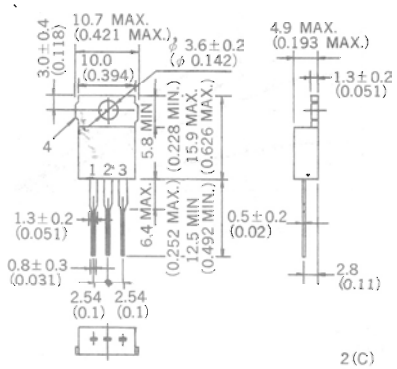
NEC
ELECTRON DEVICE

PNP SILICON DARLINGTON POWER TRANSISTOR
2SB1061

DESCRIPTION The 2SB1061 is PNP silicon epitaxial darlington transistor designed for pulse motor driver and relay driver application.

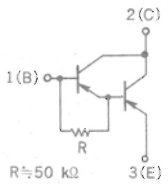
FEATURES
- Operates from IC without Predriver.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 15 W

Maximum Voltage and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−300	V
V_{CEO}	Collector to Emitter Voltage	−300	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current (DC)	−300	mA
$I_{C(pulse)}$	Collector Current (pulse)*	−600	mA
$I_{B(DC)}$	Base Current (DC)	−30	mA

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

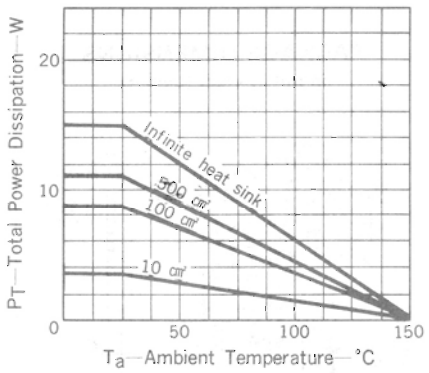
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{EF1}	DC Current Gain**	1000			–	V_{CE} = −1.5 V, I_C = −20 mA
h_{FE2}	DC Current Gain**	1500	6000	30000	–	V_{CE} = −1.5 V, I_C = −100 mA
$V_{CE(sat)}$	Collector Saturation Voltage**		−0.8	−1.5	V	I_C = −100 mA, I_B = −0.2 mA
$V_{BE(sat)}$	Base Saturation Voltage**		−1.4	−2.0	V	I_C = −100 mA, I_B = −0.2 mA
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −300 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{BE} = −60 V, I_C = 0
f_T	Gain Bandwidth Product		15		MHz	V_{CE} = −1.5 V, I_C = −20 mA
C_{ob}	Output Capacitance		50		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz

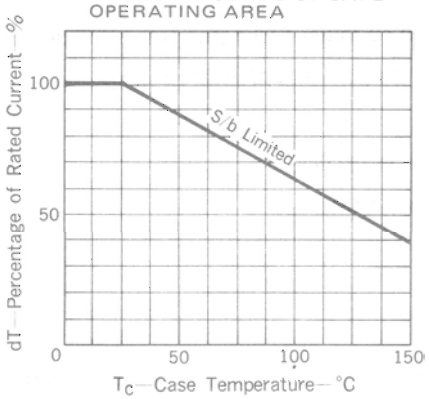
**Pulse Test: PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

TYPICAL CHARACTERISTICS (T_a = 25 °C)

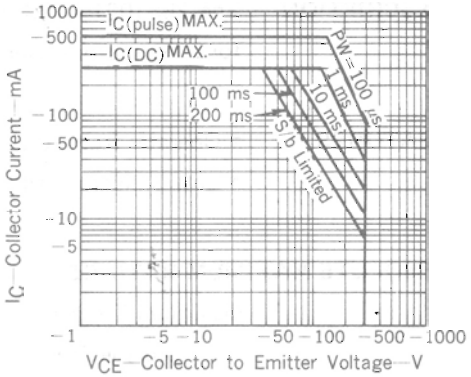
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



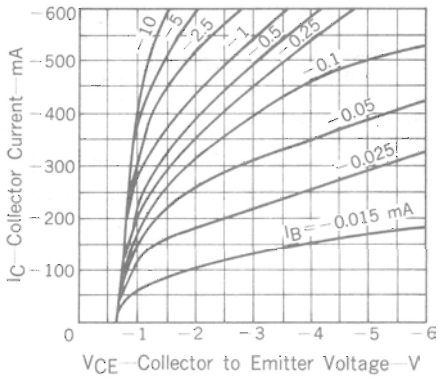
DERATING CURVE OF SAFE OPERATING AREA



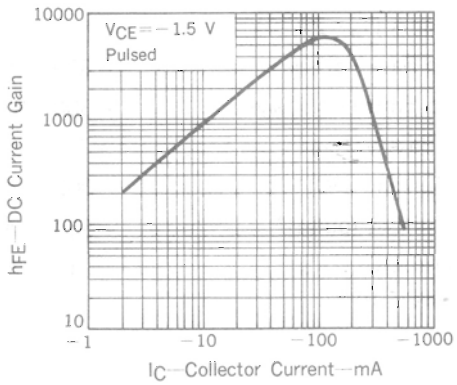
FORWARD BIAS SAFE OPERATING AREA



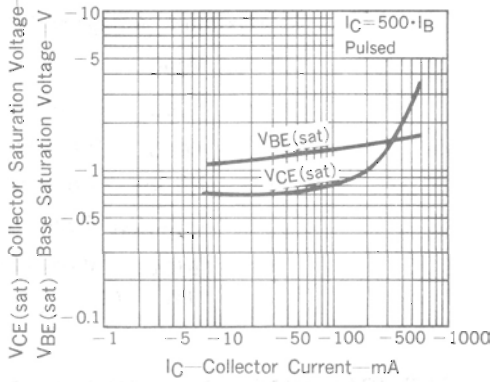
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



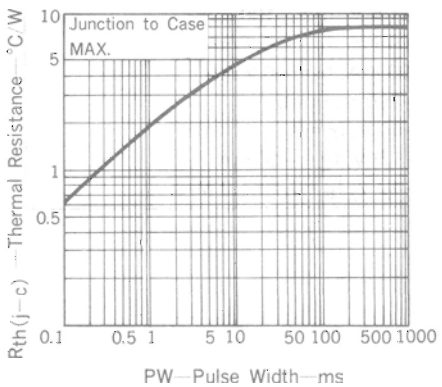
DC CURRENT GAIN vs. COLLECTOR CURRENT



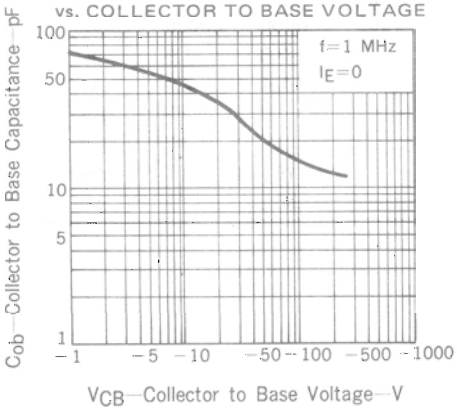
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TRANSIENT THERMAL RESISTANCE



COLLECTOR TO BASE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

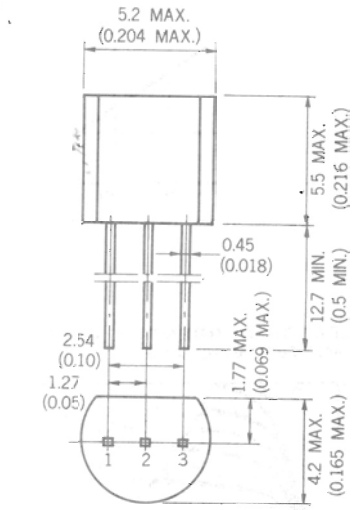
PNP SILICON TRANSISTOR
2SB1068

DESCRIPTION The 2SB1068 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- Low Collector Saturation Voltage
  $V_{CE(sat)}$: −0.25 V TYP. (I_C = −1.0 A, I_B = −10 mA)
- High DC Current Gain
  h_{FE} : 350 TYP. (V_{CE} = −2.0 V, I_C = −100 mA)
- High Total Power Dissipation P_T : 0.75 W (T_a = 25 °C)
- Complementary to The NEC 2SD1513 NPN Transistor

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −20 V
- V_{CEO} Collector to Emitter Voltage . . . . . −16 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- $I_{C(DC)}$ Collector Current . . . . . −2.0 A
- $I_{C(pulse)}$* Collector Current . . . . . −3.0 A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135	350	650	—	V_{CE} = −2.0 V, I_C = −100 mA
h_{FE2}	DC Current Gain	100			—	V_{CE} = −2.0 V, I_C = −1.5 A
f_T	Gain Bandwidth Product	100	180		MHz	V_{CE} = −10 V, I_E = 50 mA
C_{ob}	Output Capacitance		60		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −16 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−550	−600	−650	mV	V_{CE} = −6.0 V, I_C = −5.0 mA
$V_{CE(sat)1}$	Collector Saturation Voltage		−0.25	−0.40	V	I_C = −1.0 A, I_B = −10 mA
$V_{CE(sat)2}$	Collector Saturation Voltage		−0.31	−0.50	V	I_C = −1.5 A, I_B = −75 mA
$V_{CE(sat)3}$	Collector Saturation Voltage		−0.33	−0.50	V	I_C = −1.5 A, I_B = −20 mA
$V_{BE(sat)}$	Base Saturation Voltage		−1.05	−1.2	V	I_C = −1.5 A, I_B = −75 mA

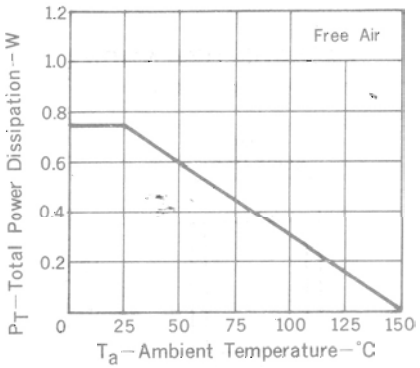
Classification of h_{FE}

Rank	L	K	U
Range	135 − 270	200 − 400	300 − 650

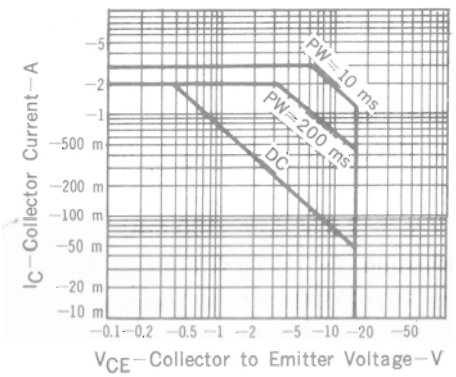
Test Conditions : V_{CE} = −2.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

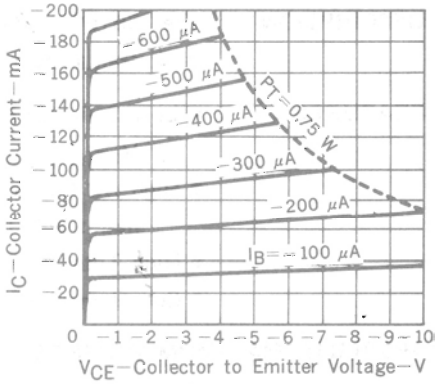
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



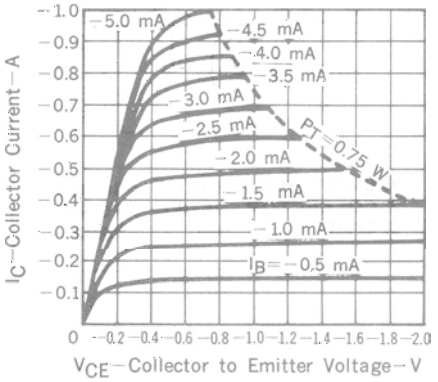
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



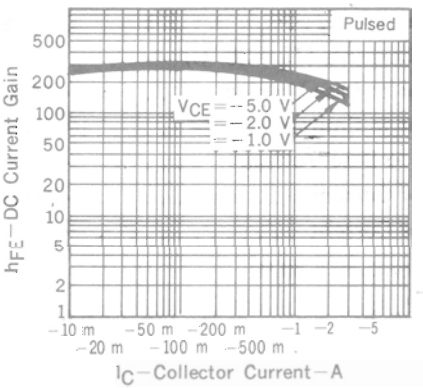
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



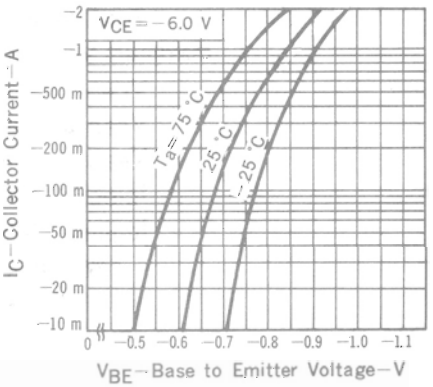
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



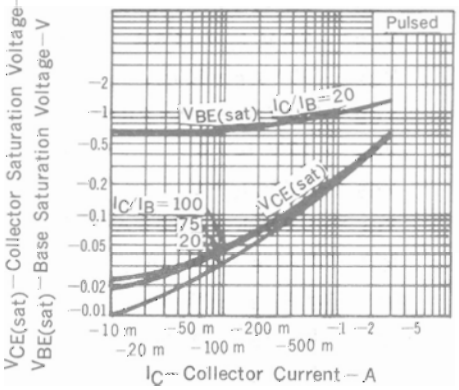
DC CURRENT GAIN vs. COLLECTOR CURRENT



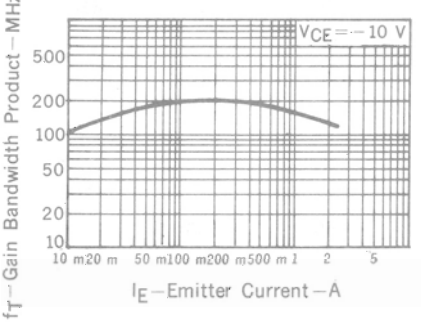
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



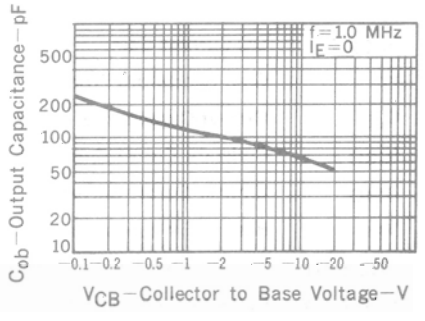
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



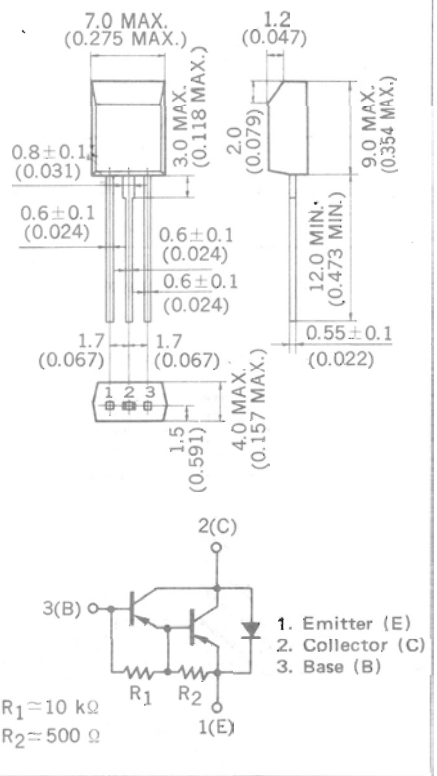
NEC
ELECTRON DEVICE

PNP SILICON DARLINGTON TRANSISTOR
2SB1093

DESCRIPTION The 2SB1093 is a darlington transistor including a dumper diode at C-E.
It is suitable for general driving use, such as hammer, solenoid, lamp or motor.

FEATURES
- High DC current gain.
- High current capability, wide ASO and low collector saturation voltage.
- Includes a dumper diode at C-E.
- A complementary pair with NEC's 2SD1579.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −80 V
- V_{CEO} Collector to Emitter Voltage . . . . . −80 V
- V_{EBO} Emitter to Base Voltage . . . . . −8.0 V
- I_C Collector Current (DC) . . . . . ∓1.5 A
- I_C Collector Current (Pulse)* . . . . . ∓3.0 A
- I_B Base Current (DC) . . . . . −0.15 A

*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	1000			–	V_{CE} = −2.0 V, I_C = −0.5 A
h_{FE2}	DC Current Gain	2000		30000	–	V_{CE} = −2.0 V, I_C = −1.0 A
t_{on}	Turn-On Time		0.5		μs	(I_C = −1.0 A, R_L = 50 Ω, $I_{B1} = -I_{B2}$ = −1.0 mA, V_{CC} = −50 V, See Test Circuit)
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −80 V, I_E = 0
I_{CER}	Collector Cutoff Current			−1.0	mA	V_{CE} = −80 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			−10	μA	V_{CE} = −80 V, $V_{BE(off)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			−1.0	mA	V_{CE} = −80 V, $V_{BE(off)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			−1.0	mA	V_{EB} = −5.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			−1.5	V	I_C = −1.0 A, I_B = −1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage			−2.0	V	
f_T	Gain Bandwidth Product		80		MHz	V_{CE} = −10 V, I_E = 1.0 A

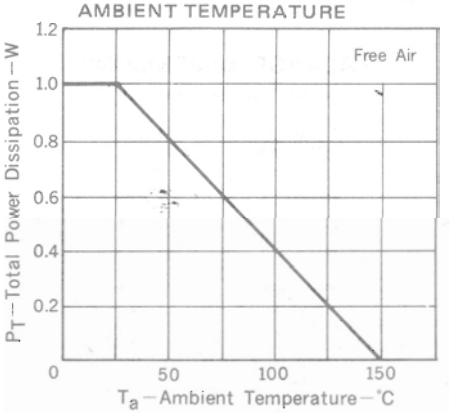
Classification of h_{FE2}

Rank	M	L	K
Range	2000 – 5000	4000 – 10000	8000 – 30000

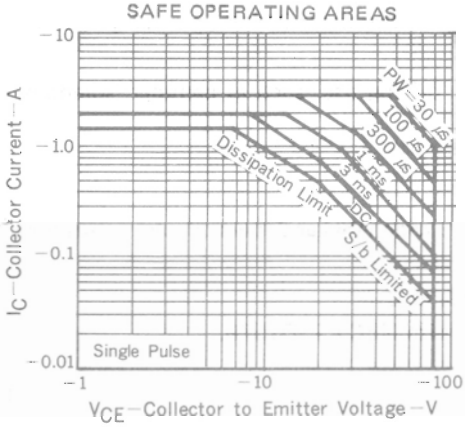
Test Conditions: V_{CE} = −2.0 V, I_C = −1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

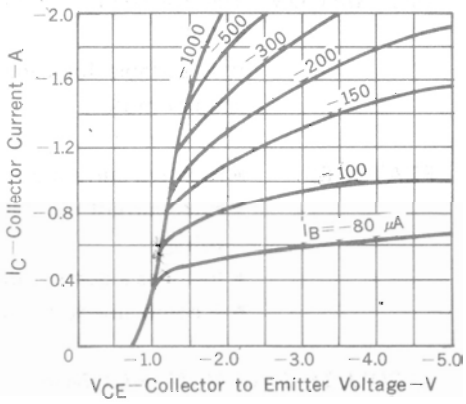
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



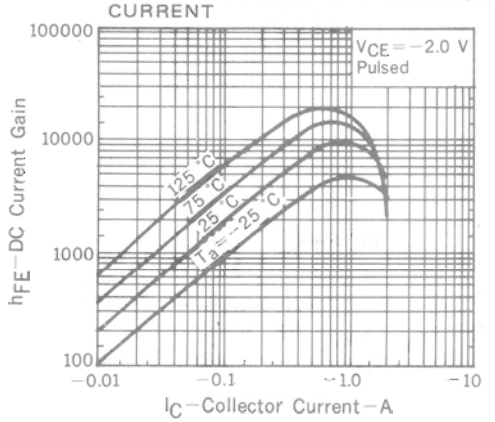
SAFE OPERATING AREAS



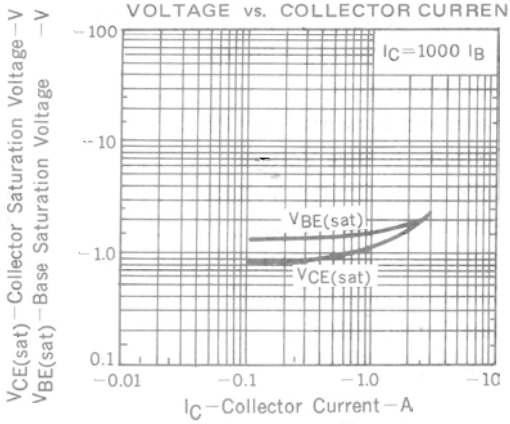
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



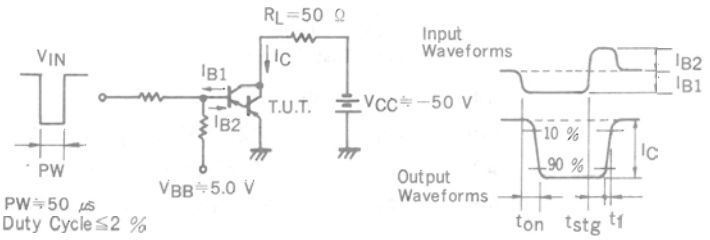
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CURCUIT



NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SB1094

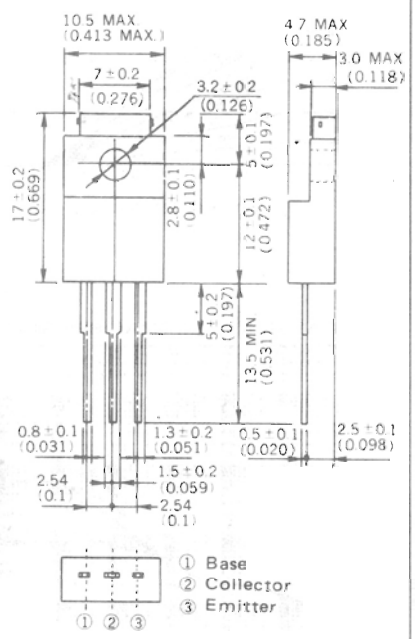
NEW DEVICE

DESCRIPTION The 2SB1094 is PNP general purpose transistor designed for use in audio frequency power amplifier.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Complementary to the 2SD1585.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . 2.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . −60 V
- V_{EBO} Emitter to Base Voltage . . . . . −7.0 A
- $I_{C(DC)}$ Collector Current (DC) . . . . . −3.0 A
- $I_{C(pulse)}$ Collector Current (Pulse)* . . . . −5.0 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	20				V_{CE} = −5.0 V, I_C = −50 mA
h_{FE2}**	DC Current Gain	40		200		V_{CE} = −5.0 V, I_C = −0.5 A
f_T	Gain Bandwidth Product		20		MHz	V_{CE} = −5.0 V, I_C = −0.1 A
C_{ob}	Output Capacitance		70		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −7.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage			−1.5	V	I_C = −2.0 A, I_B = −0.2 A
$V_{BE(sat)}$**	Base Saturation Voltage			−2.0	V	I_C = −2.0 A, I_B = −0.2 A

**Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

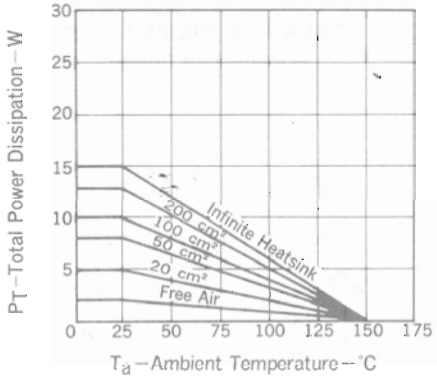
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

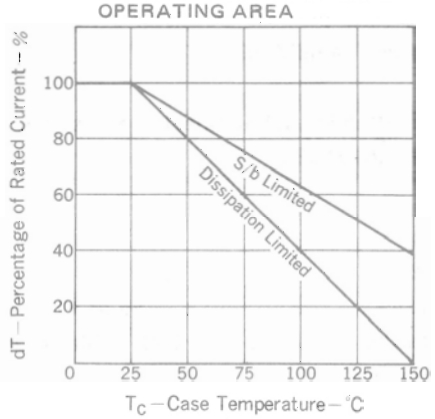
Test Conditions: V_{CE} = −5.0 V, I_C = −0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

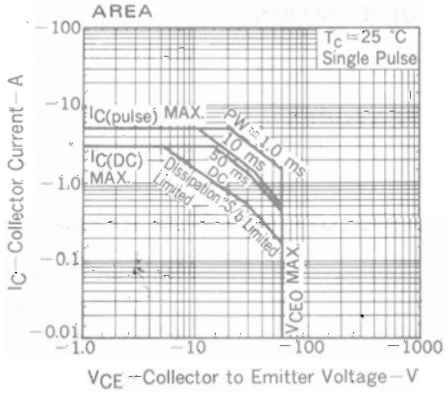
TOTAL POWER DISSIPATION vs AMBIENT TEMPERATURE



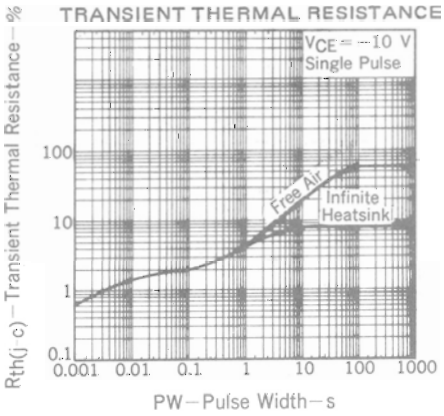
DERATING CURVE OF SAFE OPERATING AREA



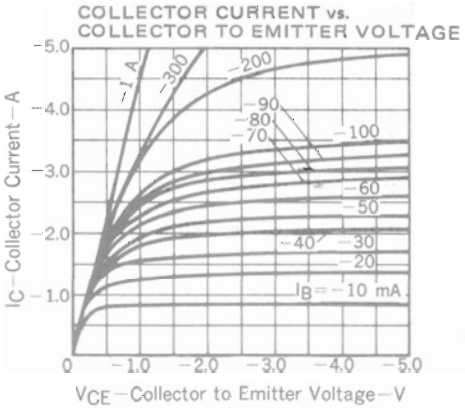
FORWARD BIAS SAFE OPERATING AREA



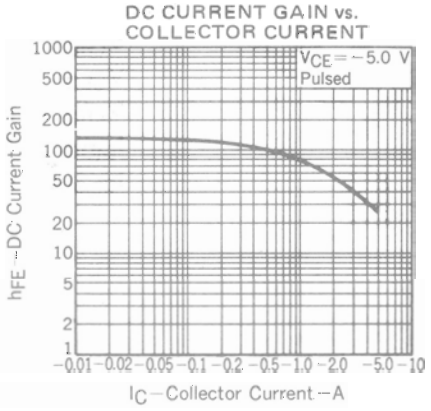
TRANSIENT THERMAL RESISTANCE



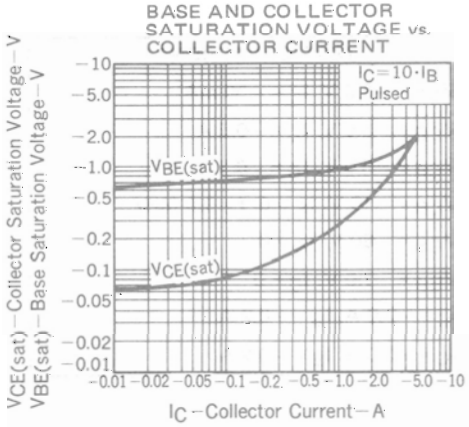
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



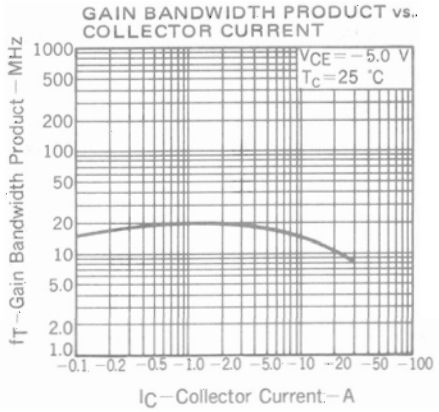
DC CURRENT GAIN vs. COLLECTOR CURRENT



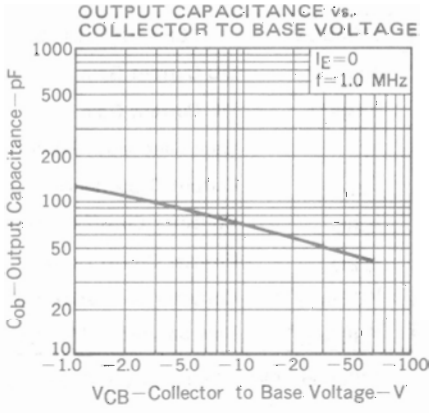
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

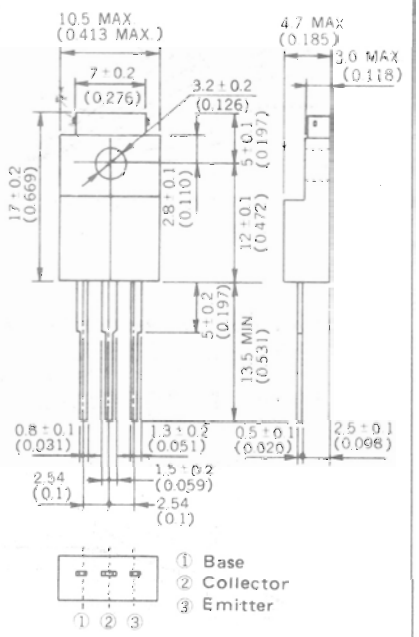
PNP SILICON POWER TRANSISTOR
2SB1095

DESCRIPTION The 2SB1095 is a PNP general purpose transistor designed for use in audio frequency power amplifier.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Complementary to the 2SD1586.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . 2.0 W
- Total Power Dissipation (T_C = 25 °C) . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −100 V
- V_{CEO} Collector to Emitter Voltage . . . −100 V
- V_{EBO} Emitter to Base Voltage . . . . . −7.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −4.0 A
- $I_{C(pulse)}$ Collector Current (Pulse)* . . . . −6.0 A

*PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	20				V_{CE} = −5.0 V, I_C = −50 mA
h_{FE2}**	DC Current Gain	40		200		V_{CE} = −5.0 V, I_C = −0.5 A
f_T	Gain Bandwidth Product		20		MHz	V_{CE} = −5.0 V, I_C = −0.1 A
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −7.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			−1.5	V	I_C = −3.0 A, I_B = −0.3 A
$V_{BE(sat)}$	Base Saturation Voltage			−2.0	V	I_C = −3.0 A, I_B = −0.3 A

**Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE2}

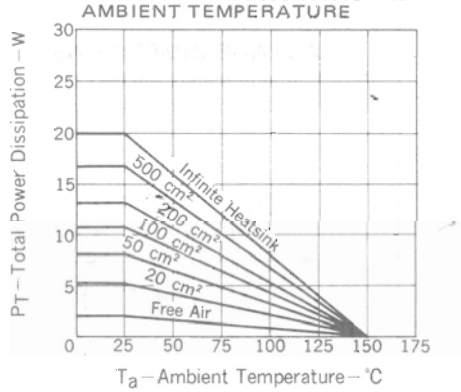
Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

Test Conditions: V_{CE} = −5.0 V, I_C = −0.5 A

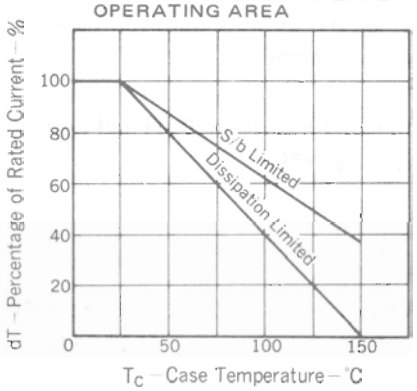
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

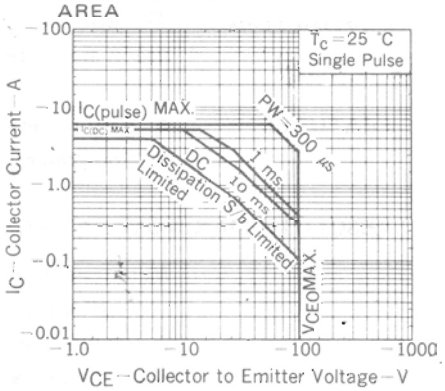
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



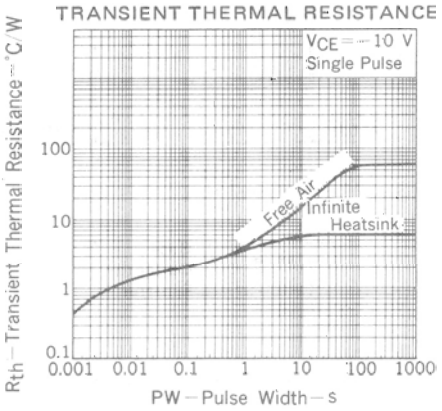
DERATING CURVE OF SAFE OPERATING AREA



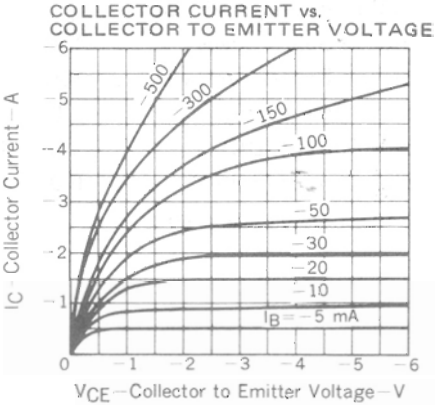
FORWARD BIAS SAFE OPERATING AREA



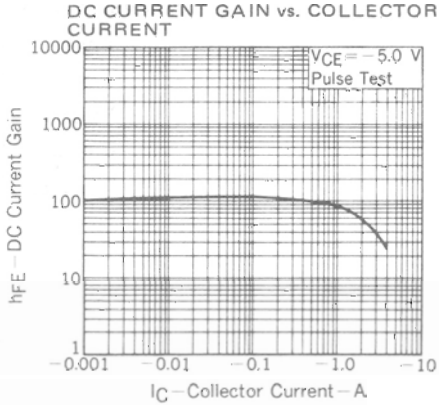
TRANSIENT THERMAL RESISTANCE



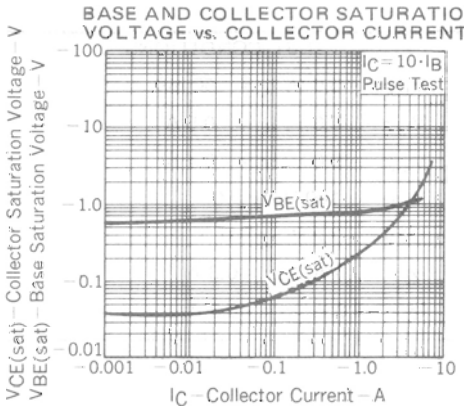
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SB1096

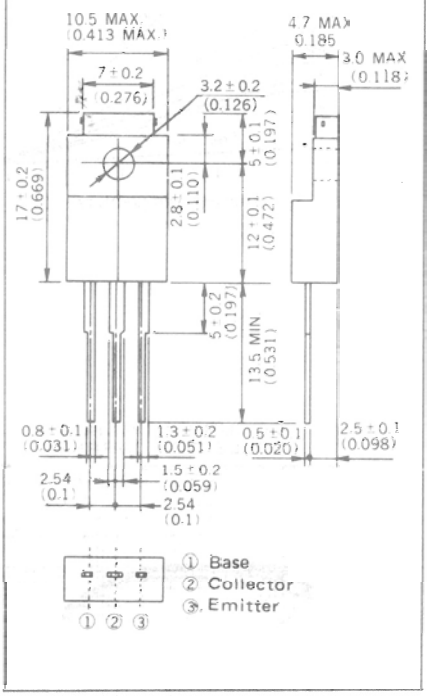
NEW DEVICE

DESCRIPTION The 2SB1096 is PNP general purpose transistor designed for use in audio frequency power amplifier.

FEATURES

- Easy mount by eliminating Sheet and Bushing.
- Complementary to the 2SD1587.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . 2.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−200	V
V_{CEO}	Collector to Emitter Voltage	−150	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
$I_{C(DC)}$	Collector Current (DC)*	−2.0	A
$I_{C(pulse)}$	Collector Current (Pulse)	−3.0	A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}**	DC Current Gain	40		200		V_{CE} = −10 V, I_C = −0.4 A
f_T	Gain Bandwidth Product		5		MHz	V_{CE} = −10 V, I_C = −0.4 A
I_{CBO}	Collector Cutoff Current			−50	μA	V_{CB} = −150 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−50	μA	V_{EB} = −4.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage			−1.0	V	I_C = −500 mA, I_B = −50 mA

** Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

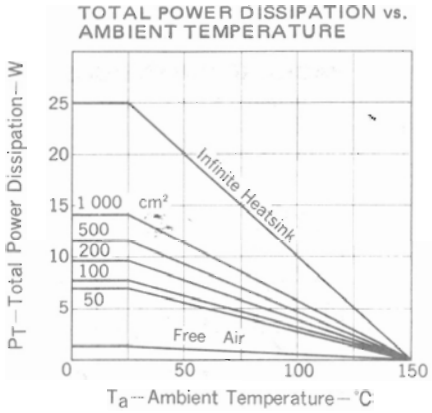
Classification of h_{FE}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

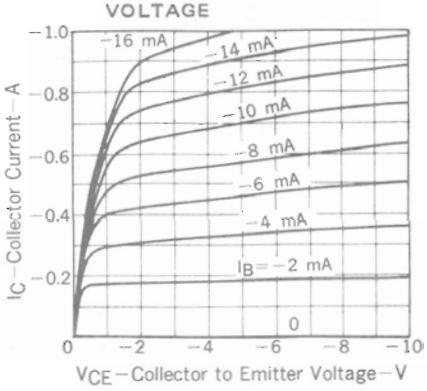
Test Conditions: V_{CE} = −10 V, I_C = −0.4 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

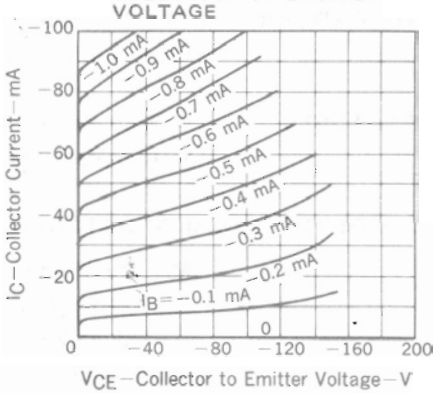
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



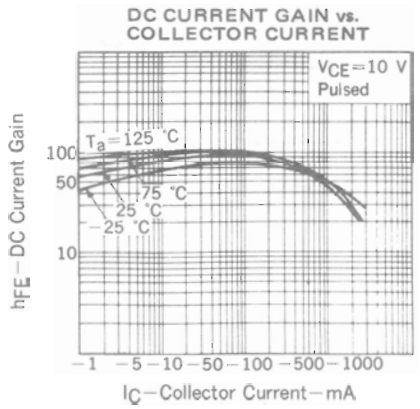
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



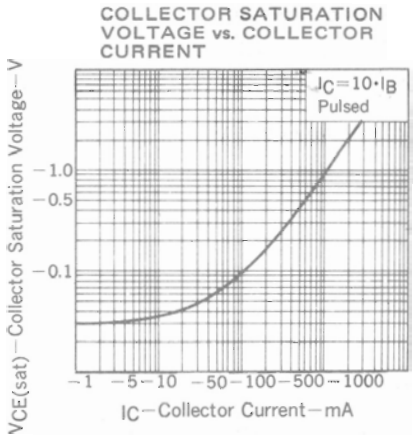
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



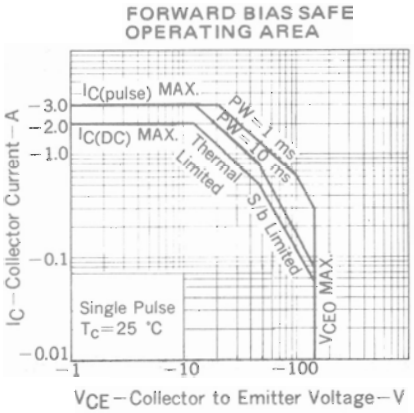
DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



FORWARD BIAS SAFE OPERATING AREA



NEC
ELECTRON DEVICE

PNP SILICON DARLINGTON POWER TRANSISTOR

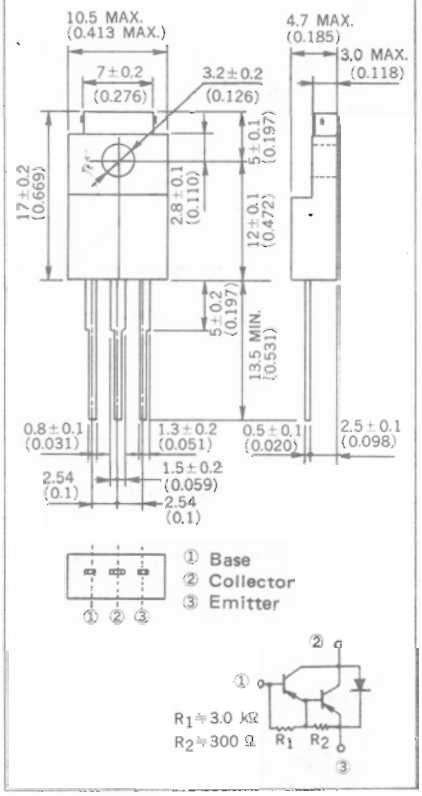
2SB1098

DESCRIPTION The 2SB1098 is PNP silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Collector to Emitter Reverse Diode is built-in.
- Low Collector Saturation Voltage.
- Complementary to 2SD1589.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100 V
V_{CEO}	Collector to Emitter Voltage	−100 V
V_{EBO}	Emitter to Base Voltage	−7.0 V
$I_{C(DC)}$	Collector Current (DC)	∓5.0 A
$I_{C(pulse)}$	Collector Current (pulse)*	∓10 A
$I_{B(DC)}$	Base Current (DC)	−0.5 A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	2000		20000	—	V_{CE} = −2.0 V, I_C = −2.0 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = −2.0 V, I_C = −4.0 A
t_{on}	Turn-on Time		0.5		μs	I_C = −2.0 A, I_{B1} = −I_{B2} = −2.0 mA, R_L = 25 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**			−1.5	V	I_C = −2.0 A, I_B = −2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage**			−2.0	V	I_C = −2.0 A, I_B = −2.0 mA
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB} = −100 V, I_E = 0

**PW ≤ 350 μs, Duty Cycle ≤ 2 %

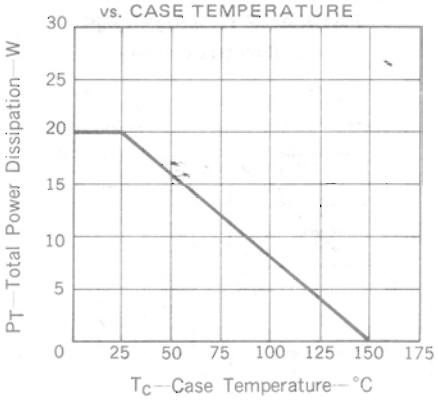
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 20000

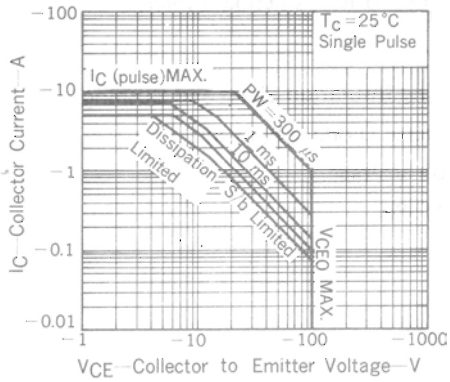
Test Conditions: V_{CE} = −2.0 V, I_C = −2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

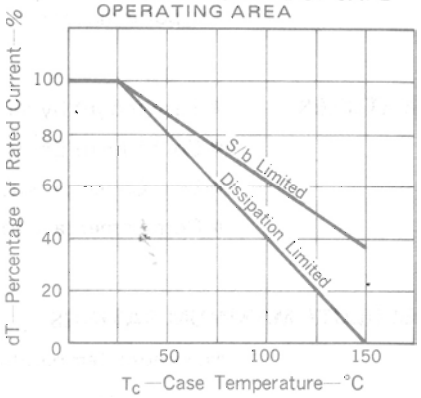
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



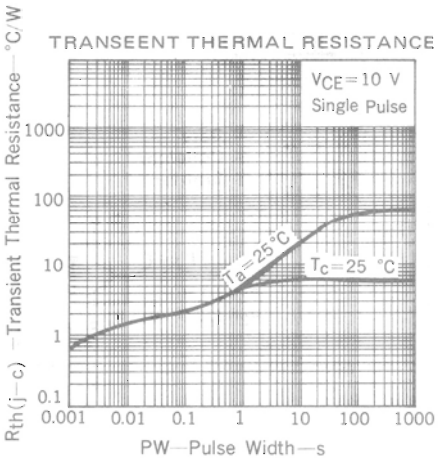
FORWARD BIAS SAFE OPERATING AREA



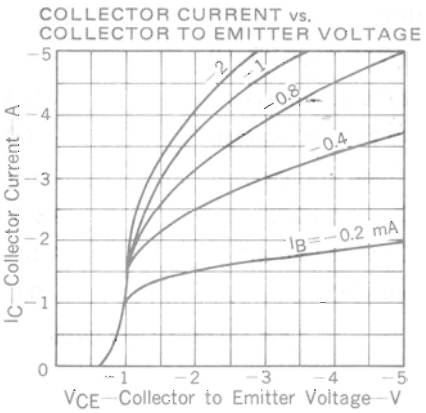
DERATING CURVE OF SAFE OPERATING AREA



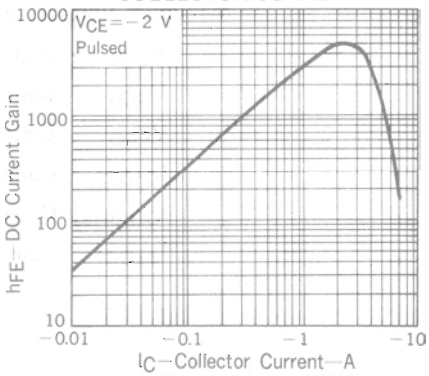
TRANSEENT THERMAL RESISTANCE



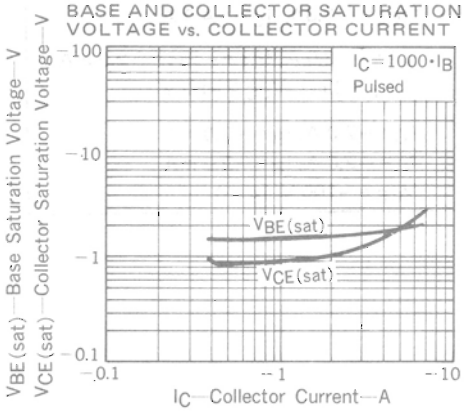
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



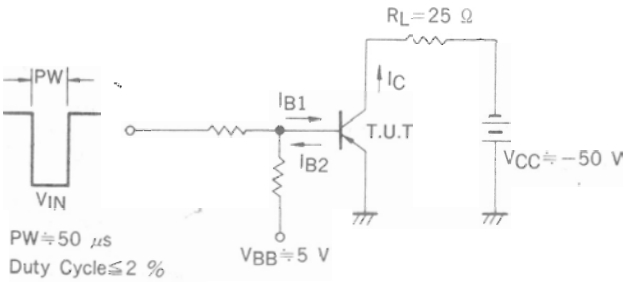
DC CURRENT GAIN vs. COLLECTOR CURRENT

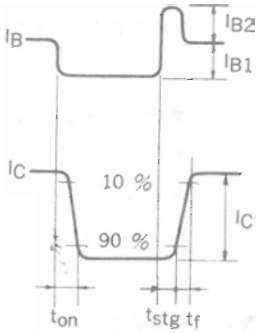


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

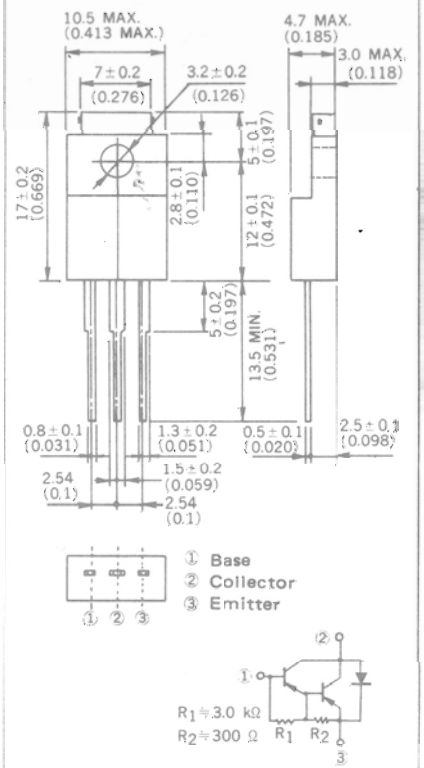
PNP SILICON DARLINGTON POWER TRANSISTOR
2SB1099

DESCRIPTION The 2SB1099 is PNP silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Collector to Emitter Reverse Diode is built-in.
- Low Collector Saturation Voltage.
- Complementary to 2SD1590.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−100 V
V_{CEO}	Collector to Emitter Voltage	−100 V
V_{EBO}	Emitter to Base Voltage	−7.0 V
$I_{C(DC)}$	Collector Current (DC)	−8.0, +5.0 A
$I_{C(pulse)}$	Collector Current (pulse)*	−12, +8.0 A
$I_{B(DC)}$	Base Current (DC)	−0.8 A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	2000		15000	—	V_{CE} = −2.0 V, I_C = −3.0 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = −2.0 V, I_C = −5.0 A
t_{on}	Turn-on Time		0.5		μs	I_C = −3.0 A, I_{B1} = −I_{B2} = −3.0 mA, R_L = 16.7 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**		−0.9	−1.5	V	I_C = −3.0 A, I_B = −3.0 mA
$V_{BE(sat)}$	Base Saturation Voltage**		−1.6	−2.0	V	I_C = −3.0 A, I_B = −3.0 mA
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB} = −100 V, I_E = 0

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

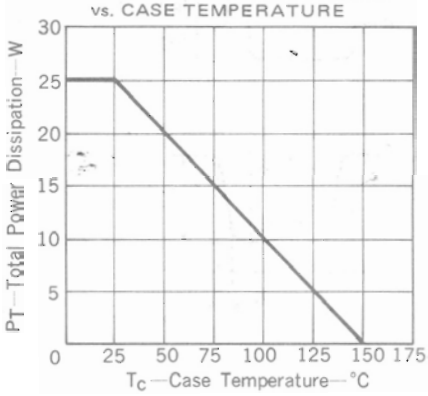
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	3000 to 7000	5000 to 15000

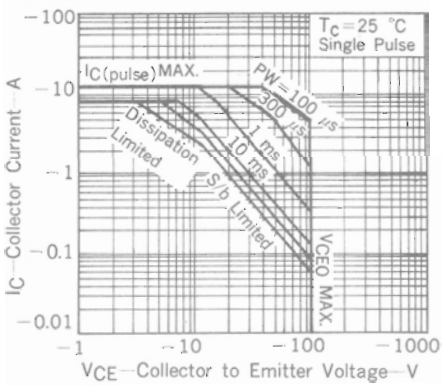
Test Conditions: V_{CE} = −2.0 V, I_C = −3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

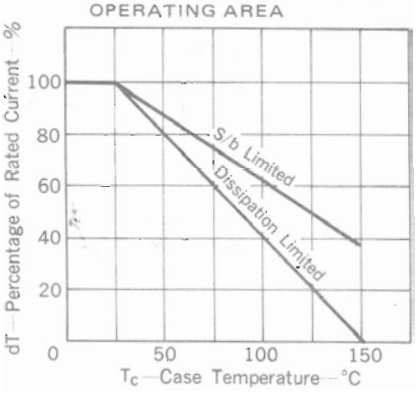
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



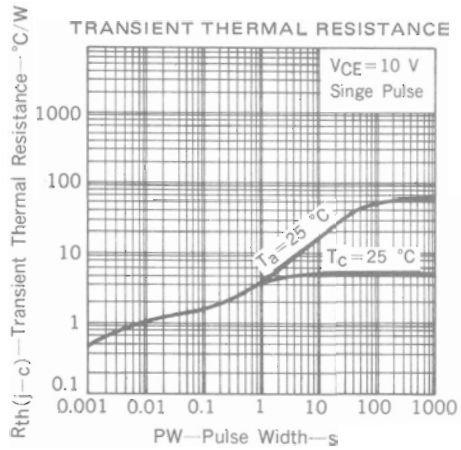
FORWARD BIAS SAFE OPERATING AREA



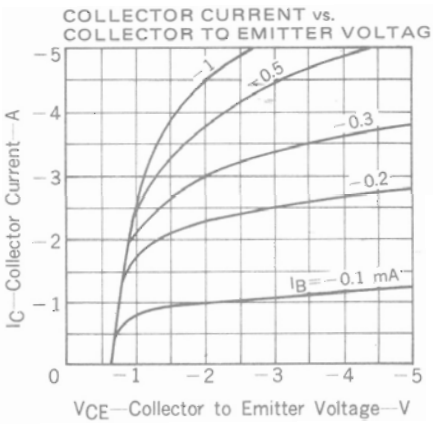
DERATING CURVE OF SAFE OPERATING AREA



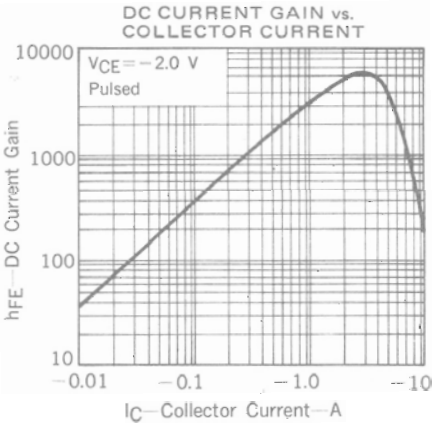
TRANSIENT THERMAL RESISTANCE



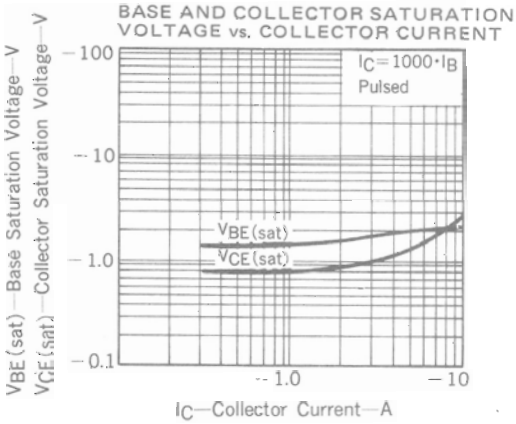
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



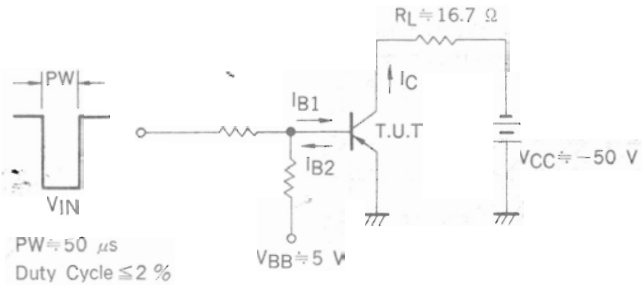
DC CURRENT GAIN vs. COLLECTOR CURRENT

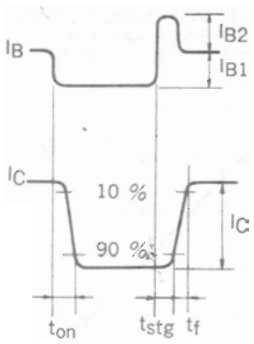


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

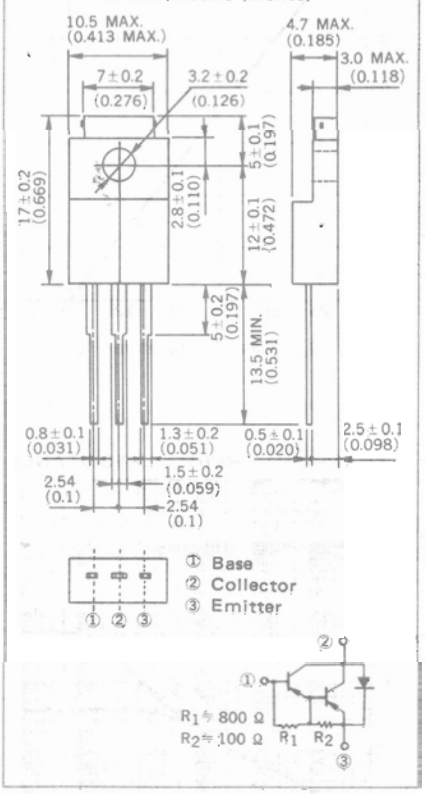
PNP SILICON DARLINGTON POWER TRANSISTOR
2SB1100

DESCRIPTION The 2SB1100 is PNP silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- High DC Current Gain.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . −100 V

V_{CEO} Collector to Emitter Voltage . . . . . −100 V

V_{EBO} Emitter to Base Voltage . . . . . −8.0 V

$I_{C(DC)}$ Collector Current (DC) . . . . . ∓10 A

$I_{C(pluse)}$ Collector Current (pulse)* . . . . . ∓20 A

$I_{B(DC)}$ Base Current (DC) . . . . . −1.0 A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain**	1000	6000	30000	–	V_{CE} = −2.0 V, I_C = −10 A
t_{on}	Turn-on Time		1.0		μs	I_C = −10 A, I_{B1} = −I_{B2} = −25 mA, R_L = 5.0 Ω, V_{CC} ≒ −50 V
t_{stg}	Storage Time		5.0		μs	
t_f	Fall Time		2.0		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**		−1.1	−1.5	V	I_C = −10 A, I_B = −25 mA
$V_{BE(sat)}$	Base Saturation Voltage**		−1.8	−2.2	V	I_C = −10 A, I_B = −25 mA
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −100 V, I_E = 0

**PW ≤ 350 μs, Duty Cycle ≤ 2 %

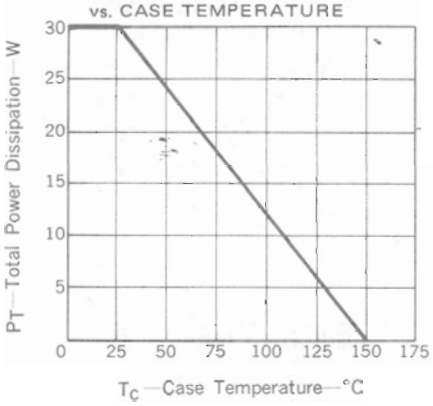
Classification of h_{FE}

Rank	M	L	K	J
Range	1000 to 3000	2000 to 5000	4000 to 10000	8000 to 30000

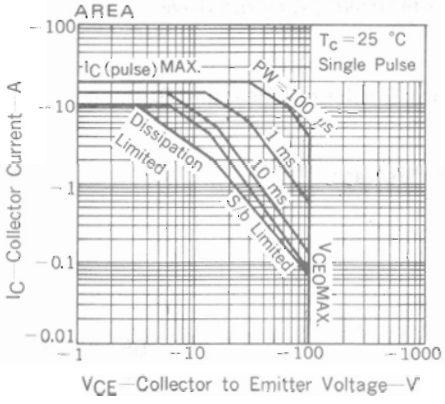
Test Conditions: V_{CE} = −2.0 V, I_C = −10 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

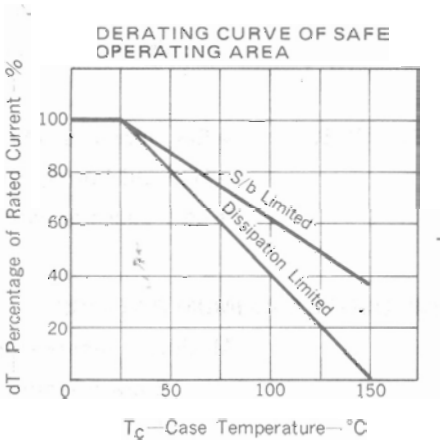
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



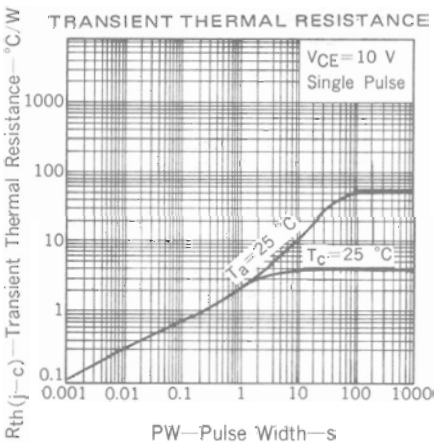
FORWARD BIAS SAFE OPERATING AREA



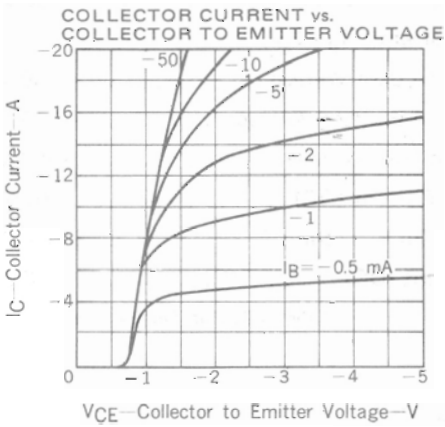
DERATING CURVE OF SAFE OPERATING AREA



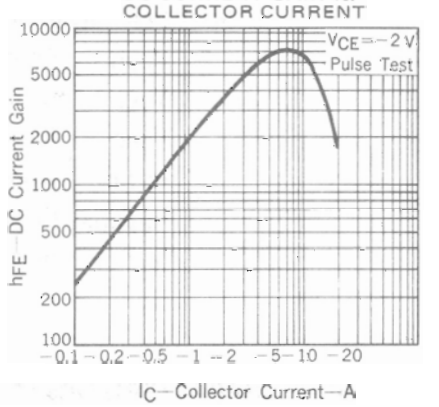
TRANSIENT THERMAL RESISTANCE



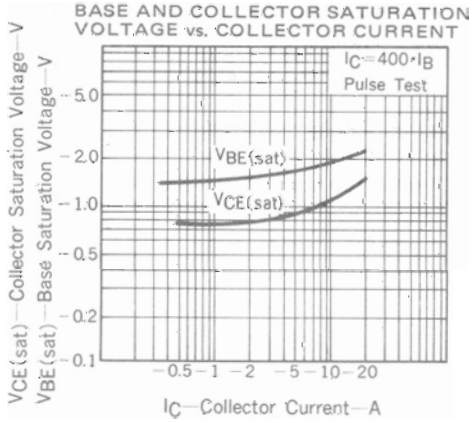
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



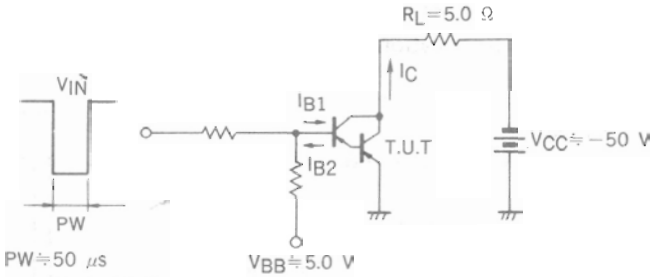
DC CURRENT GAIN vs. COLLECTOR CURRENT



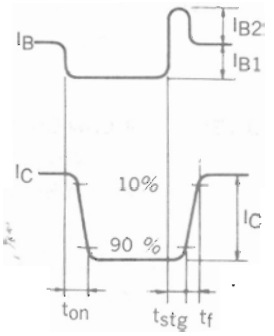
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT



PW≒50 μs
Duty Cycle≦2 %



NEC
ELECTRON DEVICE

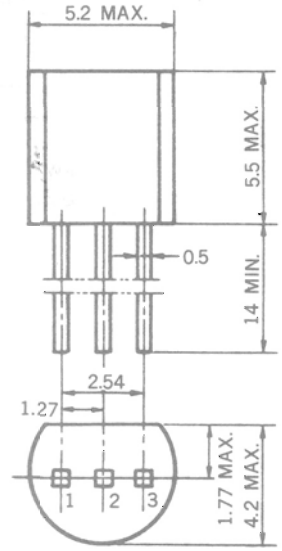
PNP SILICON TRANSISTORS
2SB1116, 2SB1116A

DESCRIPTION The 2SB1116/2SB1116A are designed for use in driver and output stages of AF amplifier, general purpose application.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = −0.20 V TYP. (I_C = −1.0 A, I_B = −50 mA)
- High Break Down Voltage.
  V_{CEO} = −50 V/−60 V (2SB1116/2SB1116A)
- High Total Power Dissipation. : P_T = 0.75 W (T_a = 25 °C)
- Complementary to the NEC 2SD1616/2SD1616A NPN Transistor.

PACKAGE DIMENSIONS
in millimeters



1. Emitter
2. Collector
3. Base

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C) 2SB1116/2SB1116A

V_{CBO}	Collector to Base Voltage	−60 V/−80 V
V_{CEO}	Collector to Emitter Voltage	−50 V/−60 V
V_{EBO}	Emitter to Base Voltage	−6.0 V
I_C	Collector Current (DC)	−1.0 A
I_C	Collector Current (pulse)*	−2.0 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

2SB1116/2SB1116A

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	135		600	−	V_{CE} = −2.0 V, I_C = −100 mA
h_{FE2}**	DC Current Gain	81			−	V_{CE} = −2.0 V, I_C = −1.0 A
f_T	Gain Bandwidth Product	70	120		MHz	V_{CE} = −2.0 V, I_C = −100 mA
C_{ob}	Output Capacitance		25		pF	V_{CB} = −10 V, I_E = 0, f ≈ 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −60 V/−80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −6.0 V, I_C = 0
V_{BE}**	Base to Emitter Voltage	−600		−700	mV	V_{CE} = −2.0 V, I_C = −50 mA
$V_{CE(sat)}$**	Collector Saturation Voltage		−0.2	−0.3	V	I_C = −1.0 A, I_B = −50 mA
$V_{BE(sat)}$**	Base Saturation Voltage		−0.9	−1.2	V	I_C = −1.0 A, I_B = −50 mA
t_{on}	Turn-On Time		0.07		μs	V_{CC} = −10 V, I_C = −100 mA
t_{stg}	Storage Time		0.70		μs	I_{B1} = −I_{B2} = −10 mA
t_f	Fall Time		0.07		μs	$V_{BE(off)}$ = 2 to 3 V

**Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

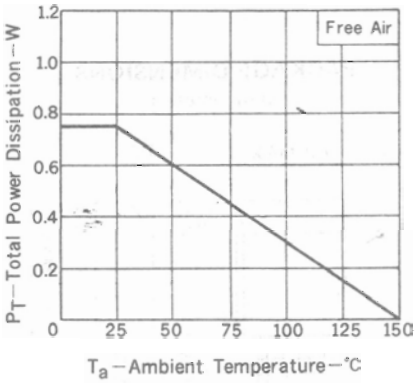
Classification of h_{FE1}

Rank	L	K	U
Range	135 to 270	200 to 400	300 to 600

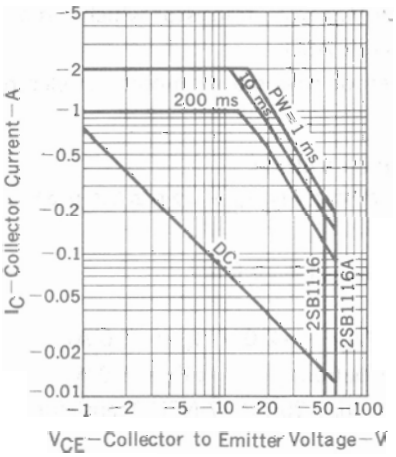
Test Conditions: V_{CE} = −2.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

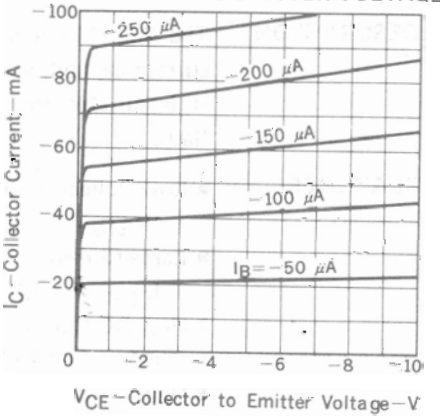
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



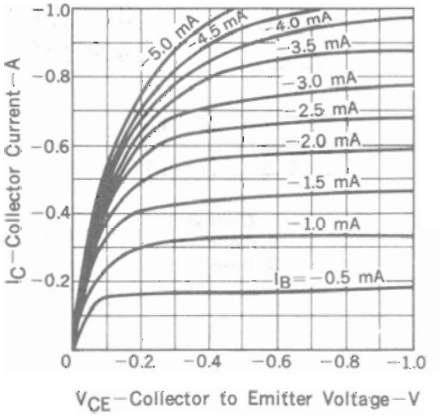
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



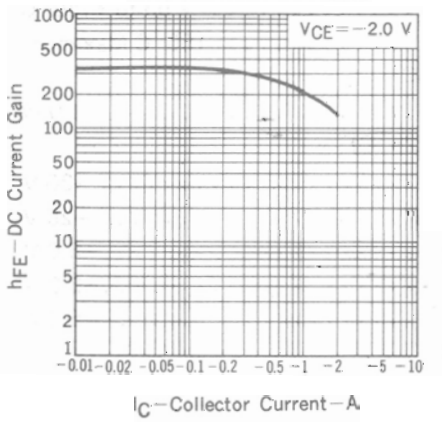
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



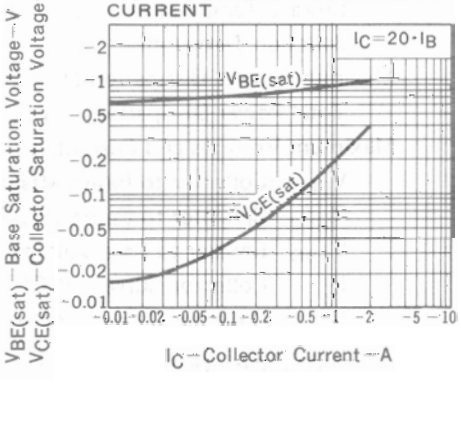
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



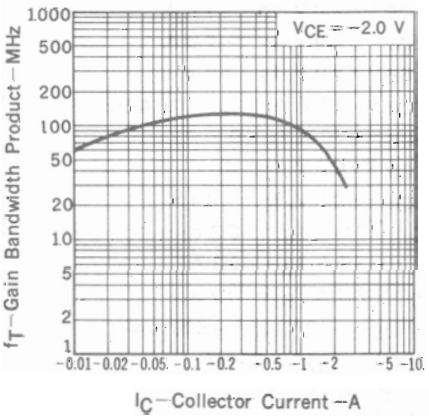
DC CURRENT GAIN vs. COLLECTOR CURRENT



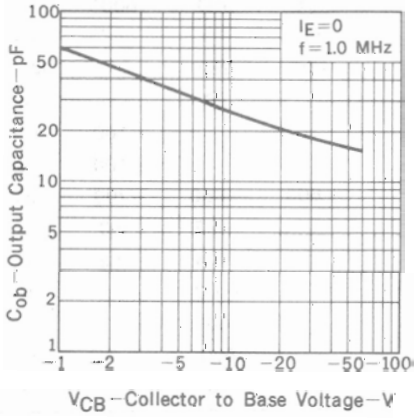
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



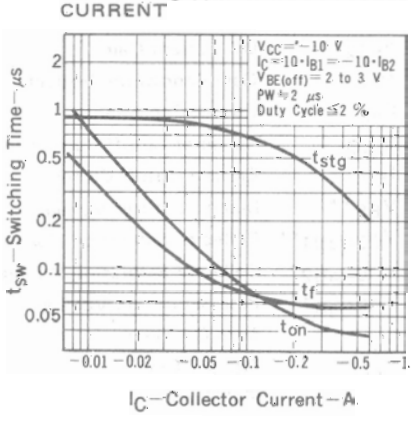
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

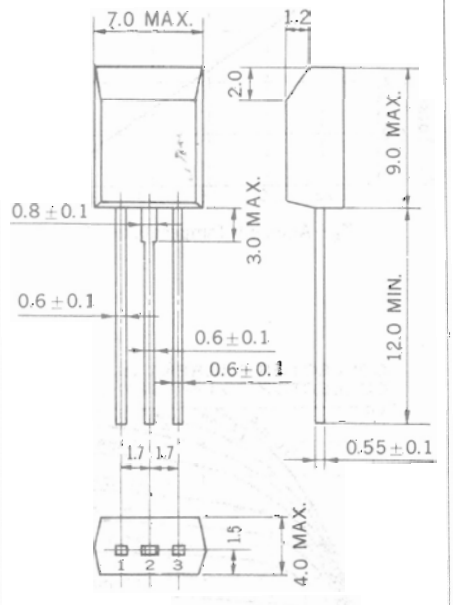
PNP SILICON TRANSISTOR
2SB1117

DESCRIPTION The 2SB1117 is a Low $V_{CE(sat)}$ transistor which has a large current capability and wide ASO.
It is suitable for driver of solenoid or motor, or electronic flash.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = −0.2 V TYP. (@ I_C/I_B = −2.0 A/−0.2 A)
- Large Current.
  $I_{C(DC)}$ = −3.0 A, $I_{C(pulse)}$ = −5.0 A
- High DC Current Gain. :
  h_{FE} = 300 TYP. (@ V_{CE} = −2.0 V, I_C = −1.0 A)
- High Total Power Dissipation. : P_T = 1.0 W
- Complementary to the NEC 2SD1617 NPN Transistor.

PACKAGE DIMENSIONS
in millimeters



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −30 V
- V_{CEO} Collector to Emitter Voltage . . . . . −25 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current (DC) . . . . . −3.0 A
- I_C Collector Current (pulse)* . . . . . −5.0 A

*PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	135	300	600	—	V_{CE} = −2.0 V, I_C = −1.0 A
h_{FE2}**	DC Current Gain	81			—	V_{CE} = −2.0 V, I_C = −2.0 A
f_T	Gain Bandwidth Product	100	280		MHz	V_{CE} = −5.0 V, I_E = 1.0 A
C_{ob}	Output Capacitance		90		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −6.0 V, I_C = 0
V_{BE}**	Base to Emitter Voltage	−600	−660	−700	mV	V_{CE} = −2.0 V, I_C = −0.1 A
$V_{CE(sat)1}$**	Collector Saturation Voltage		−0.2	−0.3	V	I_C = −2.0 A, I_B = −0.2 A
$V_{CE(sat)2}$**	Collector Saturation Voltage		−0.3	−0.5	V	I_C = −3.0 A, I_B = −0.3 A
$V_{BE(sat)}$**	Base Saturation Voltage		−1.0	−1.2	V	I_C = −2.0 A, I_B = −0.2 A
t_{on}	Turn On Time		80		ns	V_{CE} = −10 V, I_C = −500 mA
t_{stg}	Storage Time		500		ns	I_{B1} = −I_{B2} = −50 mA
t_f	Fall Time		70		ns	$V_{BE(off)}$ = 2 to 3 V

**Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2%

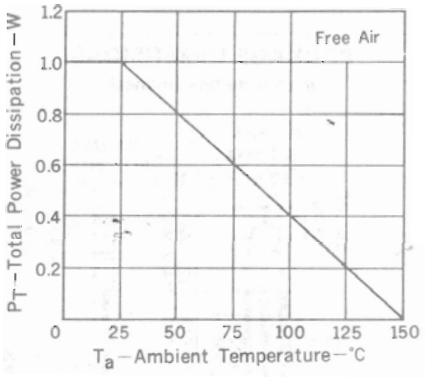
Classification of h_{FE1}

Rank	L	K	U
Range	135 to 270	200 to 400	300 to 600

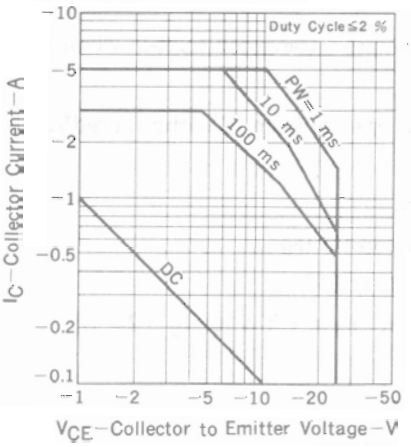
Test Conditions: V_{CE} = −2.0 V, I_C = −1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

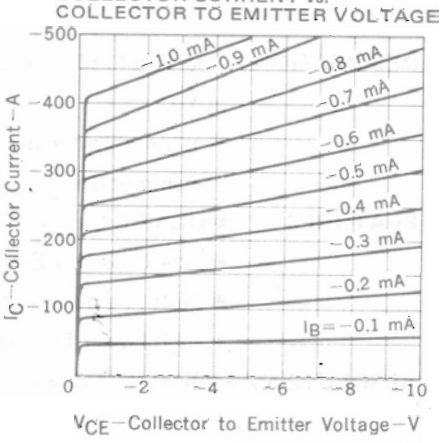
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



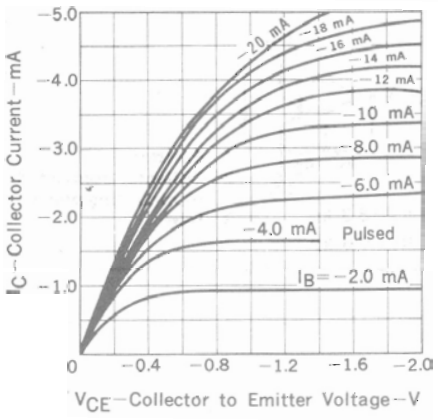
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



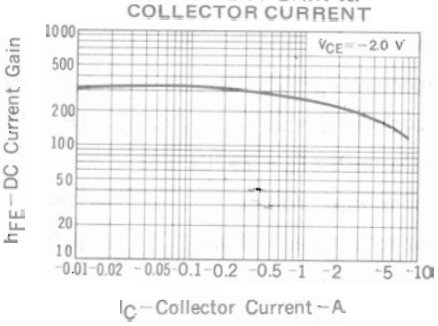
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



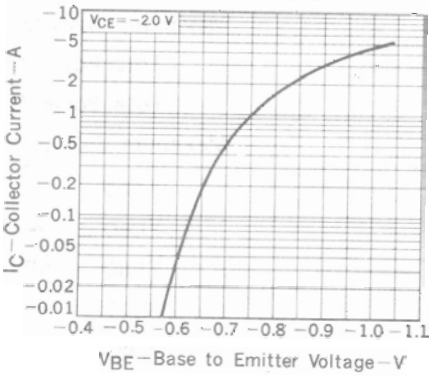
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



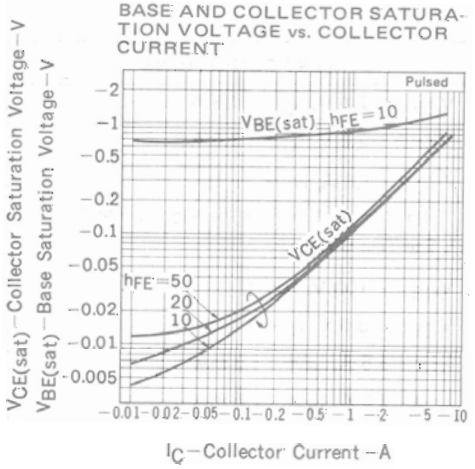
DC CURRENT GAIN vs. COLLECTOR CURRENT



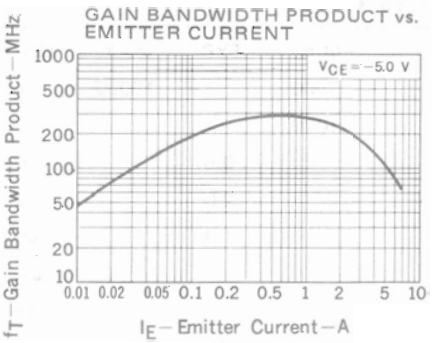
BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



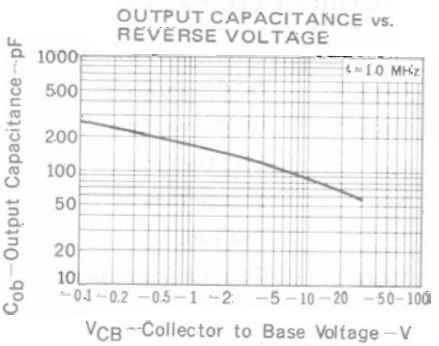
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

PNP SILICON DARLINGTON TRANSISTOR
2SB1149

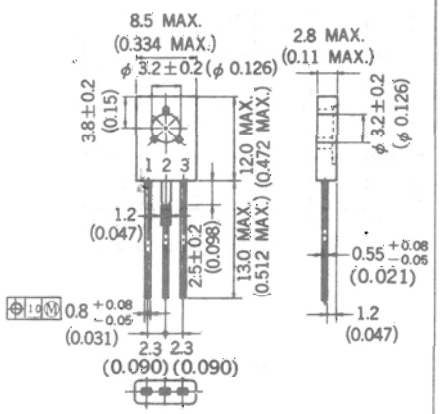
DESCRIPTION The 2SB1149 is a darlington transistor built-in dumper diode at E-C.

It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES

- High DC Current Gain.
- Low Collector Saturation Voltage.
- Built-in a dumper diode at E-C.
- High Power Dissipation: P_T = 1.3 W (at T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −100 V
- V_{CEO} Collector to Emitter Voltage . . . . . −100 V
- V_{EBO} Emitter to Base Voltage . . . . . −8.0 V
- $I_{C(DC)}$ Collector Current . . . . . ∓3.0 A
- $I_{C(pulse)}$* Collector Current . . . . . ∓5.0 A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	2000		15000	—	V_{CE} = −2.0 V, I_C = −1.5 A
h_{FE2}**	DC Current Gain	1000			—	V_{CE} = −2.0 V, I_C = −3.0 A
t_{on}	Turn On Time		0.5		μs	I_C = −1.5 A, R_L = 27 Ω
t_{stg}	Storage Time		2.0		μs	I_{B1} = −I_{B2} = −1.5 mA, V_{CC} ≒ −40 V
t_f	Fall Time		1.0		μs	See Test Circuit.
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	mA	V_{EB} = −5.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage		−0.9	−1.2	V	I_C = −1.5 A, I_B = −1.5 mA
$V_{BE(sat)}$**	Base Saturation Voltage		−1.5	−2.0	V	I_C = −1.5 A, I_B = −1.5 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

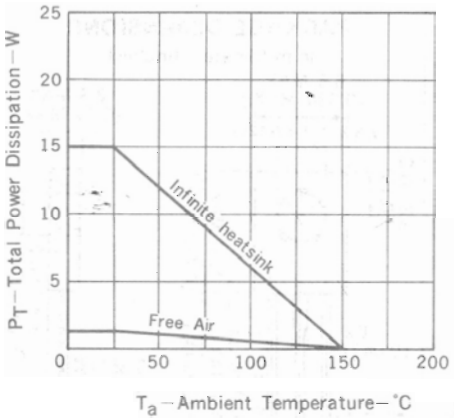
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	3000 to 7000	5000 to 15000

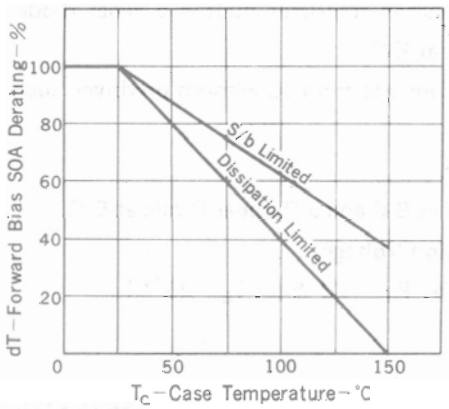
Test Conditions: V_{CE} = −2.0 V, I_C = −1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

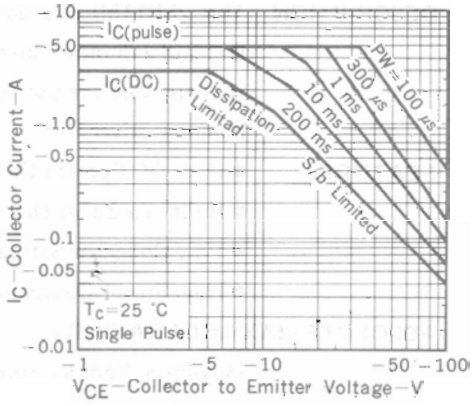
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



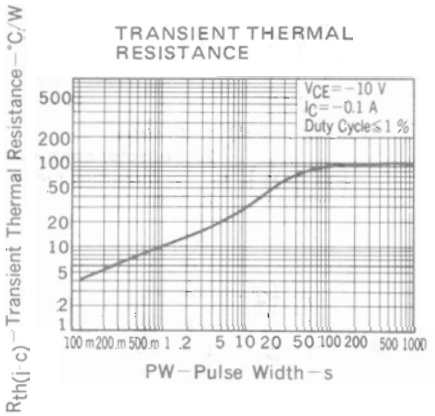
DERATING CURVE OF SAFE OPERATING AREA



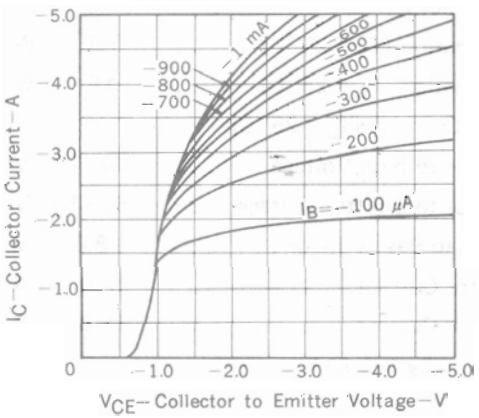
FORWARD BIAS SAFE OPERATING AREA



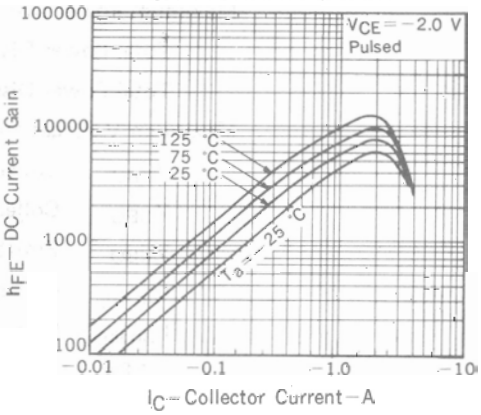
TRANSIENT THERMAL RESISTANCE



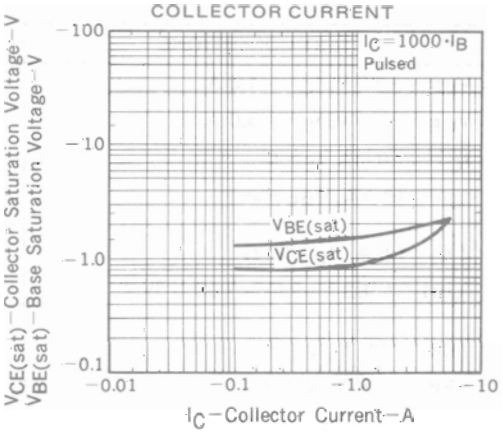
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



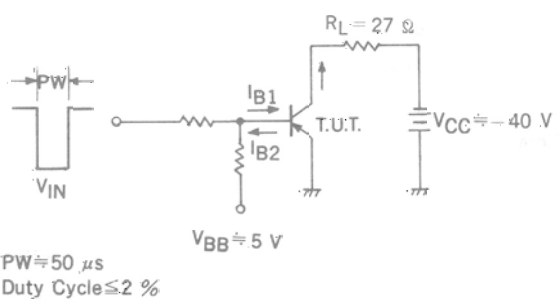
DC CURRENT GAIN vs. COLLECTOR CURRENT



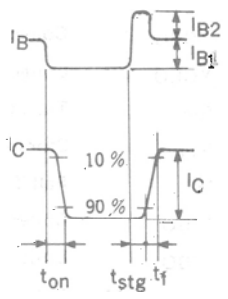
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



PW ≒ 50 μs
Duty Cycle ≤ 2 %



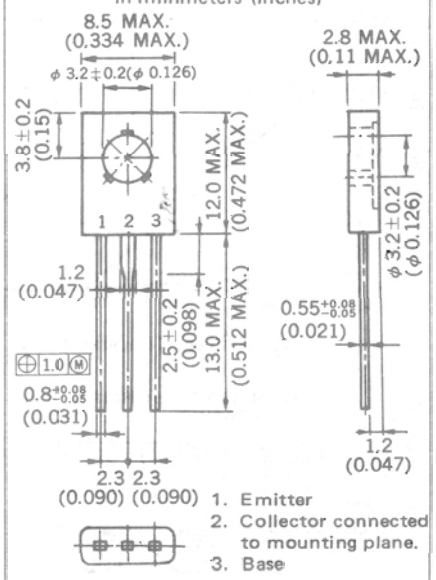
NEC
ELECTRON DEVICE

PNP SILICON DARLINGTON TRANSISTOR
2SB1150

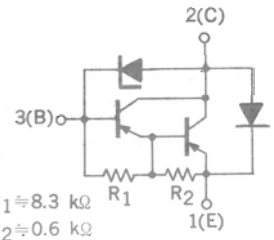
DESCRIPTION The 2SB1150 is a darlington transistor built-in a zener diode at B-C and a dumper diode at E-C.
It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES
- High DC Current Gain.
- Built-in a Zener Diode at B-C and a Dumper Diode at E-C.
- Low Collector Saturation Voltage.
- High Power Dissipation: P_T = 1.3 W (at T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane.
3. Base



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation (T_a = 25 °C)	1.3	W
Total Power Dissipation (T_c = 25 °C)	15	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−60 ∓10	V
V_{CEO}	Collector to Emitter Voltage	−60 ∓10	V
V_{EBO}	Emitter to Base Voltage	−8.0	V
$I_{C(DC)}$	Collector Current	∓3.0	A
$I_{C(pulse)}$*	Collector Current	∓5.0	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	2000		15000	—	V_{CE} = −2.0 V, I_C = −1.5 A
h_{FE2}**	DC Current Gain	1000			—	V_{CE} = −2.0 V, I_C = −3.0 A
V_{CBO}	Collector to Base Voltage	−50	−60	−70	V	I_C = −1.0 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	−50	−60	−70	V	I_C = −10 mA, R_{BE} = ∞
t_{on}	Turn On Time		0.5		μs	I_C = 1.5 A, R_L = 27 Ω I_{B1} = −I_{B2} = 1.5 mA, V_{CC} ≒ 40 V
t_{stg}	Storage Time		2.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−1.0	mA	V_{EB} = −5.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage		−0.9	−1.2	V	I_C = −1.5 A, I_B = −1.5 mA
$V_{BE(sat)}$**	Base Saturation Voltage		−1.5	−2.0	V	I_C = −1.5 A, I_B = −1.5 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

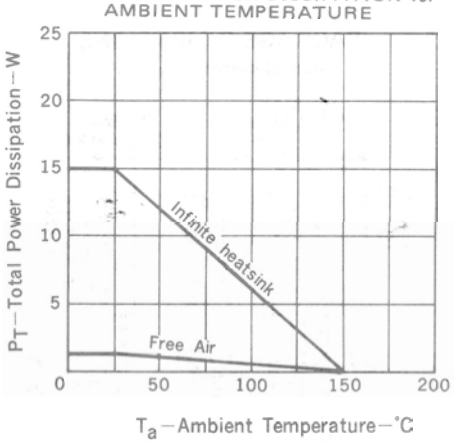
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	3000 to 7000	5000 to 15000

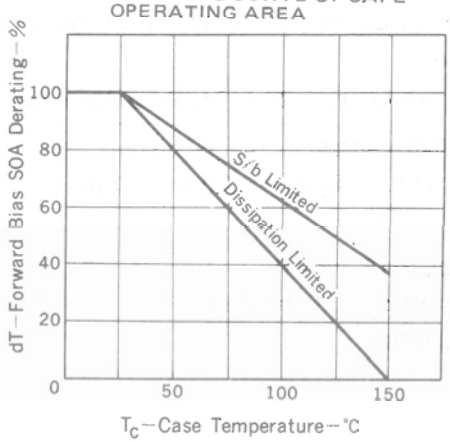
Test Conditions: V_{CE} = −2.0 V, I_C = −1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

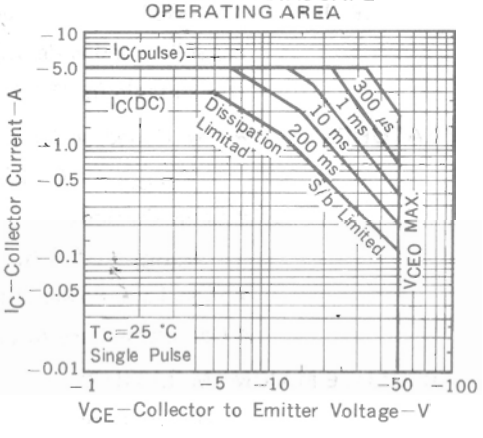
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



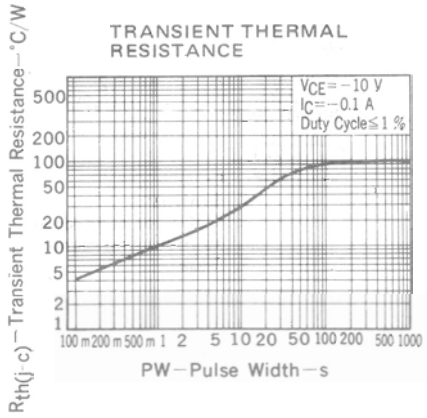
DERATING CURVE OF SAFE OPERATING AREA



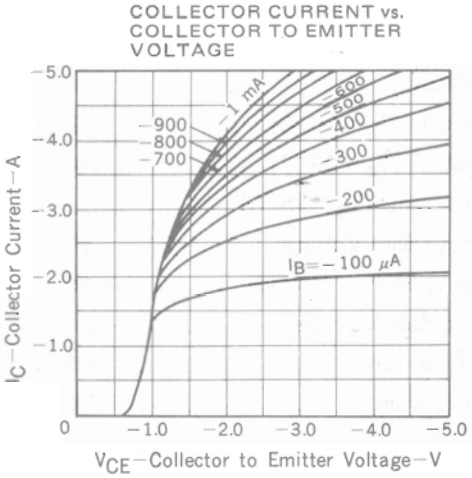
FORWARD BIAS SAFE OPERATING AREA



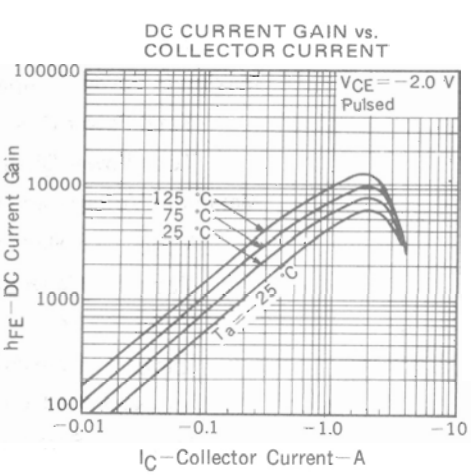
TRANSIENT THERMAL RESISTANCE



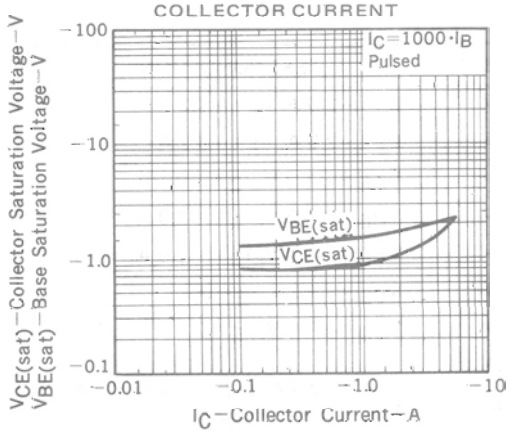
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



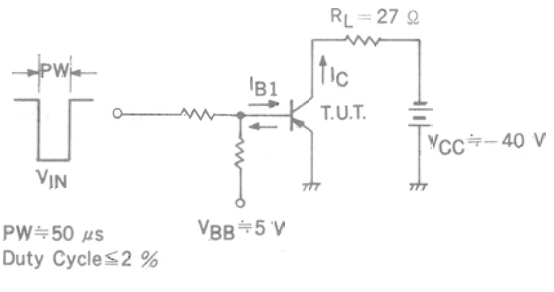
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SB1151

DESCRIPTION The 2SB1151 is a Low $V_{CE(sat)}$ transistor which has a large current capability and wide SOA.

It is suitable for DC-DC converter, or driver of solenoid or motor.

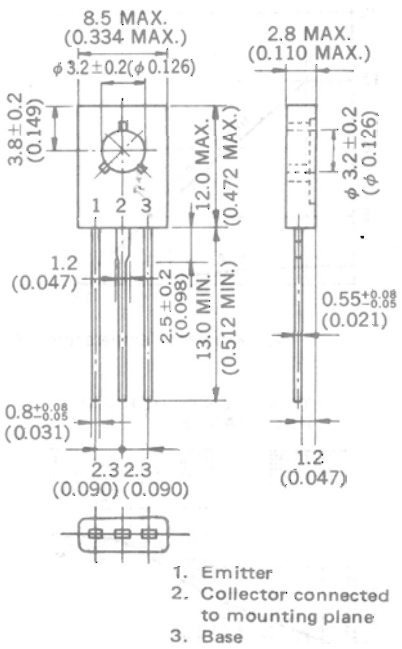
FEATURES

- Low Collector Saturation Voltage.

  $V_{CE(sat)}$ = −0.14 V TYP. (@ I_C/I_B = −2.0 A/−0.2 A)
- Large Current.

  $I_{C(DC)}$ = −5.0 A, $I_{C(pulse)}$ = −8.0 A
- High Total Power Dissipation. : P_T = 1.3 W
- Complementary to 2SD1691.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −60 V
- V_{EBO} Emitter to Base Voltage . . . . . −7.0 V
- $I_{C(DC)}$ Collector Current . . . . . −5.0 A
- $I_{C(pulse)}$* Collector Current . . . . . −8.0 A
- $I_{B(DC)}$ Base Current . . . . . −1.0 A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$V_{CE(sat)}$**	Collector Saturation Voltage		−0.14	−0.3	V	I_C = −2.0 A, I_B = −0.2 A
$V_{BE(sat)}$**	Base Saturation Voltage		−0.9	−1.2	V	I_C = −2.0 A, I_B = −0.2 A
h_{FE1}**	DC Current Gain	60			−	V_{CE} = −1.0 V, I_C = −0.1 A
h_{FE2}**	DC Current Gain	100	200	400	−	V_{CE} = −1.0 V, I_C = −2.0 A
h_{FE3}**	DC Current Gain	50			−	V_{CE} = −2.0 V, I_C = −5.0 A
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −7.0 V, I_C = 0
t_{on}	Turn On Time		0.15	1.0	μs	I_C = −2.0 A, I_{B1} = −I_{B2} = 0.2 A R_L = 5.0 Ω, V_{CC} ≒ −10 V
t_{stg}	Storage Time		0.78	2.5	μs	
t_f	Fall Time		0.18	1.0	μs	

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

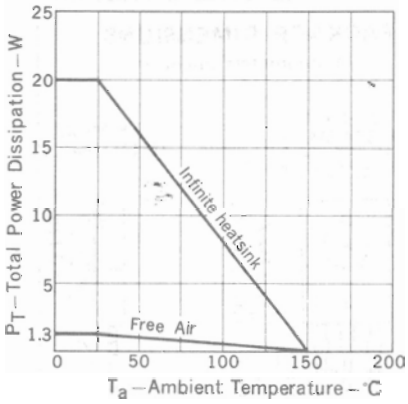
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	160 to 320	200 to 400

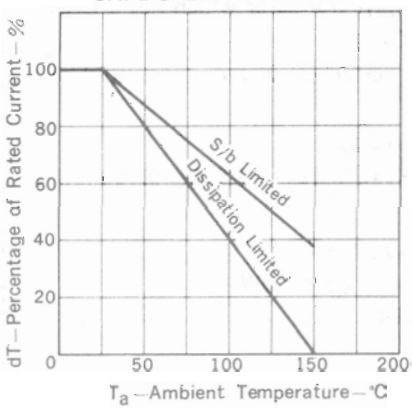
Test Conditions: V_{CE} = −1.0 V, I_C = −2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

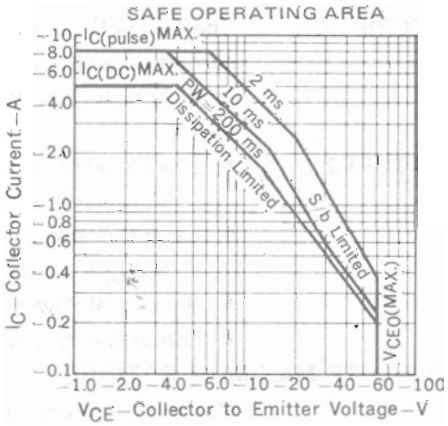
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



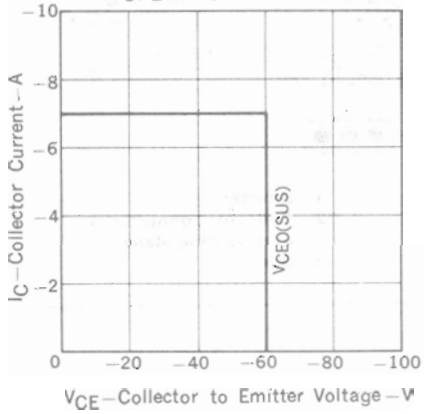
DERATING CURVE OF SAFE OPERATING AREA



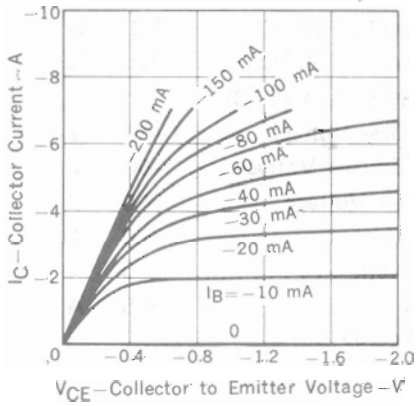
SAFE OPERATING AREA



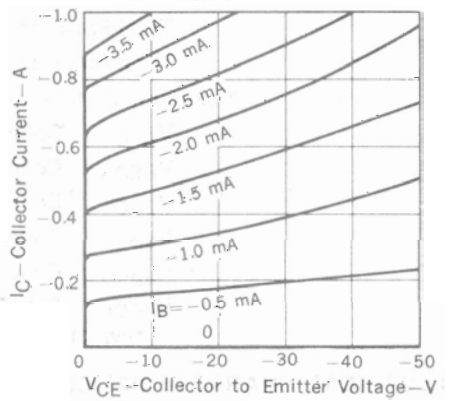
REVERSE BIAS SAFE OPERATING AREA



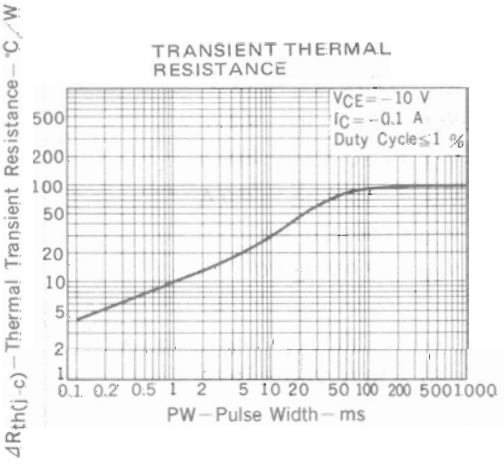
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



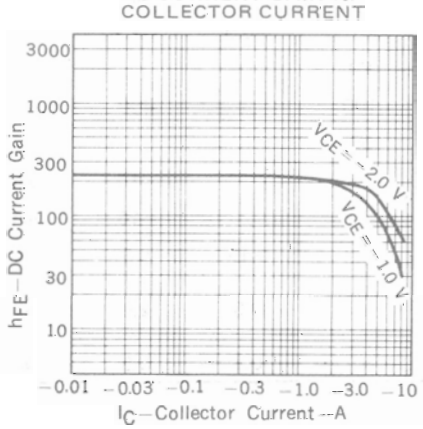
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



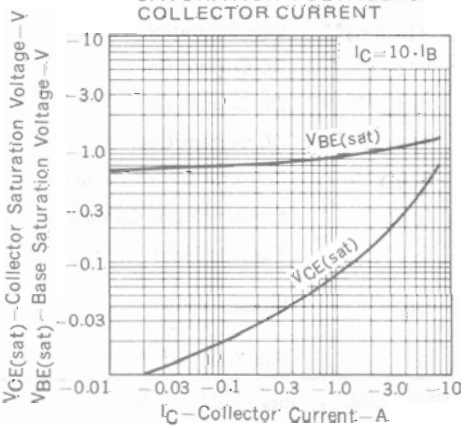
TRANSIENT THERMAL RESISTANCE



DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

PNP SILICON POWER TRANSISTOR
2SB1217

DESCRIPTION The 2SB1217 is a Low $V_{CE(sat)}$ transistor which has a large current capability and wide SOA.
It is suitable for DC-DC converter, or driver of solenoid or motor.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = −0.3 V MAX. (@I_C/I_B = −1.5 A/−0.15 A)
- Large Current
  $I_{C(DC)}$ = −3.0 A, $I_{C(pulse)}$ = −5.0 A
- High Total Power Dissipation.: P_T = 1.3W
- Complementary to 2SD1818

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C
Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

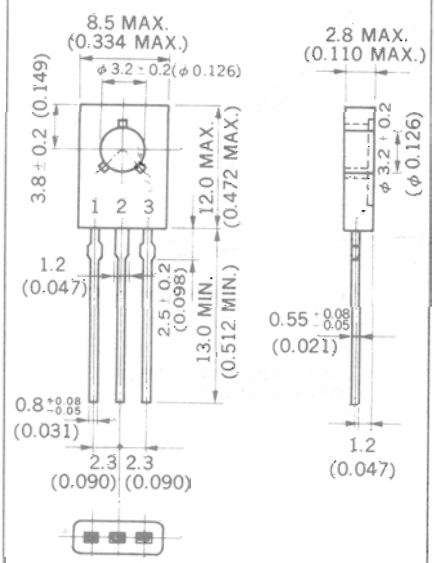
Total Power Dissipation (T_a = 25 °C) . . .	1.3	W
Total Power Dissipation (T_C = 25 °C) . . .	10	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	−60	V
V_{CEO}	Collector to Emitter Voltage . .	−60	V
V_{EBO}	Emitter to Base Voltage	−7.0	V
$I_{C(DC)}$	Collector Current	−3.0	A
$I_{C(pulse)}$*	Collector Current	−5.0	A
$I_{B(DC)}$	Base Current	−0.5	A

*PW ≦ 10 μs, Duty Cycle ≦ 50 %

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$V_{CE(sat)}$**	Collector Saturation Voltage		−0.2	−0.3	V	I_C = −1.5 A, I_B = −0.15 A
$V_{BE(sat)}$**	Base Saturation Voltage		−0.9	−1.2	V	I_C = −1.5 A, I_B = −0.15 A
h_{FE1}**	DC Current Gain	60			—	V_{CE} = −2.0 V, I_C = −0.2 A
h_{FE2}**	DC Current Gain	100		400	—	V_{CE} = −2.0 V, I_C = −0.6 A
h_{FE3}**	DC Current Gain	50			—	V_{CE} = −2.0 V, I_C = −2.0 A
I_{CBO}	Collector Cutoff Current			−10	μA	V_{CB} = −60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−10	μA	V_{EB} = −7.0 V, I_C = 0
t_{on}	Turn-On Time		0.15	0.5	μs	I_C = −1.0 A, I_{B1} = −I_{B2} = −0.1 A R_L = 10 Ω, V_{CC} ≒ −10 V
t_{stg}	Storage Time		0.5	2.0	μs	
t_f	Fall Time		0.1	0.5	μs	

**PW ≦ 350 μs, Duty Cycle ≦ 2 %

Classification of h_{FE2}

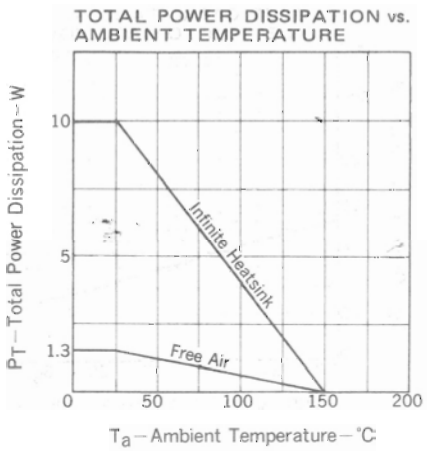
Rank	M	L	K
Range	100 to 200	160 to 320	200 to 400

Test Conditions V_{CE} = −2.0 V, I_C = −0.6 A

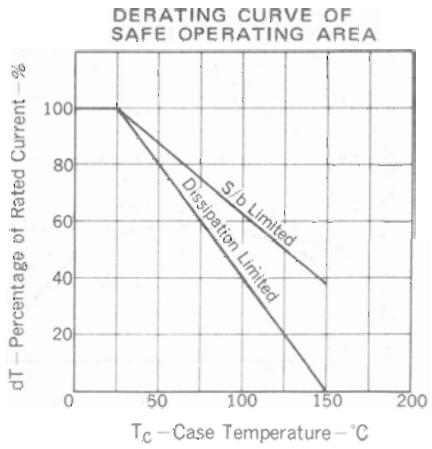
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

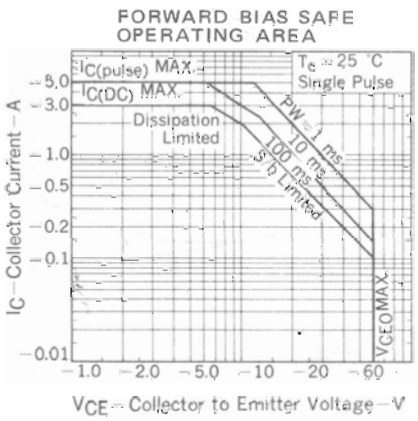
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



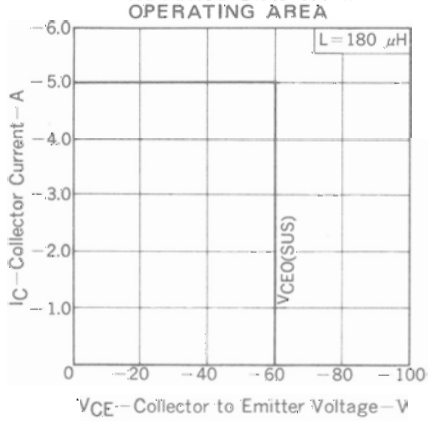
DERATING CURVE OF SAFE OPERATING AREA



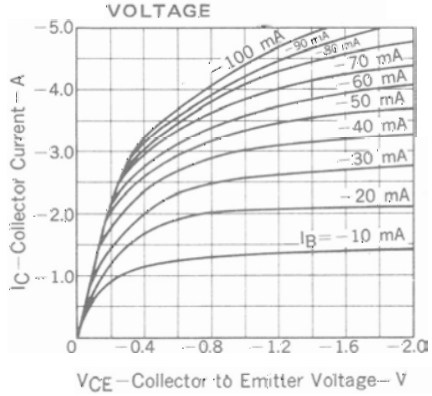
FORWARD BIAS SAFE OPERATING AREA



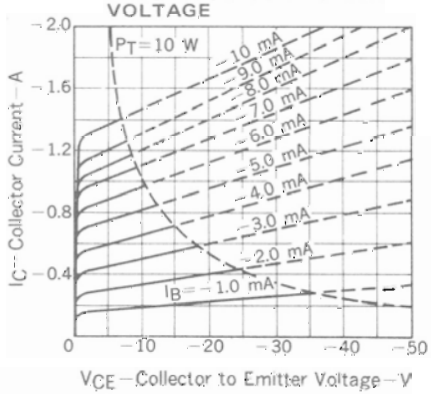
REVERSE BIAS SAFE OPERATING AREA



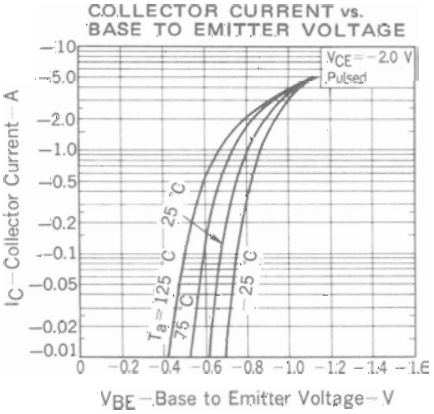
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



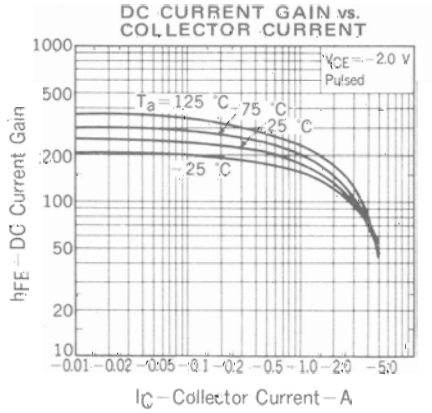
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



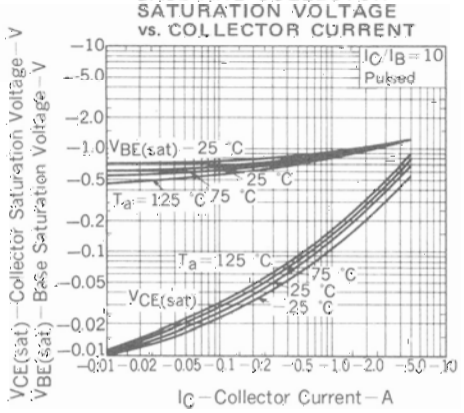
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



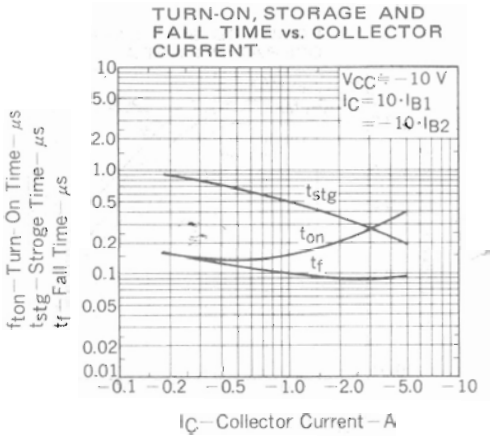
DC CURRENT GAIN vs. COLLECTOR CURRENT



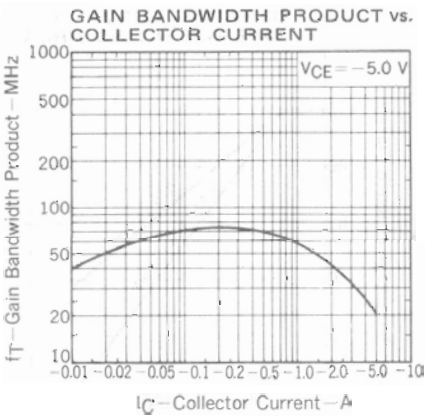
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



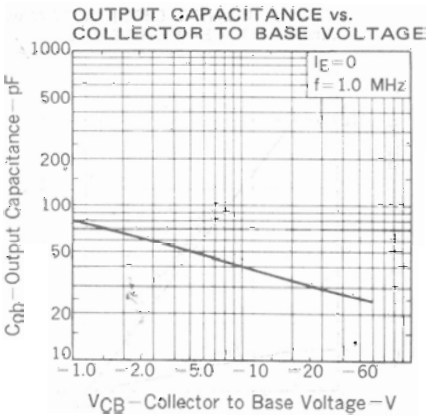
TURN-ON, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
2SC287A(B)

DESCRIPTION

The 2SC287A(B) is an NPN silicon epitaxial transistor intended for use as VHF oscillator in a tuner of a TV receiver.

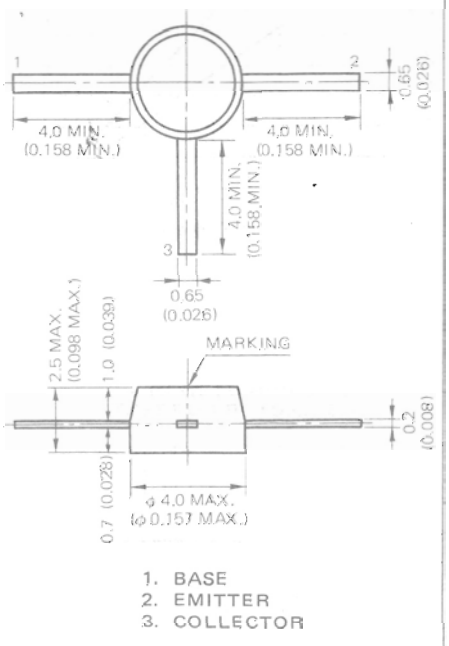
The device features stable oscillation and small frequency drift against any change of the supply voltage and the ambient temperature.

FEATURES

- High gain bandwidth product;
  f_T=1 100 MHz TYP.
- Low collector to base time constant;
  $C_c \cdot r_{b'b}$=10 ps TYP.
- Low output capacitance;
  C_{ob}=1.0 pF MAX.

PACKAGE DIMENSIONS

in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Currents (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	35 V
V_{CEO}	Collector to Emitter Voltage . .	15 V
V_{EBO}	Emitter to Base Voltage	4.0 V
I_C	Collector Current	20 mA
I_B	Base Current	10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	100	200		V_{CE}=10 V, I_C=5.0 mA
f_T	Gain Bandwidth Product	600	1 100		MHz	V_{CE}=10 V, I_E=−5.0 mA
C_{ob}	Output Capacitance		0.8	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
C_{rb}*	Reverse Transfer Capacitance		0.35	0.4	pF	V_{CE}=10 V, f=1.0 MHz
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		10	20	ps	V_{CE}=10 V, I_E=−5.0 mA, f=31.9 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.6	V	I_C=10 mA, I_B=1.0 mA

* The base terminal should be connected to the guard terminal of the capacitance bridge.

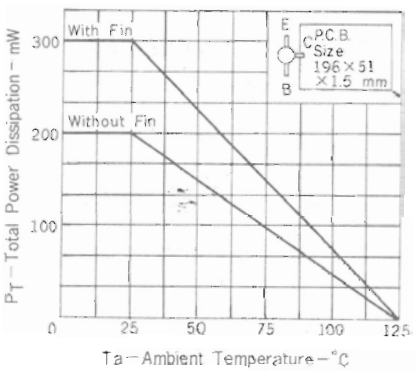
Classification of h_{FE}

Rank	F	E
Range	60 – 120	100 – 200

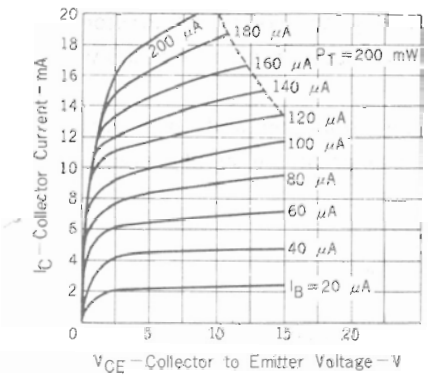
h_{FE} Test Conditions: V_{CE}=10 V, I_C=5.0 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

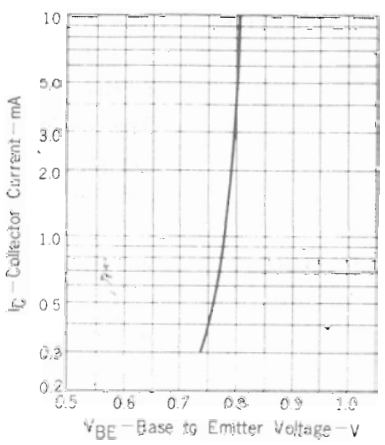
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



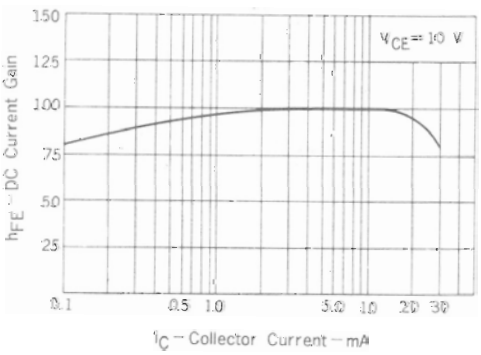
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



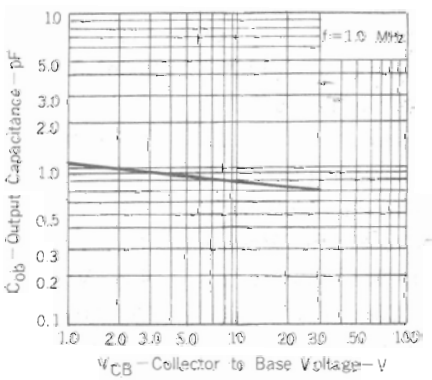
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



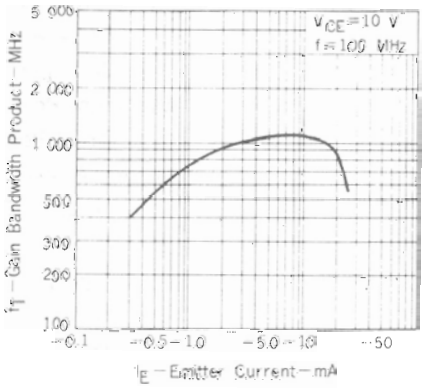
DC CURRENT GAIN vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

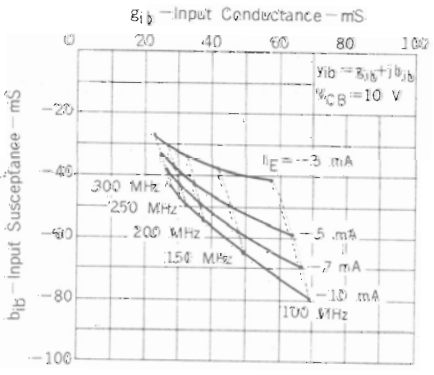


GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT

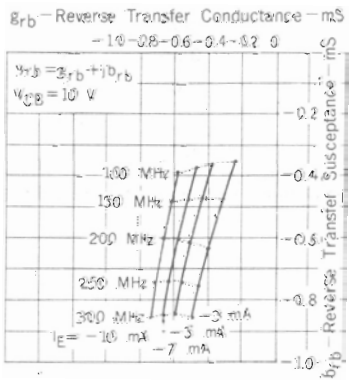


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

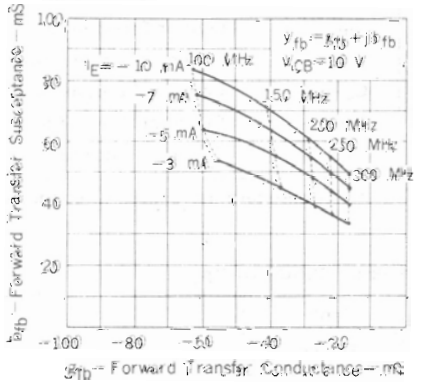
INPUT ADMITTANCE (y_{ib}) vs. FREQUENCY



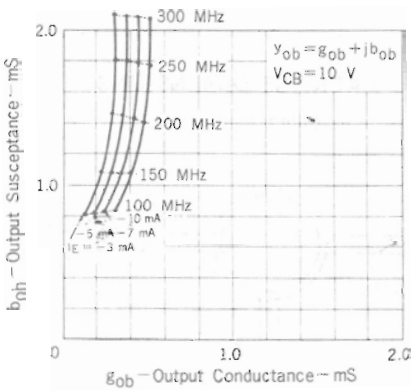
REVERSE TRANSFER ADMITTANCE (y_{rb}) vs. FREQUENCY



FORWARD TRANSFER ADMITTANCE (y_{fb}) vs. FREQUENCY



OUTPUT ADMITTANCE (y_{ob})
vs. FREQUENCY



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC288A(5·B)

DESCRIPTION

The 2SC288A(5·B) is an NPN silicon epitaxial transistor intended for use as UHF oscillator in a tuner of a TV receiver.

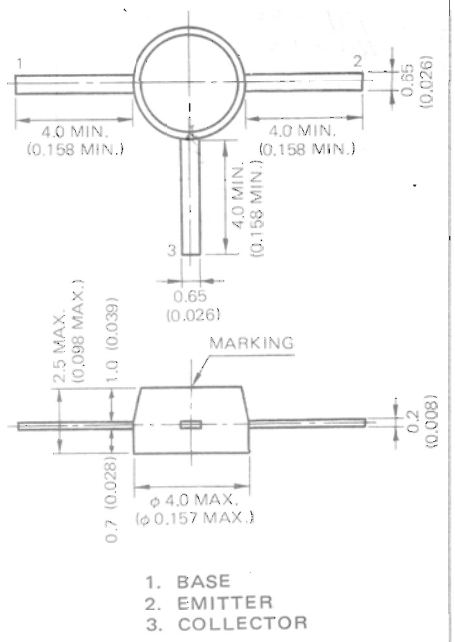
The device features stable oscillation and small frequency drift against any change of the supply voltage and the ambient temperature.

FEATURES

- High gain bandwidth product;
  f_T=1 300 MHz TYP.
- Low collector to base time constant;
  $C_c \cdot r_{b'b}$=8 ps TYP.
- Low output capacitance;
  C_{ob}=1.0 pF MAX.

PACKAGE DIMENSIONS

in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

Total Power Dissipation . . . . . .200 mW

Maximum Voltages and Currents (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage . .	15	V
V_{EBO}	Emitter to Base Voltage	4.0	V
I_C	Collector Current	20	mA
I_B	Base Current	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	100	200		V_{CE}=10 V, I_C=5.0 mA
f_T	Gain Bandwidth Product	1000	1300		MHz	V_{CE}=10 V, I_E=−5.0 mA
C_{ob}	Output Capacitance		0.8	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		8	15	ps	V_{CE}=10 V, I_E=−5.0 mA, f=31.9 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.5	V	I_C=10 mA, I_B=1.0 mA

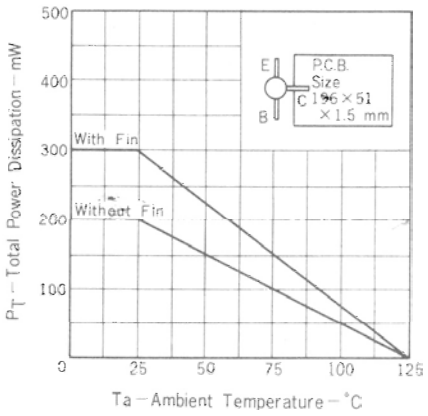
Classification of h_{FE}

Rank	F	E
Range	60 – 120	100 – 200

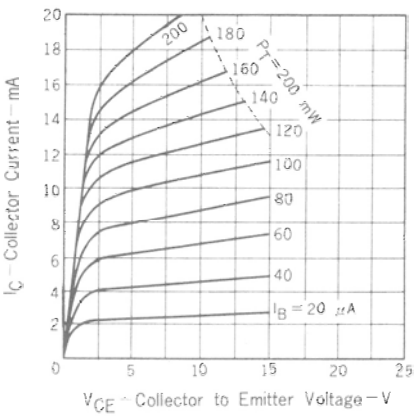
h_{FE} Test Conditions : V_{CE}=10 V, I_C=5.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

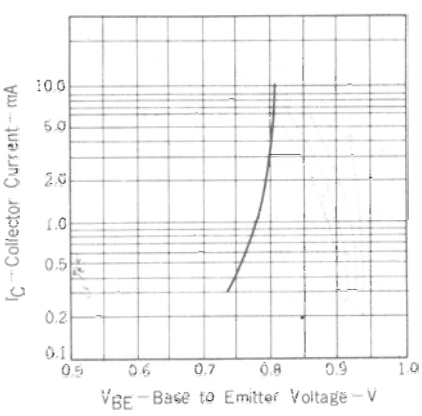
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



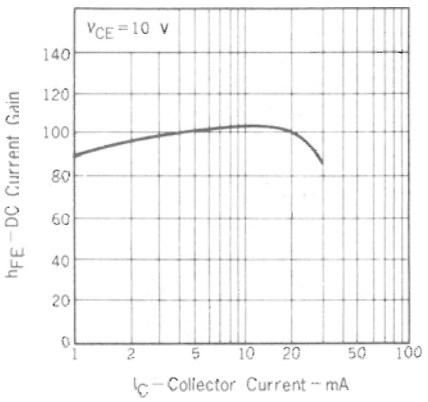
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



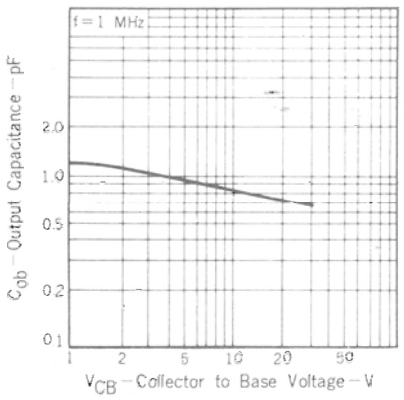
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



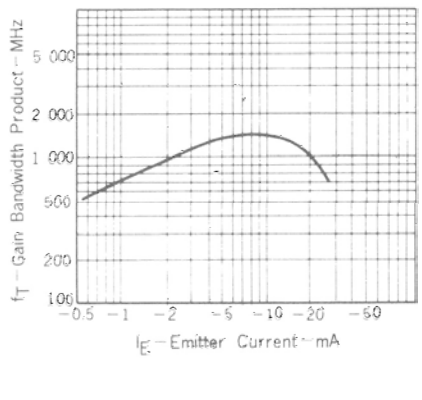
DC CURRENT GAIN vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

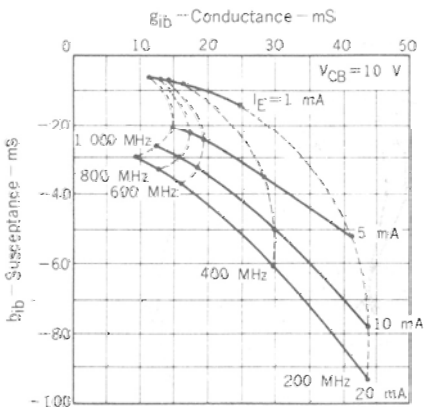


GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT

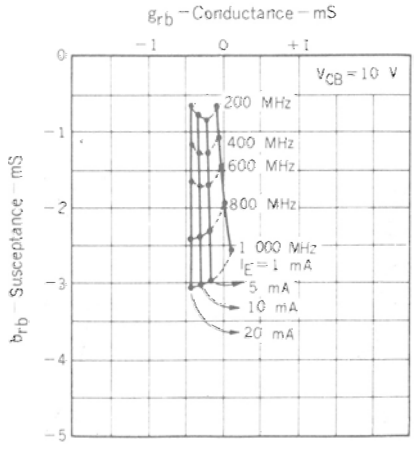


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

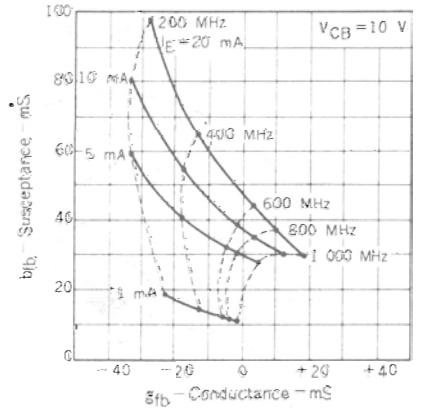
y_{ib} vs. f



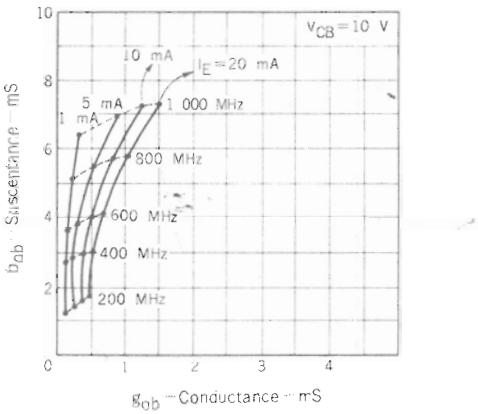
y_{rb} vs. f



y_{fb} vs. f

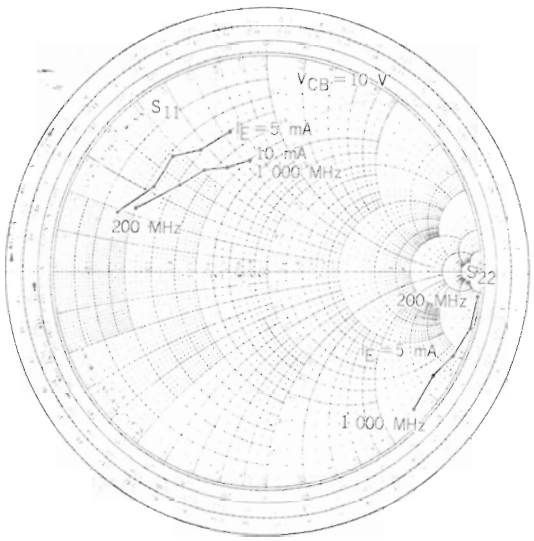


Y_{ob} vs. f

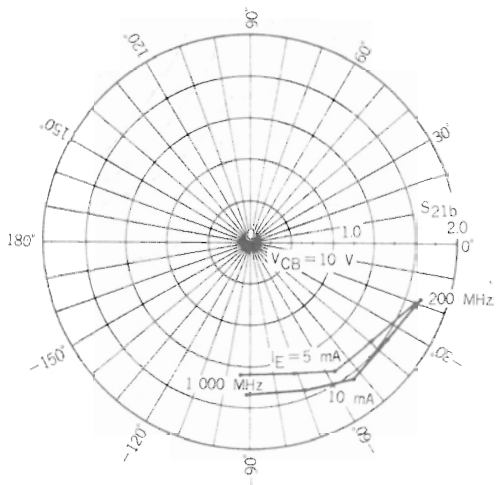


TYPICAL CHARACTERISTICS of "S" PARAMETERS

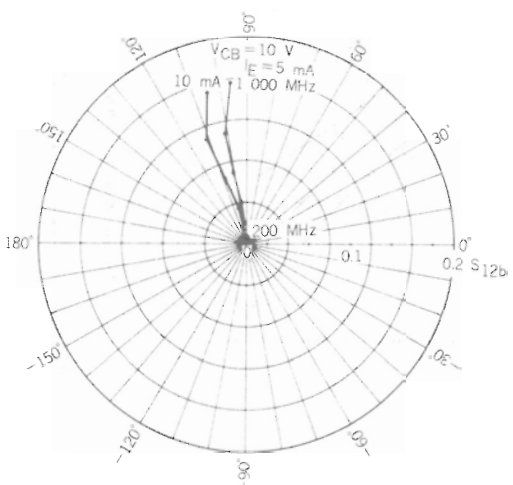
S_{11} vs. f, S_{22} vs. f



S_{21b} vs. f



S_{12b} vs. f



NEC
ELECTRON DEVICE

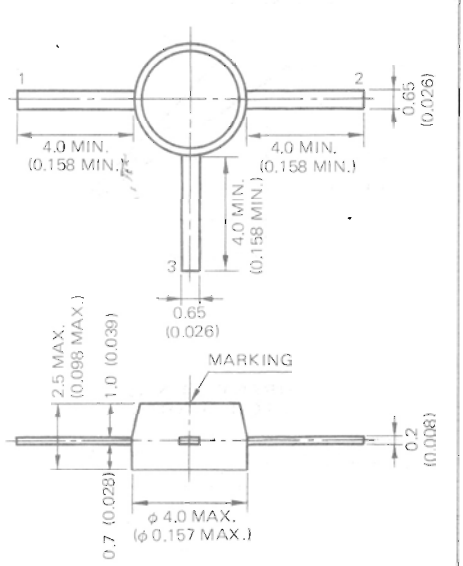
NPN SILICON TRANSISTORS
2SC605(B),2SC606(B)

DESCRIPTION The 2SC605(B), 2SC606(B) are designed for use in MIXER for VHF Tuner (2SC605(B)) and forward AGC for VHF RF Amplifier (2SC606(B)).

FEATURES

- High f_T
  TYP. 530 MHz @ V_{CE}=10 V, I_E= –3.0 mA
- Low Noise
  TYP. 2.0 dB @ f=200 MHz

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . –55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)
- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Currents (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage . . .	30	V
V_{EBO}	Emitter to Base Voltage	4.0	V
I_C	Collector Current	20	mA
I_B	Base Current	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	2SC605 (B) MIN.	2SC605 (B) TYP.	2SC605 (B) MAX.	2SC606 (B) MIN.	2SC606 (B) TYP.	2SC606 (B) MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	100	200	60	100	200		V_{CE}=10 V, I_C=3.0 mA
I_{AGC}	AGC Current				–8.0		–11	mA	f=200 MHz I_E at gain reduction of 30 dB.
f_T	Gain Bandwidth Product	350	530		400	530		MHz	V_{CE}=10 V, I_E=–3.0 mA
C_{ob}	Output Capacitance		0.55	1.0		0.55	1.0	pF	V_{CB}=10 V, f=1.0 MHz, I_E=0
G_{pe}	Power Gain	18	23		20	23		dB	f=200 MHz, I_C=3.0 mA See Test Circuit
NF	Noise Figure		2.0	4.0		2.0	3.3	dB	f=200 MHz, I_C=3.0 mA
I_{CBO}	Collector Cutoff Current			0.2			0.2	μA	V_{CB}=20 V, I_E=0

Classification of h_{FE}

Rank	M	L	K
Range	40 – 80	60 – 120	100 – 200

h_{FE} Test Conditions : V_{CE}=10 V, I_C=3.0 mA

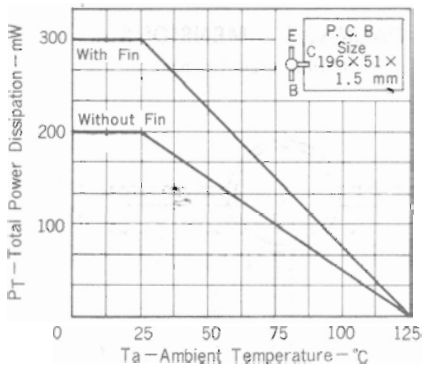
Classification of I_{AGC}

Rank	V	T
Range (mA)	–8.0 – –10.5	–9.0 – –11

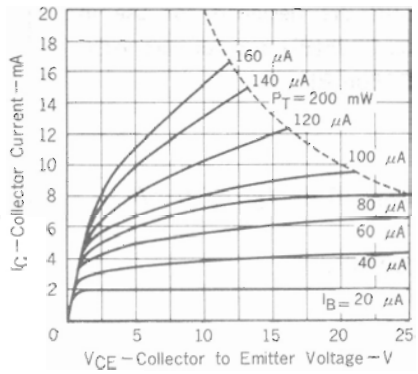
Test Conditions : f=200 MHz. I_E at gain reduction of 30 dB.

TYPICAL CHARACTERISTICS (Ta=25 °C)

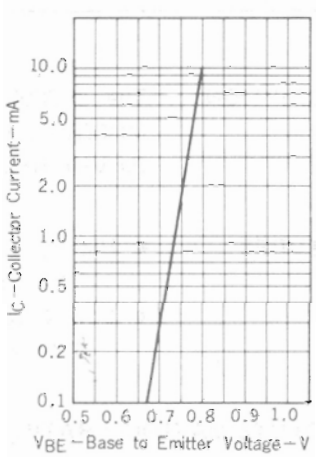
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



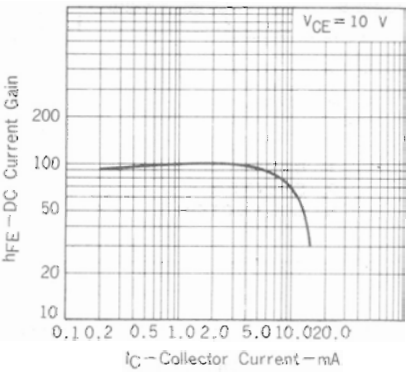
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



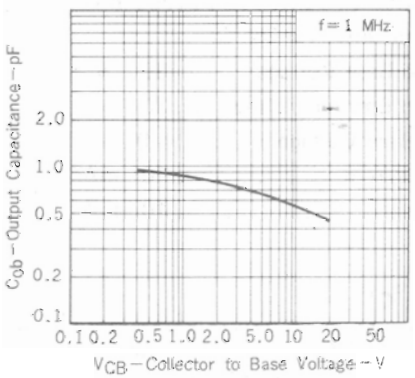
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



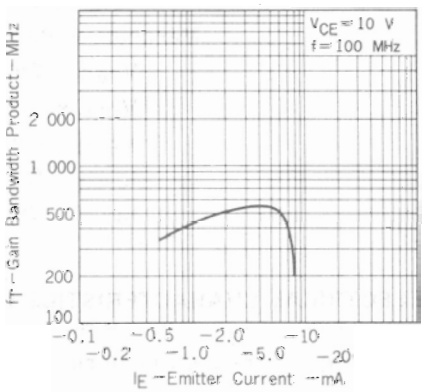
DC CURRENT GAIN vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

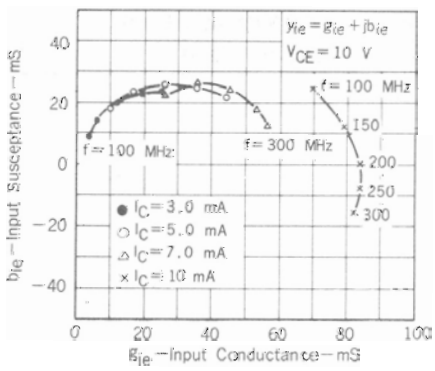


GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT

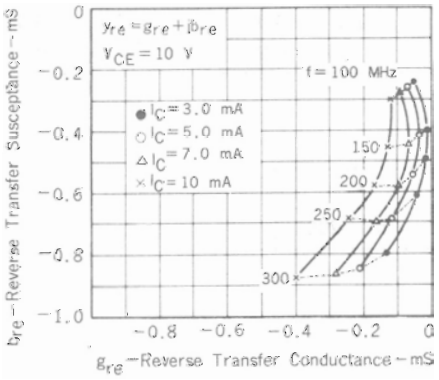


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

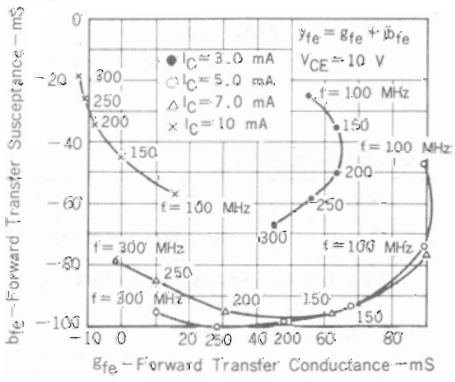
INPUT ADMITTANCE (y_{ie}) vs. FREQUENCY



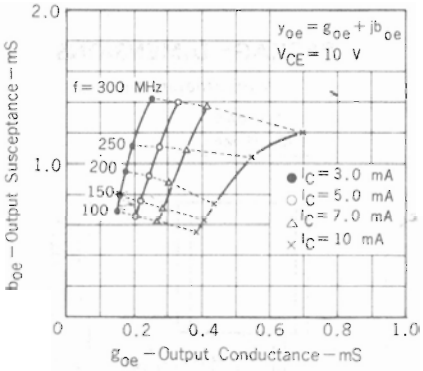
REVERSE TRANSFER ADMITTANCE (y_{re}) vs. FREQUENCY



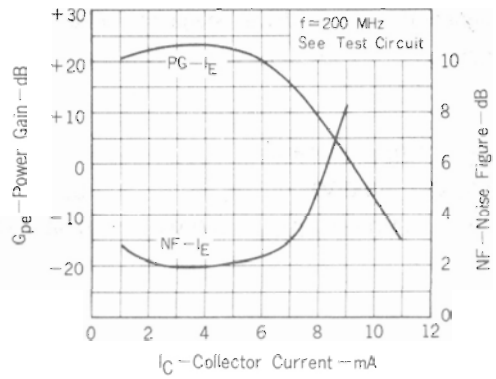
FORWARD TRANSFER ADMITTANCE (y_{fe}) vs. FREQUENCY



OUTPUT ADMITTANCE (y_{oe}) vs. FREQUENCY

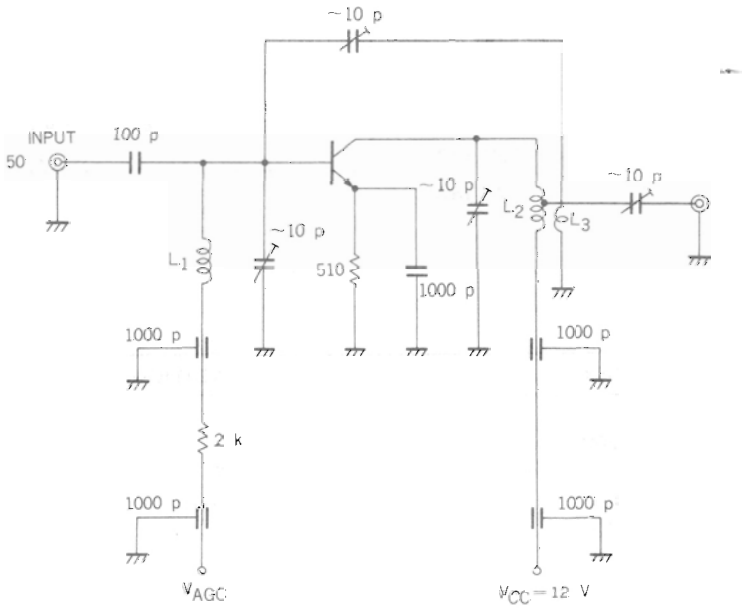


POWER GAIN AND NOISE FIGURE vs. COLLECTOR CURRENT



POWER GAIN, NOISE FIGURE AND I_{AGC} TEST CIRCUIT

f=200 MHz



L_1,L_2:0.6mm U.E.W 6.0φ 4T

L_3: 0.6mm U.E.W 6.0φ 2T

NEC
ELECTRON DEVICE

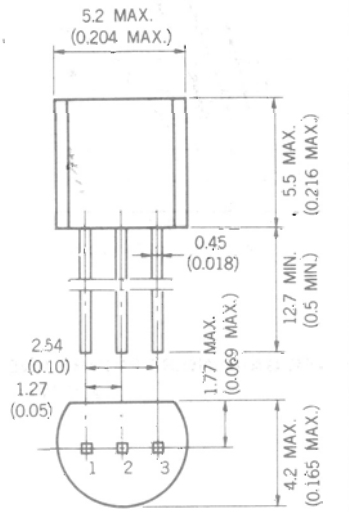
NPN SILICON TRANSISTOR
2SC923

DESCRIPTION The 2SC923 is designed for use in driver stage of AF amplifier and low speed switching.

FEATURES

- High h_{FE} and Excellent h_{FE} Linearity
  - h_{FE} (I_C = 1.0 mA, V_{CE} = 6.0 V) : 500 TYP.
  - h_{FE1} (0.1 mA) / h_{FE2} (1.0 mA) (V_{CE} = 6.0 V) : 0.94 TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 40 V
- V_{CEO} Collector to Emitter Voltage . . . . . 35 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	50	470		—	V_{CE}=6.0 V, I_C=0.1 mA
h_{FE2}	DC Current Gain	90	500	1200	—	V_{CE}=6.0 V, I_C=1.0 mA
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE}=6.0 V, I_E=−10 mA
C_{ob}	Collector to Base Capacitance		3.0	4.0	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=40 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55	0.62	0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.3	V	I_C=100 mA, I_B=10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.86	1.0	V	I_C=100 mA, I_B=10 mA

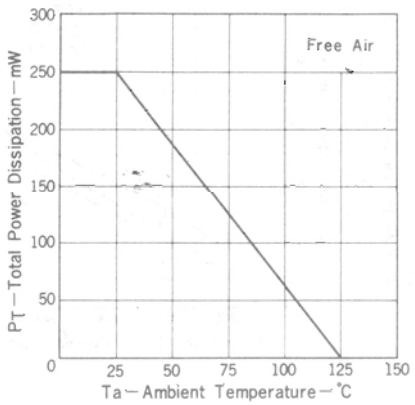
Classification of h_{FE2}

Rank	R	Q	P	K	E	U
Range	90 – 180	135 – 270	200 – 400	300 – 600	400 – 800	600 – 1200

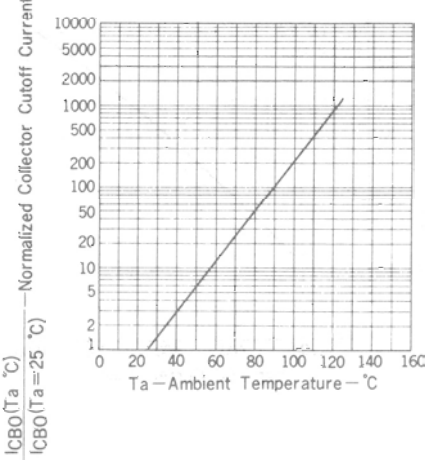
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

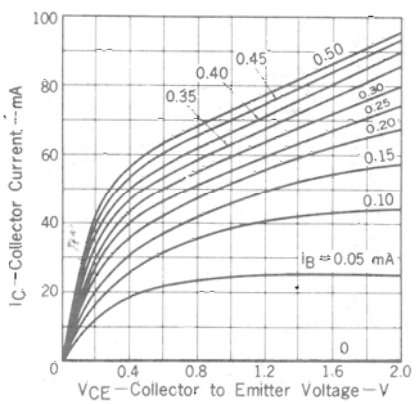
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



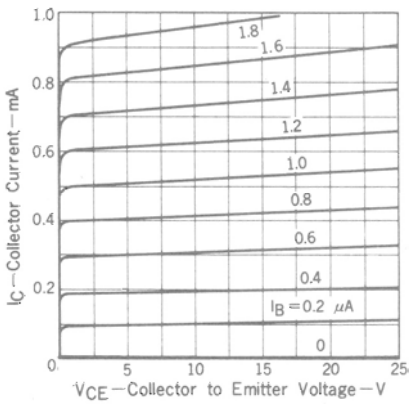
NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE



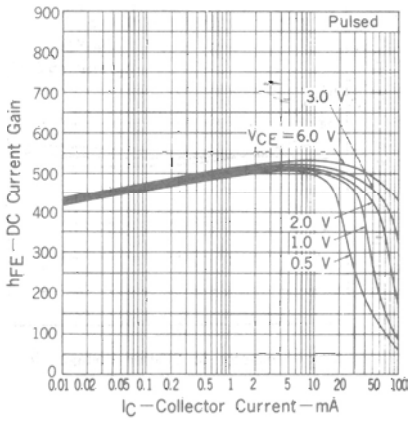
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



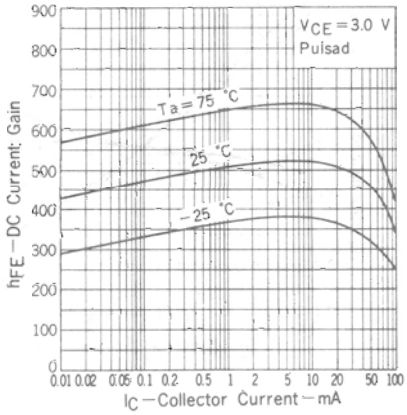
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



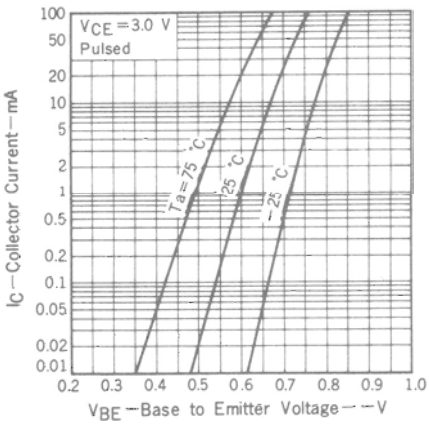
DC CURRENT GAIN vs. COLLECTOR CURRENT



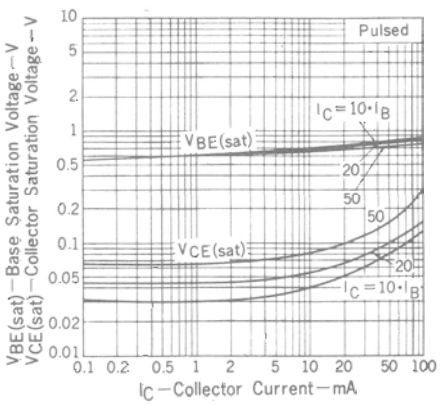
DC CURRENT GAIN vs. COLLECTOR CURRENT



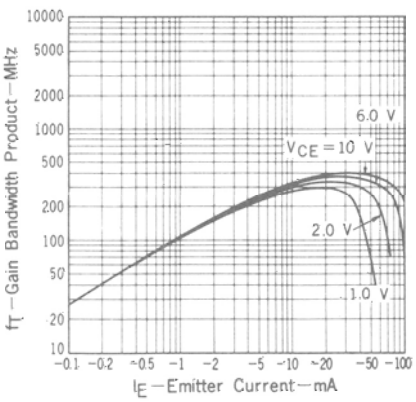
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



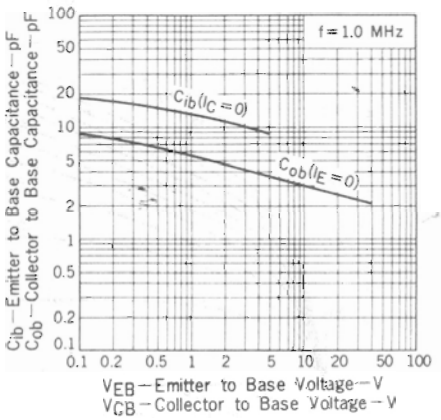
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



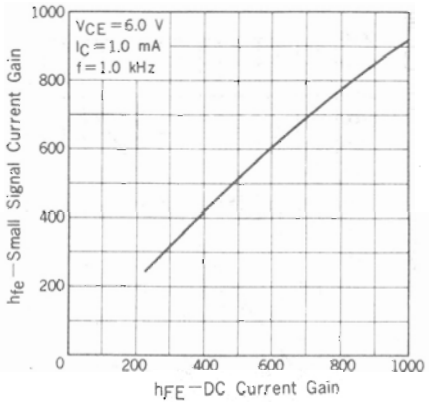
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



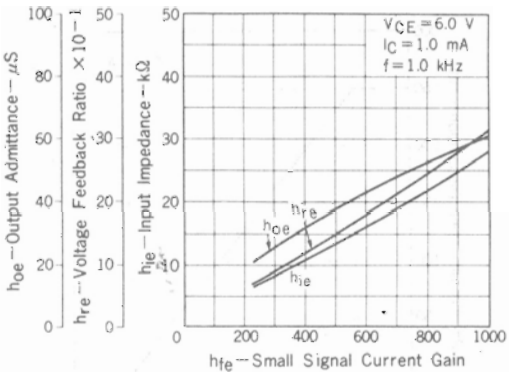
EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



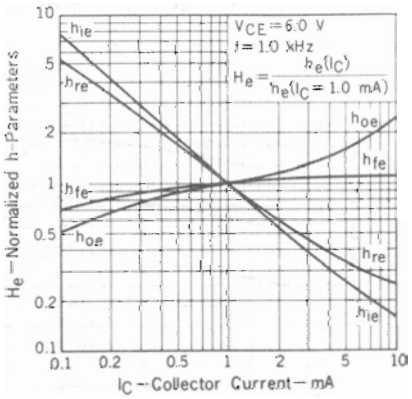
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



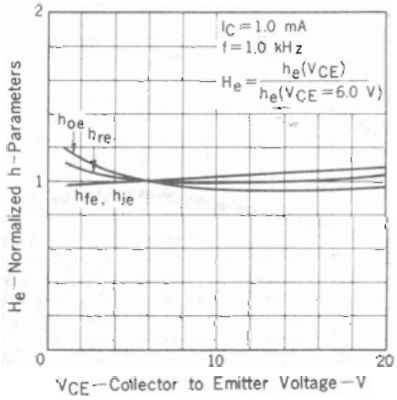
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



NEC
ELECTRON DEVICE

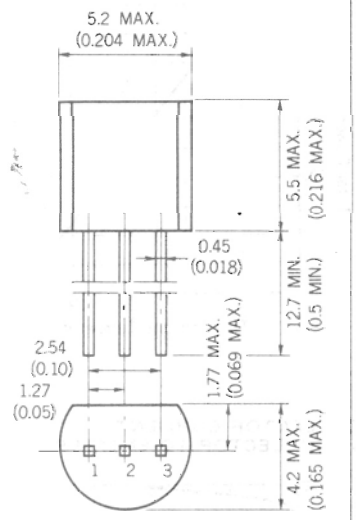
NPN SILICON TRANSISTOR
2SC945

DESCRIPTION The 2SC945 is designed for use in driver stage of AF amplifier and low speed switching.

FEATURES

- High Voltage LV_{CEO} : 50 V MIN.
- Excellent h_{FE} Linearity
  h_{FE1} (0.1 mA)/h_{FE2} (1.0 mA) : 0.92 TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC 43B
JEDEC : TO 92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	50	185			V_{CE}=6.0 V, I_C=0.1 mA
h_{FE2}	DC Current Gain	90	200	600		V_{CE}=6.0 V, I_C=1.0 mA
NF	Noise Figure		0.8	15	dB	V_{CE}=6.0 V, I_C=0.1 mA, R_G=2.0 kΩ, f=1.0 kHz
f_T	Gain Bandwidth Product	150	250	450	MHz	V_{CE}=6.0 V, I_E=−10 mA
C_{ob}	Collector to Base Capacitance		3.0	4.0	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55	0.62	0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.3	V	I_C=100 mA, I_B=10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.86	1.0	V	I_C=100 mA, I_B=10 mA

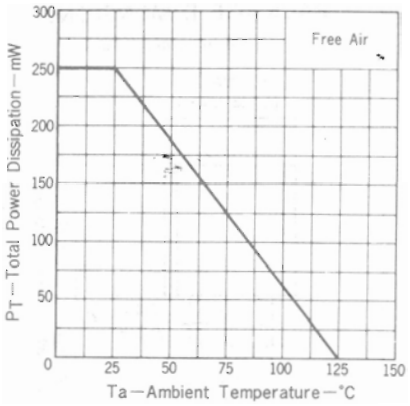
Classification of h_{FE2}

Rank	R	Q	P	K
Range	90 − 180	135 − 270	200 − 400	300 − 600

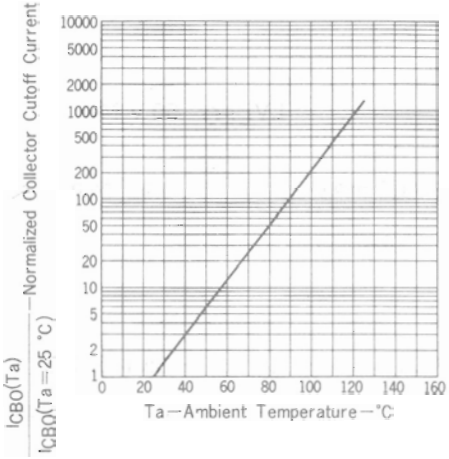
h_{FE2} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

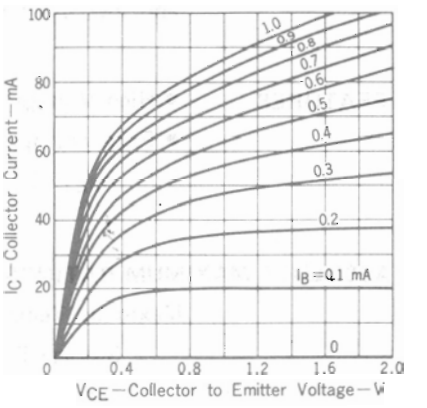
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



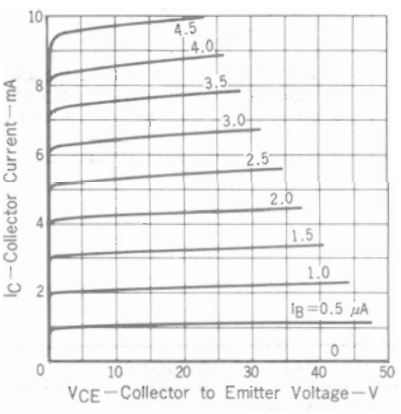
NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE



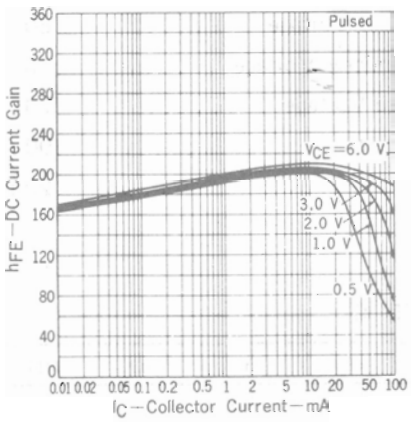
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



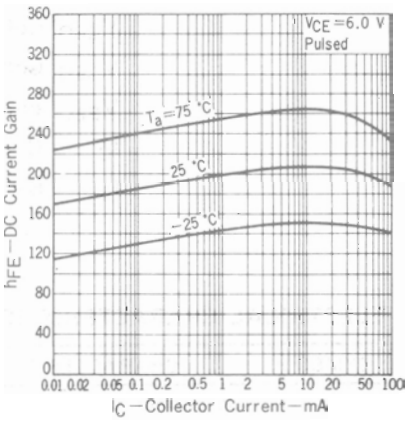
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



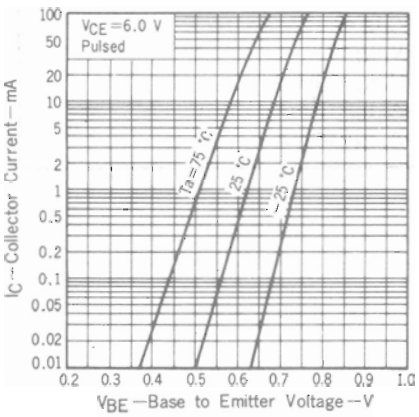
DC CURRENT GAIN vs. COLLECTOR CURRENT



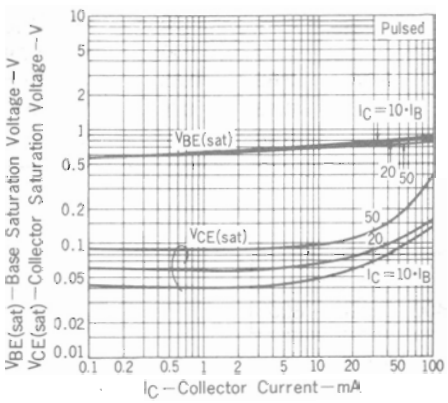
DC CURRENT GAIN vs. COLLECTOR CURRENT



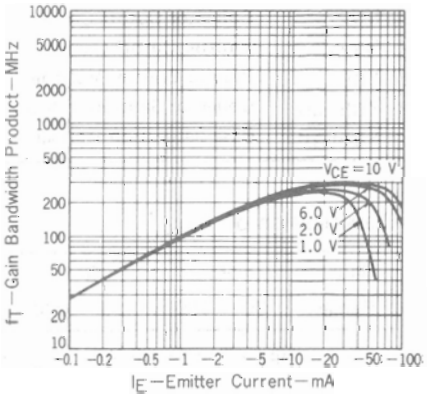
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



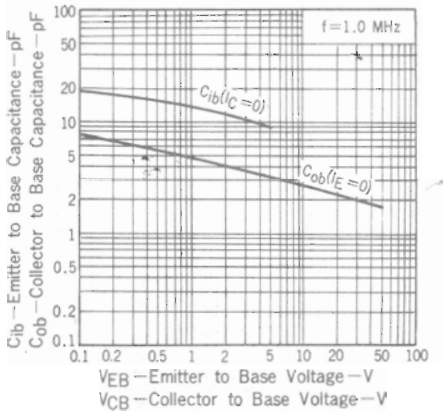
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



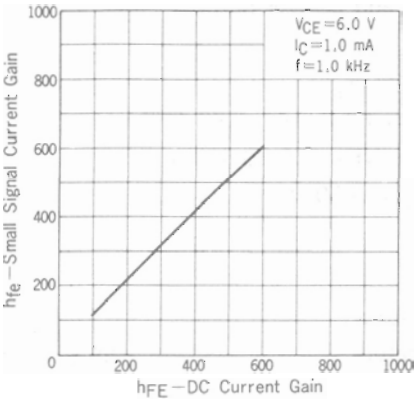
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



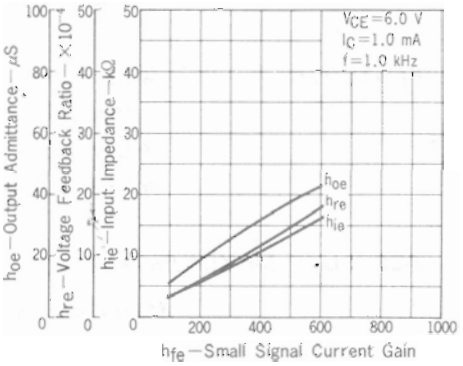
EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



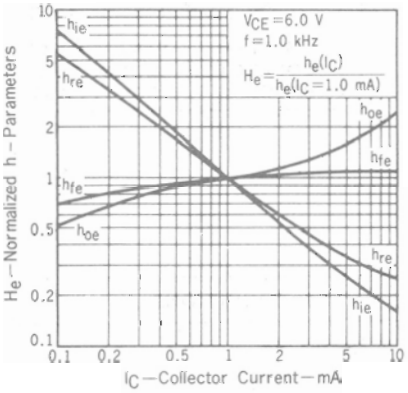
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



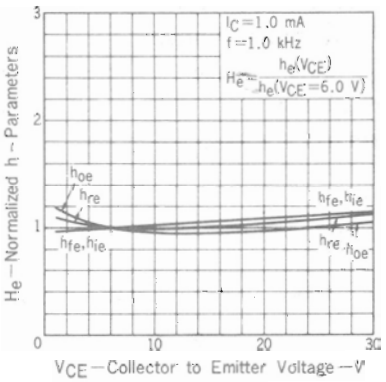
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



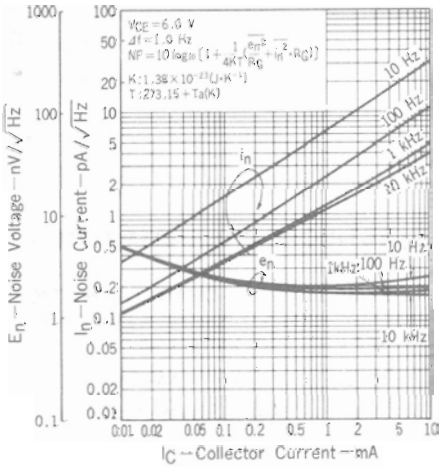
NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



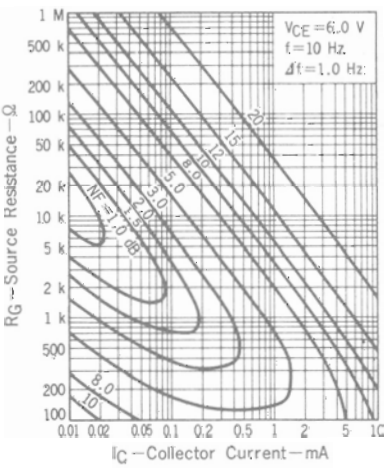
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



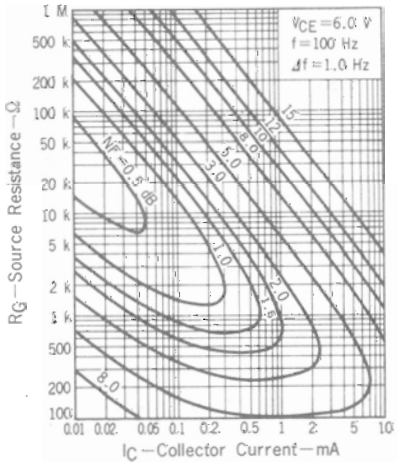
E_n AND I_n vs. COLLECTOR CURRENT



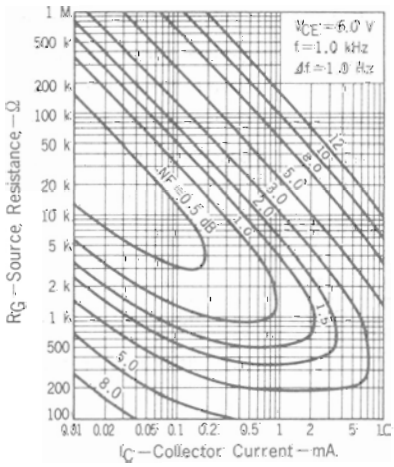
NOISE FIGURE MAP 1



NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC945(L)

DESCRIPTION

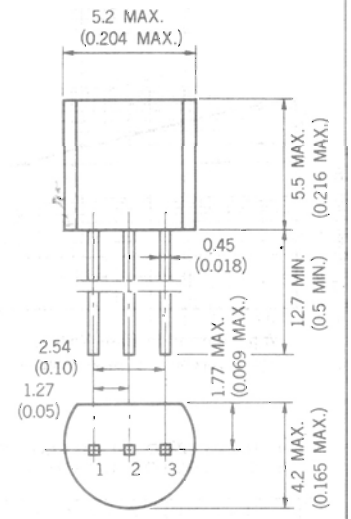
The 2SC945(L) is designed for use in an AF amplifier of low level low noise and general purpose.

FEATURES

- Excellent h_{FE} Linearity
  (h_{FE1}(0.1 mA)/h_{FE2}(1.0 mA): 0.92 TYP.)
- Low Noise Figure (NF_1: 2.5 dB TYP.)
- High Voltage (V_{CEO} > 50 V)

PACKAGE DIMENSIONS

in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	50	185		–	V_{CE}=6.0 V, I_C=0.1 mA
h_{FE2}	DC Current Gain	90	200	600	–	V_{CE}=6.0 V, I_C=1.0 mA
NF_1	Noise Figure (h_{FE2} Rank K, Q)		2.5	20	dB	V_{CE}=6.0 V, I_C=0.3 mA, R_G=10 kΩ, f=100 Hz
NF_2	Noise Figure		1.2	20	dB	V_{CE}=6.0 V, I_C=0.3 mA, R_G=2.0 kΩ, f=100 Hz
f_T	Gain Bandwidth Product	150	250	450	MHz	V_{CE}=6.0 V, I_E=−10 mA
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55	0.62	0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.30	V	I_C=100 mA, I_B=10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.86	1.00	V	I_C=100 mA, I_B=10 mA

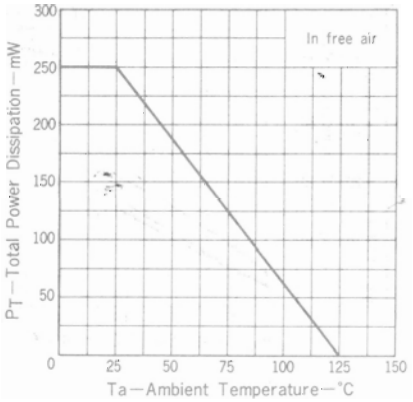
Classification of h_{FE2}

Rank	R	Q	P	K
Range	90 – 180	135 – 270	200 – 400	300 – 600

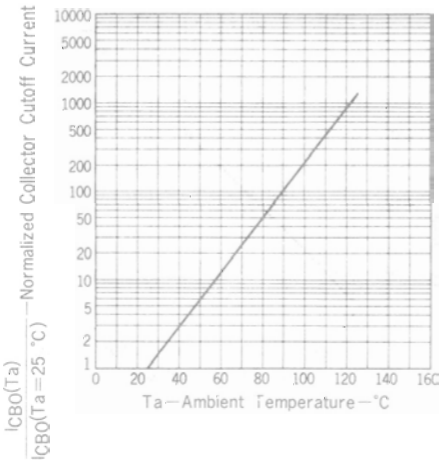
h_{FE2} Test Conditions : V_{CE}=6.0 V, I_C=1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

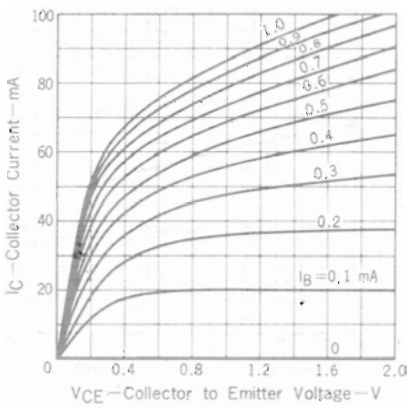
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



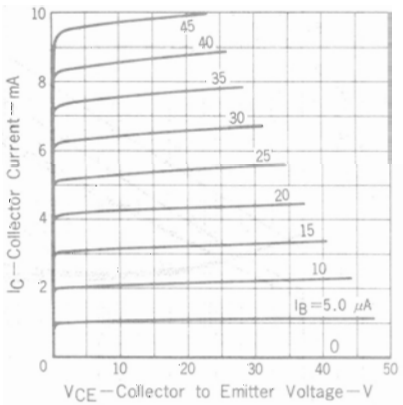
NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE



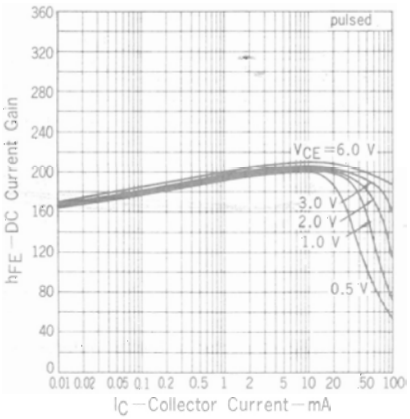
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



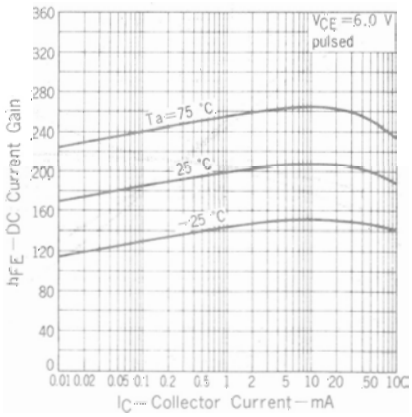
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



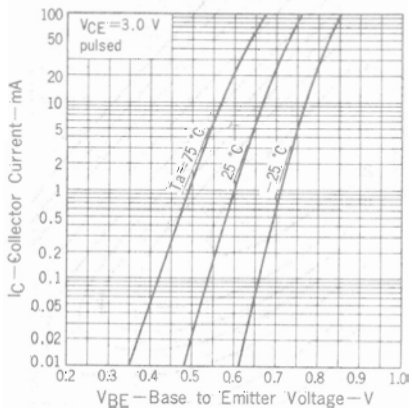
DC CURRENT GAIN vs. COLLECTOR CURRENT



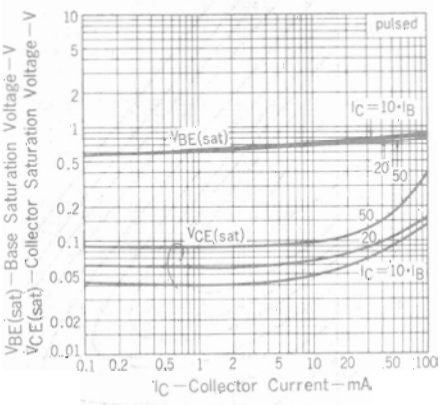
DC CURRENT GAIN vs. COLLECTOR CURRENT



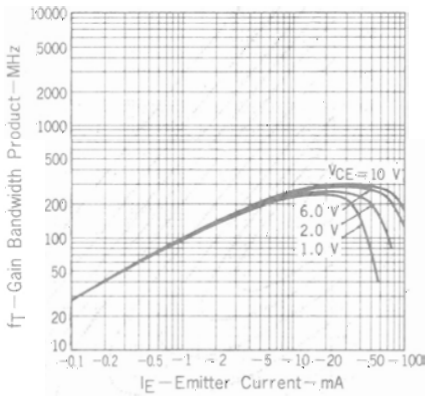
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



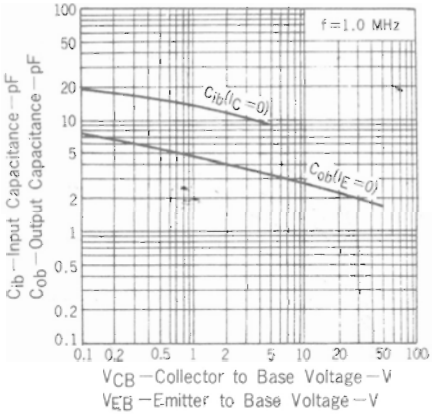
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



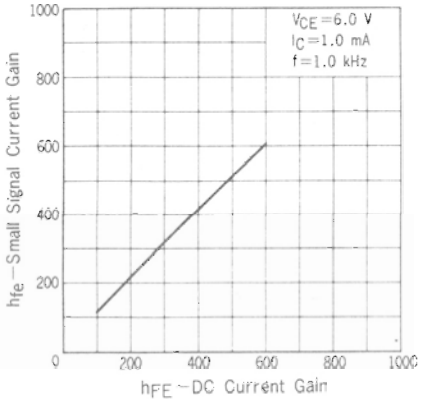
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



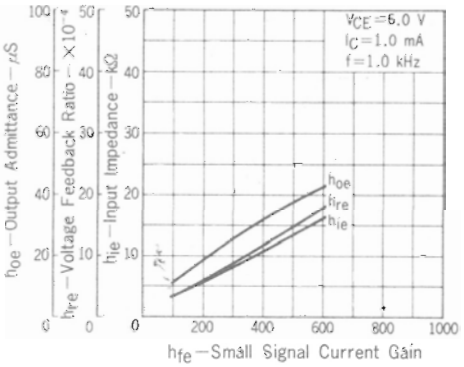
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



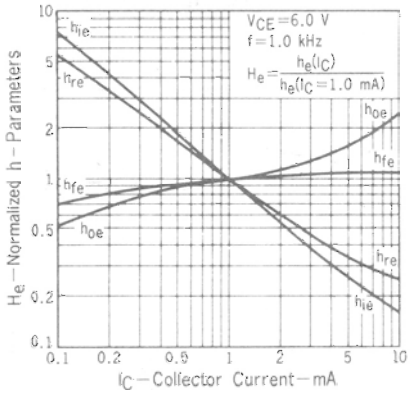
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



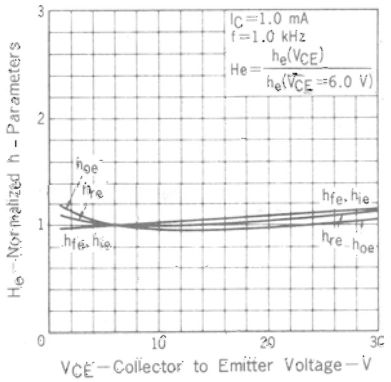
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



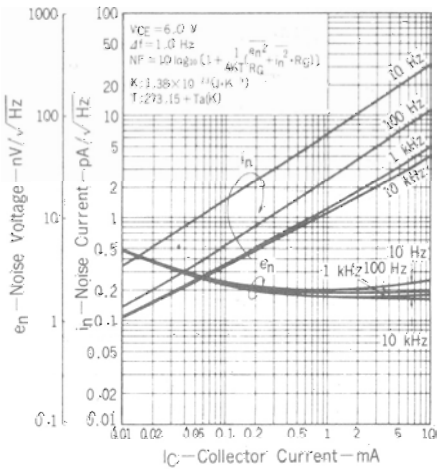
NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



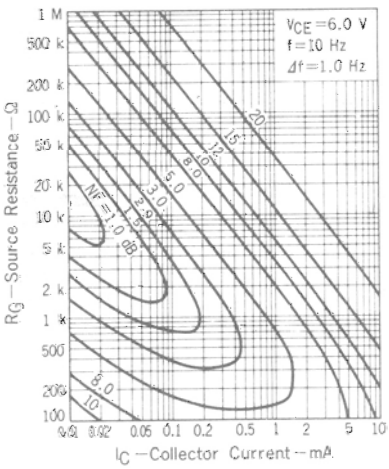
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



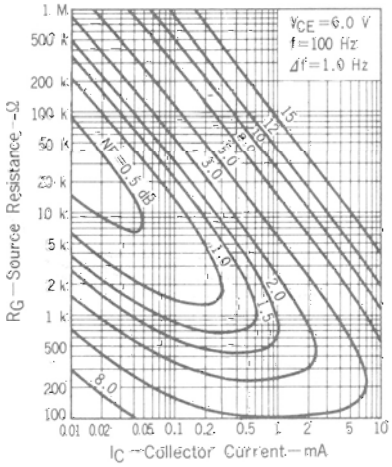
e_n AND i_n vs. COLLECTOR CURRENT



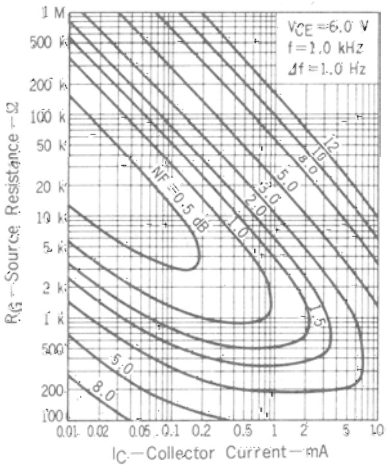
NOISE FIGURE MAP 1



NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NEC
ELECTRON DEVICE

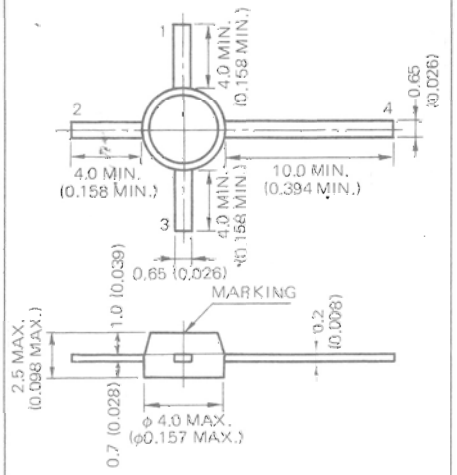
NPN SILICON TRANSISTORS
2SC1070(1), 2SC1070(2)

DESCRIPTION The 2SC1070(1) is specifically designed for UHF RF amplifier applications. The 2SC1070(2) is specifically designed for UHF mixer applications. They feature high power gain, low noise figure and excellent forward AGC characteristics in a tiny four-lead plastic package.

FEATURES

- Low NF high G_{pb}.
  NF=2.8 dB TYP. G_{pb}= 18 dB TYP. (f=900 MHz)
- Forward AGC characteristic.
- Balanced base.

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)
- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Currents (Ta=25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . . 25 V
- V_{EBO} Emitter to Base Voltage . . . . . 3.0 V
- I_C Collector Current . . . . . 20 mA
- I_B Base Current . . . . . 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	2SC1070(1) MIN.	TYP.	MAX.	2SC1070(2) MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	80	200	40	80	200	–	V_{CE}=10 V, I_C=3.0 mA
I_{AGC}	AGC Current	−8.0		−11				mA	f=200 MHz I_E at gain reduction of 30 dB.
f_T	Gain Bandwidth Product	750	1000		750	1000		MHz	V_{CE}=10 V, I_E=−3.0 mA
C_{ob}	Output Capacitance		0.55	0.8		0.55	0.8	pF	V_{CB}=10 V, f=1.0 MHz, I_E=0
G_{pb}	Power Gain	14			14			dB	V_{CB}=10 V, I_E=−3.0 mA, f=900 MHz See Test Circuit
NF	Noise Figure		2.8	4.0		2.8	4.0	dB	V_{CB}=10 V, I_E=−3.0 mA, f=900 MHz
I_{CBO}	Collector Cutoff Current			0.1			0.1	μA	V_{CB}=25 V, I_E=0

2SC1070(1) Classification of I_{AGC}

Rank	Q	P
Range (mA)	−8.0 – −10	−9.0 – −11

I_{AGC} Test Conditions : I_E for which $G_{pbAGC}=G_{pb}-30$ dB

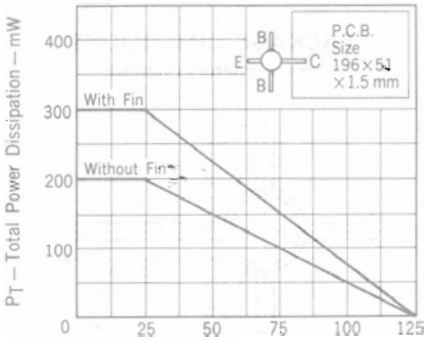
2SC1070(2) Classification of h_{FE}

Rank	F
Range	40 – 200

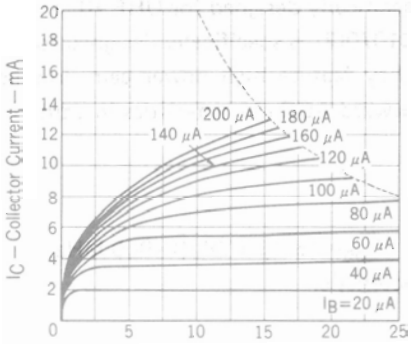
h_{FE} Test Conditions : V_{CE}= 10 V, I_C=3.0 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

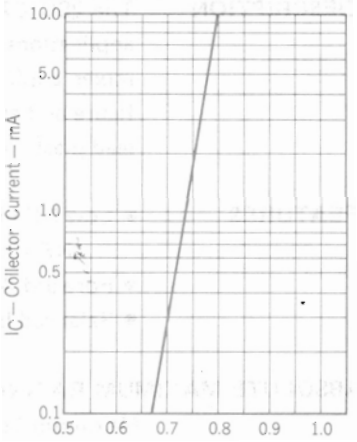
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



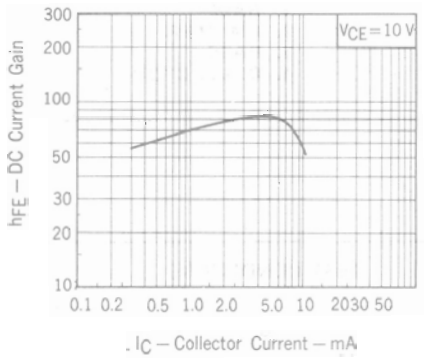
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



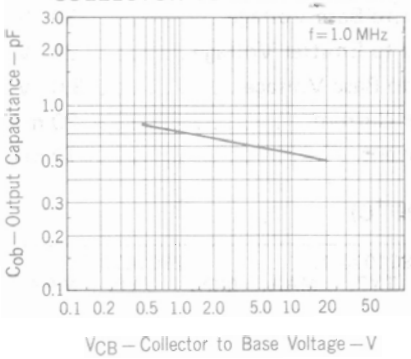
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



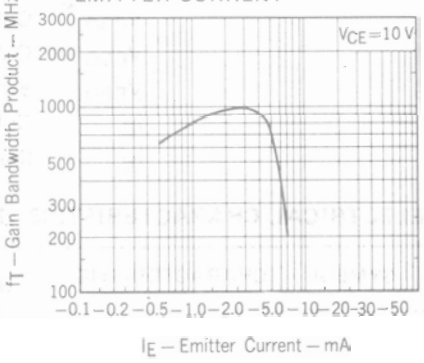
DC CURRENT GAIN vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

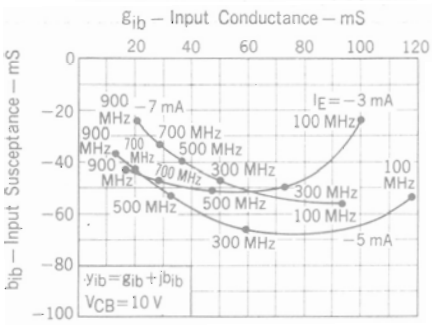


GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT

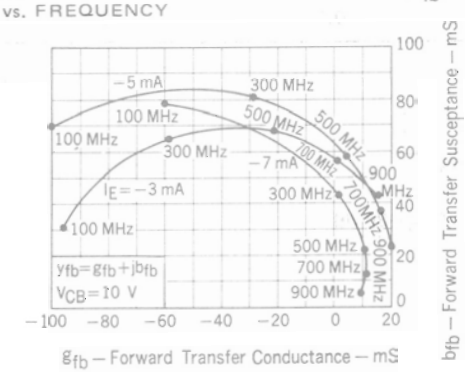


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

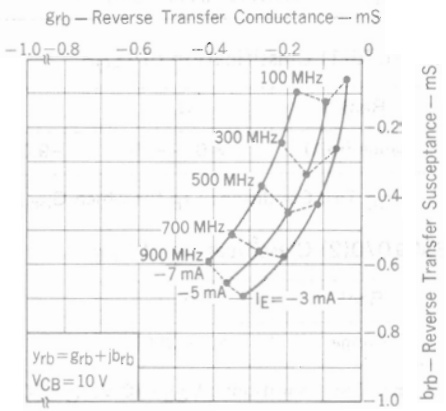
INPUT ADMITTANCE (y_{ib}) vs. FREQUENCY



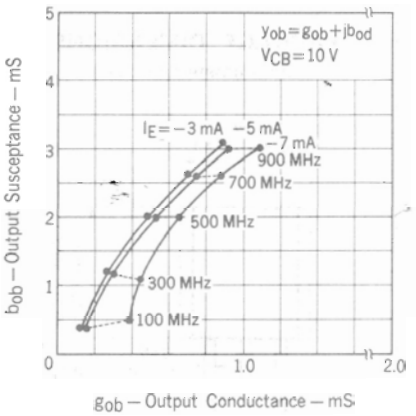
FORWARD TRANSFER ADMITTANCE (y_{fb}) vs. FREQUENCY



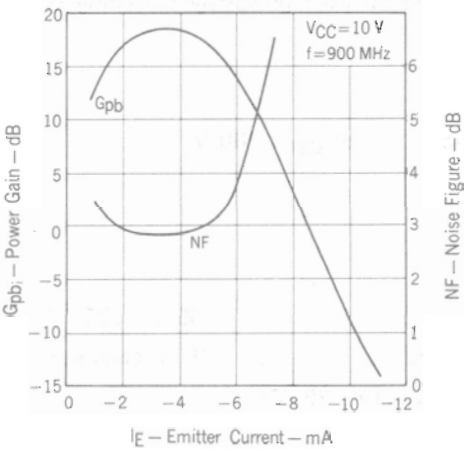
REVERSE TRANSFER ADMITTANCE (y_{rb}) vs. FREQUENCY



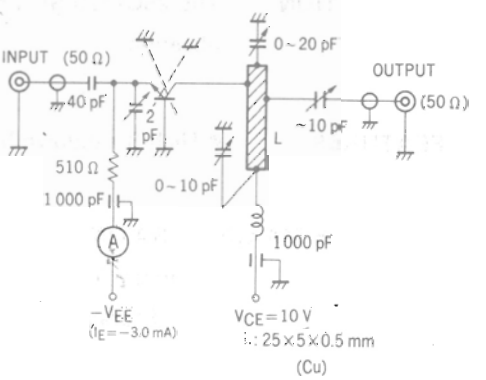
OUTPUT ADMITTANCE (Y_{ob}) vs. FREQUENCY



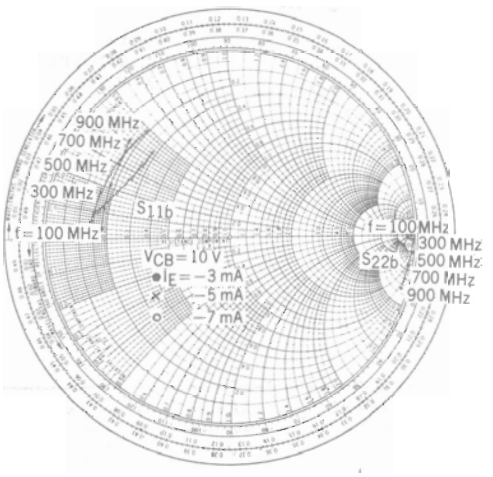
NOISE FIGURE, POWER GAIN vs. EMITTER CURRENT



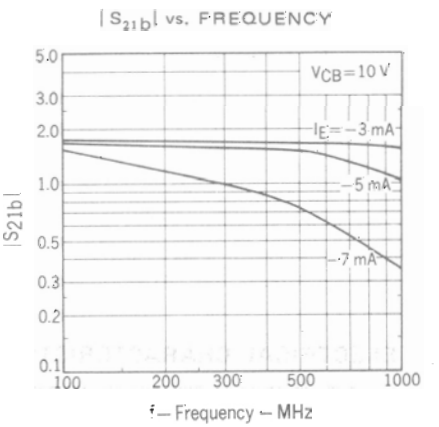
900 MHz G_{pb} & NF Test Circuit



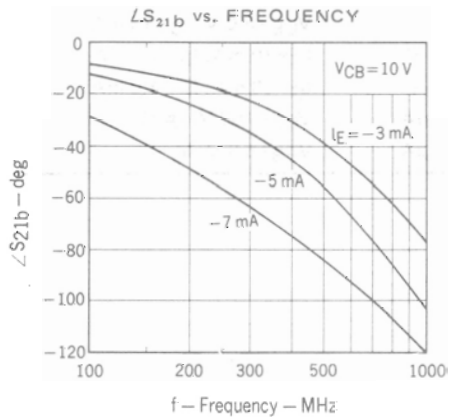
TYPICAL CHARACTERISTICS of "S" PARAMETERS



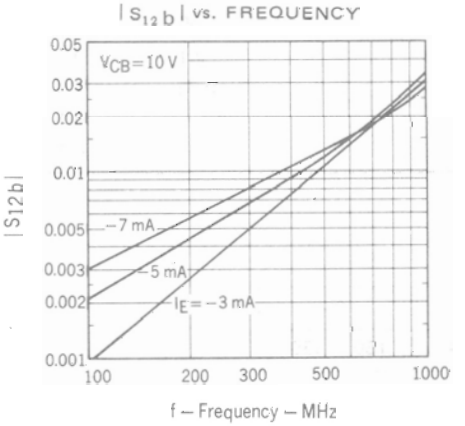
$|S_{21b}|$ vs. FREQUENCY



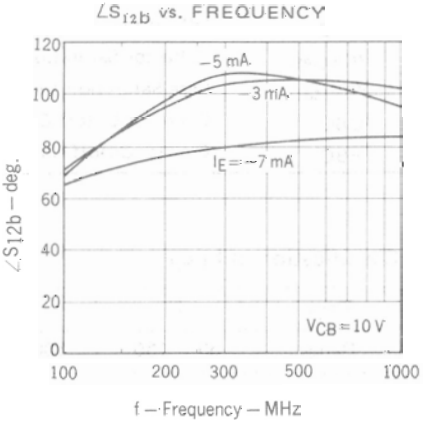
$\angle S_{21b}$ vs. FREQUENCY



$|S_{12b}|$ vs. FREQUENCY



$\angle S_{12b}$ vs. FREQUENCY



NEC
ELECTRON DEVICE

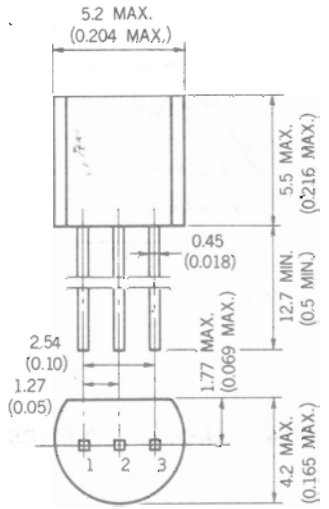
NPN SILICON TRANSISTOR
2SC1279Ⓢ

DESCRIPTION The 2SC1279Ⓢ is designed for use high voltage switching application.

FEATURES

- High Breakdown Voltage BV_{CBO}: 180 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 180 V
- V_{CEO} Collector to Emitter Voltage . . . . . 160 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 50 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
f_T	Gain Bandwidth Product		150		MHz	V_{CE}=10 V, I_E=−10 mA
C_{ob}	Output Capacitance		4.5		pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
h_{FE1}	DC Current Gain	40	90		—	V_{CE}=3.0 V, I_C=1.0 mA
h_{FE2}	DC Current Gain	50	100	330	—	V_{CE}=3.0 V, I_C=15 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.5	V	I_C=10 mA, I_B=1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.73	1.0	V	I_C=10 mA, I_B=1.0 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=100 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB}=5.0 V, I_C=0

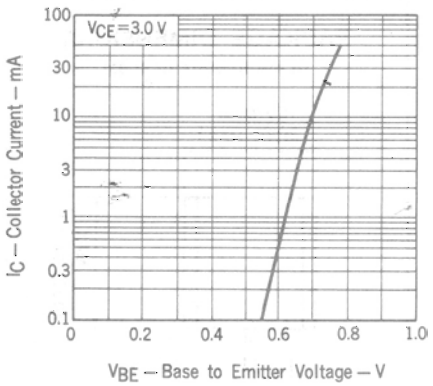
Classification of h_{FE2}

Rank	H	F	E
Range	50 – 130	100 – 200	150 – 330

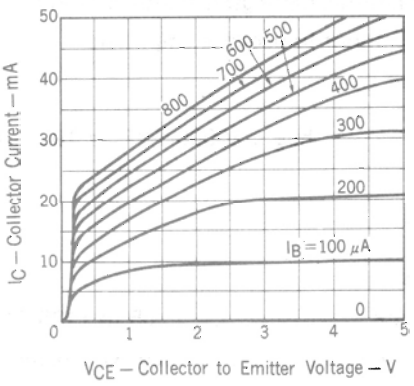
Test Conditions: V_{CE}=3.0 V, I_C=15 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

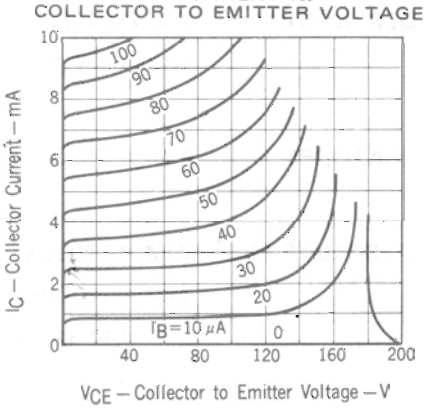
COLLECTOR CURRENT vs.
BASE TO EMITTER VOLTAGE



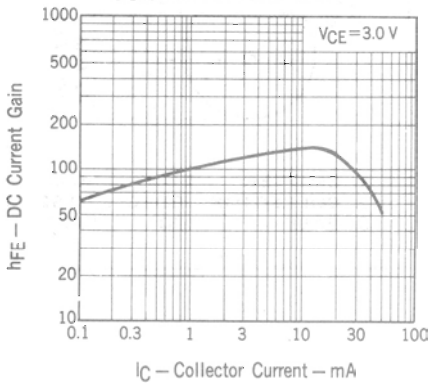
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



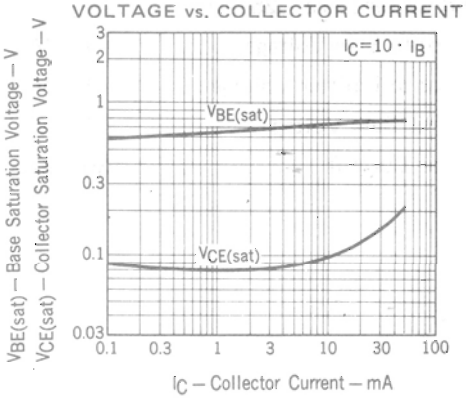
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



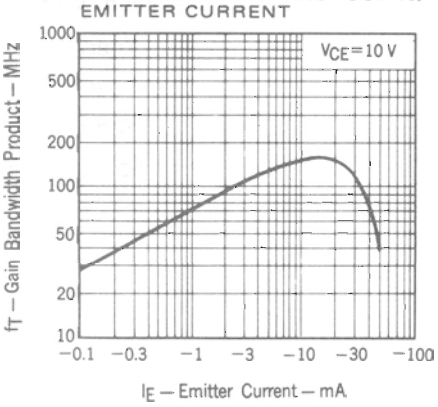
DC CURRENT GAIN vs.
COLLECTOR CURRENT



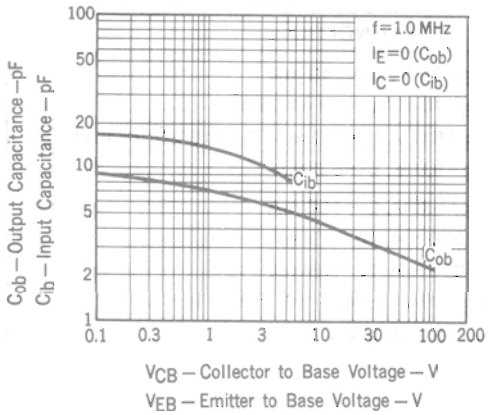
BASE AND COLLECTOR SATURATION
VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs.
EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs.
REVERSE VOLTAGE



NEC
ELECTRON DEVICE

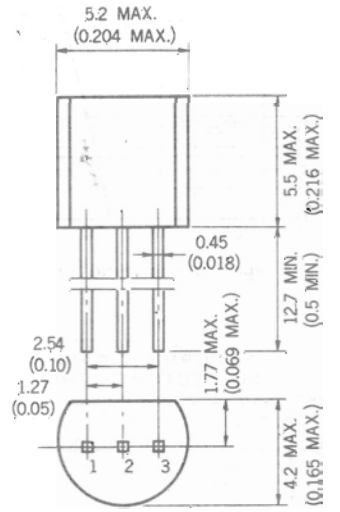
NPN SILICON DARLINGTON TRANSISTOR
2SC1280Ⓢ

DESCRIPTION The 2SC1280Ⓢ is a monolithic darlington transistor, designed for use high gain and high Input Impedance amplifier.

FEATURES

- High DC Current Gain h_{FE} : 20000 TYP. at 100 mA

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta = 25 °C)

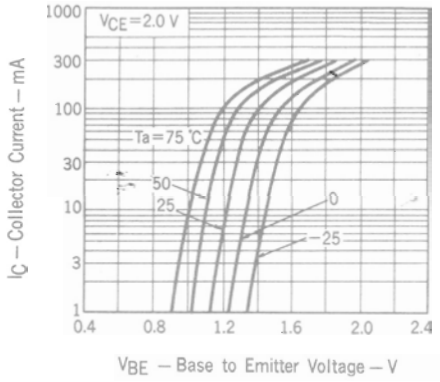
- V_{CBO} Collector to Base Voltage . . . . . 15 V
- V_{CEO} Collector to Emitter Voltage . . . . . 15 V
- V_{EBO} Emitter to Base Voltage . . . . . 10 V
- I_C Collector Current . . . . . 300 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

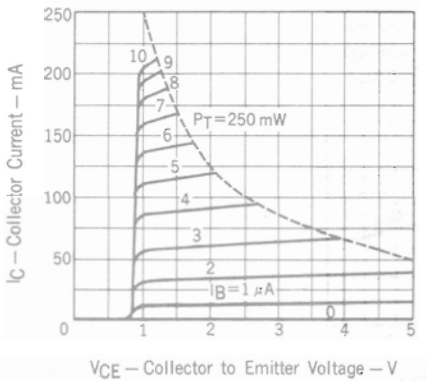
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
f_T	Gain Bandwidth Product		180		MHz	V_{CE}=10 V, I_E=−10 mA
C_{ob}	Output Capacitance		5.0		pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
NF	Noise Figure		2.5		dB	V_{CE}=5.0 V, I_C=3.0 mA, R_G=10 kΩ, f=1.0 kHz
h_{FE1}	DC Current Gain	4000	13000		—	V_{CE}=5.0 V, I_C=5.0 mA
h_{FE2}	DC Current Gain	5000	20000		—	V_{CE}=5.0 V, I_C=100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.8	1.1	V	I_C=200 mA, I_B=0.5 mA
$V_{BE(sat)}$	Base Saturation Voltage		1.4	2.0	V	I_C=200 mA, I_B=0.5 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=10 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0

TYPICAL CHARACTERISTICS (Ta=25 °C)

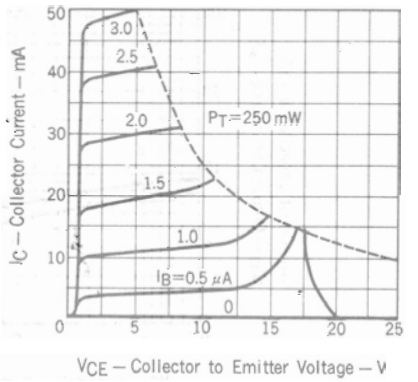
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



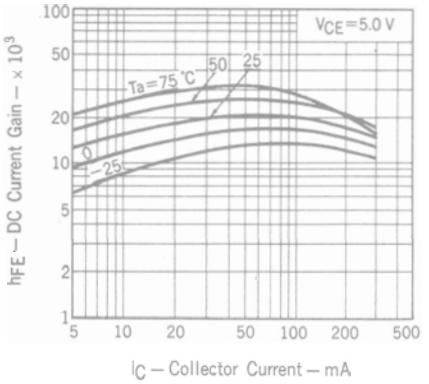
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



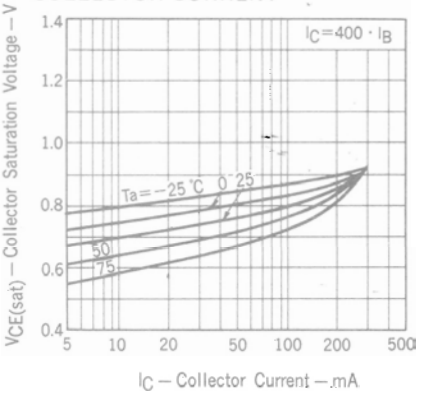
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



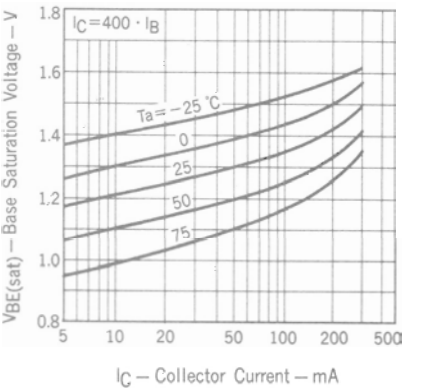
DC CURRENT GAIN vs. COLLECTOR CURRENT



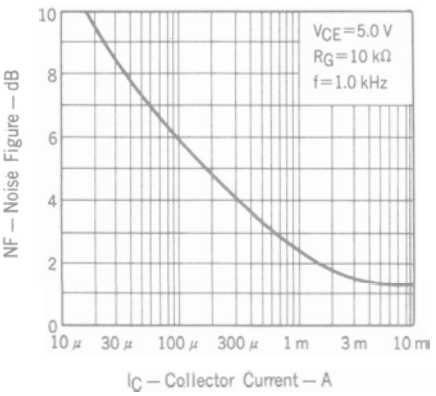
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



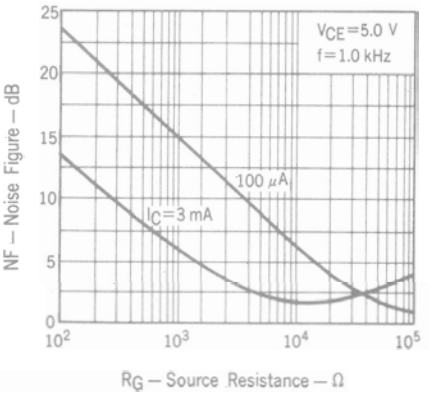
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



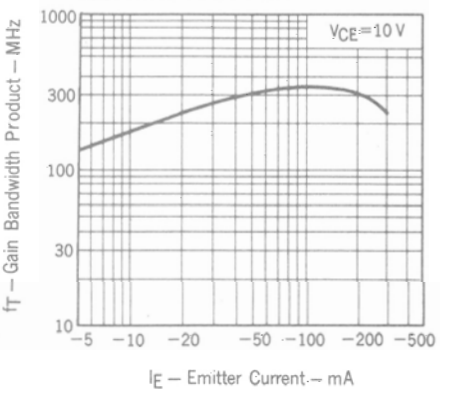
NOISE FIGURE vs. COLLECTOR CURRENT



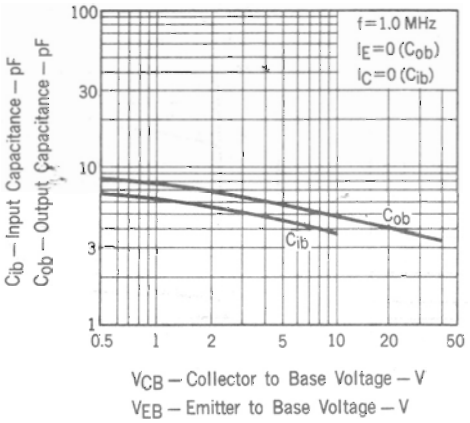
NOISE FIGURE vs. SIGNAL SOURCE RESISTANCE



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs.
REVERSE VOLTAGE



NEC
ELECTRON DEVICE

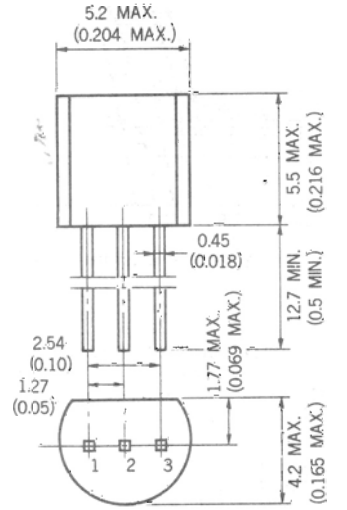
NPN SILICON DARLINGTON TRANSISTOR
2SC1280A(S)

DESCRIPTION The 2SC1280A(S) is a monolithic darlington transistor, designed for use high gain and high Input Impedance amplifier.

FEATURES

- High DC Current Gain h_{FE} : 30000 TYP. at 100 mA

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta = 25 °C)

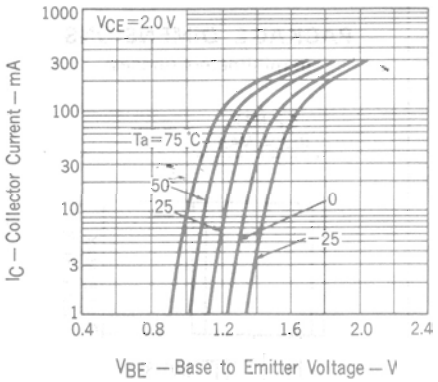
- V_{CBO} Collector to Base Voltage . . . . . 40 V
- V_{CEO} Collector to Emitter Voltage . . . . . 30 V
- V_{EBO} Emitter to Base Voltage . . . . . 10 V
- I_C Collector Current . . . . . 300 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

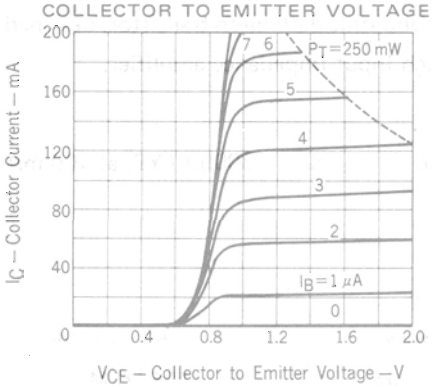
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
f_T	Gain Bandwidth Product		180		MHz	V_{CE}=10 V, I_E=−10 mA
C_{ob}	Output Capacitance		5.0		pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
NF	Noise Figure		1.5		dB	V_{CE}=5.0 V, I_C=3.0 mA, R_G=10 kΩ, f=1.0 kHz
h_{FE1}	DC Current Gain	12000	20000			V_{CE}=2.0 V, I_C=10 mA
h_{FE2}	DC Current Gain	12000	30000			V_{CE}=2.0 V, I_C=100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.76	1.0	V	I_C=100 mA, I_B=0.1 mA
$V_{BE(sat)}$	Base Saturation Voltage		1.4	2.0	V	I_C=100 mA, I_B=0.1 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=8.0 V, I_C=0

TYPICAL CHARACTERISTICS (Ta=25 °C)

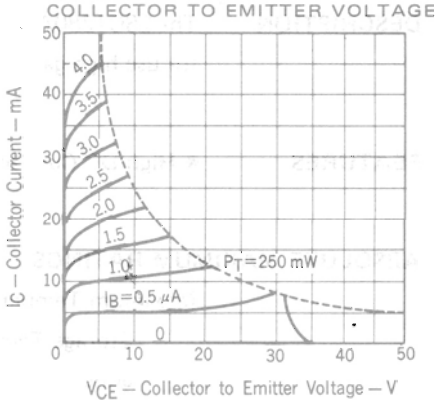
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



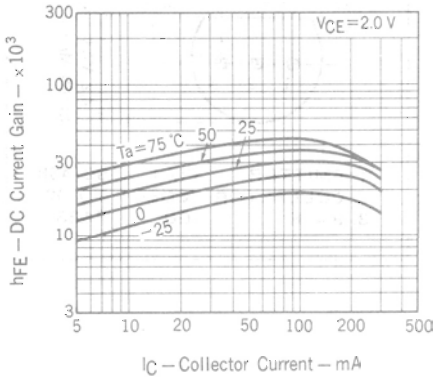
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



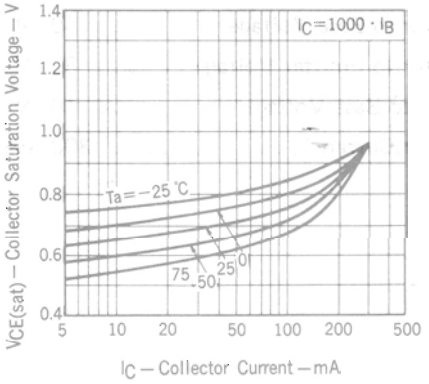
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



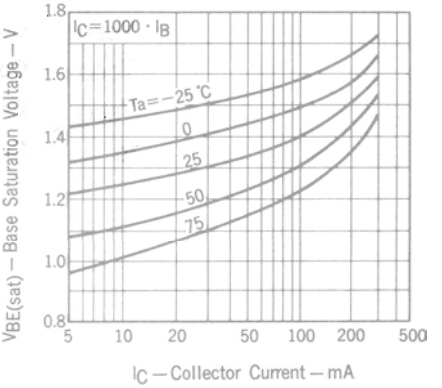
DC CURRENT GAIN vs. COLLECTOR CURRENT



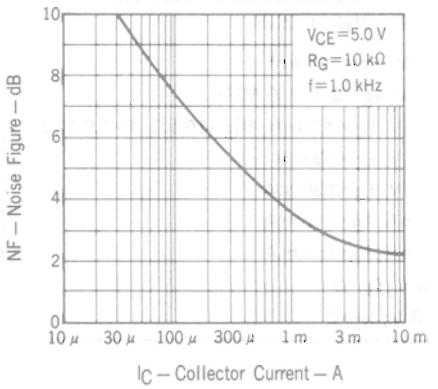
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



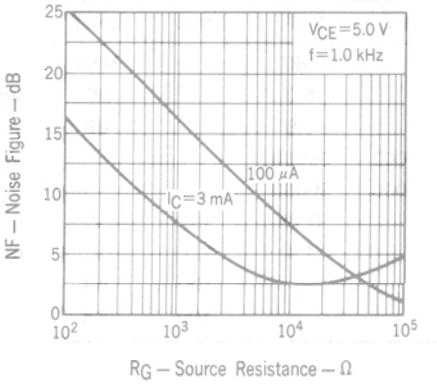
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



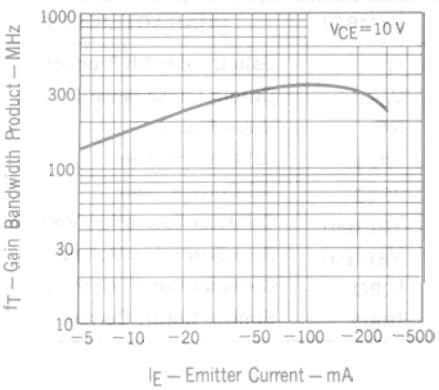
NOISE FIGURE vs. COLLECTOR CURRENT



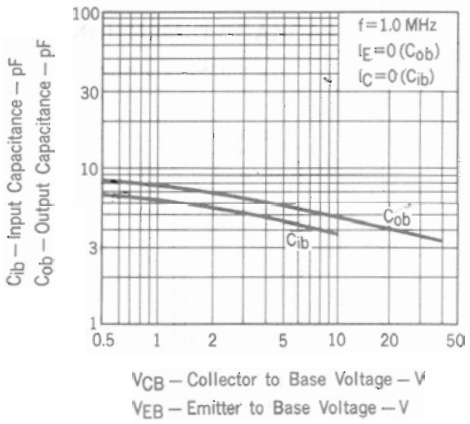
NOISE FIGURE vs. SIGNAL SOURCE RESISTANCE



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE
vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

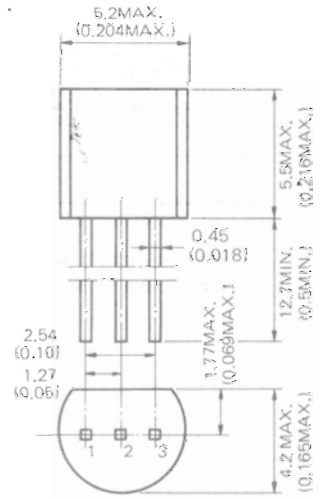
NPN SILICON TRANSISTORS
2SC1393, 2SC1394

DESCRIPTION The 2SC1393 and 2SC1394 are designed for use in VHF RF Amplifier (2SC1393) and VHF Mixer (2SC1394) for TV Tuner.

FEATURES

- Low NF high G_{pe}.
  NF=2.0 dB TYP. G_{pe}=24 dB TYP. (f=200 MHz)
- Forward AGC capability to 30 dB.
- Low feedback capacity. C_{re}=0.35 pF TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage	30	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	20	mA
I_B	Base Current	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	2SC1393			2SC1394			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
h_{FE}	DC Current Gain	40	100	180	40	100	180		V_{CE}=10 V, I_C=2.0 mA
I_{AGC}	AGC Current		−10	−12				mA	f=200 MHz, I_E at gain reduction of 30 dB.
f_T	Gain Bandwidth Product	400	700		400	700		MHz	V_{CE}=10 V, I_E=−3.0 mA
C_{re}	Feed-back Capacitance		0.35	0.5		0.35	0.5	pF	f=1.0 MHz, V_{CB}=10 V, I_E=0
G_{pe}	Power Gain	20	24		20			dB	f=200 MHz, I_C=3.0 mA
NF	Noise Figure		2.0	3.0			3.5	dB	f=200 MHz, I_C=3.0 mA
I_{CBO}	Collector Cutoff Current			0.1			0.1	μA	V_{CB}=20 V, I_E=0

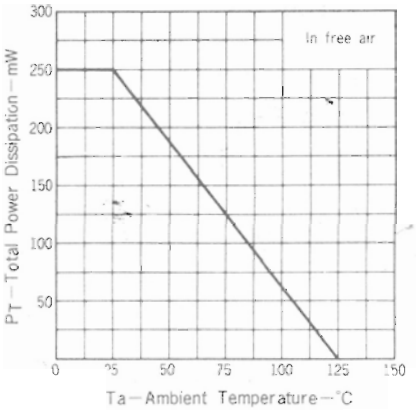
Classification of h_{FE}

Rank	M	L	K
Range	40 – 80	60 – 120	90 – 180

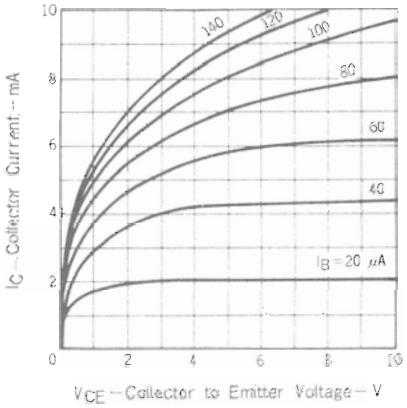
h_{FE} Test Conditions : V_{CE}=10 V, I_C=2.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

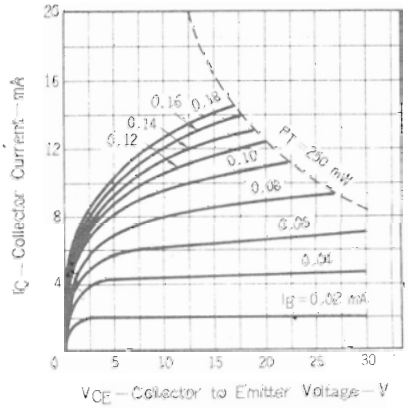
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



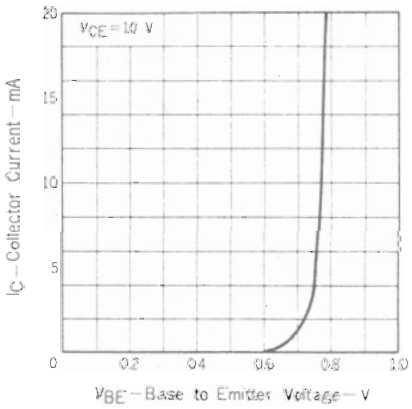
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



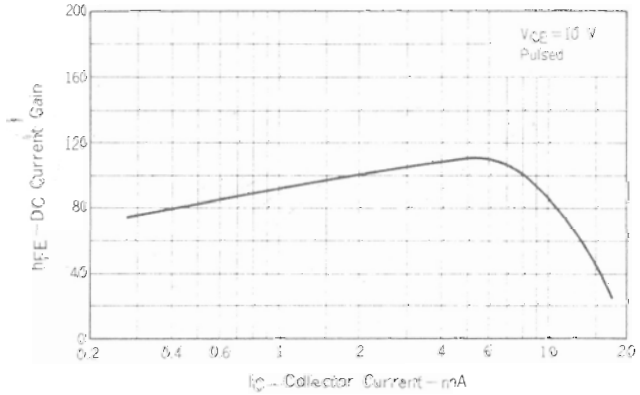
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



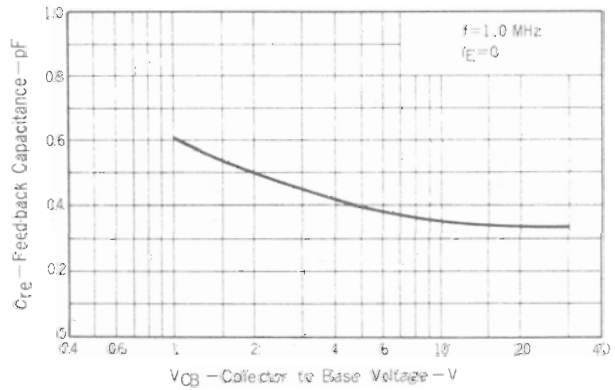
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



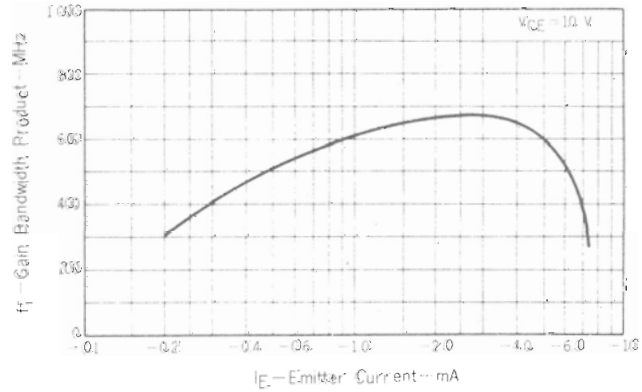
DC CURRENT GAIN vs. COLLECTOR CURRENT



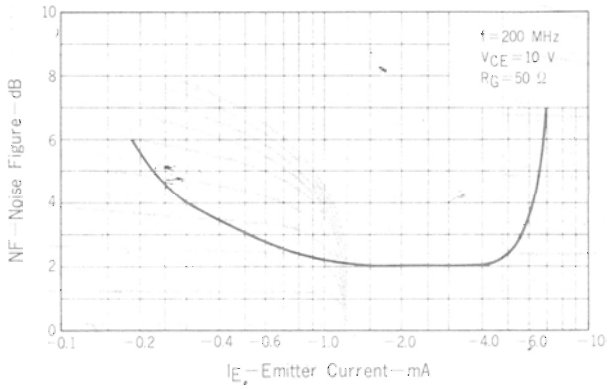
FEED-BACK CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



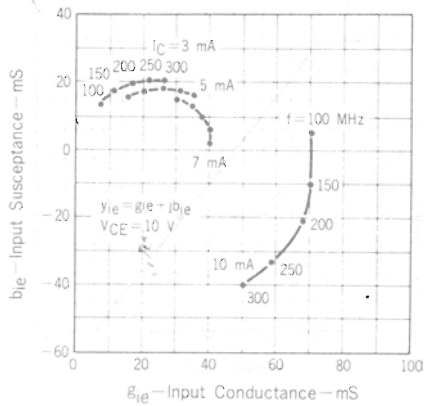
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



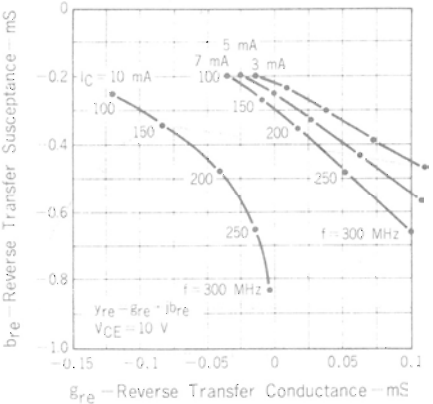
NOISE FIGURE vs. EMITTER CURRENT



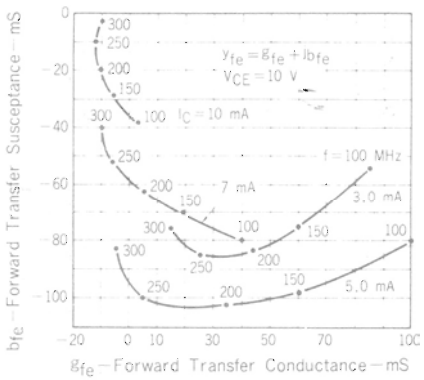
INPUT ADMITTANCE (y_{ie}) vs. FREQUENCY



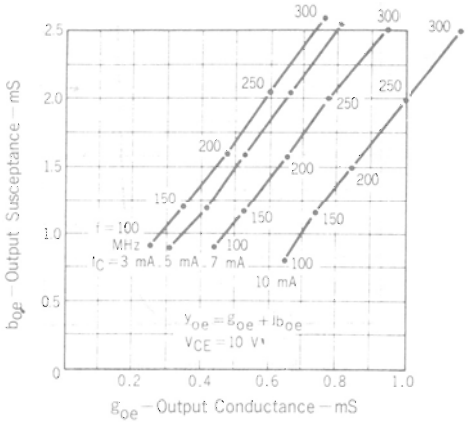
REVERSE TRANSFER ADMITTANCE (y_{re}) vs. FREQUENCY



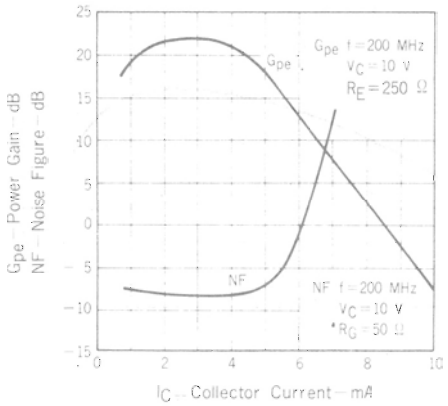
FORWARD TRANSFER ADMITTANCE (y_{fe}) vs. FREQUENCY



OUTPUT ADMITTANCE (y_{oe}) vs. FREQUENCY

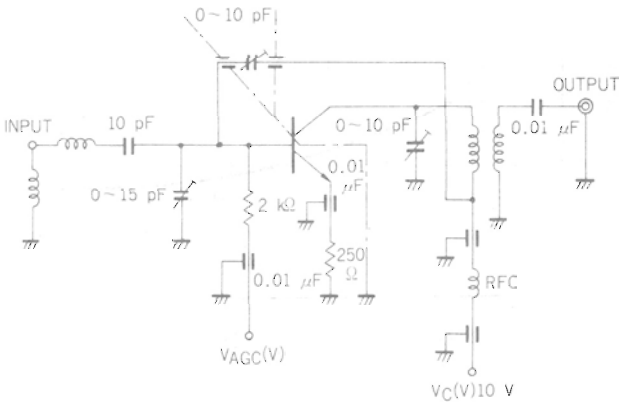


POWER GAIN AND NOISE FIGURE vs. COLLECTOR CURRENT



POWER GAIN AND NOISE FIGURE TEST CIRCUIT

f = 200 MHz, B.W = 6.0 MHz



NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC1449

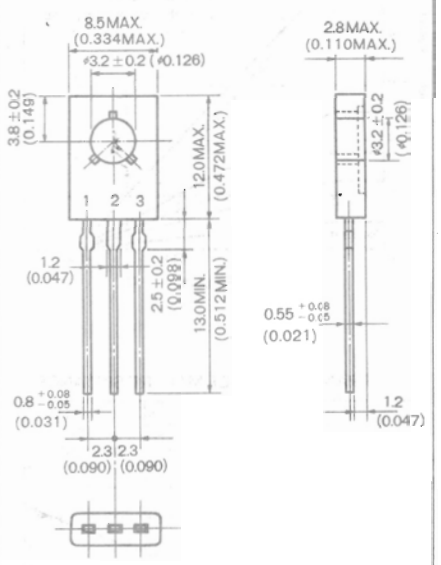
DESCRIPTION The 2SC1449 is an NPN general purpose transistor designed for use in audio and radio frequency power amplifiers.

FEATURES

- Suitable for use in output stage of 3-watt audio amplifiers.
- High current: I_C: 20 A, $I_{C(pulse)}$: 3.0 A
- The smallest package in 3 watt class power transistor.

PACKAGE DIMENSIONS

in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation

- Total Power Dissipation (T_a=25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c=25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 40 V
- V_{CEO} Collector to Emitter Voltage . . . . . 35 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current (DC) . . . . . 2.0 A
- $I_{C(pulse)}$* Collector Current (pulse) . . . . . 3.0 A

*Pulse Test PW≦350 μs, Duty Cycle≦2 %

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	90	250		V_{CE}=2.0 V, I_C=300 mA**
f_T	Gain Bandwidth Product		55		MHz	V_{CE}=5.0 V, I_C=100 mA
C_{ob}	Output Capacitance		20		pF	V_{CB}=10 V, I_E=0, f=1 MHz
I_{CBO}	Collector Cutoff Current			0.5	μA	V_{CB}=35 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.5	μA	V_{EB}=3.0 V, I_C=0
$V_{CE(sat)}$	Collector Saturation Voltage		0.2	0.7	V	I_C=500 mA, I_B=50 mA**
$V_{BE(sat)}$	Base Saturation Voltage		0.9	1.5	V	I_C=500 mA, I_B=50 mA**

**Pulse Test PW≦350 μs, Duty Cycle≦2 %

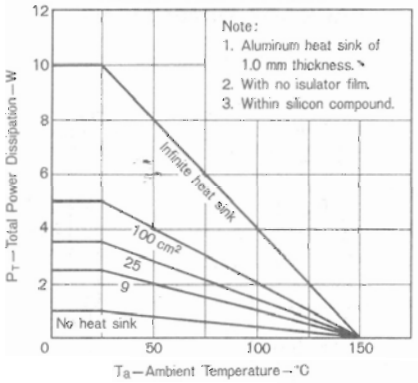
Classification of h_{FE}

Rank	N	M	L	K
Range	40 to 80	60 to 120	80 to 160	120 to 250

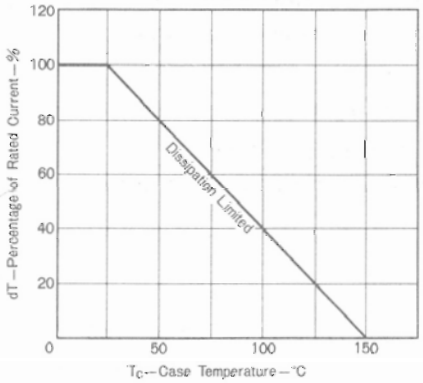
Test Conditions: V_{CE}=2.0 V, I_C=300 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

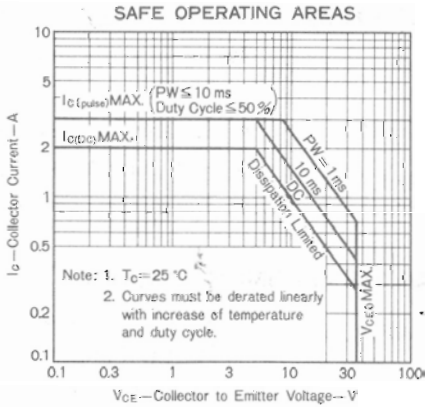
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



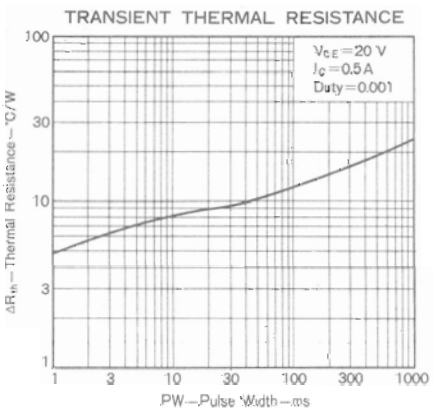
DERATING CURVE OF SAFE OPERATING AREAS



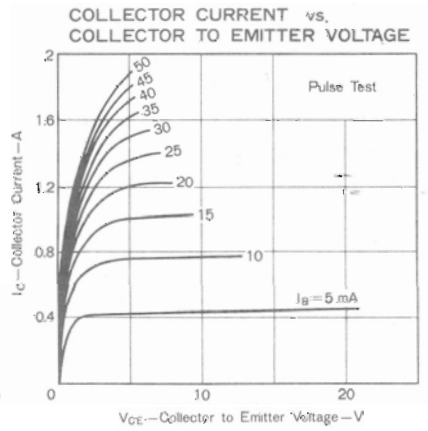
SAFE OPERATING AREAS



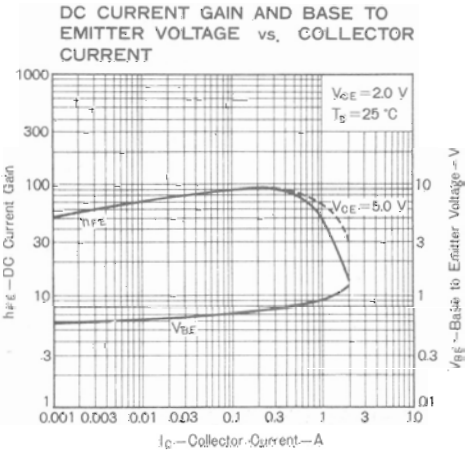
TRANSIENT THERMAL RESISTANCE



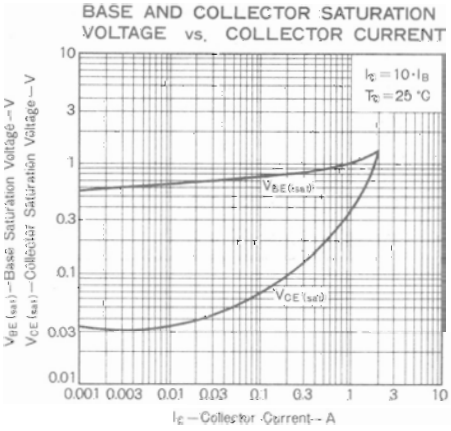
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



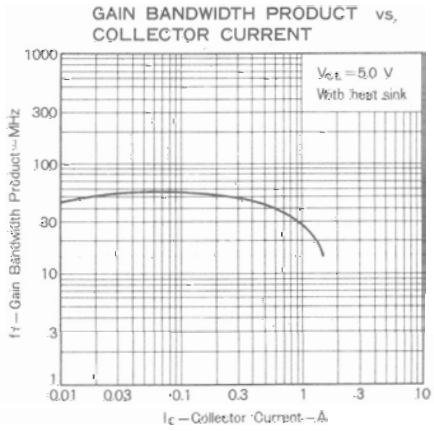
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



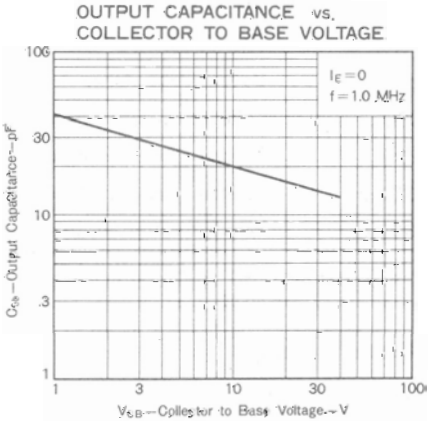
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

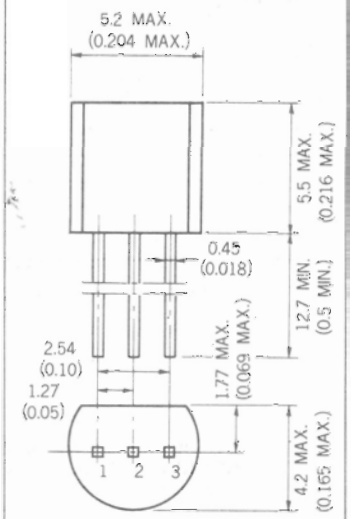
NPN SILICON TRANSISTOR
2SC1674

DESCRIPTION The 2SC1674 is designed for use in FM RF amplifier and local oscillator of FM tuner.

FEATURES

- High gain bandwidth product (f_T = 600 MHz TYP.)
- Small output capacitance (C_{ob} = 1.0 pF TYP.)
- Low noise figure (NF = 3.0 dB TYP. @100 MHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . 20 V
- V_{EBO} Emitter to Base Voltage . . . . . 4.0 V
- I_C Collector Current . . . . . 20 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	90	180	—	V_{CE} = 6.0 V, I_C = 1.0 mA
C_{ob}	Output Capacitance		1.0	1.3	pF	V_{CB} = 6.0 V, I_E = 0, f = 1.0 MHz
NF	Noise Figure		3.0	5.0	dB	V_{CE} = 6.0 V, I_E = −1.0 mA, R_G = 50 Ω, f = 100 MHz See test circuit
f_T	Gain Bandwidth Product	400	600		MHz	V_{CE} = 6.0 V, I_E = −1.0 mA
G_{pe}	Power Gain	18	22		dB	V_{CE} = 6.0 V, I_E = −1.0 mA, R_G = 50 Ω, f = 100 MHz See test circuit
$C_c \cdot r_{bb'}$	Collector to Base Time Constant		12	15	ps	V_{CE} = 6.0 V, I_E = −1.0 mA, f = 31.9 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 3.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage		0.72		V	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.3	V	I_C = 10 mA, I_B = 1.0 mA

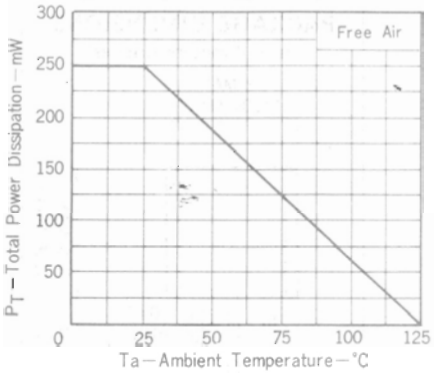
Classification of h_{FE}

Rank	M	L	K
Range	40 – 80	60 – 120	90 – 180

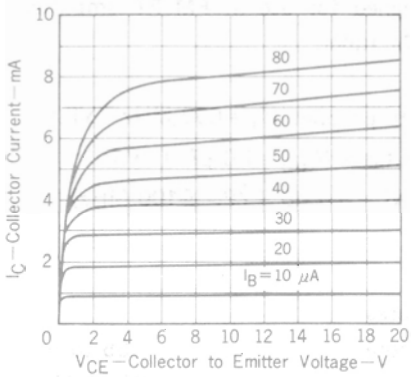
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

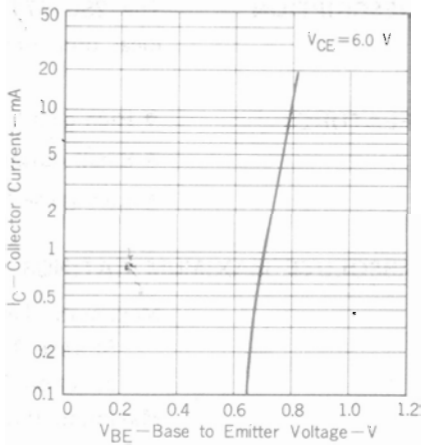
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



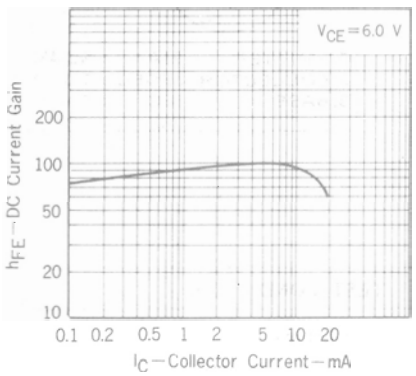
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



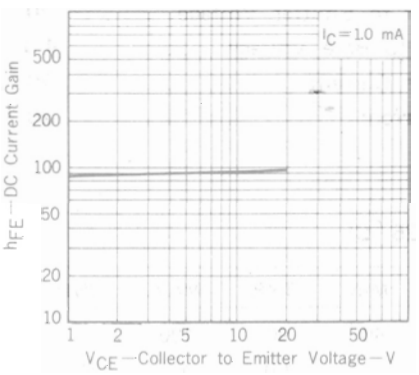
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



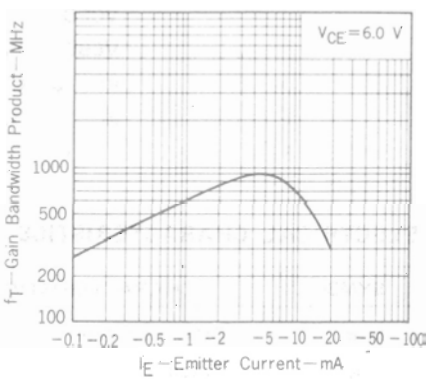
DC CURRENT GAIN vs. COLLECTOR CURRENT



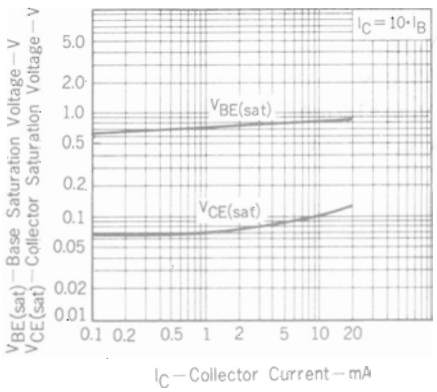
DC CURRENT GAIN vs. COLLECTOR TO EMITTER VOLTAGE



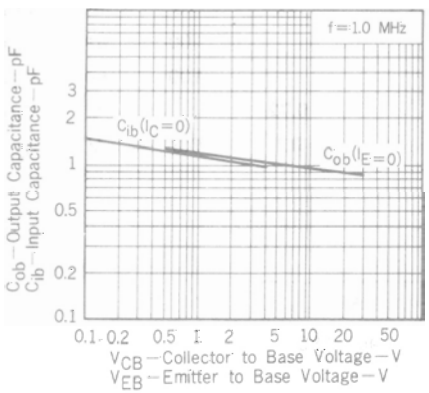
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



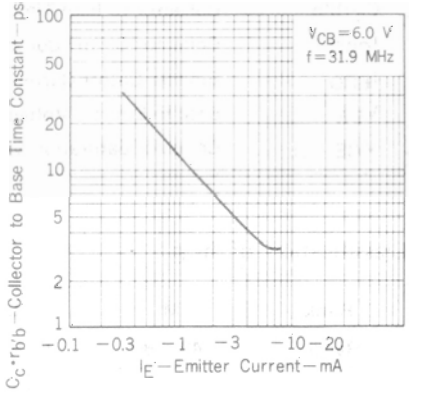
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



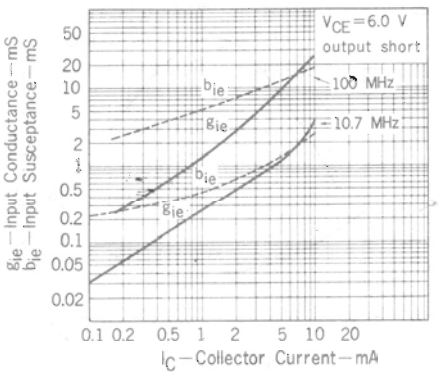
INPUT CAPACITANCE vs. EMITTER TO BASE VOLTAGE, OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



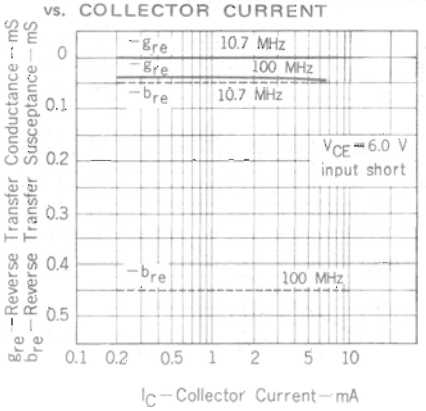
COLLECTOR TO BASE TIME CONSTANT vs. EMITTER CURRENT



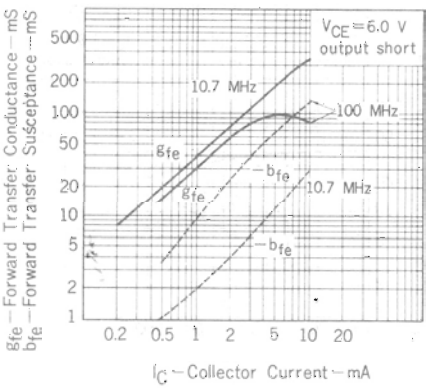
INPUT ADMITTANCE vs. COLLECTOR CURRENT



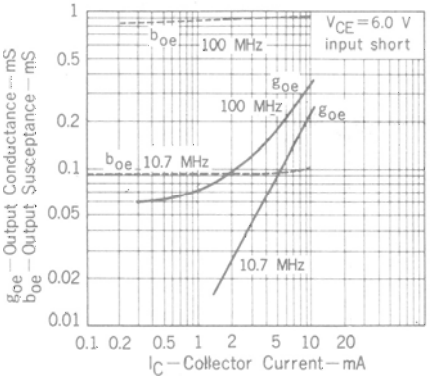
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



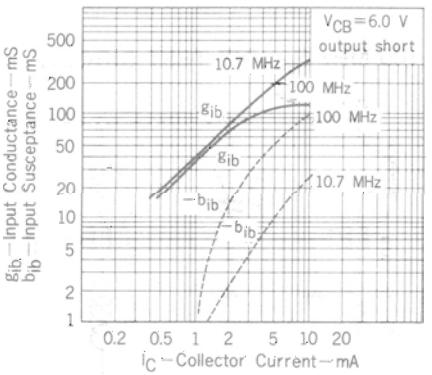
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



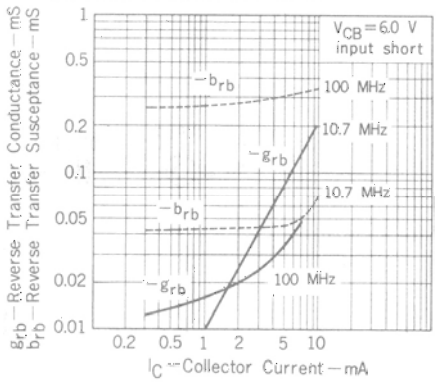
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



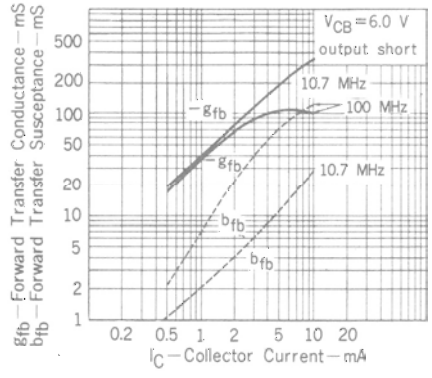
INPUT ADMITTANCE vs. COLLECTOR CURRENT



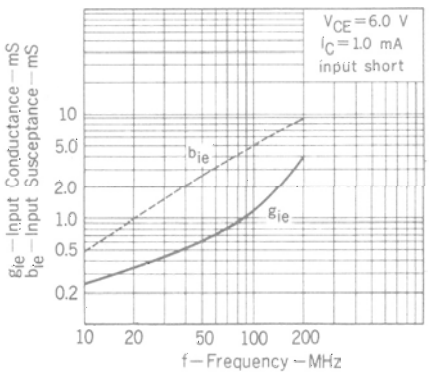
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



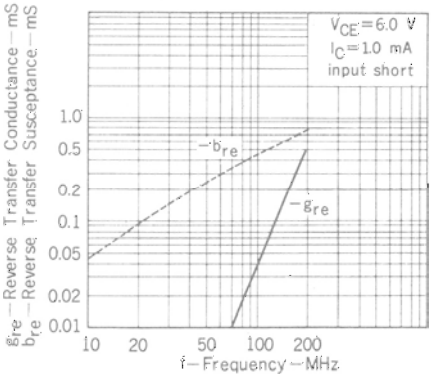
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



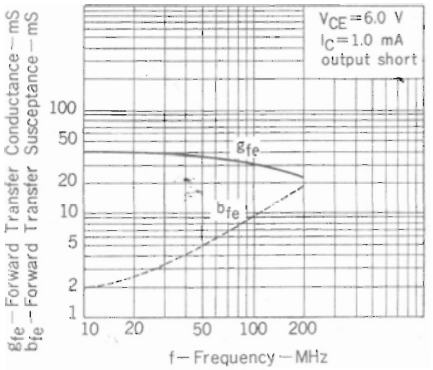
INPUT ADMITTANCE vs. FREQUENCY



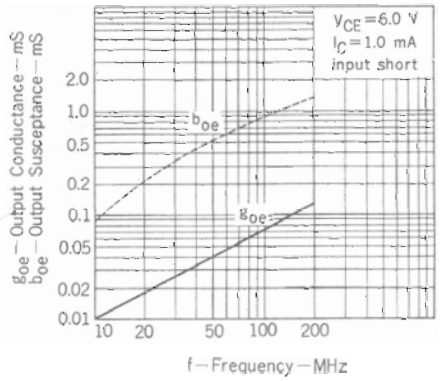
REVERSE TRANSFER ADMITTANCE vs. FREQUENCY



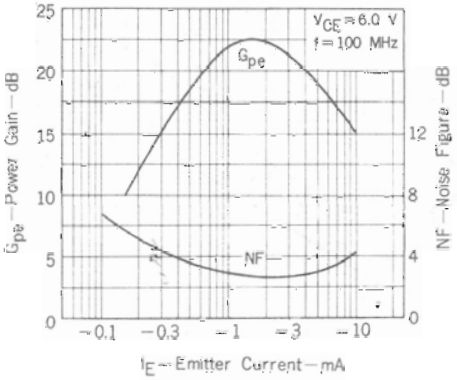
FORWARD TRANSFER ADMITTANCE vs. FREQUENCY



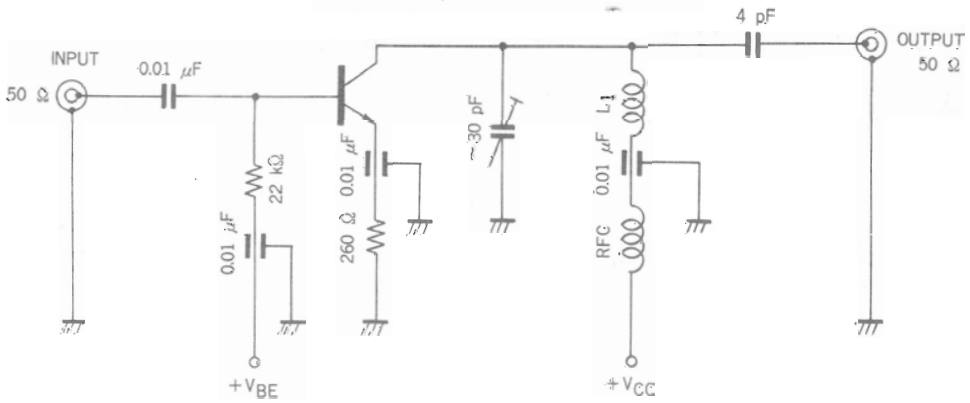
OUTPUT ADMITTANCE vs. FREQUENCY



POWER GAIN, NOISE FIGURE vs. EMITTER CURRENT



100 MHz G_{pe}, NF TEST CIRCUIT



NEC
ELECTRON DEVICE

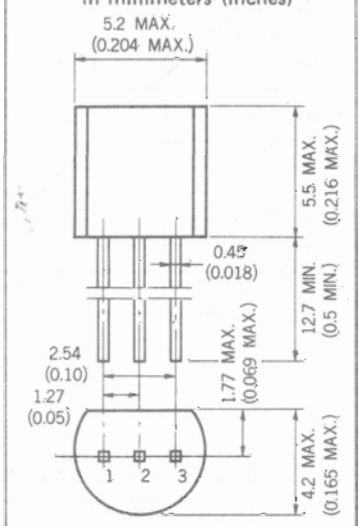
NPN SILICON TRANSISTOR
2SC1675

DESCRIPTION The 2SC1675 is designed for use in AM converter, AM/FM IF amplifier and local oscillator of AM/FM tuner.

FEATURES

- Small output capacitance (C_{ob} = 1.9 pF TYP.)
- Low noise figure (NF = 2.0 dB TYP. @1.0 MHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 50 V
- V_{CEO} Collector to Emitter Voltage . . . . . 30 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 30 mA
- I_B Base Current . . . . . 30 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	90	180	–	V_{CE}=6.0 V, I_C=1.0 mA
C_{ob}	Output Capacitance		1.9	2.2	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
NF	Noise Figure		2.0	4.0	dB	V_{CE}=6.0 V, I_E=−1.0 mA, R_G=500 Ω, f=1.0 MHz
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE}=6.0 V, I_E=−1.0 mA
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		10	15	ps	V_{CE}=6.0 V, I_E=−10 mA, f=31.9 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.65	0.70	0.75	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.08	0.30	V	I_C=10 mA, I_B=1.0 mA

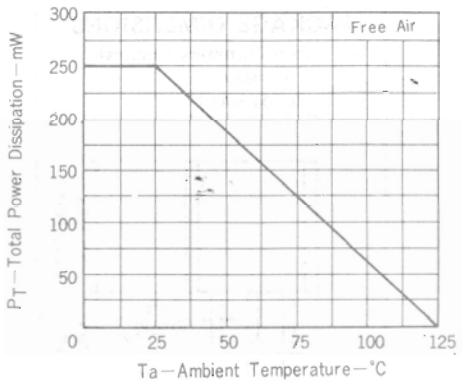
Classification of h_{FE}

Rank	M	L	K
Range	40−80	60−120	90−180

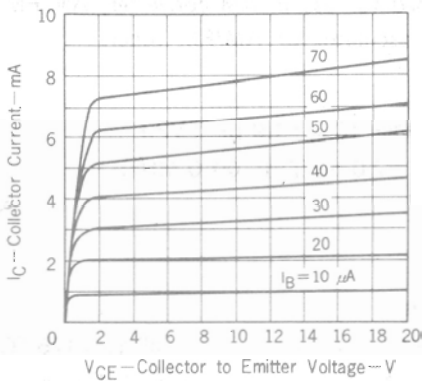
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C unless otherwise noted)

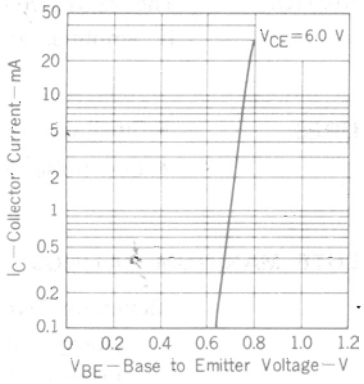
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



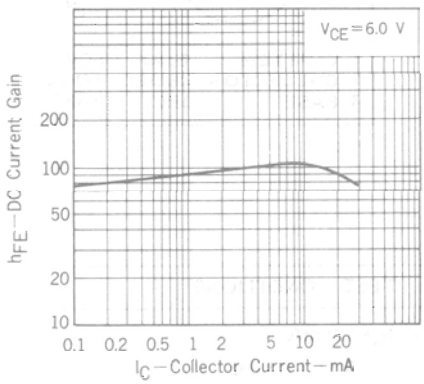
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



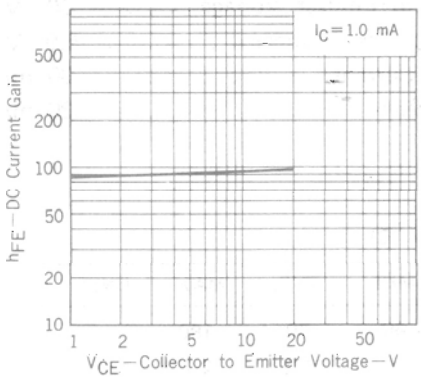
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



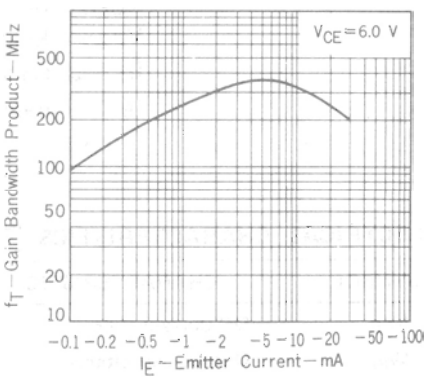
DC CURRENT GAIN vs. COLLECTOR CURRENT



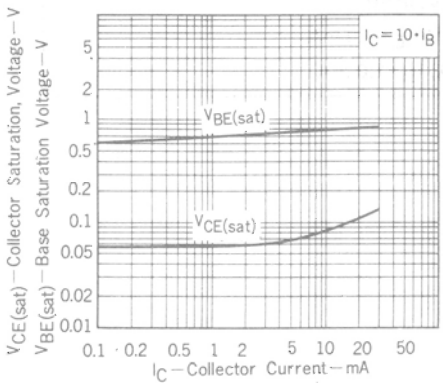
DC CURRENT GAIN vs. COLLECTOR TO EMITTER VOLTAGE



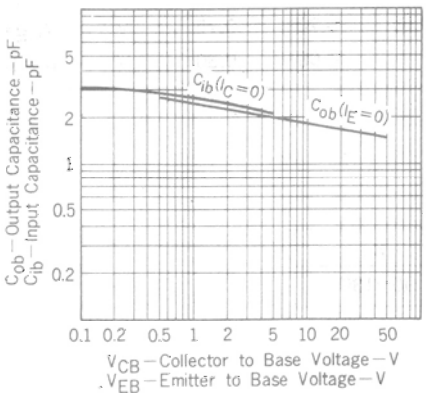
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



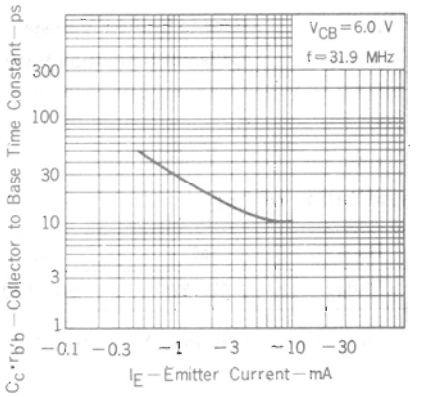
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



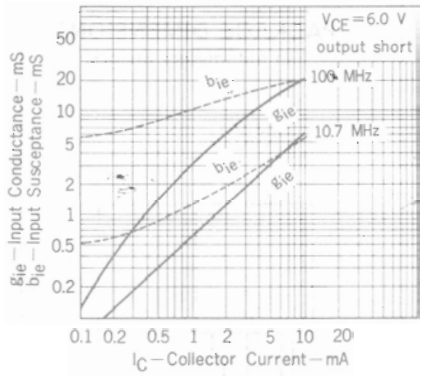
INPUT CAPACITANCE vs. EMITTER TO BASE VOLTAGE, OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



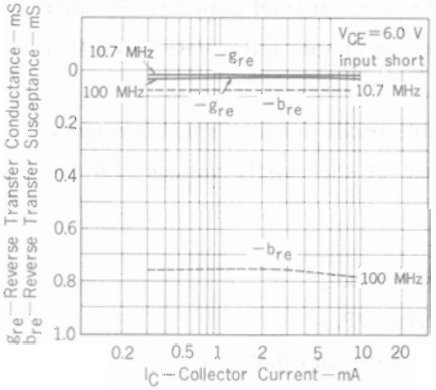
COLLECTOR TO BASE TIME CONSTANT vs. EMITTER CURRENT



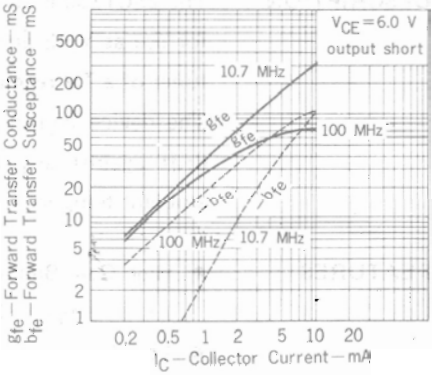
INPUT ADMITTANCE vs. COLLECTOR CURRENT



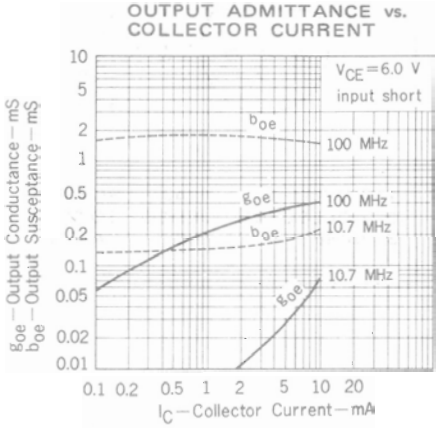
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



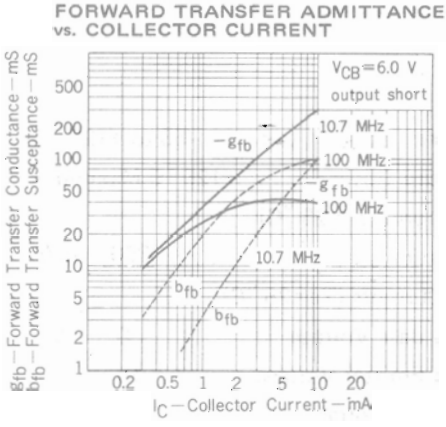
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



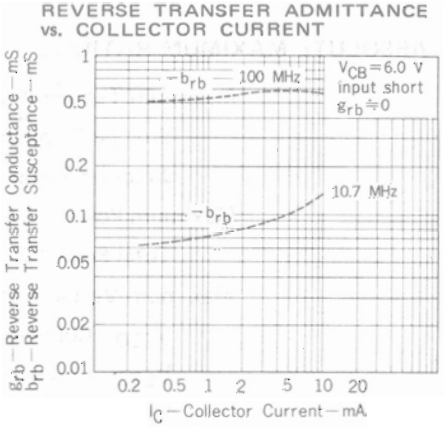
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



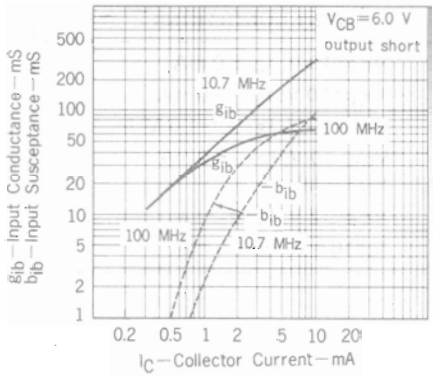
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



INPUT ADMITTANCE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC1730

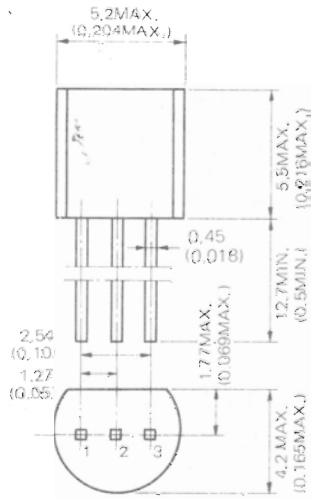
DESCRIPTION The 2SC1730 is an NPN silicon epitaxial transistor intended for use as VHF and UHF oscillators and a VHF mixer in a tuner of a TV receiver.

The device features stable oscillation and small frequency drift against any change of the supply voltage and the ambient temperature.

FEATURES

- High Gain Bandwidth Product;
  f_T=1 100 MHz TYP.
- Low Collector to Base Time Constant;
  $C_c \cdot r_{b'b}$=10 ps TYP.
- Low Output Capacitance;
  C_{ob}=1.5 pF MAX.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage	15	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	50	mA
I_B	Base Current.	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	120	180		V_{CE}=10 V, I_C=5.0 mA
f_T	Gain Bandwidth Product	800	1 100		MHz	V_{CE}=10 V, I_E=−5.0 mA
C_{ob}	Output Capacitance			1.5	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		10	15	ps	V_{CE}=10 V, I_E=−5.0 mA f=31.9 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=12 V, I_E=0
$V_{CE(sat)}$	Collector Saturation Voltage			0.5	V	I_C=10 mA, I_B=1.0 mA

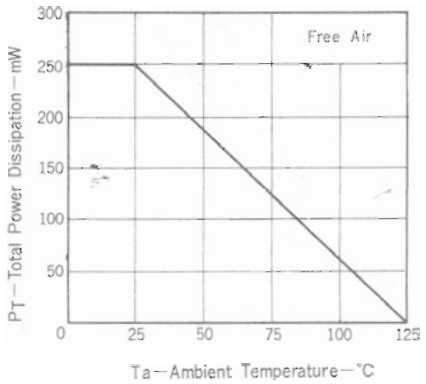
Classification of h_{FE}

Rank	L	K
Range	60 – 120	90 – 180

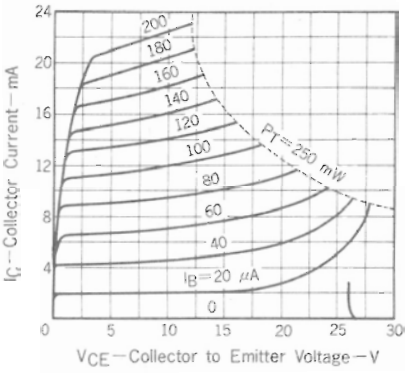
h_{FE} Test Conditions: V_{CE} = 10 V, I_C = 5.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

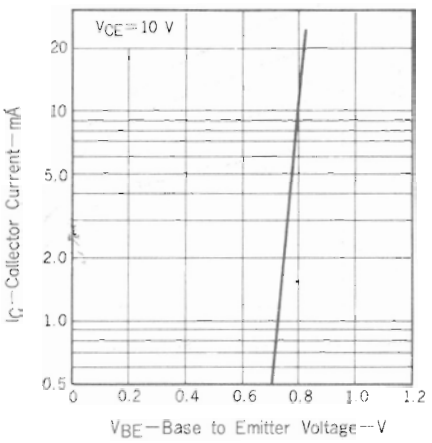
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



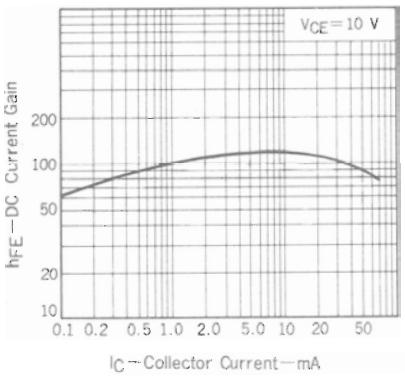
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



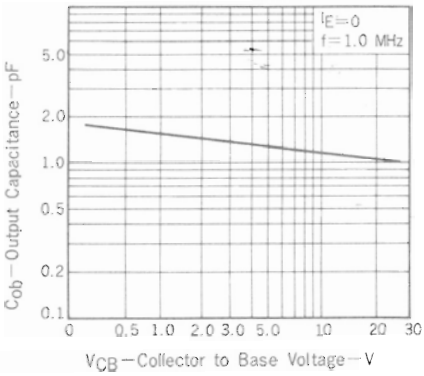
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



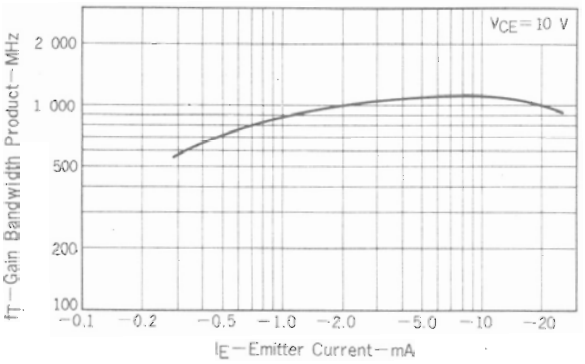
DC CURRENT GAIN vs. COLLECTOR CURRENT



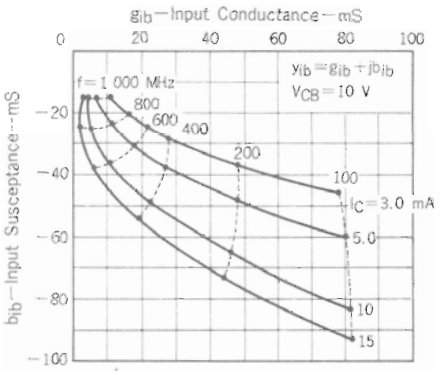
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



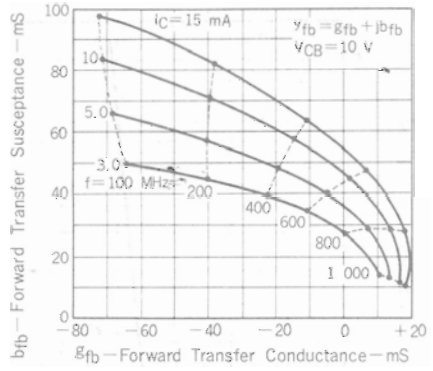
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



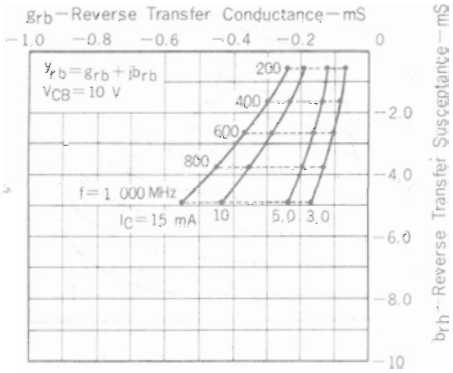
INPUT ADMITTANCE (y_{ib}) vs. FREQUENCY



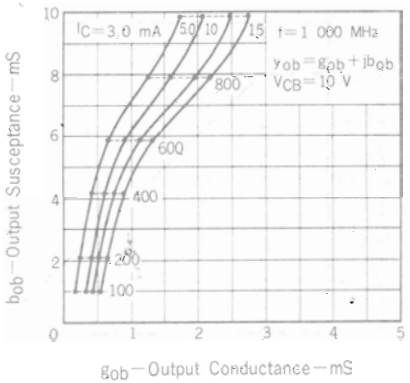
FORWARD TRANSFER ADMITTANCE (y_{fb}) vs. FREQUENCY



REVERSE TRANSFER ADMITTANCE (y_{rb}) vs. FREQUENCY



OUTPUT ADMITTANCE (y_{ob}) vs. FREQUENCY



NEC
ELECTRON DEVICE

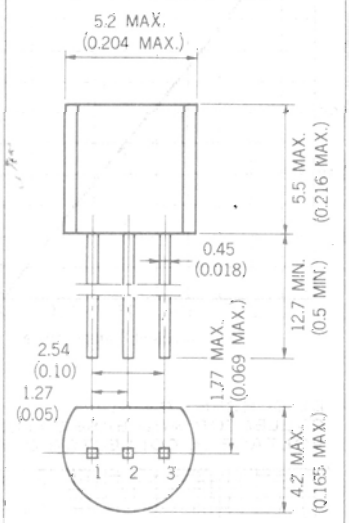
NPN SILICON TRANSISTOR
2SC1840

DESCRIPTION The 2SC1840 is designed for use in AF amplifier, driver and low speed switching.

FEATURES

- High h_{FE} h_{FE} : 400 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA).

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 40 V
- V_{CEO} Collector to Emitter Voltage . . . . . 35 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	370		–	V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	400	800	–	V_{CE} = 6.0 V, I_C = 1.0 mA
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = 6.0 V, I_E = −1.0 mA
Cob	Output Capacitance			8.0	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.55	0.59	0.65	V	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.13	0.30	V	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.84	1.00	V	I_C = 100 mA, I_B = 10 mA

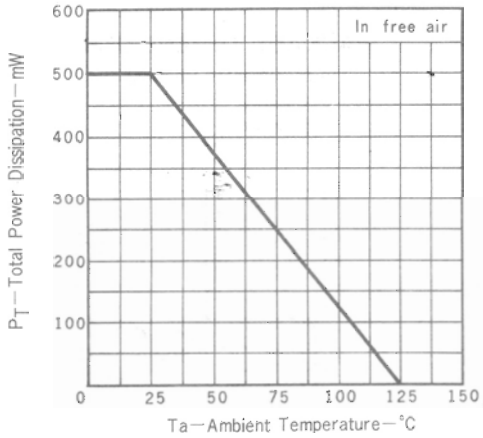
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

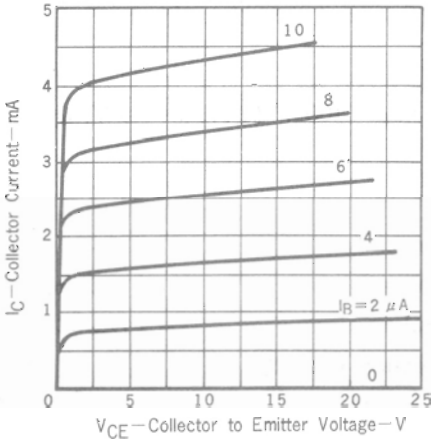
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

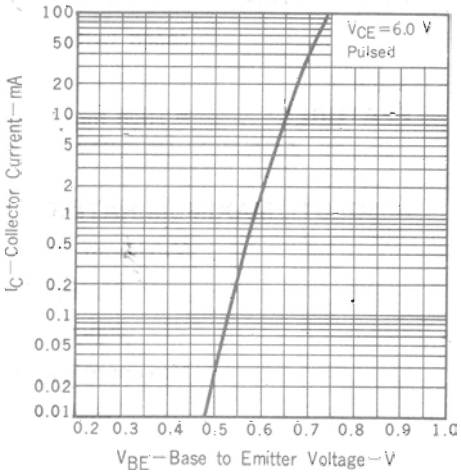
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



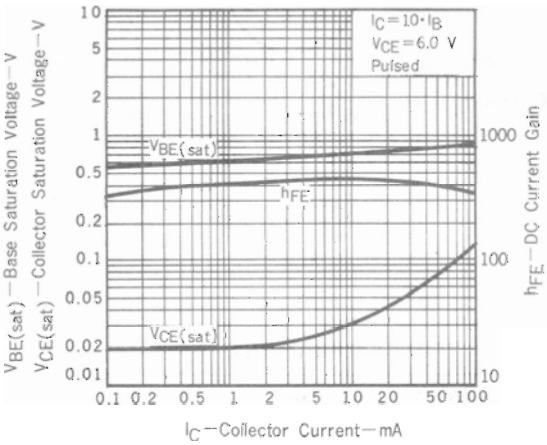
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



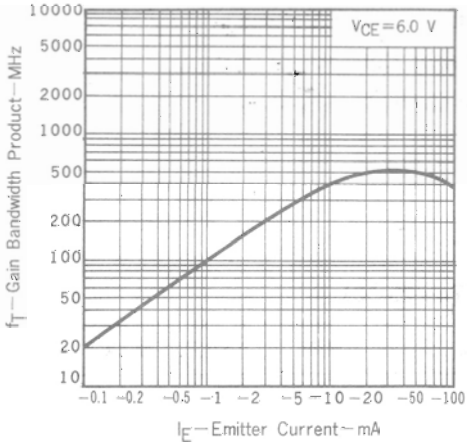
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



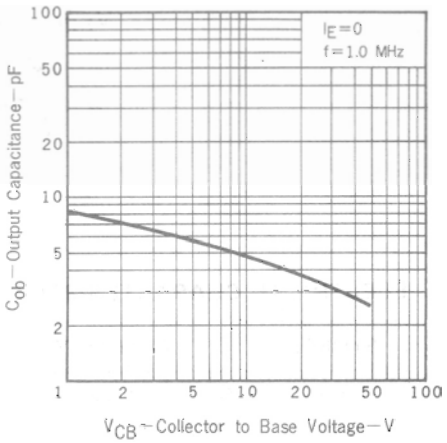
DC CURRENT GAIN, COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

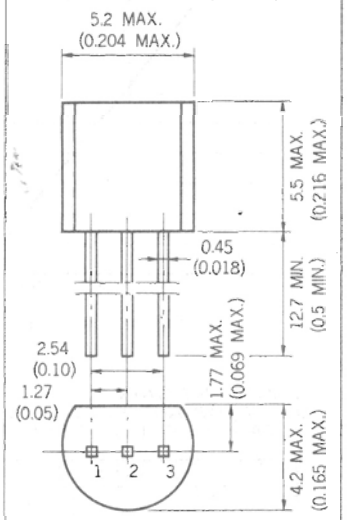
NPN SILICON TRANSISTOR
2SC1841

DESCRIPTION The 2SC1841 is designed for use in AF amplifier, driver and low speed switching.

FEATURES

- High Voltage V_{CEO} : 120 V
- High h_{FE} h_{FE} : 600 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 120 V
- V_{CEO} Collector to Emitter Voltage . . . . . 120 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 50 mA
- I_B Base Current . . . . . 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	580			V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	600	1200		V_{CE} = 6.0 V, I_C = 1.0 mA
f_T	Gain Bandwidth Product	50	110		MHz	V_{CE} = 6.0 V, I_E = −1.0 mA
C_{ob}	Output Capacitance		1.6	2.5	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB} = 120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	550	590	650	mV	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.73	1.0	V	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		70	300	mV	I_C = 10 mA, I_B = 1.0 mA

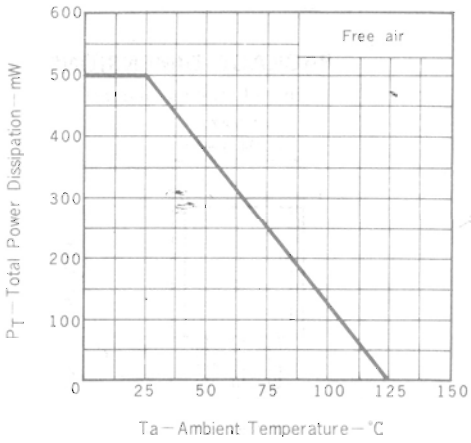
Classification of h_{FE2}

Rank	P	F	E	U
Range	200 – 400	300 – 600	400 – 800	600 – 1200

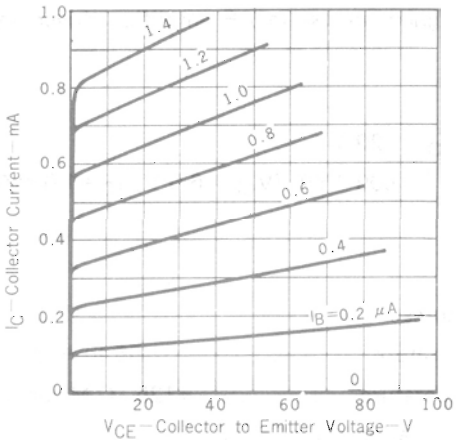
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

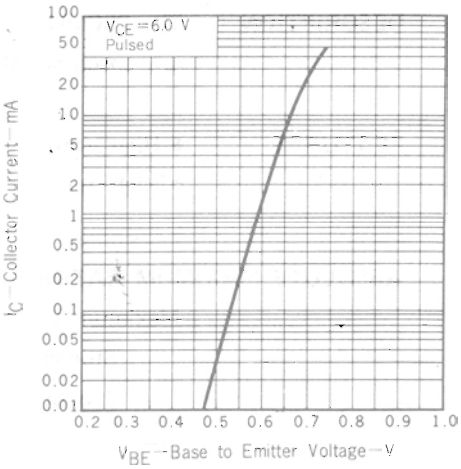
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



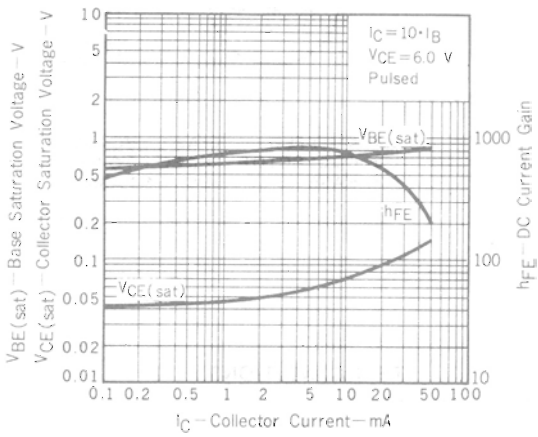
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



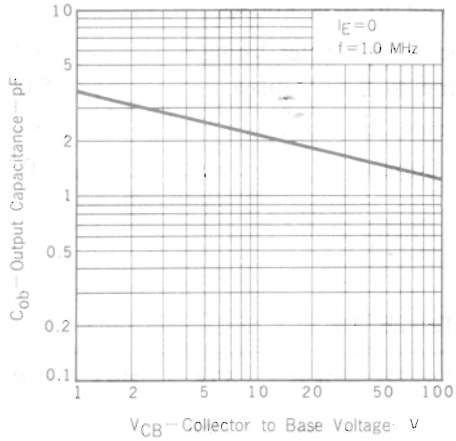
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



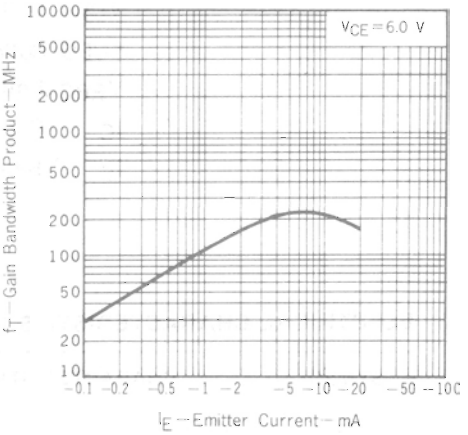
DC CURRENT GAIN, COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



NEC
ELECTRON DEVICE

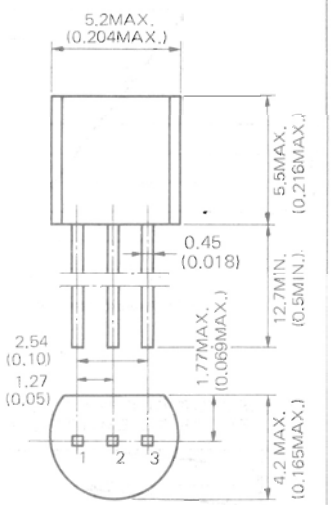
NPN SILICON TRANSISTOR
2SC1842

DESCRIPTION The 2SC1842 is designed for use in an AF amplifier and general purpose.

FEATURES

- High h_{FE}. h_{FE} : 600 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA)
- Low Noise Voltage. NV : 30 mV TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 40 V
- V_{CEO} Collector to Emitter Voltage . . . . . 35 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	580		—	V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	600	1200	—	V_{CE} = 6.0 V, I_C = 1.0 mA
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 6.0 V, I_E = −10 mA
Cob	Output Capacitance		3.0	4.0	pF	V_{CB} = 6.0 V, I_E = 0, f = 1.0 MHz
NV	Noise Voltage		30	50	mV	V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
$V_{BE(sat)}$	Base Saturation Voltage		0.86	1.0	V	I_C = 100 mA, I_B = 10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.3	V	I_C = 100 mA, I_B = 10 mA
V_{BE}	Base to Emitter Voltage	0.55	0.60	0.65	V	V_{CE} = 6.0 V, I_C = 1.0 mA

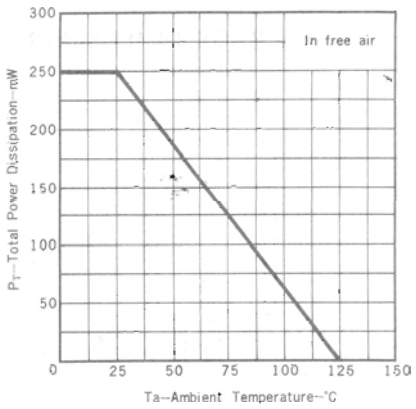
Classification of h_{FE2}

Rank	P	F	E	U
Range	200 – 400	300 – 600	400 – 800	600 – 1200

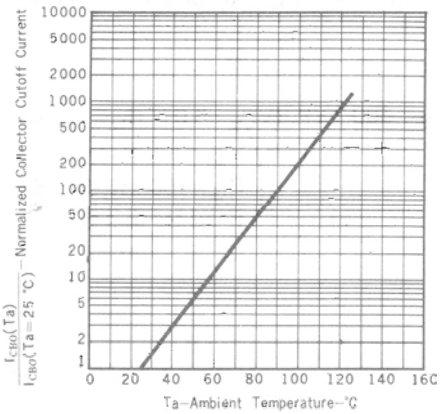
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

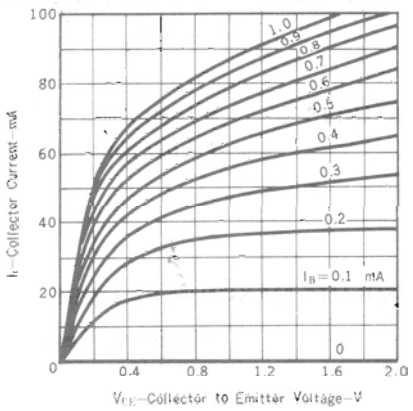
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



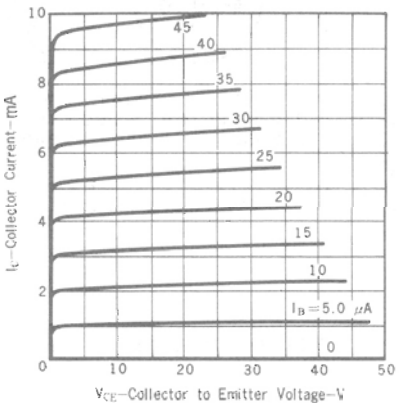
NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE



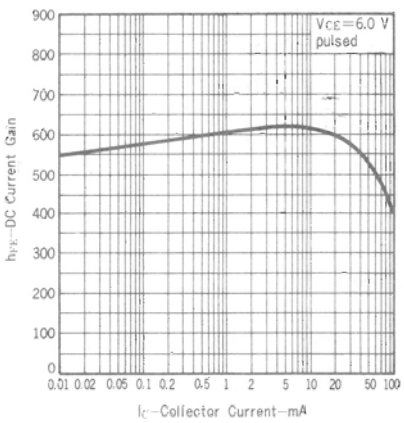
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



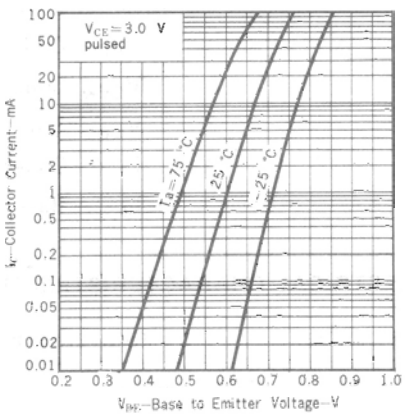
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



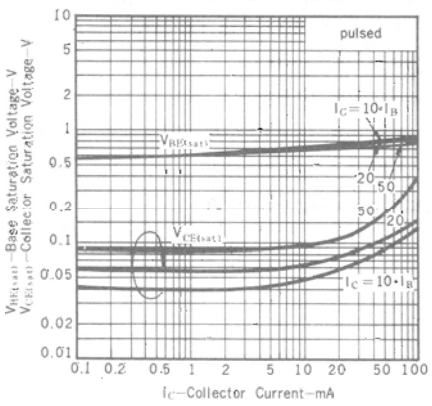
DC CURRENT GAIN vs. COLLECTOR CURRENT



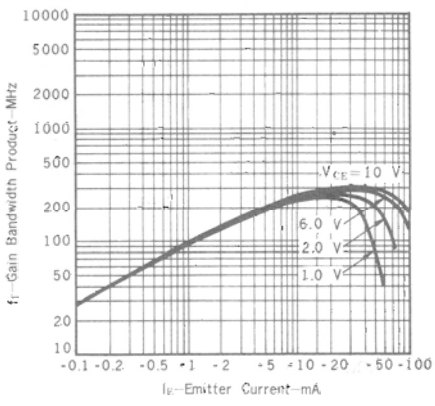
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



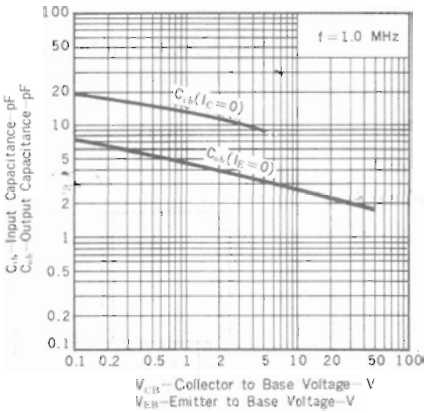
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



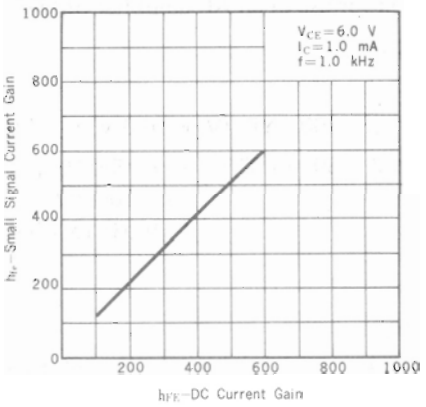
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



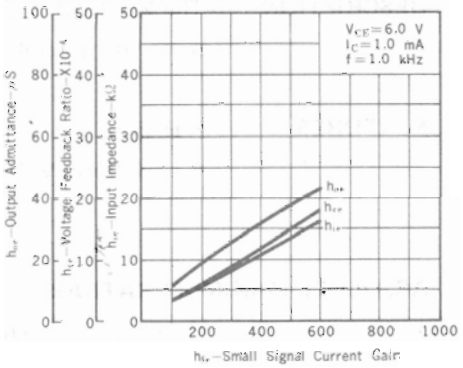
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



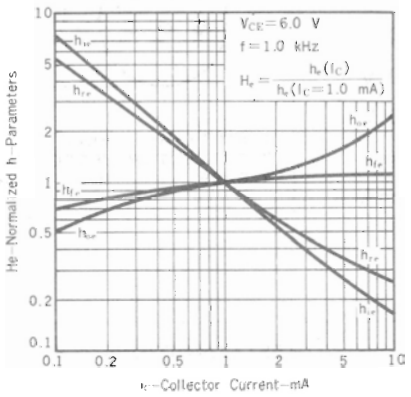
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



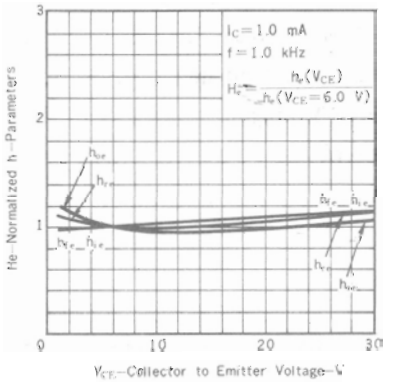
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



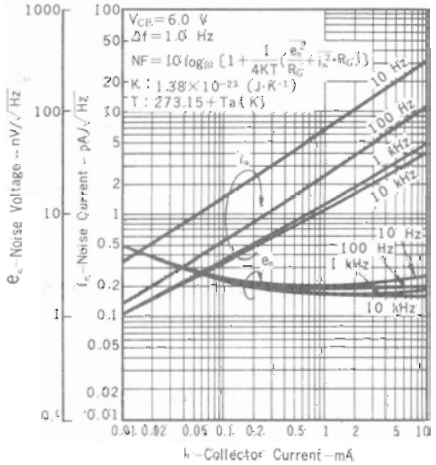
NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



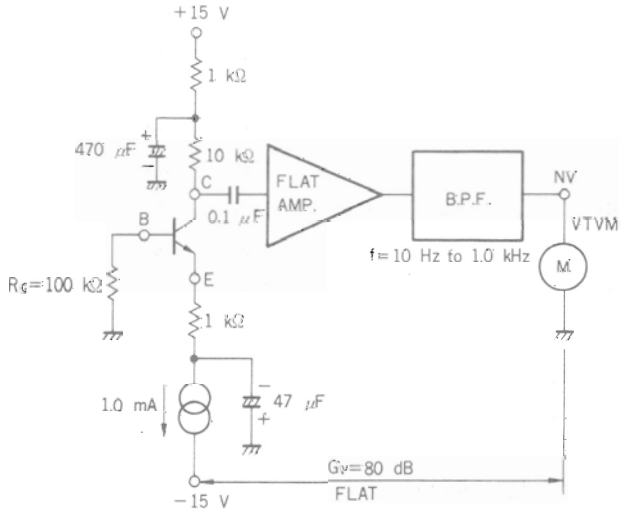
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



e_n AND i_n vs. COLLECTOR CURRENT



NOISE VOLTAGE TEST CIRCUIT



V_{CE} = 5 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

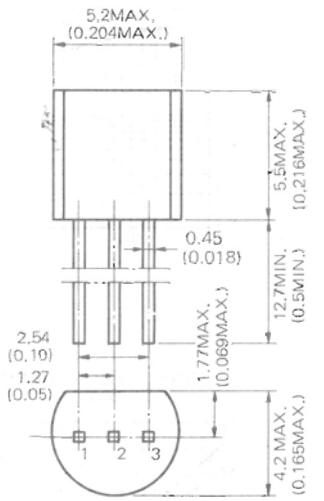
NPN SILICON TRANSISTOR
2SC1843

DESCRIPTION The 2SC1843 is designed for use in an AF amplifier of low level low noise and general purpose.

FEATURES

- High h_{FE}. h_{FE} : 400 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA)
- Low Noise Voltage. NV : 30 mV TYP. (V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	370		−	V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	400	800	−	V_{CE} = 6.0 V, I_C = 1.0 mA
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 6.0 V, I_E = −10 mA
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB} = 6.0 V, I_E = 0, f = 1.0 MHz
NV	Noise Voltage		30	40	mV	V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.55	0.60	0.65	V	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.30	V	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.86	1.0	V	I_C = 100 mA, I_B = 10 mA

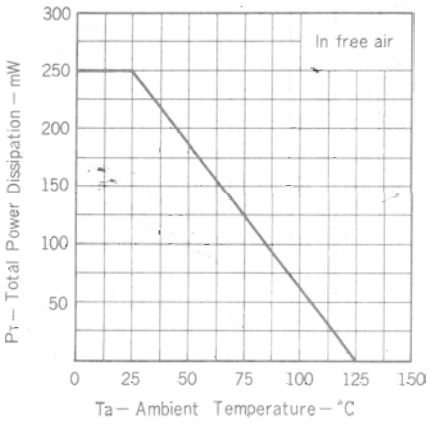
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

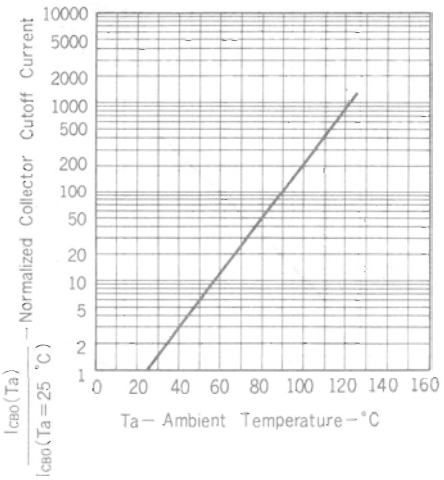
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

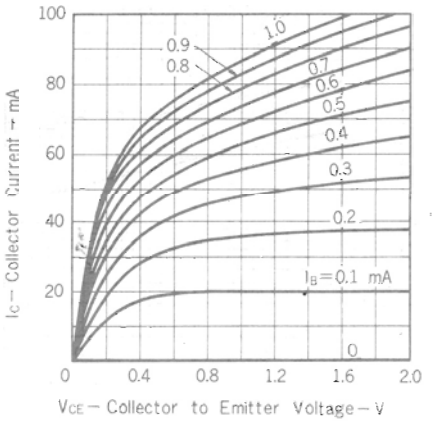
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



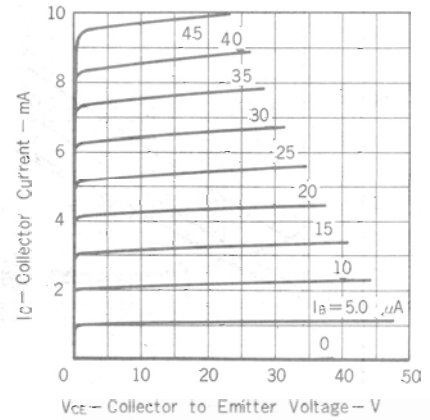
NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE



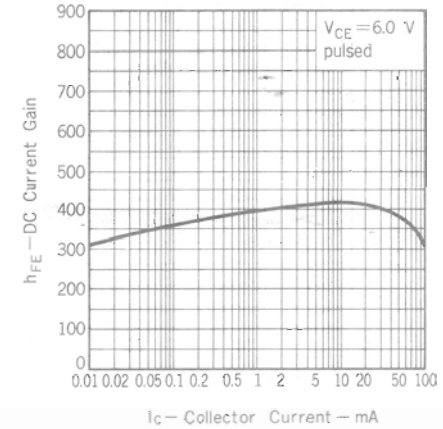
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



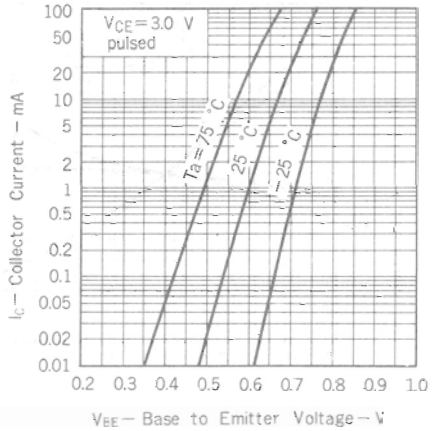
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



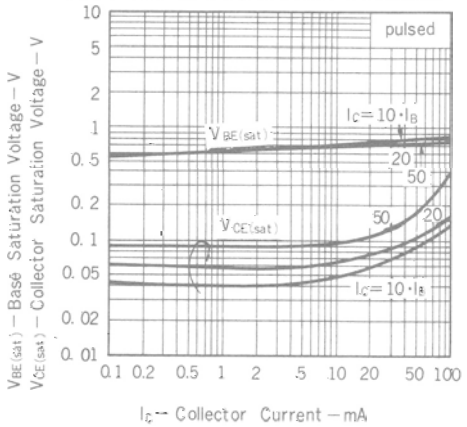
DC CURRENT GAIN vs. COLLECTOR CURRENT



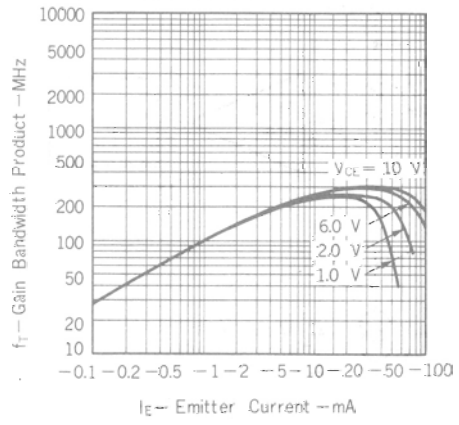
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



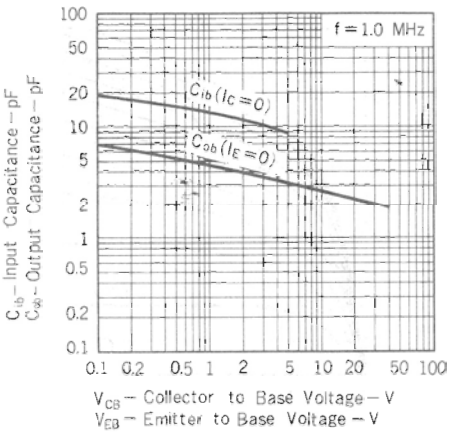
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



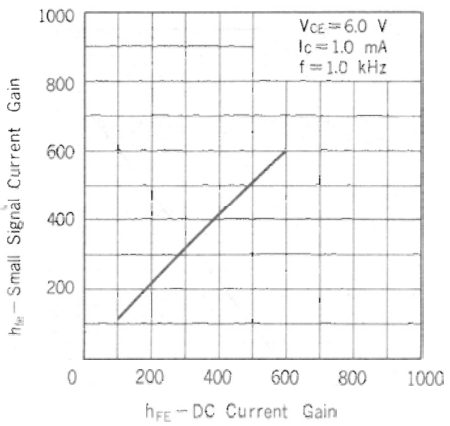
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



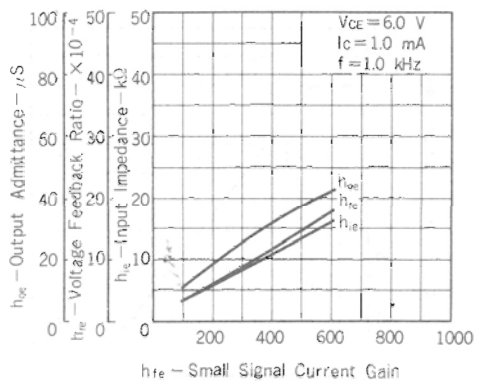
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



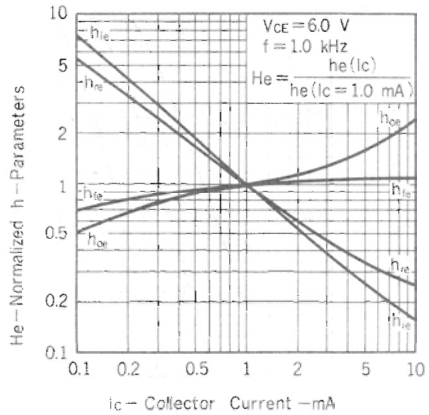
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



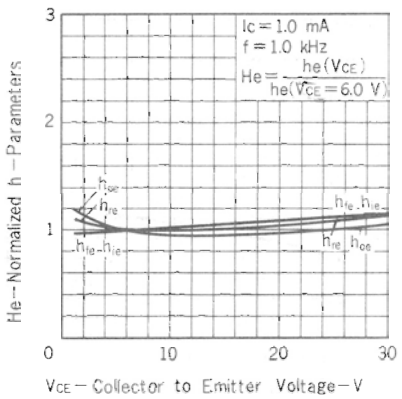
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



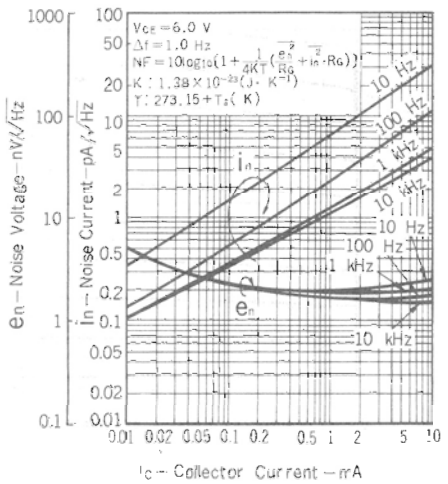
NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



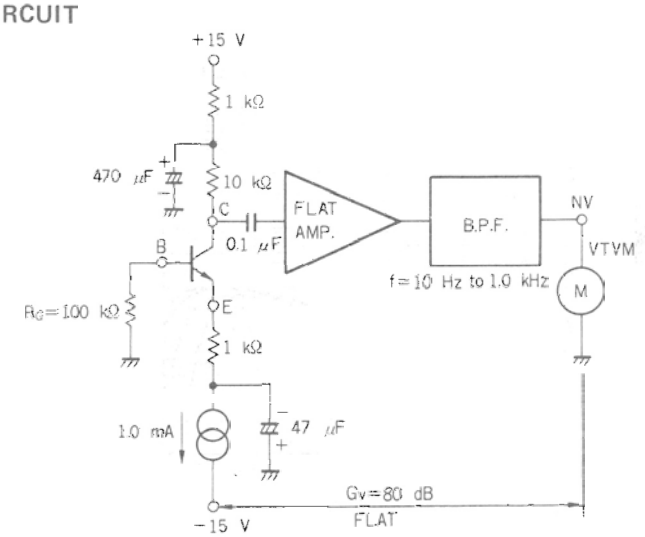
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



e_n AND i_n vs. COLLECTOR CURRENT



NOISE VOLTAGE TEST CIRCUIT



V_{CE} ≒ 5 V, I_C = 1.0 mA, R_G = 100 kΩ, Gv = 80 dB, FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR

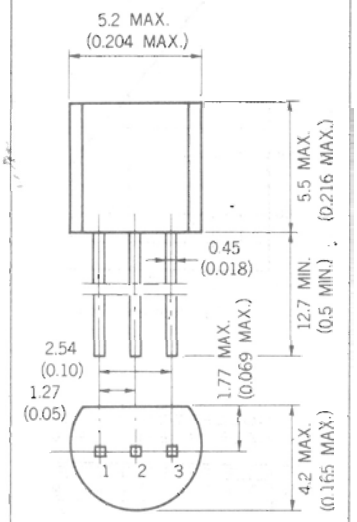
☆ 2SC1844

DESCRIPTION The 2SC1844 is the best for the head amplifier of tape recorders, the equalizer of moving coil type record players, and etc.

FEATURES

- Super Low Noise. NV : 30 mV TYP. (See test circuit.)
- High h_{FE}. h_{FE} : 400 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA)
- Complementary to 2SA991.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 60 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA
- I_B Base Current . . . . . 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	370		—	V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	400	800	—	V_{CE} = 6.0 V, I_C = 1.0 mA
f_T	Gain Bandwidth Product	50	100		MHz	V_{CE} = 6.0 V, I_E = −1.0 mA
Cob	Output Capacitance		4.8	8.0	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
NV	Noise Voltage		30	45	mV	V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 100 kΩ G_V = 80 dB, f = 10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.55	0.59	0.65	V	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.13	0.30	V	I_C = 100 mA, I_B = 10 mA

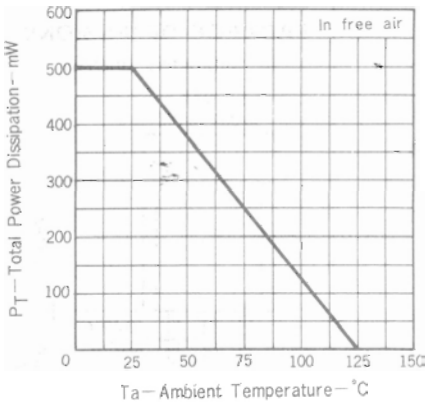
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

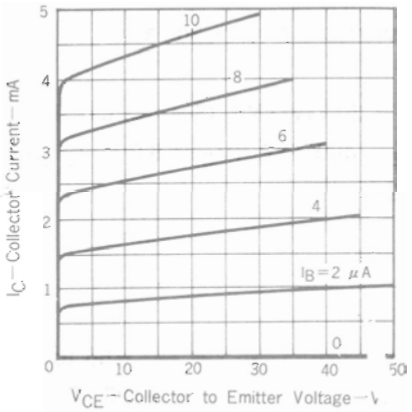
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C unless otherwise noted)

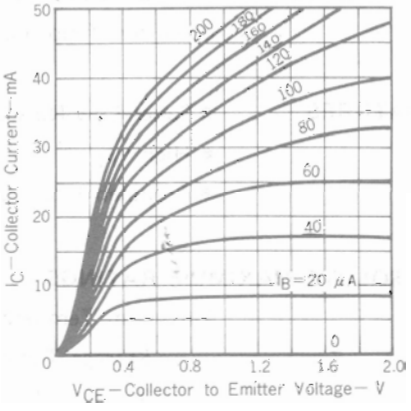
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



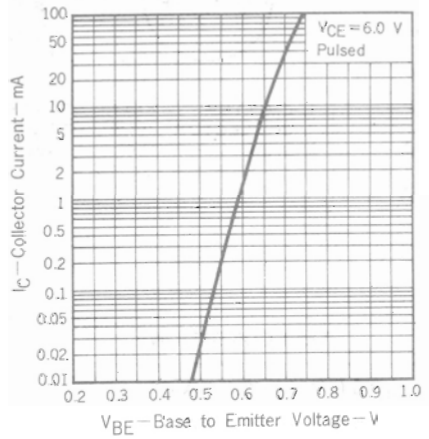
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



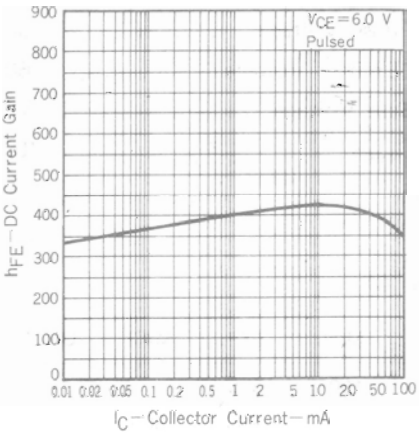
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



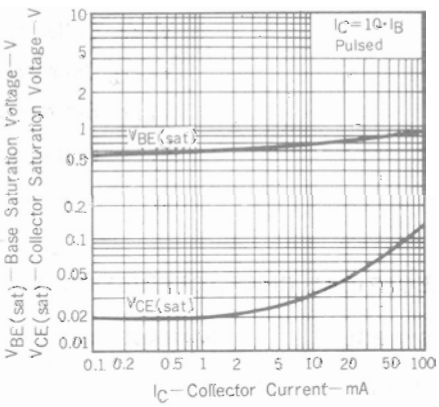
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



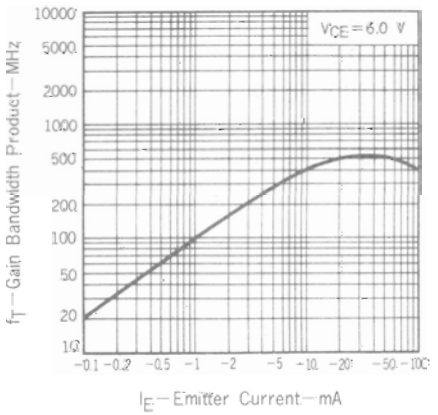
DC CURRENT GAIN vs. COLLECTOR CURRENT



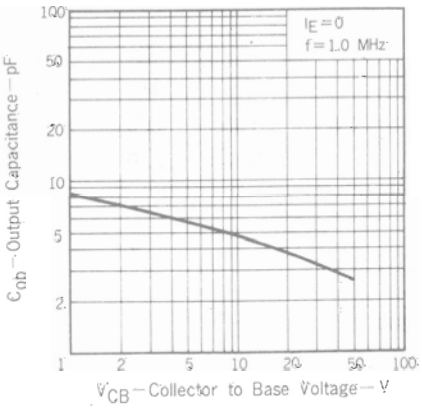
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



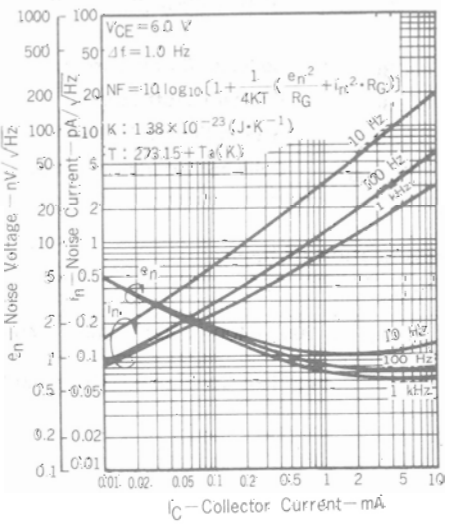
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



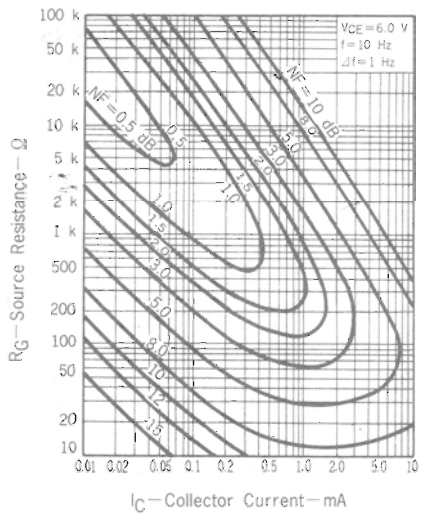
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



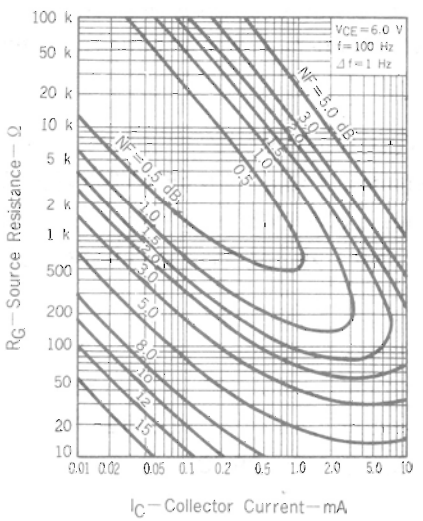
e_n AND i_n vs. COLLECTOR CURRENT



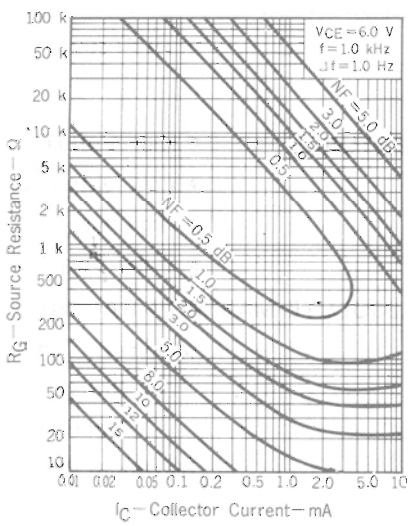
NOISE FIGURE MAP



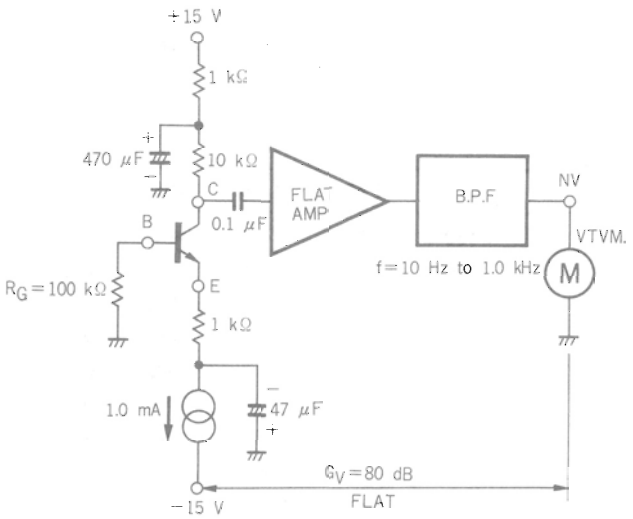
NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NOISE VOLTAGE TEST CIRCUIT



$V_{CE} \fallingdotseq 5$ V, $I_C = 1.0$ mA, $R_G = 100$ kΩ, $G_V = 80$ dB FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

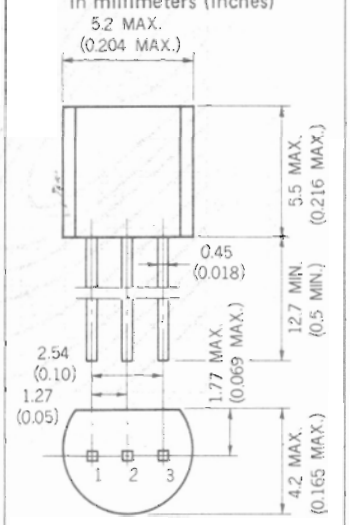
NPN SILICON TRANSISTOR
2SC1845

DESCRIPTION The 2SC1845 is the best for use as the middle range amplifier in Hi-Fi stereo control amplifiers, power amplifiers, and etc.

FEATURES

- High Voltage. V_{CEO} : 120 V
- Low Output Capacitance. C_{ob} : 1.6 pF TYP. (V_{CB} = 30 V)
- High h_{FE}. h_{FE} : 600 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA)
- Super Low Noise. NV : 25 mV TYP. (See test Circuit.)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 500 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 120 V
- V_{CEO} Collector to Emitter Voltage . . . . . 120 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 50 mA
- I_B Base Current . . . . . 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	580		–	V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	600	1200	–	V_{CE} = 6.0 V, I_C = 1.0 mA
f_T	Gain Bandwidth Product	50	110		MHz	V_{CE} = 6.0 V, I_E = −1.0 mA
C_{ob}	Output Capacitance		1.6	2.5	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
NV	Noise Voltage		25	40	mV	V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, f = 10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB} = 120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.55	0.59	0.65	V	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.07	0.30	V	I_C = 10 mA, I_B = 1.0 mA

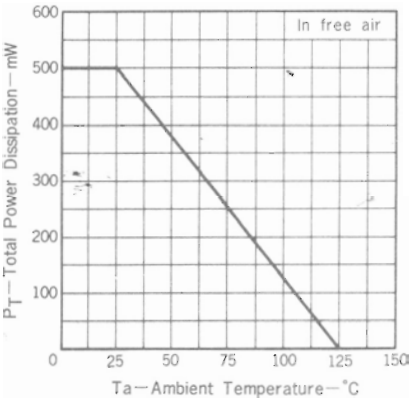
Classification of h_{FE2}

Rank	P	F	E	U
Range	200 – 400	300 – 600	400 – 800	600 – 1200

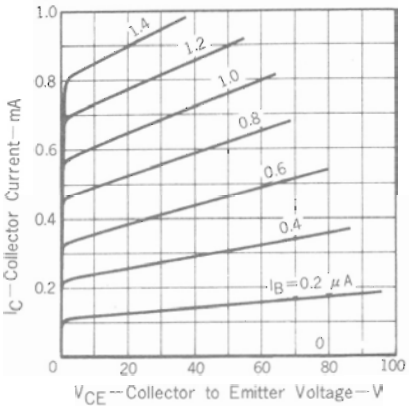
h_{FE} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

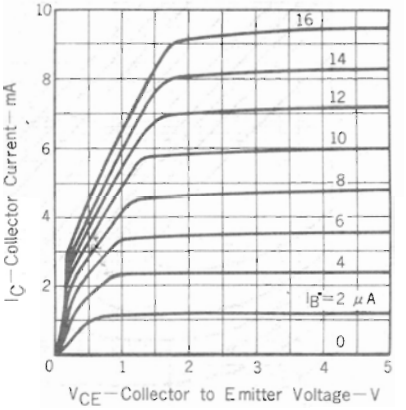
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



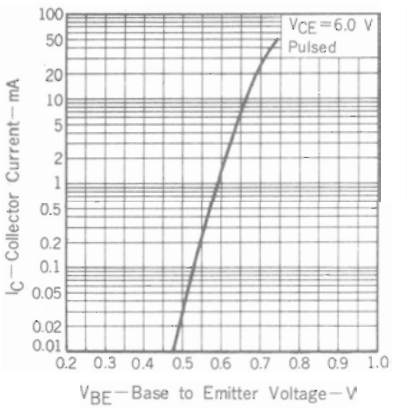
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



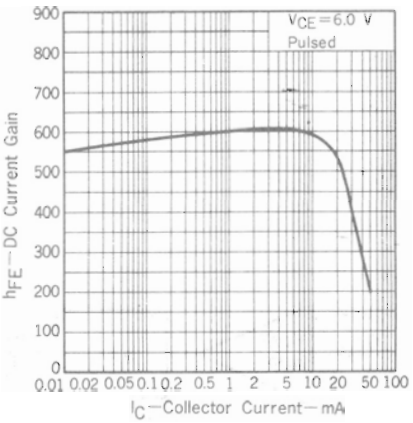
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



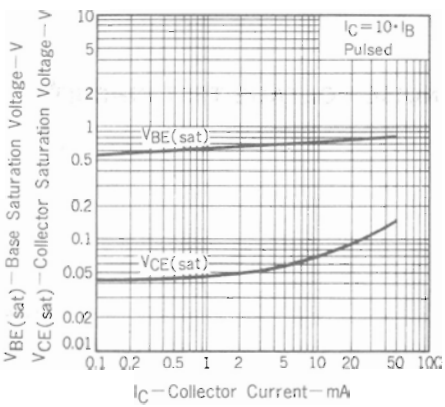
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



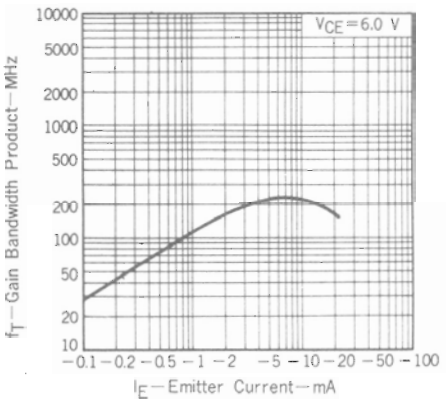
DC CURRENT GAIN vs. COLLECTOR CURRENT



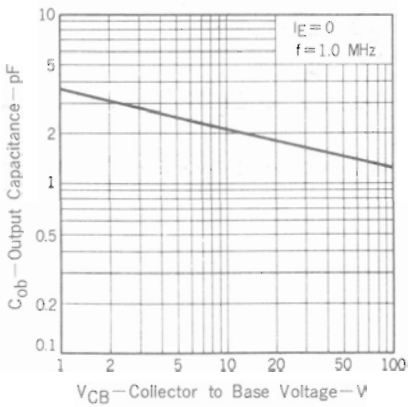
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



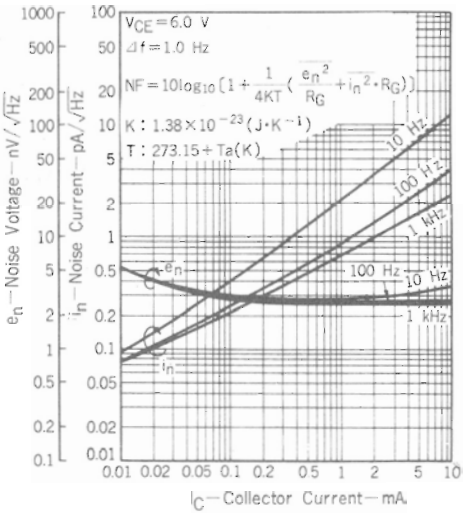
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



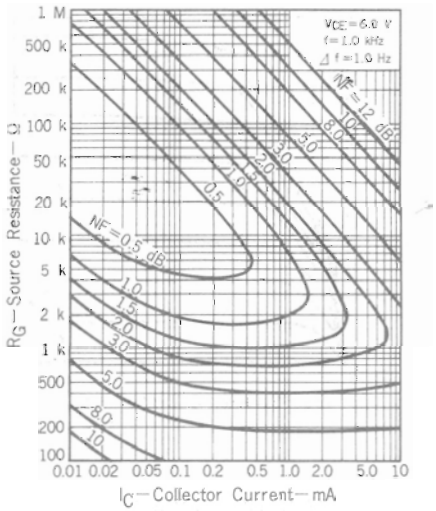
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



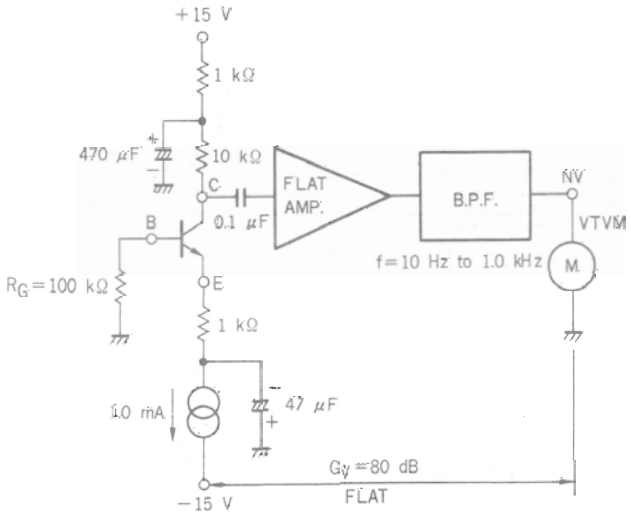
e_n AND i_n vs. COLLECTOR CURRENT



NOISE FIGURE MAP.



NOISE VOLTAGE TEST CIRCUIT



V_{CE} = 5 V, I_C = 1.0 mA, R_G = 100 kΩ, G_V = 80 dB, FLAT (f = 10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

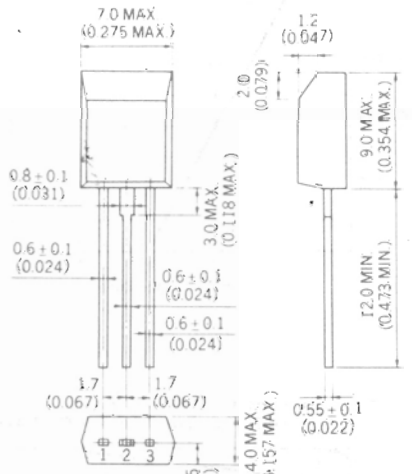
NPN SILICON TRANSISTOR
2SC1940

DESCRIPTION The 2SC1940 is designed for use in driver stages of audio frequency amplifiers.

FEATURES

- High total power dissipation and high breakdown voltage: 1.0 W at 25 °C ambient temperature/V_{CEO}=120 V
- Complementary to the NEC 2SA915 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 1.0 W
- Thermal Resistance(Junction to Ambient) . . . . . 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	120	V
V_{CEO}	Collector to Emitter Voltage	120	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	50	mA
I_B	Base Current	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	–	V_{CE}=10 V, I_C=10 mA
h_{FE2}	DC Current Gain	50	180		–	V_{CE}=10 V, I_C=1.0 mA
f_T	Gain Bandwidth Product	50	120		MHz	V_{CE}=10 V, I_E=−10 mA
C_{ob}	Output Capacitance		2.3	3.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=120 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	650	685	750	mV	V_{CE}=10 V, I_C=10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.07	0.6	V	I_C=20 mA, I_B=2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.75	1.0	V	I_C=20 mA, I_B=2.0 mA

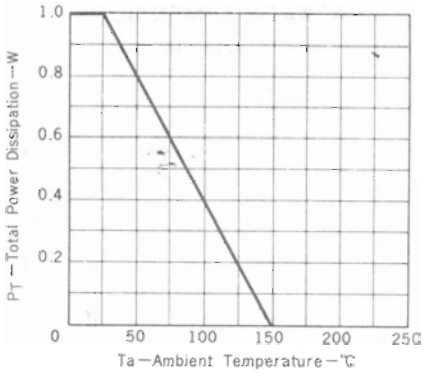
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

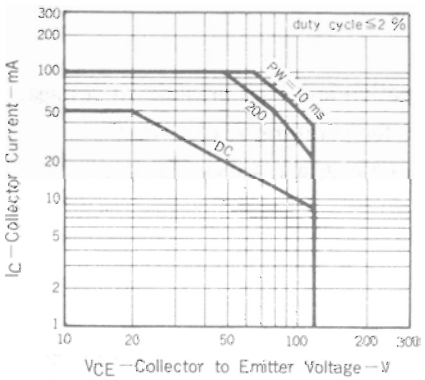
h_{FE1} Test Conditions: V_{CE}=10 V, I_C=10 mA

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

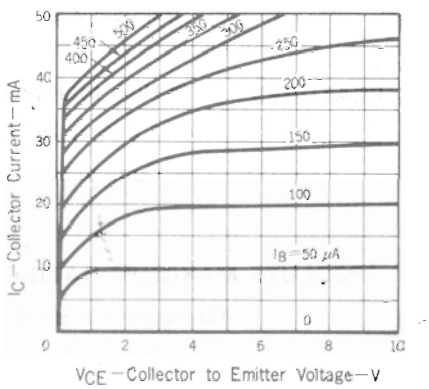
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



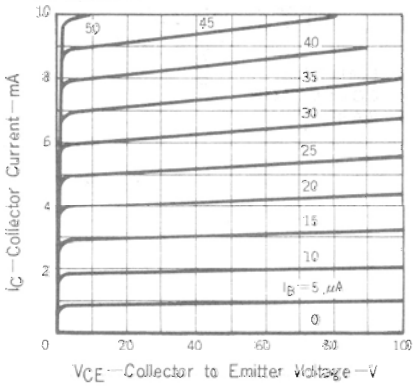
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



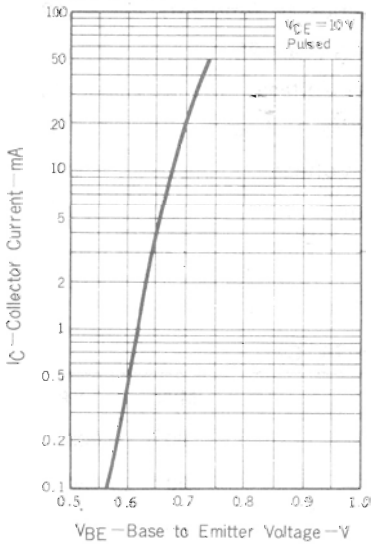
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



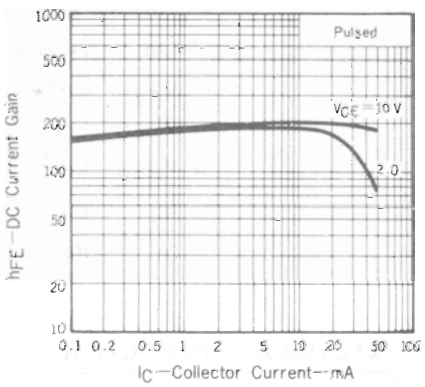
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



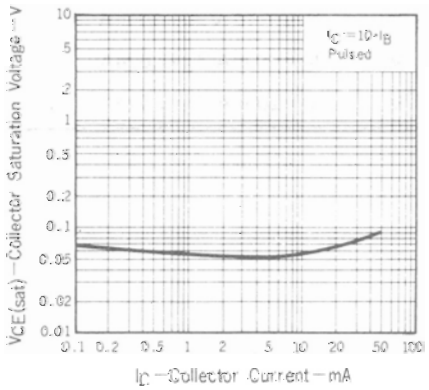
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



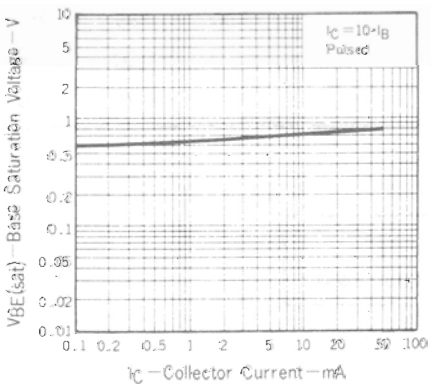
DC CURRENT GAIN vs. COLLECTOR CURRENT



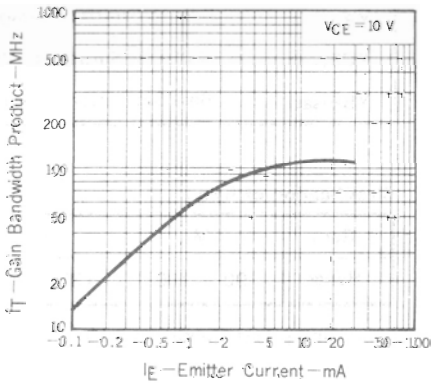
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



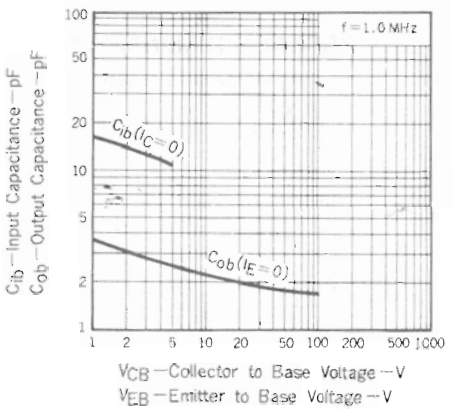
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE
vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

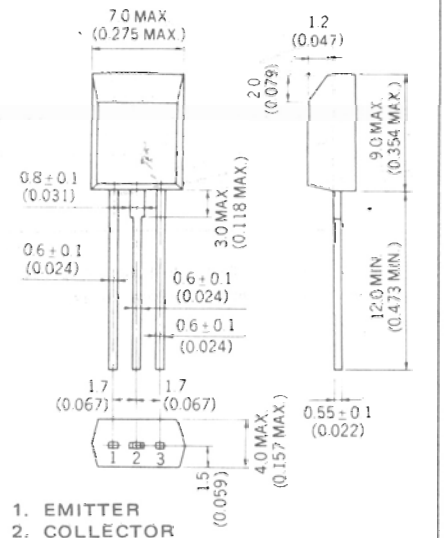
NPN SILICON TRANSISTOR
2SC1941

DESCRIPTION The 2SC1941 is designed for use in driver stages of audio frequency amplifiers.

FEATURES

- High total power dissipation and high breakdown voltage: 1.0 W at 25 °C ambient temperature/V_{CEO}=160 V
- Complementary to the NEC 2SA916 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 1.0 W
- Thermal Resistance(junction to Ambient) ... 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... 160 V
- V_{CEO} Collector to Emitter Voltage ..... 160 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 50 mA
- I_B Base Current ..... 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	—	V_{CE} = 10 V, I_C=10 mA
h_{FE2}	DC Current Gain	50	180		—	V_{CE} = 10 V, I_C=1.0 mA
f_T	Gain Bandwidth Product	50	120		MHz	V_{CE} = 10 V, I_E=−10 mA
C_{ob}	Output Capacitance		2.3	3.0	pF	V_{CB} = 10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 160 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	650	685	750	mV	V_{CE} = 10 V, I_C=10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.07	0.6	V	I_C = 20 mA, I_B=2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.75	1.0	V	I_C = 20 mA, I_B=2.0 mA

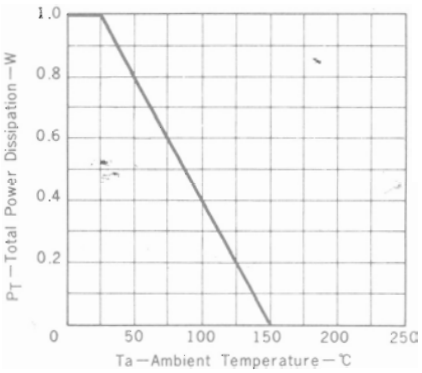
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

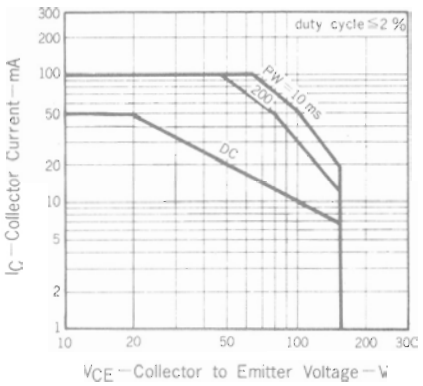
h_{FE1} Test Conditions: V_{CE} = 10 V, I_C = 10 mA

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

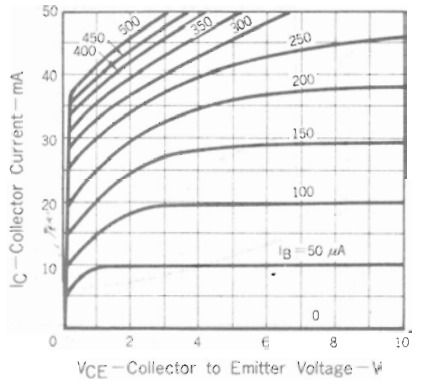
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



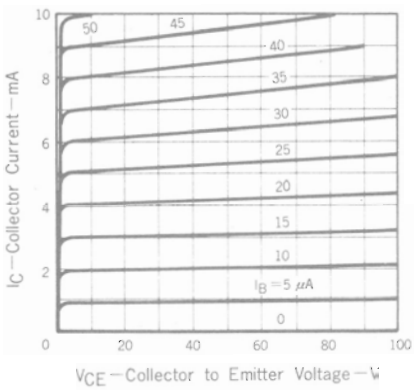
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



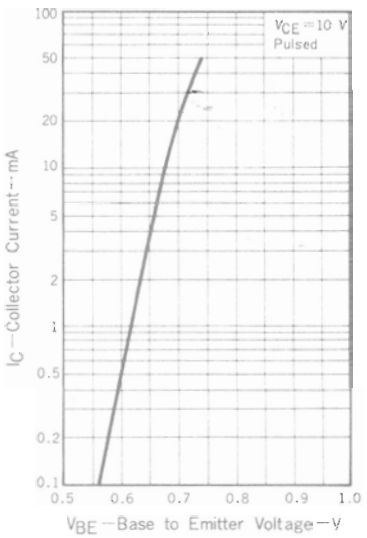
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



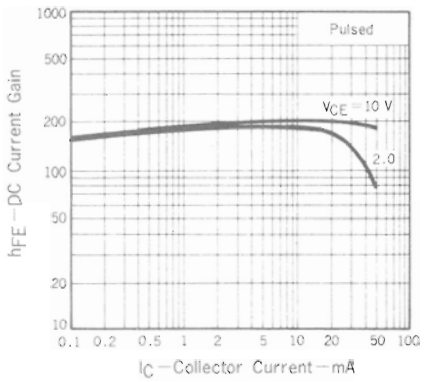
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



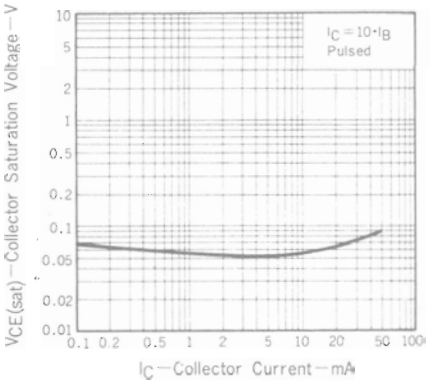
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



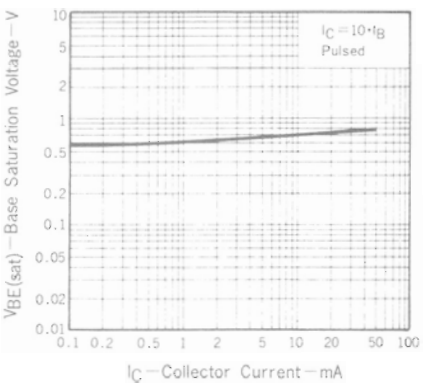
DC CURRENT GAIN vs. COLLECTOR CURRENT



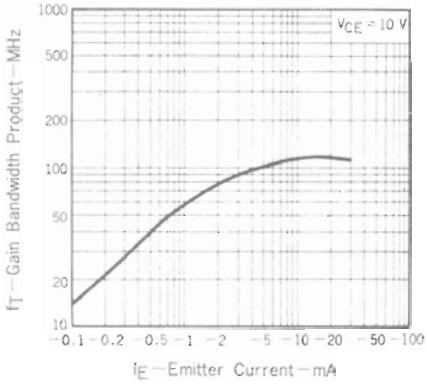
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



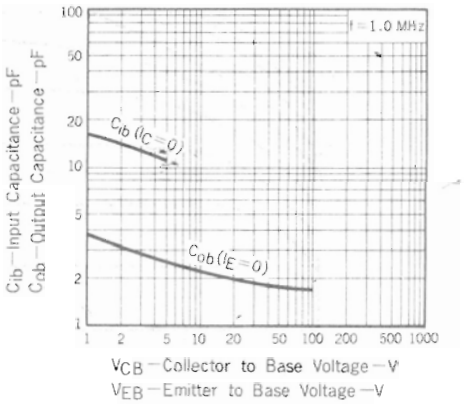
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE
vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC1957

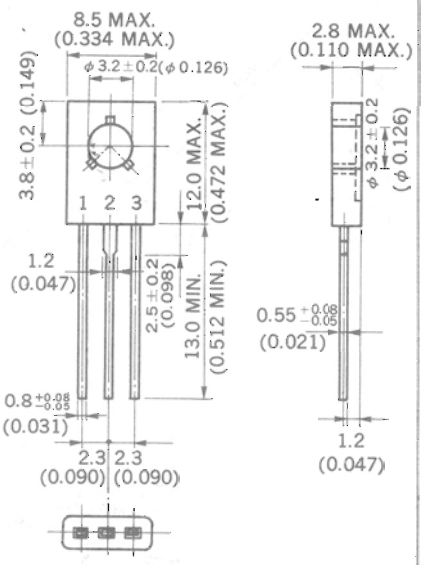
DESCRIPTION

The 2SC1957 is designed for use in large signal output amplifier stages. This device is intended for use in Citizen Band and Ham Band communications equipment operating to 50 MHz.
High breakdown voltage allows to withstand an open and short circuit load in AM operation.

FEATURES

- Specified 12 V, 27 MHz characteristics.
  - Output Power 1.8 W TYP.
  - Power Gain 17 dB TYP.
  - Efficiency 65 % TYP.
- High breakdown voltage 75 V MIN.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	150 °C Maximum	

Maximum Power Dissipations

Total Power Dissipation (T_a = 25 °C)	0.75	W
Total Power Dissipation (T_c = 25 °C)	5.0	W

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	75	V
V_{CEO}	Collector to Emitter Voltage	40	V
V_{EBO}	Emitter to Base Voltage	4.0	V
I_C	Collector Current	1.0	A

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	20	90	200	—	V_{CE} = 10 V, I_C = 0.5 A
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 10 V, I_C = 150 mA
C_{ob}	Output Capacitance		14	20	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
P_O	Output Power	1.0	1.8		W	V_{CC} = 12 V, f = 27 MHz
η_c	Collector Efficiency	60			%	P_i = 35 mW See Test Circuit.
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 40 V, I_E = 0
$V_{CE(sat)}$	Collector Saturation Voltage		0.3	0.5	V	I_C = 0.5 A, I_B = 0.05 A

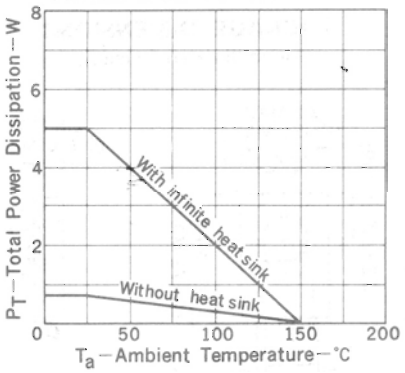
Classification of h_{FE}

Rank	S	R	Q	K
Range	30 to 60	45 to 90	80 to 200	20 to 200

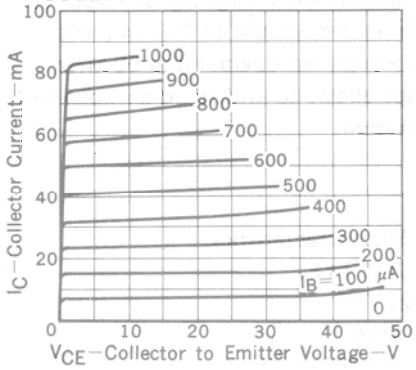
Test Conditions : V_{CE} = 10 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

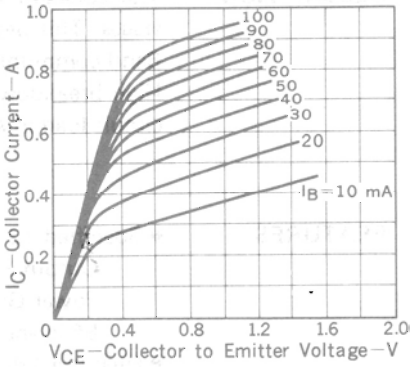
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



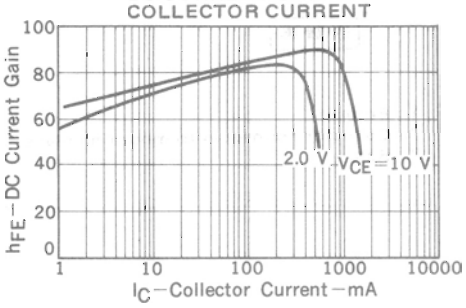
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



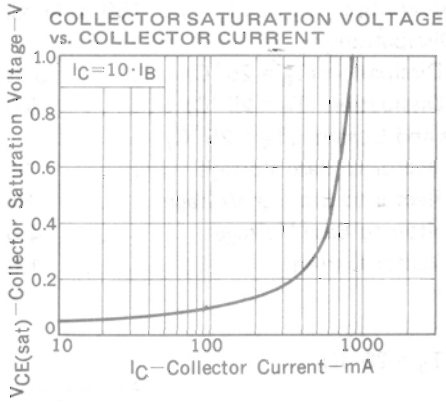
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



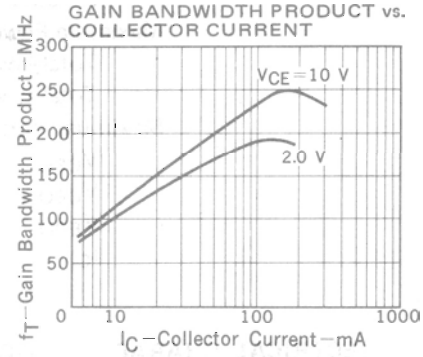
DC CURRENT GAIN vs. COLLECTOR CURRENT



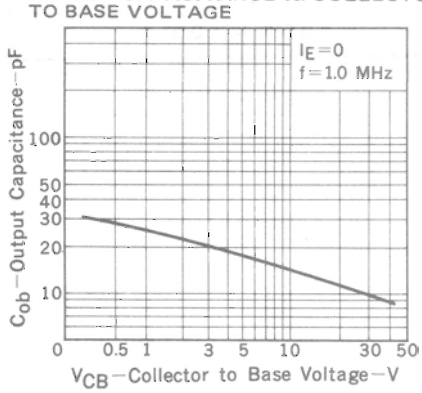
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



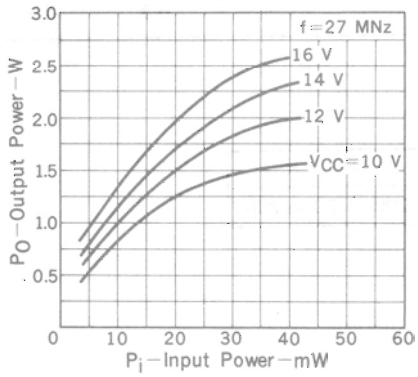
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



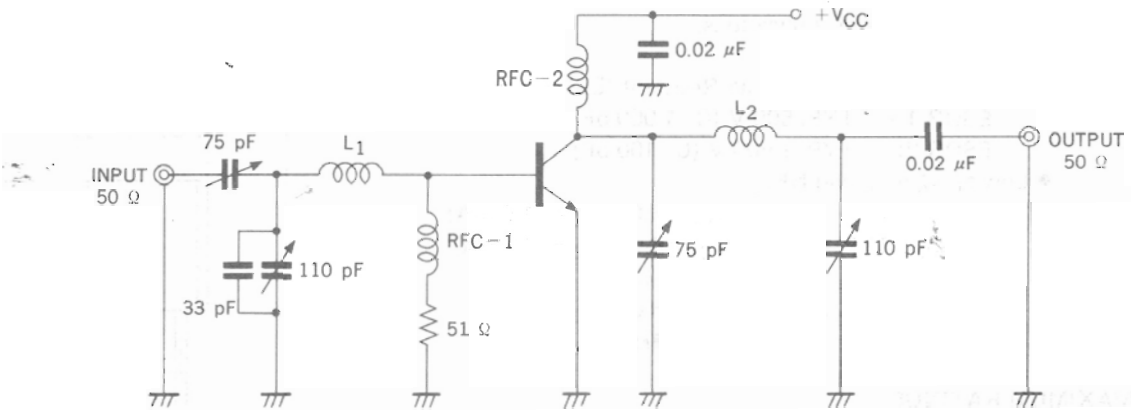
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



OUTPUT POWER vs. INPUT POWER



OUTPUT POWER TEST CIRCUIT (27 MHz)



L_1 : 5T, ϕ 0.4 mm Enameled wire, ϕ 8 mm Bobbin with ferrite rod
L_2 : 4T, ϕ 0.4 mm Enameled wire, ϕ 8 mm Bobbin with ferrite rod

RFC-1: 20T, ϕ 0.4 mm Enameled wire, ϕ 8 mm Bobbin
RFC-2: 17T, ϕ 0.4 mm Enameled wire, ϕ 8 mm Bobbin

NEC
ELECTRON DEVICE

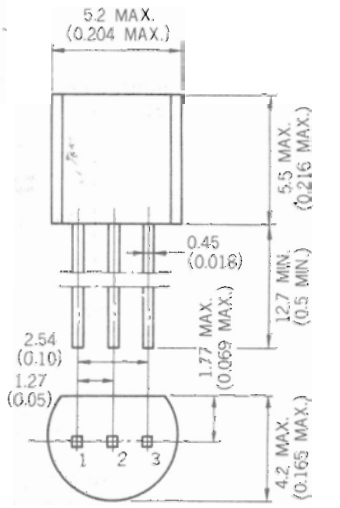
NPN SILICON TRANSISTOR
2SC2000

DESCRIPTION The 2SC2000 is designed for use in AM/RF stage of CAR RADIO and general purpose applications.

FEATURES

- High Electrostatic-Discharge-Resistant (E-B reverse bias)
  - ESDR 1: TYP. 500 V (C=1 000 pF)
  - ESDR 2: TYP. 1 600 V (C=100 pF)
- Low f_T, $C_c \cdot r_{b'b}$ and NF.
  - f_T: TYP. 70 MHz (V_{CE}=6.0 V, I_E=−1.0 mA)
  - $C_c \cdot r_{b'b}$: TYP. 6.0 ps (V_{CB}=6.0 V, I_E=−10 mA, f=31.9 MHz)
  - NF: TYP. 3.0 dB (V_{CE}=6.0 V, I_C=1.0 mA, f=1.0 MHz, R_G=500 Ω)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (Ta=25 °C)

- V_{CBO} Collector to Base Voltage ..... 60 V
- V_{CEO} Collector to Emitter Voltage ..... 50 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 200 mA
- I_B Base Current ..... 20 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	90	180	–	V_{CE}=6.0 V, I_C=1.0 mA
C_{ob}	Output Capacitance		3.7	4.5	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
f_T	Gain Bandwidth Product	40	70		MHz	V_{CE}=6.0 V, I_E=−1.0 mA
NF	Noise Figure		3.0		dB	V_{CE}=6.0 V, I_C=1.0 mA, R_G=500 Ω, f=1.0 MHz
ESDR	Electrostatic-Discharge-Resistant		500		V	See Test Circuit
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	600	650	700	mV	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		110	300	mV	I_C=100 mA, I_B=10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.85	1.5	V	I_C=100 mA, I_B=10 mA
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		6.0	15	ps	V_{CB}=6.0 V, I_E=−10 mA, f=31.9 MHz

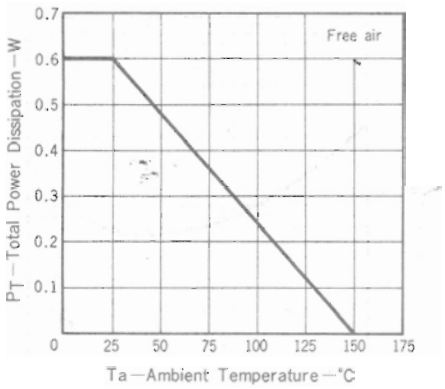
Classification of h_{FE}

Rank	M	L	K
Range	40 – 80	60 – 120	90 – 180

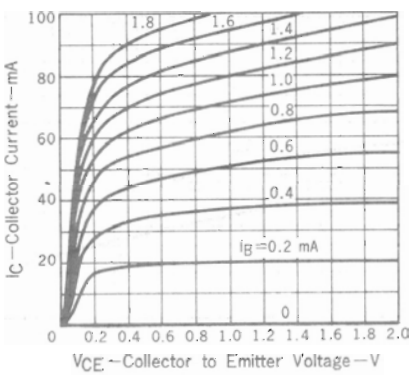
h_{FE} Test Conditions : V_{CE}=6.0 V, I_C=1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

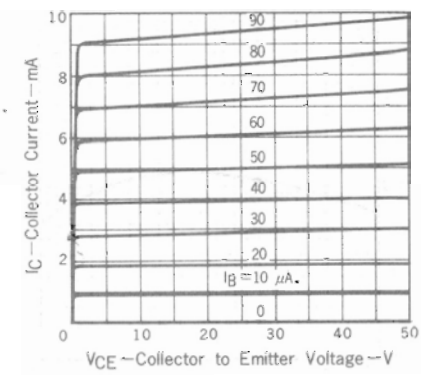
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



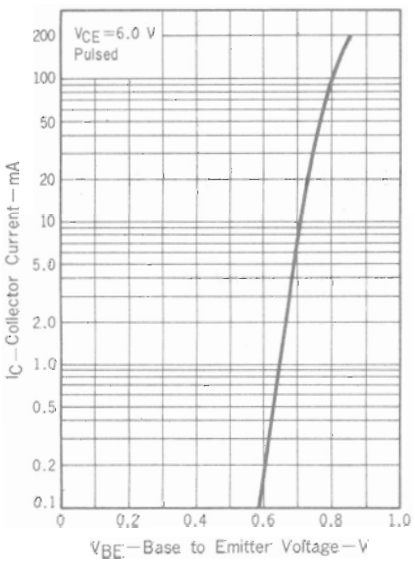
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



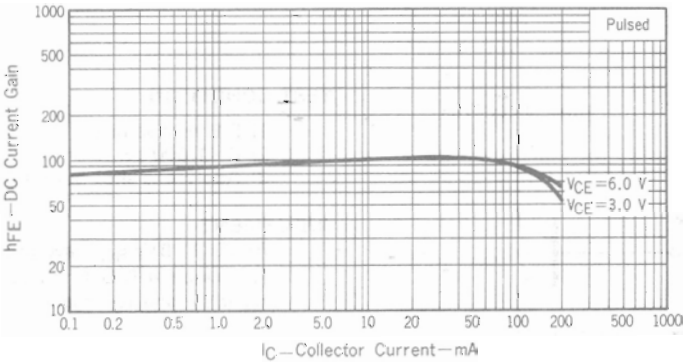
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



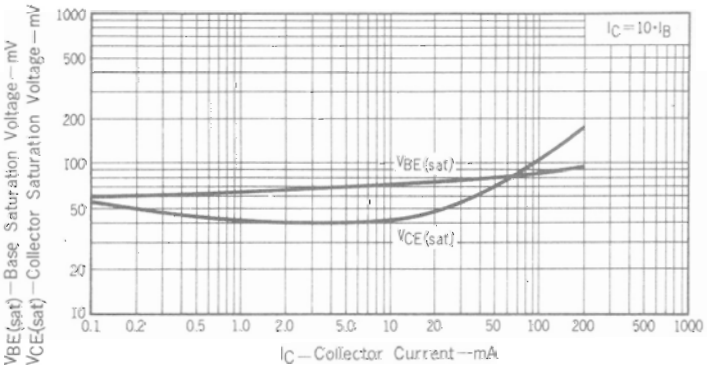
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



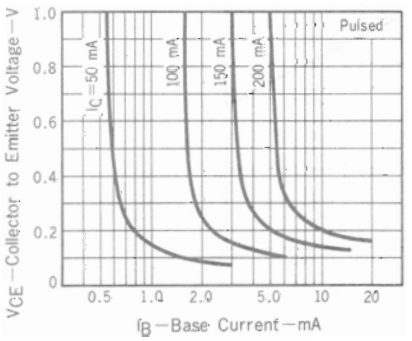
DC CURRENT GAIN vs. COLLECTOR CURRENT



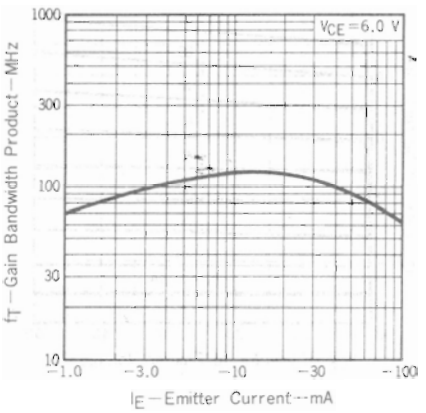
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



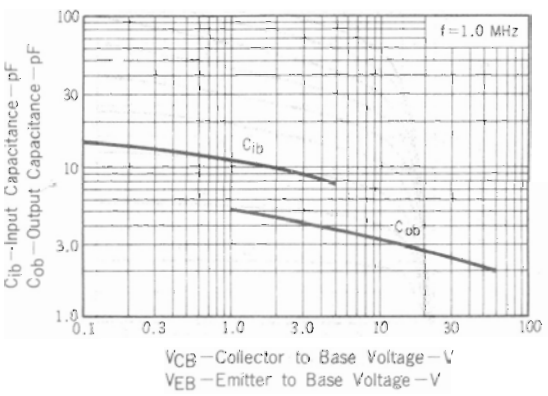
COLLECTOR TO EMITTER VOLTAGE vs. BASE CURRENT



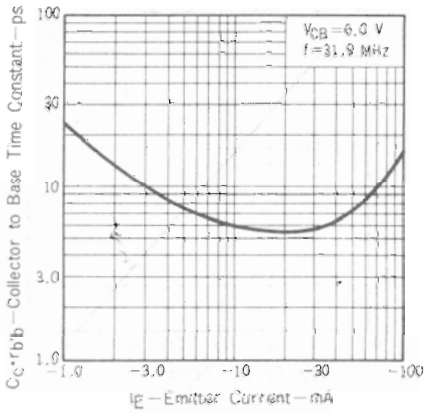
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



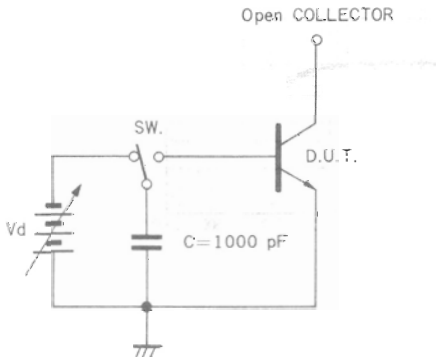
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



COLLECTOR TO BASE TIME CONSTANT vs EMITTER CURRENT



ELECTROSTATIC-DISCHARGE-RESISTANT TEST CIRCUIT



TEST CONDITION

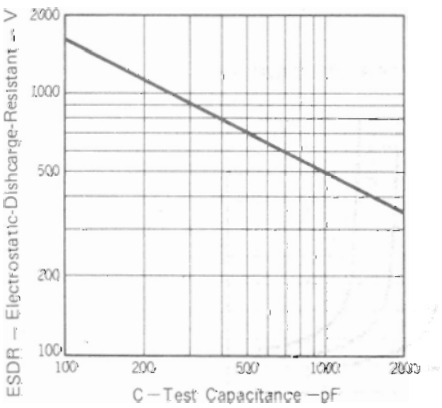
1) E-B reverse bias
2) C = 1 000 pF
3) Apply one shot pulse to D.U.T. (Device Under the Test) by SW.

JUDGEMENT

REJECT: BV_{EBO} waveform defect

As a result if D.U.T. is not rejected, apply higher voltage to capacitor and test again.

ELECTROSTATIC-DISCHARGE-RESISTANT vs. CAPACITANCE



NEC
ELECTRON DEVICE

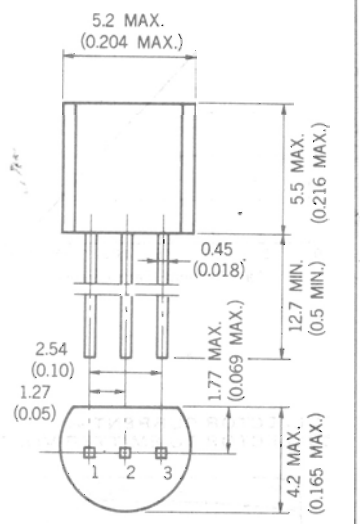
NPN SILICON TRANSISTOR
2SC2001

DESCRIPTION The 2SC2001 is designed for use in output stage of portable RADIO and cassette type tape recorder, general purpose applications.

FEATURES

- High total power dissipation.
  P_T : 600 mW
- High h_{FE} and low $V_{CE(sat)}$
  h_{FE} (I_C = 100 mA) : 200 TYP.
  $V_{CE(sat)}$ (700 mA) : 0.20 V TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... 30 V
- V_{CEO} Collector to Emitter Voltage ..... 25 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 700 mA
- I_B Base Current ..... 150 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	90	200	400	–	V_{CE} = 1.0 V, I_C = 100 mA
h_{FE2}*	DC Current Gain	50	140		–	V_{CE} = 1.0 V, I_C = 700 mA
C_{ob}	Collector to Base Capacitance		13	25	pF	V_{CB} = 6.0 V, I_E = 0 f = 1.0 MHz
f_T	Gain Bandwidth Product	50	170		MHz	V_{CE} = 6.0 V, I_E = −10 mA
V_{BE}*	Base to Emitter Voltage	600	640	700	mV	V_{CE} = 6.0 V, I_C = 10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.2	0.6	V	I_C = 700 mA, I_B = 70 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.95	1.2	V	I_C = 700 mA, I_B = 70 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0

* Pulsed PW ≦ 350 μs, duty cycle ≦ 2.0 %

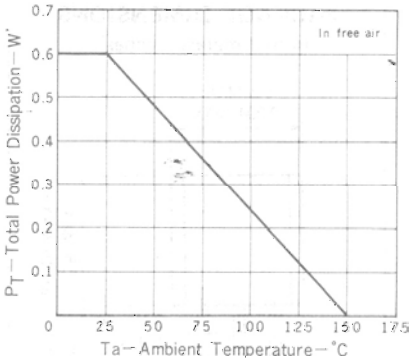
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

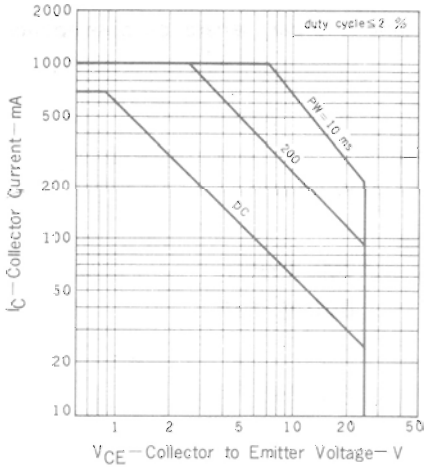
h_{FE} Test Conditions : V_{CE} = 1.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

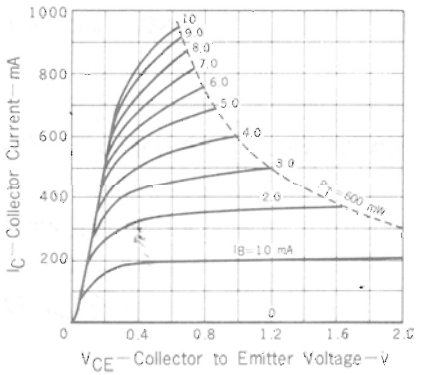
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



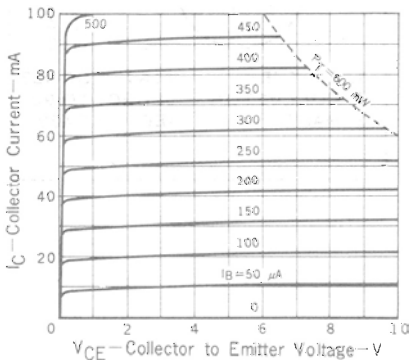
SAFE OPERATING AREAS (TRANSIENT THERMAL RESIDUANCE)



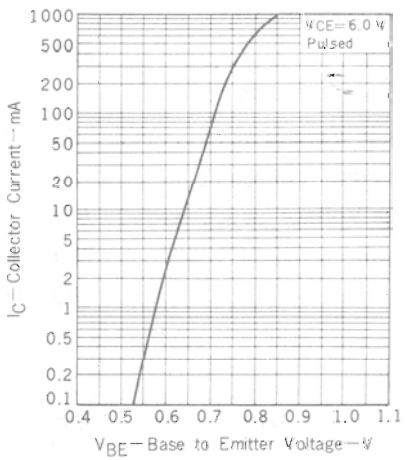
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



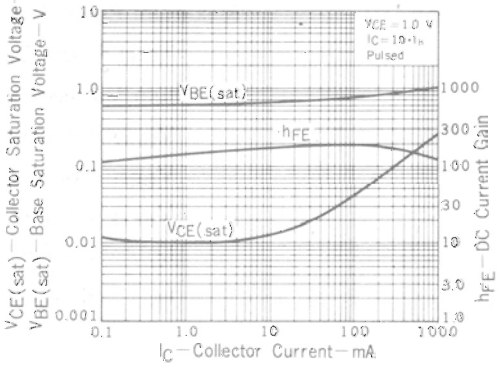
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



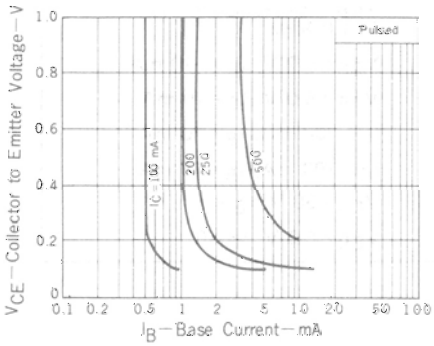
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



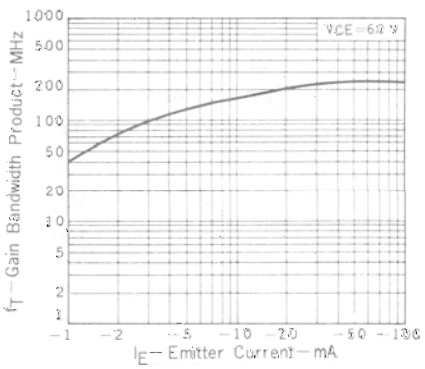
DC CURRENT GAIN, BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



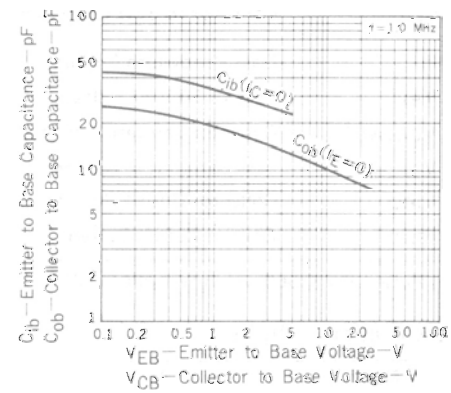
COLLECTOR TO EMITTER VOLTAGE vs. BASE CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

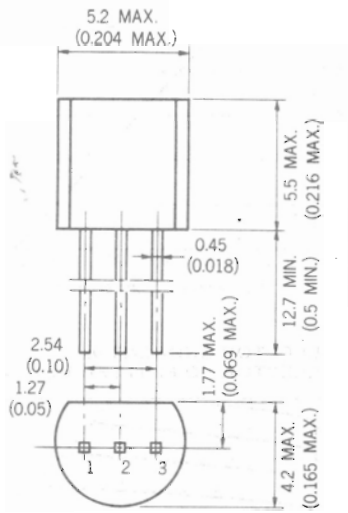
NPN SILICON TRANSISTOR
2SC2002

DESCRIPTION The 2SC2002 is designed for use in driver stage of high voltage audio equipments.

FEATURES

- High total power dissipation.
  P_T : 600 mW
- High h_{FE} and high voltage.
  h_{FE} (I_C = 50 mA) : 200 TYP.
  V_{CEO} : 60 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	300	mA
I_B	Base Current	60	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	90	200	400	–	V_{CE} = 1.0 V, I_C = 50 mA
h_{FE2}*	DC Current Gain	30	80		–	V_{CE} = 2.0 V, I_C = 300 mA
C_{ob}	Collector to Base Capacitance		7.0	15	pF	V_{CB} = 6.0 V, I_E = 0 f = 1.0 MHz
f_T	Gain Bandwidth Product	50	140		MHz	V_{CE} = 6.0 V, I_E = −10 mA
V_{BE}*	Base to Emitter Voltage	600	645	700	mV	V_{CE} = 6.0 V, I_C = 10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.15	0.6	V	I_C = 300 mA, I_B = 30 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.86	1.2	V	I_C = 300 mA, I_B = 30 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_E = 0

*Pulsed PW ≦ 350 μs, duty cycle ≦ 2.0 %.

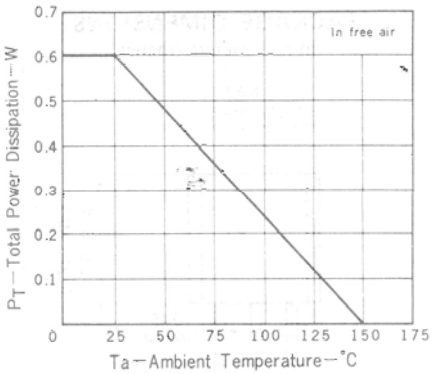
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

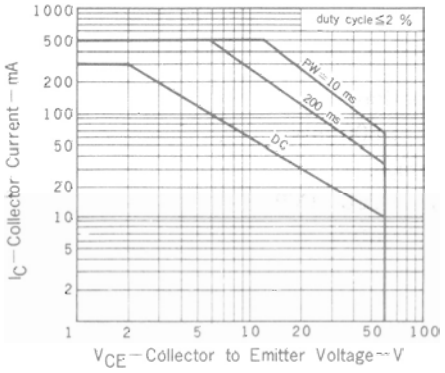
h_{FE} Test Conditions : V_{CE} = 1.0 V, I_C = 50 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

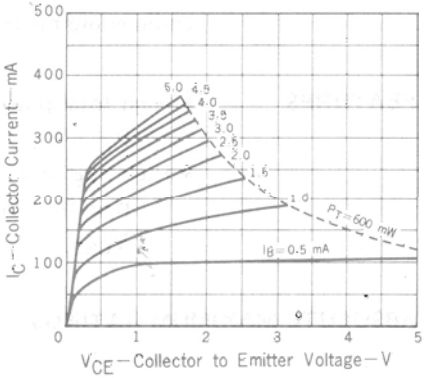
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



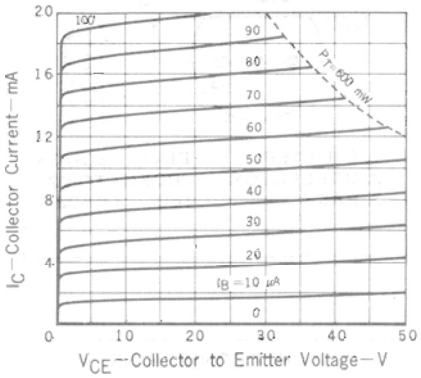
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



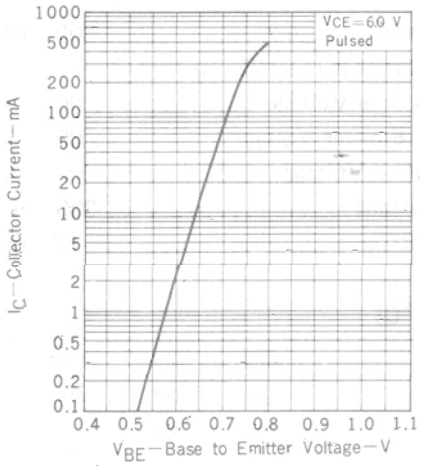
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



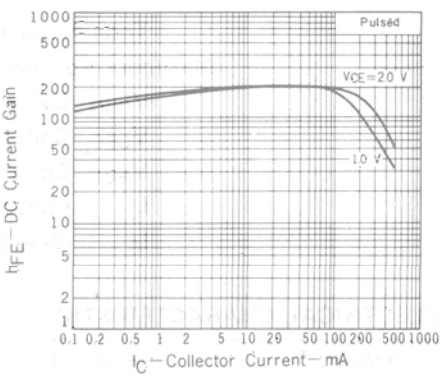
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



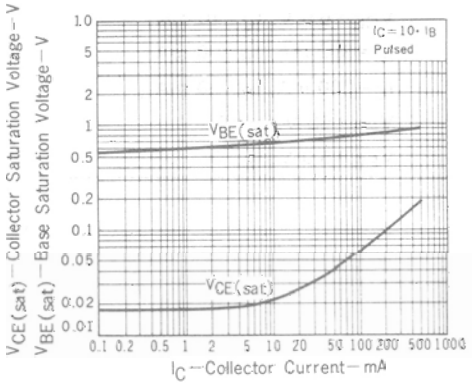
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



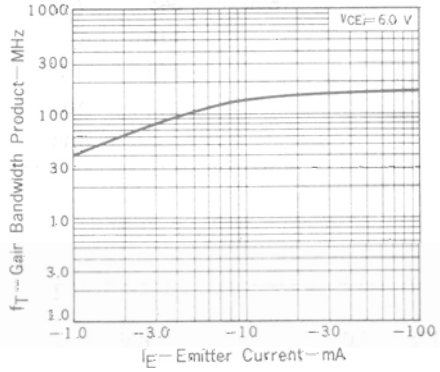
DC CURRENT GAIN vs. COLLECTOR CURRENT



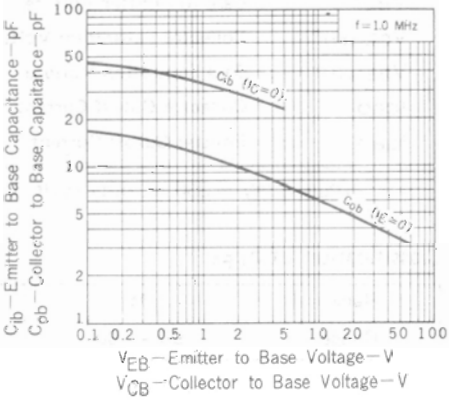
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

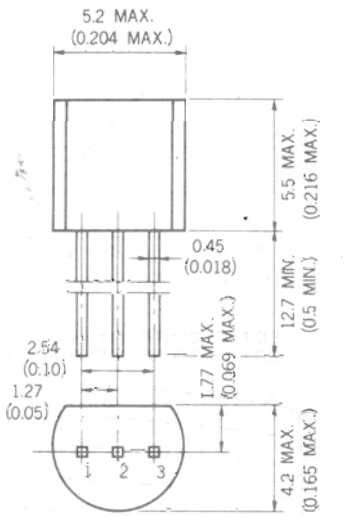
NPN SILICON TRANSISTOR
2SC2003

DESCRIPTION The 2SC2003 is designed for use in driver stage of high voltage audio equipments.

FEATURES

- High total power dissipation.
  P_T : 600 mW
- High h_{FE} and high voltage.
  h_{FE} (I_C = 50 mA) : 200 TYP.
  V_{CEO} : 80 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	80	V
V_{CEO}	Collector to Emitter Voltage	80	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	300	mA
I_B	Base Current	60	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	90	200	400	—	V_{CE} = 1.0 V, I_C = 50 mA
h_{FE2}*	DC Current Gain	30	80		—	V_{CE} = 2.0 V, I_C = 300 mA
C_{ob}	Collector to Base Capacitance		7.0	15	pF	V_{CB} = 6.0 V, I_E = 0 f = 1.0 MHz
f_T	Gain Bandwidth Product	50	140		MHz	V_{CE} = 6.0 V, I_E = −10 mA
V_{BE}*	Base to Emitter Voltage	600	645	700	mV	V_{CE} = 6.0 V, I_C = 10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.15	0.6	V	I_C = 300 mA, I_B = 30 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.86	1.2	V	I_C = 300 mA, I_B = 30 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_E = 0

*Pulsed PW ≦ 350 μs, duty cycle ≦ 2.0 %.

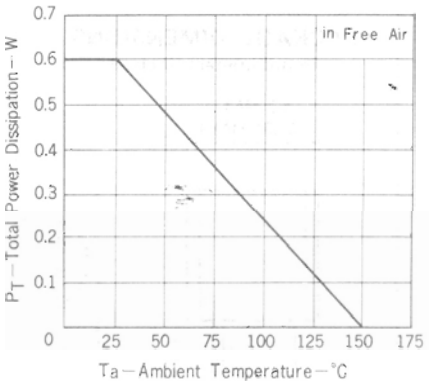
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

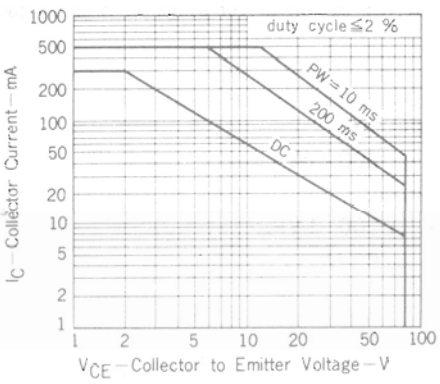
h_{FE} Test Conditions : V_{CE} = 1.0 V, I_C = 50 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

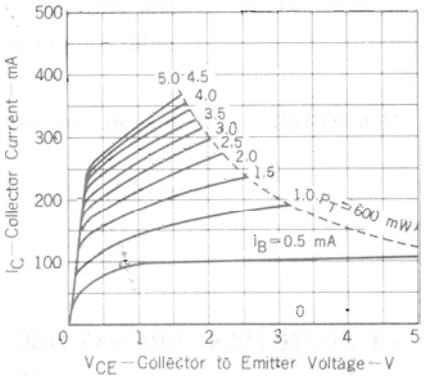
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



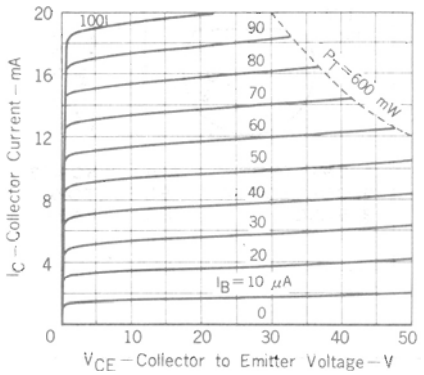
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



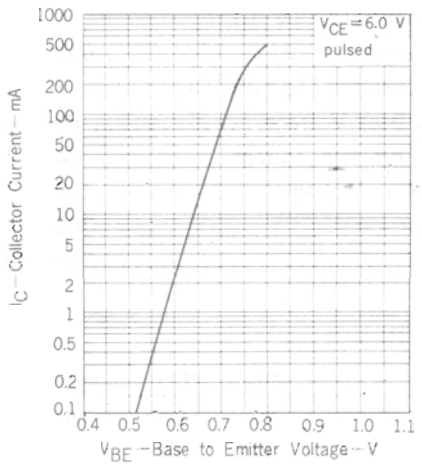
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



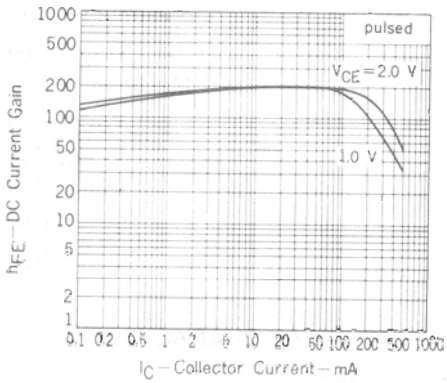
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



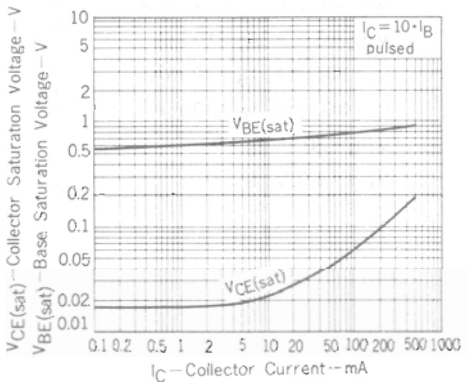
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



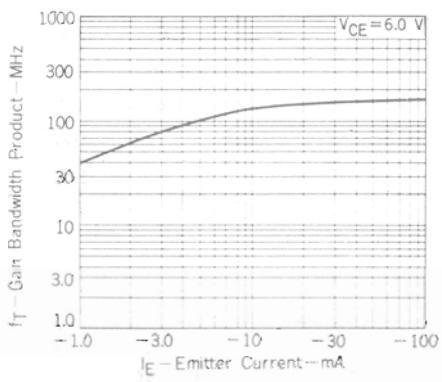
DC CURRENT GAIN vs. COLLECTOR CURRENT



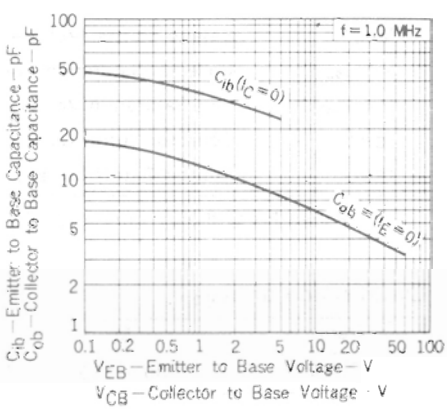
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

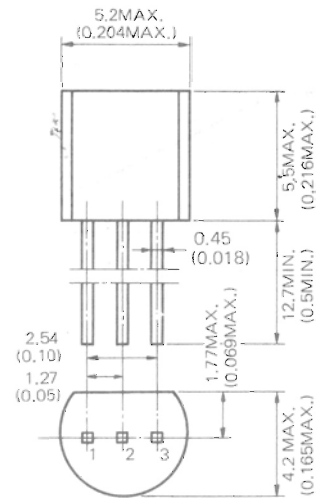
NPN SILICON TRANSISTOR
2SC2026

DESCRIPTION Suitable for low noise amplifier in the VHF to UHF band.

FEATURES

- NF 3.0 dB TYP. @f = 500 MHz
- G_{pe} 15 dB TYP. @f = 500 MHz
- f_T 2.0 GHz TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . . 14 V
- V_{EBO} Emitter to Base Voltage . . . . . 3.0 V
- I_C Collector Current . . . . . 50 mA

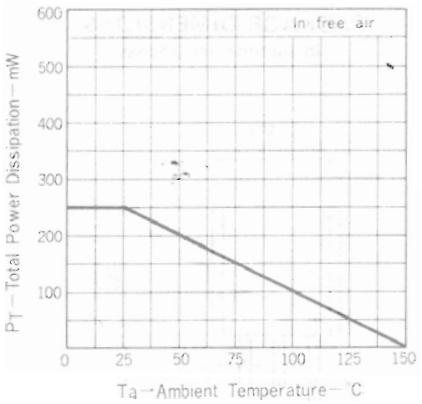
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	25	80	200		V_{CE}=10 V, I_C=10 mA
f_T	Gain Bandwidth Product	1.5	2.0		GHz	V_{CE}=10 V, I_E=10 mA
C_{ob}	Output Capacitance		0.75	1.1	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz*
G_{pe}	Power Gain	13	15		dB	V_{CE}=10 V, I_C=10 mA, f=500 MHz
NF	Noise Figure		3.0	4.0	dB	V_{CE}=10 V, I_C=3.0 mA, f=500 MHz, R_G=50 Ω
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB}=2.0 V, I_C=0

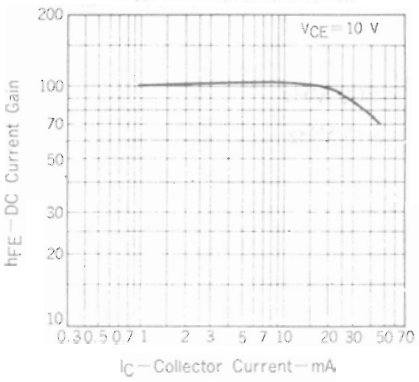
* The emitter terminal should be connected to the gurad terminal of the three-terminal capacitance bridge.

TYPICAL CHARACTERISTICS (Ta=25 °C)

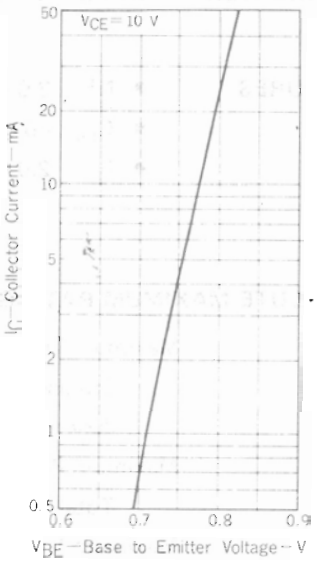
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



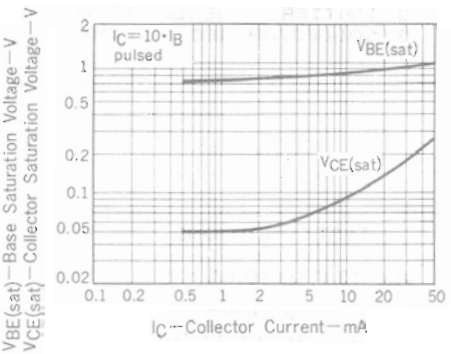
DC CURRENT GAIN vs. COLLECTOR CURRENT



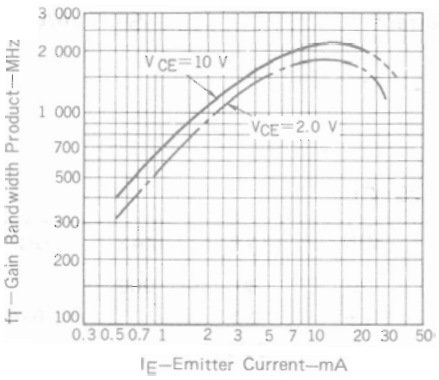
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



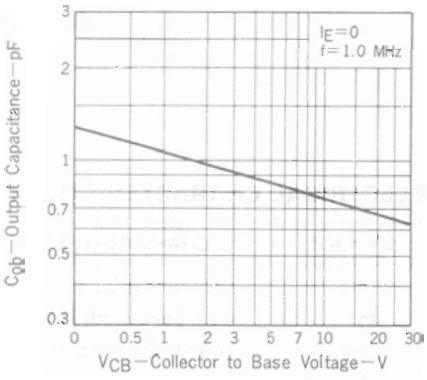
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



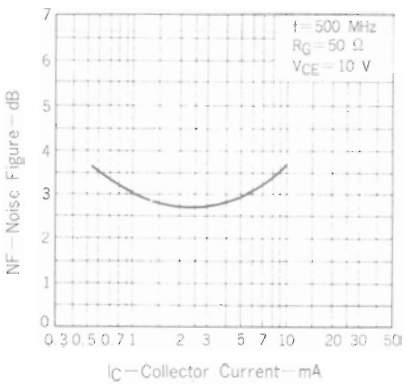
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NOISE FIGURE vs. COLLECTOR CURRENT

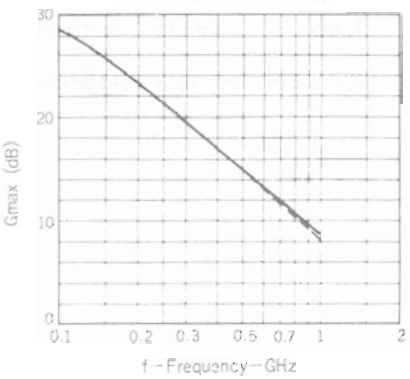


TYPICAL S-PARAMETER

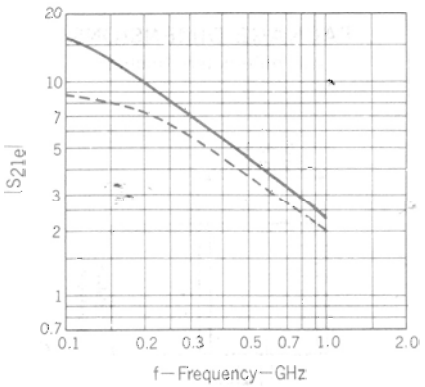
Z_o = 50 Ω
V_{CE} = 10 V
——— I_C = 10 mA
– – – – – I_C = 3.0 mA

$$G_{max} = |S_{21}|^2 \cdot \frac{1}{1-|S_{11}|^2} \cdot \frac{1}{1-|S_{22}|^2}$$

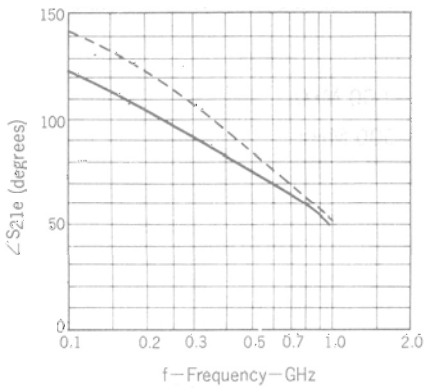
G_{max} vs. FREQUENCY



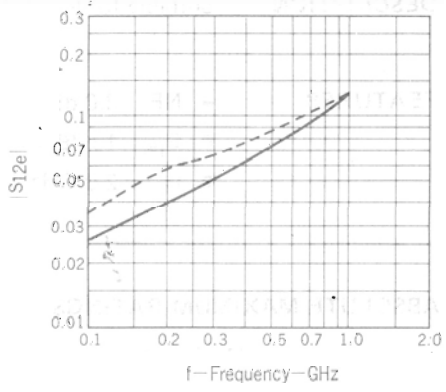
FORWARD TRANSFER COEFFICIENT vs. FREQUENCY



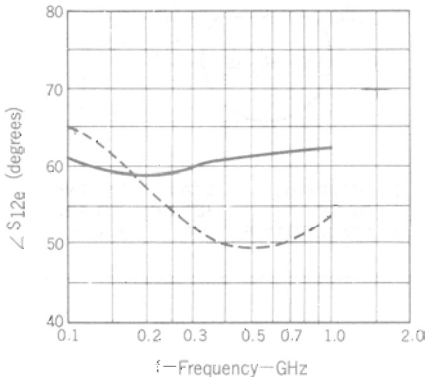
FORWARD TRANSFER COEFFICIENT vs. FREQUENCY



REVERSE TRANSFER COEFFICIENT vs. FREQUENCY



REVERSE TRANSFER COEFFICIENT vs. FREQUENCY



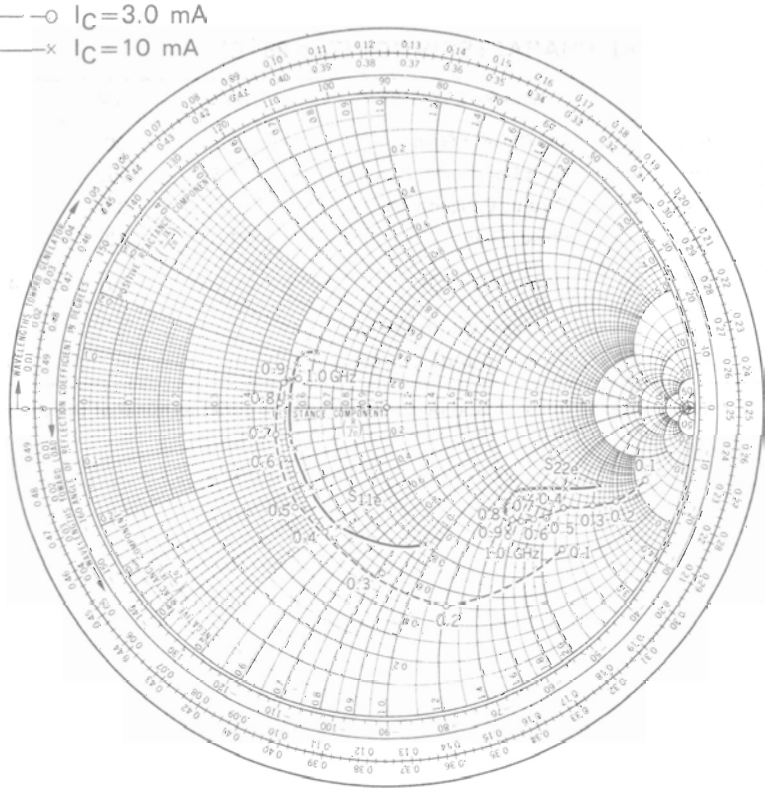
S_{11e}, S_{22e}

V_{CE}=10 V

Z_o=50 Ω

○——○ I_C=3.0 mA

×——× I_C=10 mA



NEC
ELECTRON DEVICE

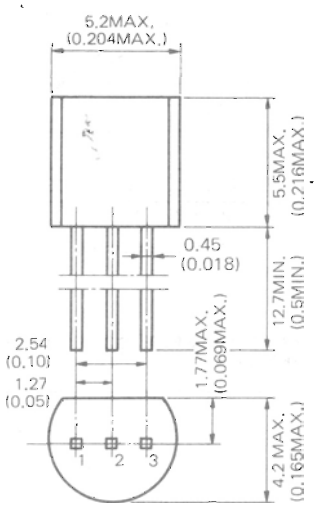
NPN SILICON TRANSISTOR
2SC2037

DESCRIPTION Suitable for low noise amplifier in the VHF to UHF band.

FEATURES

- NF 3.0 dB TYP. @f = 500 MHz
- G_{pe} 13 dB TYP. @f = 500 MHz
- f_T 2.0 GHz TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . . 14 V
- V_{EBO} Emitter to Base Voltage . . . . . 3.0 V
- I_C Collector Current . . . . . 50 mA

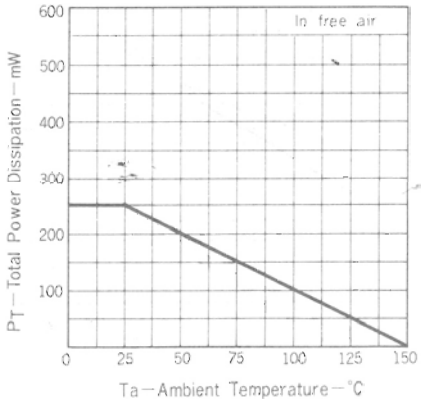
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	25	80	200		V_{CE}=10 V, I_C=10 mA
f_T	Gain Bandwidth Product	1.5	2.0		GHz	V_{CE}=10 V, I_E=10 mA
C_{ob}	Output Capacitance		0.9	1.3	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz*
G_{pe}	Power Gain	11	13		dB	V_{CE}=10 V, I_C=10 mA, f=500 MHz
NF	Noise Figure		3.0	4.0	dB	V_{CE}=10 V, I_C=3.0 mA, f=500 MHz, R_G=50 Ω
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB}=2.0 V, I_C=0

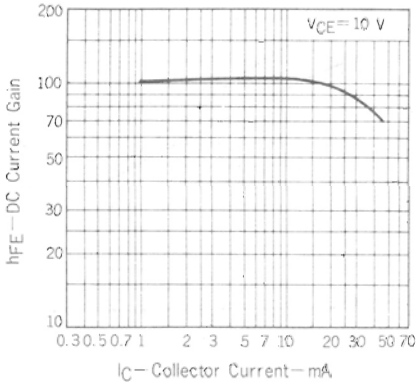
* The emitter terminal should be connected to the gurad terminal of the three-terminal capacitance bridge.

TYPICAL CHARACTERISTICS (Ta=25 °C)

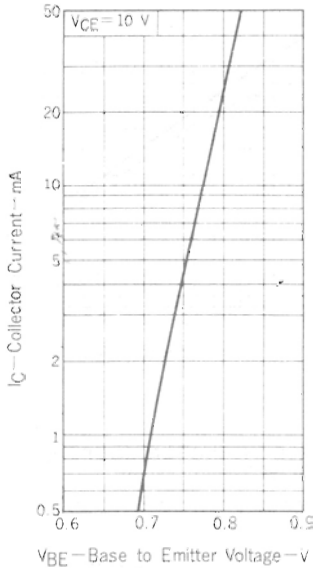
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



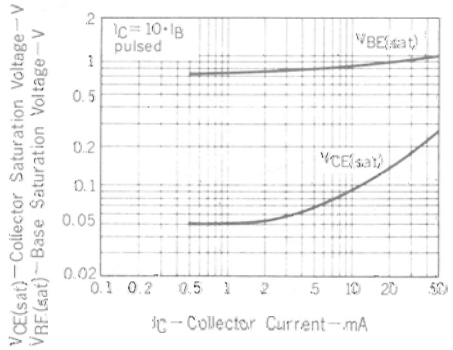
DC CURRENT GAIN vs. COLLECTOR CURRENT



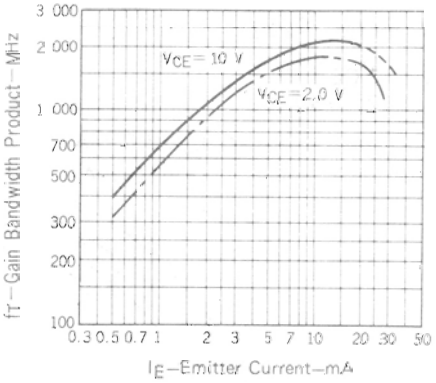
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



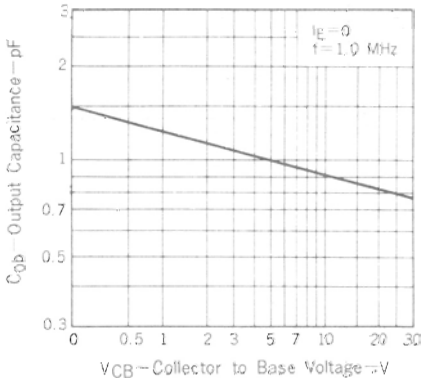
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



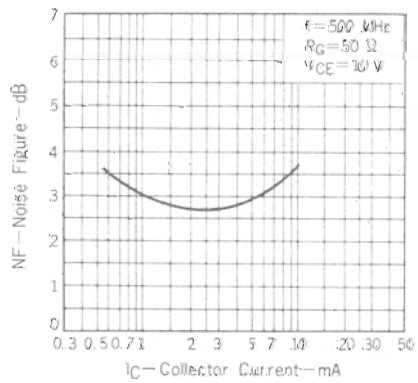
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NOISE FIGURE vs. COLLECTOR CURRENT



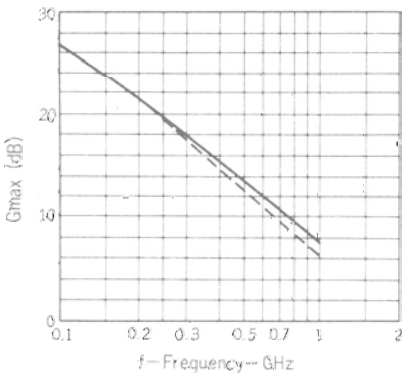
TYPICAL S-PARAMETER

$Z_o = 50\ \Omega$
$V_{CE} = 10\ V$

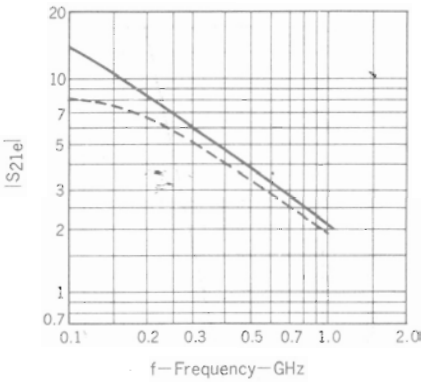
——— $I_C = 10$ mA
– – – – $I_C = 3.0$ mA

$$G_{max} = |S_{21}|^2 \cdot \frac{1}{1 - |S_{11}|^2} \cdot \frac{1}{1 - |S_{22}|^2}$$

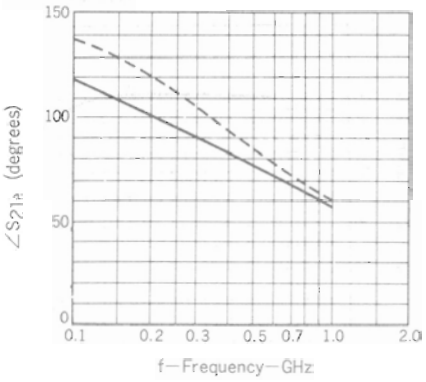
G_{max} vs. FREQUENCY



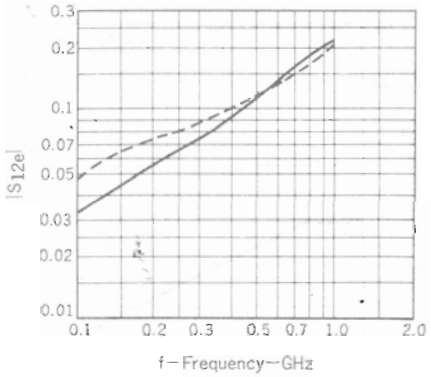
FORWARD TRANSFER COEFFICIENT vs. FREQUENCY



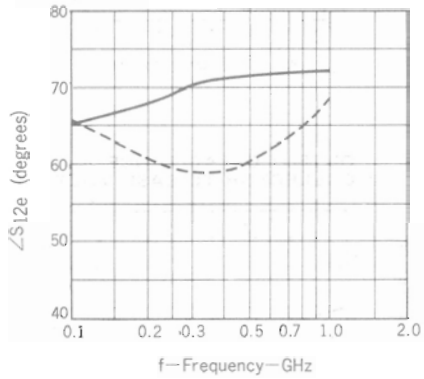
FORWARD TRANSFER COEFFICIENT vs. FREQUENCY



REVERSE TRANSFER COEFFICIENT vs. FREQUENCY



REVERSE TRANSFER COEFFICIENT vs. FREQUENCY



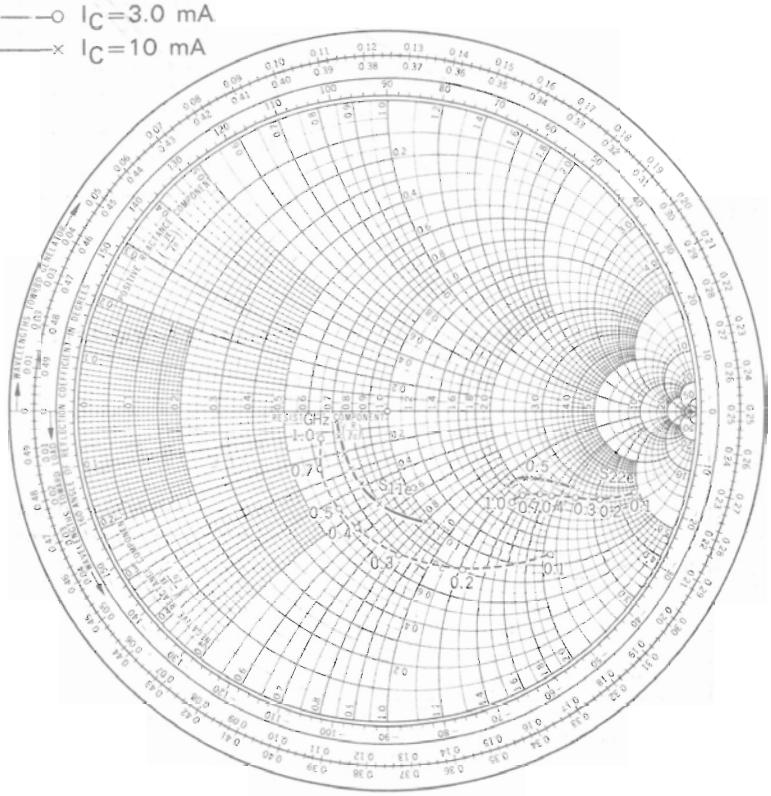
S_{11e}, S_{22e}

V_{CE}=10 V

Z_o=50 Ω

○———○ I_C=3.0 mA

×———× I_C=10 mA



NEC
ELECTRON DEVICE

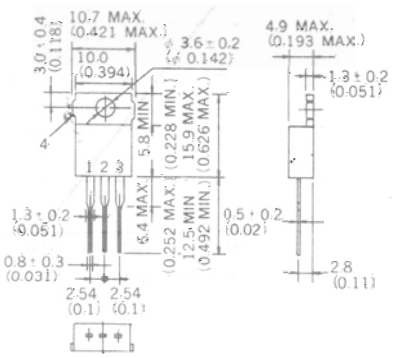
NPN SILICON POWER TRANSISTOR
2SC2333

DESCRIPTION The 2SC2333 is NPN silicon triple diffused transistor designed for switching regulator, DC-DC converter and ultrasonic appliance applications.

FEATURES

- High speed switching.
- Low collector saturation voltage.
- Specified of reverse biased SOA with inductive loads.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 500 V
- V_{CEO} Collector to Emitter Voltage . . . . . 400 V
- V_{EBO} Emitter to Base Voltage . . . . . 7.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 2.0 A
- $I_{C(pulse)}$ Collector Current (pulse)* . . . . . 4.0 A
- $I_{B(DC)}$ Base Current (DC) . . . . . 1.0 A

* PW ≤ 350 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			1.0	μs	I_C = 0.5 A, I_{B1} = −I_{B2} = 0.1 A
t_{stg}	Storage Time			2.5	μs	R_L = 300 Ω, V_{CC} ≒ 150 V
t_f	Fall Time			1.0	μs	See Test Circuit.
h_{FE1}	DC Current Gain**	20		80	—	V_{CE} = 5.0 V, I_C = 0.1 A
h_{FE2}	DC Current Gain**	10			—	V_{CE} = 5.0 V, I_C = 0.5 A
$V_{CE(sat)}$	Collector Saturation Voltage**			1.0	V	I_C = 0.5 A, I_B = 0.1 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.2	V	I_C = 0.5 A, I_B = 0.1 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 0.5 A, I_B = 0.1 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 0.5 A, I_{B1} = −I_{B2} = 0.1 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 1.0 A, I_{B1} = 0.2 A, −I_{B2} = 0.2 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −5.0 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −5.0 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

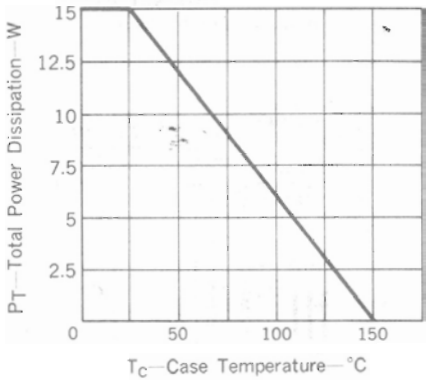
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

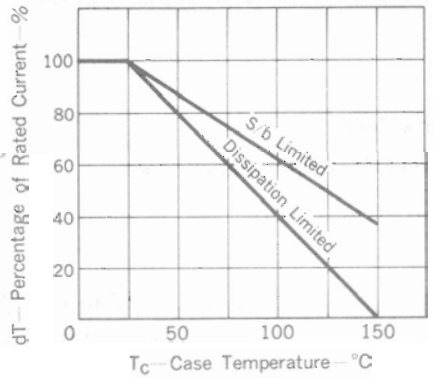
Test Conditions : V_{CE} = 5.0 V, I_C = 0.1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

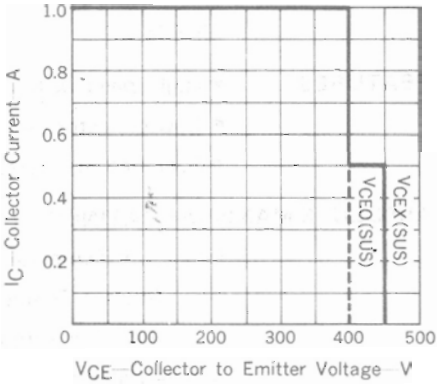
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



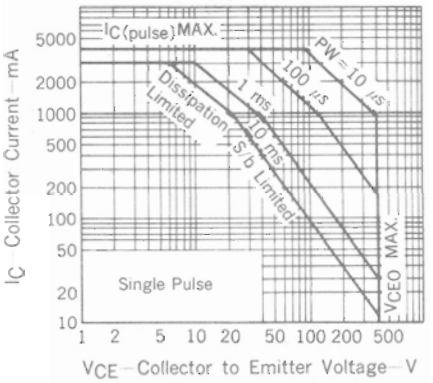
DERATING CURVE OF SAFE OPERATING AREA



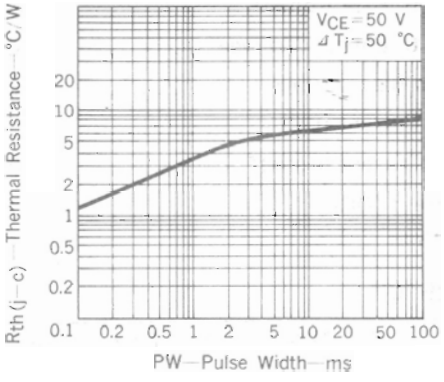
REVERSE BIAS SAFE OPERATING AREA



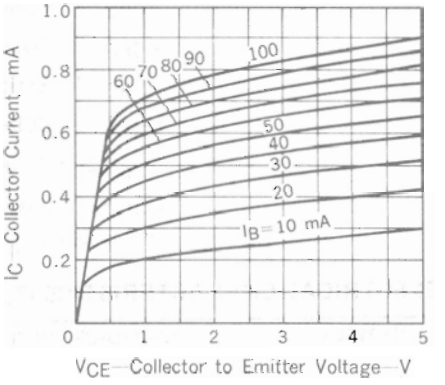
FORWARD BIAS SAFE OPERATING AREA



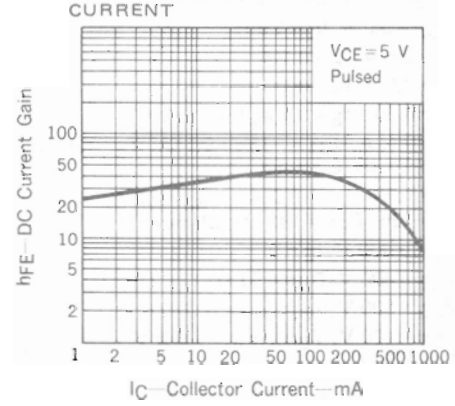
TRANSIENT THERMAL RESISTANCE



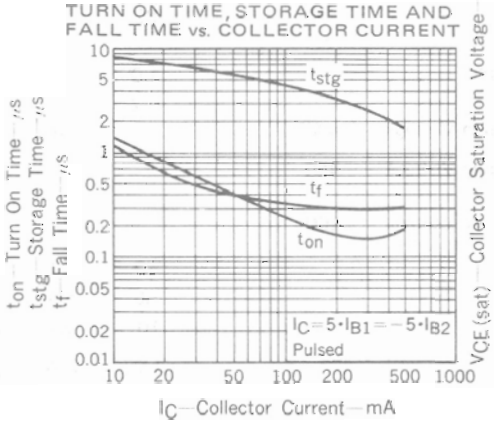
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



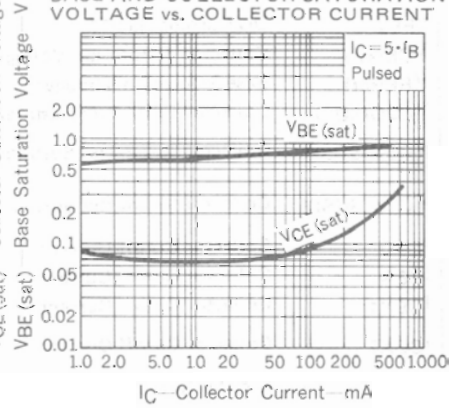
DC CURRENT GAIN vs. COLLECTOR CURRENT



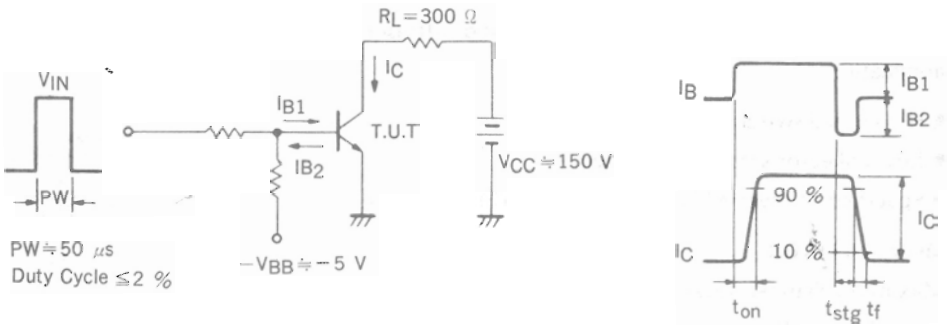
TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

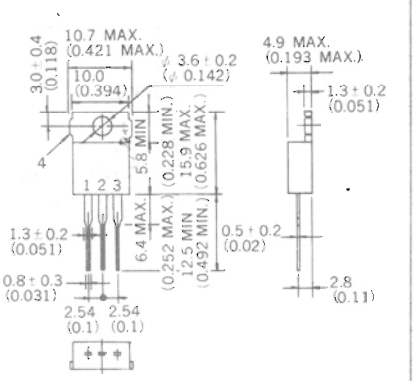
NPN SILICON POWER TRANSISTOR
2SC2335

DESCRIPTION The 2SC2335 is NPN silicon triple diffused transistor designed for switching regulator, DC-DC converter and ultrasonic appliance applications.

FEATURES

- High speed switching.
- Low collector saturation voltage.
- Specified of reverse biased SOA with inductive loads.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 40 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 500 V
- V_{CEO} Collector to Emitter Voltage . . . . . 400 V
- V_{EBO} Emitter to Base Voltage . . . . . 7.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 7.0 A
- $I_{C(pulse)}$ Collector Current (pulse)* . . . . . 15 A
- $I_{B(DC)}$ Base Current (DC) . . . . . 3.5 A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			1.0	μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.6 A
t_{stg}	Storage Time			2.5	μs	R_L = 50 Ω, V_{CC} = 150 V
t_f	Fall Time			1.0	μs	See Test Circuit.
h_{FE1}	DC Current Gain**	20		80	—	V_{CE} = 5.0 V, I_C = 0.1 A
h_{FE2}	DC Current Gain**	20		80	—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE3}	DC Current Gain**	10			—	V_{CE} = 5.0 V, I_C = 3.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			1.0	V	I_C = 3.0 A, I_B = 0.6 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.2	V	I_C = 3.0 A, I_B = 0.6 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 3.0 A, I_B = 0.6 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.6 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 6.0 A, I_{B1} = 2.0 A, −I_{B2} = 0.6 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

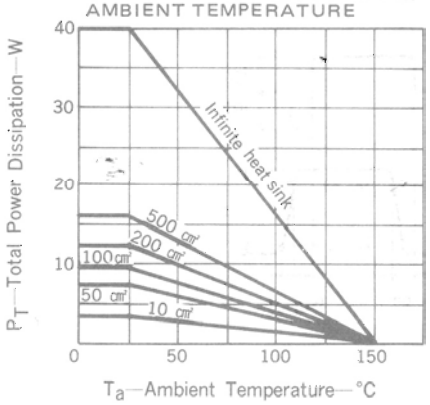
Classification of h_{FE2}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

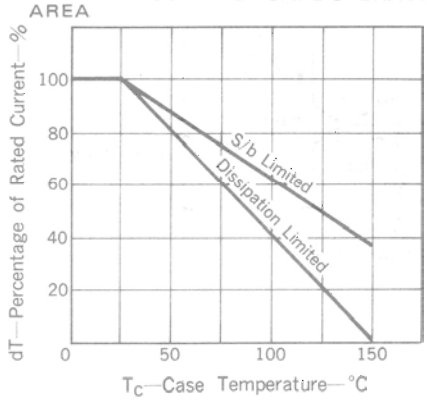
Test Conditions : V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

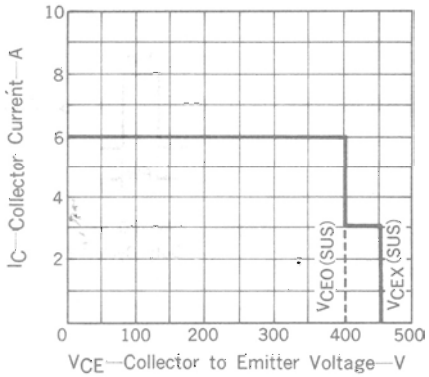
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



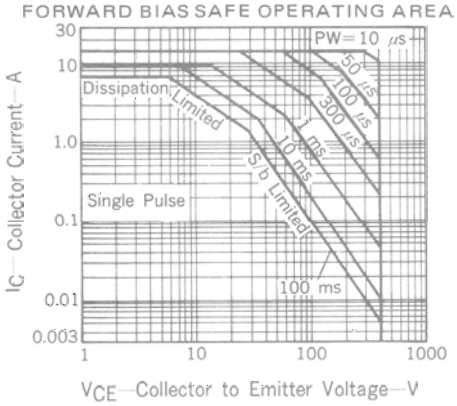
DERATING CURVE OF SAFE OPERATING AREA



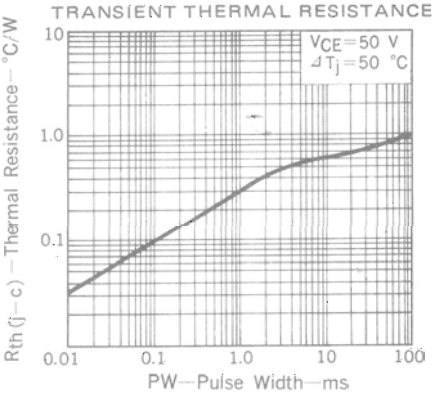
REVERSE BIAS SAFE OPERATING AREA



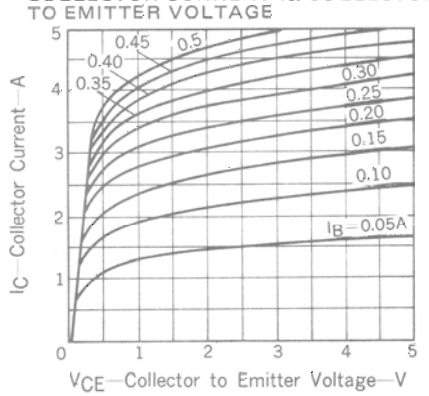
FORWARD BIAS SAFE OPERATING AREA



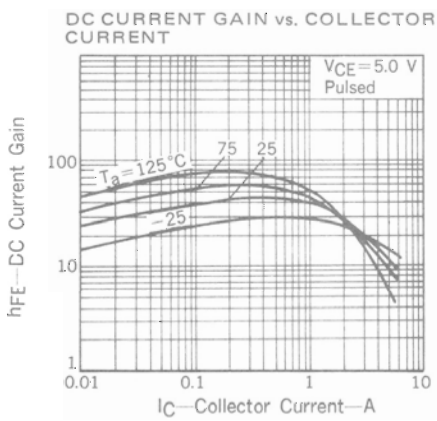
TRANSIENT THERMAL RESISTANCE



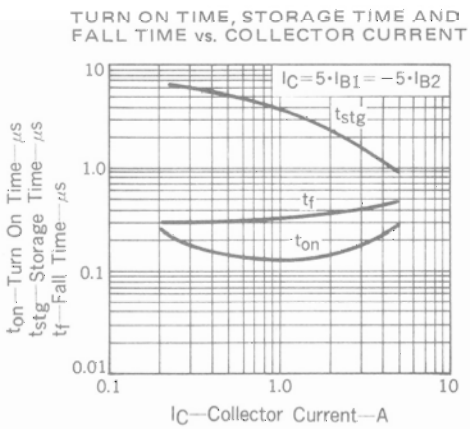
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



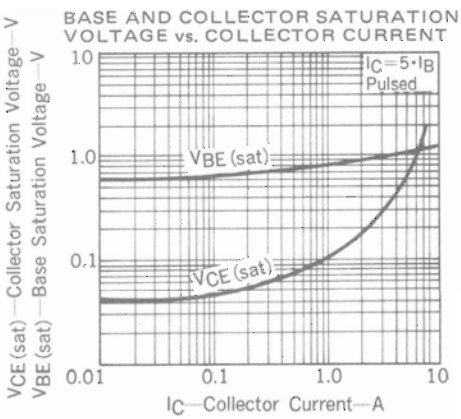
DC CURRENT GAIN vs. COLLECTOR CURRENT



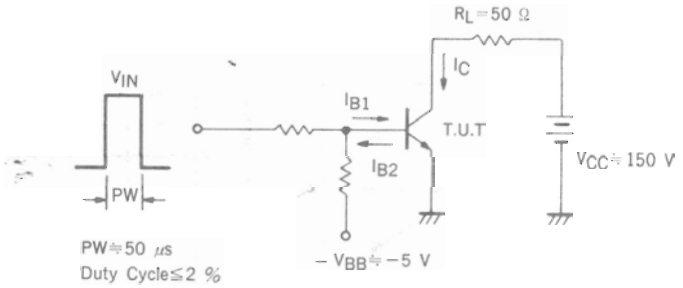
TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

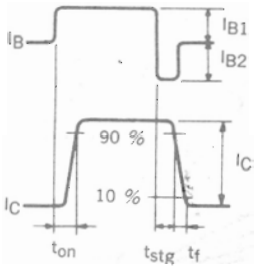


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

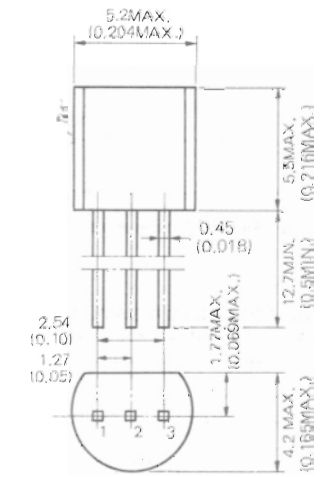
NPN SILICON TRANSISTOR
2SC2352

DESCRIPTION The 2SC2352 is an NPN silicon epitaxial transistor intended for use as a VHF mixer in a tuner of a TV receiver. The device features are high conversion gain and low distortion.

FEATURES

- Low C_{re}. : 0.4 pF TYP.
- High conversion gain. : 15 dB TYP.
- Excellent h_{FE} linearity.

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
IEC : PA33
JEDEC : TO-92

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage	20	V
V_{EBO}	Emitter to Base Voltage	4.0	V
I_C	Collector Current	30	mA
I_B	Base Current.	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	100	200		V_{CE}=10 V, I_C=5.0 mA
f_T	Gain Bandwidth Product	500	850		MHz	V_{CE}=10 V, I_E=−5.0 mA
C_{re}	Feed Back Capacitance		0.4	0.7	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
G_C	Conversion Gain	12			dB	V_{CE}=10 V, I_E=−5.0 mA f=200 MHz, f_L=258 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=20 V, I_E=0
$V_{CE(sat)}$	Collector Saturation Voltage			0.5	V	I_C=10 mA, I_B=1.0 mA

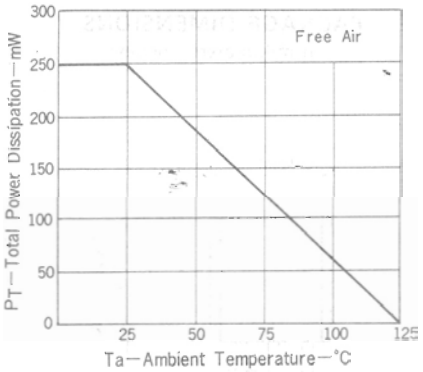
Classification of h_{FE}

Rank	L	K
Range	60 – 120	100 – 200

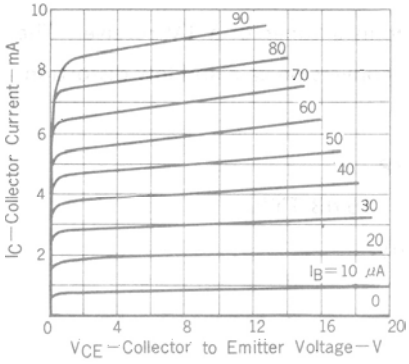
h_{FE} Test Conditions: V_{CE}=10 V, I_C=5.0 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

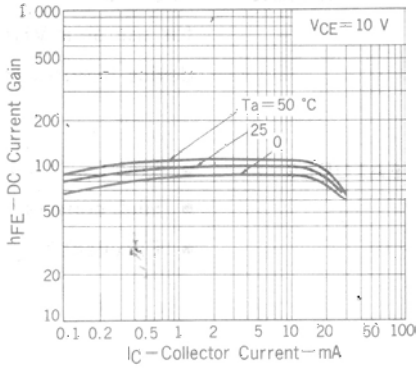
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



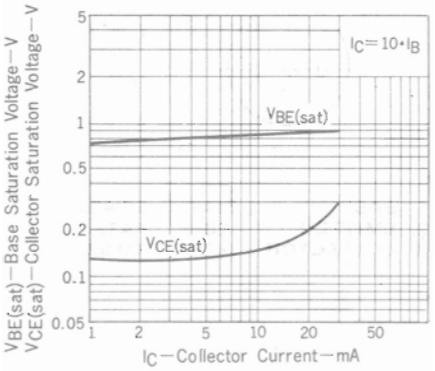
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



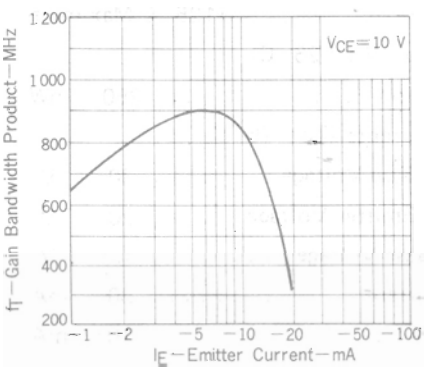
DC CURRENT GAIN vs. COLLECTOR CURRENT



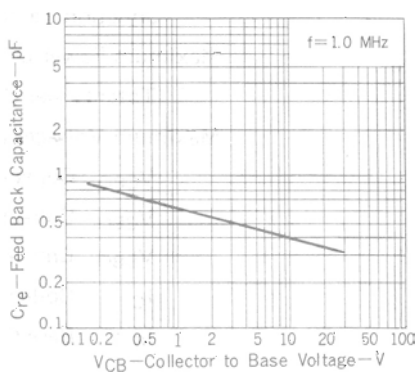
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



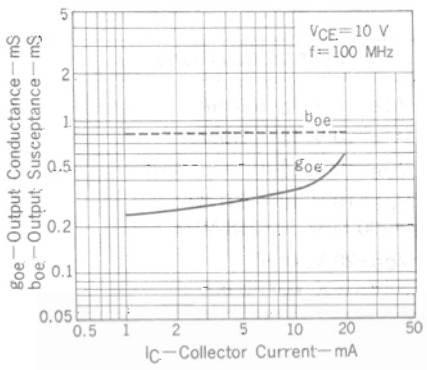
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



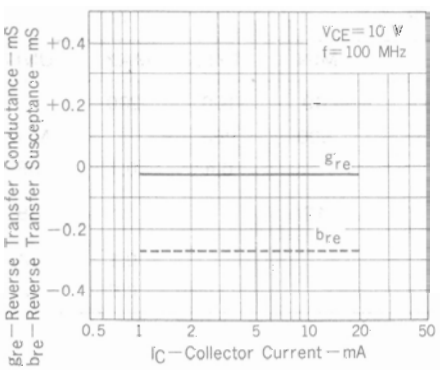
FEED BACK CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



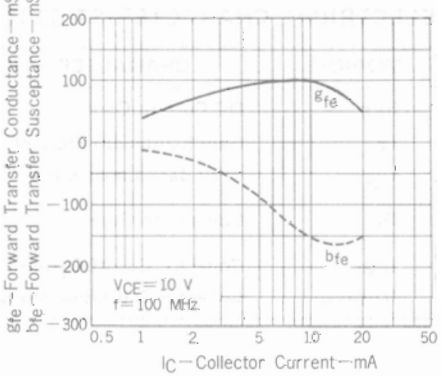
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



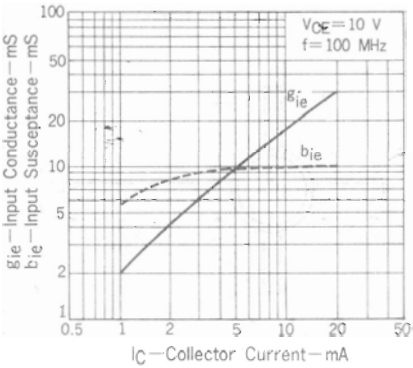
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



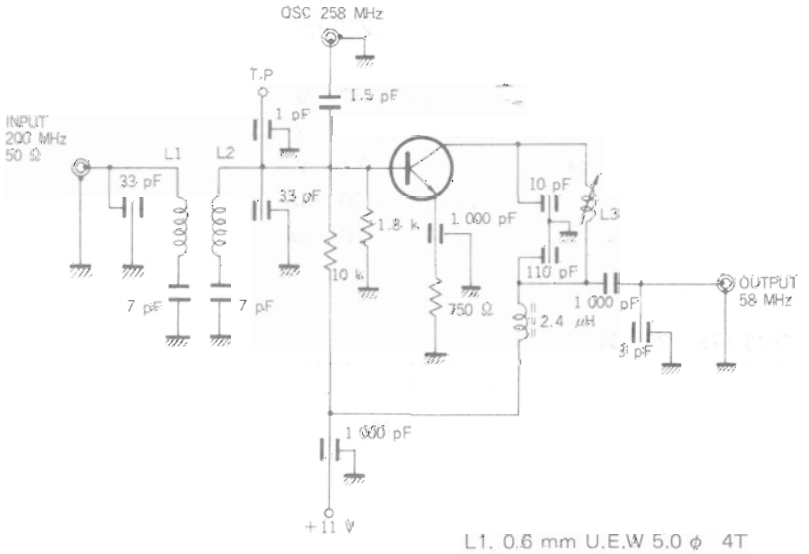
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



INPUT ADMITTANCE vs.
COLLECTOR CURRENT



CONVERSION GAIN TEST CIRCUIT



L1. 0.6 mm U.E.W 5.0 ϕ 4T
L2. 0.6 mm U.E.W 5.0 ϕ 4T
L3. 0.3 mm U.E.W 6.0 ϕ 11T

NEC
ELECTRON DEVICE

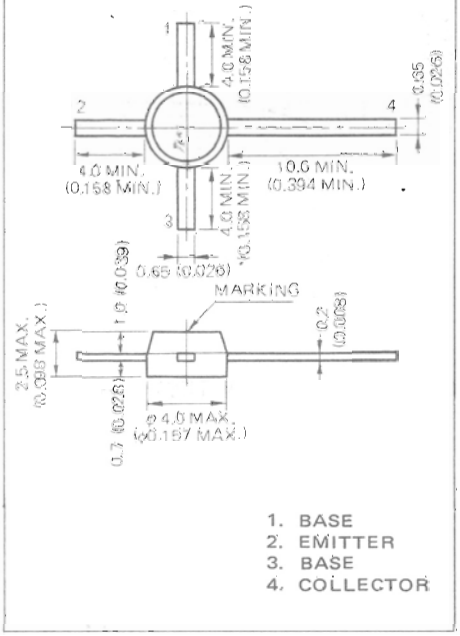
NPN SILICON TRANSISTOR
2SC2353

DESCRIPTION The 2SC2353 is specially designed for use as VHF and UHF mixer in a tuner of TV receiver. The influence of mirror effect is little by balanced base.

FEATURES

- Packaged in tiny plastic mold package.
- Low noise. NF : 4.0 dB (TYP.)
- High conversion gain. G_{cb} : 12.5 dB (TYP.)
- Balanced base.

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Currents (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage	14	V
V_{EBO}	Emitter to Base Voltage	3.0	V
I_C	Collector Current	50	mA
I_B	Base Current	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	100	180		V_{CE}=10 V, I_C=5.0 mA
f_T	Gain Bandwidth Product	1.5	2.3		GHz	V_{CE}=10 V, I_E=−5.0 mA
C_{ob}	Output Capacitance		0.85	1.0	pF	V_{CB}=10 V, I_E=0, f=1 MHz
NF	Noise Figure		4.0	5.0	dB	V_{CB}=10 V, I_E=−5.0 mA, f=900 MHz
G_{pb}	Power Gain	14	16		dB	V_{CB}=10 V, I_E=−5.0 mA, f=900 MHz
G_{cb}	Conversion Gain	10	12.5		dB	f_{RF}=900 MHz, f_{LOC}=930 MHz V_{CB}=10 V, I_E=−5.0 mA Local level=110 mV
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0

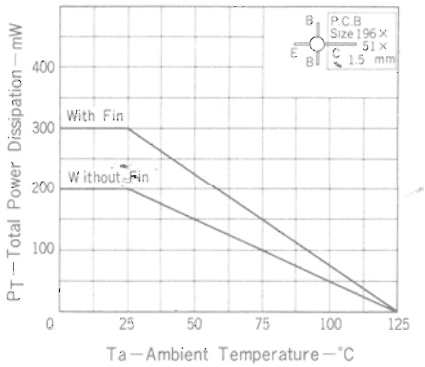
Classification of h_{FE}

Rank	L	K
Range	60 – 120	90 – 180

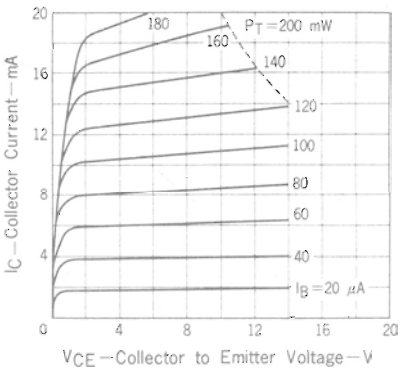
h_{FE} Test Conditions : V_{CE}=10 V, I_C=5.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

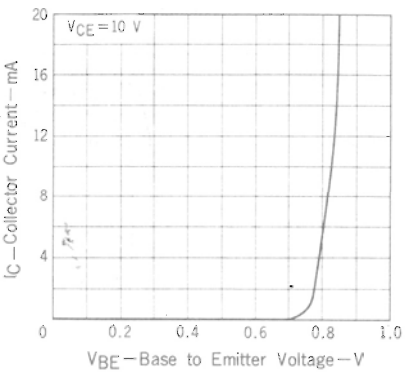
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



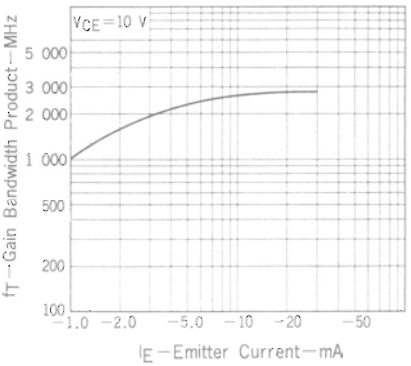
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



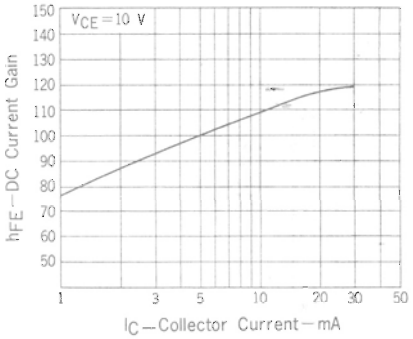
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



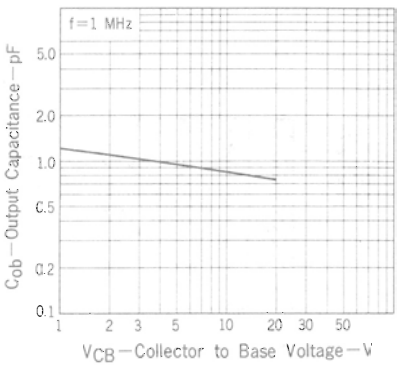
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT

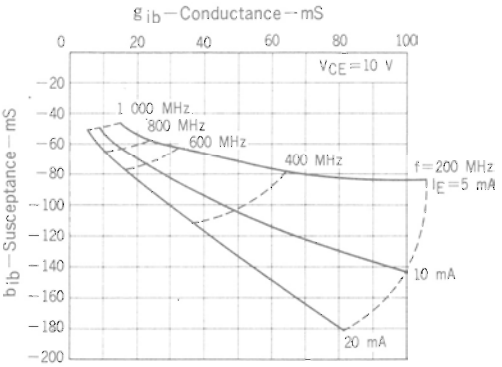


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

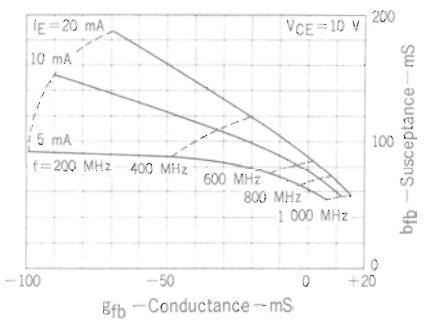


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

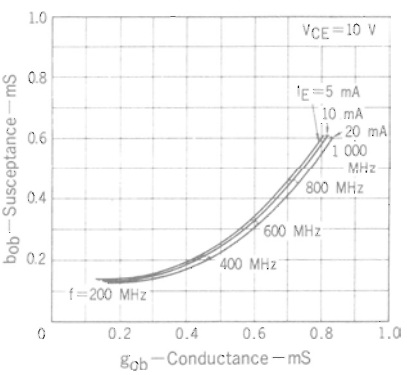
y_{ib} vs. f



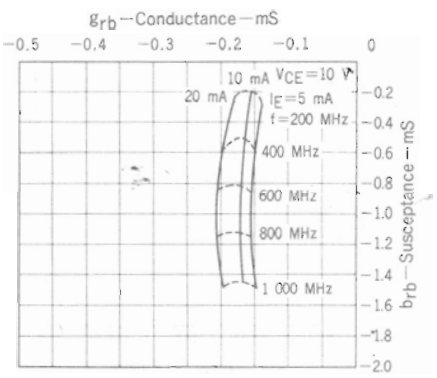
y_{fb} vs. f



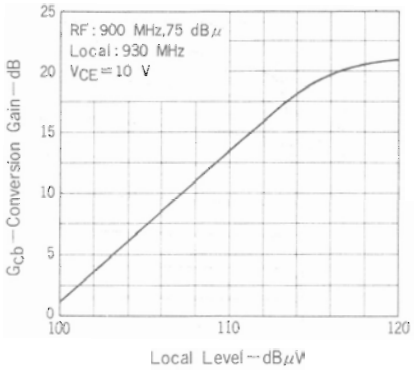
y_{ob} vs. f



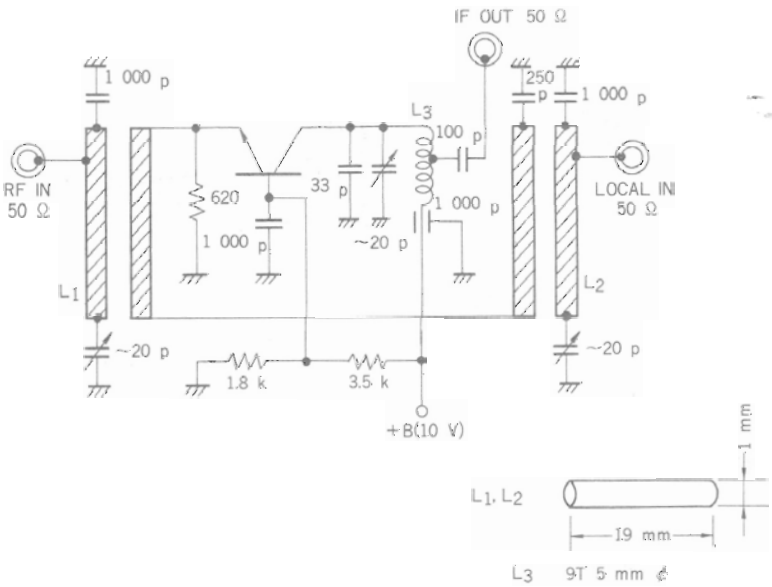
Y_{rb} vs. f



CONVERSION GAIN vs. LOCAL OSCILLATOR LEVEL



900 MHz G_{cb} Test Circuit



L_3 9T 5 mm ϕ

NEC
ELECTRON DEVICE

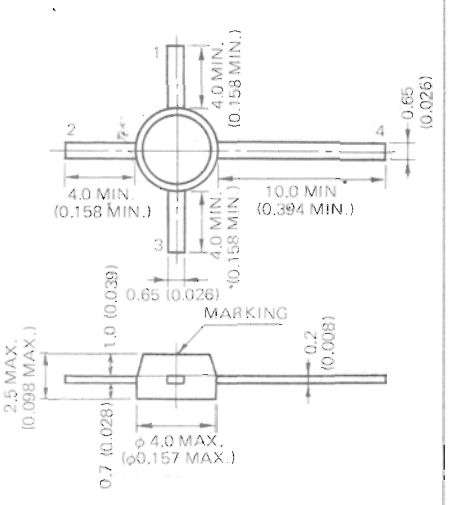
NPN SILICON TRANSISTOR
2SC2368

DESCRIPTION 2SC2368 is designed for High frequency Low Noise Amplifier.

FEATURES

- NF 2.3 dB TYP. @ 500 MHz
- MAG 17 dB TYP. @ 500 MHz

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta=25 °C)

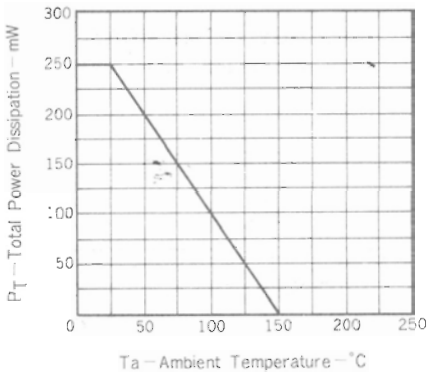
V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage . . .	14	V
V_{EBO}	Emitter to Base Voltage	3.0	V
I_C	Collector Current	50	mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

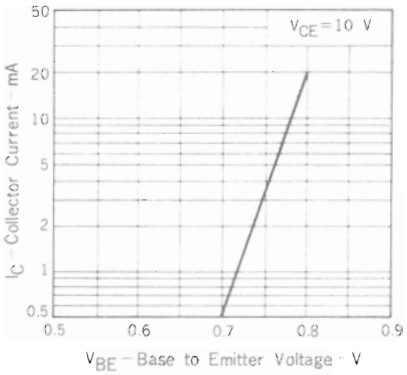
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40		200		V_{CE}=10 V, I_C=10 mA
f_T	Gain Bandwidth Product		2.8		GHz	V_{CE}=10 V, I_E=10 mA
C_{ob}	Output Capacitance		0.7	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$\|S_{21e}\|^2$	Insertion Power Gain	13	14.5		dB	V_{CE}=10 V, I_C=10 mA, f=500 MHz
NF	Noise Figure		2.3	3.5	dB	V_{CE}=10 V, I_C=3 mA, f=500 MHz
MAG	Maximum Available Gain		17		dB	V_{CE}=10 V, I_C=10 mA, f=500 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB}=2.0 V, I_C=0

TYPICAL CHARACTERISTICS (Ta=25 °C)

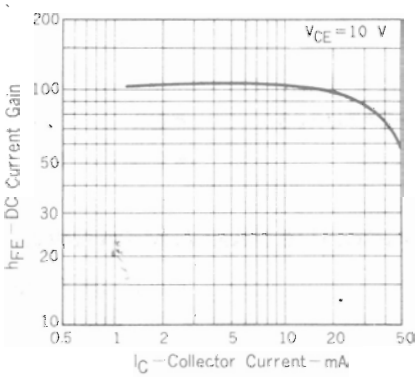
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



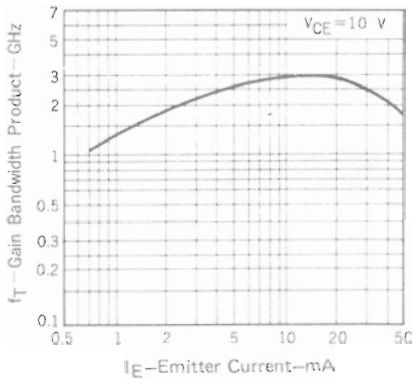
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



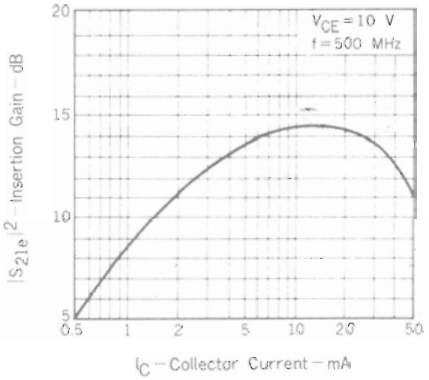
DC CURRENT GAIN vs. COLLECTOR CURRENT



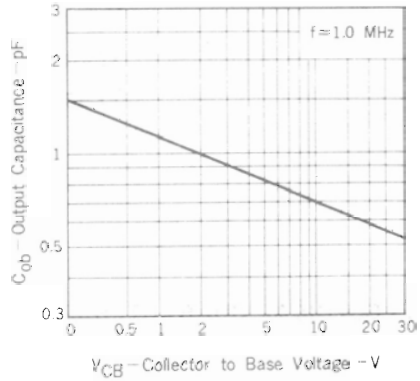
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



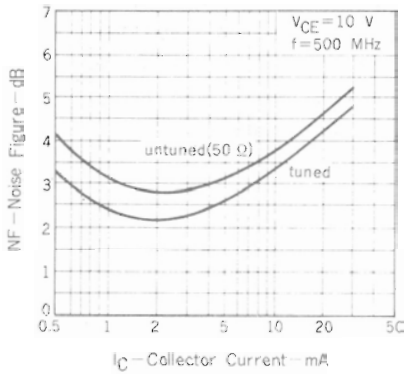
INSERTION GAIN vs. COLLECTOR CURRENT



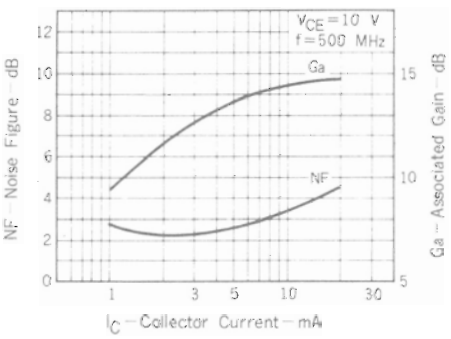
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NOISE FIGURE vs. COLLECTOR CURRENT



NF, Ga vs. COLLECTOR CURRENT



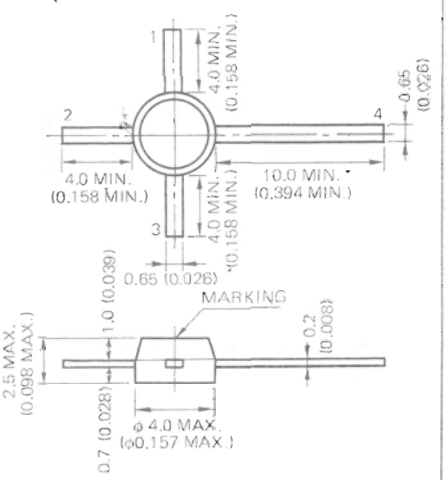
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC2369

DESCRIPTION 2SC2369 is designed for High frequency Low Noise Amplifier.

FEATURES
- NF 1.5 dB TYP. @ f=1.0 GHz
- MAG 14 dB TYP. @ f=1.0 GHz

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (Ta=25 °C)

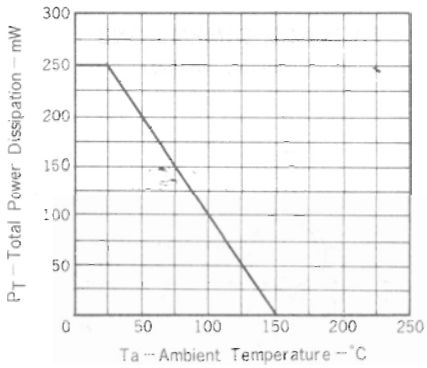
V_{CBO}	Collector to Base Voltage	25	V
V_{CEO}	Collector to Emitter Voltage	12	V
V_{EBO}	Emitter to Base Voltage	3.0	V
I_C	Collector Current	70	mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

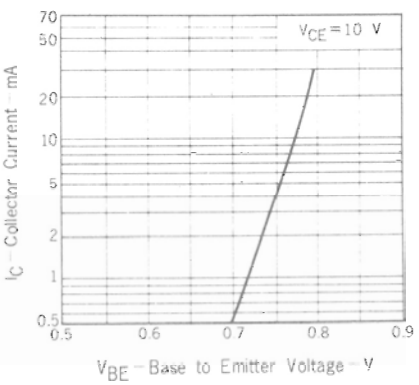
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40		200		V_{CE}=10 V, I_C=20 mA
f_T	Gain Bandwidth Product		4.5		GHz	V_{CE}=10 V, I_E=20 mA
C_{ob}	Output Capacitance		0.75	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$\|S_{21e}\|^2$	Insertion Power Gain	9	11		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
NF	Noise Figure		1.5	3.0	dB	V_{CE}=10 V, I_C=5 mA, f=1.0 GHz
MAG	Maximum Available Gain		14		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB}=2.0 V, I_C=0

TYPICAL CHARACTERISTICS (Ta=25 °C)

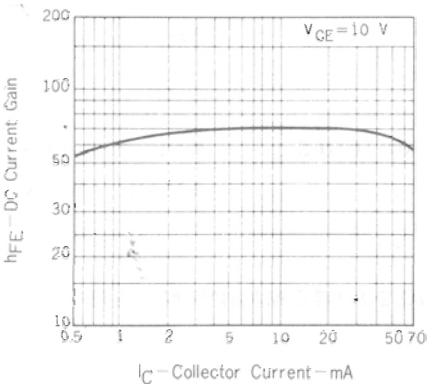
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



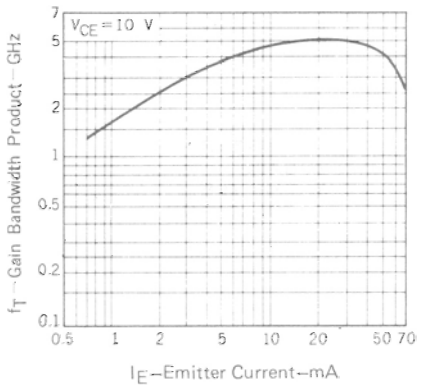
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



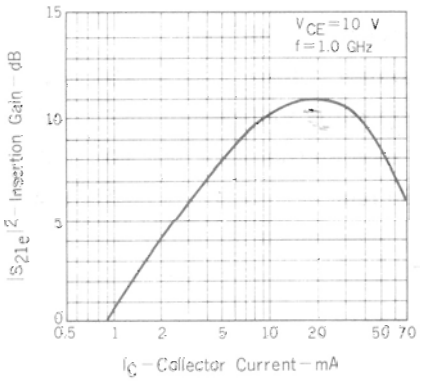
DC CURRENT GAIN vs. COLLECTOR CURRENT



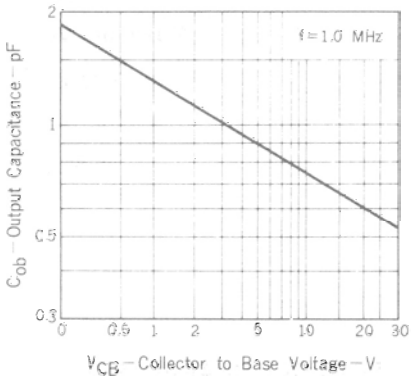
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



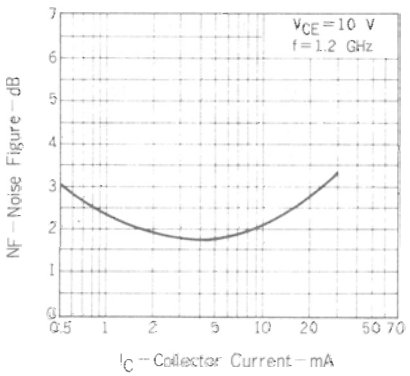
INSERTION GAIN vs. COLLECTOR CURRENT



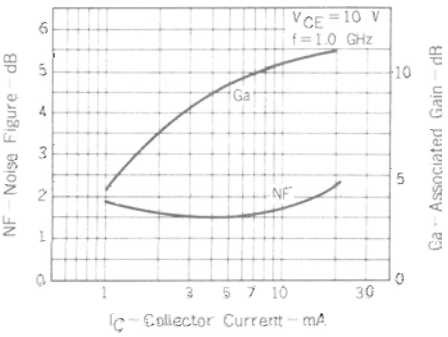
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NOISE FIGURE vs. COLLECTOR CURRENT



NF, Ga vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

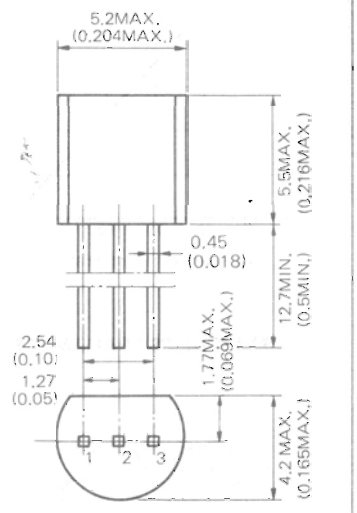
NPN SILICON TRANSISTOR
2SC2407

DESCRIPTION The 2SC2407 is designed for UHF and VHF amplifier.

FEATURES

- P_{out}: 160 mW TYP. @ f=500 MHz, V_{CC}=12.6 V
  P_i=5 mW (Class B)

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Currents (Ta=25 °C)

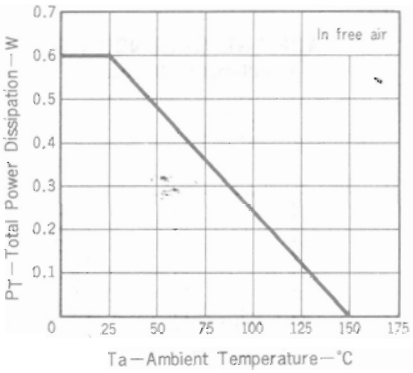
- V_{CBO} Collector to Base Voltage . . . . . 35 V
- V_{CEO} Collector to Emitter Voltage . . . . . 18 V
- V_{EBO} Emitter to Base Voltage . . . . . 3.0 V
- I_C Collector Current . . . . . 150 mA
- I_B Base Current . . . . . 50 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

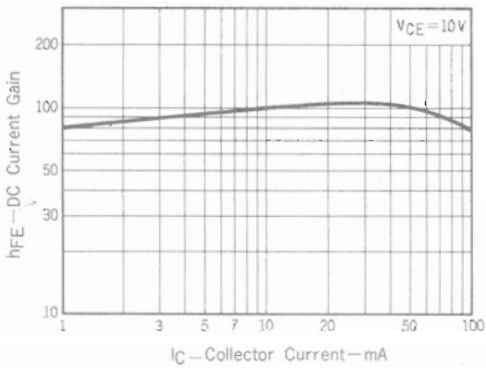
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	20	60	200		V_{CE}=10 V, I_C=50 mA
C_{ob}	Output Capacitance		1.0	2.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
P_{out}	Output Power	20	22		dBm	V_{CC}=12.6 V, P_{in}=7 dBm, f=500 MHz (Class B)
I_{CBO}	Collector Cutoff Current			0.5	μA	V_{CB}=20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.5	μA	V_{EB}=2.0 V, I_C=0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

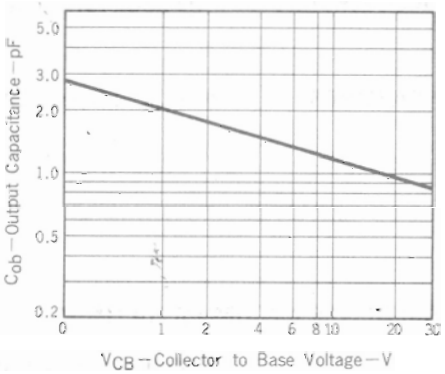
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



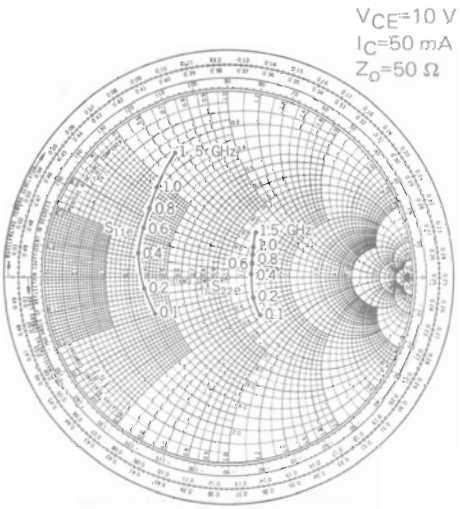
DC CURRENT GAIN vs. COLLECTOR CURRENT



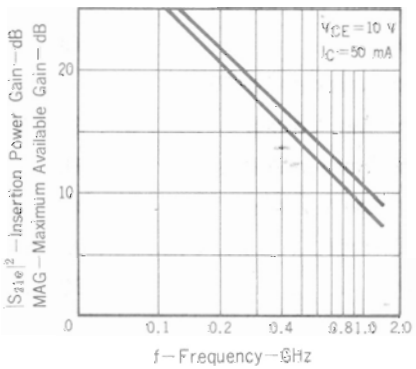
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



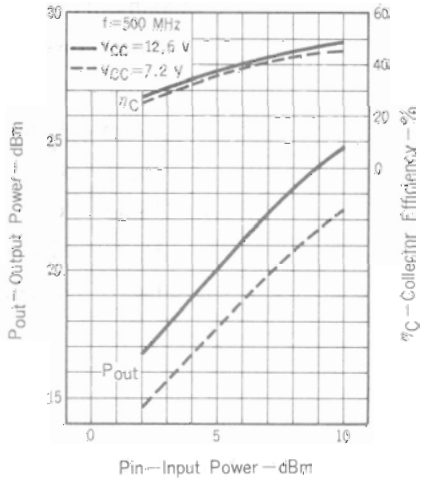
TYPICAL "S" PARAMETERS



INSERTION POWER GAIN AND MAXIMUM AVAILABLE GAIN vs. FREQUENCY



OUTPUT POWER AND COLLECTOR EFFICIENCY vs. INPUT POWER



NEC
ELECTRON DEVICE

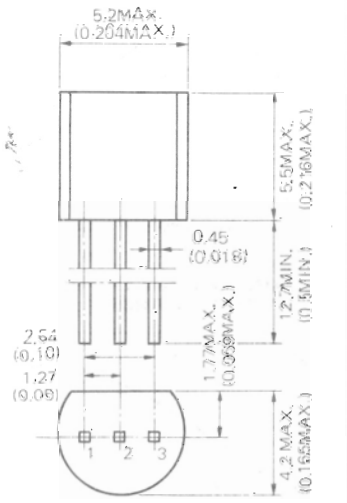
NPN SILICON TRANSISTOR
2SC2408

DESCRIPTION 2SC2408 is designed for High frequency Wide Band Amplifier.

FEATURES

- $|S_{21e}|^2$: 21 dB TYP. @200 MHz
- NF : 2.4 dB TYP. @200 MHz

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Current (Ta=25 °C)

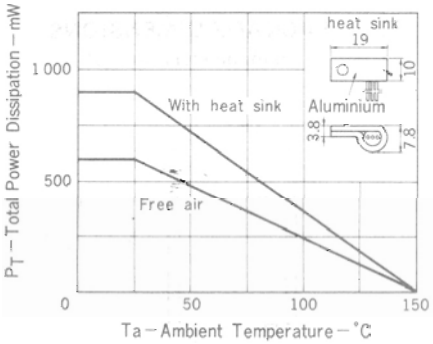
- V_{CBO} Collector to Base Voltage . . . . . 35 V
- V_{CEO} Collector to Emitter Voltage . . . . . 18 V
- V_{EBO} Emitter to Base Voltage . . . . . 3.0 V
- I_C Collector Current . . . . . 150 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

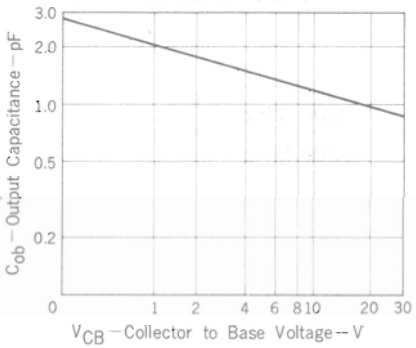
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	30	100	200		V_{CE}=10 V, I_C=50 mA
f_T	Gain Bandwidth Product		3.5		GHz	V_{CE}=10 V, I_E=50 mA
C_{ob}	Output Capacitance		1.25	2.0	pF	V_{CB}=10 V, I_E=0, f=200 MHz
$\|S_{21e}\|^2$	Insertion Power Gain	18	21		dB	V_{CE}=10 V, I_C=50 mA, f=200 MHz, R_G=50 Ω
NF	Noise Figure		2.4	4.0	dB	V_{CE}=10 V, I_C=30 mA, f=200 MHz, R_G=50 Ω
I_{CBO}	Collector Cutoff Current			0.5	μA	V_{CB}=20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.5	μA	V_{EB}=2.0 V, I_C=0

TYPICAL CHARACTERISTICS (Ta=25 °C)

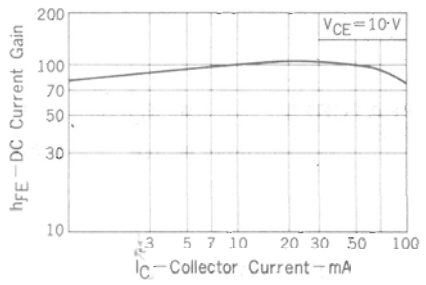
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



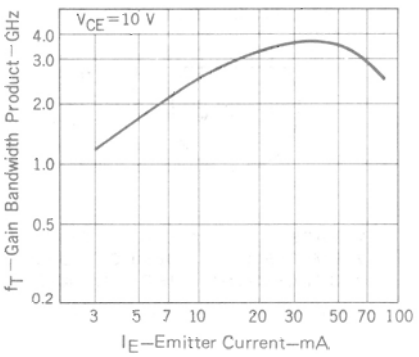
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



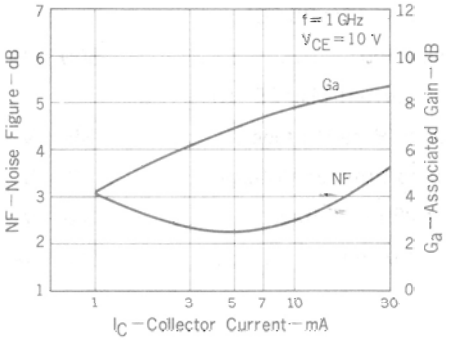
DC CURRENT GAIN vs. COLLECTOR CURRENT



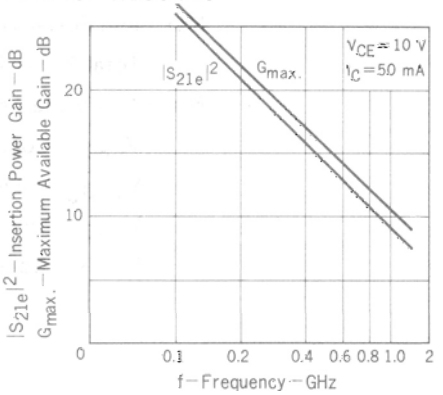
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



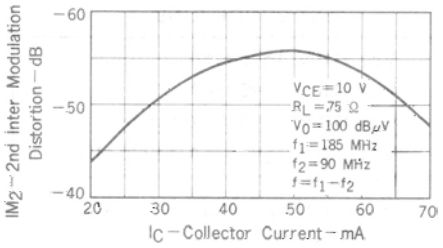
NOISE FIGURE, ASSOCIATED GAIN vs. COLLECTOR CURRENT



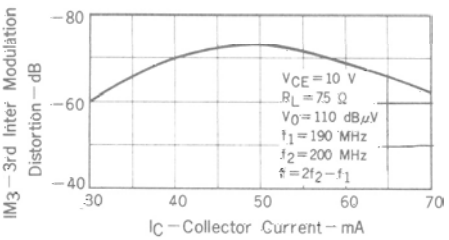
INSERTION GAIN, MAXIMUM AVAILABLE GAIN vs. FREQUENCY



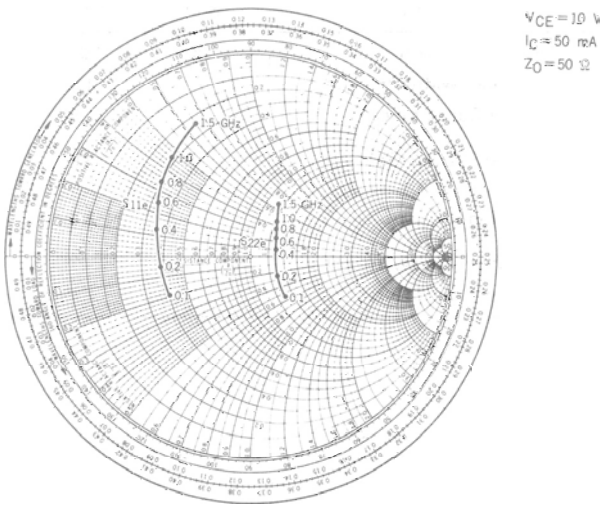
INTER MODULATION DISTORTION vs. COLLECTOR CURRENT



INTER MODULATION DISTORTION vs. COLLECTOR CURRENT



TYPICAL "S" PARAMETER



NEC
ELECTRON DEVICE

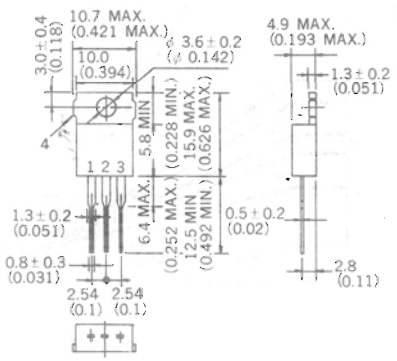
NPN SILICON POWER TRANSISTOR
2SC2518

DESCRIPTION The 2SC2518 is NPN triple diffused transistor designed for switching regulator, DC-DC converter and ultrasonic appliance applications.

FEATURES

- High speed, high voltage switching.
- Low collector saturation voltage.
- Specified of reverse biased SOA with inductive loads.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 40 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500 V
V_{CEO}	Collector to Emitter Voltage	400 V
V_{EBO}	Emitter to Base Voltage	8.0 V
$I_{C(DC)}$	Collector Current (DC)	5.0 A
$I_{C(pulse)}$	Collector Current (pulse)*	10 A
$I_{B(DC)}$	Base Current (DC)	2.5 A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			1.0	μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.4 A
t_{stg}	Storage Time			2.5	μs	R_L = 75 Ω, V_{CC} ≒ 150 V
t_f	Fall Time			0.7	μs	See Test Circuit.
h_{FE1}	DC Current Gain**	20		80	—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE2}	DC Current Gain**	10			—	V_{CE} = 5.0 V, I_C = 2.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			1.0	V	I_C = 2.0 A, I_B = 0.4 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.5	V	I_C = 2.0 A, I_B = 0.4 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 2.0 A, I_B = 0.4 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.4 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 4.0 A, I_{B1} = 0.8 A, −I_{B2} = 0.4 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

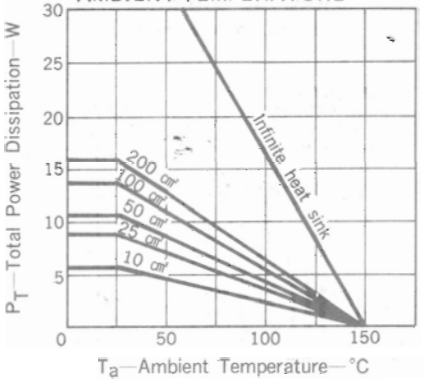
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

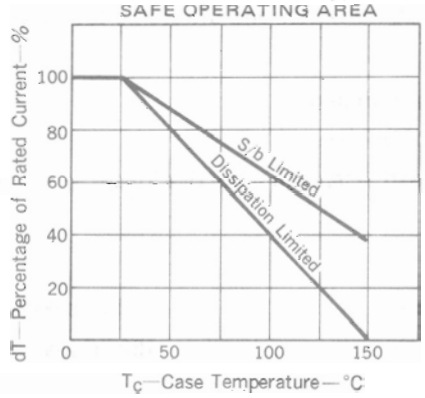
Test Conditions : V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

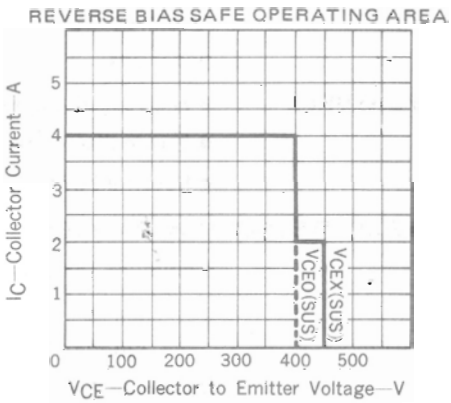
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



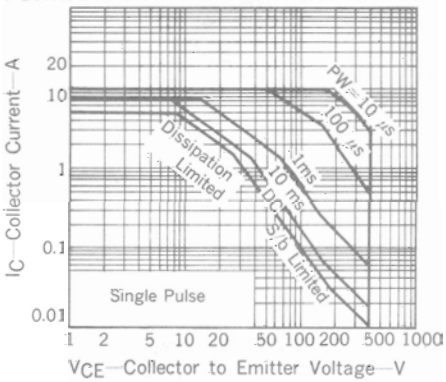
DERATING CURVE OF SAFE OPERATING AREA



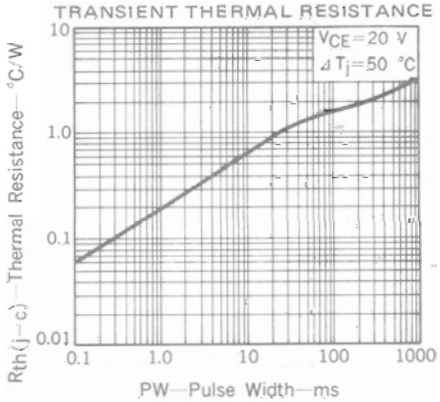
REVERSE BIAS SAFE OPERATING AREA



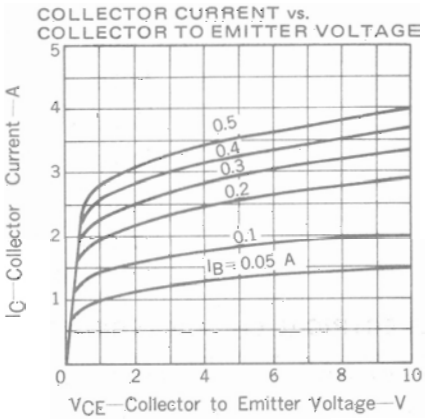
FORWARD BIAS SAFE OPERATING AREA



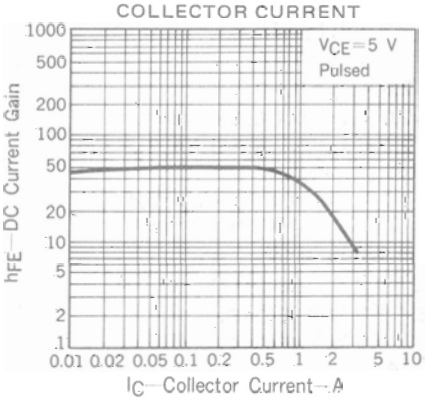
TRANSIENT THERMAL RESISTANCE



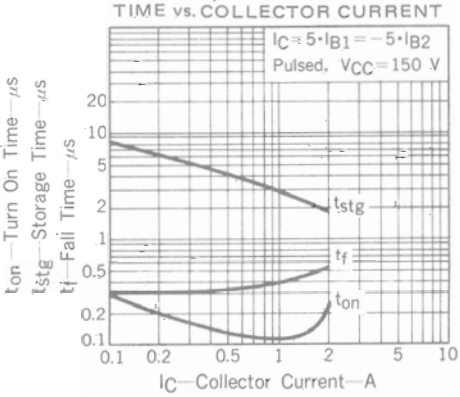
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



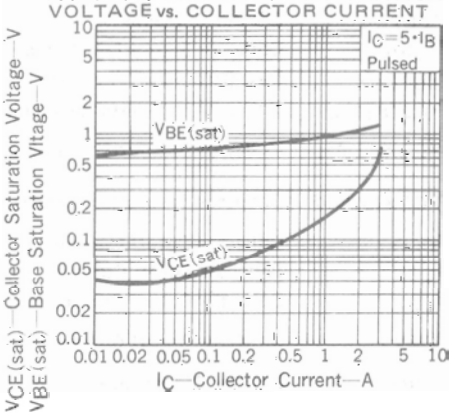
DC CURRENT GAIN vs. COLLECTOR CURRENT



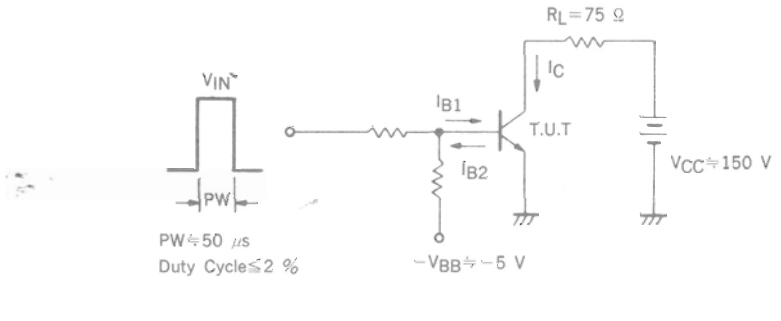
TURN ON, STORAGE AND FALL TIME vs. COLLECTOR CURRENT

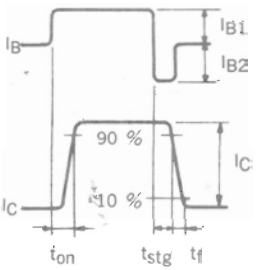


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

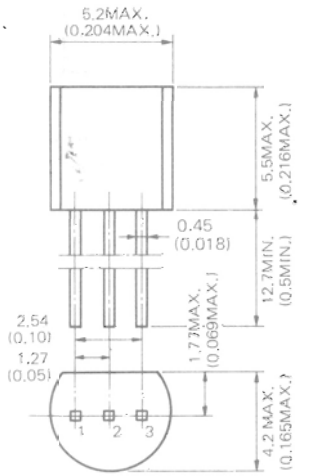
NPN SILICON TRANSISTOR
2SC2570A

DESCRIPTION The 2SC2570A is designed for use in Low Noise Amplifier of VHF & UHF stages.

FEATURES

- Low Noise and High Gain.
  NF=1.5 dB TYP.
  Ga= 8 dB TYP. @ V_{CE}=10 V, I_C=5.0 mA, f=1.0 GHz
- Wide Dynamic Range.
  NF=1.9 dB
  Ga= 9 dB @ f=1 GHz, V_{CE}=10 V, I_C=15 mA

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)
- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Current (Ta=25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 25 V
- V_{CEO} Collector to Emitter Voltage . . . . . 12 V
- V_{EBO} Emitter to Base Voltage . . . . . 3.0 V
- I_C Collector Current . . . . . 70 mA

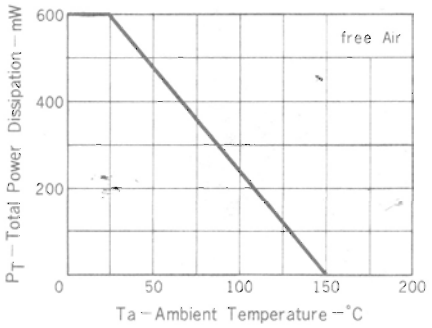
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40		200		V_{CE}=10 V, I_C=20 mA
f_T	Gain Bandwidth Product		5.0		GHz	V_{CE}=10 V, I_E=20 mA
C_{ob}*	Output Capacitance		0.7	0.9	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$\|S_{21e}\|^2$	Insertion Power Gain	8	10		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
NF	Noise Figure		1.5	3.0	dB	V_{CE}=10 V, I_C=5 mA, f=1.0 GHz
MAG	Maximum Available Gain		11.5		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=15 V, I_E=0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB}=2.0 V, I_C=0

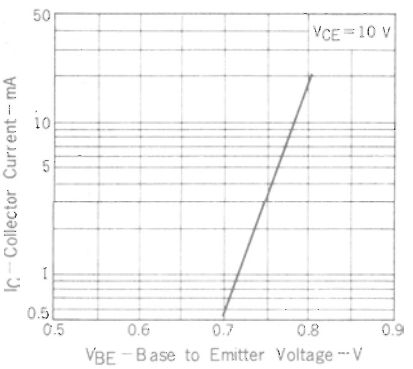
* The emitter and case terminal should be connected to the guard terminal of the capacitance bridge.

TYPICAL CHARACTERISTICS (Ta=25 °C)

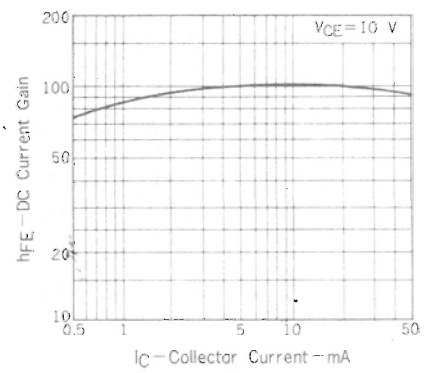
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



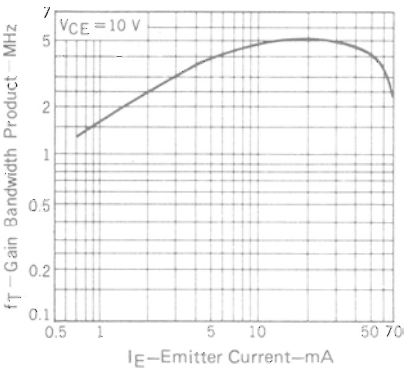
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



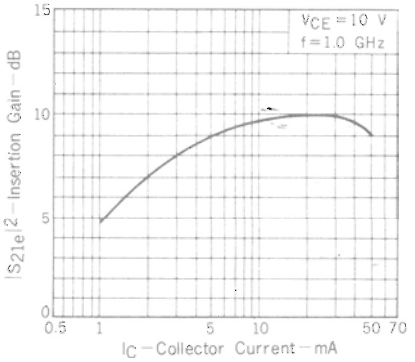
DC CURRENT GAIN vs. COLLECTOR CURRENT



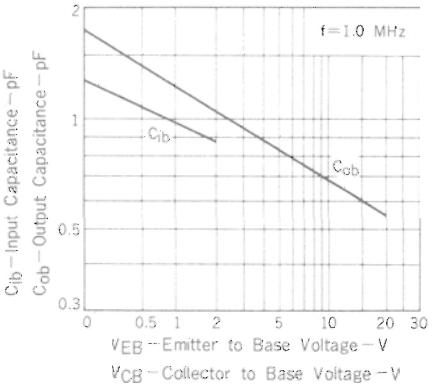
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



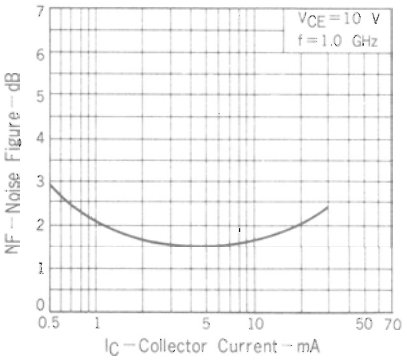
INSERTION GAIN vs. COLLECTOR CURRENT



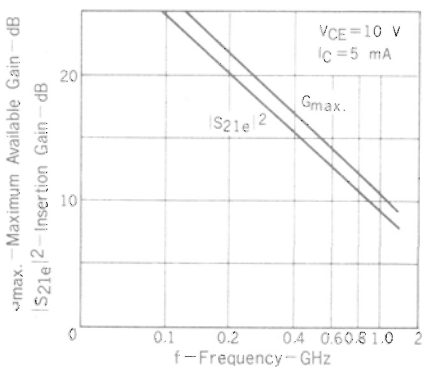
OUTPUT AND INPUT CAPACITANCE vs. REVERSE VOLTAGE



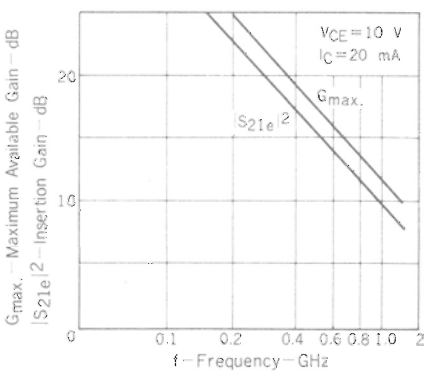
NOISE FIGURE vs. COLLECTOR CURRENT



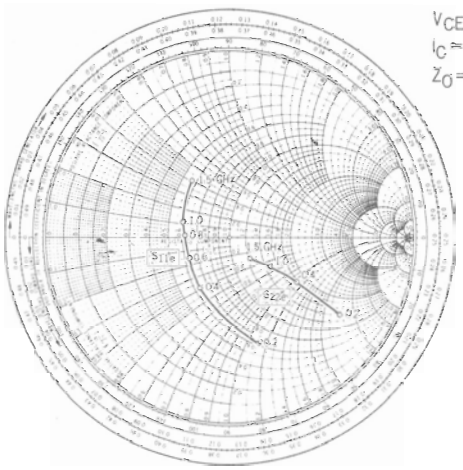
INSERTION GAIN, MAXIMUM AVAILABLE GAIN vs. FREQUENCY

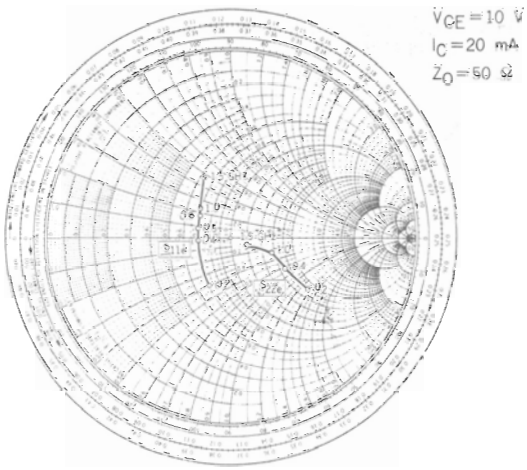


INSERTION GAIN, MAXIMUM AVAILABLE GAIN vs. FREQUENCY



TYPICAL "S" PARAMETERS





NEC
ELECTRON DEVICE

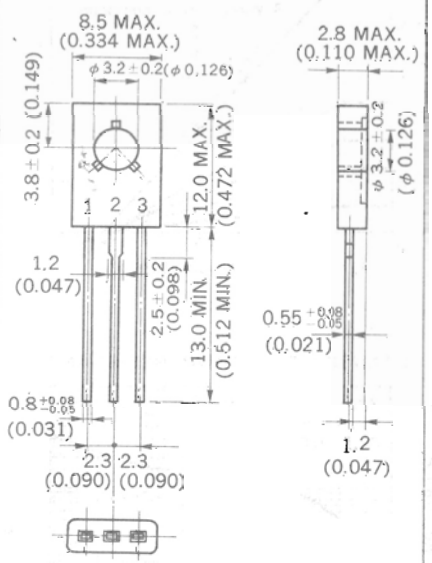
NPN SILICON POWER TRANSISTOR
2SC2682

DESCRIPTION The 2SC2682 is designed for use in Audio frequency power amplifier.

FEATURES

- High voltage. $V_{CEO} > 180$ V
- Low C_{ob}, High f_T
  $f_T = 200$ MHz, $C_{ob} = 3.2$ pF
- Complementary to the NEC 2SA1142 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations
- Total Power Dissipation ($T_a = 25$ °C) . . . . . 1.2 W
- Total Power Dissipation ($T_c = 25$ °C) . . . . . 10 W

Maximum Voltages and Current ($T_a = 25$ °C)
- V_{CBO} Collector to Base Voltage . . . . . 180 V
- V_{CEO} Collector to Emitter Voltage . . . . . 180 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 100 mA

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	190		—	$V_{CE} = 5.0$ V, $I_C = 1.0$ mA*
h_{FE2}	DC Current Gain	100	200	320	—	$V_{CE} = 5.0$ V, $I_C = 10$ mA*
f_T	Gain Bandwidth Product		200		MHz	$V_{CE} = 10$ V, $I_C = 20$ mA
C_{ob}	Output Capacitance		3.2	5.0	pF	$V_{CB} = 10$ V, $I_E = 0$, $f = 1.0$ MHz
NF	Noise Figure		4.0		dB	$V_{CE} = 10$ V, $I_C = 1.0$ mA, $R_G = 10$ kΩ, $f = 1.0$ kHz
I_{CBO}	Collector Cutoff Current			1.0	μA	$V_{CB} = 180$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			1.0	μA	$V_{EB} = 3.0$ V, $I_C = 0$
$V_{CE(sat)}$	Collector Saturation Voltage		0.12	0.5	V	$I_C = 50$ mA, $I_B = 5.0$ mA*
$V_{BE(sat)}$	Base Saturation Voltage		0.8	1.5	V	$I_C = 50$ mA, $I_B = 5.0$ mA*

*Pulse Test : PW ≦ 350 μs, Duty Cycle ≦ 2 %

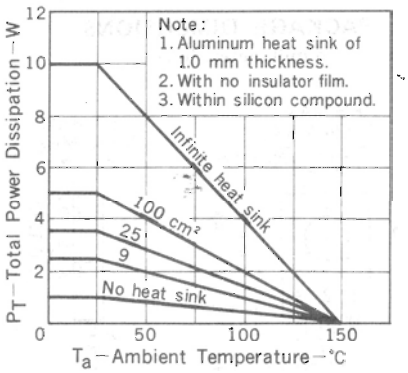
Classification of h_{FE}

Rank	Q	P
Range	100 to 200	160 to 320

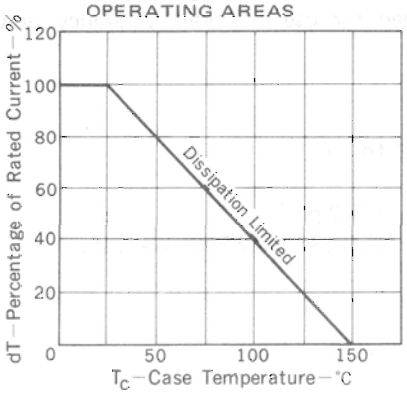
Test Conditions : $V_{CE} = 5.0$ V, $I_C = 10$ mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

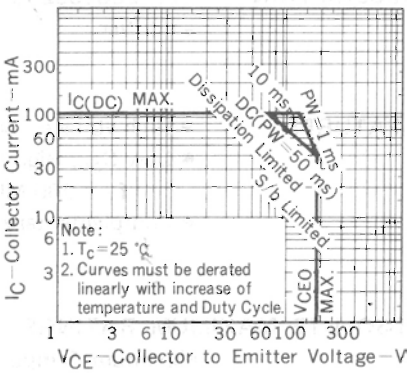
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



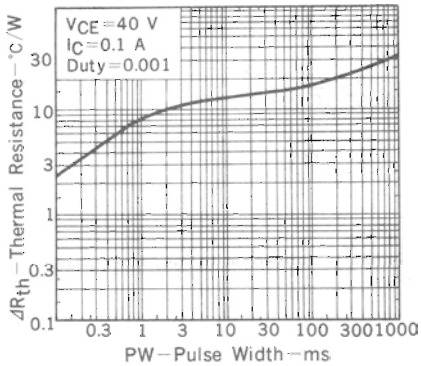
DERATING CURVE OF SAFE OPERATING AREAS



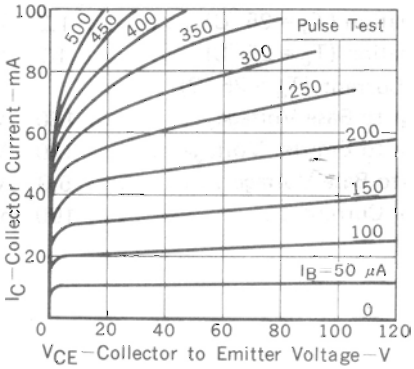
SAFE OPERATING AREAS



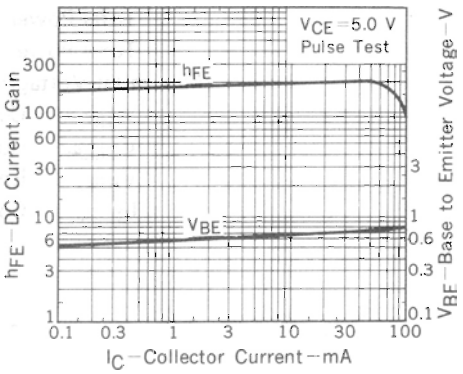
TRANSIENT THERMAL RESISTANCE



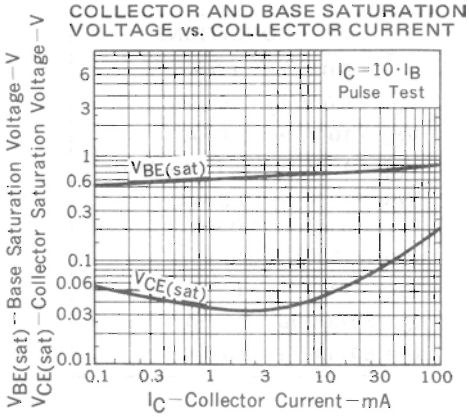
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



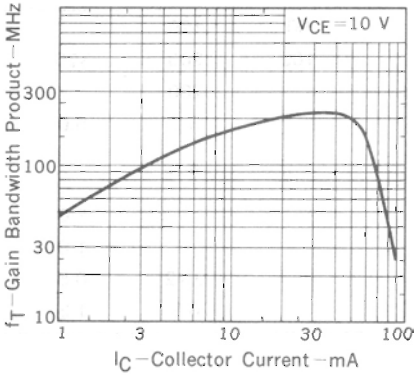
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



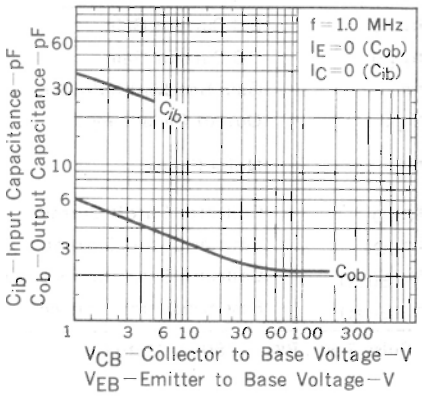
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURREENT



OUTPUT AND INPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

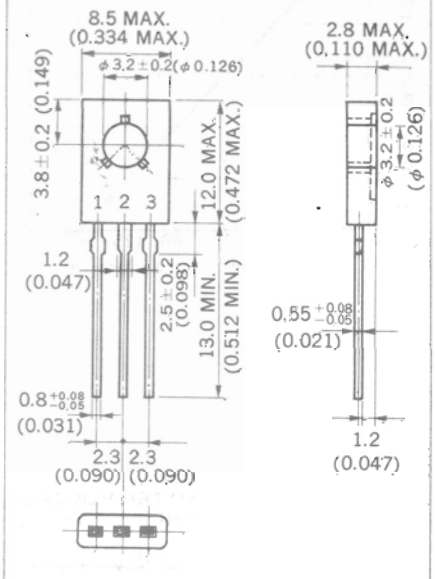
NPN SILICON TRANSISTOR
2SC2688

DESCRIPTION The 2SC2688 is designed for use in Color TV chroma output circuits.

FEATURES

- High Electrostatic-Discharge-Resistance. (E-B reverse bias, C = 2 300 pF) ESDR : TYP. 1 000 V
- Low C_{re}, High f_T
  $C_{re} \leqq 3.0$ pF (V_{CB} = 30 V)
  $f_T \geqq 50$ MHz (V_{CE} = 30 V, I_E = −10 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations
- Total Power Dissipation (T_a = 25 °C) . . . . . 1.25 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 10 W

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	300	V
V_{CEO}	Collector to Emitter Voltage	300	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	80	250		V_{CE} = 10 V, I_C = 10 mA*
f_T	Gain Bandwidth Product	50	80		MHz	V_{CE} = 30 V, I_E = −10 mA
C_{re}	Feedback Capacitance			3.0	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			1.5	V	I_C = 50 mA, I_B = 5.0 mA

*Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

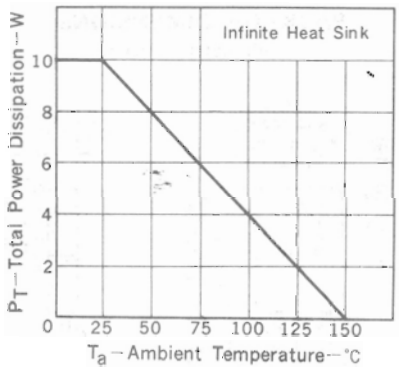
Classification of h_{FE}

Rank	N	M	L	K
Range	40 to 80	60 to 120	100 to 200	160 to 250

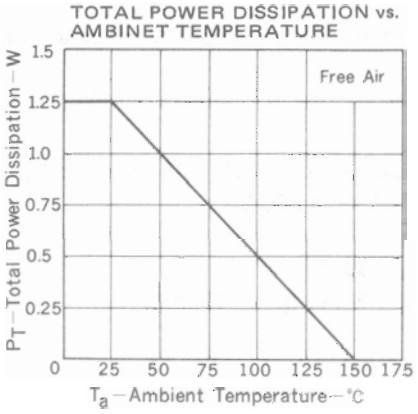
Test Conditions : V_{CE} = 10 V, I_C = 10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

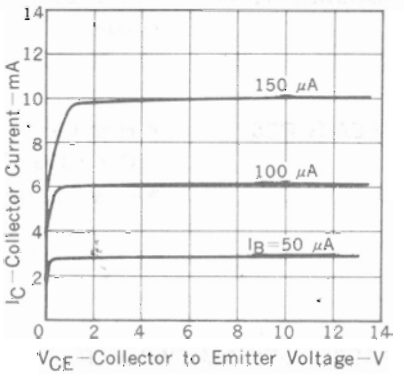
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



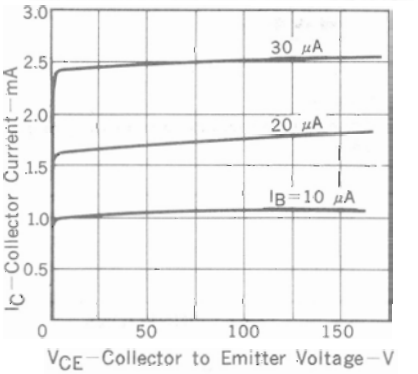
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



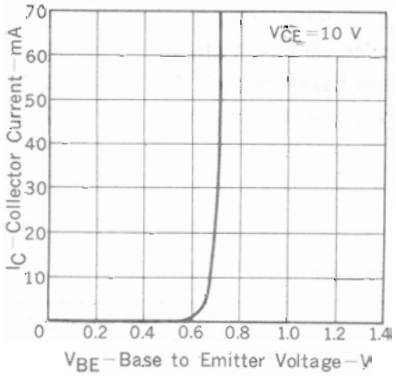
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



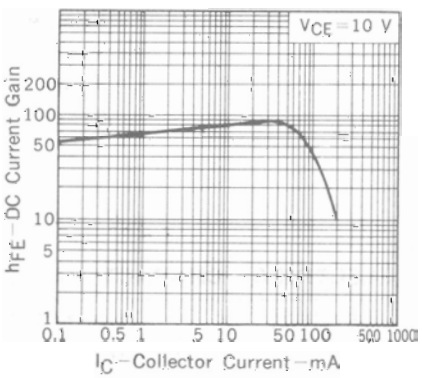
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



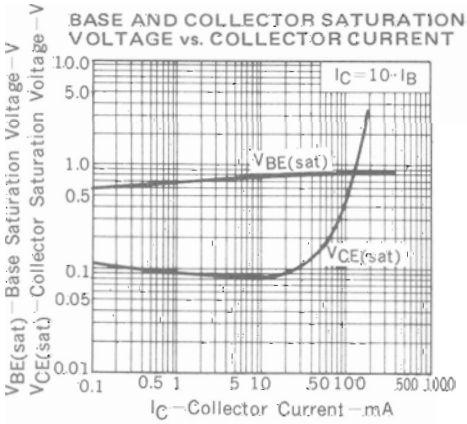
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



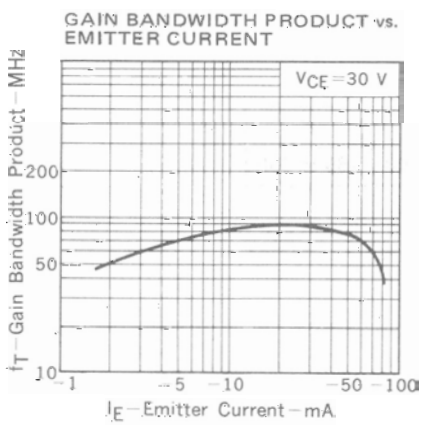
DC CURRENT GAIN vs. COLLECTOR CURRENT



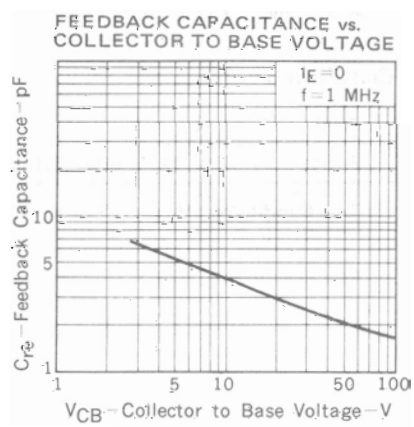
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



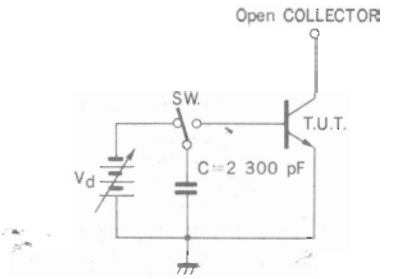
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



FEEDBACK CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



BURNOUT TEST CIRCUIT BY DISCHARGE OF CAPACITOR



TEST CONDITION

1) E-B reverse bias
2) C = 2300 pF
3) Apply one shot pulse to T.U.T. (Transistor Under the Test) by SW.

JUDGEMENT

REJECT; BV_{EBO} waveform defect
As a result if T.U.T. is not rejected, apply higher voltage to capacitor and test again.

NEC
ELECTRON DEVICE

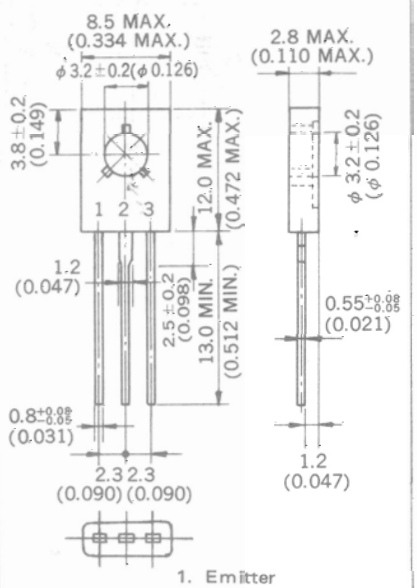
NPN SILICON POWER TRANSISTORS
2SC2690, 2SC2690A

DESCRIPTION The 2SC2690, 2SC2690A are general purpose transistors designed for use in audio and radio frequency power amplifiers.

FEATURES

- Suitable for use in driver stage of 50 to 100 W audio amplifiers and output stage of TV vertical deflection circuit.
- High Voltage and High f_T
  V_{CEO} = 120 V/160 V (2SC2690, 2SC2690A)
  f_T = 175 MHz (@V_{CE} = 5.0 V, I_C = 0.2 A)
- Complementary to the NEC 2SA1220, 2SA1220A PNP Transistors.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.2 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SC2690	2SC2690A	
V_{CBO}	Collector to Base Voltage	120	160	V
V_{CEO}	Collector to Emitter Voltage	120	160	V
V_{EBO}	Emitter to Base Voltage	5.0		V
$I_{C(DC)}$	Collector Current	1.2		A
$I_{C(pulse)}$ *	Collector Current	2.5		A
$I_{B(DC)}$	Base Current	0.3		A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	35	150		—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2} **	DC Current Gain	60	140	320	—	V_{CE} = 5.0 V, I_C = 0.3 A
f_T	Gain Bandwidth Product		175		MHz	V_{CE} = 5.0 V, I_C = 0.2 A
C_{ob}	Output Capacitance		26		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 3.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage		0.4	0.7	V	I_C = 1.0 A, I_B = 0.2 A
$V_{BE(sat)}$ **	Base Saturation Voltage		1.0	1.3	V	I_C = 1.0 A, I_B = 0.2 A

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

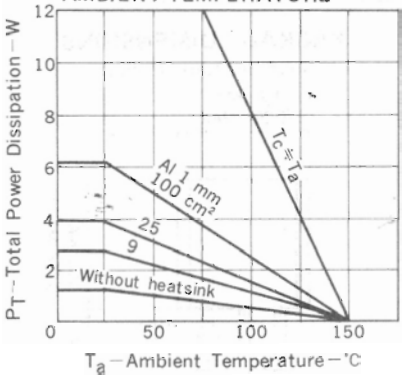
Classification of h_{FE2}

Rank	R	Q	P
Range	60 to 120	100 to 200	160 to 320

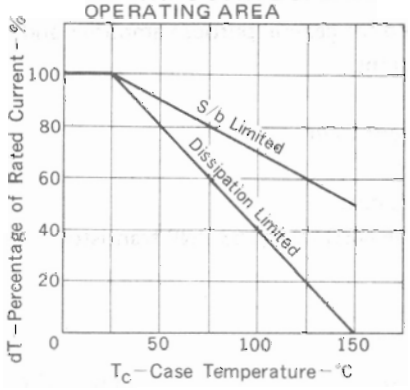
Test Condition: V_{CE} = 5.0 V, I_C = 0.3 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

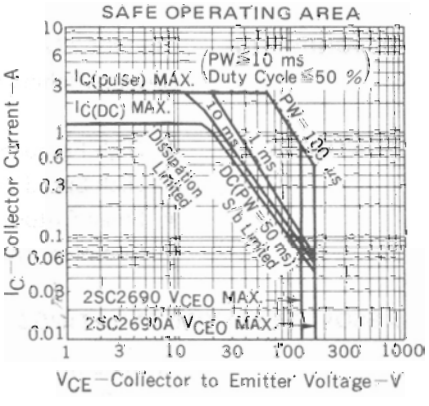
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



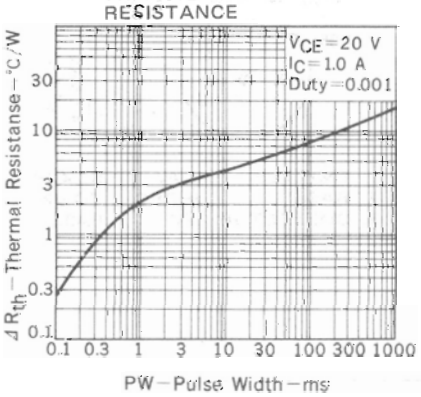
DERATING CURVE OF SAFE OPERATING AREA



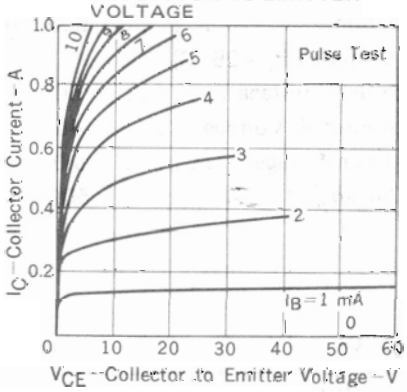
SAFE OPERATING AREA



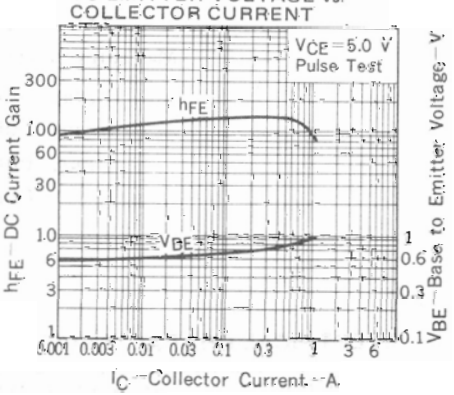
TRANSIENT THERMAL RESISTANCE



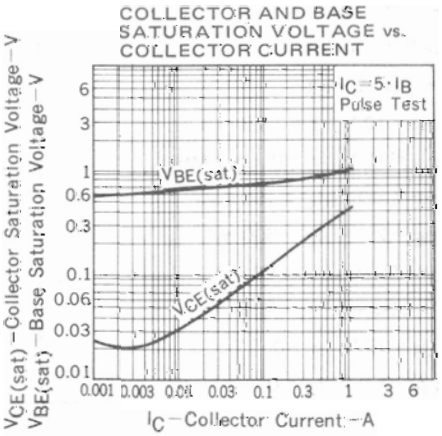
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



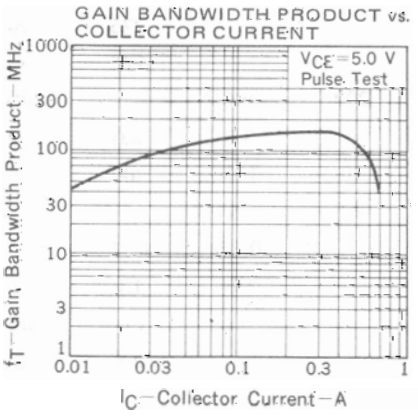
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



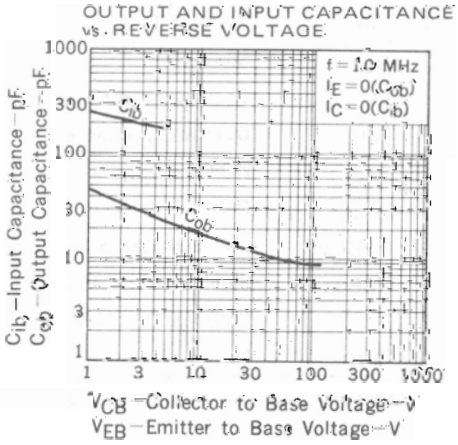
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT AND INPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

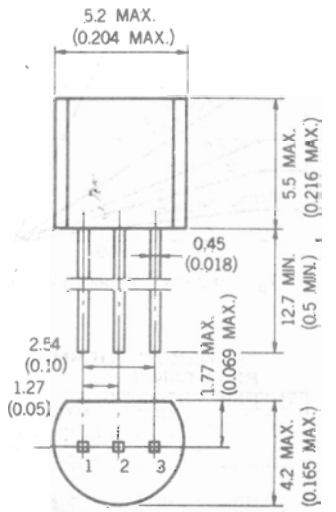
NPN SILICON TRANSISTOR
2SC2720

DESCRIPTION The 2SC2720 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.
- Complementary to the NEC 2SA1153 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Current (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 40 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 500 mA

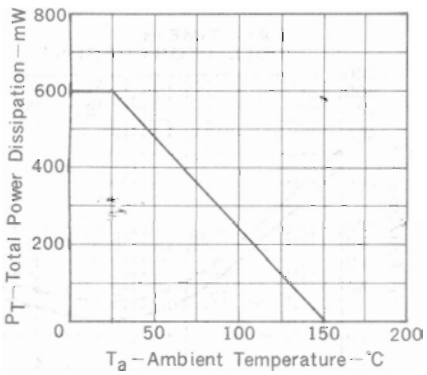
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			35	ns	See Test Circuit
t_{off}	Turn-off Time			275	ns	See Test Circuit
t_{stg}	Storage Time			225	ns	See Test Circuit
f_T	Gain Bandwidth Product	200	400		MHz	V_{CE} = 10 V, I_E = −20 mA
C_{ob}	Output Capacitance		3.5	8.0	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz
h_{FE1}*	DC Current Gain	50	150	300	—	V_{CE} = 1.0 V, I_C = 150 mA
h_{FE2}*	DC Current Gain	20	75		—	V_{CE} = 2.0 V, I_C = 500 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.25	0.75	V	I_C = 500 mA, I_B = 50 mA
$V_{BE(sat)}$*	Base Saturation Voltage		1.0	1.2	V	I_C = 500 mA, I_B = 50 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB} = 4.0 V, I_C = 0

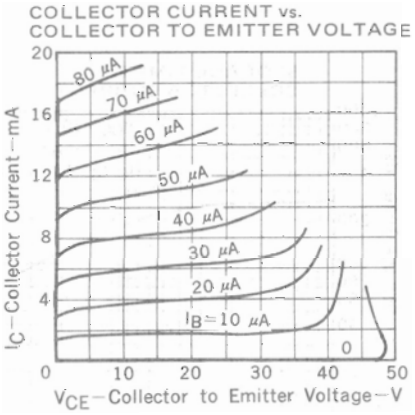
* Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

TYPICAL CHARACTERISTICS (T_a = 25 °C)

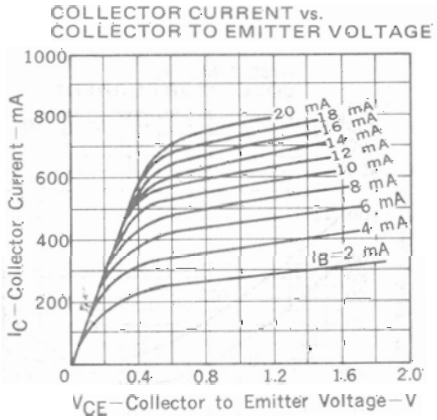
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



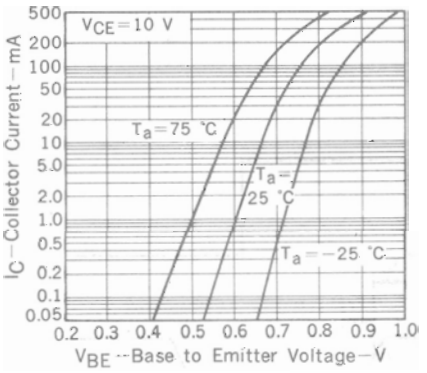
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



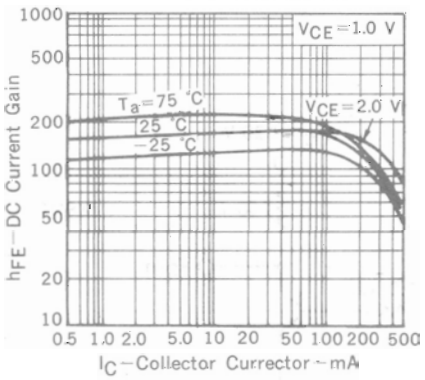
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



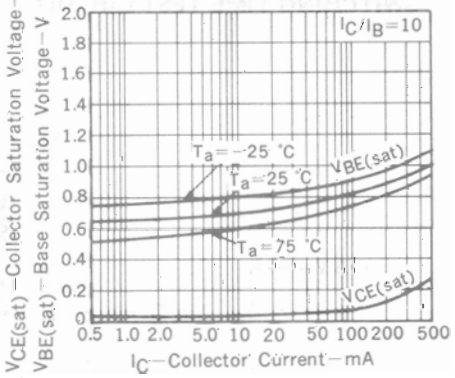
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



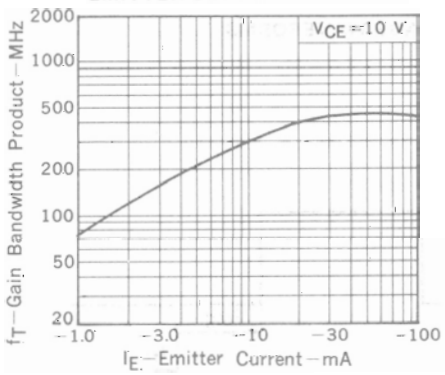
DC CURRENT GAIN vs. COLLECTOR CURRENT



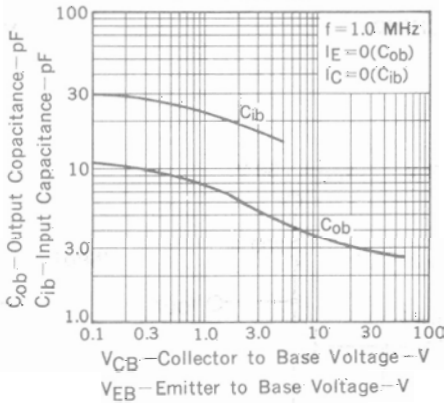
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



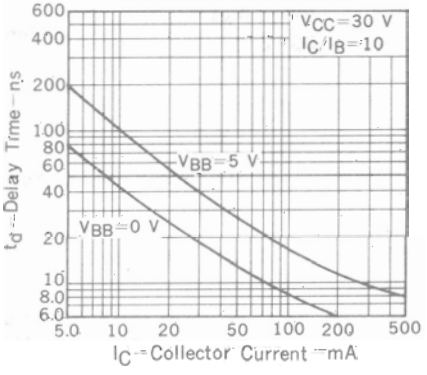
GAIN BANDWITH PRODUCT vs. EMITTER CURRENT



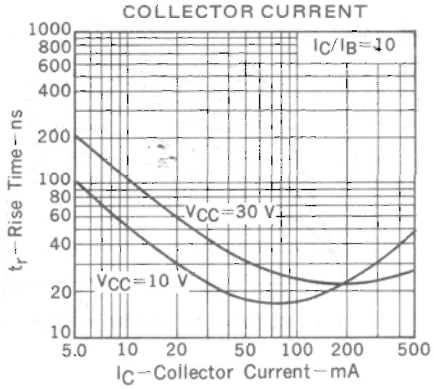
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



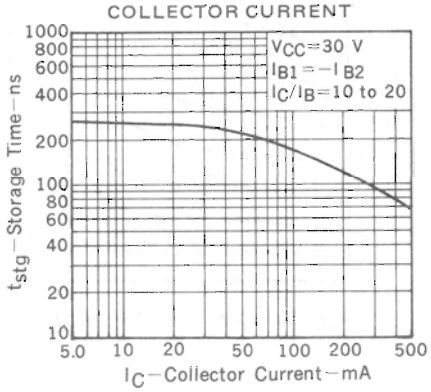
DELAY TIME vs. COLLECTOR CURRENT



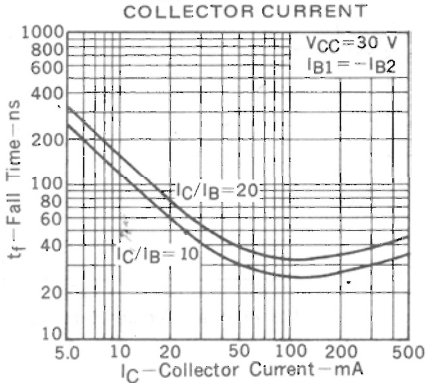
RISE TIME vs. COLLECTOR CURRENT



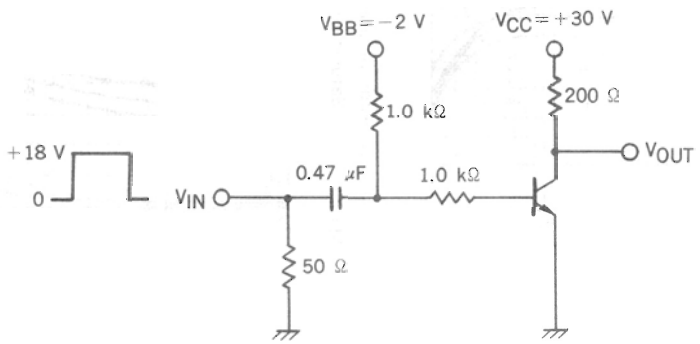
STORAGE TIME vs. COLLECTOR CURRENT



FALL TIME vs. COLLECTOR CURRENT

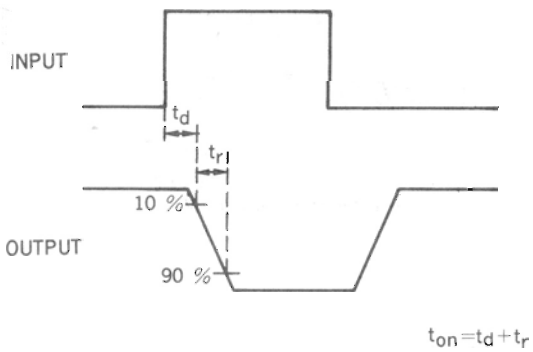


SWITCHING TIME TEST CIRCUIT

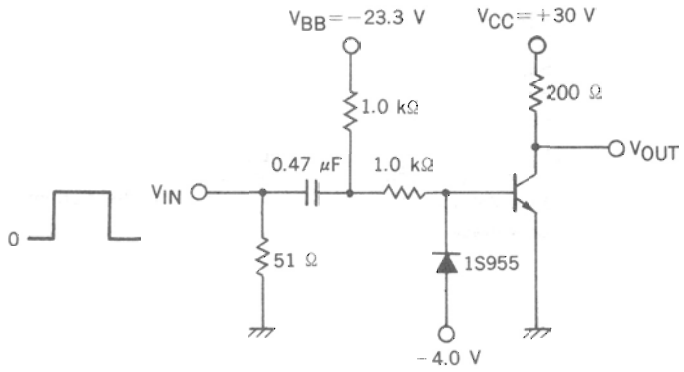


t_r<2.0 ns
PW=1.0 μs
DC=2 %

t_{on} SWITCHING

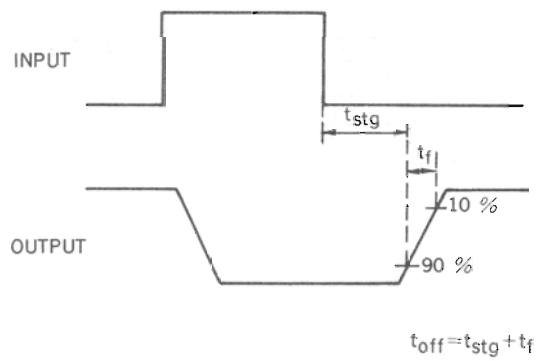


VOLTAGE WAVEFORMS



t_r≤2.0 ns
PW=1.0 μs
DC=2 %

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

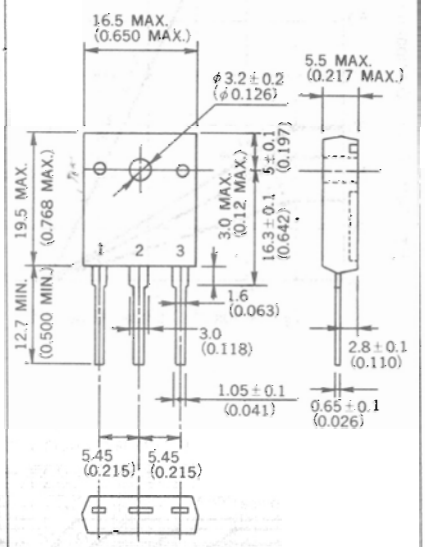
NPN SILICON POWER TRANSISTOR
2SC2749

DESCRIPTION The 2SC2749 is NPN silicon triple diffused transistor designed for switching regulator and ultrasonic appliance applications.

FEATURES

- High speed switching.
- High voltage rating.
- Wide safe operating area.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 100 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 500 V
- V_{CEO} Collector to Emitter Voltage . . . . . 400 V
- V_{EBO} Emitter to Base Voltage . . . . . 7.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 10 A
- $I_{C(pulse)}$ Collector Current (pulse)* . . . . . 20 A
- $I_{B(DC)}$ Base Current (DC) . . . . . 5.0 A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			1.0	μs	I_C = 6.0 A, I_{B1} = −I_{B2} = 1.2 A
t_{stg}	Storage Time			2.5	μs	R_L = 25 Ω, V_{CC} = 150 V
t_f	Fall Time			0.7	μs	See Test Circuit.
h_{FE1}	DC Current Gain**	15	35	80	—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE2}	DC Current Gain**	10			—	V_{CE} = 5.0 V, I_C = 3.0 A
h_{FE3}	DC Current Gain**	7.0			—	V_{CE} = 5.0 V, I_C = 6.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			1.0	V	I_C = 6.0 A, I_B = 1.2 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.5	V	I_C = 6.0 A, I_B = 1.2 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 6.0 A, I_B = 1.2 A, L = 100 μH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 6.0 A, I_{B1} = −I_{B2} = 1.2 A, T_a = 125 °C L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 12 A, I_{B1} = 2.4 A, −I_{B2} = 1.2 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

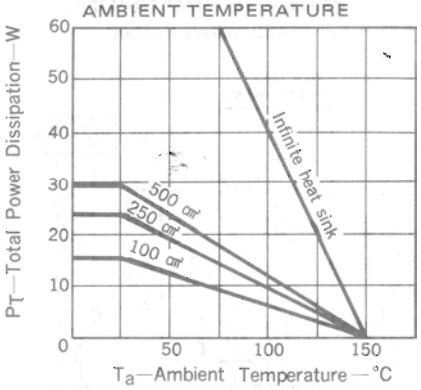
Classification of h_{FE1}

Rank	N	M	L	K
Range	15 to 30	20 to 40	30 to 60	40 to 80

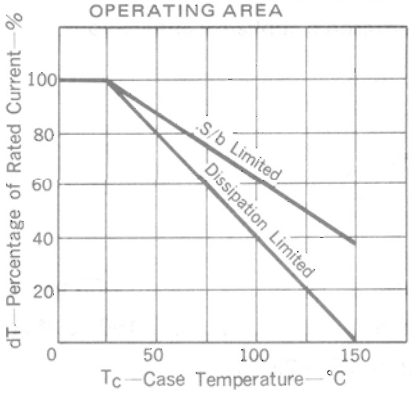
Test Conditions : V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

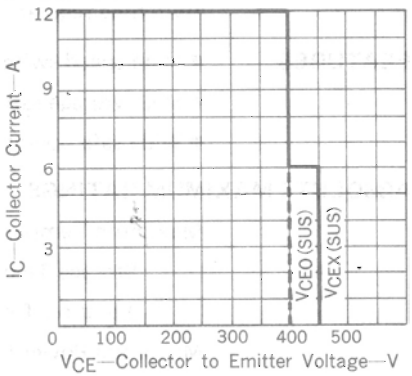
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



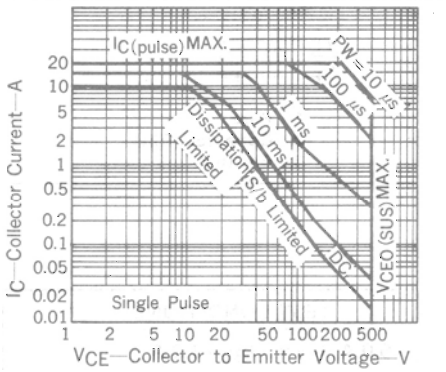
DERATING CURVE OF SAFE OPERATING AREA



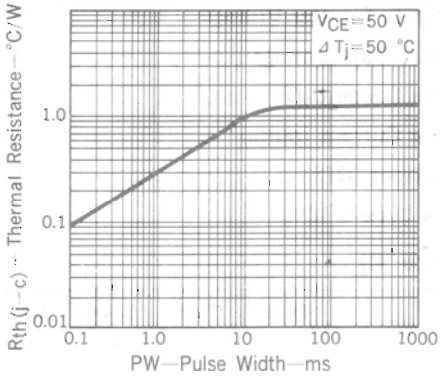
REVERSE BIAS SAFE OPERATING AREA



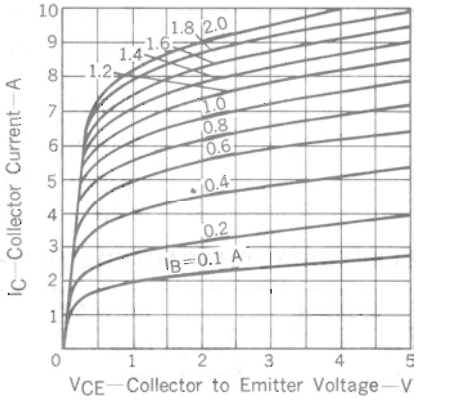
FORWARD BIAS SAFE OPERATING AREA



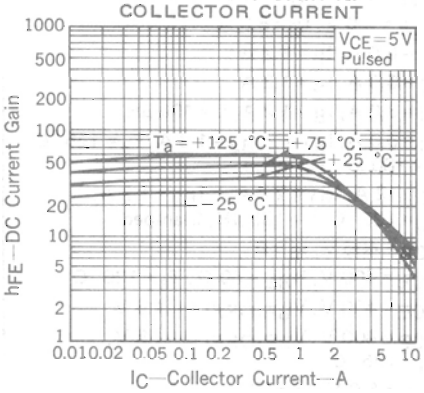
TRANSIENT THERMAL RESISTANCE



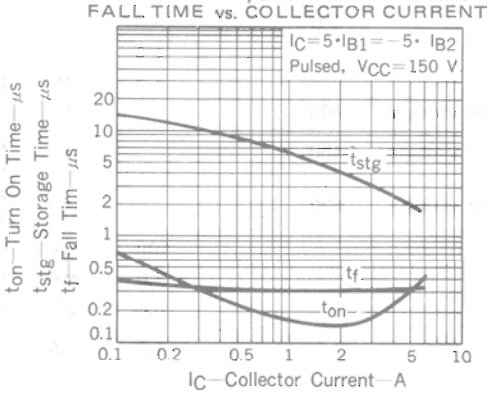
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



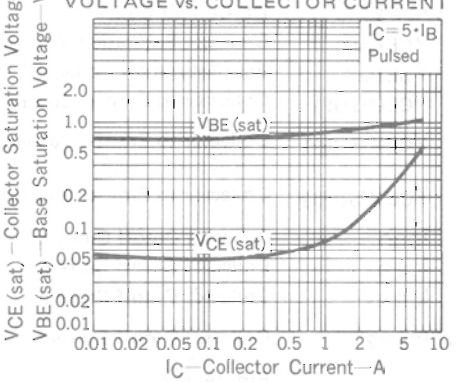
DC CURRENT GAIN vs. COLLECTOR CURRENT



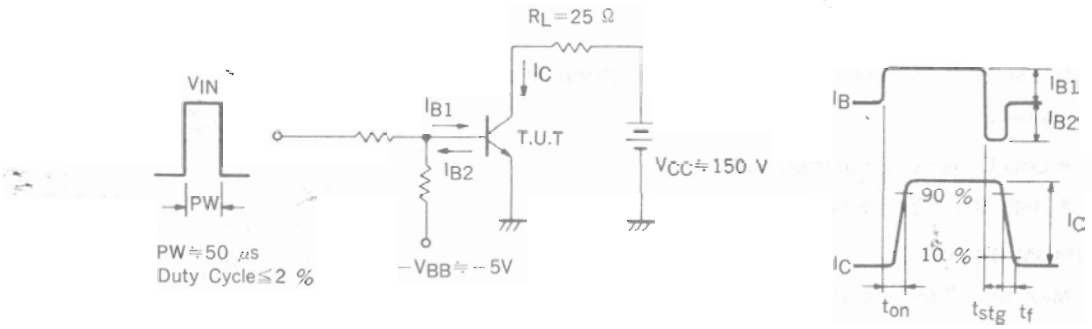
TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



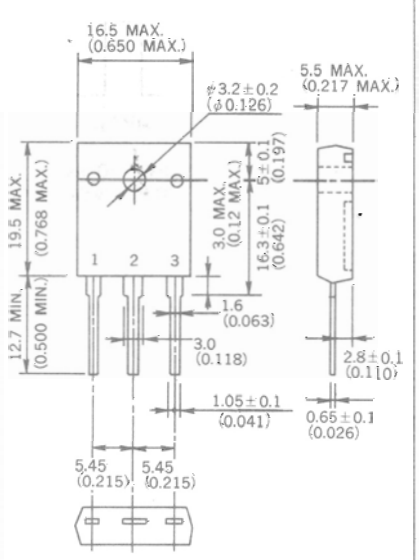
NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC2750

DESCRIPTION The 2SC2750 is designed for use in high speed and high voltage, high current switching.
It is suitable for switching regulators and ultrasonic appliance applications.

FEATURES
- Low Collector Saturation Voltage.
- High Speed Switching.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_c = 25 °C)

Total Power Dissipation	100	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	15	A
$I_{C(pulse)}$	Collector Current (Pulse)*	30	A
$I_{B(DC)}$	Base Current (DC)	5.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			1.0	μs	I_C = 10 A, I_{B1} = −I_{B2} = 1.0 A, R_L = 5 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}	DC Current Gain**	30		120	—	V_{CE} = 5.0 V, I_C = 5.0 A
h_{FE2}	DC Current Gain**	20			—	V_{CE} = 5.0 V, I_C = 10 A
$V_{CE(sat)}$	Collector Saturation Voltage**			0.6	V	I_C = 10 A, I_B = 1.0 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.5	V	I_C = 10 A, I_B = 1.0 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 10 A, I_B = 1.0 A, L = 100 μH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	150			V	I_C = 10 A, I_{B1} = −I_{B2} = 1.0 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 20 A, I_{B1} = 2.0 A, −I_{B2} = 1.0 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 100 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			500	μA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

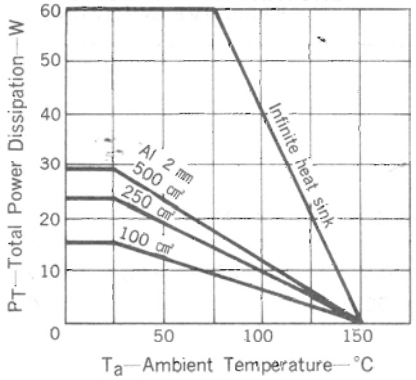
Classification of h_{FE1}

Rank	M	L	K
Range	30 to 60	40 to 80	60 to 120

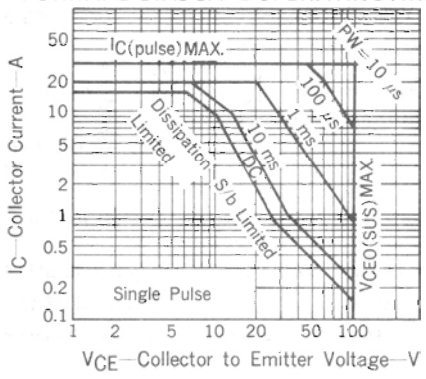
Test Conditions: V_{CE} = 5.0 V, I_C = 5.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

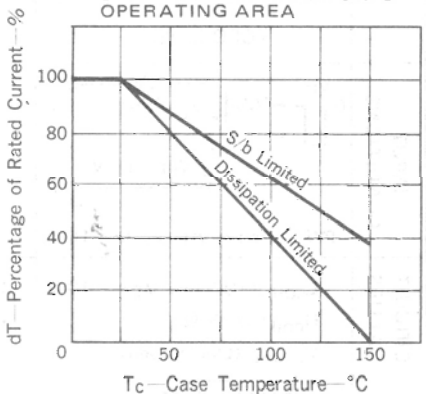
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



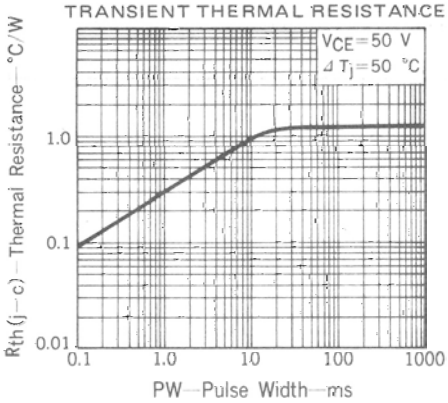
FORWARD BIAS SAFE OPERATING AREA



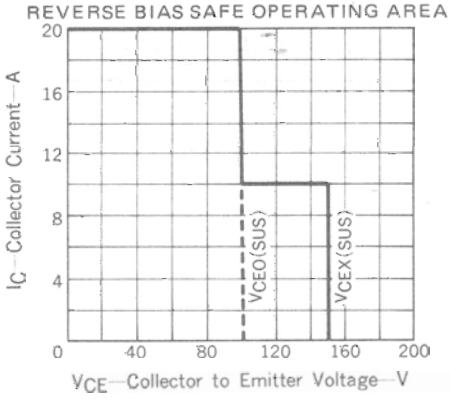
DERATING CURVE OF SAFE OPERATING AREA



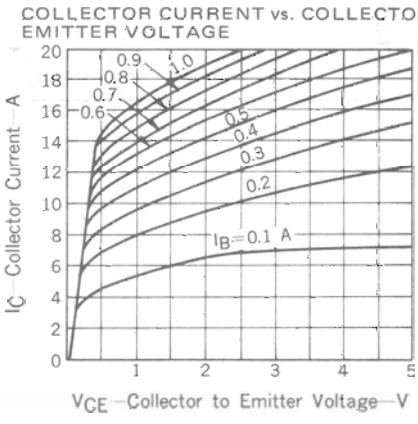
TRANSIENT THERMAL RESISTANCE



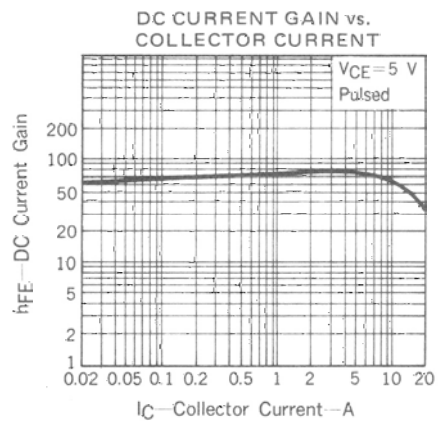
REVERSE BIAS SAFE OPERATING AREA



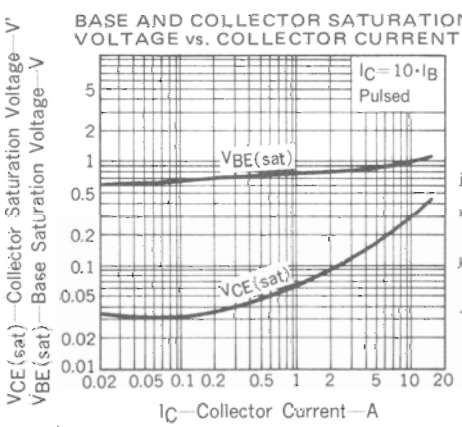
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

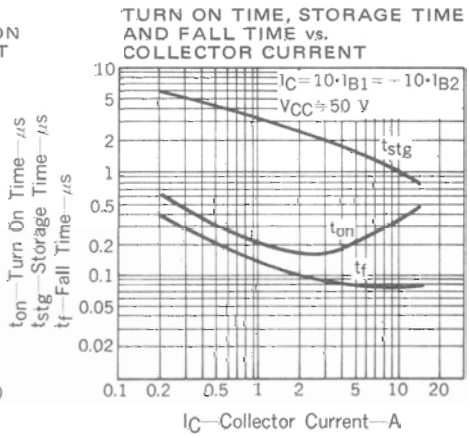
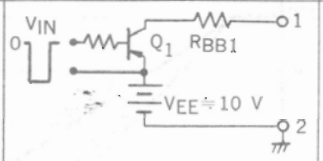
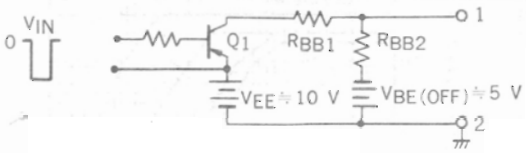
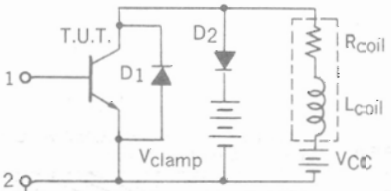
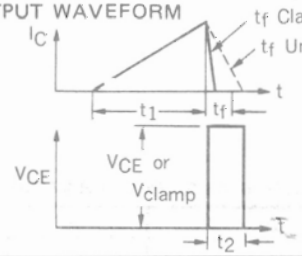
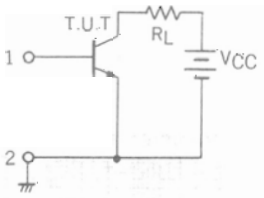


TABLE 1.—TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V_{CEO} (SUS)	V_{CEX} (SUS)	$E_{S/B}$	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 10 A	 PW Varied to Attain I_C = 10 A Duty Cycle ≦ 2 %		Q_1 ≒ 2SA959
CIRCUIT VALUES	L_{coil} = 100 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω V_{clamp} (Unclamped)	L_{coil} = 180 μH, V_{CC} = 20 V R_{coil} = 0.05 Ω V_{clamp} = Rated V_{CEX} Value	L_{coil} = 40 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω, R_{BB2} = 50 Ω V_{clamp} (Unclamped)	R_L = 25 Ω, V_{CC} ≒ 150 V
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  D_1 = F114F D_2 = 6FH4S	OUTPUT WAVEFORM  t_1 Adjust to Obtain I_C $t_1 = \frac{L_{coil}(I_{C\,pk})}{V_{CC}}$ $t_2 = \frac{L_{coil}(I_{C\,pk})}{V_{clamp}}$		RESISTIVE TEST CIRCUIT 

NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC2751

DESCRIPTION The 2SC2751 is designed for use in high speed, high voltage and high current switching.

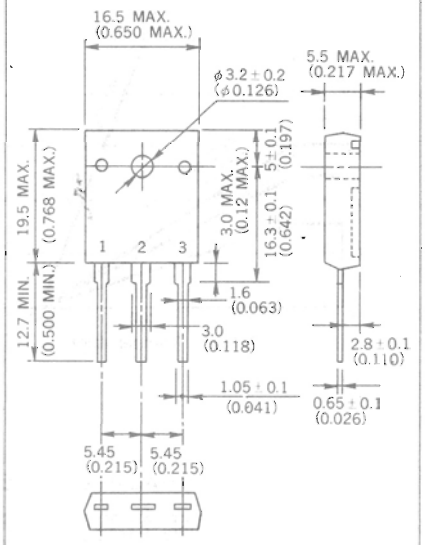
It is suitable for switching regulators, DC-DC converters and ultra-sonic appliance applications.

FEATURES

- High speed switching.
- Wide reverse S.O.A.

  $V_{CEX(SUS)}$ (I_C = 10 A) : 450 V MIN.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	15	A
$I_{C(pulse)}$	Collector Current (Pulse)*	30	A
$I_{B(DC)}$	Base Current (DC)	7.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time		0.3	1.0	μs	I_C = 10 A, I_{B1} = −I_{B2} = 2.0 A, R_L = 15 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time		1.8	2.5	μs	
t_f	Fall Time		0.3	0.7	μs	
h_{FE1}	DC Current Gain**	15	35	80	—	V_{CE} = 5.0 V, I_C = 2.0 A
h_{FE2}	DC Current Gain**	10			—	V_{CE} = 5.0 V, I_C = 5.0 A
h_{FE3}	DC Current Gain**	7			—	V_{CE} = 5.0 V, I_C = 10 A
$V_{CE(sat)}$	Collector Saturation Voltage**		0.3	1.0	V	I_C = 10 A, I_B = 2.0 A
$V_{BE(sat)}$	Base Saturation Voltage**		1.0	1.5	V	I_C = 10 A, I_B = 2.0 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 10 A, I_B = 2.0 A, L = 50 μH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 10 A, I_{B1} = −I_{B2} = 2.0 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 20 A, I_{B1} = 4.0 A, −I_{B2} = 2.0 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

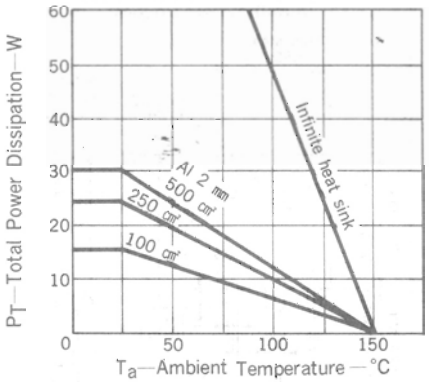
Classification of h_{FE1}

Rank	N	M	L	M
Range	15 to 30	20 to 40	30 to 60	40 to 80

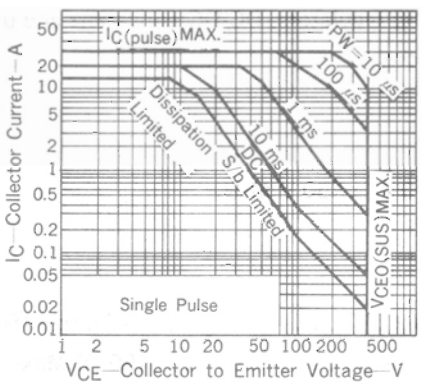
Test Conditions : V_{CE} = 5.0 V, I_C = 2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

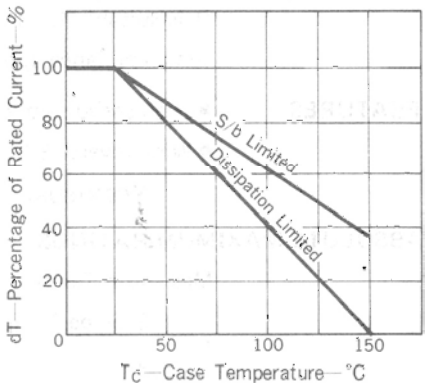
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



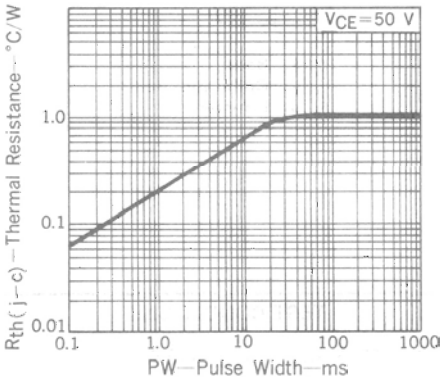
FORWARD BIAS SAFE OPERATING AREA



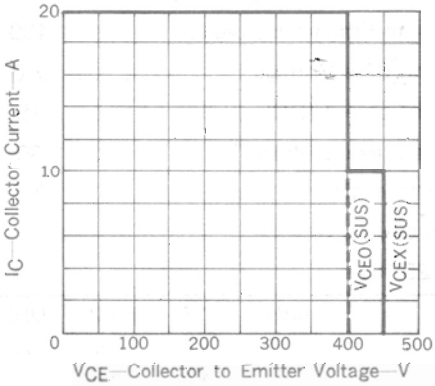
DERATING CURVE OF SAFE OPERATING AREA



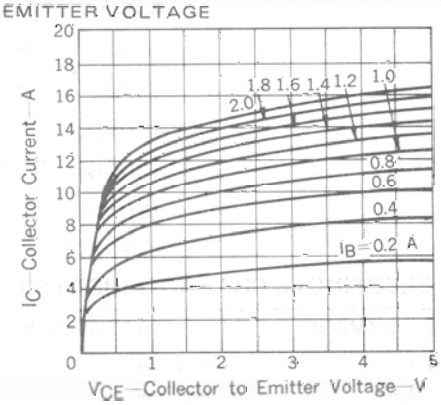
TRANSIENT THERMAL RESISTANCE



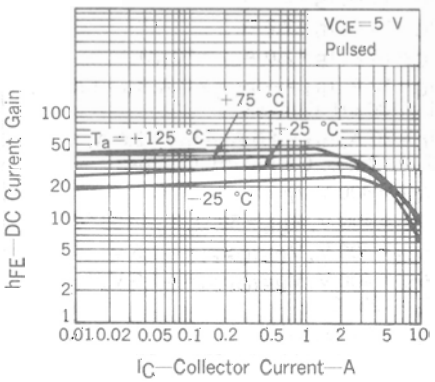
REVERSE BIAS SAFE OPERATING AREA



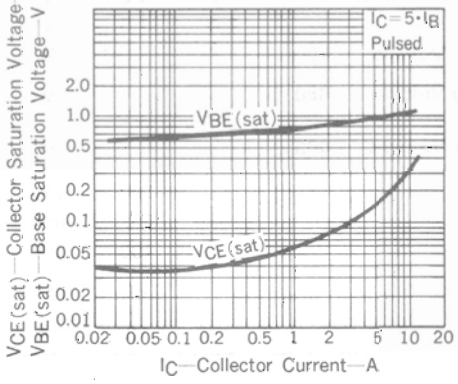
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

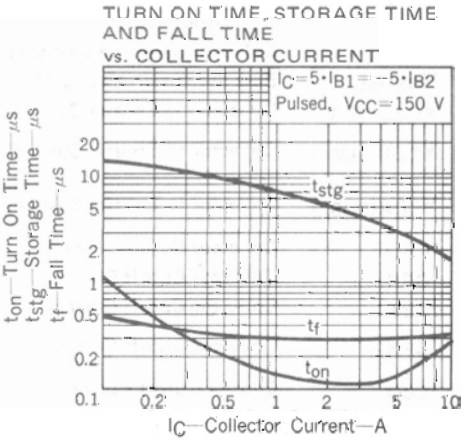
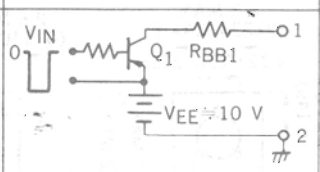
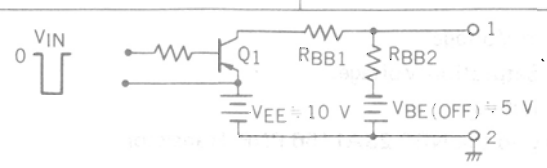
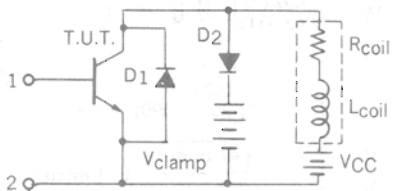
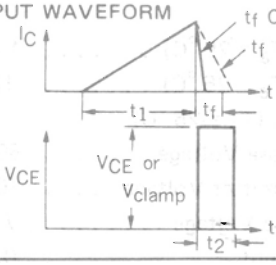
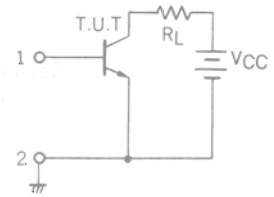


TABLE 1.—TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(SUS)}$	$V_{CEX(SUS)}$	$E_{S/B}$	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 10 A	 PW Varied to Attain I_C = 10 A Duty Cycle ≦ 2 % ※ Q_1 = 2SA959		
CIRCUIT VALUES	L_{coil} = 50 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω V_{clamp} (Unclamped)	L_{coil} = 180 μH, V_{CC} = 20 V R_{coil} = 0.05 Ω V_{clamp} = Rated V_{CEX} Value	L_{coil} = 40 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω, R_{BB2} = 50 Ω V_{clamp} (Unclamped)	R_L = 25 Ω, V_{CC} ≒ 150 V
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  D_1 = F114F D_2 = 6FH4S	OUTPUT WAVEFORM  $t_1 = \frac{L_{coil}(I_{C\,pk})}{V_{CC}}$ $t_2 = \frac{L_{coil}(I_{C\,pk})}{V_{clamp}}$		RESISTIVE TEST CIRCUIT 

NEC
ELECTRON DEVICE

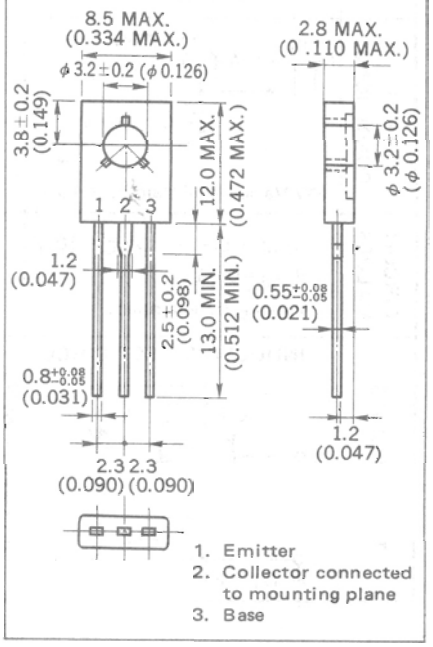
NPN SILICON POWER TRANSISTOR
2SC2752

DESCRIPTION The 2SC2752 is suitable for Low Power Switching regulator, DC-DC converter and High Voltage Switch.

FEATURES

- High Breakdown Voltage.
- Low Collector Saturation Voltage.
- High Speed Switching.
- Complementary to the NEC 2SA1156 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current	0.5	A
$I_{C(pulse)}$*	Collector Current	1.0	A
$I_{B(DC)}$	Base Current	0.25	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} *	DC Current Gain	20		80	—	V_{CE} = 5.0 V, I_C = 0.05 A
h_{FE2} *	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 0.3 A
t_{on}	Turn On Time			1.0	μs	(I_C = 0.3 A, I_{B1} = −I_{B2} = 0.06 A, PW ≒ 50 μs, R_L ≒ 500 Ω, V_{CC} ≒ 150 V)
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			1.0	μs	
$V_{ECO(sus)}$	Collector to Emitter Sustaining Voltage	400			V	Table 1, I_C = 0.3 A, I_{B1} = 0.06 A, L = 10 mH
$V_{CEX(sus)1}$	Collector to Emitter Sustaining Voltage	450			V	(Table 1, I_C = 0.3 A, I_{B1} = −I_{B2} = 0.06 A, V_{clamp} = Rated V_{CEX}, T_a = 125 °C, L = 10 mH)
$V_{CEX(sus)2}$	Collector to Emitter Sustaining Voltage	400			V	(Table 1, I_C = 0.6 A, I_{B1} = 0.2 A, I_{B2} = −0.06 A, V_{clamp} = Rated V_{CEX}, T_a = 125 °C, L = 10 mH)
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	(V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C)
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$ *	Collector Saturation Voltage			1.0	V	I_C = 0.3 A, I_B = 0.06 A
$V_{BE(sat)}$ *	Base Saturation Voltage			1.2	V	I_C = 0.3 A, I_B = 0.06 A

* Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

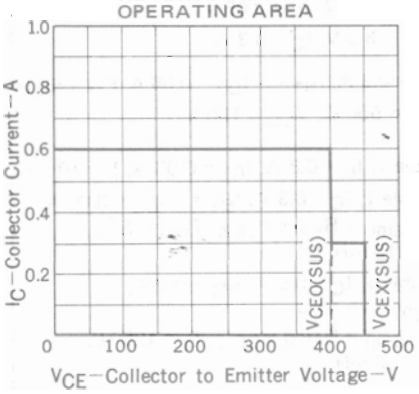
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

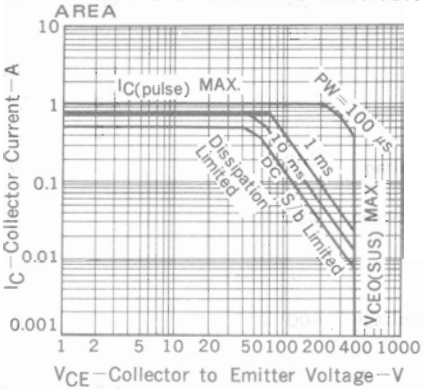
Test Conditions: V_{CE} = 5.0 V, I_C = 0.05 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

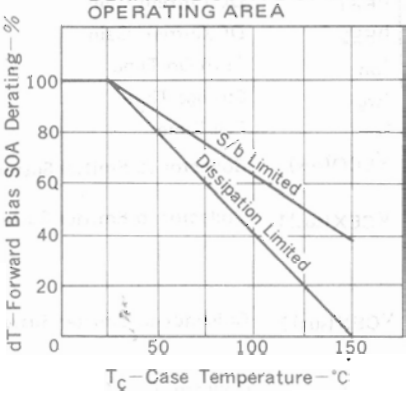
REVERSE BIAS SAFE OPERATING AREA



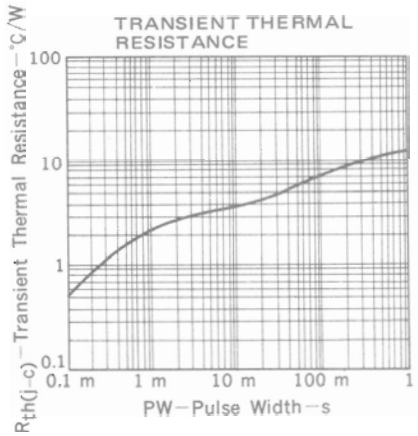
FORWARD BIAS SAFE OPERATION AREA



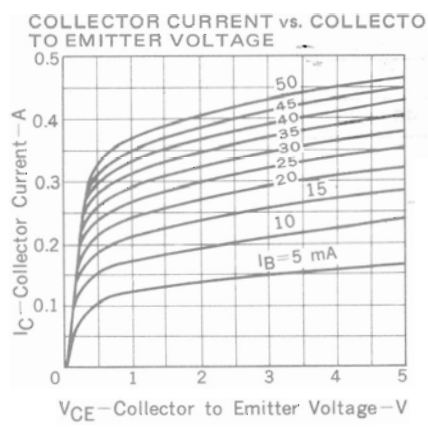
DERATING CURVE OF SAFE OPERATING AREA



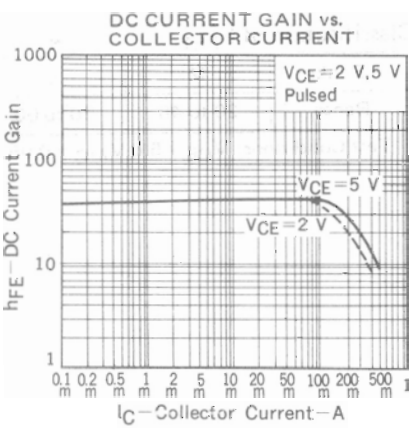
TRANSIENT THERMAL RESISTANCE



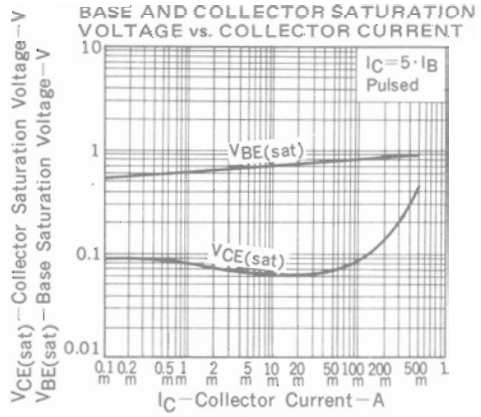
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

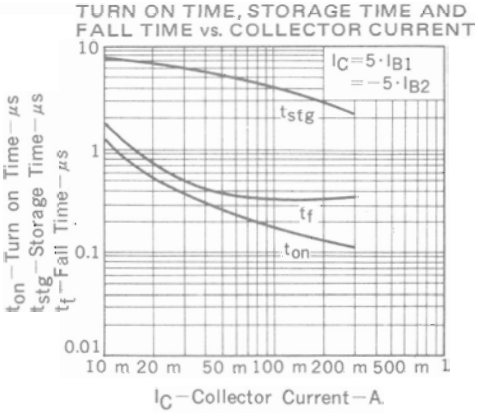
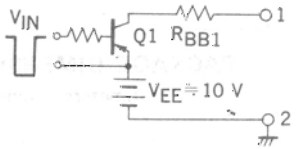
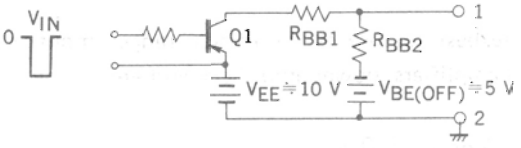
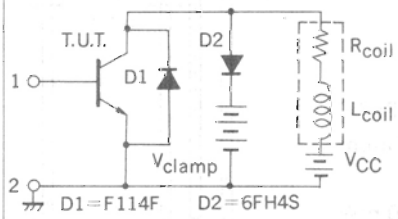
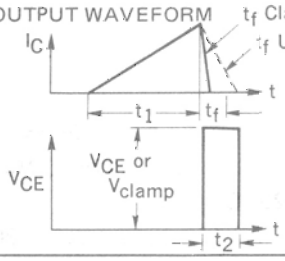
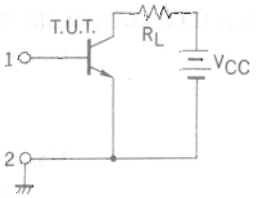


TABLE 1. – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V_{CEO} (SUS)	V_{CEX} (SUS)	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 10 A	 PW Varied to Attain I_C = 10 A Duty Cycle ≦ 2 % Q_1 = 2SA959	
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} ≦ 0.5 Ω V_{clamp} (Unclamped)	L_{coil} = 10 mH, V_{CC} = 20 V R_{coil} ≦ 0.5 Ω V_{clamp} = Rated V_{CEX} Value	R_L = 500 Ω, V_{CC} ≒ 150 V
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  D1 = F114F D2 = 6FH4S	OUTPUT WAVEFORM  $t_1 = \frac{L_{coil}(I_{C\ pk})}{V_{CC}}$ $t_2 = \frac{L_{coil}(I_{C\ pk})}{V_{clamp}}$	RESISTIVE TEST CIRCUIT 

NEC
ELECTRON DEVICE

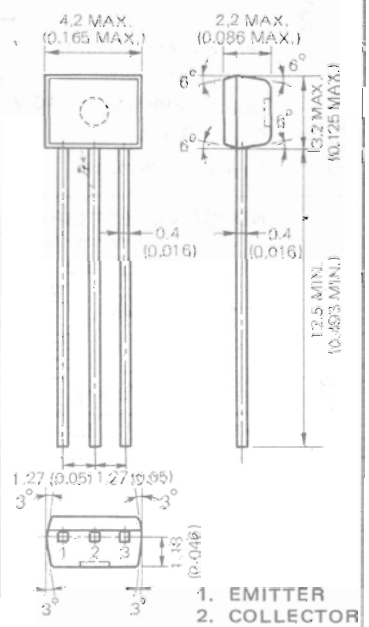
NPN SILICON TRANSISTOR
2SC2784

DESCRIPTION The 2SC2784 is the best for use as the middle range amplifier in Hi-Fi stereo control amplifiers, power amplifiers, and etc.

FEATURES

- High voltage. V_{CEO} : 120 V
- Low output capacitance. C_{ob} : 1.6 pF TYP. (V_{CB} = 30 V)
- High h_{FE} h_{FE} : 600 TYP. (V_{CE} = 6.0 V, I_C = 1.0 mA)
- Super low noise. NV : 25 mV TYP. (See test circuit.)
- Complementary to the NEC 2SA1174 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −55 to +125 °C
- Junction Temperature ..... +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation ..... 300 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage ..... 120 V
- V_{CEO} Collector to Emitter Voltage ..... 120 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 50 mA
- I_B Base Current ..... 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	580		—	V_{CE}=6.0 V, I_C=0.1 mA
h_{FE2}	DC Current Gain	200	600	1200	—	V_{CE}=6.0 V, I_C=1.0 mA
f_T	Gain Bandwidth Product	50	110		MHz	V_{CE}=6.0 V, I_E=1.0 mA
C_{ob}	Output Capacitance		1.6	2.5	pF	V_{CB}=30 V, I_E=0, f=1.0 MHz
NV	Noise Voltage		25	40	mV	V_{CE}=5.0 V, I_C=1.0 mA, R_G=100 kΩ
						G_V=80 dB, f=10 Hz to 1.0 kHz
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB}=120 V, I_E=0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55	0.59	0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.07	0.30	V	I_C=10 mA, I_B=1.0 mA

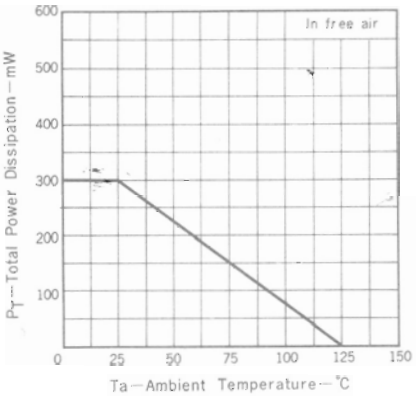
Classification of h_{FE2}

Rank	P	F	E	U
Range	200 – 400	300 – 600	400 – 800	600 – 1200

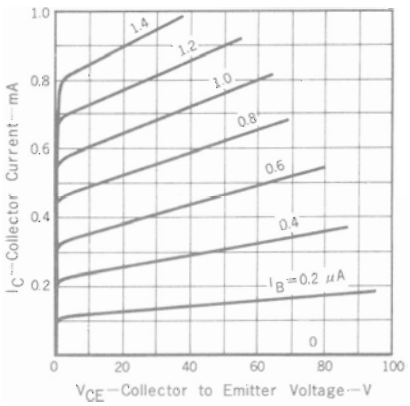
h_{FE2} Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

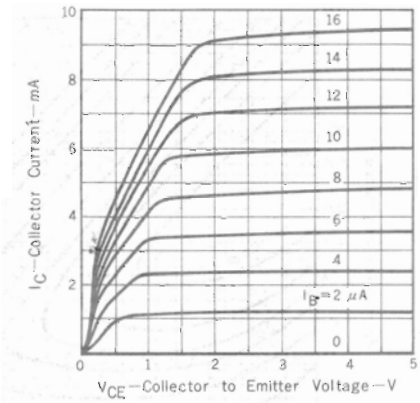
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



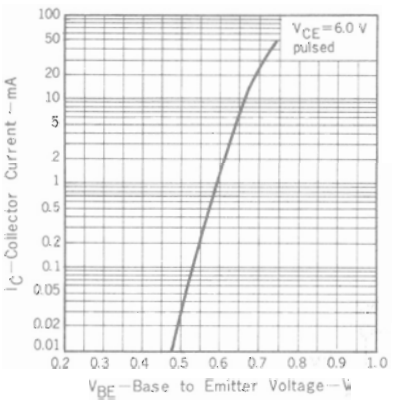
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



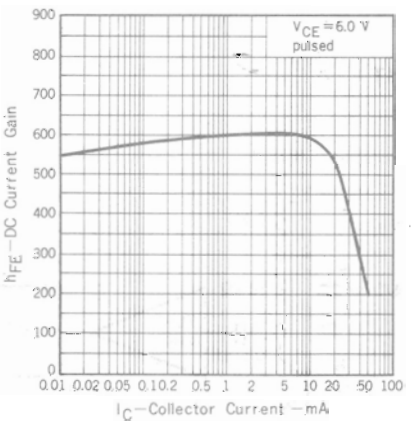
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



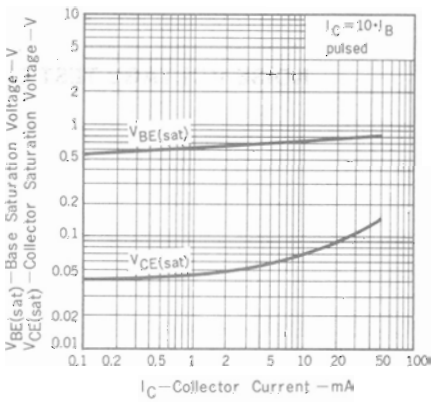
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



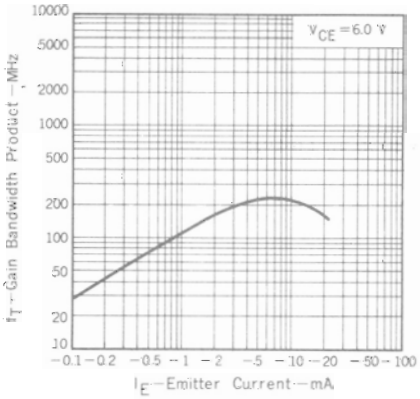
DC CURRENT GAIN vs. COLLECTOR CURRENT



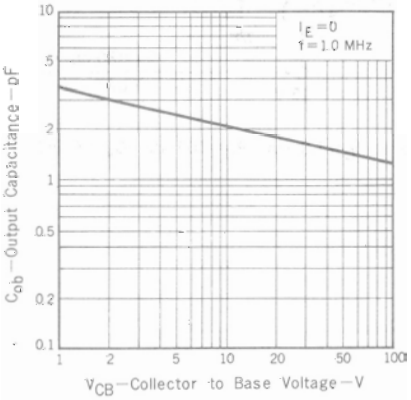
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



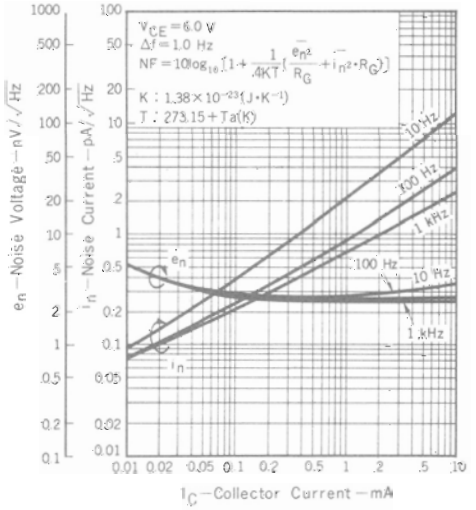
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



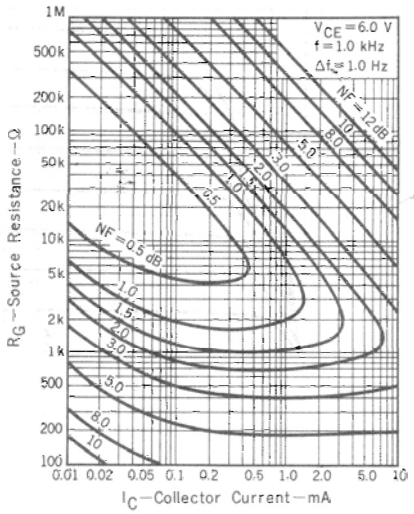
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



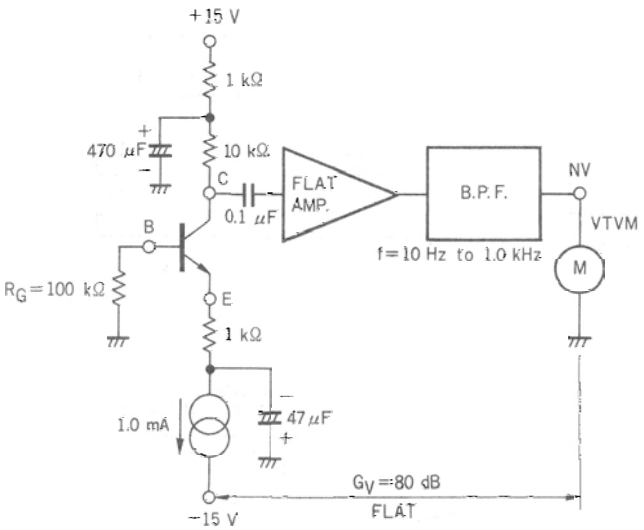
e_n AND i_n vs. COLLECTOR CURRENT



NOISE FIGURE MAP



NOISE VOLTAGE TEST CIRCUIT



V_{CE}≒5 V, I_C=1.0 mA, R_G=100 kΩ, G_V=80 dB, FLAT(f=10 Hz to 1.0 kHz)

NEC
ELECTRON DEVICE

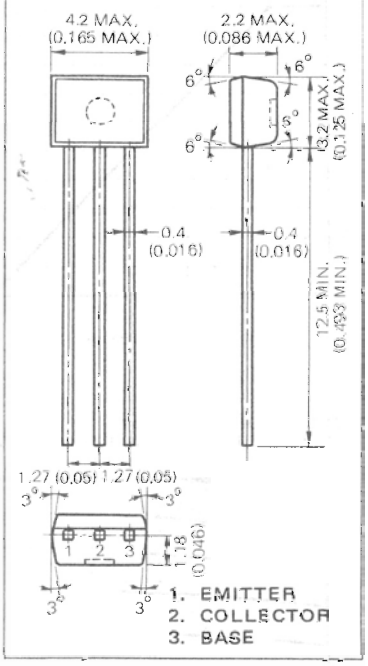
NPN SILICON TRANSISTOR
2SC2785

DESCRIPTION The 2SC2785 is designed for use in driver stage of AF amplifier and low speed switching.

FEATURES

- High Voltage V_{CEO} : 50 V MIN.
- Excellent h_{FE} Linearity : 0.92 TYP.
  h_{FE1} (0.1 mA)/h_{FE2} (1.0 mA)
- Complementary to the NEC 2SA1175 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... 60 V
- V_{CEO} Collector to Emitter Voltage ..... 50 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 100 mA
- I_B Base Current ..... 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	50	185			V_{CE}=6.0 V, I_C=0.1 mA
h_{FE2}	DC Current Gain	110	200	600		V_{CE}=6.0 V, I_C=1.0 mA
NF	Noise Figure		0.8	15	dB	V_{CE}=6.0 V, I_C=0.1 mA, R_G=2.0 kΩ, f=1.0 kHz
f_T	Gain Bandwidth Product	150	250	450	MHz	V_{CE}=6.0 V, I_E=−10 mA
C_{ob}	Collector to Base Capacitance		3.0	4.0	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55	0.62	0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.3	V	I_C=100 mA, I_B=10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.86	1.0	V	I_C=100 mA, I_B=10 mA

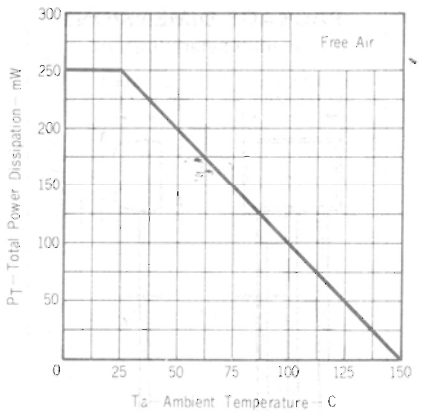
Classification of h_{FE2}

Rank	RF	JF	HF	FF	EF	KF
Range	110 – 180	135 – 220	170 – 270	200 – 320	250 – 400	300 – 600

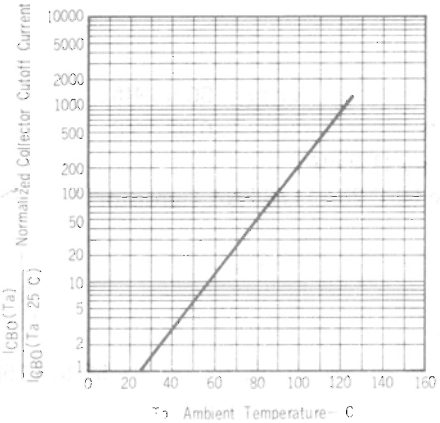
h_{FE2} Test Conditions : V_{CE}=6.0 V, I_C=1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

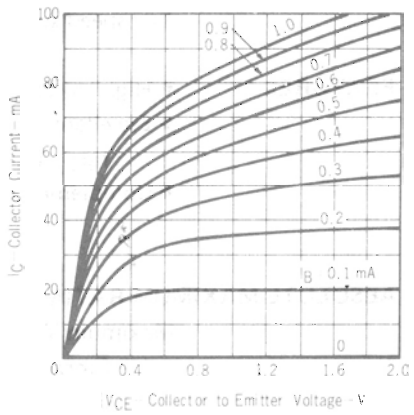
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



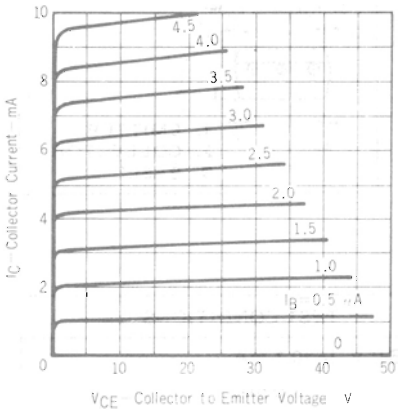
NORMALIZED COLLECTOR CUTOFF CURRENT vs. AMBIENT TEMPERATURE



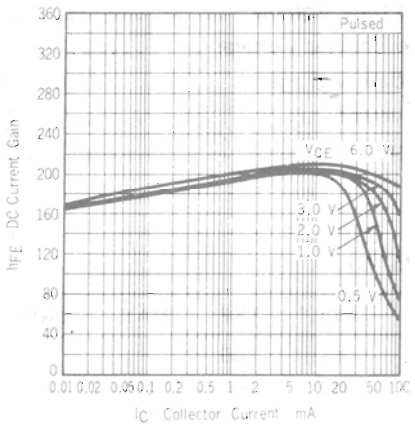
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



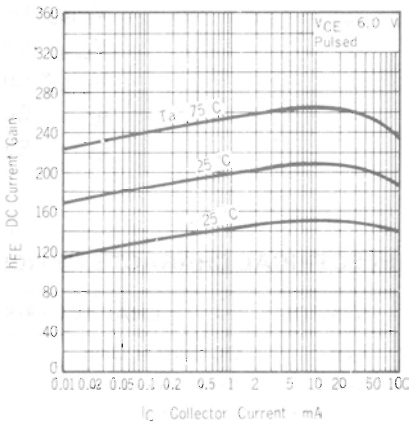
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



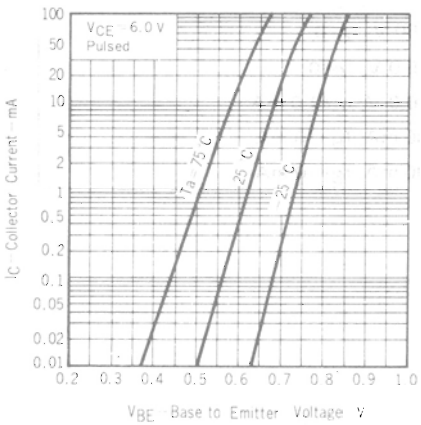
DC CURRENT GAIN vs. COLLECTOR CURRENT



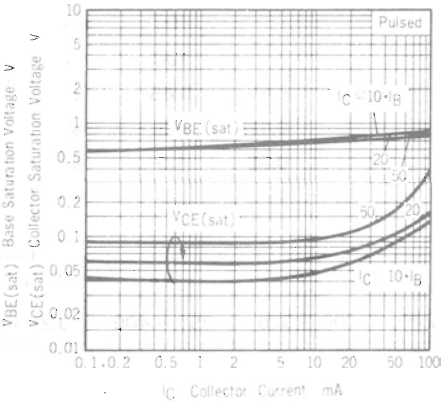
DC CURRENT GAIN vs. COLLECTOR CURRENT



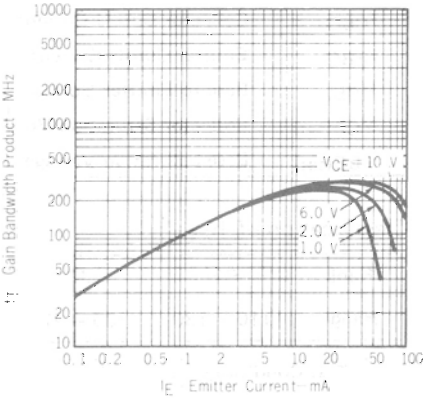
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



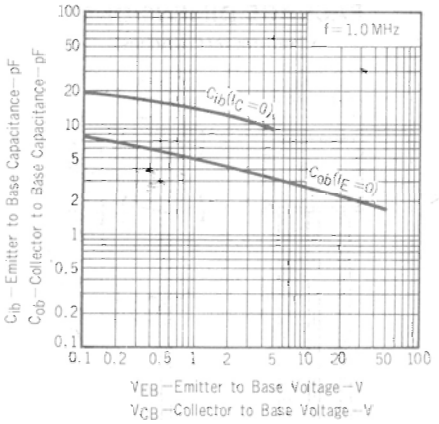
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



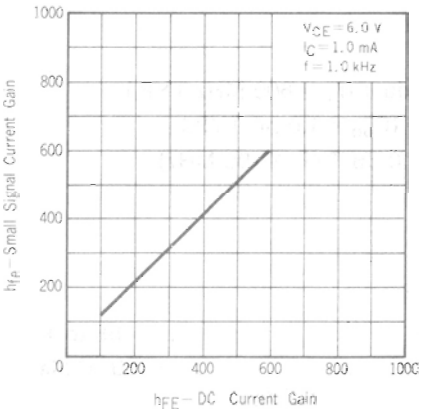
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



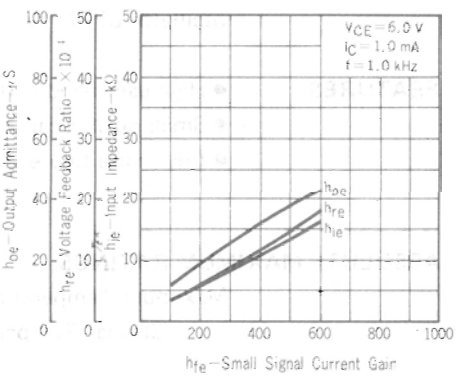
EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



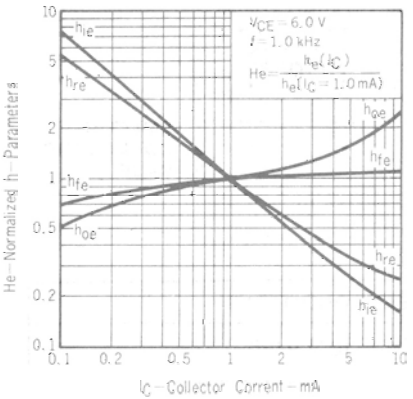
SMALL SIGNAL CURRENT GAIN vs. DC CURRENT GAIN



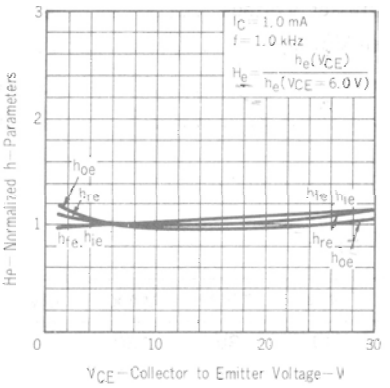
INPUT IMPEDANCE, VOLTAGE FEEDBACK RATIO AND OUTPUT ADMITTANCE vs. SMALL SIGNAL CURRENT GAIN



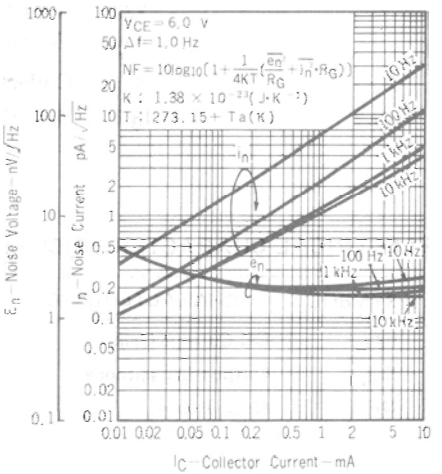
NORMALIZED h-PARAMETERS vs. COLLECTOR CURRENT



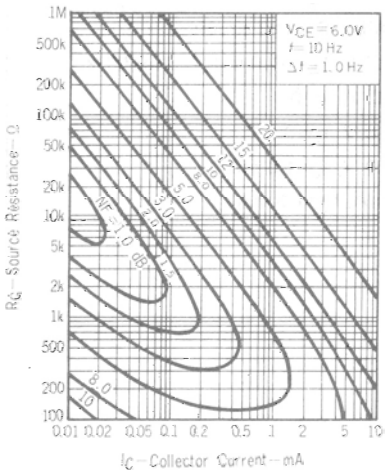
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



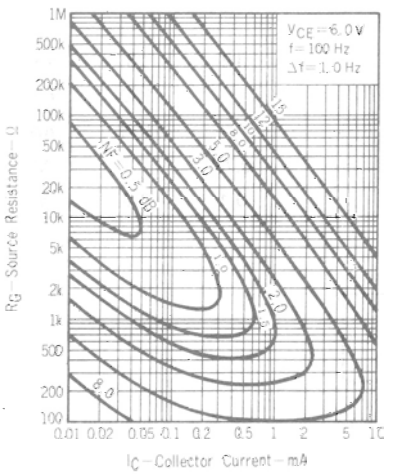
E_n AND I_n vs. COLLECTOR CURRENT



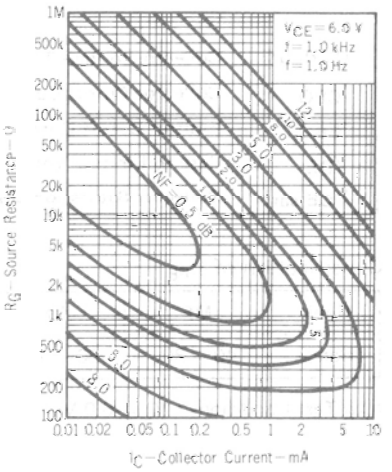
NOISE FIGURE MAP 1



NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NEC
ELECTRON DEVICE

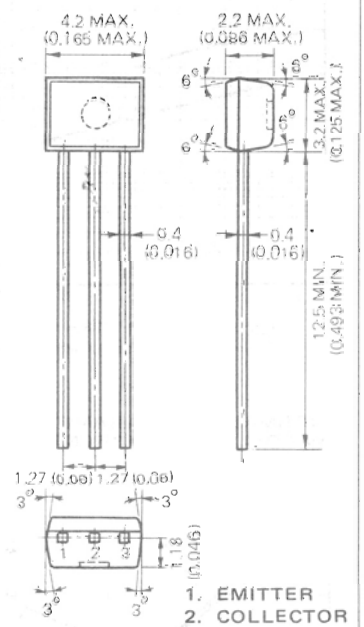
NPN SILICON TRANSISTOR
2SC2786

DESCRIPTION The 2SC2786 is designed for use in FM RF amplifier and local oscillator of FM tuner.

FEATURES

- High gain bandwidth product (f_T = 600 MHz TYP.)
- Small output capacitance (C_{ob} = 1.0 pF TYP.)
- Low noise figure (NF = 3.0 dB TYP. @100 MHz)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation ..... 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage ..... 30 V
- V_{CEO} Collector to Emitter Voltage ..... 20 V
- V_{EBO} Emitter to Base Voltage ..... 4.0 V
- I_C Collector Current ..... 20 mA
- I_B Base Current ..... 20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	90	180	–	V_{CE}=6.0 V, I_C=1.0 mA
C_{ob}	Output Capacitance		1.0	1.3	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
NF	Noise Figure		3.0	5.0	dB	V_{CE}=6.0 V, I_E=−1.0 mA, R_G=50 Ω f=100 MHz, See test circuit
f_T	Gain Bandwidth Product	400	600		MHz	V_{CE}=6.0 V, I_E=−1.0 mA
G_{pe}	Power Gain	18	22		dB	V_{CE}=6.0 V, I_E=−1.0 mA, R_G=50 Ω f=100 MHz, See test circuit
C_c·rb'b	Collector to Base Time Constant		12	15	ps	V_{CE}=6.0 V, I_E=−1.0 mA, f=31.9 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=4.0 V, I_C=0
V_{BE}	Base to Emitter Voltage		0.72		V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.3	V	I_C=10 mA, I_B=1.0 mA

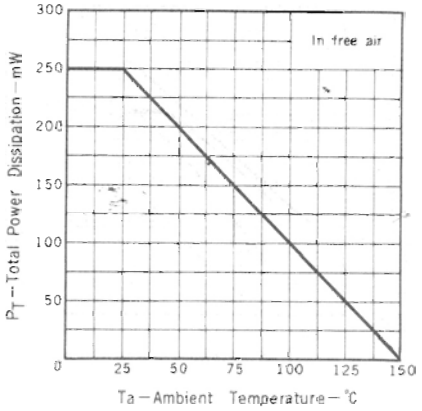
Classification of h_{FE}

Rank	MF	LF	KF
Range	40 – 80	60 – 120	90 – 180

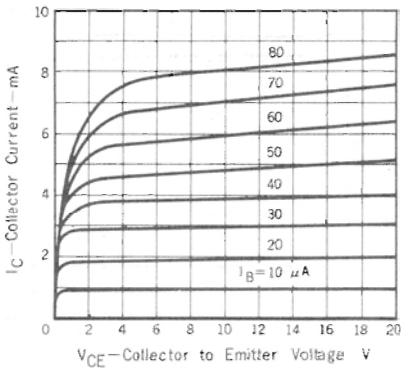
h_{FE} Test Conditions : V_{CE}=6.0 V, I_C=1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

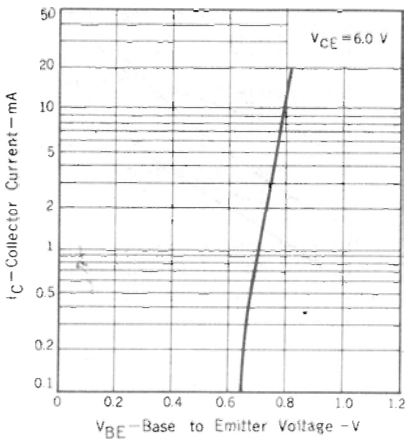
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



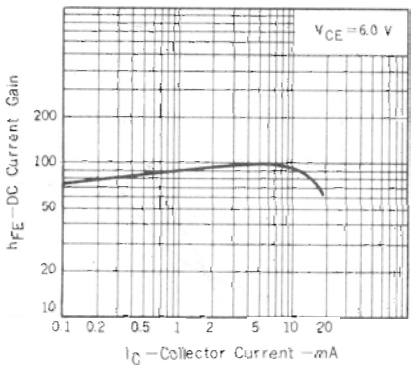
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



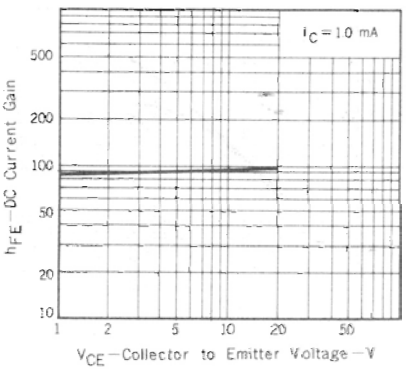
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



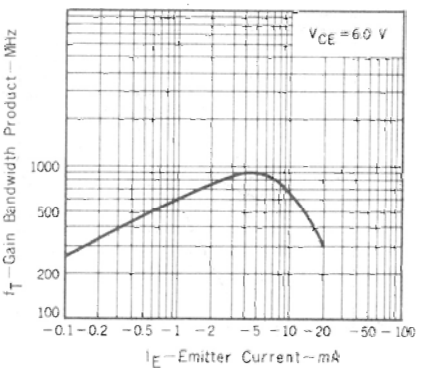
DC CURRENT GAIN vs. COLLECTOR CURRENT



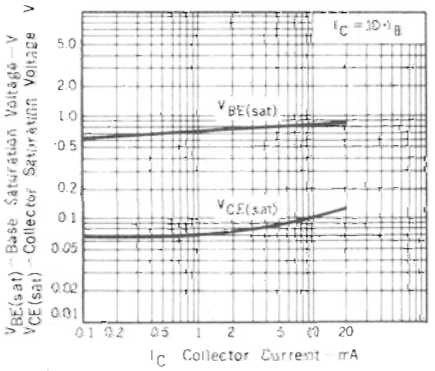
DC CURRENT GAIN vs. COLLECTOR TO EMITTER VOLTAGE



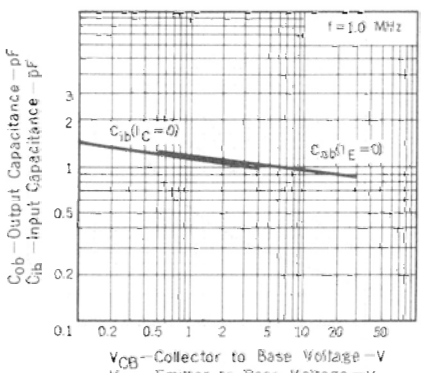
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



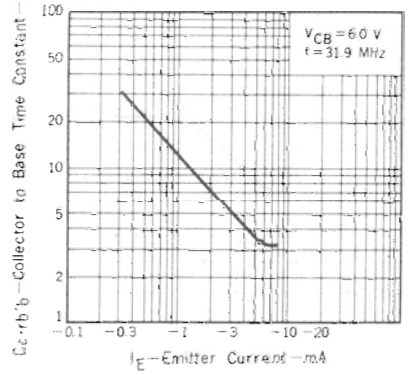
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



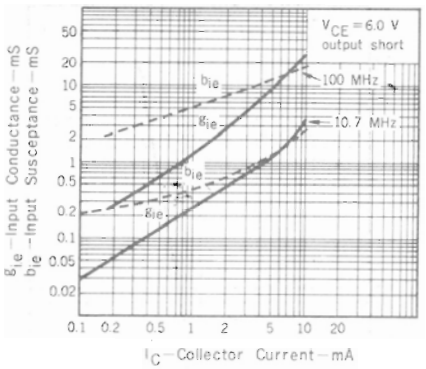
INPUT CAPACITANCE vs. EMITTER TO BASE VOLTAGE, OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



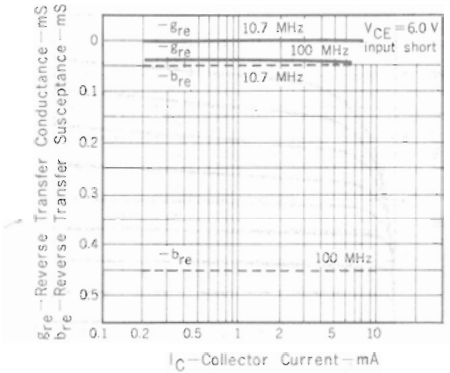
COLLECTOR TO BASE TIME CONSTANT vs. EMITTER CURRENT



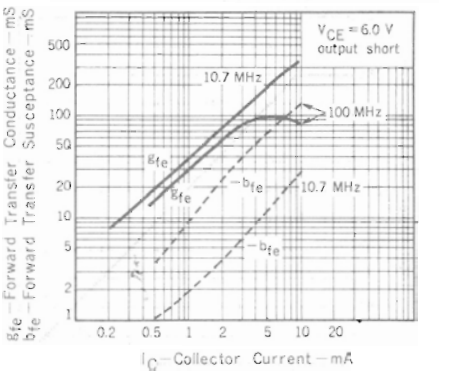
INPUT ADMITTANCE vs. COLLECTOR CURRENT



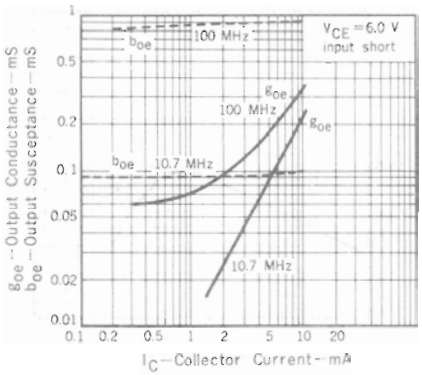
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



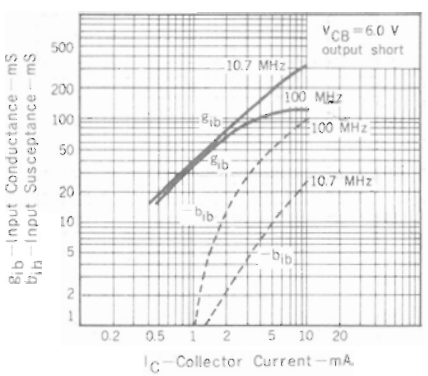
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



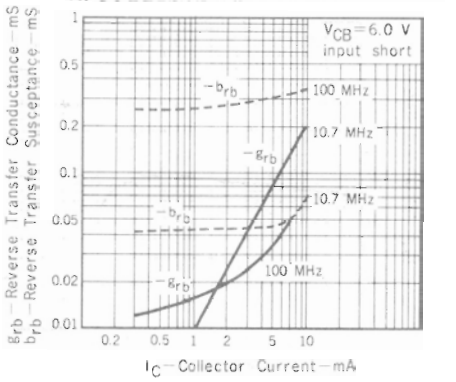
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



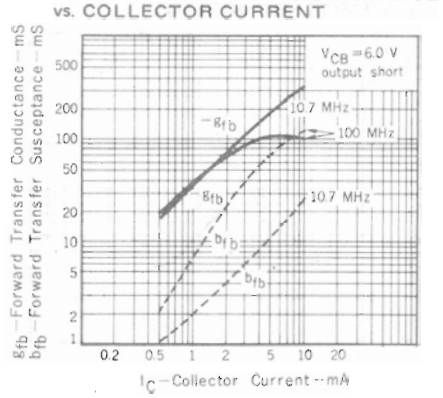
INPUT ADMITTANCE vs. COLLECTOR CURRENT



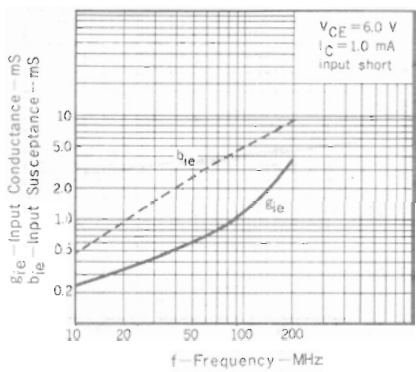
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



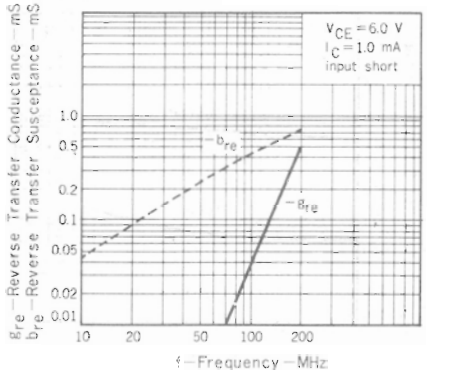
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



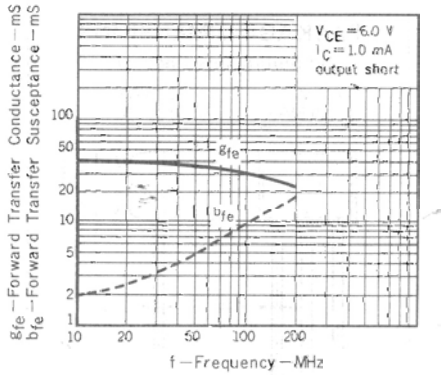
INPUT ADMITTANCE vs. FREQUENCY



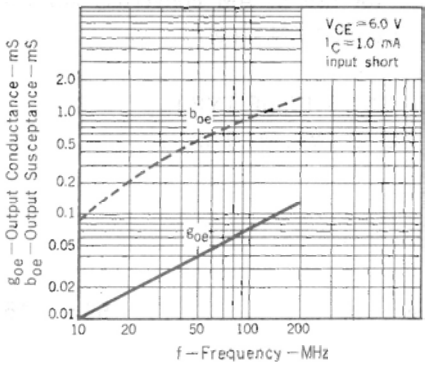
REVERSE TRANSFER ADMITTANCE vs. FREQUENCY



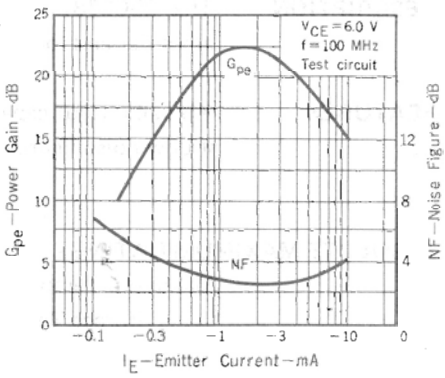
FORWARD TRANSFER ADMITTANCE vs. FREQUENCY



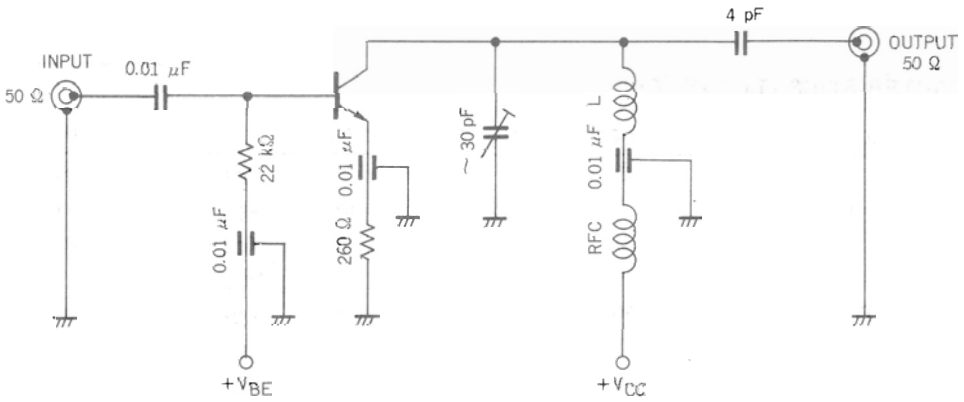
OUTPUT ADMITTANCE vs. FREQUENCY



POWER GAIN, NOISE FIGURE vs. EMITTER CURRENT



100MHz G_{pe}, NF TEST CIRCUIT



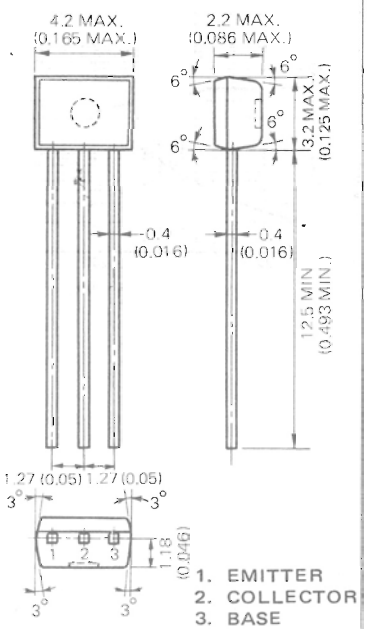
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC2787

DESCRIPTION The 2SC2787 is designed for use in AM converter, AM/FM IF amplifier and local oscillator of AM/FM tuner.

FEATURES
- Small output capacitance (C_{ob} = 1.9 pF TYP.)
- Low noise figure (NF = 2.0 dB TYP. @1.0 MHz)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation ..... 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage ..... 50 V
- V_{CEO} Collector to Emitter Voltage ..... 30 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 30 mA
- I_B Base Current ..... 30 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	40	90	180	–	V_{CE}=6.0 V, I_C=1.0 mA
C_{ob}	Output Capacitance		1.9	2.2	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
NF	Noise Figure		2.0	4.0	dB	V_{CE}=6.0 V, I_E=−1.0 mA, R_G=500 Ω, f=1.0 MHz
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE}=6.0 V, I_E=−1.0 mA
C_c·rb'b	Collector to Base Time Constant		10	15	ps	V_{CE}=6.0 V, I_E=−10 mA, f=31.9 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.65	0.70	0.75	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.08	0.30	V	I_C=10 mA, I_B=1.0 mA

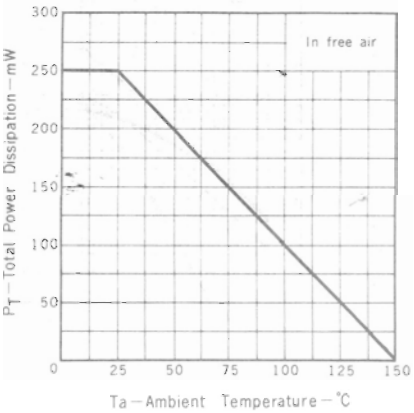
Classification of h_{FE}

Rank	MF	LF	KF
Range	40 – 80	60 – 120	90 – 180

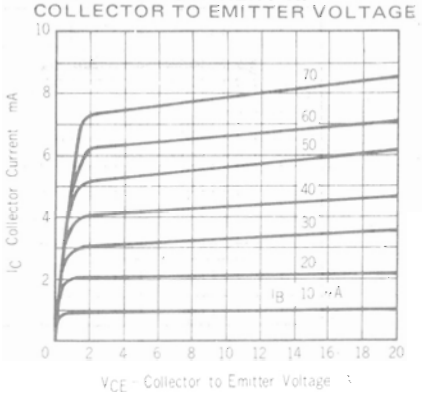
h_{FE} Test Conditions : V_{CE}=6.0 V, I_C=1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

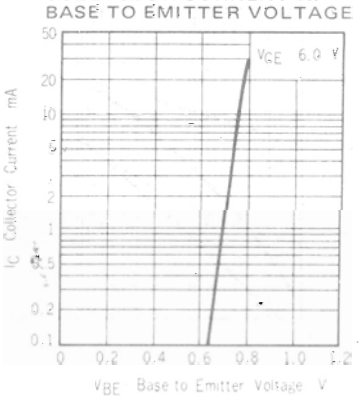
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



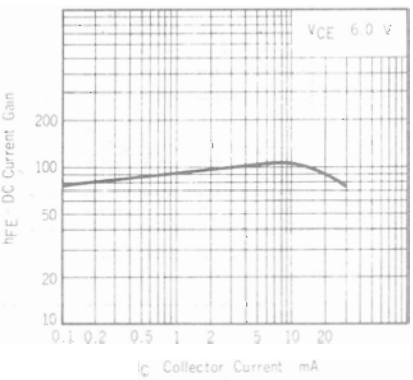
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



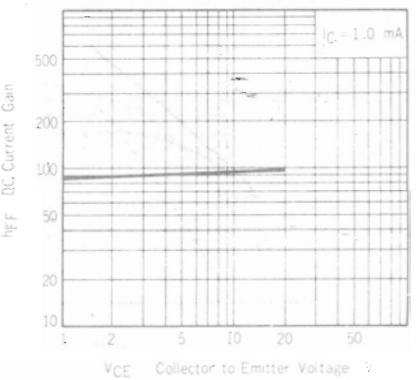
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



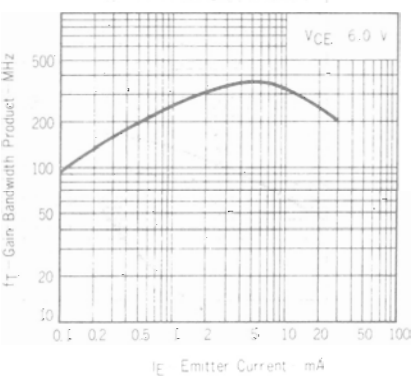
DC CURRENT GAIN vs. COLLECTOR CURRENT



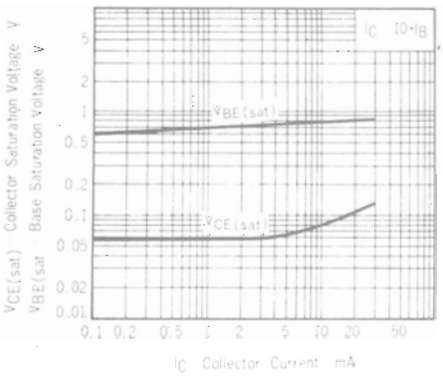
DC CURRENT GAIN vs. COLLECTOR TO EMITTER VOLTAGE



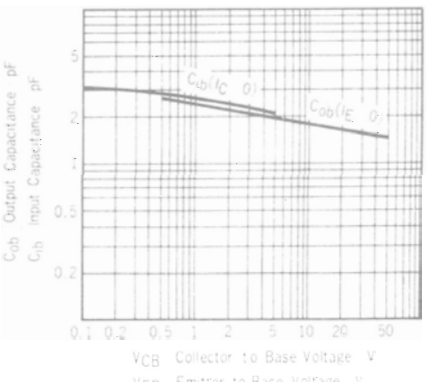
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



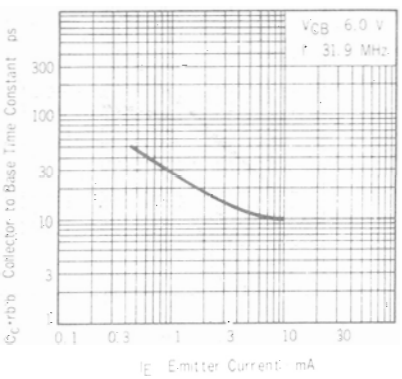
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



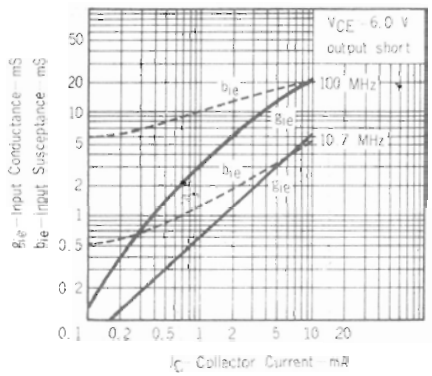
INPUT CAPACITANCE vs. EMITTER TO BASE VOLTAGE, OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



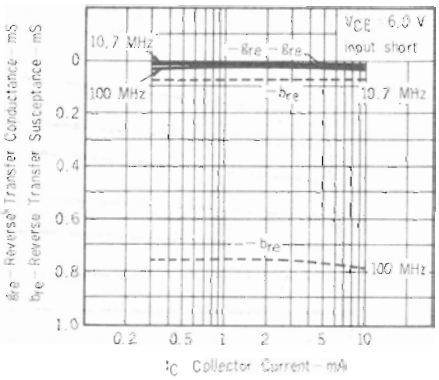
COLLECTOR TO BASE TIME CONSTANT vs. EMITTER CURRENT



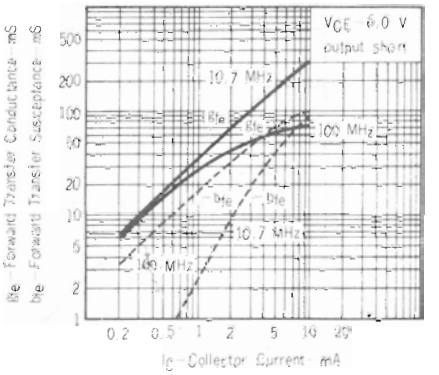
INPUT ADMITTANCE vs. COLLECTOR CURRENT



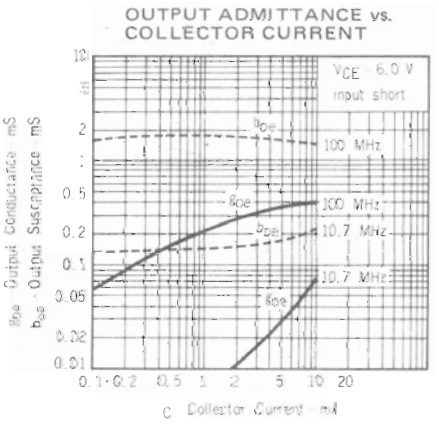
REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



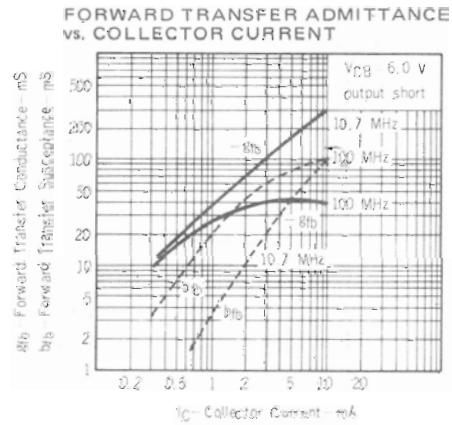
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



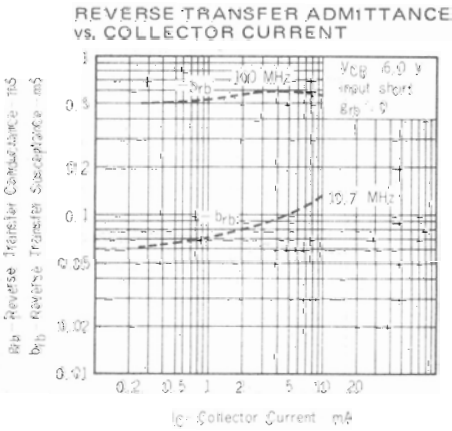
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



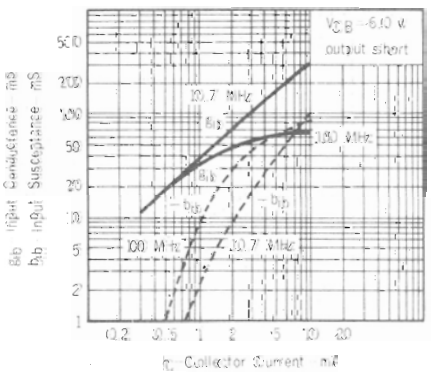
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



REVERSE TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



INPUT ADMITTANCE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

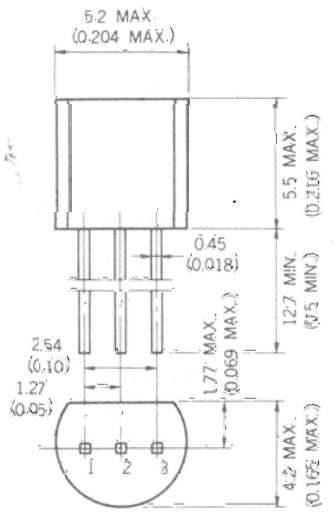
NPN SILICON TRANSISTOR
2SC2901

DESCRIPTION The 2SC2901 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 600 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	40 V
V_{CES}	Collector to Emitter Voltage	40 V
V_{CEO}	Collector to Emitter Voltage	15 V
V_{EBO}	Emitter to Base Voltage	5.0 V
I_C	Collector Current	200 mA
I_C	Collector Current (10 μs pulse)	500 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time		8.0	12	ns	V_{CC} = 3.0 V, I_C = 10 mA, I_{B1} = 3.0 mA, V_{BE} = −1.5 V
t_{off}	Turn-off Time		12	18	ns	V_{CC} = 3.0 V, I_C = 10 mA, I_{B1} = 3.0 mA, I_{B2} = −1.5 mA
t_{stg}	Storage Time		6.0	13	ns	I_C = 10 mA, I_{B1} = −I_{B2} = 10 mA
f_T	Gain Bandwidth Product	500	750		MHz	V_{CE} = 10 V, I_E = −10 mA, f = 100 MHz
C_{ob}	Output Capacitance		1.8	4.0	pF	V_{CB} = 5.0 V, I_E = 0, f = 1 MHz
h_{FE}*	DC Current Gain	40	90	200	–	V_{CE} = 1.0 V, I_C = 10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.15	0.25	V	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.80	0.85	V	I_C = 10 mA, I_B = 1.0 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 20 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB} = 3.0 V, I_C = 0

*Pulsed PW ≤ 350 μs, duty cycle ≤ 2 %

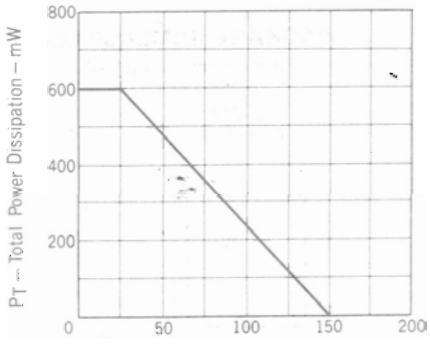
Classification of h_{FE}

Rank	L	K
Range	40 – 120	100 – 200

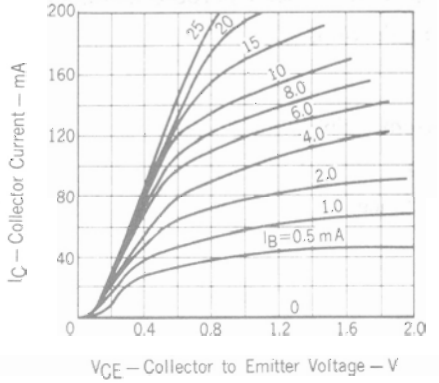
Test Conditions : V_{CE} = 1.0 V, I_C = 10 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

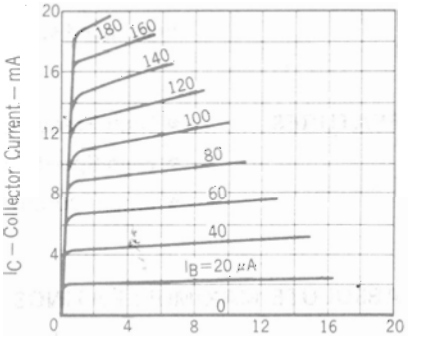
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



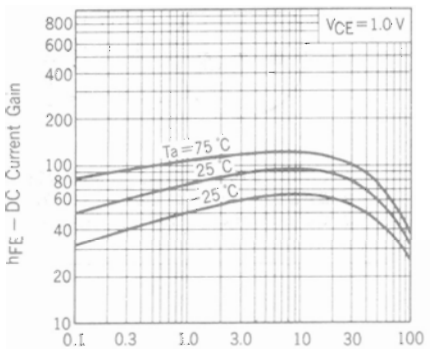
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



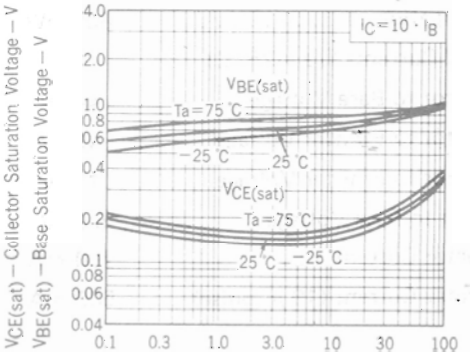
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



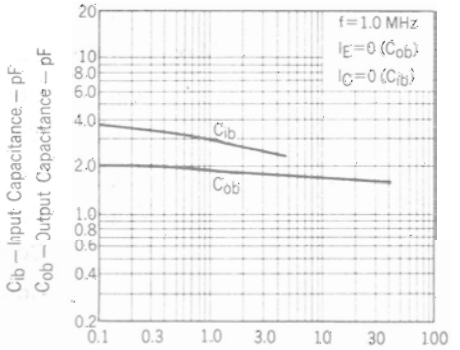
DC CURRENT GAIN vs. COLLECTOR CURRENT



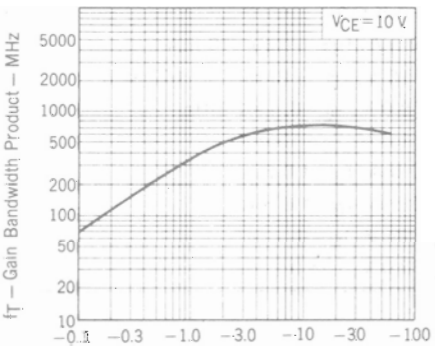
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



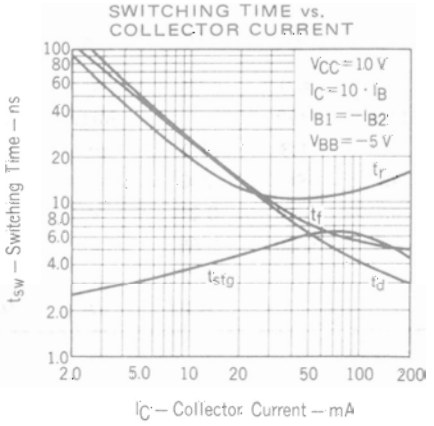
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



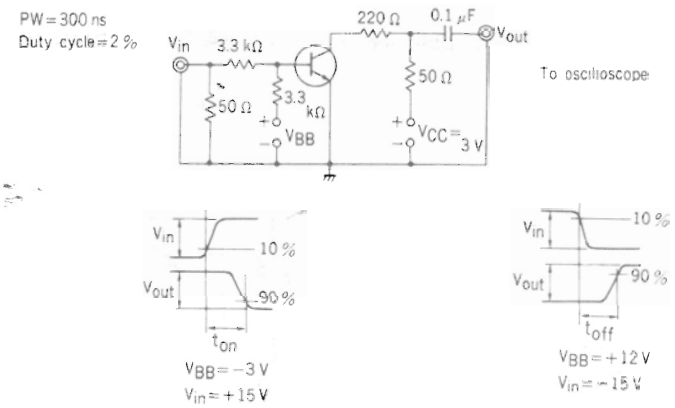
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



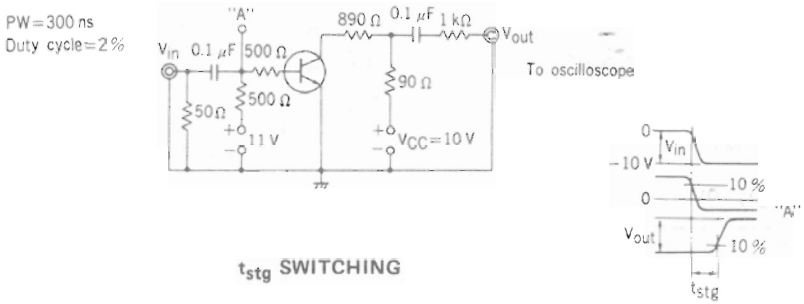
SWITCHING TIME vs. COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT



t_{on}, t_{off} SWITCHING



t_{stg} SWITCHING

Voltage waveforms

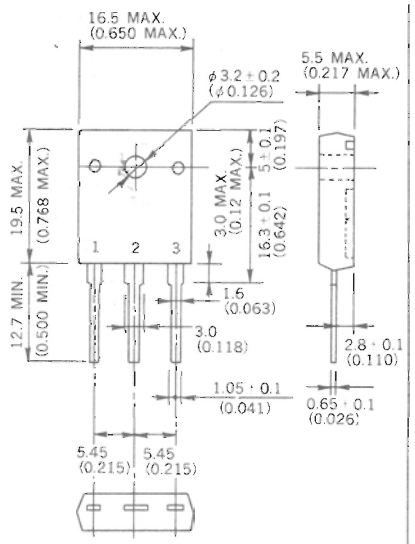
NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC2908

DESCRIPTION The 2SC2908 is designed for high speed switching.
It is suitable for switching regulators and ultrasonic appliance applications.

FEATURES
- Low collector saturation voltage.
- High Speed Switching.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

Total Power Dissipation . . . . . 50 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	200	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	12	V
$I_{C(DC)}$	Collector Current (DC)	5	A
$I_{C(pulse)}$	Collector Current (Fulse)*	10	A
$I_{B(DC)}$	Base Current (DC)	2.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			0.5	μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.3 A R_L = 16.7 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			2.0	μs	
t_f	Fall Time			1.0	μs	
h_{FE1}	DC Current Gain**	60	160	320	—	V_{CE} = 5 V, I_C = 0.3 A
h_{FE2}	DC Current Gain**	40			—	V_{CE} = 5 V, I_C = 3 A
$V_{CE(sat)}$	Collector Saturation Voltage**			1.0	V	I_C = 3.0 A, I_B = 0.3 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.5	V	I_C = 3.0 A, I_B = 0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 3.0 A, I_B = 0.3 A, L = 1.0 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	150			V	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.3 A, T_a = 125 °C, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 6.0 A, I_{B1} = 0.6 A, −I_{B2} = 0.3 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 100 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			500	μA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

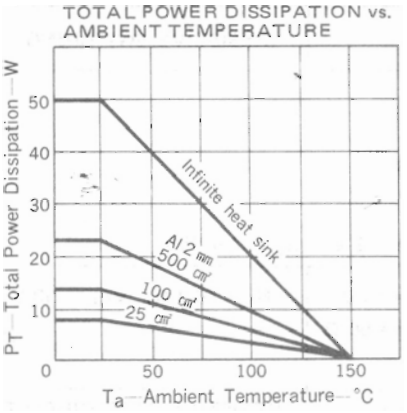
Classification of h_{FE1}

Rank	K	L	M
Range	160 to 320	100 to 200	60 to 120

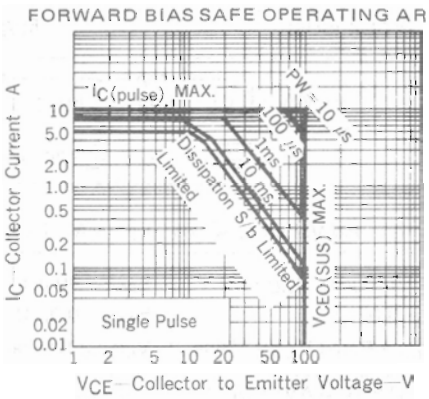
Test Conditions : V_{CE} = 5.0 V, I_C = 0.3 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

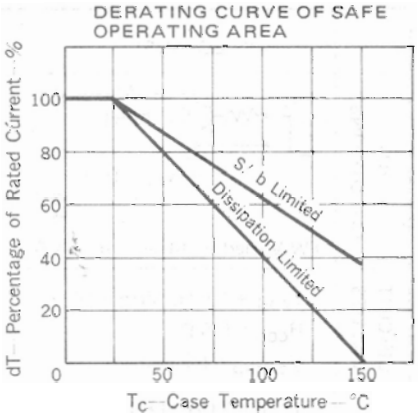
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



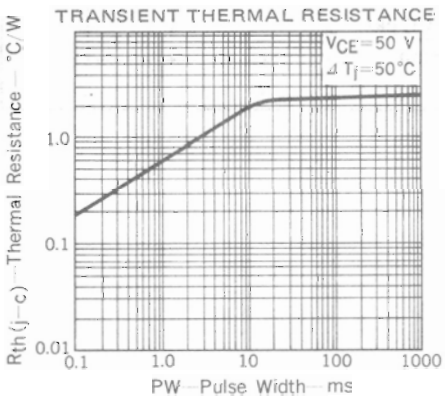
FORWARD BIAS SAFE OPERATING AREA



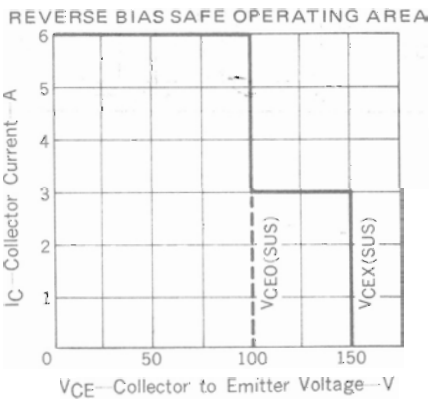
DERATING CURVE OF SAFE OPERATING AREA



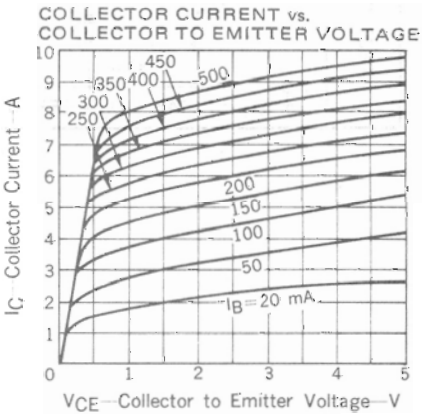
TRANSIENT THERMAL RESISTANCE



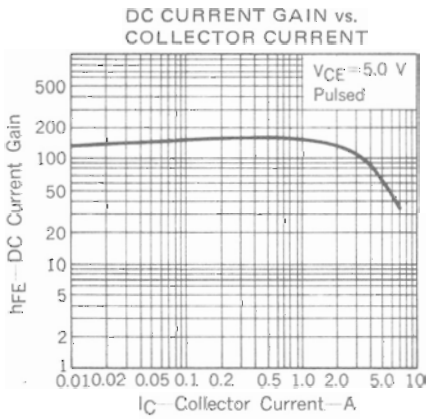
REVERSE BIAS SAFE OPERATING AREA



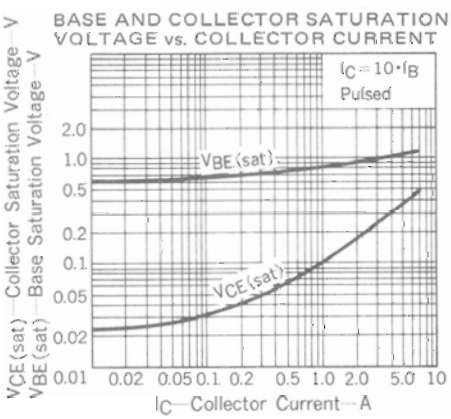
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

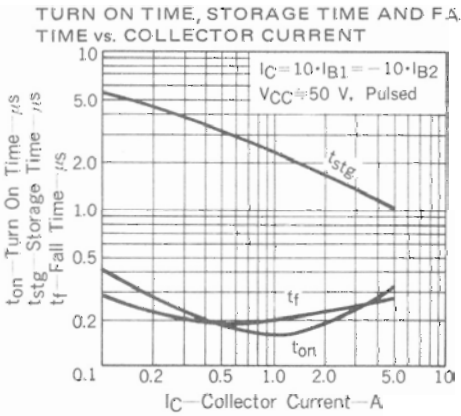
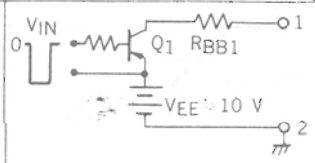
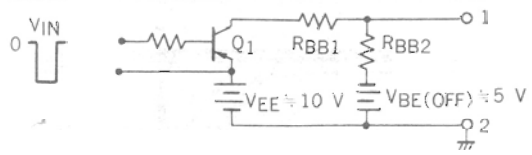
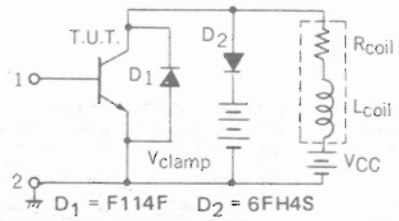
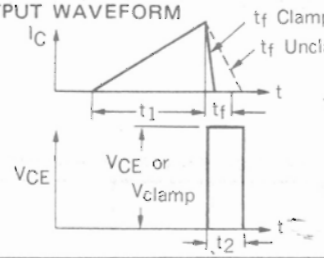
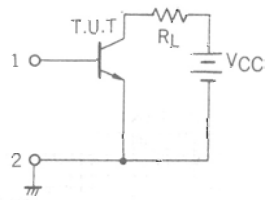


TABLE 1.—TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V_{CEO} (SUS)	V_{CEX} (SUS)	$E_{S/B}$	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 5 A	 PW Varied to Attain I_C = 5 A Duty Cycle ≦ 2 % Q_1 = 2SA959		
CIRCUIT VALUES	L_{coil} = 1 mH, V_{CC} = 10 V R_{coil} = 0.5 Ω V_{clamp} (Unclamped)	L_{coil} = 180 μH, V_{CC} = 20 V R_{coil} = 0.05 Ω V_{clamp} = Rated V_{CEX} Value	L_{coil} = 40 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω, R_{BB2} = 50 Ω V_{clamp} (Unclamped)	R_L = 16.7 Ω, V_{CC} ≒ 50 V
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  D_1 = F114F D_2 = 6FH4S	OUTPUT WAVEFORM  $t_1 = \frac{L_{coil}(I_{C\,pk})}{V_{CC}}$ $t_2 = \frac{L_{coil}(I_{C\,pk})}{V_{clamp}}$		RESISTIVE TEST CIRCUIT 

NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC3209

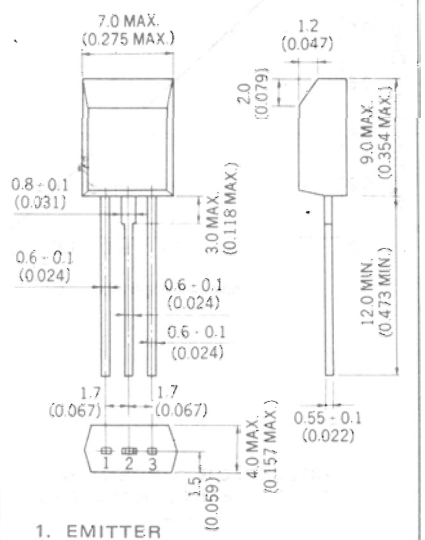
DESCRIPTION

The 2SC3209 is designed for use in TV chroma output circuits and TV horizontal deflection output circuits.

FEATURES

- High voltage $V_{CEO} \geq 300$ V
- High Electrostatic-Discharge-Resistant (E-B reverse bias, C=2 300 pF) V_{ESDR}: TYP. 1 000 V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 300 V
- V_{CEO} Collector to Emitter Voltage . . . . . 300 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE} *	DC Current Gain	60	150	250		V_{CE} = 10 V, I_C = 10 mA
t_d	Delay Time			1.0	μs	(V_{CC} = 30 V, I_C = 100 mA, $I_{B1} = -I_{B2}$ = 10 mA)
t_r	Rise Time			1.0	μs	
t_{stg}	Storage Time			2.0	μs	
t_f	Fall Time			1.0	μs	
f_T	Gain Bandwidth Product		50		MHz	V_{CE} = 30 V, I_E = −10 mA
V_{ESDR}	Electrostatic-Discharge-Resistant		1000		V	See Test Circuit
C_{ob}	Output Capacitance		2.8	3.5	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE} *	Base to Emitter Voltage	600	670	700	mV	V_{CE} = 10 V, I_C = 10 mA
$V_{CE(sat)}$ *	Collector Saturation Voltage		0.15	1.5	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.80	1.5	V	I_C = 50 mA, I_B = 5.0 mA

* Pulsed PW≤300 μs, duty cycle≤2 %

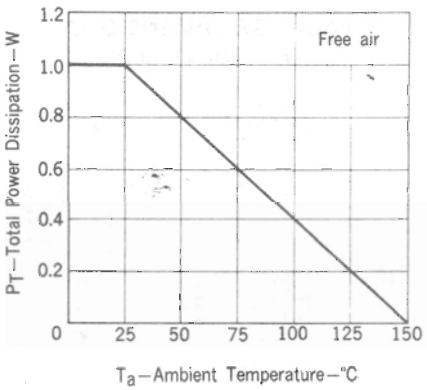
Classification of h_{FE1}

Rank	M	L	K
Range	60 – 120	100 – 200	160 – 250

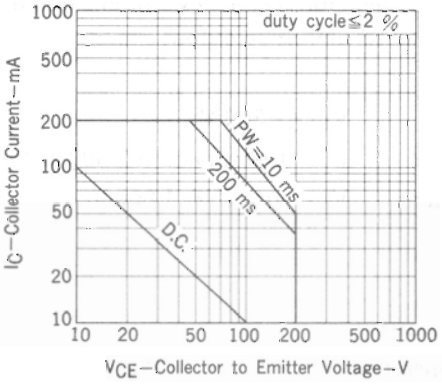
Test Conditions: V_{CE} = 10 V, I_C = 10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

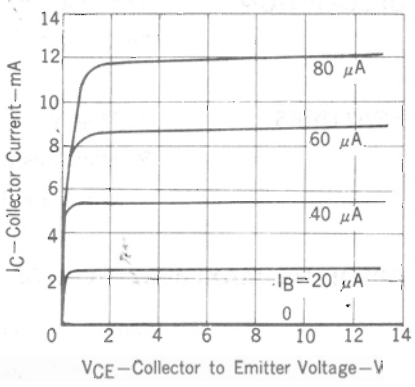
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



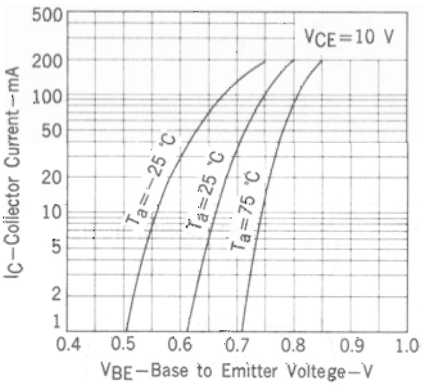
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



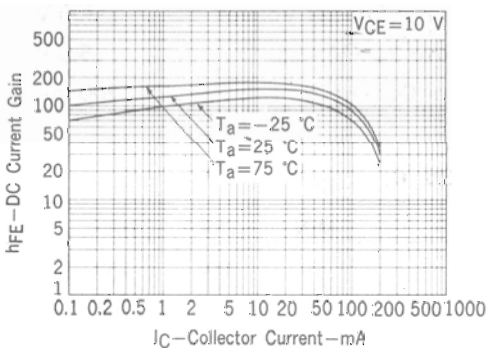
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



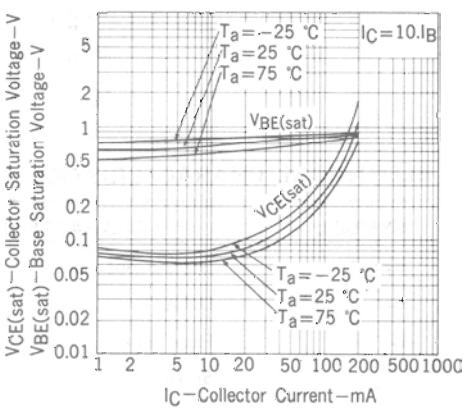
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



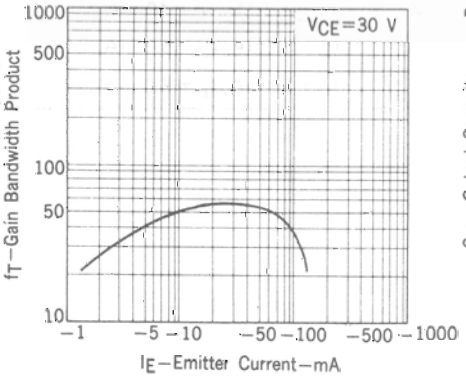
DC CURRENT GAIN vs. COLLECTOR CURRENT



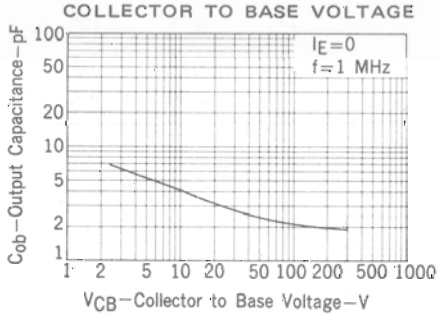
COLLECTOR SATURATION VOLTAGE, BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



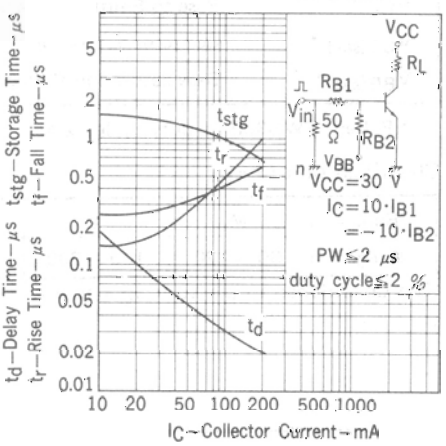
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



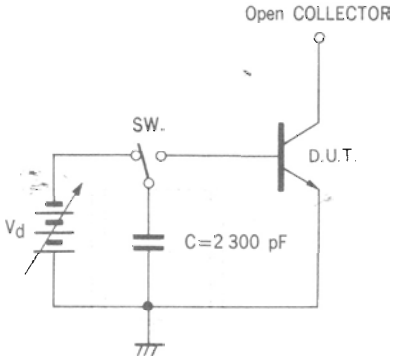
OUTPUT CAPACITANCE vs COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



ELECTROSTATIC-DISCHARGE-RESISTANT TEST CIRCUIT



TEST CONDITION

1) E-B reverse bias
2) C = 2 300 pF
3) Apply one shot pluse to D.U.T. (Transistor Under the Test) by SW.

JUDGEMENT

REJECT; BV_{EBO} waveform defect
As a result if D.U.T. is not rejected, apply higher voltage to capacitor and test again.

NEC
ELECTRON DEVICE

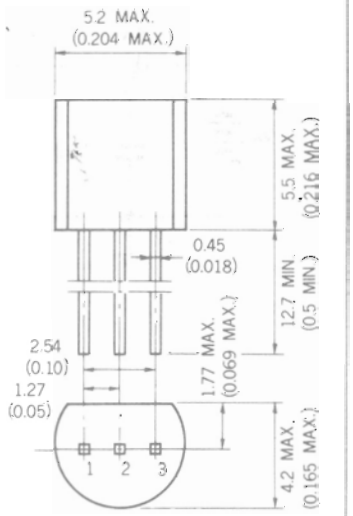
SILICON TRANSISTOR
2SC3355

DESCRIPTION The 2SC3355 is an NPN silicon epitaxial transistor designed for low noise amplifier at VHF, UHF and CATV band.
It has large dynamic range and good current characteristic.

FEATURES

- Low Noise and High Gain
  NF=1.1 dB TYP., G_a=8.0 dB TYP. @V_{CE}=10 V, I_C=7 mA, f=1.0 GHz
  NF=1.8 dB TYP., G_a=9.0 dB TYP. @V_{CE}=10 V, I_C=40 mA, f=1.0 GHz
- High Power Gain
  MAG=11 dB TYP. @V_{CE}=10 V, I_C=20 mA, f=1.0 GHz

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −65 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation ..... 600 mW

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage ..... 20 V
- V_{CEO} Collector to Emitter Voltage ..... 12 V
- V_{EBO} Emitter to Base Voltage ..... 3.0 V
- I_C Collector Current ..... 100 mA

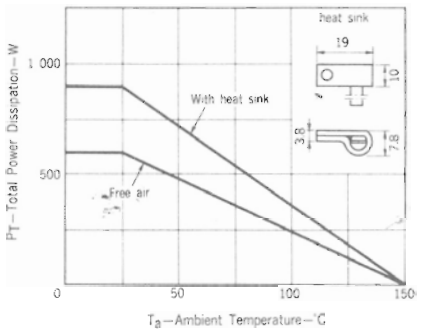
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB}=10 V, I_E=0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB}=1.0 V, I_C=0
h_{FE}	DC Current Gain	50	120	300		V_{CE}=10 V, I_C=20 mA
f_T	Gain Bandwidth Product		6.5		GHz	V_{CE}=10 V, I_C=20 mA
C_{ob}*	Output Capacitance		0.65	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$\|S_{21e}\|^2$	Insertion Power Gain		9.5		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
NF	Noise Figure		1.1		dB	V_{CE}=10 V, I_C=7 mA, f=1.0 GHz
NF	Noise Figure		1.8	3.0	dB	V_{CE}=10 V, I_C=40 mA, f=1.0 GHz

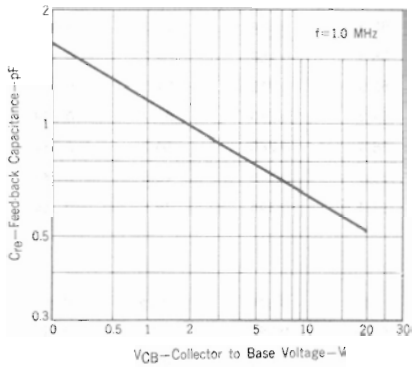
* The emitter terminal should be connected to the gurad terminal of the three-terminal capacitance bridge.

TYPICAL CHARACTERISTICS (T_a=25 °C)

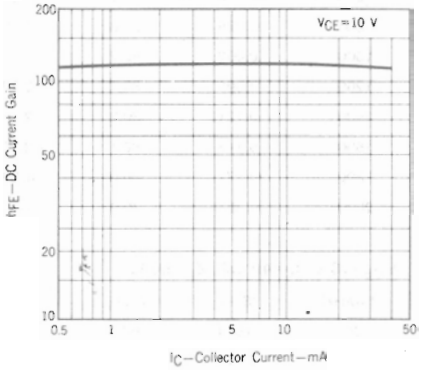
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



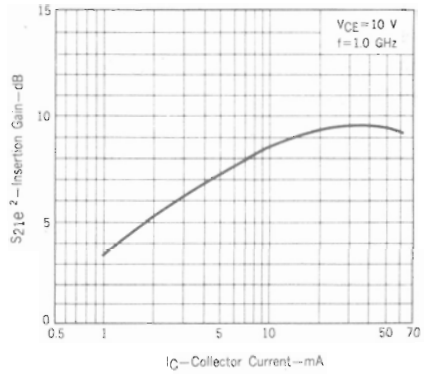
FEED-BACK CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



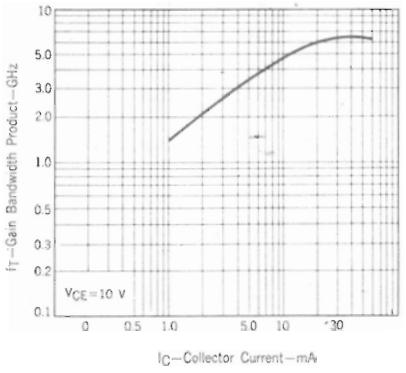
DC CURRENT GAIN vs. COLLECTOR CURRENT



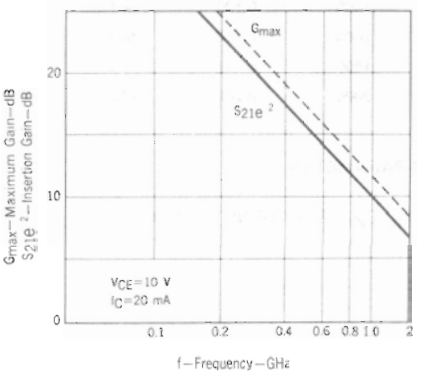
INSERTION GAIN vs. COLLECTOR CURRENT



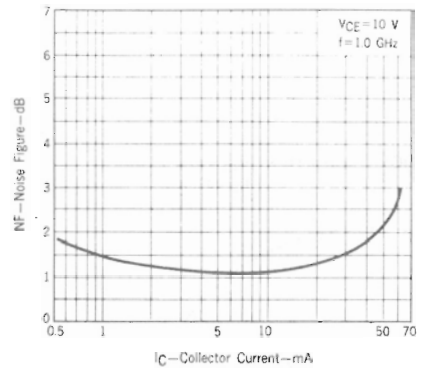
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



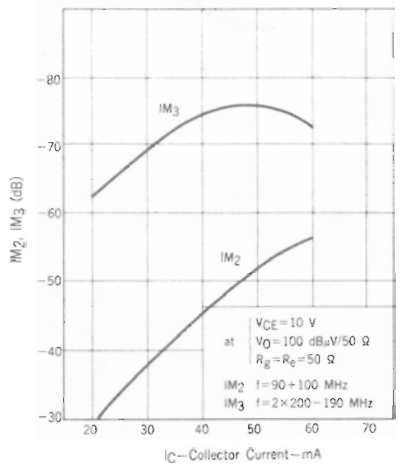
INSERTION GAIN, MAXIMUM GAIN vs. FREQUENCY



NOISE FIGURE vs. COLLECTOR CURRENT



INTERMODULATION DISTORTION vs. COLLECTOR CURRENT



S-PARAMETER

V_{CE}=10 V, I_C=20 mA, Z_O=50 Ω

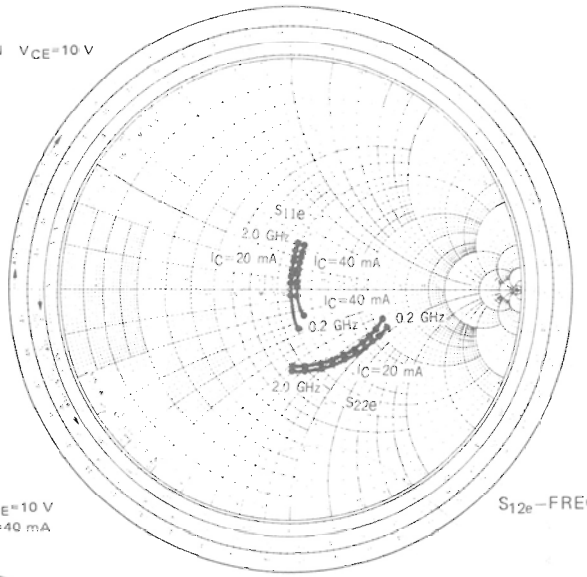
f (MHz)	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{22}\|$	$\angle S_{22}$
200	0.173	−80.3	13.652	103.4	0.041	73.8	0.453	−21.8
400	0.054	−77.0	7.217	85.1	0.066	71.2	0.427	−26.0
600	0.013	−57.9	4.936	74.0	0.113	69.3	0.428	−30.8
800	0.028	81.8	3.761	62.3	0.144	67.0	0.414	−37.2
1000	0.062	82.2	3.094	58.3	0.183	64.7	0.392	−43.2
1200	0.091	80.7	2.728	52.9	0.215	61.7	0.377	−51.4
1400	0.121	80.2	2.321	44.9	0.240	58.7	0.359	−58.3
1600	0.148	80.1	2.183	36.4	0.288	50.7	0.354	−67.2
1800	0.171	80.0	1.892	30.2	0.305	46.8	0.345	−80.0
2000	0.207	79.9	1.814	21.4	0.344	39.1	0.344	−90.4

V_{CE}=10 V, I_C=40 mA, Z_O=50 Ω

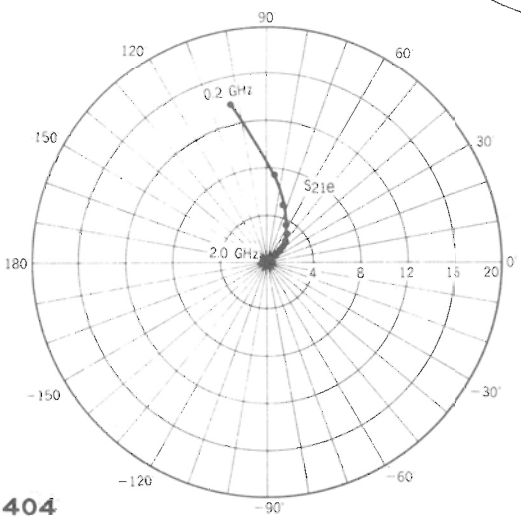
f (MHz)	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{22}\|$	$\angle S_{22}$
200	0.011	−60.1	13.76	105.4	0.040	−73.3	0.421	−17.5
400	0.028	−42.9	7.338	82.9	0.069	66.7	0.416	−22.8
600	0.027	25.1	4.996	72.7	0.114	69.4	0.414	−28.7
800	0.043	65.7	3.801	61.9	0.144	67.8	0.406	−35.7
1000	0.074	75.1	3.134	57.6	0.183	63.4	0.386	−41.8
1200	0.098	75.6	2.759	52.4	0.221	62.1	0.373	−49.8
1400	0.120	74.1	2.351	44.4	0.247	55.7	0.356	−56.3
1600	0.146	75.8	2.203	36.0	0.291	49.6	0.347	−66.6
1800	0.171	77.2	1.910	29.9	0.299	46.0	0.342	−78.8
2000	0.205	78.0	1.825	21.3	0.344	39.4	0.335	−89.6

S-PARAMETER

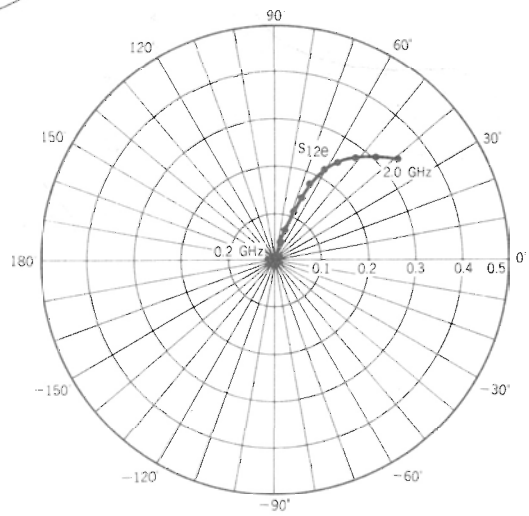
S_{11e}, S_{22e}—FREQUENCY CONDITION V_{CE}=10 V



S_{21e}—FREQUENCY CONDITION V_{CE}=10 V, I_C=40 mA



S_{12e}—FREQUENCY CONDITION V_{CE}=10 V, I_C=40 mA



NEC
ELECTRON DEVICE

SILICON TRANSISTOR
2SC3358

DESCRIPTION

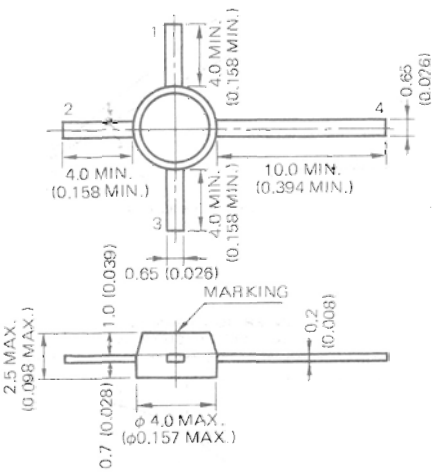
The 2SC3358 is an NPN silicon epitaxial transistor designed for low noise amplifier at VHF, UHF and CATV band.
It has large dynamic range and good current characteristic.

FEATURES

- Low Noise and High Gain
  NF=1.1 dB TYP., G_a=12 dB TYP. @V_{CE}=10 V, I_C=7 mA, f=1.0 GHz
- High Power Gain
  MAG=15 dB TYP. @V_{CE}=10 V, I_C=20 mA, f=1.0 GHz

PACKAGE DIMENSIONS

in millimeters (inches)



1. Emitter
2. Base
3. Emitter
4. Collector

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . –65 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	20 V
V_{CEO}	Collector to Emitter Voltage	12 V
V_{EBO}	Emitter to Base Voltage	3.0 V
I_C	Collector Current	100 mA

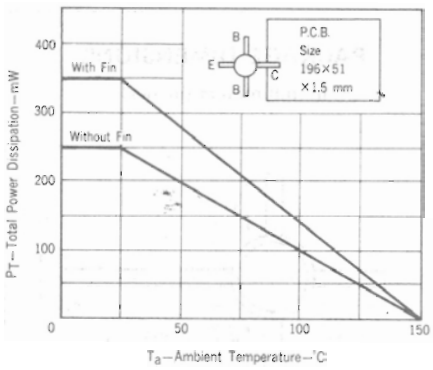
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB}=10 V, I_E=0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB}=1.0 V, I_C=0
h_{FE}	DC Current Gain	50	120	300		V_{CE}=10 V, I_C=20 mA
f_T	Gain Bandwidth Product		7		GHz	V_{CE}=10 V, I_C=20 mA
C_{ob}*	Output Capacitance		0.5	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$\|S_{21e}\|^2$	Insertion Power Gain		13		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
NF	Noise Figure		1.1	2.0	dB	V_{CE}=10 V, I_C=7 mA, f=1.0 GHz

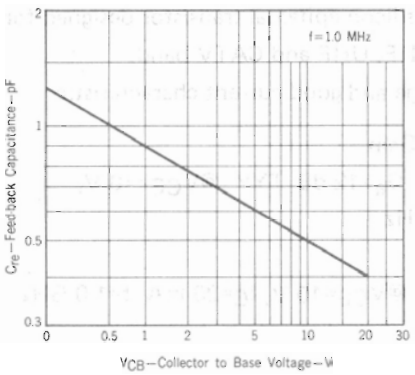
* The emitter terminal should be connected to the gurad terminal of the three-terminal capacitance bridge.

TYPICAL CHARACTERISTICS (T_a=25 °C)

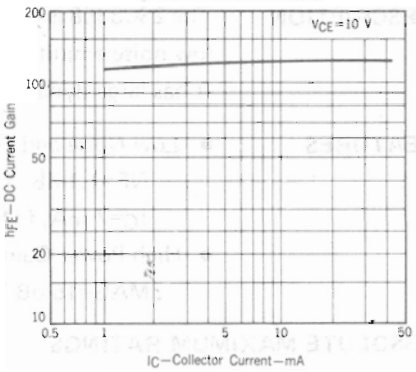
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



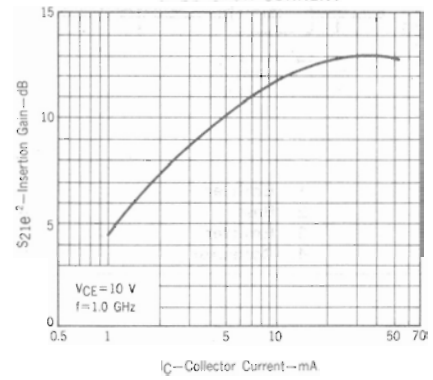
FEED-BACK CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



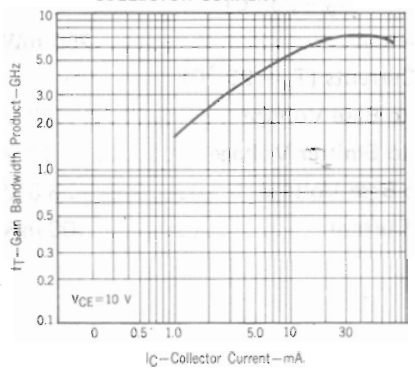
DC CURRENT GAIN vs. COLLECTOR CURRENT



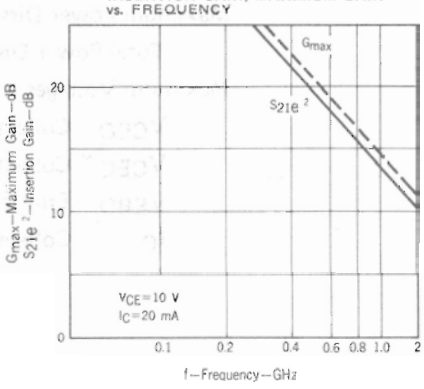
INSERTION GAIN vs. COLLECTOR CURRENT



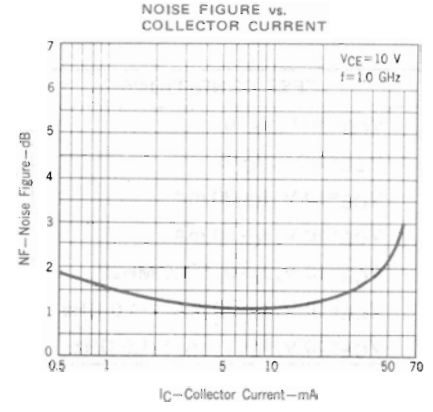
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



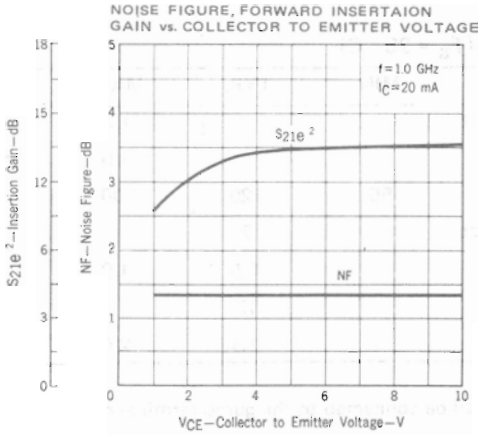
INSERTION GAIN, MAXIMUM GAIN vs. FREQUENCY



NOISE FIGURE vs. COLLECTOR CURRENT



NOISE FIGURE, FORWARD INSERTAION GAIN vs. COLLECTOR TO EMITTER VOLTAGE



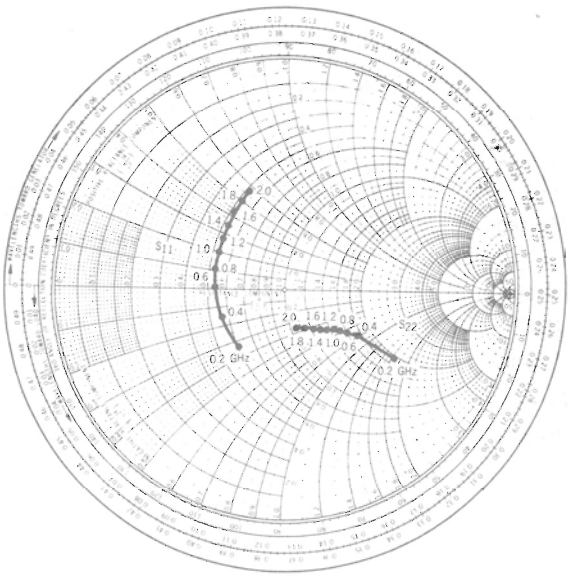
S-PARAMETER

V_{CE}=10 V, I_C=20 mA, Z_O=50 Ω

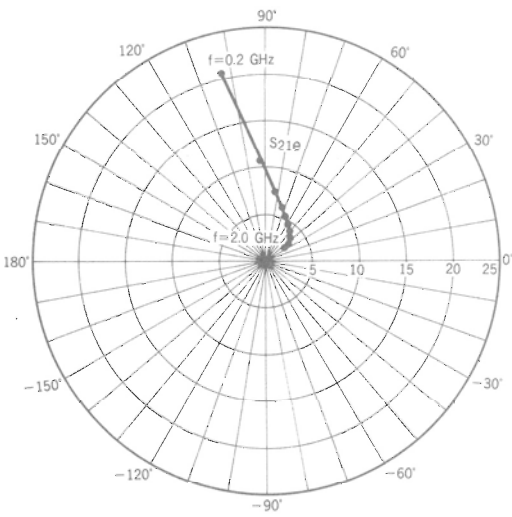
f (MHz)	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{22}\|$	$\angle S_{22}$
200	0.312	−126.3	21.352	103.3	0.015	55.6	0.567	−30.6
400	0.245	−156.8	10.660	91.3	0.040	54.0	0.374	−31.0
600	0.304	179.7	7.256	82.4	0.057	59.4	0.333	−33.2
800	0.317	162.8	5.574	74.3	0.075	57.2	0.310	−32.9
1000	0.332	149.3	5.143	64.8	0.099	56.3	0.284	−35.0
1200	0.353	139.4	3.831	59.5	0.110	55.6	0.260	−41.7
1400	0.379	130.3	3.203	52.0	0.133	54.0	0.230	−41.2
1600	0.409	123.0	2.895	43.9	0.153	49.6	0.207	−50.9
1800	0.443	117.0	2.442	38.8	0.165	48.2	0.185	−63.9
2000	0.473	111.0	2.255	30.3	0.182	40.6	0.173	−72.3

S-PARAMETER

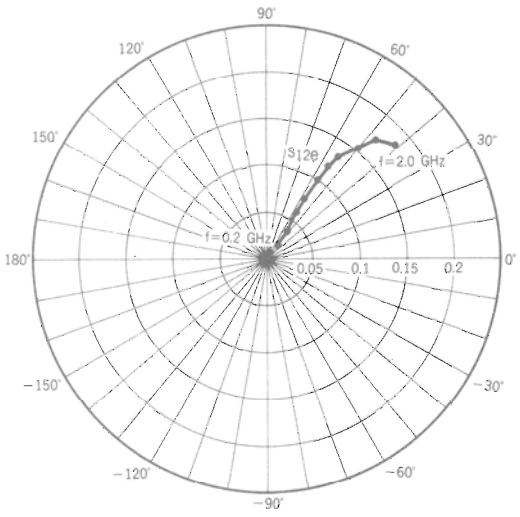
S_{11e}, S_{22e}—FREQUENCY CONDITION V_{CE}=10 V, I_C=20 mA



S_{21e}—FREQUENCY CONDITION V_{CE}=10 V, I_C=20 mA



S_{12e}—FREQUENCY CONDITION V_{CE}=10 V, I_C=20 mA



NEC
ELECTRON DEVICE

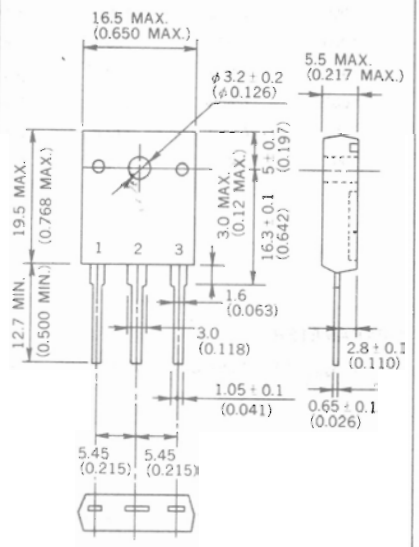
NPN SILICON POWER TRANSISTOR
2SC3434

DESCRIPTION The 2SC3434 is designed for ultra high speed, high voltage, high current switching.
This is suitable for switching regulators and high frequency applications.

FEATURES

- High Switching Speed $t_f < 0.3\ \mu s$, $t_{stg} < 1.5\ \mu s$
- Wide Reverse Bias Safe Operating Area
  $V_{CEX(SUS)1} > 450$ V @$I_C = 5$ A

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_C = 25$ °C)

- Total Power Dissipation . . . . . 100 W

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage . . .	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	10	A
$I_{C(pulse)}$	Collector Current (pulse)*	20	A
$I_{B(DC)}$	Base Current (DC)	5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

NEW DEVICE

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-On Time		0.2	0.5	μs	I_C = 5 A, I_{B1} = $-I_{B2}$ = 1 A, R_L = 30 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time		1.1	1.5	μs	
t_f	Fall Time		0.1	0.3	μs	
h_{FE1}*	DC Current Gain	10		60	—	V_{CE} = 5 V, I_C = 1 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5 V, I_C = 2 A
h_{FE3}*	DC Current Gain	10			—	V_{CE} = 5 V, I_C = 5 A
$V_{CE(sat)}$*	Collector Saturation Voltage		0.75	1.0	V	I_C = 5 A, I_B = 1 A
$V_{BE(sat)}$*	Base Saturation Voltage		1.1	1.5	V	I_C = 5 A, I_B = 1 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 5 A, I_B = 1 A, L = 500 μH, Clamped
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 5 A, 2·I_{B1} = $-I_{B2}$ = 2 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 10 A, I_{B1} = 2 A, $-I_{B2}$ = 4 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2	mA	V_{CE} = 500 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 500 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2	mA	V_{CE} = 500 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5 V, I_C = 0
f_T	Gain Band Width Product		30		MHz	V_{CE} = 10 V, I_C = 1 A
C_{ob}	Output Capacitance		120		pF	V_{CB} = 10 V, f = 1.0 MHz

* Pulsed : PW ≦ 350 μs, Duty Cycle ≦ 2 %

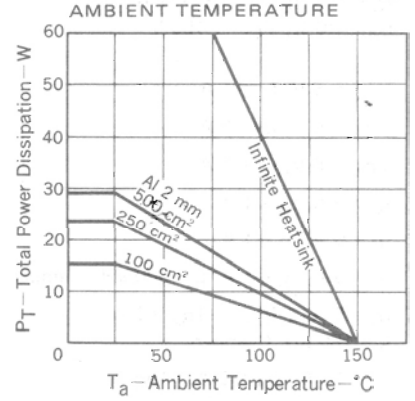
Classification of h_{FE1}

Rank	M	L	K
Range	10 to 30	20 to 40	30 to 60

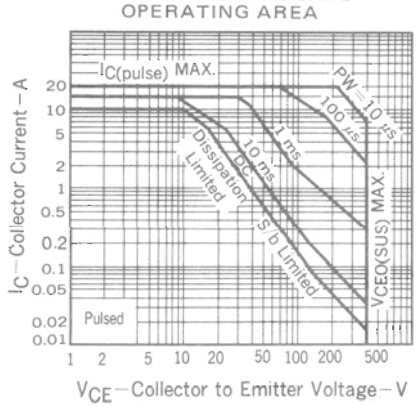
Test Conditions: V_{CE} = 5 V, I_C = 1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

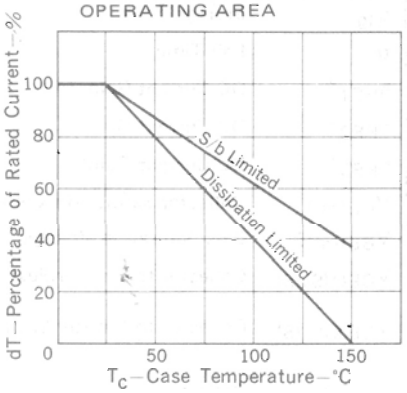
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



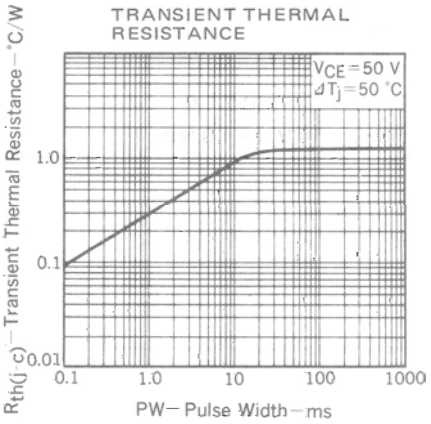
FORWARD BIAS SAFE OPERATING AREA



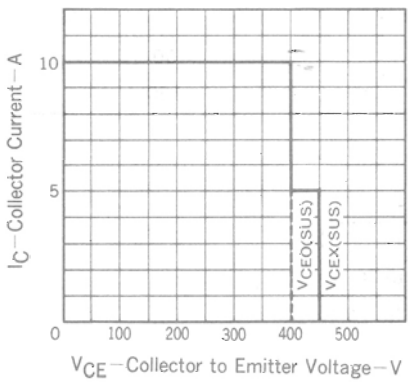
DERATING CURVE OF SAFE OPERATING AREA



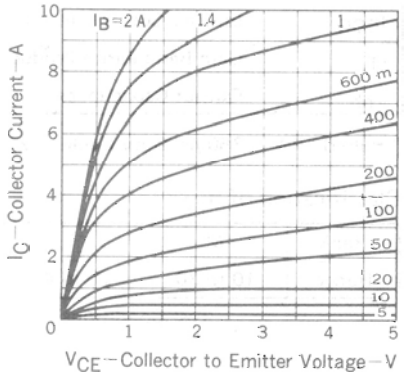
TRANSIENT THERMAL RESISTANCE



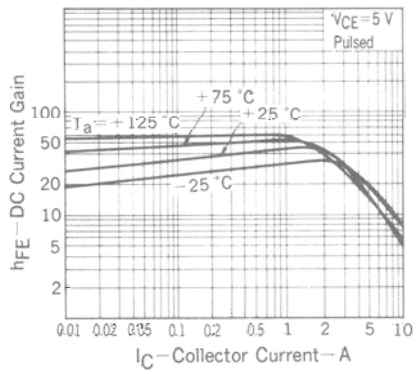
REVERSE BIAS SAFE OPERATING AREA



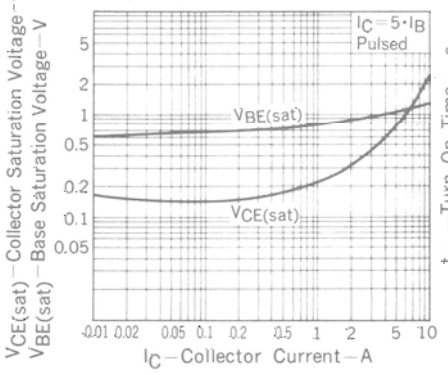
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN-ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

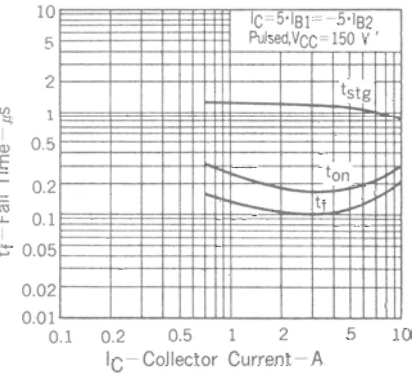
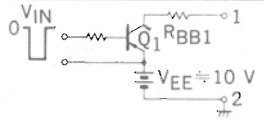
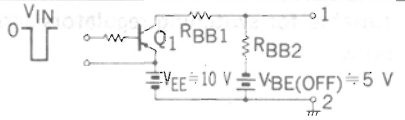
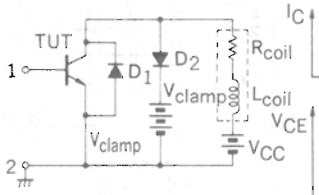
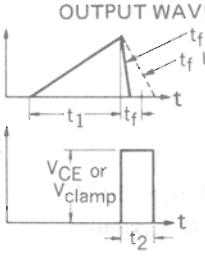
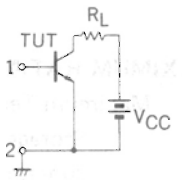


TABLE 1. — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	V_{CEO} (SUS)	V_{CEX} (SUS)	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 5 A	 PW Varied to Attain I_C = 5 A Duty Cycle ≦ 2 % Q_1 = 2SA959	
CIRCUIT VALUES	L_{coil} = 100 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω V_{clamp} = $V_{CEO(SUS)}$ Value	L_{coil} = 180 μH, V_{CC} = 20 V R_{coil} = 0.05 Ω V_{clamp} = $V_{CEX(SUS)}$ Value	R_L = 25 Ω, V_{CC} = 150 V PW ≒ 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  D_1 = F114F D_2 = 6FH4S	OUTPUT WAVEFORM  $t_1 = \frac{L_{coil}\ (I_{C\ pk})}{V_{CC}}$ $t_2 = \frac{L_{coil}\ (I_{C\ pk})}{V_{clamp}}$	RESISTIVE TEST CIRCUIT 

NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC3435

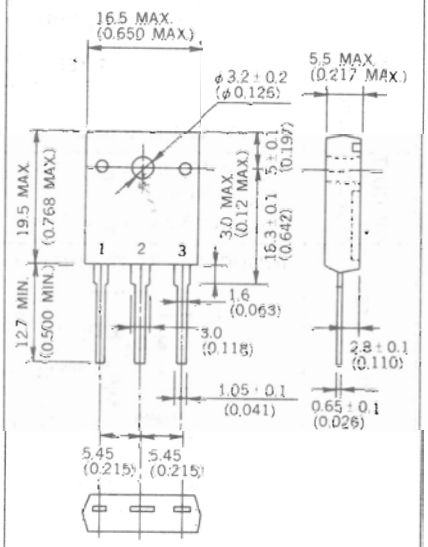
NEW DEVICE

DESCRIPTION The 2SC3435 is designed for ultra high speed, high voltage, high current switching.
This is suitable for switching regulators and high frequency applications.

FEATURES

- High Switching Speed $t_f < 0.3\ \mu s$
- Wide Reverse Safe Operating Area
  $V_{CEX(SUS)1} > 450$ V @$I_C = 8$ A

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_C = 25$ °C)

- Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage . . .	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	15	A
$I_{C(pulse)}$	Collector Current (pulse)*	30	A
$I_{B(DC)}$	Base Current (DC)	7.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = 7.5 A, I_{B1} = −I_{B2} = 1.5 A, R_L = 20 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	10		60	—	V_{CE} = 5 V, I_C = 1.5 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5 V, I_C = 3 A
h_{FE3}*	DC Current Gain	7			—	V_{CE} = 5 V, I_C = 7.5 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 7.5 A, I_B = 1.5 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.5	V	I_C = 7.5 A, I_B = 1.5 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 10 A, I_B = 2 A, L = 500 μH, Clamped
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 8 A, I_{B1} = 2 A, −I_{B2} = 1.5 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	425			V	I_C = 8 A, I_{B1} = 2 A, −I_{B2} = 1.5 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2	mA	V_{CE} = 500 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 500 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2	mA	V_{CE} = 500 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5 V, I_C = 0
f_T	Gain Bandwidth Product		30		MHz	V_{CE} = 10 V, I_C = 1.5 A
C_{ob}	Output Capacitance		170		pF	V_{CB} = 10 V, f = 1 MHz

* Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

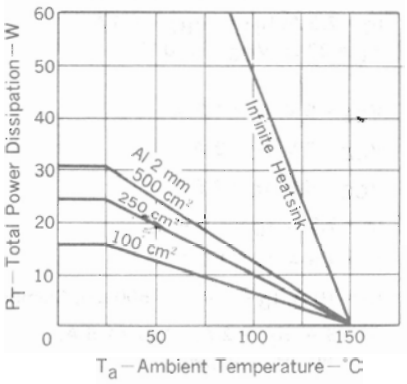
Classification of h_{FE1}

Rank	M	L	K
Range	10 to 30	20 to 40	30 to 60

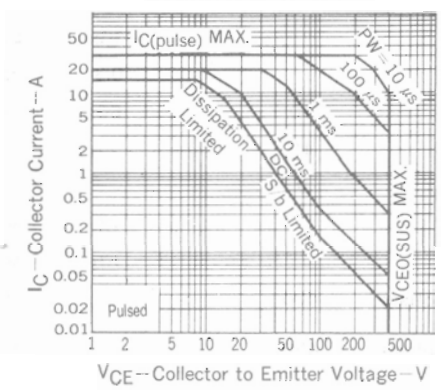
Test Conditions: V_{CE} = 5 V, I_C = 1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

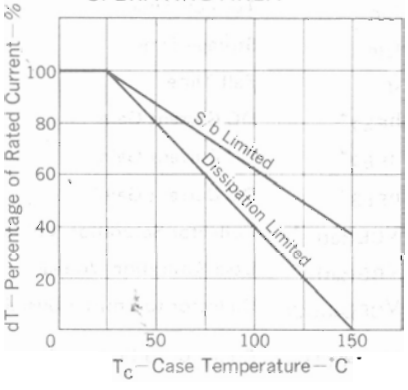
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



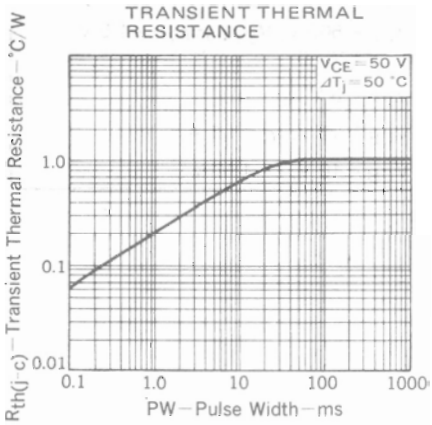
FORWARD BIAS SAFE OPERATING AREA



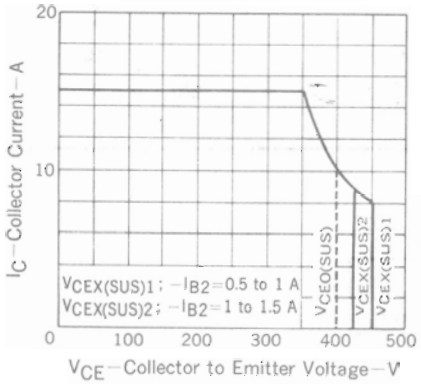
DERATING CURVE OF SAFE OPERATING AREA



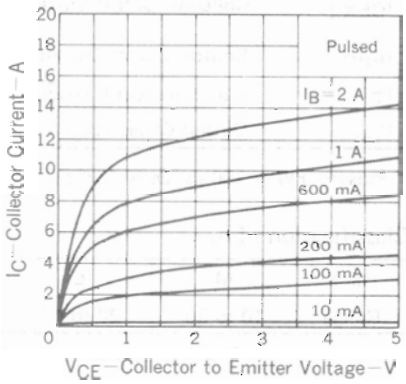
TRANSIENT THERMAL RESISTANCE



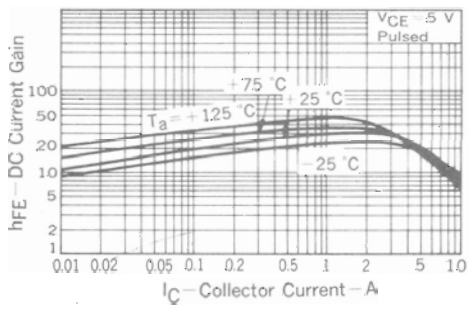
REVERSE BIAS SAFE OPERATING AREA



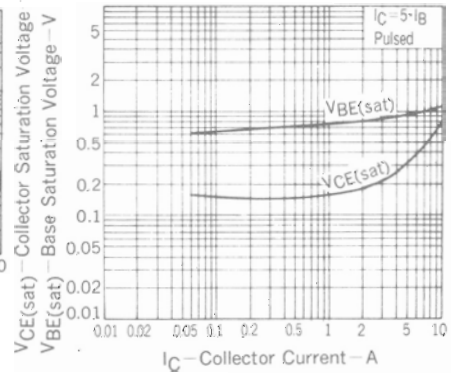
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT

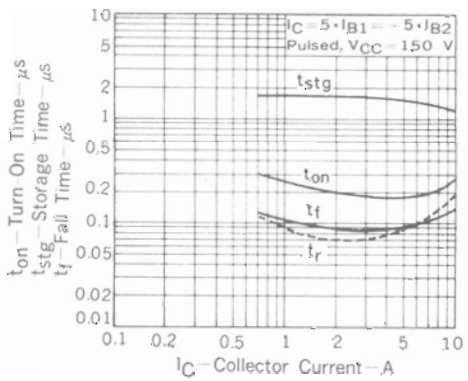
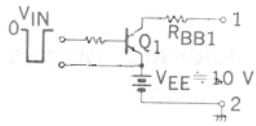
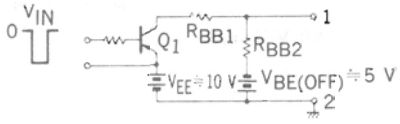
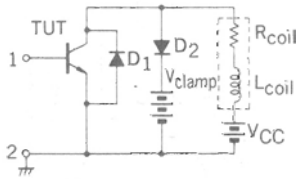
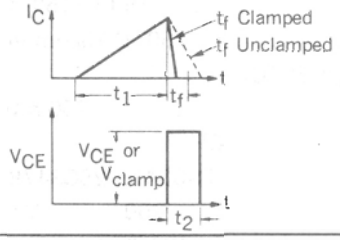
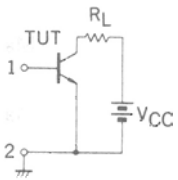


TABLE 1. — TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(SUS)}$	$V_{CEX(SUS)}$	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 10 A	 PW Varied to Attain I_C = 8 A Duty Cycle ≦ 2 % Q_1 = 2SA959	
CIRCUIT VALUES	L_{coil} = 50 μH, V_{CC} = 10 V R_{coil} = 0.05 Ω V_{clamp} = $V_{CEO(SUS)}$ Value	L_{coil} = 180 μH, V_{CC} = 20 V R_{coil} = 0.05 Ω V_{clamp} = $V_{CEX(SUS)}$ Value	R_L = 15 Ω, V_{CC} ≒ 150 V PW ≒ 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  D_1 = F114F D_2 = 6FH4S	OUTPUT WAVEFORM  t_1 Adjust to Obtain I_C $t_1 = \frac{L_{coil}(I_{C\,pk})}{V_{CC}}$ $t_2 = \frac{L_{coil}(I_{C\,pk})}{V_{clamp}}$	RESISTIVE TEST CIRCUIT 

NEC
ELECTRON DEVICE

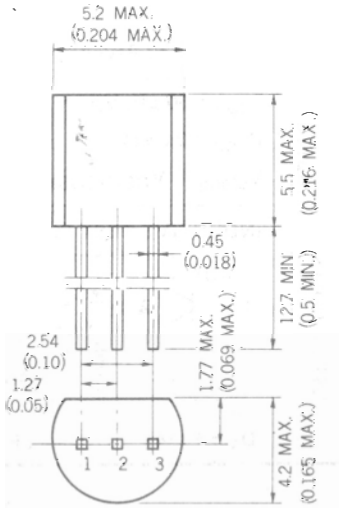
NPN SILICON TRANSISTORS
2SC3478, 2SC3478A

DESCRIPTION The 2SC3478/3478A is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Breakdown Voltage.
  V_{CEO} = 180 V/200 V (2SC3478/2SC3478A)
- Good h_{FE} linearity.
- A complementary pair with 2SA1376/2SA1376A.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 750 mW

Maximum Voltages and Currents (T_a = 25 °C)

		2SC3478/2SC3478A	
V_{CBO}	Collector to Base Voltage	200	V
V_{CEO}	Collector to Emitter Voltage . .	180/200	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current (DC)	100	mA
I_C	Collector Current (pulse)*	200	mA
I_B	Base Current (DC)	20	mA

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

2SC3478/2SC3478A

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	135		400/600	–	V_{CE} = 10 V, I_C = 10 mA
t_{on}	Turn-on Time		0.15		μs	I_C = 10 mA
t_{off}	Turn-off Time		1.6		μs	I_{B1} = −I_{B2} = 1 mA, V_{CC} = 10 V
f_T	Gain Bandwidth Product	100	150		MHz	V_{CE} = 10 V, I_E = −10 mA
C_{ob}	Output Capacitance		2.6	3.5	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 4.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600	660	700	mV	V_{CE} = 10 V, I_C = 10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.3	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.8	1.2	V	I_C = 50 mA, I_B = 5.0 mA

Classification of h_{FE}

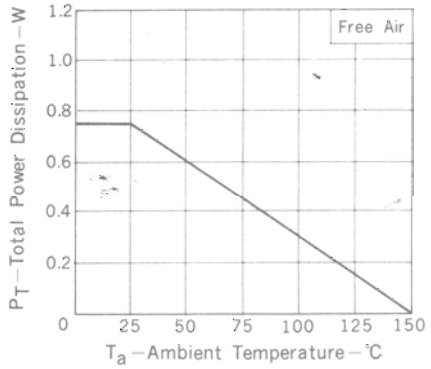
Rank	L	K	U**
Range	135 – 270	200 – 400	300 – 600

Test Conditions: V_{CE} = 10 V, I_C = 10 mA

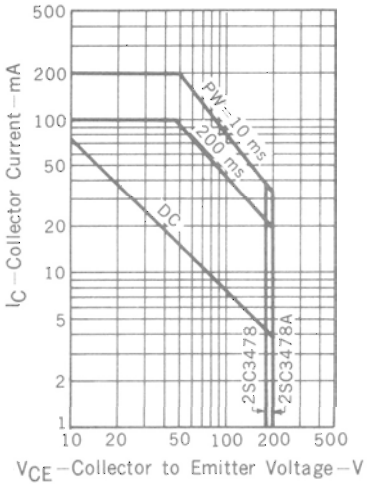
** 2SC3478A has no U rank.

TYPICAL CHARACTERISTICS (T_a = 25 °C)

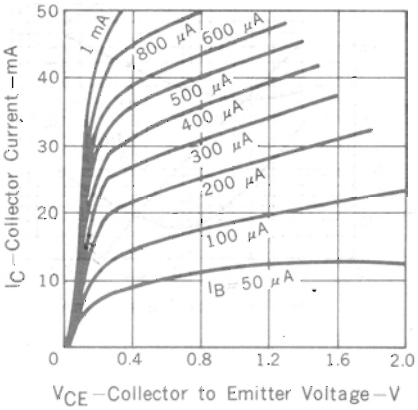
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



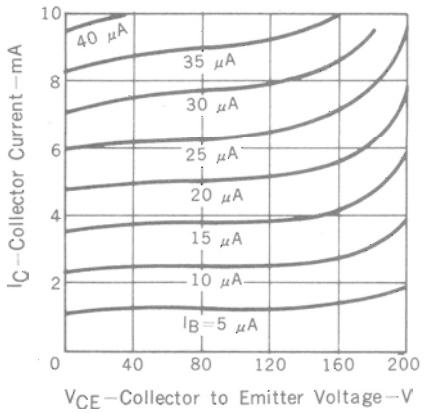
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



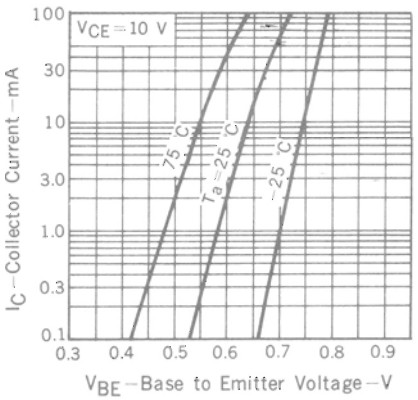
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



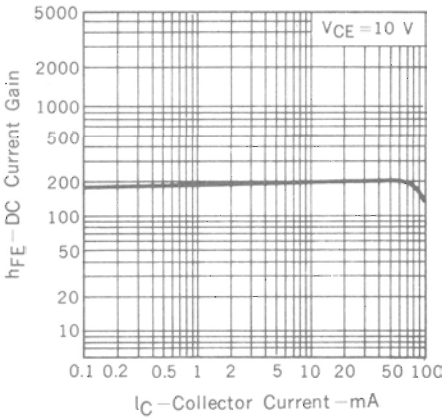
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



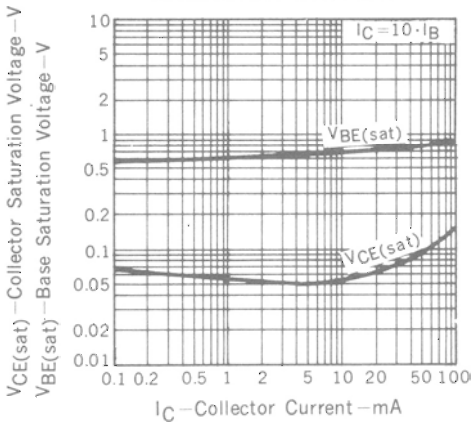
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



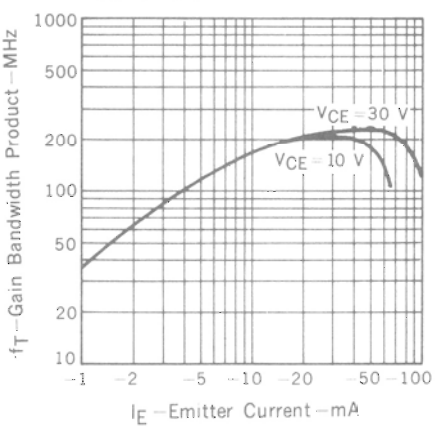
DC CURRENT GAIN vs. COLLECTOR CURRENT



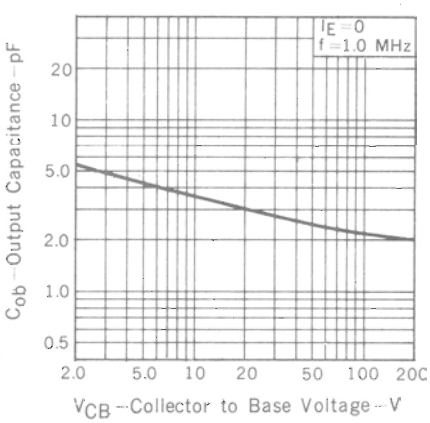
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



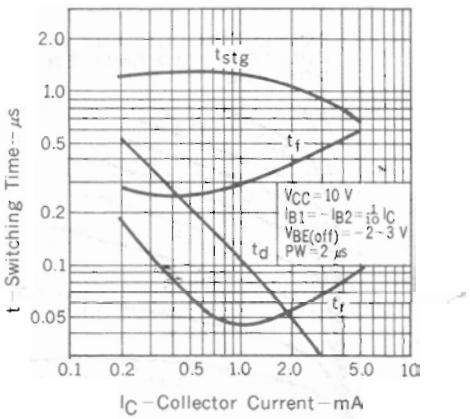
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC3531

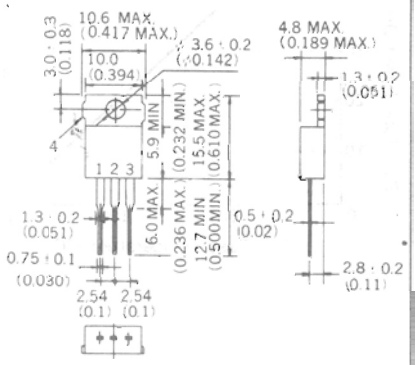
DESCRIPTION The 2SC3531 is designed for use in high speed, high voltage and high current switching.
It is suitable for switching regulators, DC-DC converters and ultrasonic appliance applications.

FEATURES

- High speed switching.
- Wide reverse S.O.A.

  $V_{CEX(SUS)}$: 800 V MIN.

PACAKGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 50 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	1 000	V
V_{CEO}	Collector to Emitter Voltage . . .	800	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	3.0	A
$I_{C(pulse)}$	Collector Current (Pulse)*	6.0	A
$I_{B(DC)}$	Base Current (DC)	1.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

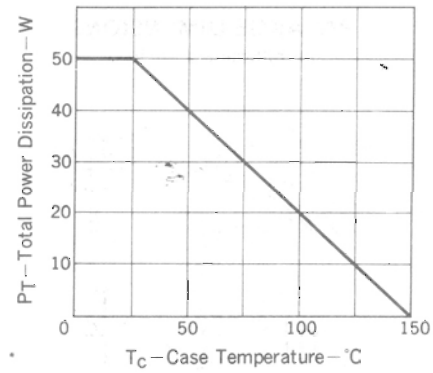
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn On Time			1.0	μs	I_C = 2.0 A, 2·I_{B1} = −I_{B2} = 0.8 A R_L = 150 Ω, V_{CC} ≒ 300 V
t_{stg}	Storage Time			3.0	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}**	DC Current Gain	10		30	—	V_{CE} = 5.0 V, I_C = 0.2 A
h_{FE2}**	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 0.4 A
h_{FE3}**	DC Current Gain	7			—	V_{CE} = 5.0 V, I_C = 1.0 A
$V_{CE(sat)}$**	Collector Saturation Voltage			1.0	V	I_C = 1.5 A, I_B = 0.3 A
$V_{BE(sat)}$**	Base Saturation Voltage			1.5	V	I_C = 1.5 A, I_B = 0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	800			V	I_C = 1.5 A, I_B = 0.3 A, L = 500 μH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	1 000			V	I_C = 1.5 A, 2·I_{B1} = −I_{B2} = 0.6 A, T_a = 125 °C, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 800 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

**Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

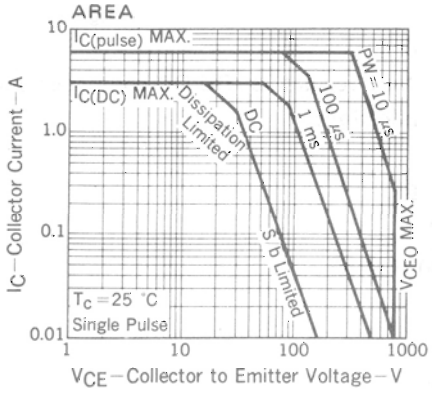
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

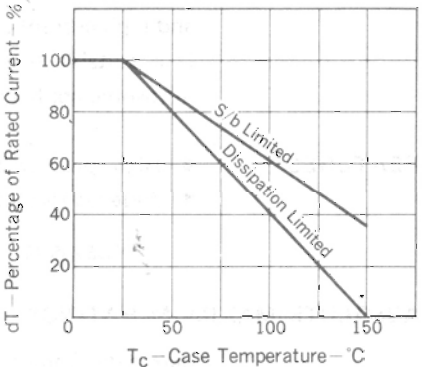
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



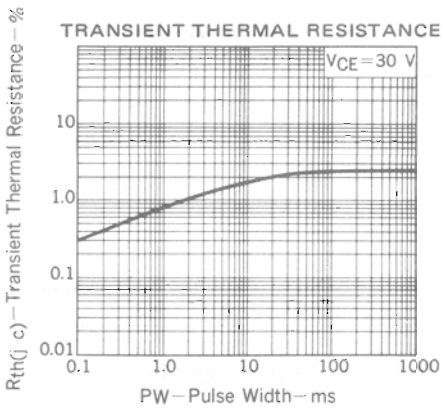
FORWARD BIAS SAFE OPERATING AREA



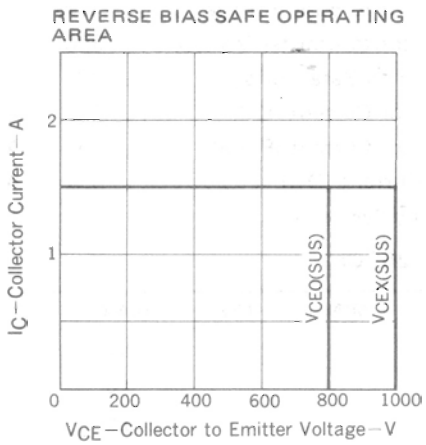
DERATING CURVE OF FORWARD BIAS SAFE OPERATING AREA



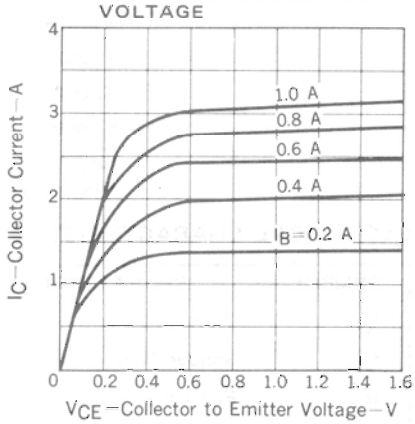
TRANSIENT THERMAL RESISTANCE



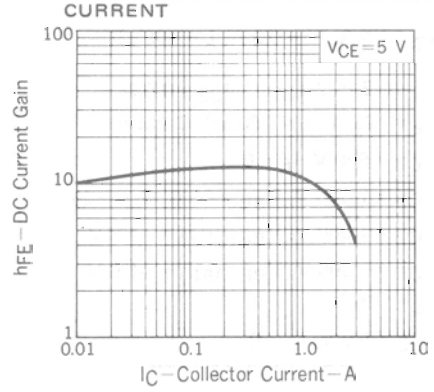
REVERSE BIAS SAFE OPERATING AREA



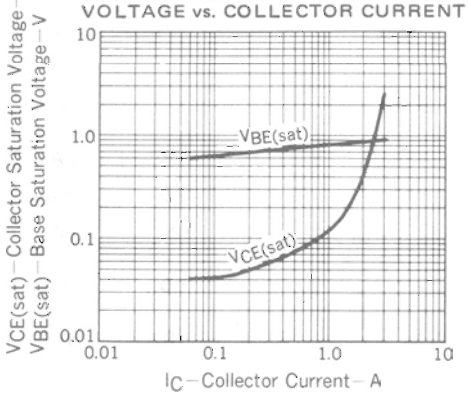
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



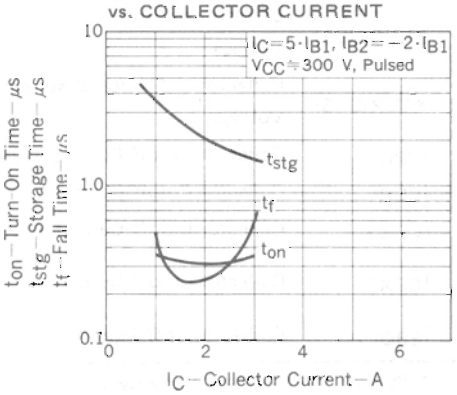
DC CURRENT GAIN vs. COLLECTOR CURRENT



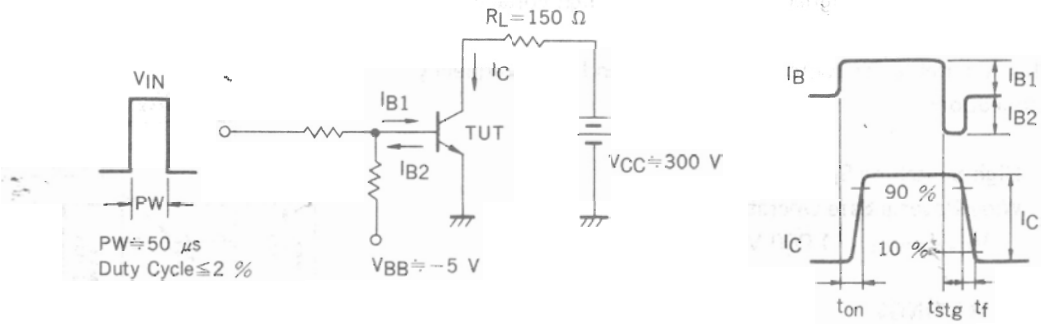
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC3533

NEW DEVICE

DESCRIPTION The 2SC3533 is designed for high speed, high voltage, high current switching.
This is suitable for switching regulators and high frequency applications.

FEATURES

- High Switching Speed
- Wide Reverse Safe Operating Area
  $V_{CEX(SUS)} \geqq 1\,000$ V @I_C = 1.5 A

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

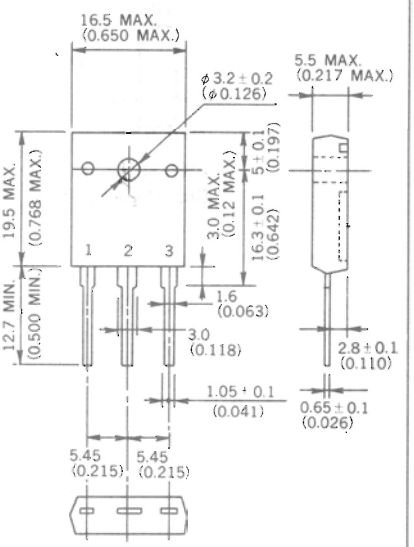
Total Power Dissipation . . . . . 70 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	1000	V
V_{CEO}	Collector to Emitter Voltage . . .	800	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	3	A
$I_{C(pulse)}$	Collector Current (pulse)*	6	A
$I_{B(DC)}$	Base Current (DC)	1.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

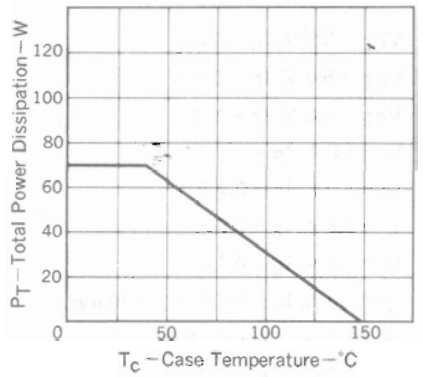
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 2 A, I_{B1} = −I_{B2} = 0.8 A, R_L = 150 Ω, V_{CC} ≒ 300 V
t_{stg}	Storage Time			3.0	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}*	DC Current Gain	10		30	—	V_{CE} = 5.0 V, I_C = 0.2 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 0.4 A
h_{FE3}*	DC Current Gain	7			—	V_{CE} = 5.0 V, I_C = 1 A
$V_{CE(sat)1}$*	Collector Saturation Voltage			0.8	V	I_C = 1.0 A, I_B = 0.2 A
$V_{BE(sat)1}$*	Base Saturation Voltage			1.5	V	I_C = 1.0 A, I_B = 0.2 A
$V_{CE(sat)2}$*	Collector Saturation Voltage			1.0	V	I_C = 1.5 A, I_B = 0.3 A
$V_{BE(sat)2}$*	Base Saturation Voltage			1.5	V	I_C = 1.5 A, I_B = 0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	800			V	I_C = 1.5 A, I_B = 0.3 A, L = 500 μH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	1000			V	I_C = 1.5 A, 2·I_{B1} = −I_{B2} = 0.6 A, L = 180 μH, T_a = 125 °C, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 800 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

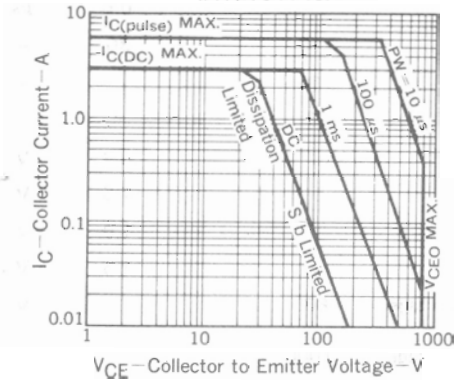
* Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

TYPICAL CHARACTERISTICS (T_a = 25 °C)

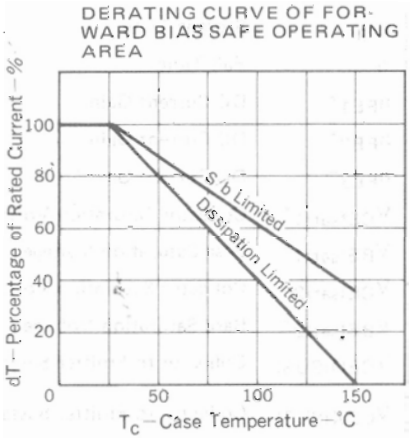
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



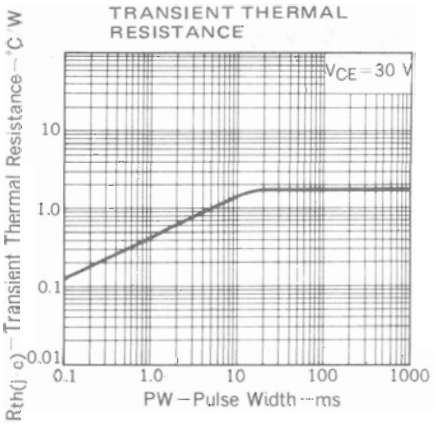
FORWARD BIAS SAFE OPERATING AREA



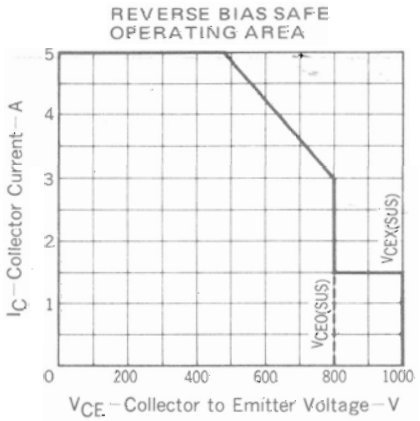
DERATING CURVE OF FORWARD BIAS SAFE OPERATING AREA



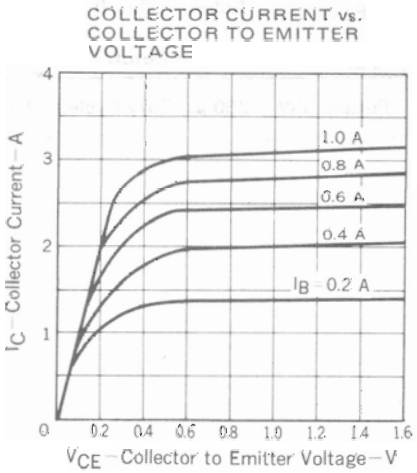
TRANSIENT THERMAL RESISTANCE



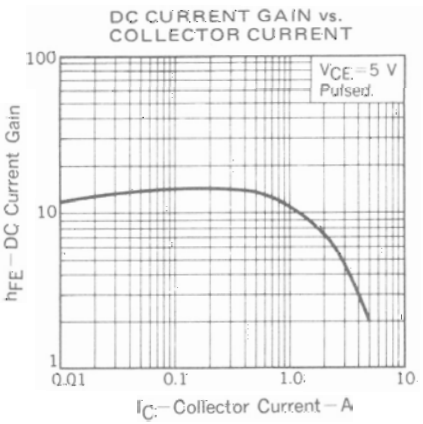
REVERSE BIAS SAFE OPERATING AREA



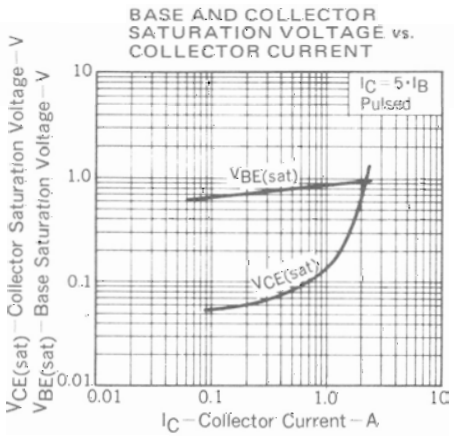
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



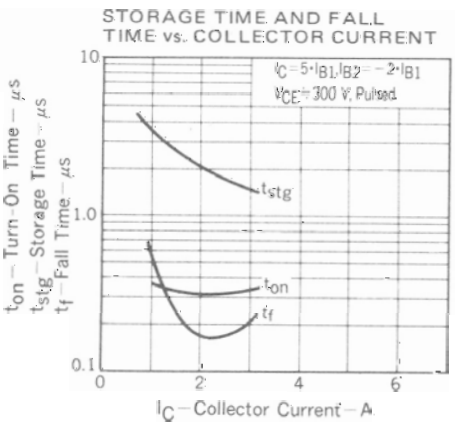
DC CURRENT GAIN vs. COLLECTOR CURRENT



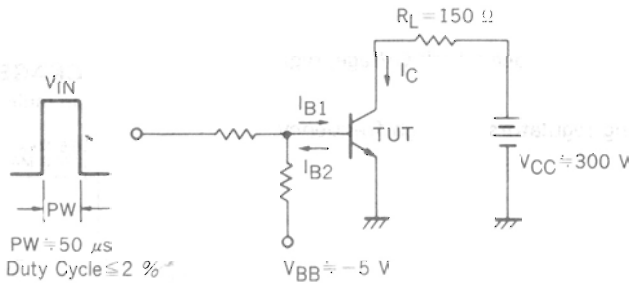
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

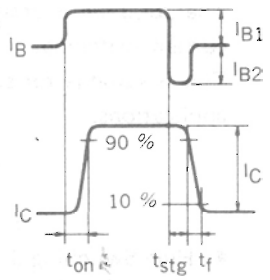


STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC3534

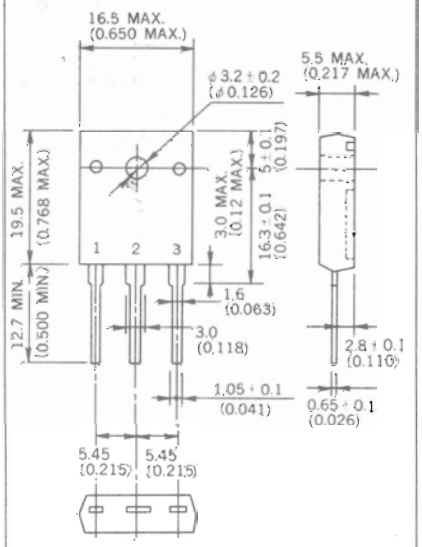
NEW DEVICE

DESCRIPTION The 2SC3534 is designed for high speed, high voltage, high current switching.
This is suitable for switching regulators and high frequency applications.

FEATURES

- High Switching Speed
- Wide Reverse Safe Operating Area
  $V_{CEX(SUS)} \geqq 1\,000$ V @$I_C = 2$ A

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_C = 25$ °C)

- Total Power Dissipation . . . . . 80 W

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{CBO}	Collector to Base Voltage	1000	V
V_{CEO}	Collector to Emitter Voltage . . .	800	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC).	4	A
$I_{C(pulse)}$	Collector Current (pulse)*.	8	A
$I_{B(DC)}$	Base Current (DC)	2	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

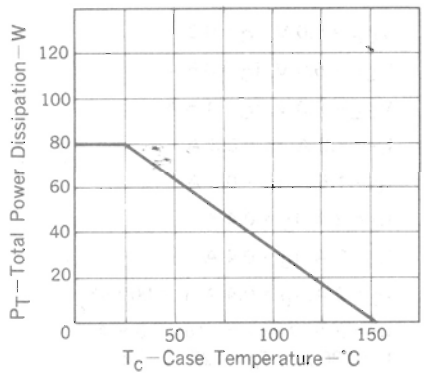
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 3 A, 2·I_{B1} = −I_{B2} = 1.2 A R_L = 100 Ω, V_{CC} ≒ 300 V
t_{stg}	Storage Time			3.0	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}*	DC Current Gain	10		30	—	V_{CE} = 5.0 V, I_C = 0.3 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 0.6 A
h_{FE3}*	DC Current Gain	7			—	V_{CE} = 5.0 V, I_C = 1.5 A
$V_{CE(sat)1}$*	Collector Saturation Voltage			0.8	V	I_C = 1.5 A, I_B = 0.3 A
$V_{BE(sat)1}$*	Base Saturation Voltage			1.5	V	I_C = 1.5 A, I_B = 0.3 A
$V_{CE(sat)2}$*	Collector Saturation Voltage			1.0	V	I_C = 2 A, I_B = 0.4 A
$V_{BE(sat)2}$*	Base Saturation Voltage			1.5	V	I_C = 2 A, I_B = 0.4 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	800			V	I_C = 2 A, I_B = 0.4 A, L = 500 μH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	1000			V	I_C = 2 A, 2·I_{B1} = −I_{B2} = 0.8 A, L = 180 μH, T_a = 125 °C, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 800 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

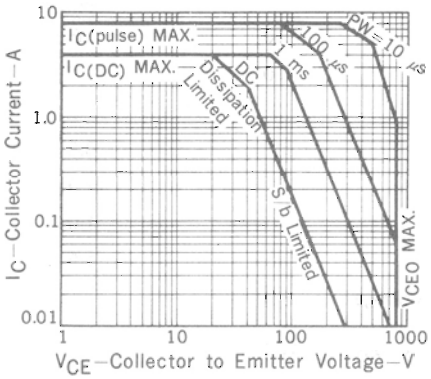
* Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

TYPICAL CHARACTERISTICS (T_a = 25 °C)

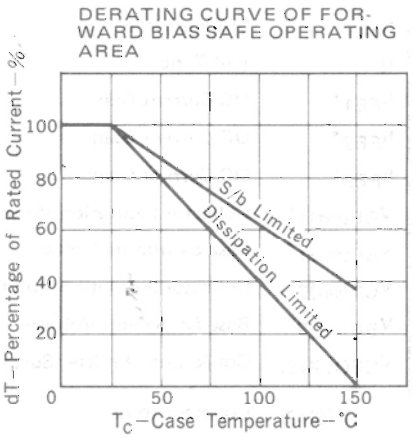
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



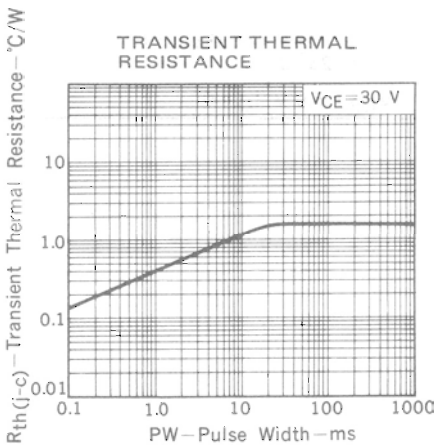
FORWARD BIAS SAFE OPERATING AREA



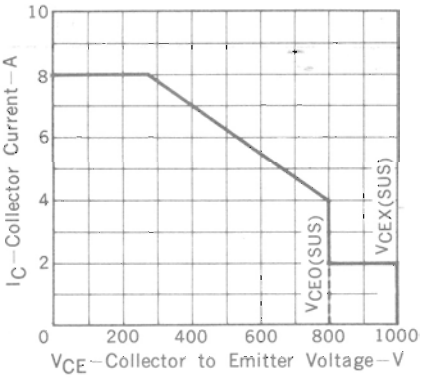
DERATING CURVE OF FORWARD BIAS SAFE OPERATING AREA



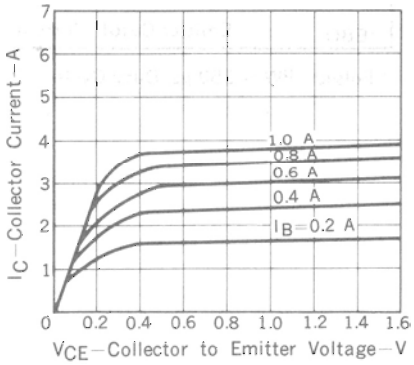
TRANSIENT THERMAL RESISTANCE



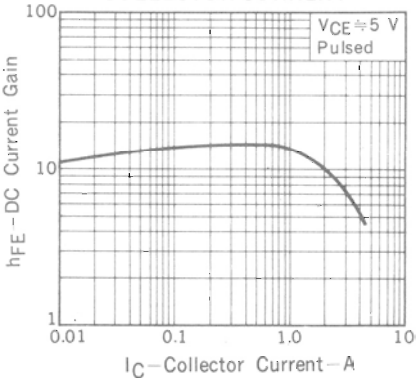
REVERSE BIAS SAFE OPERATING AREA



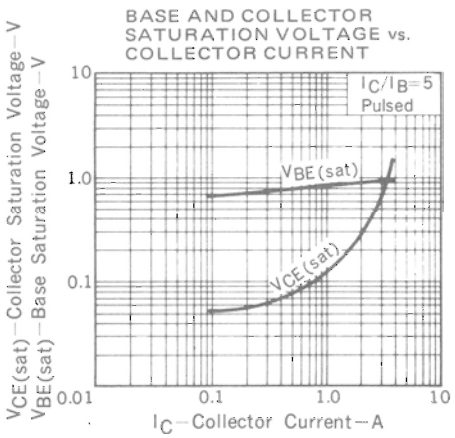
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



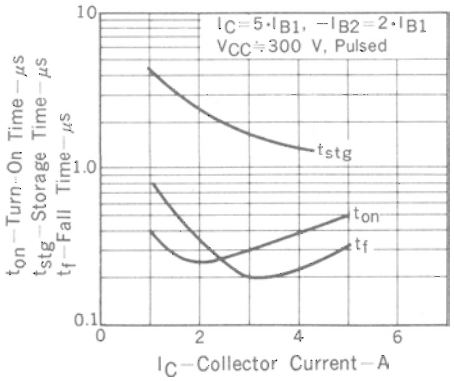
DC CURRENT GAIN vs. COLLECTOR CURRENT



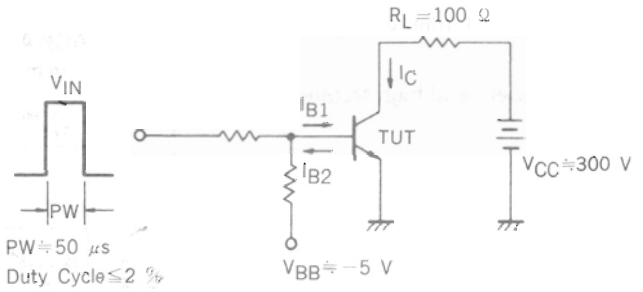
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

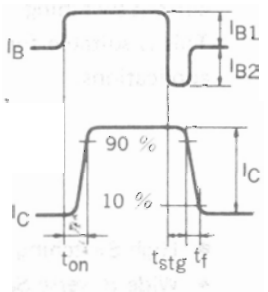


STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

NPN SILLICON POWER TRANSISTOR
2SC3535

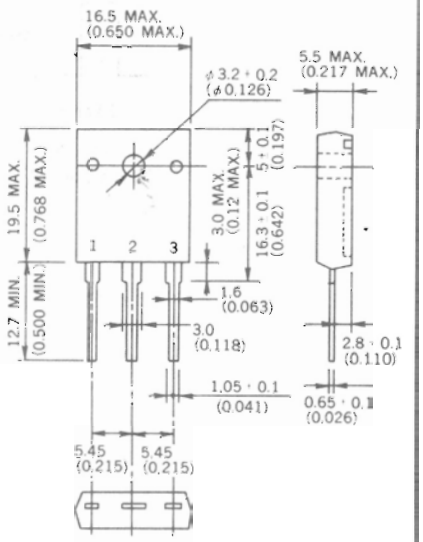
NEW DEVICE

DESCRIPTION The 2SC3535 is designed for high speed, high voltage, high current switching.
This is suitable for switching regulaters and high frequency applications.

FEATURES

- High Switching Speed
- Wide Reverse Safe Operating Area
  $V_{CEX(SUS)} \geq 1\ 000$ V @$I_C = 3$ A

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_C = 25$ °C)

Total Power Dissipation . . . . . 100 W

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{CBO}	Collector to Base Voltage	1 000	V
V_{CEO}	Collector to Emitter Voltage . . .	800	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	6	A
$I_{C(pulse)}$	Collector Current (pulse)*	12	A
$I_{B(DC)}$	Base Current (DC)	3	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

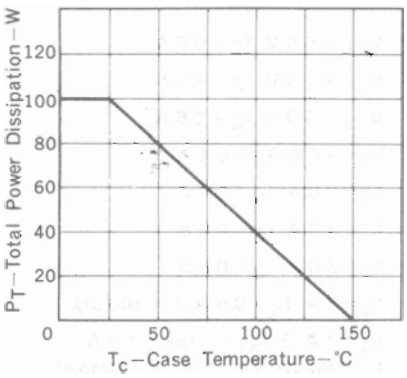
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 4 A, 2·I_{B1} = −I_{B2} = 1.6 A, R_L = 75 Ω, V_{CC} ≒ 300 V
t_{stg}	Storage Time			3.0	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}*	DC Current Gain	10		30	—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE3}*	DC Current Gain	7			—	V_{CE} = 5.0 V, I_C = 2.5 A
$V_{CE(sat)1}$*	Collector Saturation Voltage			0.8	V	I_C = 2.0 A, I_B = 0.4 A
$V_{BE(sat)1}$*	Base Saturation Voltage			1.5	V	I_C = 2.0 A, I_B = 0.4 A
$V_{CE(sat)2}$*	Collector Saturation Voltage			1.0	V	I_C = 3.0 A, I_B = 0.6 A
$V_{BE(sat)2}$*	Base Saturation Voltage			1.5	V	I_C = 3.0 A, I_B = 0.6 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	800			V	I_C = 3 A, I_B = 0.6 A, L = 500 μH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	1000			V	I_C = 3 A, 2·I_{B1} = −I_{B2} = 1.2 A, L = 180 μH, T_a = 125 °C, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 800 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

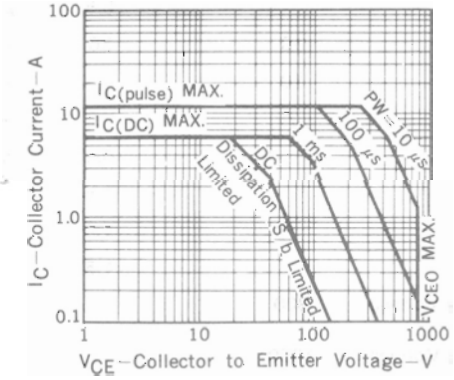
* Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

TYPICAL CHARACTERISTICS (T_a = 25 °C)

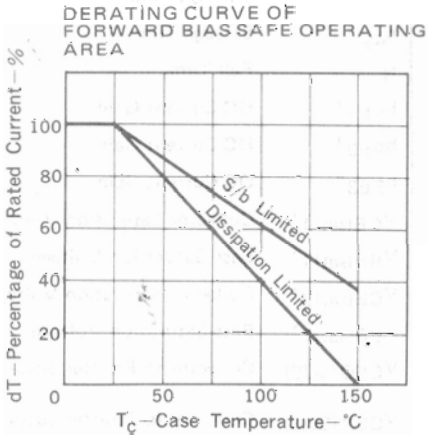
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



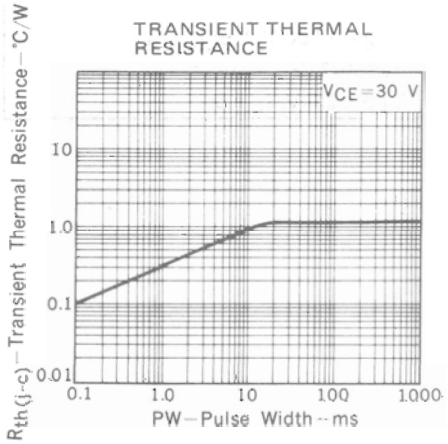
FORWARD BIAS SAFE OPERATING AREA



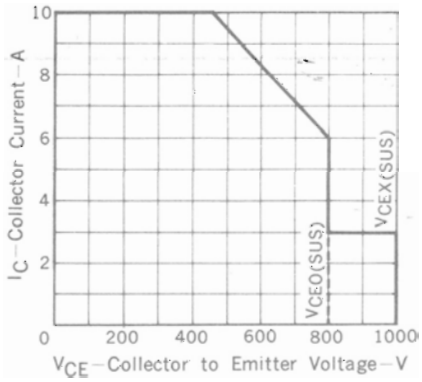
DERATING CURVE OF FORWARD BIAS SAFE OPERATING AREA



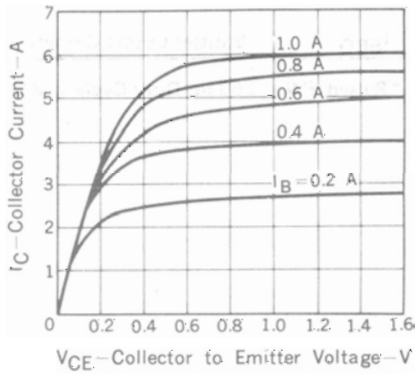
TRANSIENT THERMAL RESISTANCE



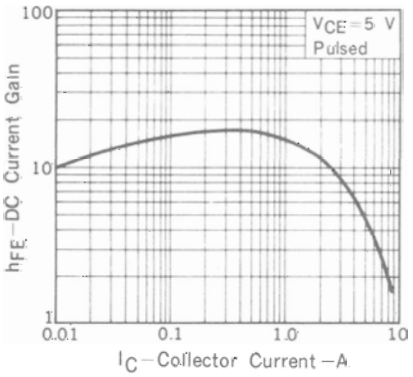
REVERSE BIAS SAFE OPERATING AREA



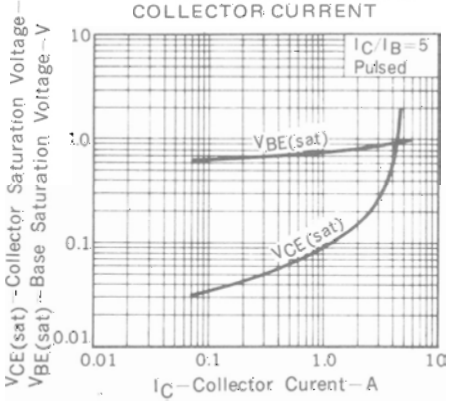
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



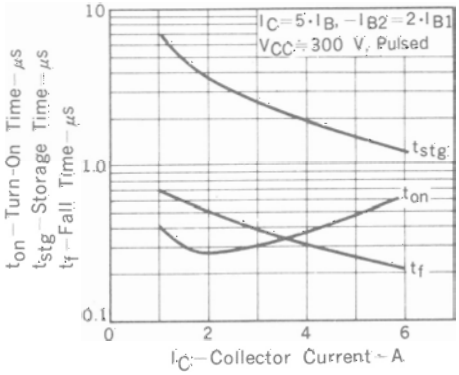
DC CURRENT GAIN vs. COLLECTOR CURRENT



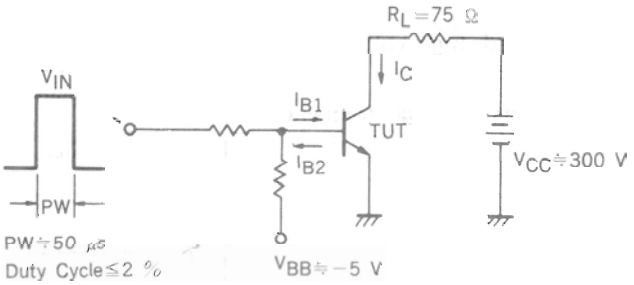
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

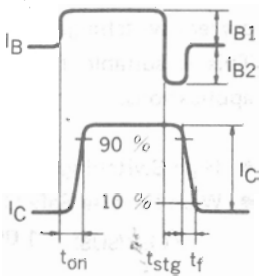


STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC3536

NEW DEVICE

DESCRIPTION The 2SC3536 is designed for high speed, high voltage, high current switching.
This is suitable for switching regulators and high frequency applications.

FEATURES

- High Switching Speed
- Wide Reverse Safe Operating Area
  $V_{CEX(SUS)} \geqq 1\,000$ V @I_C = 4 A

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

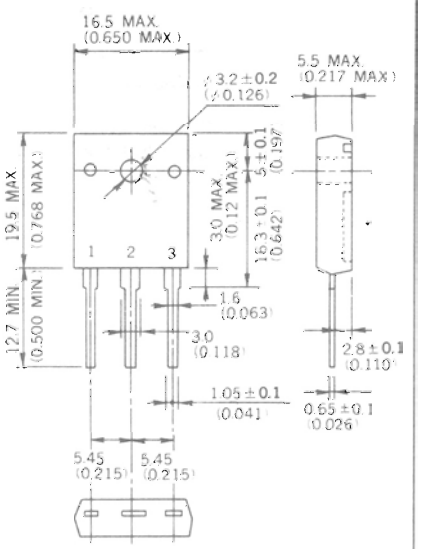
Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	1000	V
V_{CEO}	Collector to Emitter Voltage . .	800	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	8	A
$I_{C(pulse)}$	Collector Current (pulse)* . . .	16	A
$I_{B(DC)}$	Base Current (DC)	4	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

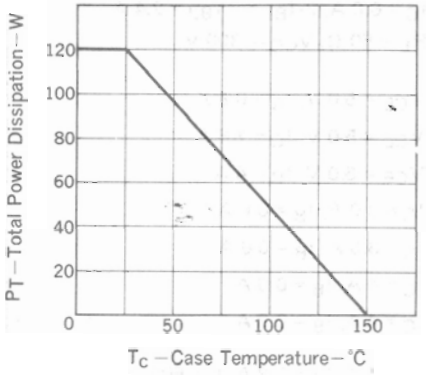
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 6.0 A, 2·I_{B1} = −I_{B2} = 2.4 A, R_L = 50 Ω, V_{CC} ≒ 300 V
t_{stg}	Storage Time			3.0	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}*	DC Current Gain	10		30	—	V_{CE} = 5.0 V, I_C = 0.8 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 1.6 A
h_{FE3}*	DC Current Gain	7			—	V_{CE} = 5.0 V, I_C = 4 A
$V_{CE(sat)1}$*	Collector Saturation Voltage			0.8	V	I_C = 3.0 A, I_B = 0.6 A
$V_{BE(sat)1}$*	Base Saturation Voltage			1.5	V	I_C = 3.0 A, I_B = 0.6 A
$V_{CE(sat)2}$*	Collector Saturation Voltage			1.0	V	I_C = 4 A, I_B = 0.8 A
$V_{BE(sat)2}$*	Base Saturation Voltage			1.5	V	I_C = 4 A, I_B = 0.8 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	800			V	I_C = 4 A, I_B = 0.8 A, L = 500 μH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	1000			V	I_C = 4.0 A, 2·I_{B1} = −I_{B2} = 1.6 A, L = 180 μH, T_a = 125 °C, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 800 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2.0	mA	V_{CE} = 1 000 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

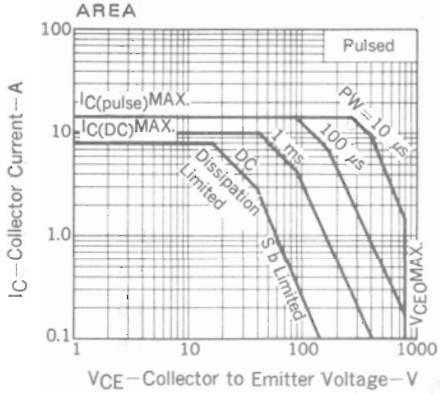
* Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

TYPICAL CHARACTERISTICS (T_a = 25 °C)

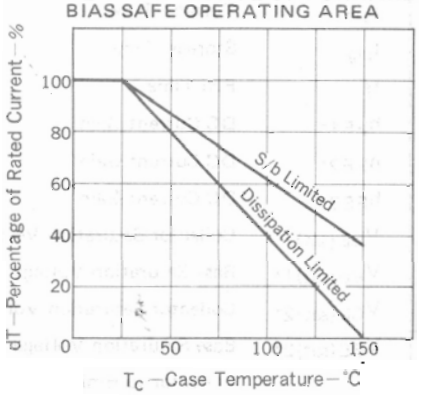
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



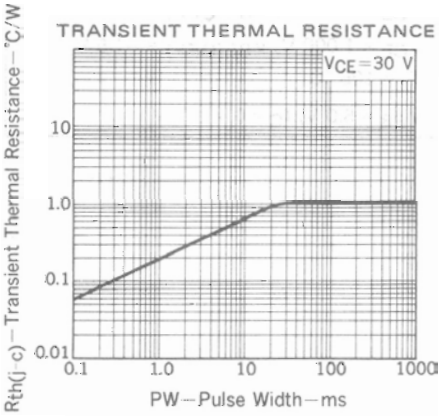
FORWARD BIAS SAFE OPERATING AREA



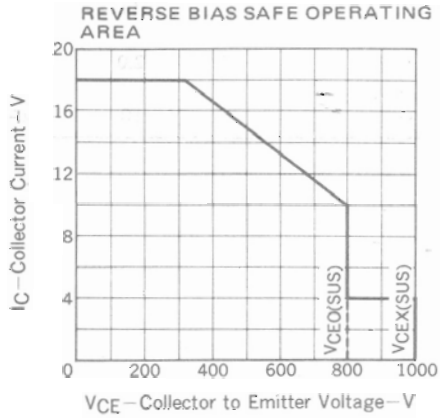
DERATING CURVE OF FORWARD BIAS SAFE OPERATING AREA



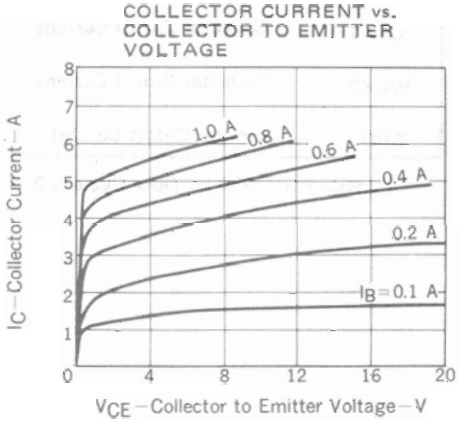
TRANSIENT THERMAL RESISTANCE



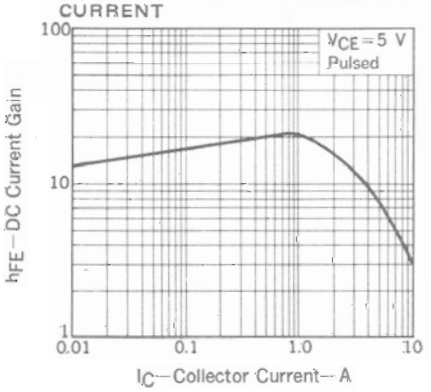
REVERSE BIAS SAFE OPERATING AREA



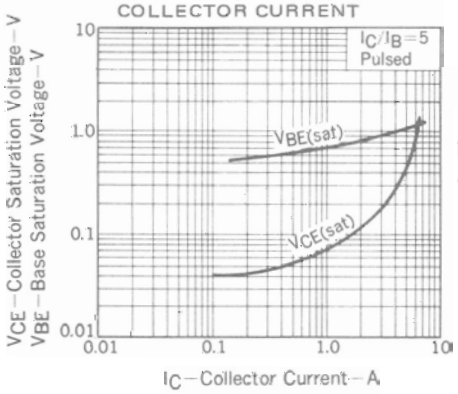
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



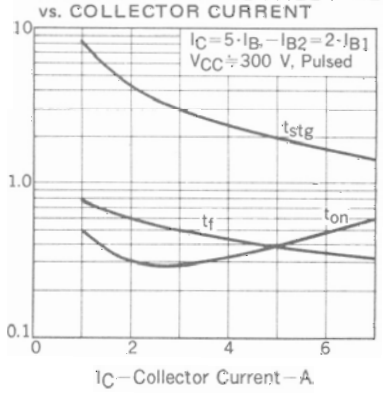
DC CURRENT GAIN vs. COLLECTOR CURRENT



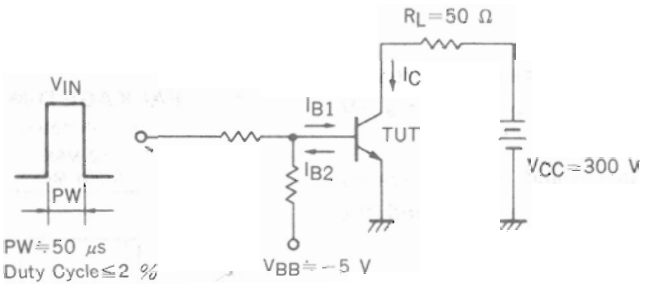
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

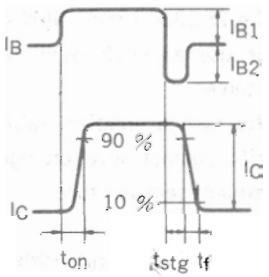


STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC3544

NEW DEVICE

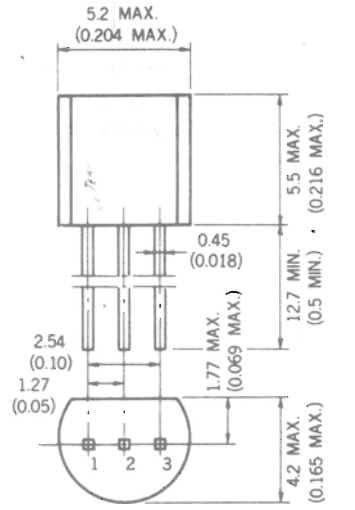
DESCRIPTION The 2SC3544 is an NPN silicon epitaxial transistor intended for use as UHF oscillator and mixer in a tuner of a TV receiver.

The device enables stable oscillation and small frequency drift against any change of the supply voltage and the ambient temperature.

FEATURES

- High Gain Bandwidth Product; f_T = 2 000 MHz TYP.
- Low Collector to Base Time Constant; $C_c \cdot r_{b'b}$ = 5 pc TYP.
- Low Feedback Capacitance; C_{re} = 0.55 pF TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage . . .	15	V
V_{EBO}	Emitter to Base Voltage	3.0	V
I_C	Collector Current	50	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	50	100	250		V_{CE} = 10 V, I_C = 5.0 mA
f_T	Gain Bandwidth Product	1.3	2.0		GHz	V_{CE} = 10 V, I_E = −5.0 mA
C_{re}	Feedback Capacitance		0.55	1.0	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		5	15	ps	V_{CE} = 10 V, I_E = −5.0 mA, f = 31.9 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 12 V, I_E = 0
$V_{CE(sat)}$	Collector Saturation Voltage			0.5	V	I_C = 10 mA, I_B = 1.0 mA

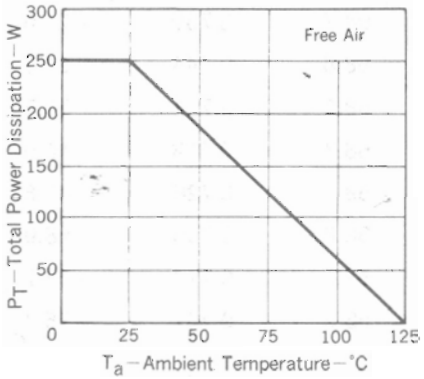
Classification of h_{FE}

Rank	M	L	K
Range	50 to 100	70 to 140	120 to 250

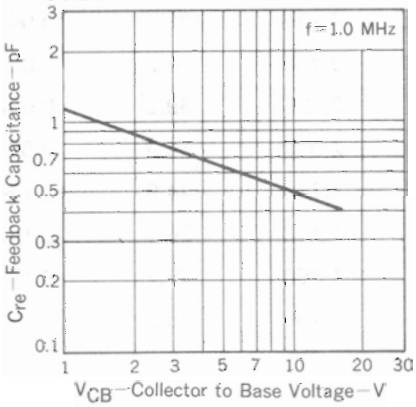
Test Conditions: V_{CE} = 10 V, I_C = 5.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

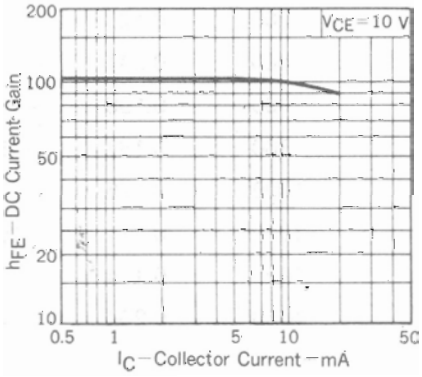
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



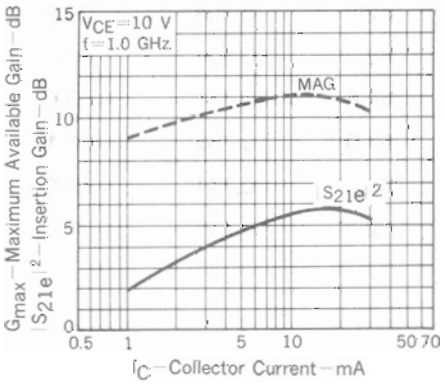
TYPICAL DEVICE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



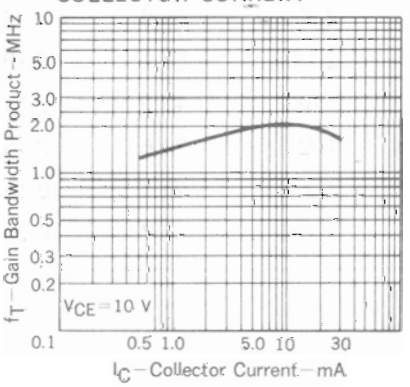
DC CURRENT GAIN vs. COLLECTOR CURRENT



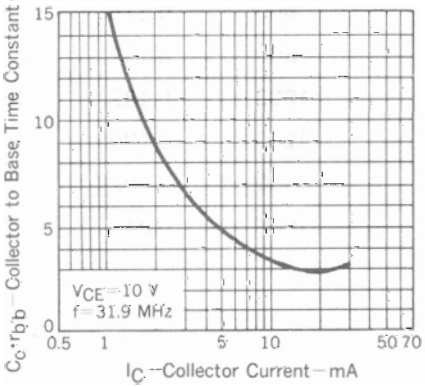
INSERTION GAIN, MAXIMUM AVAILABLE GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



COLLECTOR TO BASE TIME CONSTANT vs. COLLECTOR CURRENT



S-PARAMETER

V_{CE} = 10 V, I_C = 5 mA, Z_O = 50 Ω

f(MHz)	$\lvert S_{11} \rvert$	$\angle S_{11}$	$\lvert S_{21} \rvert$	$\angle S_{21}$	$\lvert S_{12} \rvert$	$\angle S_{12}$	$\lvert S_{22} \rvert$	$\angle S_{22}$
200	0.423	−78.0	7.244	107.7	0.047	64.7	0.780	−21.6
400	0.244	−107.9	3.756	84.2	0.062	58.8	0.744	−24.2
600	0.196	−131.7	2.686	69.2	0.088	58.0	0.721	−31.5
800	0.187	−154.3	2.037	55.8	0.099	56.7	0.718	−40.0
1000	0.175	−171.7	1.784	44.9	0.124	58.2	0.726	−49.6
1200	0.171	166.5	1.428	36.1	0.149	58.0	0.756	−58.9
1400	0.174	147.7	1.308	26.2	0.179	57.2	0.774	−67.2
1600	0.204	129.8	1.105	15.6	0.203	56.7	0.742	−75.7

V_{CE} = 10 V, I_C = 10 mA, Z_O = 50 Ω

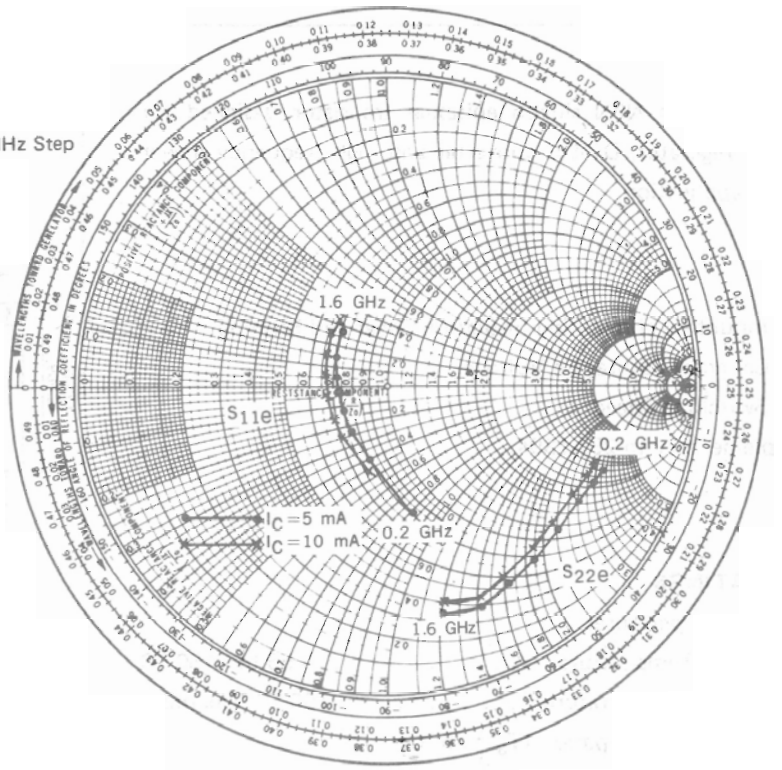
f(MHz)	$\lvert S_{11} \rvert$	$\angle S_{11}$	$\lvert S_{21} \rvert$	$\angle S_{21}$	$\lvert S_{12} \rvert$	$\angle S_{12}$	$\lvert S_{22} \rvert$	$\angle S_{22}$
200	0.281	−100.6	8.206	98.9	0.060	74.9	0.712	−21.5
400	0.220	−128.0	4.067	79.0	0.650	65.6	0.712	−22.6
600	0.218	−151.2	2.892	65.6	0.088	62.0	0.708	−29.8
800	0.181	−172.8	2.175	53.4	0.101	62.2	0.694	−38.6
1000	0.182	169.5	1.882	43.0	0.131	61.6	0.711	−48.0
1200	0.190	150.8	1.503	34.6	0.154	61.9	0.732	−58.1
1400	0.202	133.4	1.370	24.4	0.187	62.3	0.761	−66.6
1600	0.241	120.0	1.150	14.7	0.208	62.1	0.735	−74.9

TYPICAL CHARACTERISTICS (T_a = 25 °C)

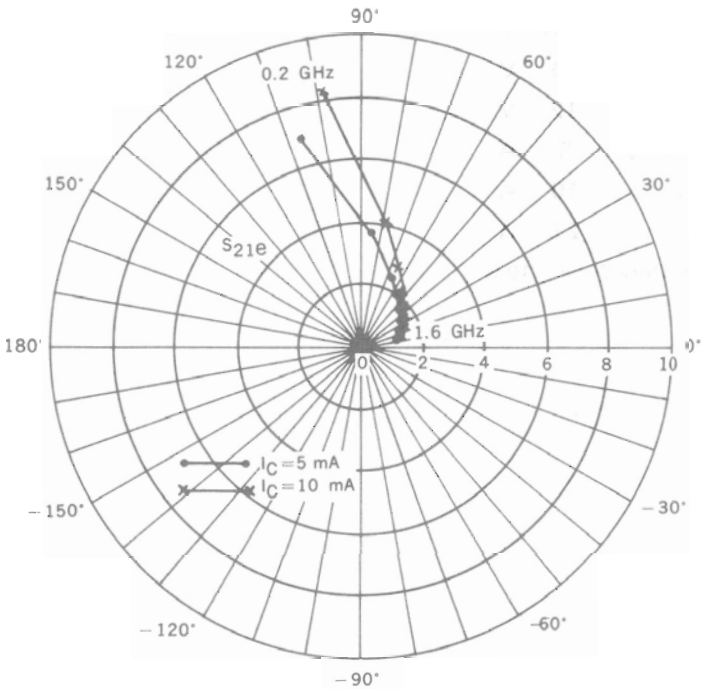
S-PARAMETER

S_{11e}, S_{22e}-FREQUENCY

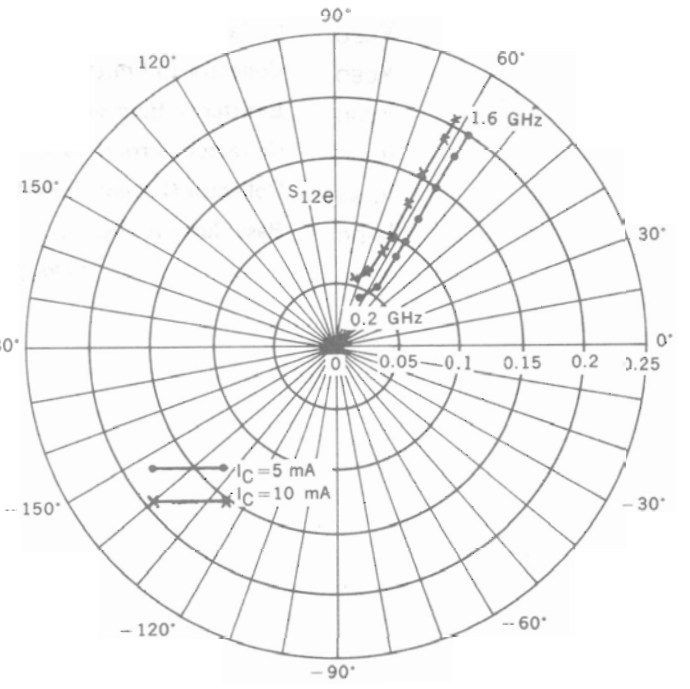
CONDITION V_{CE} = 10 V, 200 MHz Step



S_{21e}-FREQUENCY CONDITION V_{CE} = 10 V, 200 MHz Step



S_{12e}-FREQUENCY CONDITION V_{CE} = 10 V, 200 MHz Step



NEC
ELECTRON DEVICE

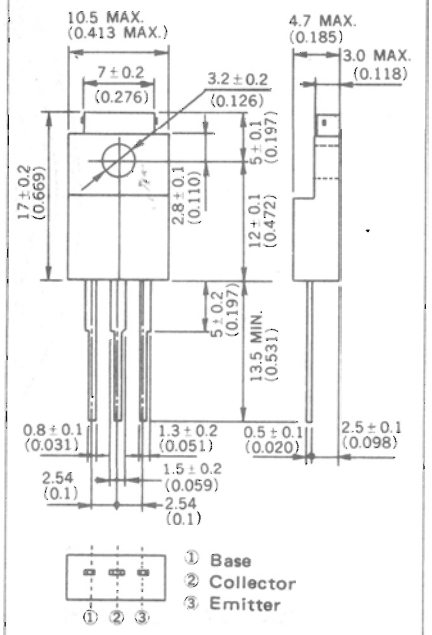
NPN SILICON POWER TRANSISTOR
2SC3566

DESCRIPTION The 2SC3566 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1394.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_a = 25 °C)

	Total Power Dissipation	25	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	12	V
$I_{C(DC)}$	Collector Current (DC)	5	A
$I_{C(pulse)}$	Collector Current (pulse)*	10	A
$I_{B(DC)}$	Base Current (DC)	2.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.3 A, R_L = 17 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}	DC Current Gain*	40			—	V_{CE} = 5.0 V, I_C = 0.3 A
h_{FE2}	DC Current Gain*	40		200	—	V_{CE} = 5.0 V, I_C = 3.0 A
$V_{CE(sat)}$	Collector Saturation Voltage*			0.6	V	I_C = 3.0 A, I_B = 0.3 A
$V_{BE(sat)}$	Base Saturation Voltage*			1.5	V	I_C = 3.0 A, I_B = 0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 3.0 A, I_B = 0.3 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.3 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 6.0 A, I_{B1} = 0.6 A, −I_{B2} = 0.3 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 10 V, I_C = 0

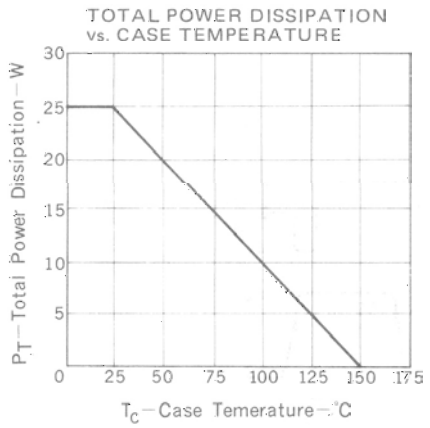
* PW ≦ 350 μs, Duty Cycle ≦ 2 %

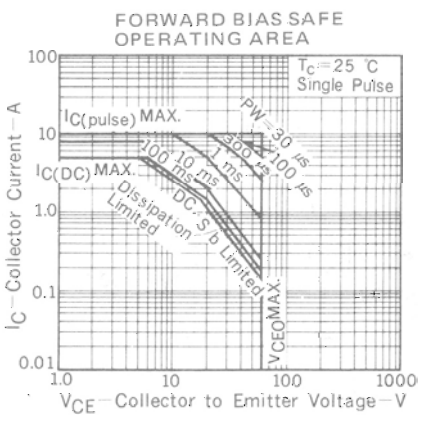
Classification of h_{FE2}

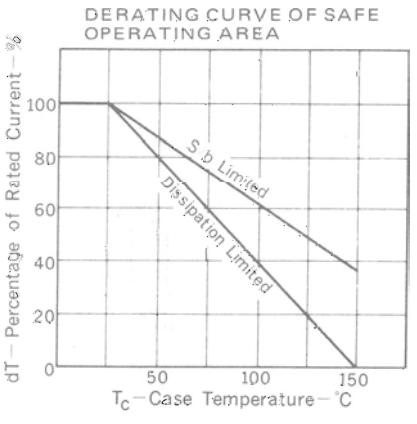
Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

Test Conditions: V_{CE} = 5.0 V, I_C = 3.0 A

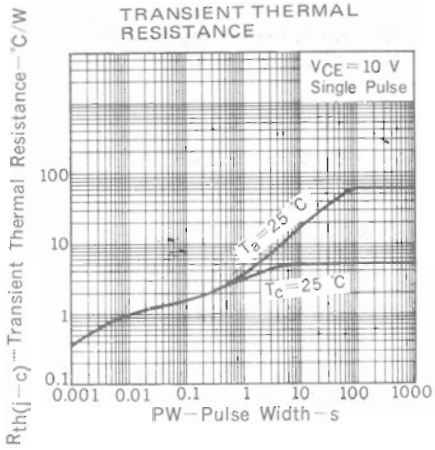
TYPICAL CHARACTERISTICS (T_a = 25 °C)



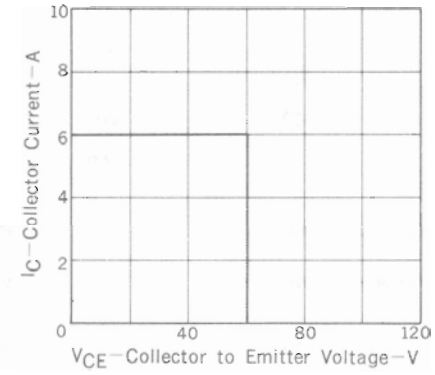




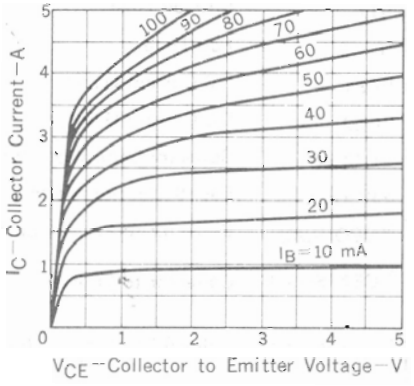
TRANSIENT THERMAL RESISTANCE



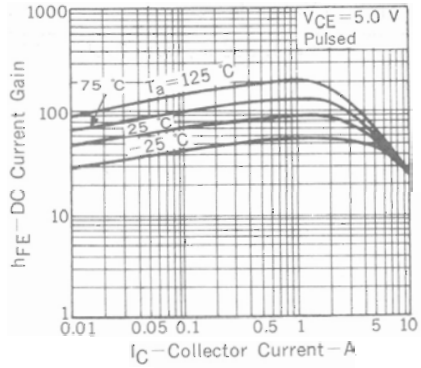
REVERSE BIAS SAFE OPERATING AREA



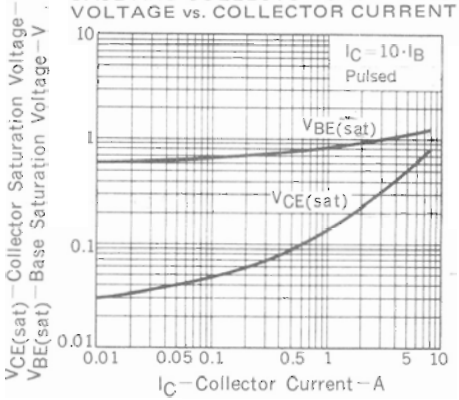
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



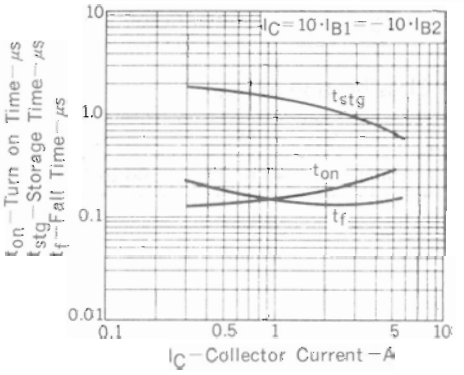
DC CURRENT GAIN vs. COLLECTOR CURRENT



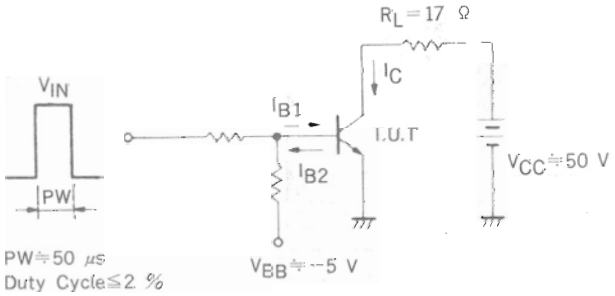
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

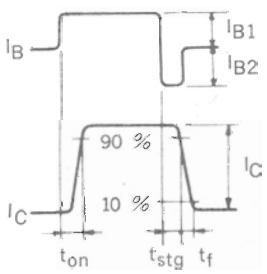


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

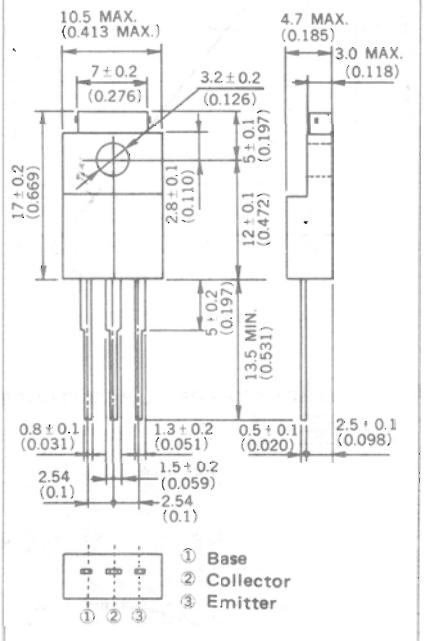
NPN SILICON POWER TRANSISTOR
2SC3567

DESCRIPTION The 2SC3567 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1395.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_a = 25 °C)

	Total Power Dissipation	1.5	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	3.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	6.0	A
$I_{B(DC)}$	Base Current (DC)	1.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT.	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = 1.5 A, I_{B1} = −I_{B2} = 0.15 A, R_L = 33 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}	DC Current Gain**	40			—	V_{CE} = 5.0 V, I_C = 0.2 A
h_{FE2}	DC Current Gain**	40		200	—	V_{CE} = 5.0 V, I_C = 1.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			0.6	V	I_C = 1.5 A, I_B = 0.15 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.5	V	I_C = 1.5 A, I_B = 0.15 A
$V_{CEO\ (SUS)}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 1.0 A, I_B = 0.1 A, L = 1 mH
$V_{CEX\ (SUS)1}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 1.0 A, I_{B1} = −I_{B2} = 0.1 A, L = 180 μH, Clamped
$V_{CEX\ (SUS)2}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.2 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 100 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

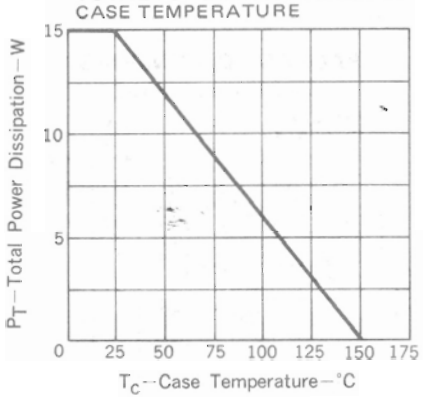
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

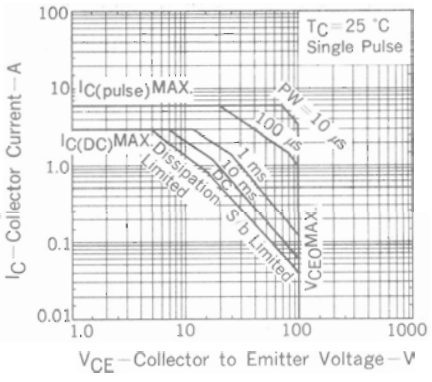
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

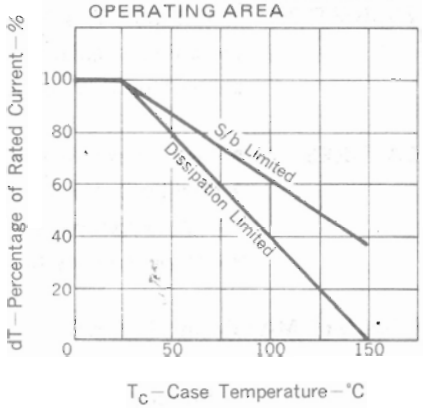
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



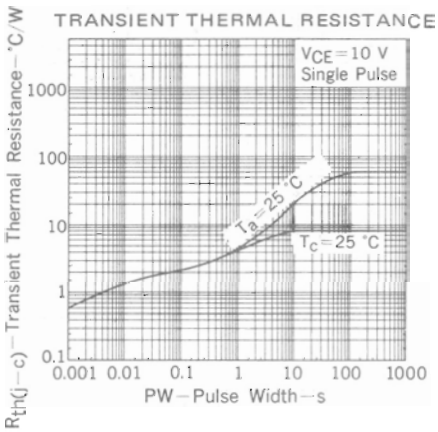
FORWARD BIAS SAFE OPERATING AREA



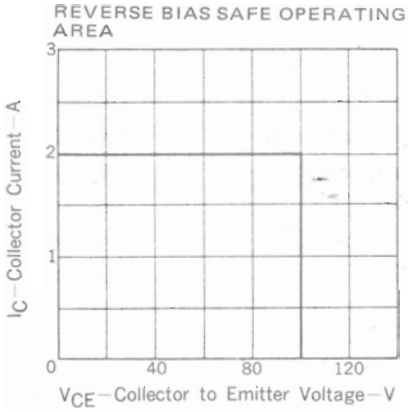
OPERATING CURVE OF SAFE OPERATING AREA



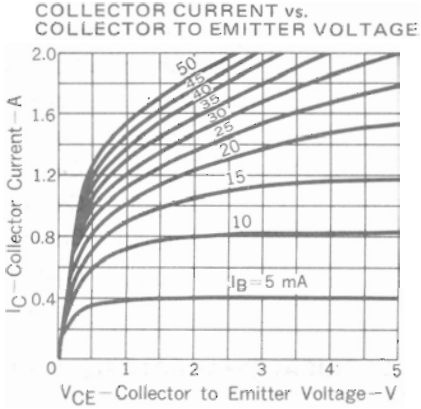
TRANSIENT THERMAL RESISTANCE



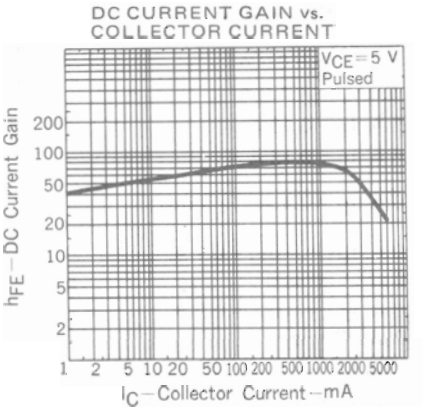
REVERSE BIAS SAFE OPERATING AREA



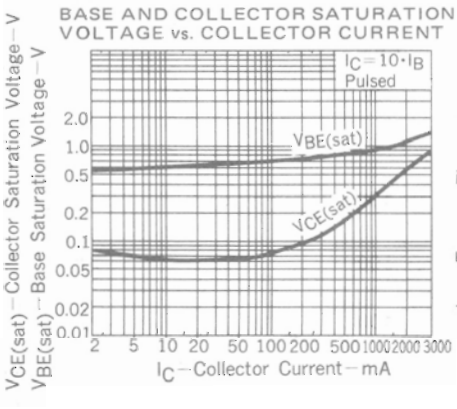
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



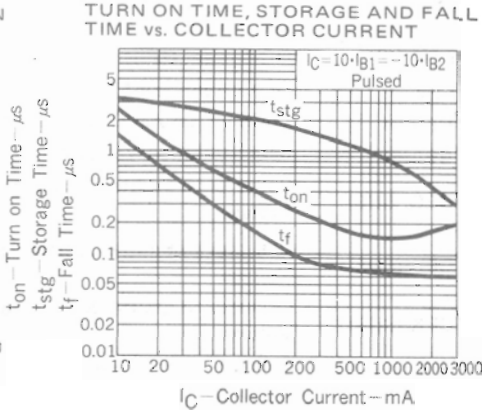
DC CURRENT GAIN vs. COLLECTOR CURRENT



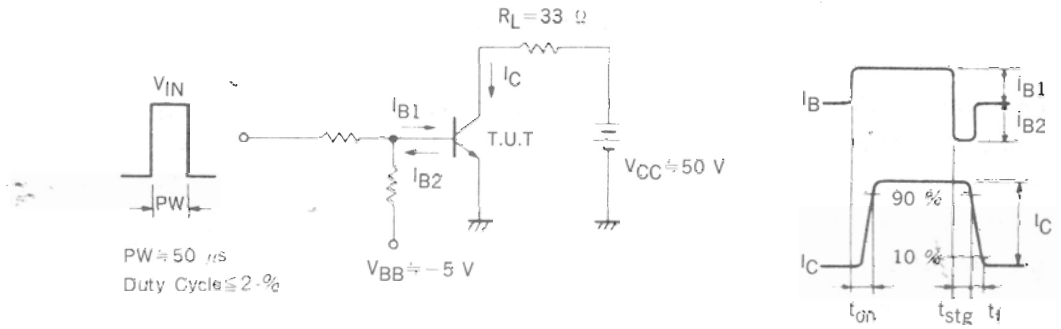
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

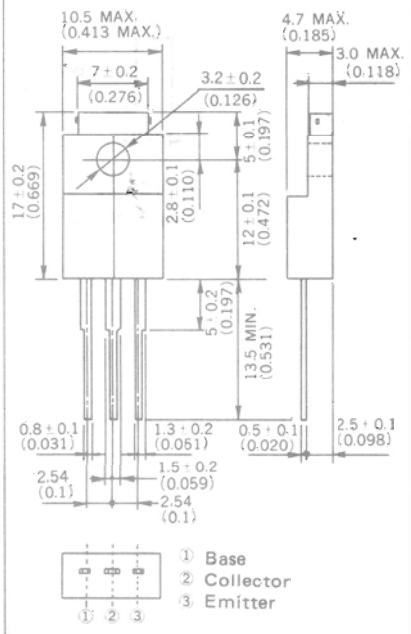
NPN SILICON POWER TRANSISTOR
2SC3568

DESCRIPTION The 2SC3568 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1396.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_C = 25 °C)

Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	10	A
$I_{C(pulse)}$	Collector Current (pulse)*	20	A
$I_{B(DC)}$	Base Current (DC)	5.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = 5.0 A, I_{B1} = −I_{B2} ≒ 0.5 A R_L = 10 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.5	μs	
h_{FE1}	DC Current Gain**	40			—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE2}	DC Current Gain**	40		200	—	V_{CE} = 5.0 V, I_C = 3.0 A
h_{FE3}	DC Current Gain**	20			—	V_{CE} = 5.0 V, I_C = 5.0 A
$V_{CE(sat)}$	Collector Saturation Voltage**			0.6	V	I_C = 5.0 A, I_B = 0.5 A
$V_{BE(sat)}$	Base Saturation Voltage**			1.5	V	I_C = 5.0 A, I_B = 0.5 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 5.0 A, I_B = 0.5 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 5.0 A, I_{B1} ≒ −I_{B2} = 0.5 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	100			V	I_C = 10 A, I_{B1} = 1.0 A, −I_{B2} = 0.5 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 100 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 100 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 100 V, $V_{BE(OFF)}$ ≒ −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

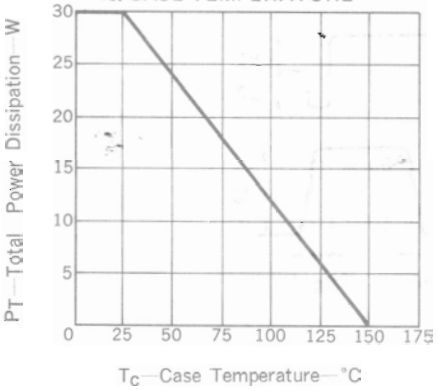
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

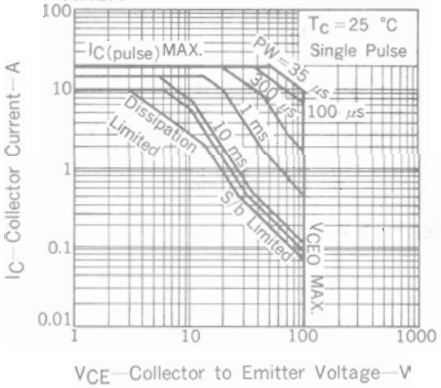
Test Conditions: V_{CE} = 5.0 V, I_C = 3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

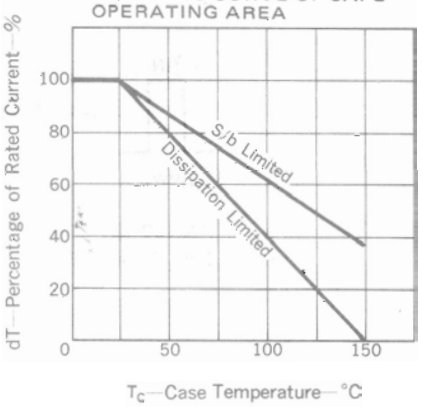
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



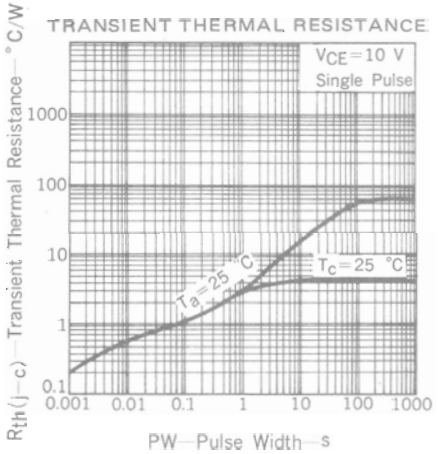
FORWARD BIAS SAFE OPERATING AREA



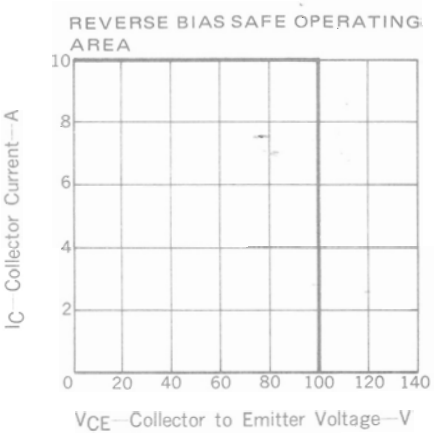
DERATING CURVE OF SAFE OPERATING AREA



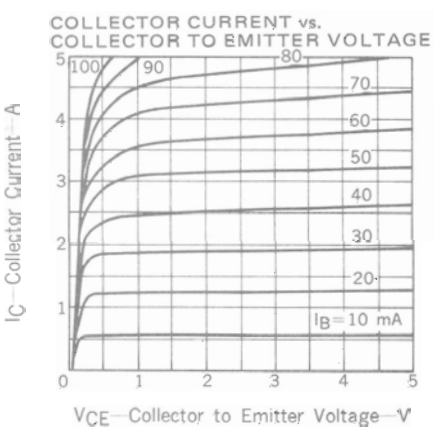
TRANSIENT THERMAL RESISTANCE



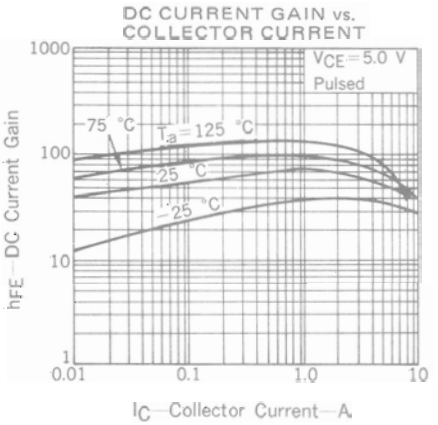
REVERSE BIAS SAFE OPERATING AREA



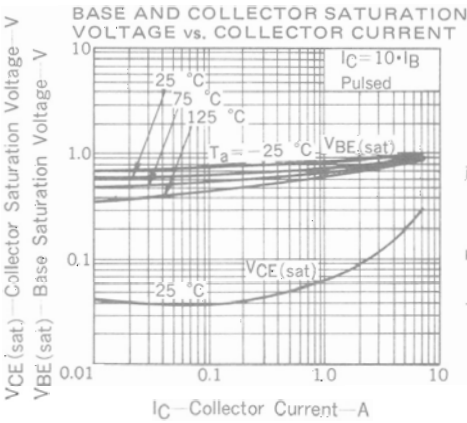
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



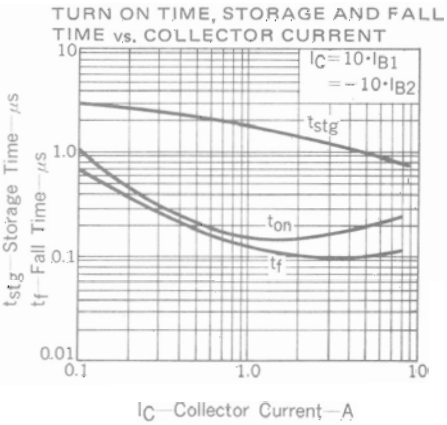
DC CURRENT GAIN vs. COLLECTOR CURRENT



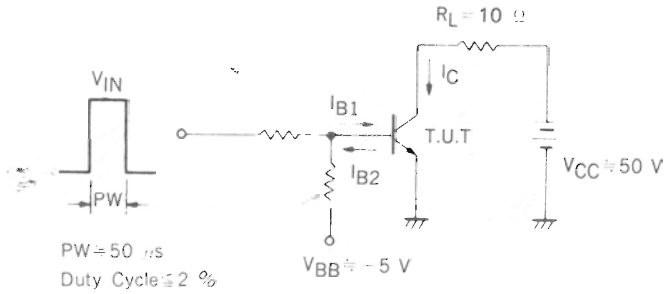
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

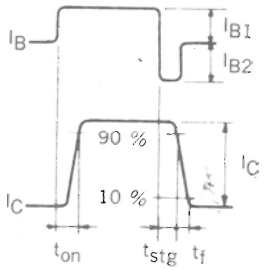


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

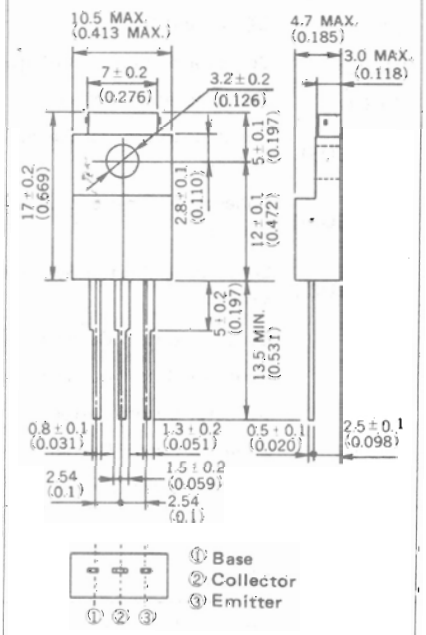
NPN SILICON POWER TRANSISTOR
2SC3569

DESCRIPTION The 2SC3569 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_C = 25 °C)

	Total Power Dissipation	15	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	2.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	4.0	A
$I_{B(DC)}$	Base Current (DC)	1.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 0.7 A, I_{B1} = −I_{B2} = 0.14 A R_L = 214 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			1.0	μs	
h_{FE1}*	DC Current Gain	20		80	—	V_{CE} = 5.0 V, I_C = 0.2 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 0.5 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 0.7 A, I_B = 0.14 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 0.7 A, I_B = 0.14 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 0.5 A, I_B = 0.1 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 0.5 A, I_{B1} = −I_{B2} = 0.1 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 1.0 A, I_{B1} = 0.2 A, −I_{B2} = 0.1 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

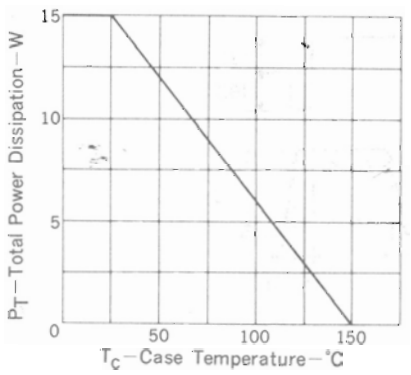
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

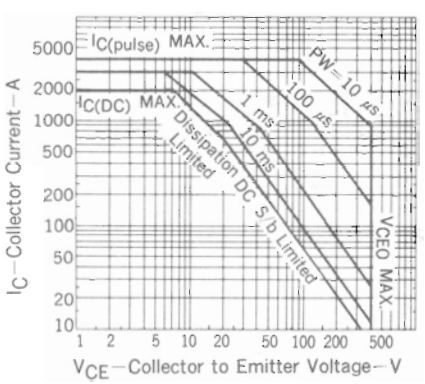
Test Conditions: V_{CE} = 5.0 V, I_C = 0.2 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

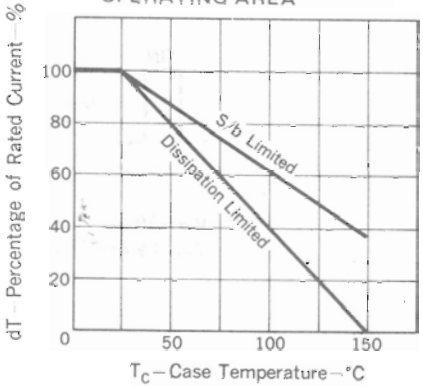
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



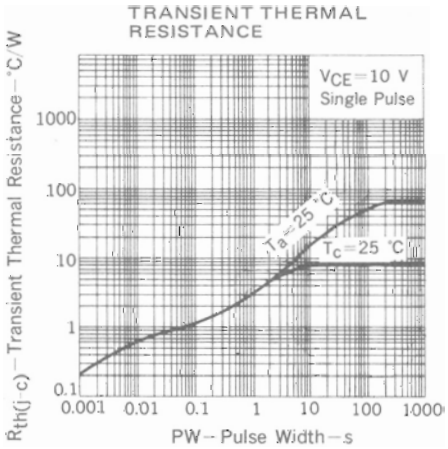
FORWARD BIAS SAFE OPERATING AREA



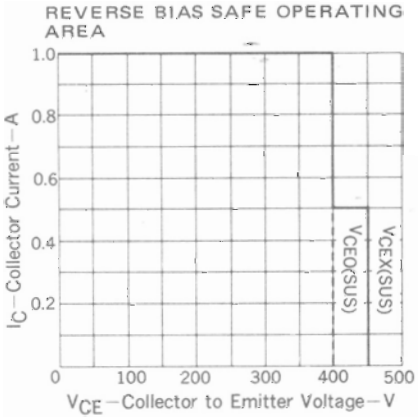
DERATING CURVE OF SAFE OPERATING AREA



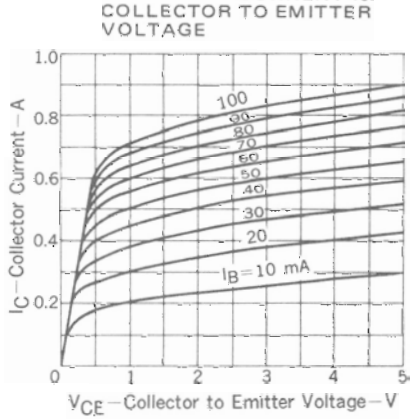
TRANSIENT THERMAL RESISTANCE



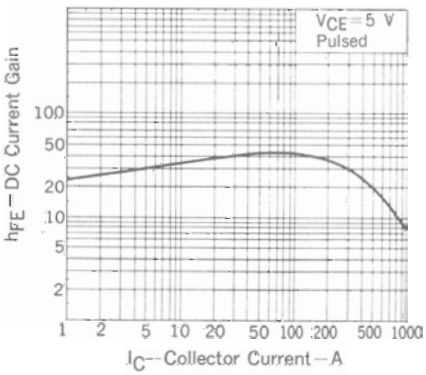
REVERSE BIAS SAFE OPERATING AREA



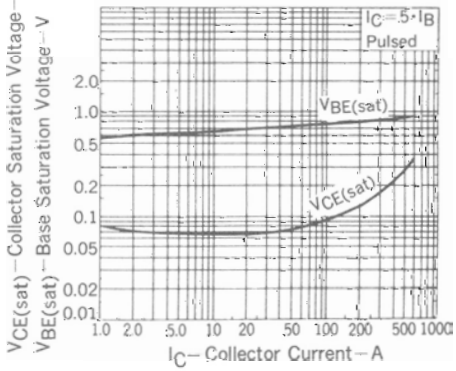
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



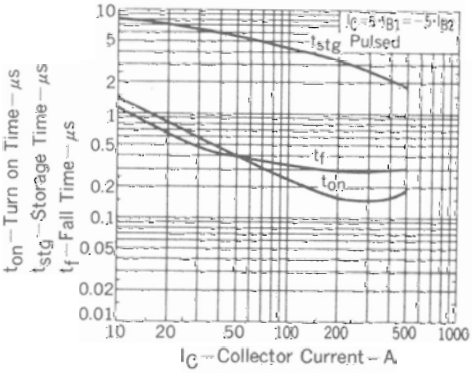
DC CURRENT GAIN vs. COLLECTOR CURRENT



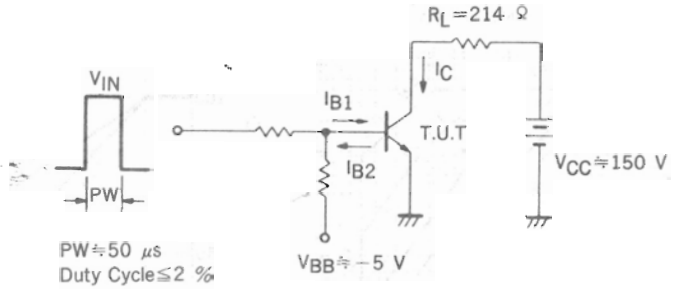
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

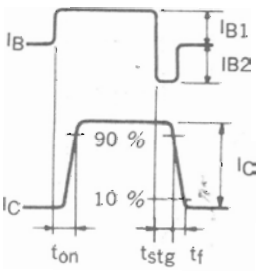


TURN ON TIME, STORAGE TIME AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

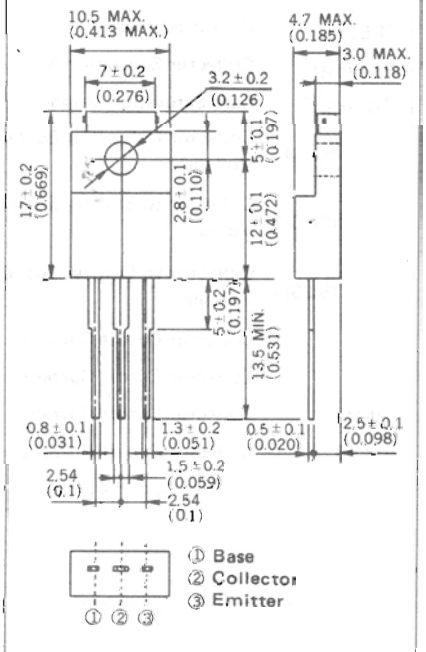
NPN SILICON POWER TRANSISTOR
2SC3570

DESCRIPTION The 2SC3570 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	8.0	V
$I_{C(DC)}$	Collector Current (DC)	5.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	10	A
$I_{B(DC)}$	Base Current (DC)	2.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.4 A R_L = 75 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			2.0	μs	
t_f	Fall Time			0.7	μs	
h_{FE1}*	DC Current Gain	20		80	—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 2.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 2.0 A, I_B = 0.4 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 2.0 A, I_B = 0.4 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 2.0 A, I_B = 0.4 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.4 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 4.0 A, I_{B1} = 0.8 A, −I_{B2} = 0.4 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

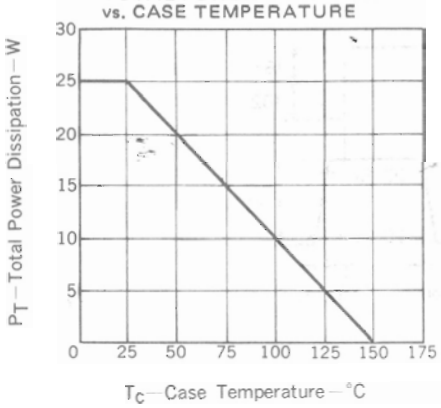
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

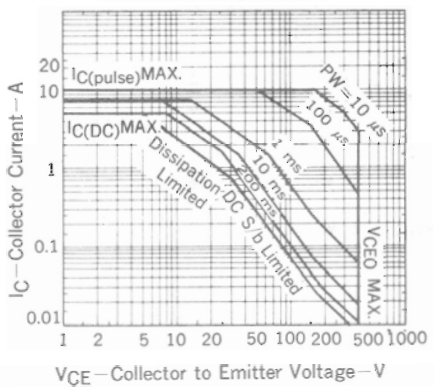
Test Conditions: V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

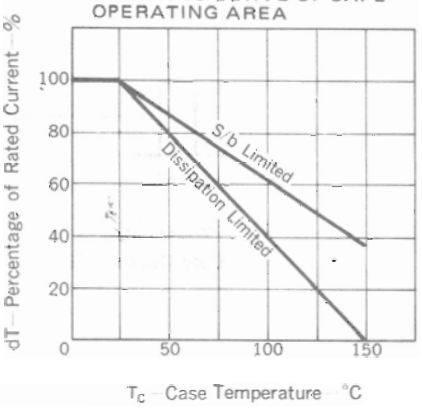
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



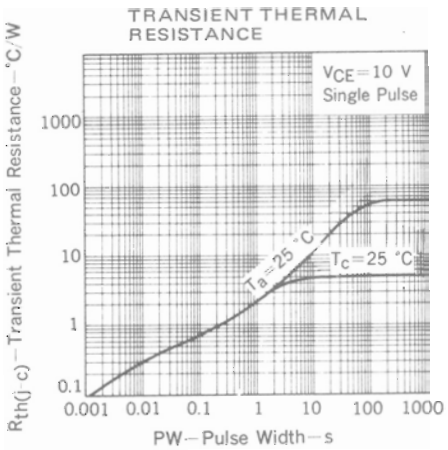
FORWARD BIAS SAFE OPERATING AREA



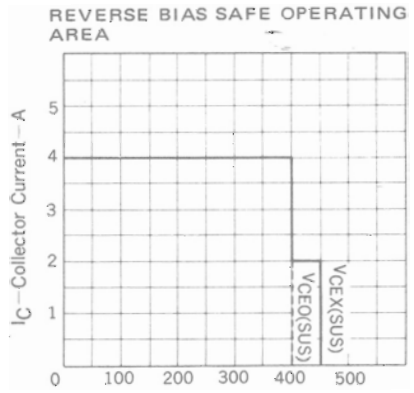
DERATING CURVE OF SAFE OPERATING AREA



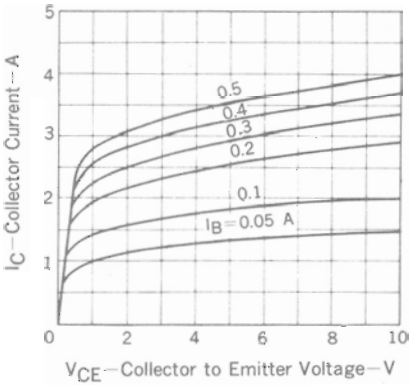
TRANSIENT THERMAL RESISTANCE



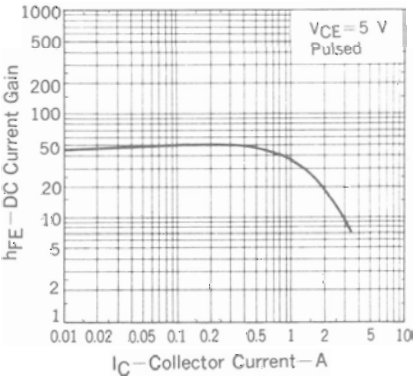
REVERSE BIAS SAFE OPERATING AREA



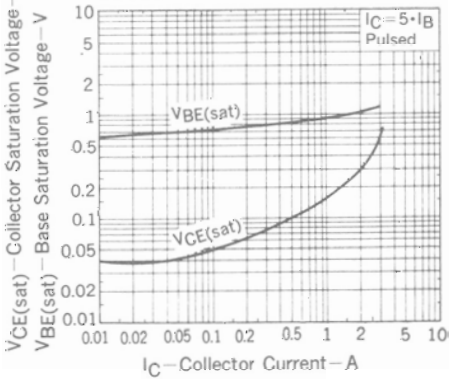
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



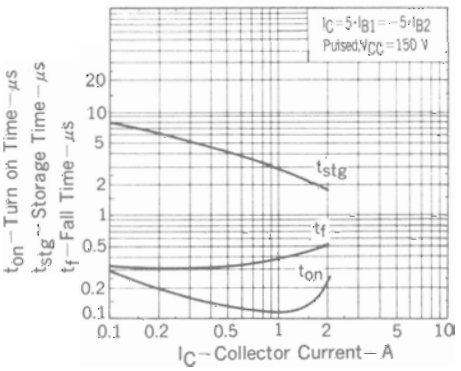
DC CURRENT GAIN vs. COLLECTOR CURRENT



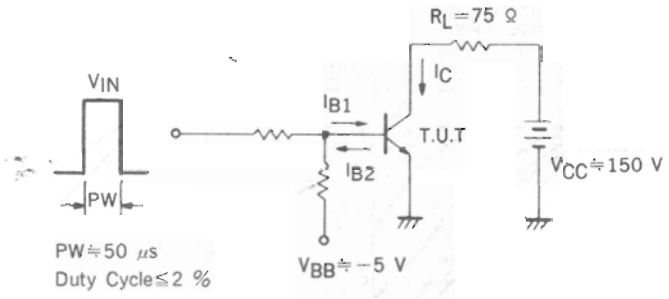
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

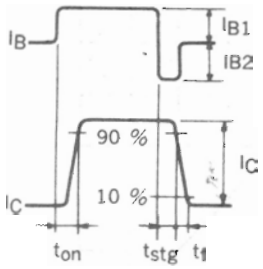


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

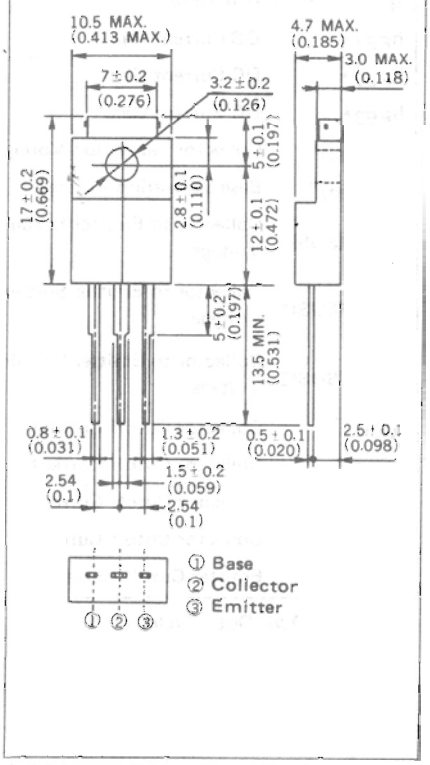
NPN SILICON POWER TRANSISTOR
2SC3571

DESCRIPTION The 2SC3571 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_C = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	7.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	15	A
$I_{B(DC)}$	Base Current (DC)	3.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.6 A R_L = 50 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			1.0	μs	
h_{FE1}*	DC Current Gain	20		80	—	V_{CE} = 5.0 V, I_C = 0.1 A
h_{FE2}*	DC Current Gain	20		80	—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE3}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 3.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 3.0 A, I_B = 0.6 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 3.0 A, I_B = 0.6 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 3.0 A, I_B = 0.6 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.6 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 6.0 A, I_{B1} = 2.0 A, −I_{B2} = 0.6 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

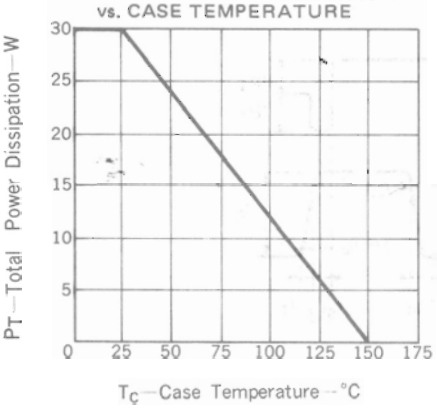
Classification of h_{FE2}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

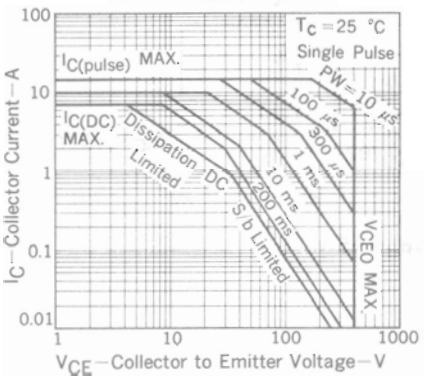
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

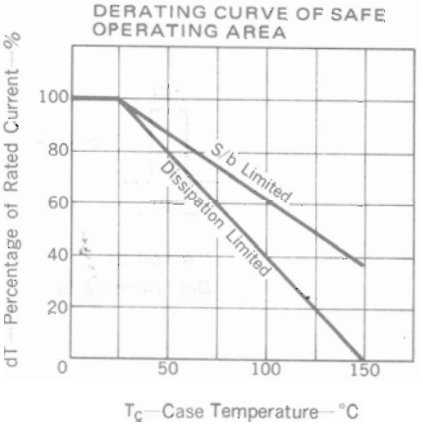
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



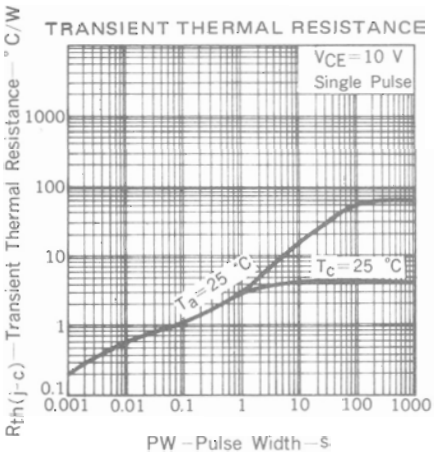
FORWARD BIAS SAFE OPERATING AREA



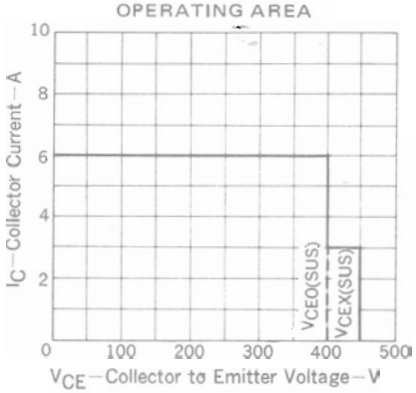
DERATING CURVE OF SAFE OPERATING AREA



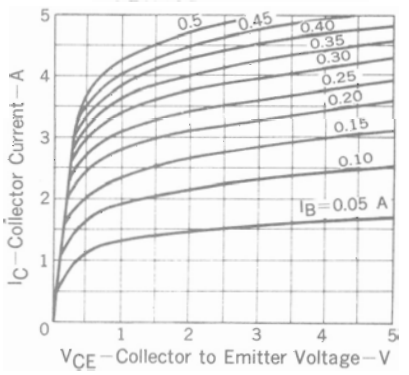
TRANSIENT THERMAL RESISTANCE



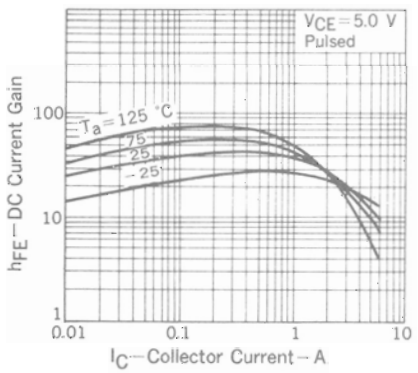
REVERSE BIAS SAFE OPERATING AREA



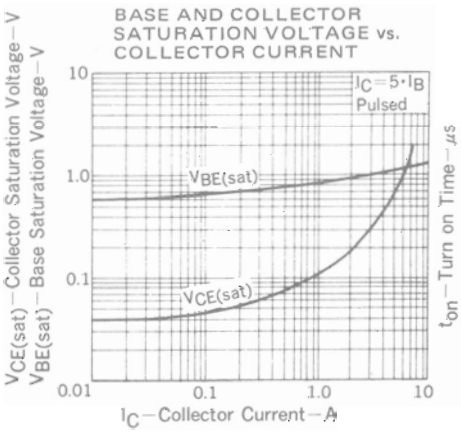
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



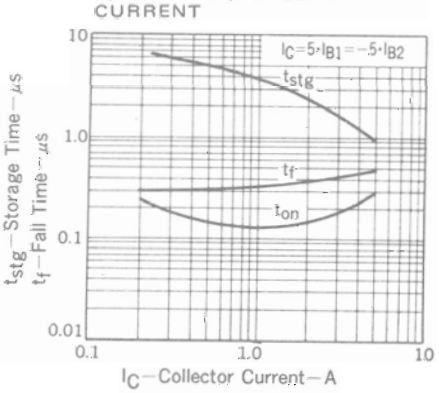
DC CURRENT GAIN vs. COLLECTOR CURRENT



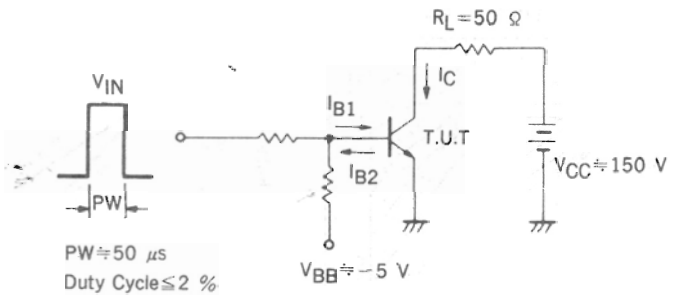
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

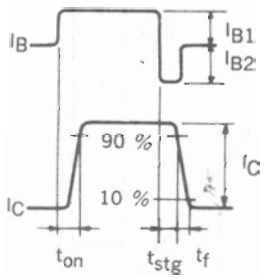


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

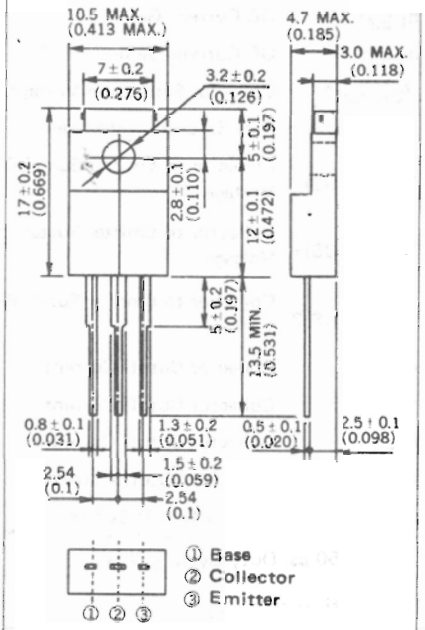
NPN SILICON POWER TRANSISTOR
2SC3572

DESCRIPTION The 2SC3572 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 Maximum	°C

Maximum Power Dissipation (T_c = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	10	A
$I_{C(pulse)}$	Collector Current (pulse)*	20	A
$I_{B(DC)}$	Base Current (DC)	5.0	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			1.0	μs	I_C = 6.0 A, I_{B1} = −I_{B2} = 1.2 A R_L = 25 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			2.5	μs	
t_f	Fall Time			0.7	μs	
h_{FE1}*	DC Current Gain	15		80	—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 3.0 A
h_{FE3}*	DC Current Gain	7.0			—	V_{CE} = 5.0 V, I_C = 6.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 6.0 A, I_B = 1.2 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.5	V	I_C = 6.0 A, I_B = 1.2 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 6.0 A, I_B = 1.2 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 6.0 A, I_{B1} = −I_{B2} = 1.2 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 12 A, I_{B1} = 2.4 A, −I_{B2} = 1.2 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			100	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

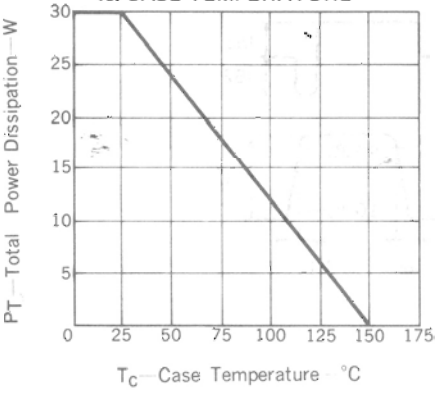
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

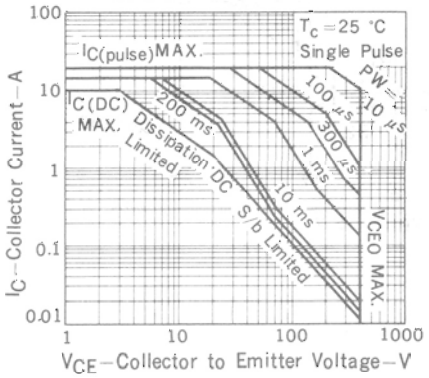
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

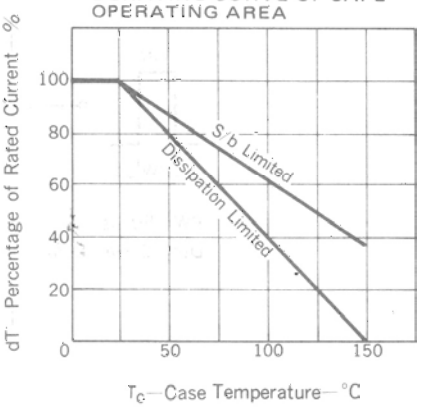
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



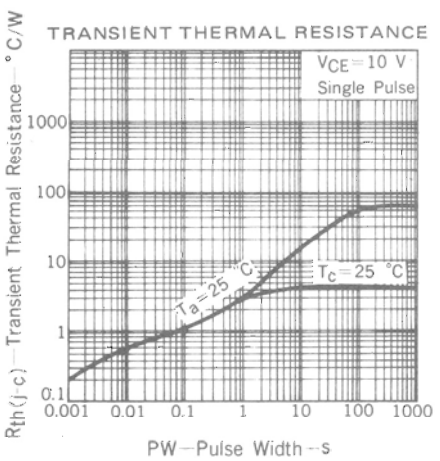
FORWARD BIAS SAFE OPERATING AREA



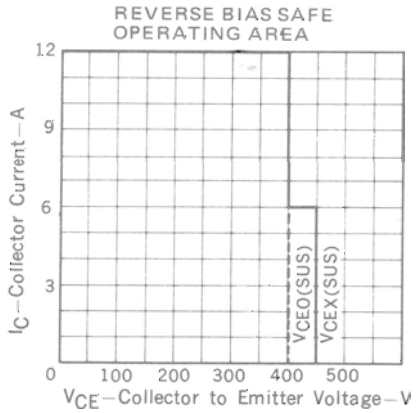
DERATING CURVE OF SAFE OPERATING AREA



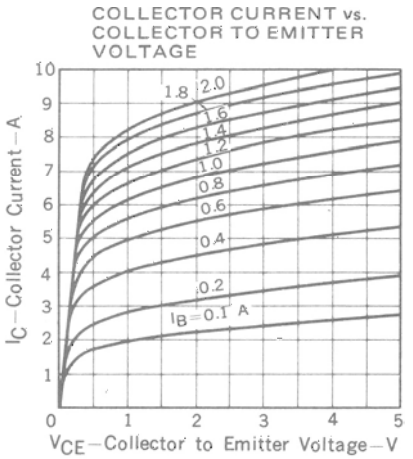
TRANSIENT THERMAL RESISTANCE



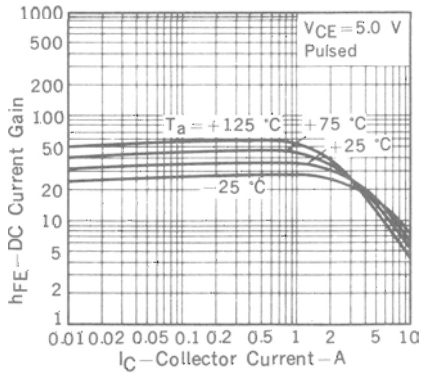
REVERSE BIAS SAFE OPERATING AREA



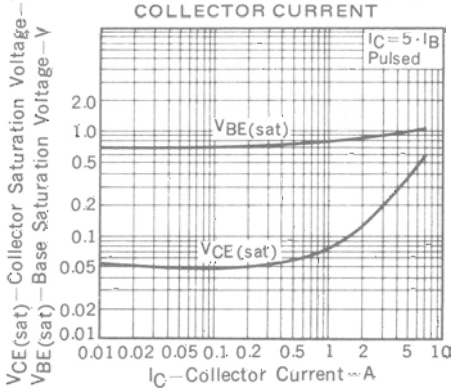
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



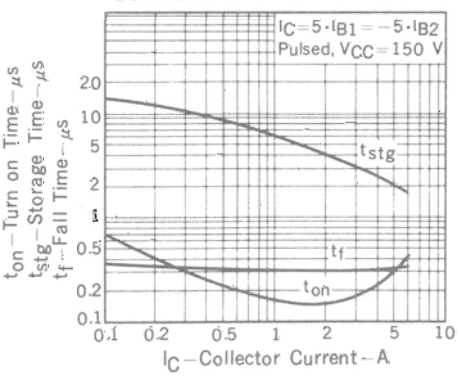
DC CURRENT GAIN vs. COLLECTOR CURRENT



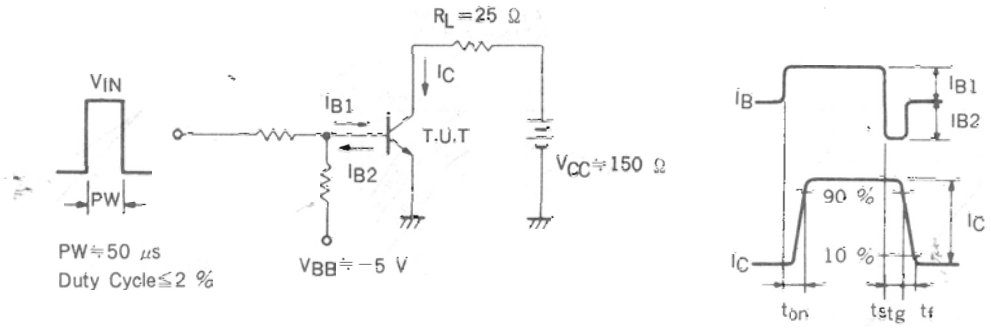
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

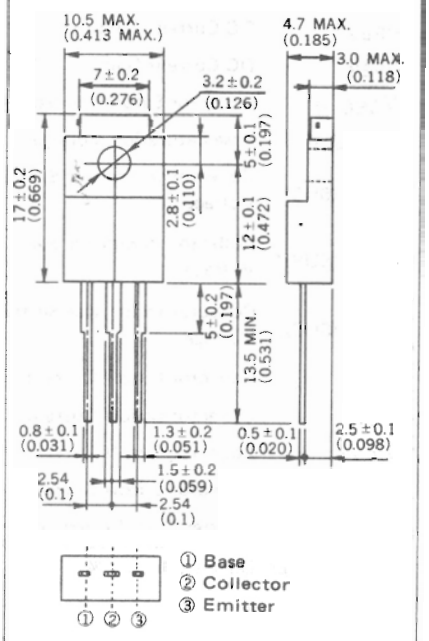
NPN SILICON POWER TRANSISTOR
2SC3573

DESCRIPTION The 2SC3573 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 Maximum	°C

Maximum Power Dissipation (T_C = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	5.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	10	A
$I_{B(DC)}$	Base Current (DC)	2.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.4 A R_L ≒ 75 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	10		60	—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE2}*	DC Current Gain	10			—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE3}*	DC Current Gain	8			—	V_{CE} = 5.0 V, I_C = 2.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 2.0 A, I_B = 0.4 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.5	V	I_C = 2.0 A, I_B = 0.4 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 2.0 A, I_B = 0.4 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.4 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 4.0 A, I_{B1} = 0.8 A, −I_{B2} = 0.4 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			100	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

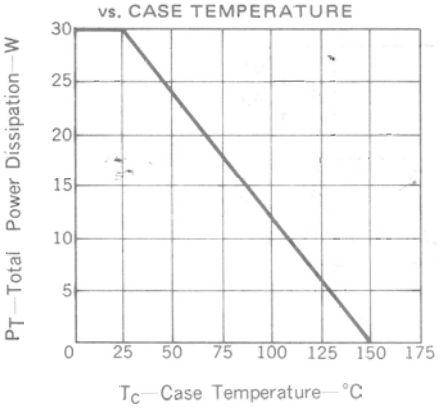
Classification of h_{FE1}

Rank	M	L	K
Range	10 to 30	20 to 40	30 to 60

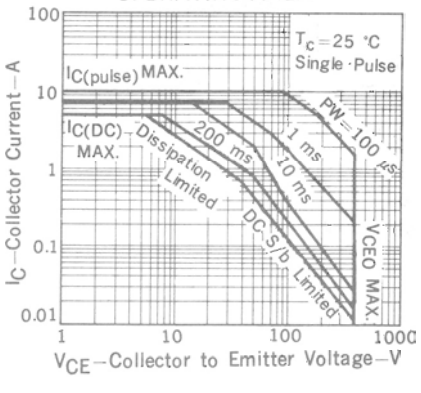
Test Conditions: V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

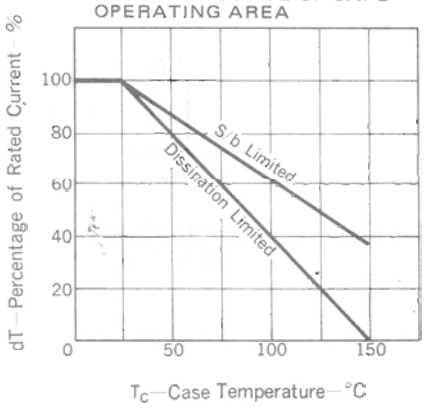
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



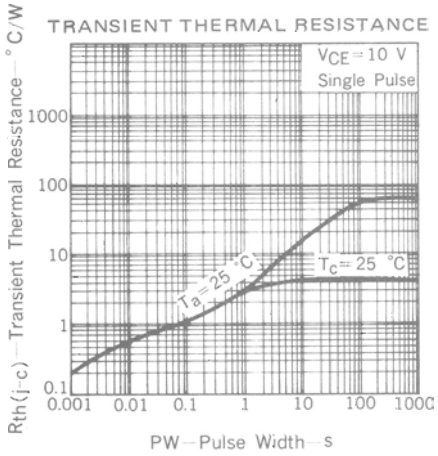
FORWARD BIAS SAFE OPERATING AREA



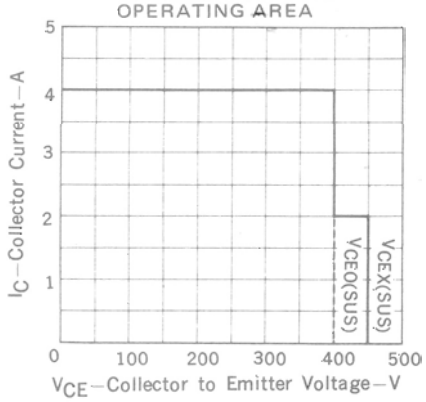
DERATING CURVE OF SAFE OPERATING AREA



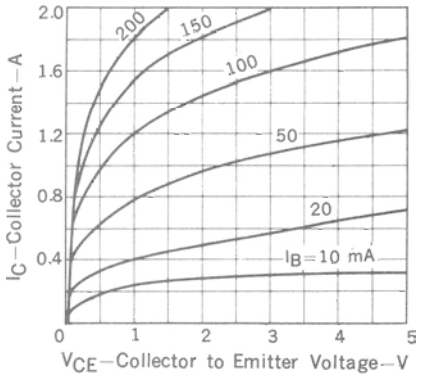
TRANSIENT THERMAL RESISTANCE



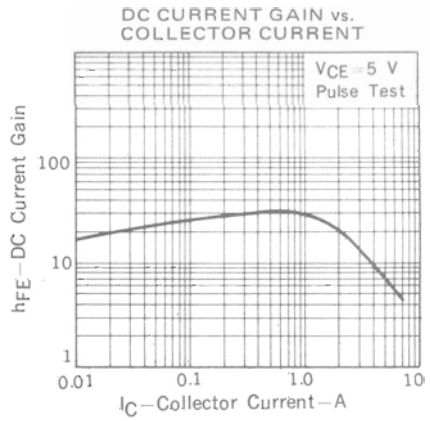
REVERSE BIAS SAFE OPERATING AREA



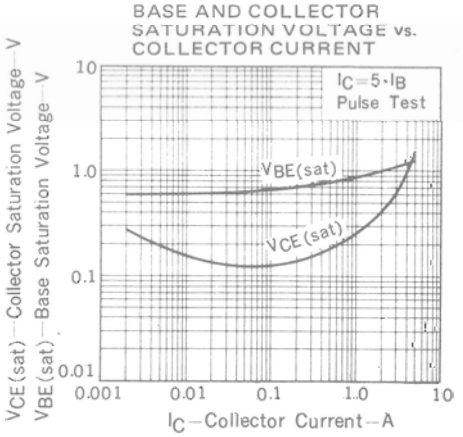
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



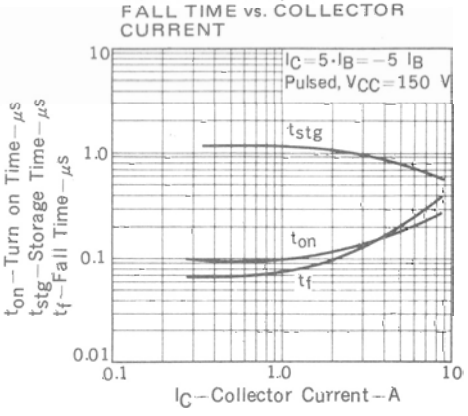
DC CURRENT GAIN vs. COLLECTOR CURRENT



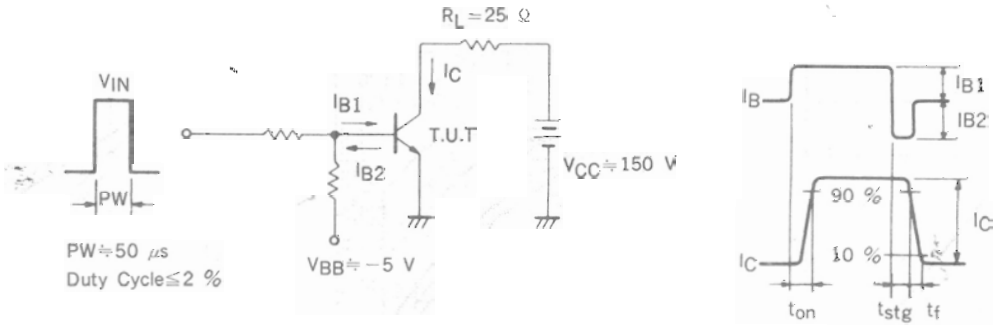
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

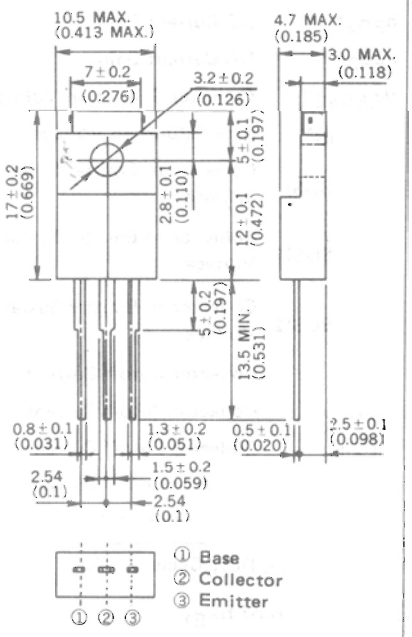
NPN SILICON POWER TRANSISTOR
2SC3574

DESCRIPTION The 2SC3574 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	7.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	15	A
$I_{B(DC)}$	Base Current (DC)	3.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.5	μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.6 A R_L = 50 Ω, V_{CC} ≒ 150 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	10		60	—	V_{CE} = 5.0 V, I_C = 0.7 A
h_{FE2}*	DC Current Gain	10		60	—	V_{CE} = 5.0 V, I_C = 1.5 A
h_{FE3}*	DC Current Gain	8			—	V_{CE} = 5.0 V, I_C = 3.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			1.0	V	I_C = 3.0 A, I_B = 0.6 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.5	V	I_C = 3.0 A, I_B = 0.6 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 3.0 A, I_B = 0.6 A, L = 1 mH
$V_{CEX(SUS)1}$	Collector to Emitter Sustaining Voltage	450			V	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.6 A, L = 180 μH, Clamped
$V_{CEX(SUS)2}$	Collector to Emitter Sustaining Voltage	400			V	I_C = 6.0 A, I_{B1} = 1.2 A, −I_{B2} = 0.6 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 400 V, I_E = 0
I_{CER}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			2.0	mA	V_{CE} = 400 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

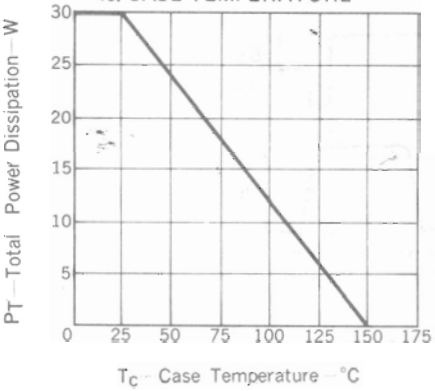
Classification of h_{FE1}

Rank	M	L	K
Range	20 to 40	30 to 60	40 to 80

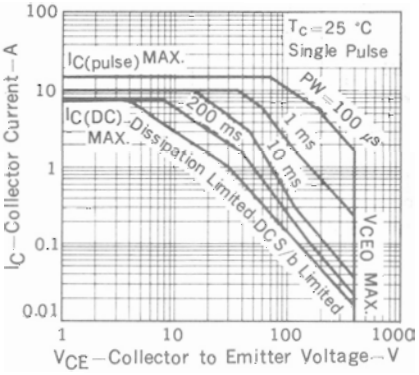
Test Conditions: V_{CE} = 5.0 V, I_C = 0.7 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

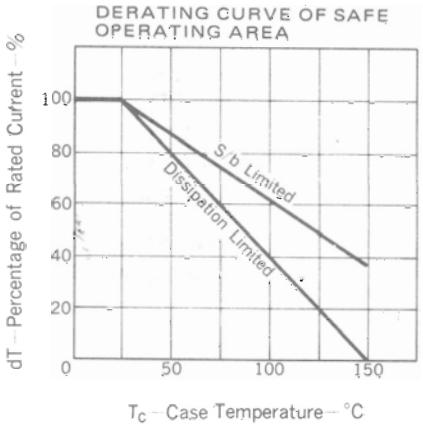
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



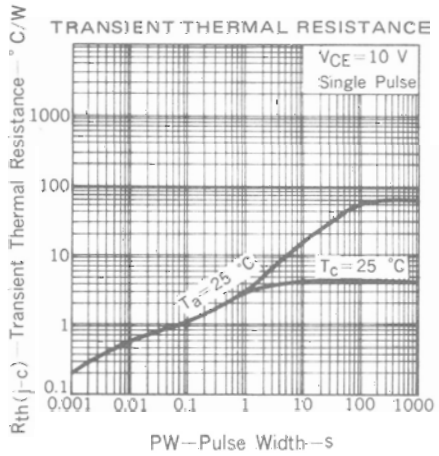
FORWARD BIAS SAFE OPERATING AREA



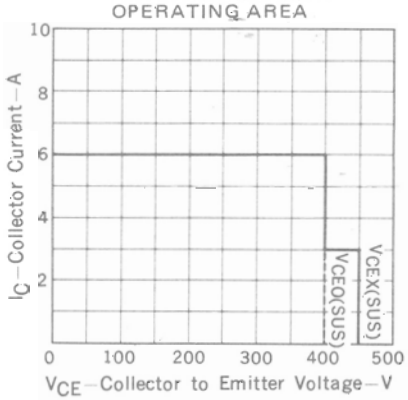
DERATING CURVE OF SAFE OPERATING AREA



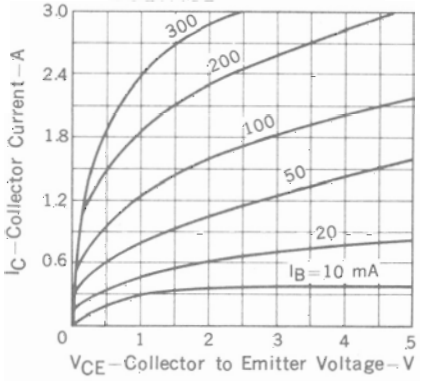
TRANSIENT THERMAL RESISTANCE



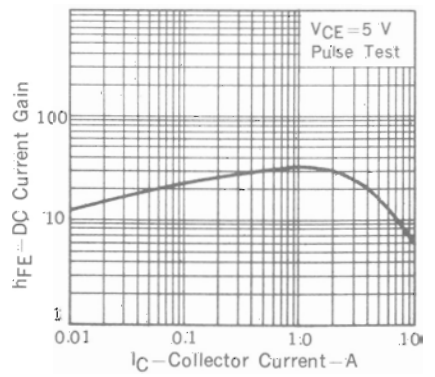
REVERSE BIAS SAFE OPERATING AREA



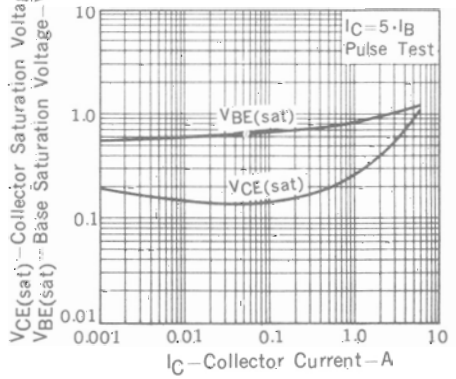
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



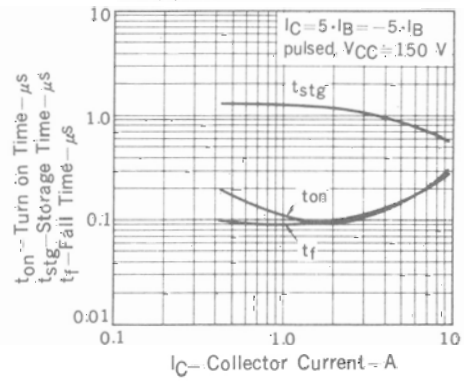
DC CURRENT GAIN vs. COLLECTOR CURRENT



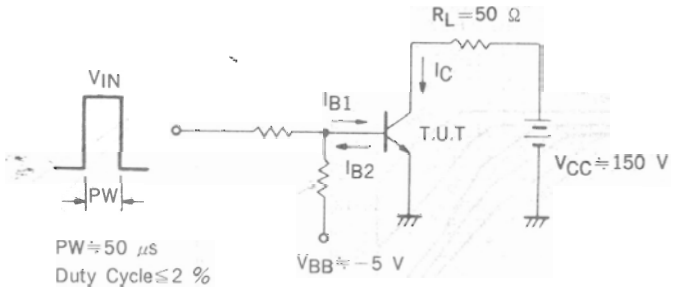
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

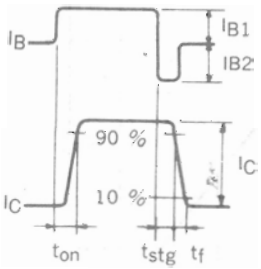


TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

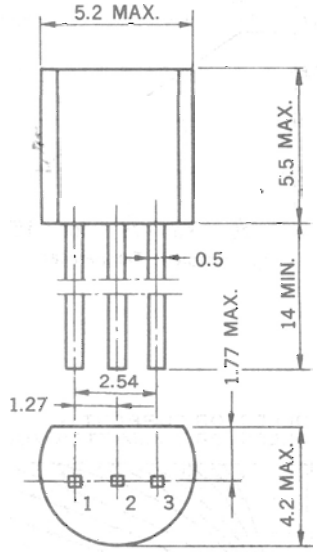
NPN SILICON TRANSISTOR
2SC3615

DESCRIPTION The 2SC3615 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving, instead of Darlington Transistor, or muting.

FEATURES

- High DC Current Gain.
  h_{FE} = 800 to 3200 (@ V_{CE} = 5.0 V, I_C = 100 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.11 V TYP. (@ I_C/I_B = 100 mA/1.0 mA)
- High V_{EBO} : V_{EBO} = 15 V
- High Total Power Dissipation. : P_T = 0.75 W (@ T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter EIAJ : SC-43B
2. Collector JEDEC : TO-92
3. Base IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	50	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	15	V
I_C	Collector Current (DC)	300	mA
I_C	Collector Current (pulse)*	500	mA

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	800		3200	–	V_{CE} = 5.0 V, I_C = 100 mA
h_{FE2}	DC Current Gain	640			–	V_{CE} = 5.0 V, I_C = 300 mA
f_T	Gain Bandwidth Product	150	220		MHz	V_{CE} = 5.0 V, I_E = −100 mA
C_{ob}	Output Capacitance		8.0		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600		700	mV	V_{CE} = 5.0 V, I_C = 100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.11	0.3	V	I_C = 100 mA, I_B = 1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.7	1.2	V	I_C = 100 mA, I_B = 1.0 mA
t_{on}	Turn-On Time		0.15		μs	(V_{CC} = 10 V, $V_{BE(off)}$ ≒ −2.7 V, I_C = 200 mA, I_{B1} = −I_{B2} = 4.0 mA)
t_{stg}	Storage Time		0.75		μs	
t_{off}	Turn-Off Time		1.1		μs	

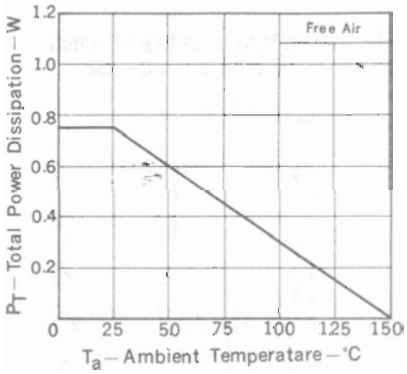
Classification of h_{FE1}

Rank	M	L	K
Range	800 to 1600	1200 to 2400	2000 to 3200

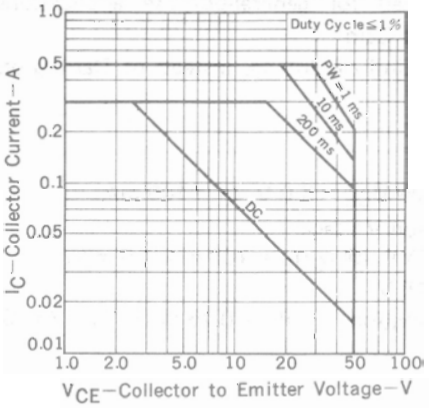
Test Conditions: V_{CE} = 5.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

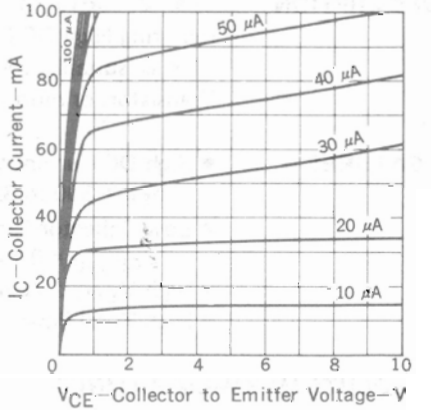
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



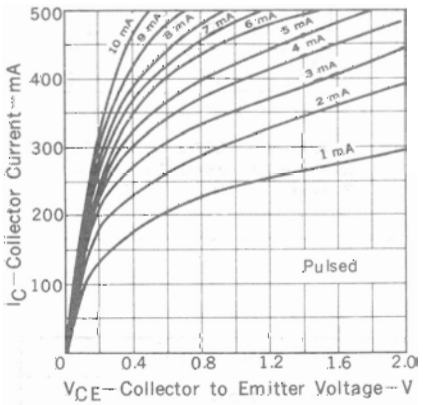
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



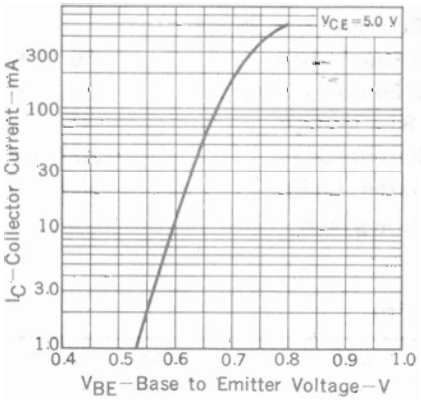
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



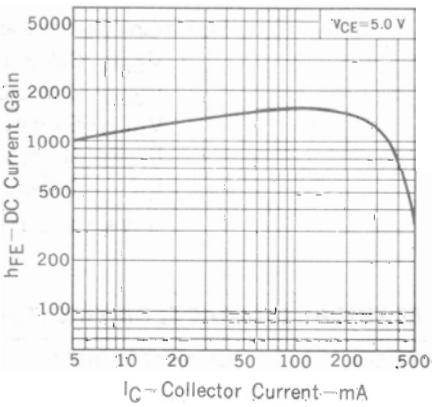
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



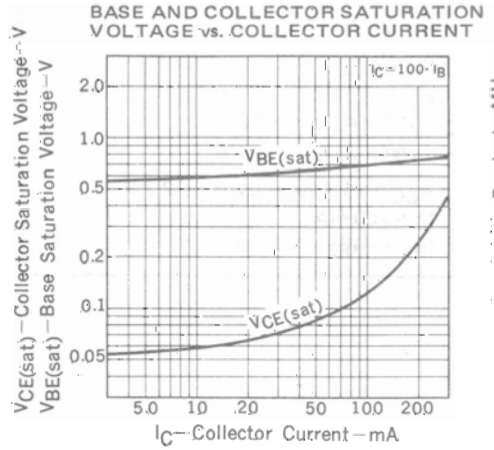
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



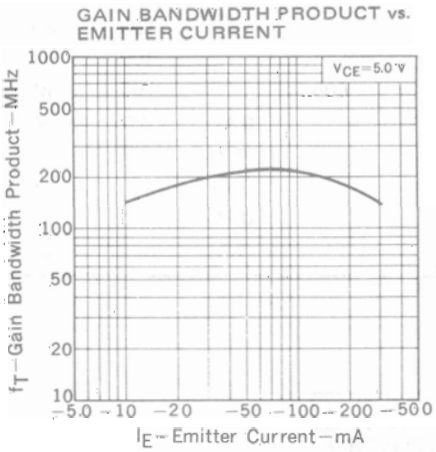
DC CURRENT GAIN vs. COLLECTOR CURRENT



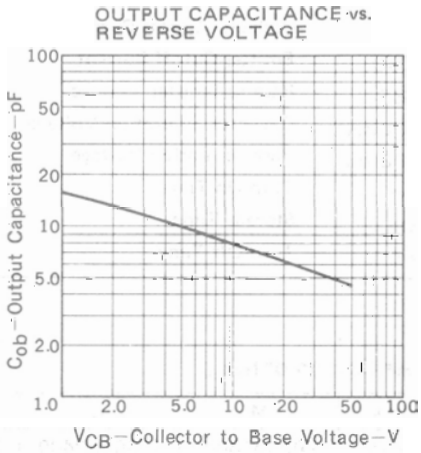
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



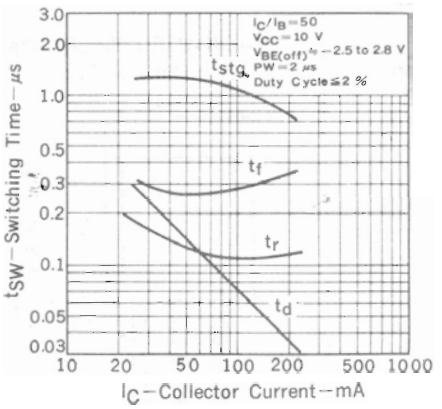
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR

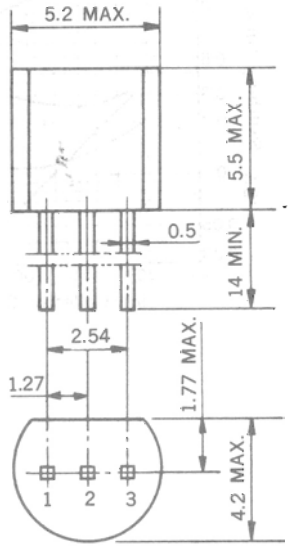
2SC3616

DESCRIPTION The 2SC3616 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving, instead of Darlington Transistor, or muting.

FEATURES

- High DC Current Gain.
  h_{FE} = 800 to 3200 (@ V_{CE} = 2.0 V, I_C = 300 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.14 V TYP. (@ I_C/I_B = 300 mA/3.0 mA)
- High V_{EBO} : V_{EBO} = 15V
- Large Current : $I_{C(DC)}$ = 700 mA, $I_{C(pulse)}$ = 1.0 A
- High Total Power Dissipation. : P_T = 0.75 W (T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector
3. Base

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	25	V
V_{CEO}	Collector to Emitter Voltage	25	V
V_{EBO}	Emitter to Base Voltage	15	V
I_C	Collector Current (DC)	700	mA
I_C	Collector Current (pulse)*	1.0	A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	800		3200	—	V_{CE} = 2.0 V, I_C = 300 mA
h_{FE2}**	DC Current Gain	640			—	V_{CE} = 2.0 V, I_C = 500 mA
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 5.0 V, I_E = −300 mA
C_{ob}	Output Capacitance		10		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 25 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}**	Base to Emitter Voltage	600		700	mV	V_{CE} = 2.0 V, I_C = 50 mA
$V_{CE(sat)}$**	Collector Saturation Voltage		0.14	0.3	V	I_C = 300 mA, I_B = 3.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.77	1.2	V	I_C = 300 mA, I_B = 3.0 mA
t_{on}	Turn-On Time		0.13		μs	(V_{CC} = 10 V, $V_{BE(off)}$ ≒ −2.7 V, I_C = 200 mA, $I_{B1} = -I_{B2}$ = 4.0 mA)
t_{stg}	Storage Time		0.90		μs	
t_{off}	Turn-Off Time		1.1		μs	

**Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

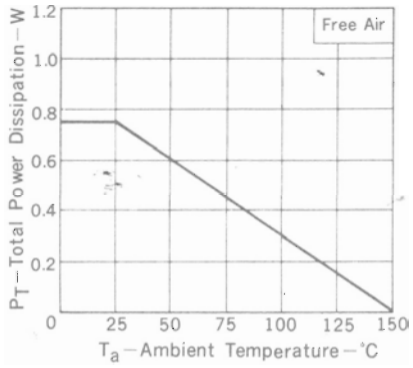
Classification of h_{FE1}

Rank	M	L	K
Range	800 to 1600	1200 to 2400	2000 to 3200

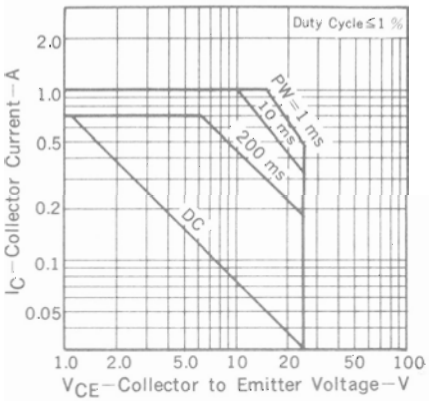
Test Conditions: V_{CE} = 2.0 V, I_C = 300 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

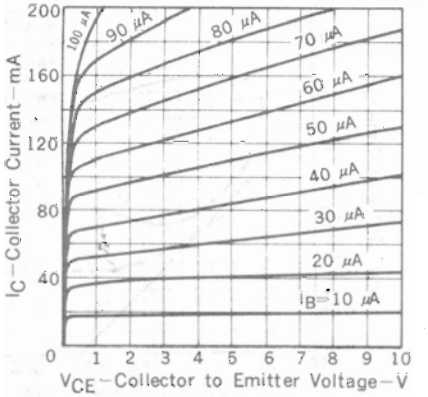
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



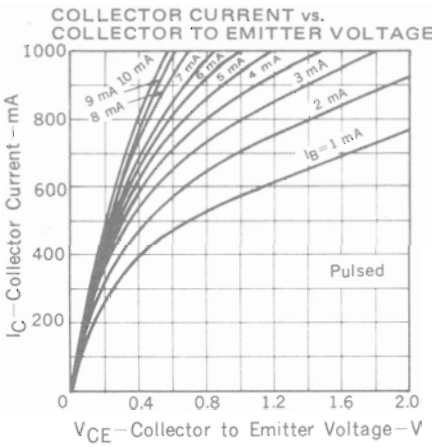
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



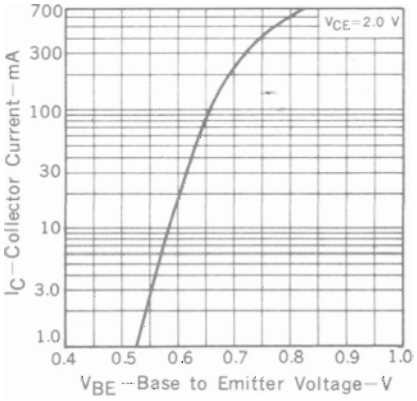
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



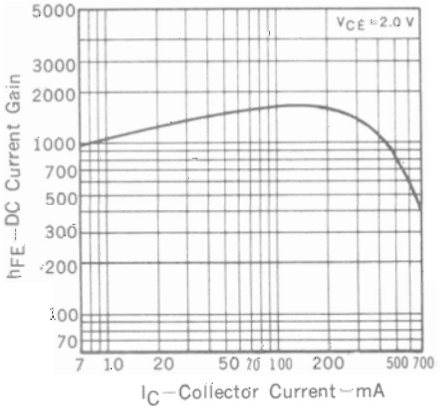
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



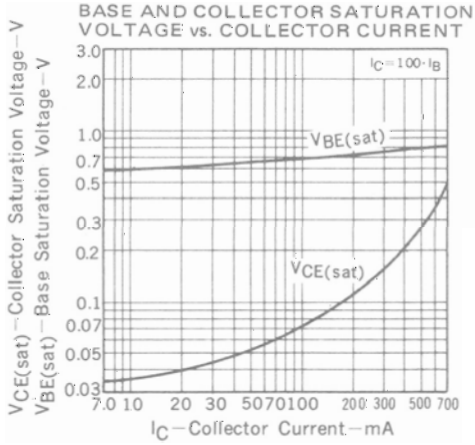
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



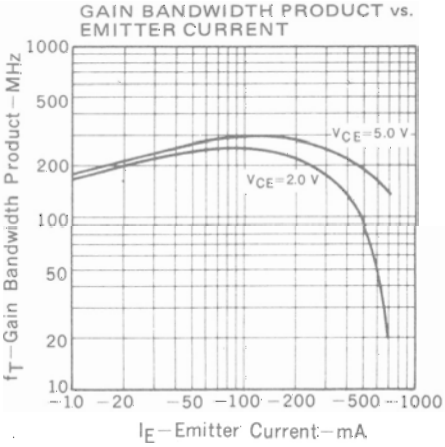
DC CURRENT GAIN vs. COLLECTOR CURRENT



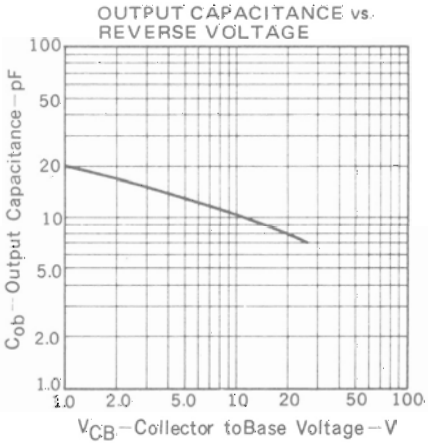
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



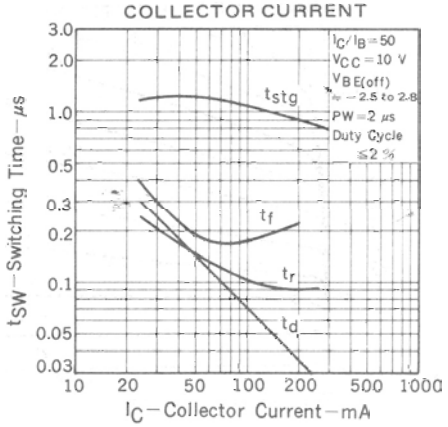
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

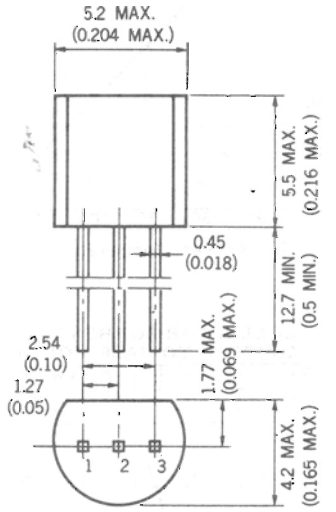
NPN SILICON TRANSISTOR
2SC3622

DESCRIPTION The 2SC3622 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving, instead of Darlington Transistor, or muting.

FEATURES

- High DC Current Gain.
  h_{FE} = 1000 to 3200 (@ V_{CE} = 5.0 V, I_C = 1.0 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.07 V TYP. (@ I_C = 50 mA, I_B = 5.0 mA)
- High V_{EBO} : $V_{EBO} > 12$ V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 12 V
- I_C Collector Current . . . . . 150 mA
- I_B Base Current. . . . . 10 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	1000	1800	3200	–	V_{CE} = 5.0 V, I_C = 1.0 mA
h_{FE2}*	DC Current Gain	200	350		–	V_{CE} = 5.0 V, I_C = 100 mA
f_T	Gain Bandwidth Product		250		MHz	V_{CE} = 5.0 V, I_E = −10 mA
C_{ob}	Output Capacitance		3.0		pF	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz
t_{on}	Turn-on Time		0.13		μs	V_{CC} = 10 V, $V_{BE(off)}$ = −2.7 V
t_f	Storage Time		0.72		μs	I_C = 50 mA
t_{off}	Turn-off Time		1.22		μs	$I_{B1} = -I_{B2}$ = 1.0 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}*	Base to Emitter Voltage		560		mV	V_{CE} = 5.0 V, I_C = 1.0 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.07	0.30	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.8	1.2	V	I_C = 50 mA, I_B = 5.0 mA

*Marked items are Pulse Test : PW 350 μs, Duty Cycle ≦ 2 %

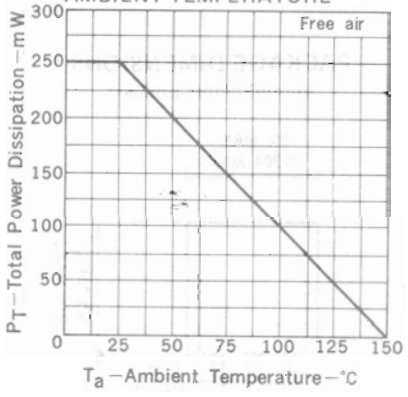
Classification of h_{FE1}

Rank	L	K
Range	1000 to 2000	1600 to 3200

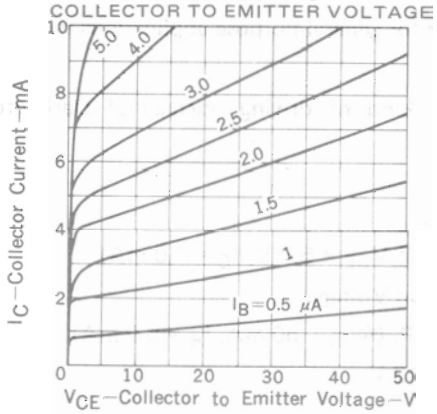
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

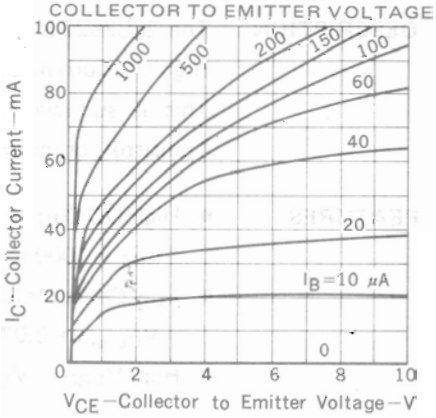
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



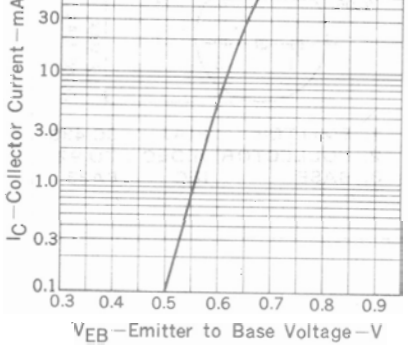
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



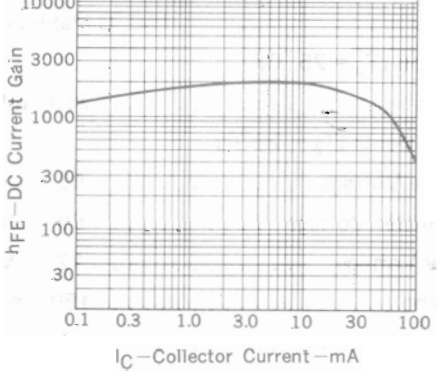
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



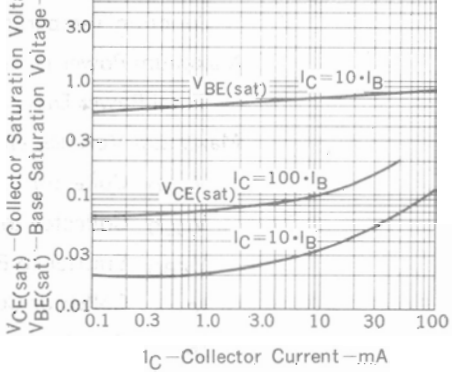
COLLECTOR CURRENT vs. EMITTER TO BASE VOLTAGE



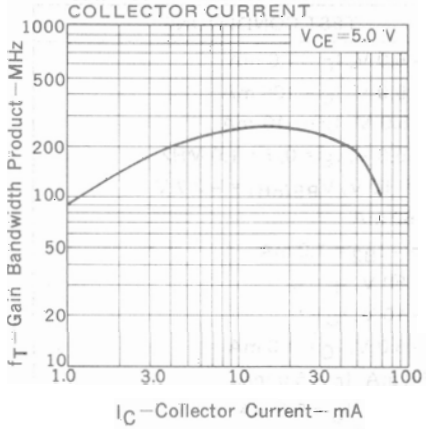
DC CURRENT GAIN vs. COLLECTOR CURRENT



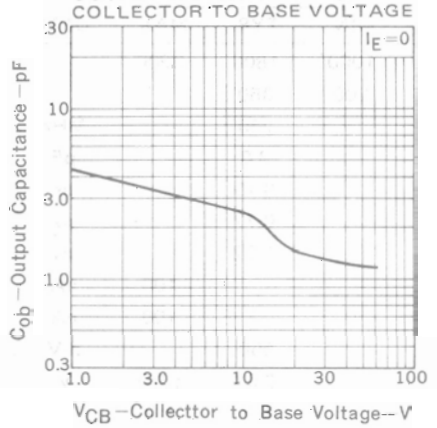
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



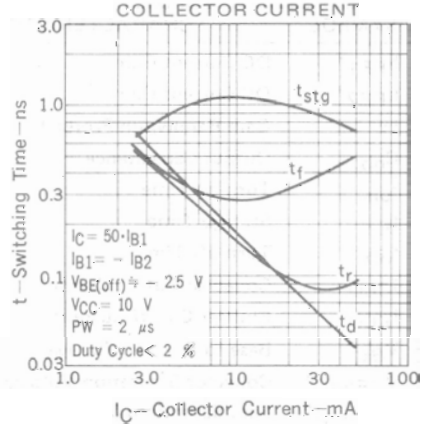
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

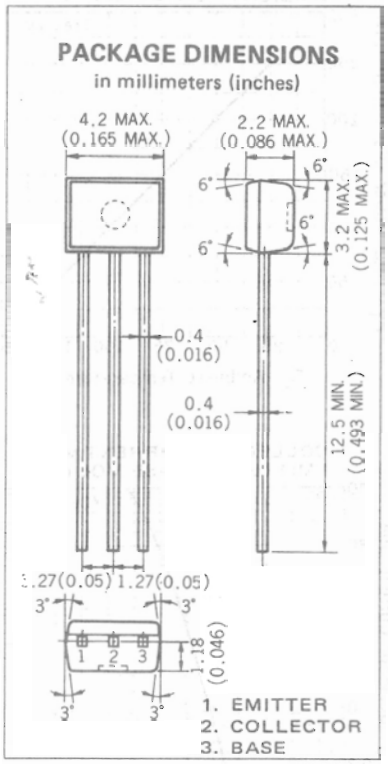
NPN SILICON TRANSISTOR
2SC3623

DESCRIPTION The 2SC3623 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving, instead of Darlington Transistor, or muting.

FEATURES

- High DC Current Gain.
  h_{FE} = 1000 to 3200 (@ V_{CE} = 5.0 V, I_C = 1.0 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.07 V TYP. (@ I_C = 50 mA, I_B = 5.0 mA)
- High V_{EBO} : V_{EBO} > 12 V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 12 V
- I_C Collector Current . . . . . 150 mA
- I_B Base Current. . . . . 10 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	1000	1800	3200	—	V_{CE} = 5.0 V, I_C = 1.0 mA
h_{FE2}*	DC Current Gain	200	350		—	V_{CE} = 5.0 V, I_C = 100 mA
f_T	Gain Bandwidth Product		250		MHz	V_{CE} = 5.0 V, I_C = −10 mA
C_{ob}	Output Capacitance		3.0		pF	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz
t_{on}	Turn-on Time		0.13		μs	V_{CC} = 10 V, $V_{BE(off)}$ = −2.7 V
t_f	Storage Time		0.72		μs	I_C = 50 mA
t_{off}	Turn-off Time		1.22		μs	I_{B1} = −I_{B2} = 1.0 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}*	Base to Emitter Voltage		560		mV	V_{CE} = 5.0 V, I_C = 1.0 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.07	0.30	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.8	1.2	V	I_C = 50 mA, I_B = 5.0 mA

*Marked items are Pulse Test : PW 350 μs
Duty Cycle ≦ 2 %

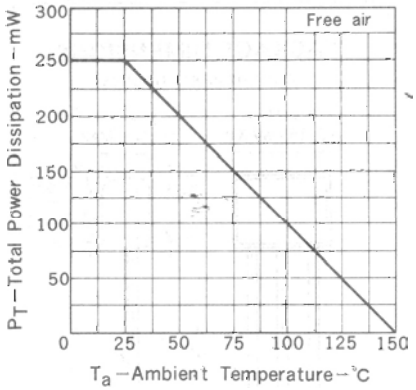
Classification of h_{FE1}

Rank	L	K
Range	1000 to 2000	1600 to 3200

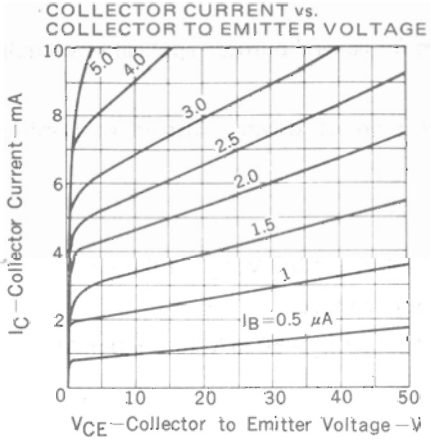
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

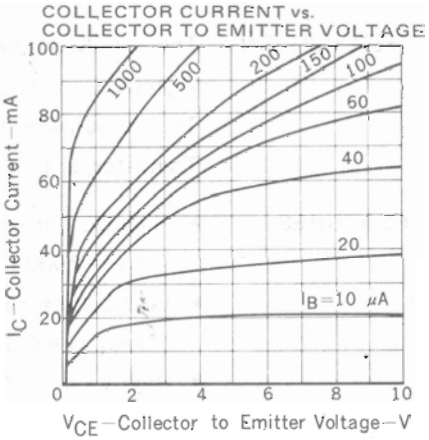
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



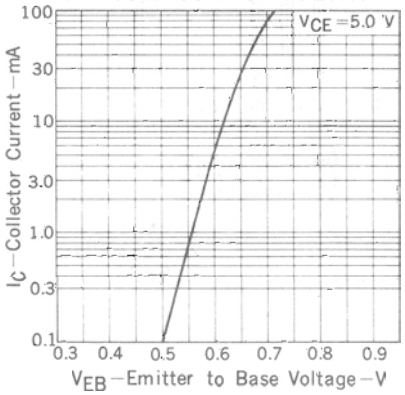
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



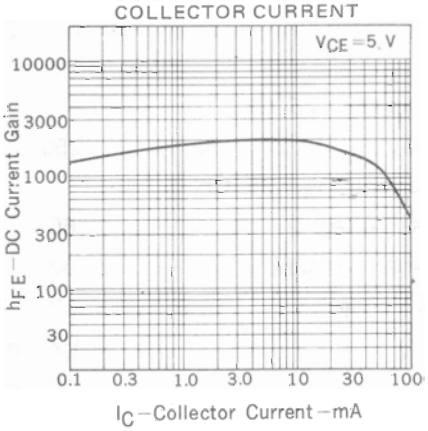
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



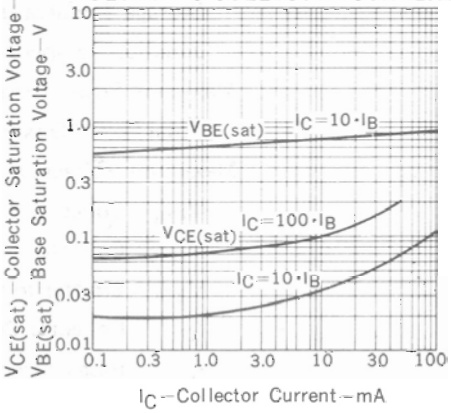
COLLECTOR CURRENT vs. EMITTER TO BASE VOLTAGE



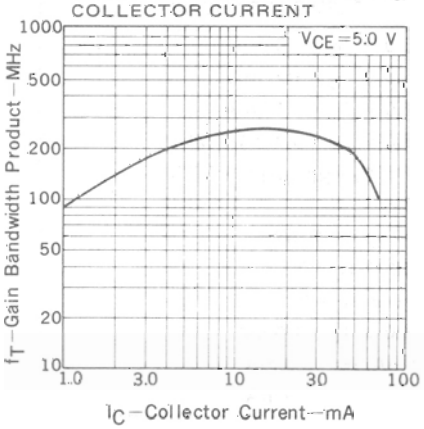
DC CURRENT GAIN vs. COLLECTOR CURRENT



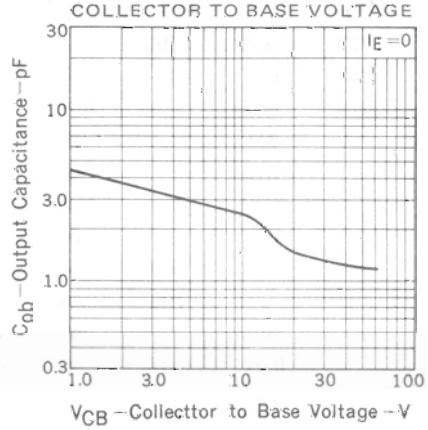
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



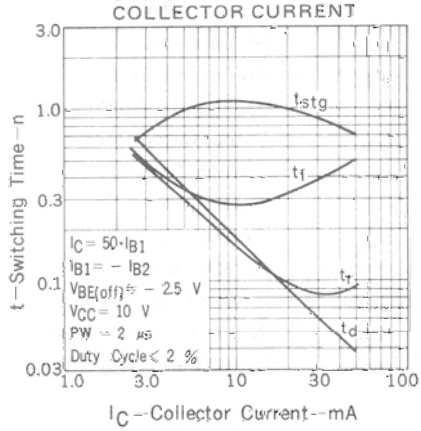
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

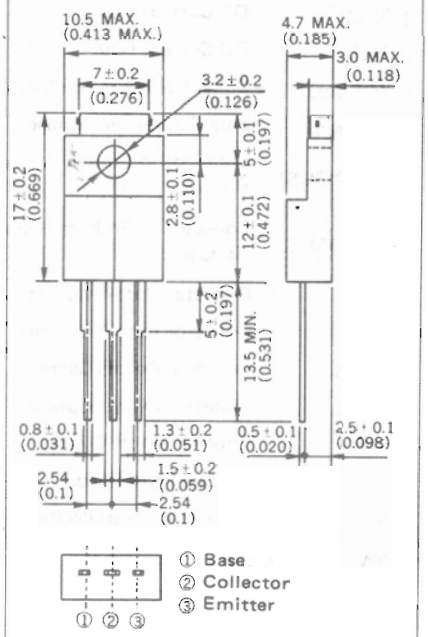
NPN SILICON POWER TRANSISTOR
2SC3691

DESCRIPTION The 2SC3691 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1441.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

Total Power Dissipation . . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	5.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	10	A
$I_{B(DC)}$	Base Current (DC)	2.5	A

* PW ≤ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.15 A R_L = 17 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = 2.0 V, I_C = 1.0 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = 2.0 V, I_C = 3.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			0.3	V	I_C = 3.0 A, I_B = 0.15 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 3.0 A, I_B = 0.15 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 3.0 A, I_B = 0.3 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 3.0 A, I_{B1} = −I_{B2} = 0.3 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0
C_{ob}	Output Capacitance		70		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		150		MHz	V_{CE} = 10 V, I_C = 0.5 A

* PW ≦ 350 μs, Duty Cycle ≦ 2 %

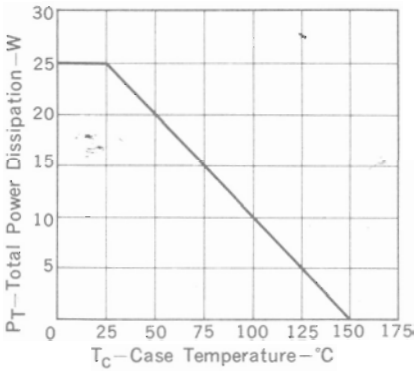
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

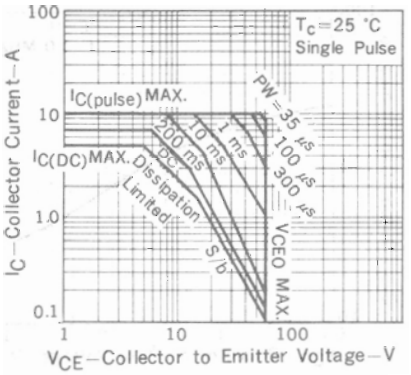
Test Conditions: V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

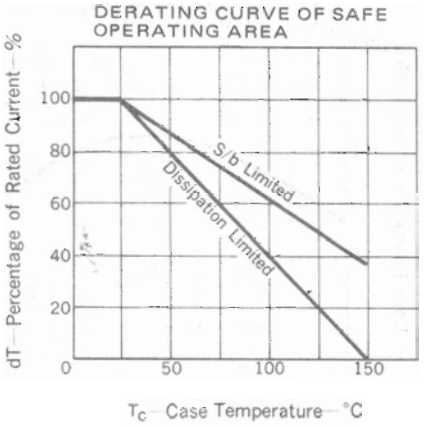
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



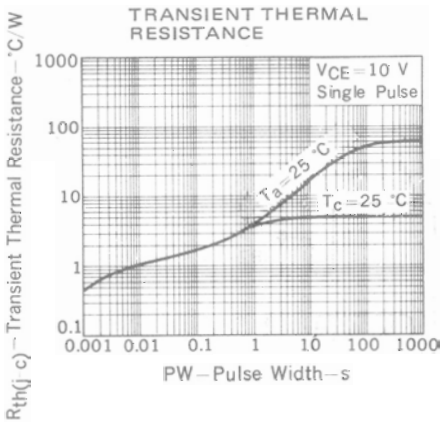
FORWARD BIAS SAFE OPERATING AREA



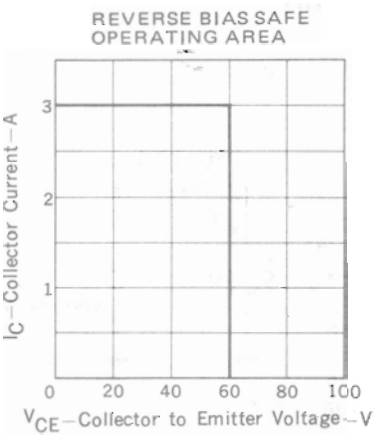
DERATING CURVE OF SAFE OPERATING AREA



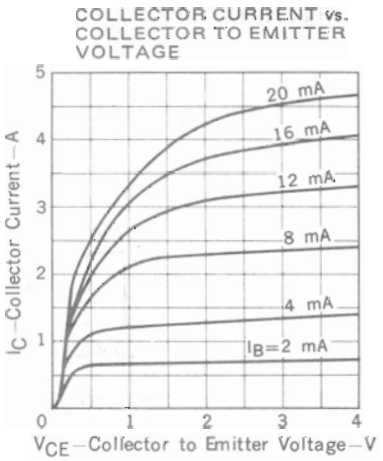
TRANSIENT THERMAL RESISTANCE



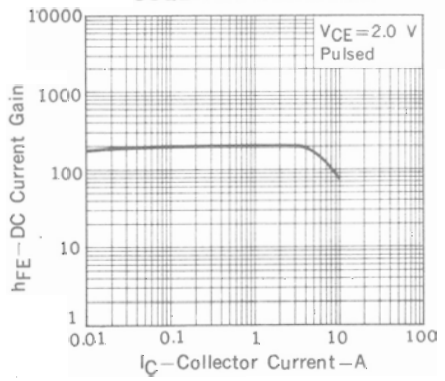
REVERSE BIAS SAFE OPERATING AREA



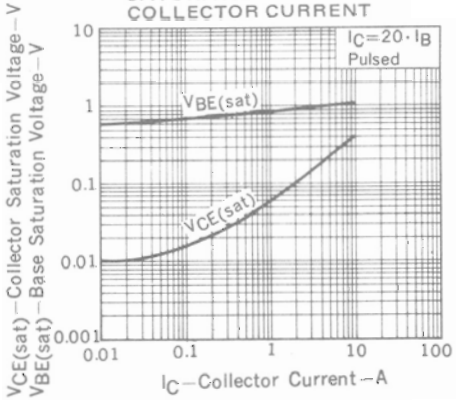
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



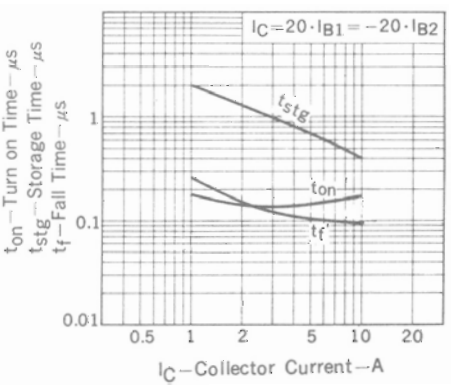
DC CURRENT GAIN vs. COLLECTOR CURRENT



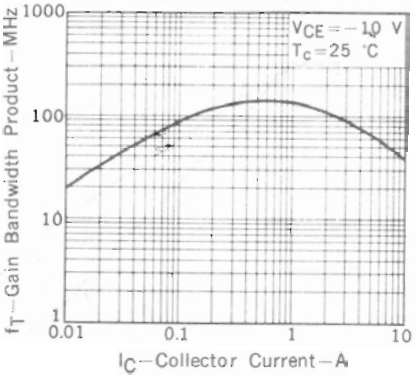
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



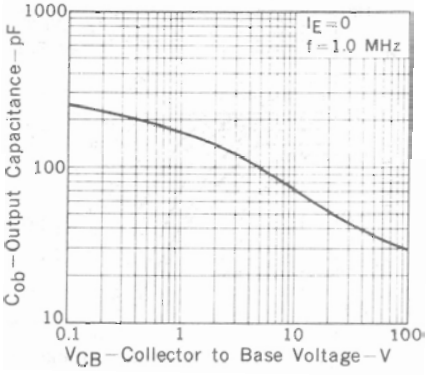
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



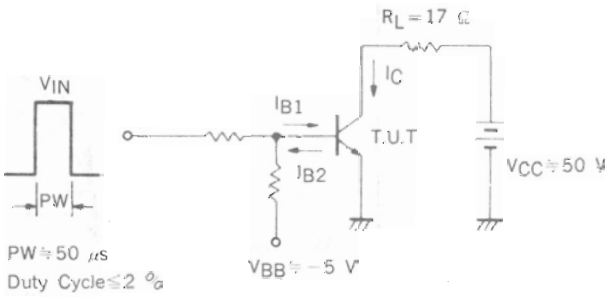
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

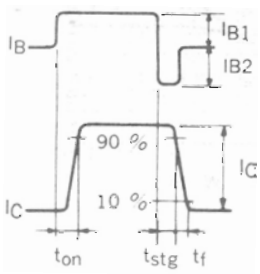


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

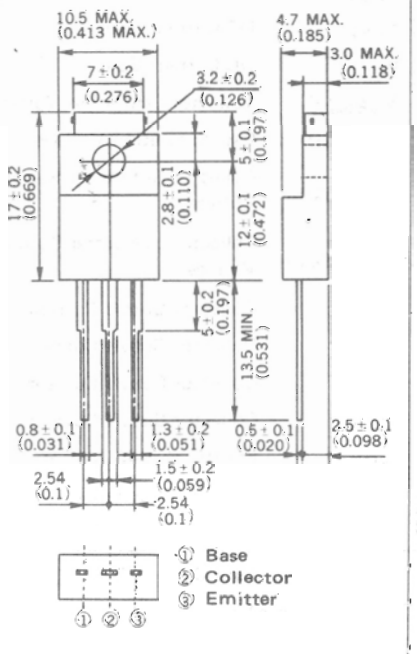
NPN SILICON POWER TRANSISTOR
2SC3692

DESCRIPTION The 2SC3692 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1442.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	7.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	14	A
$I_{B(DC)}$	Base Current (DC)	3.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = 4.0 A, I_{B1} = −I_{B2} = 0.2 A R_L = 12.5 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = 2.0 V, I_C = 0.2 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = 2.0 V, I_C = 1.5 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = 2.0 V, I_C = 4.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			0.3	V	I_C = 4.0 A, I_B = 0.2 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 4.0 A, I_B = 0.2 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 4.0 A, I_B = 0.4 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 4.0 A, I_{B1} = −I_{B2} = 0.4 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0
C_{ob}	Output Capacitance		100		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		150		MHz	V_{CE} = 10 V, I_C = 1.0 A

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

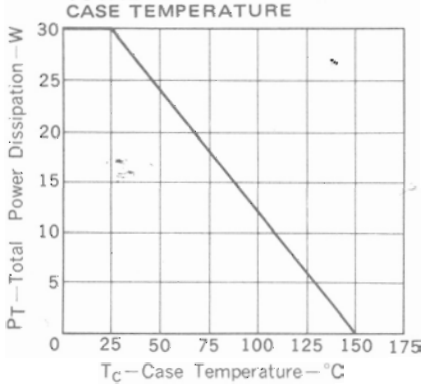
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

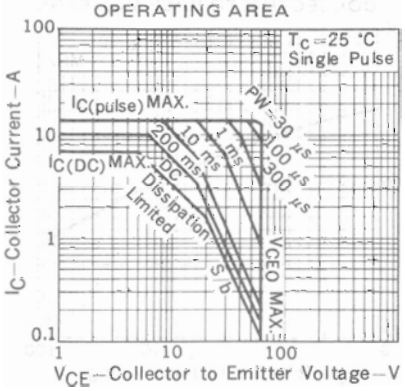
Test Conditions: V_{CE} = 2.0 V, I_C = 1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

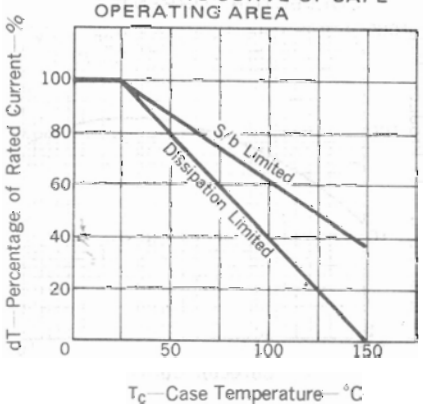
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



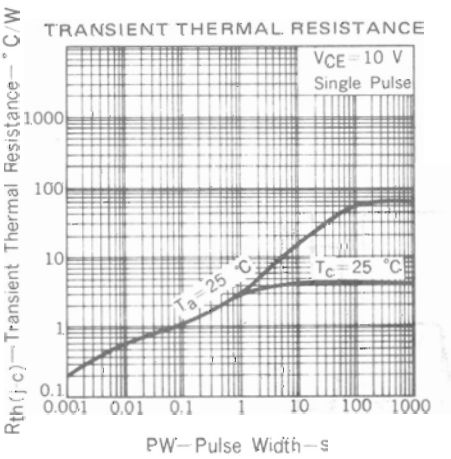
FORWARD BIAS SAFE OPERATING AREA



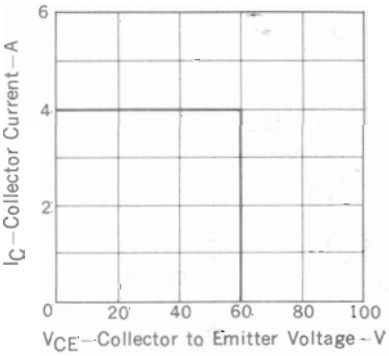
DERATING CURVE OF SAFE OPERATING AREA



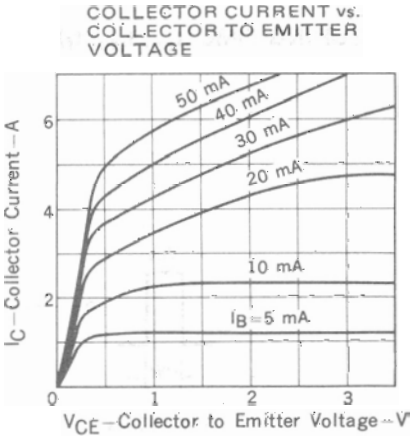
TRANSIENT THERMAL RESISTANCE



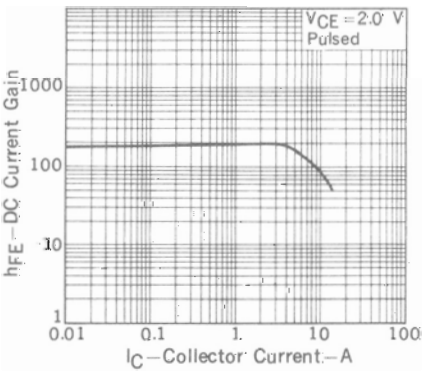
REVERSE BIAS SAFE OPERATING AREA



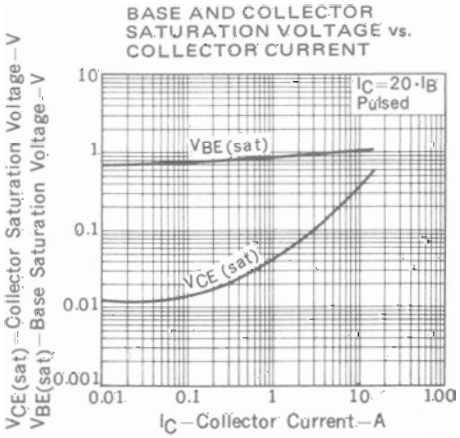
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



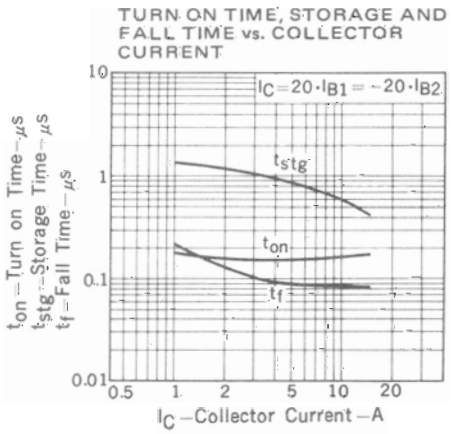
DC CURRENT GAIN vs. COLLECTOR CURRENT



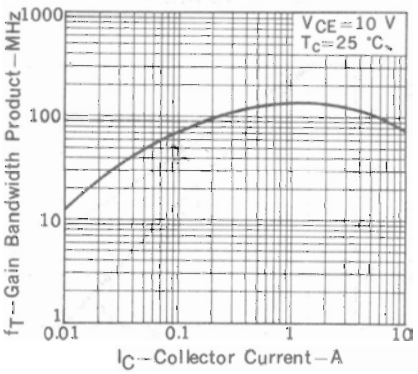
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



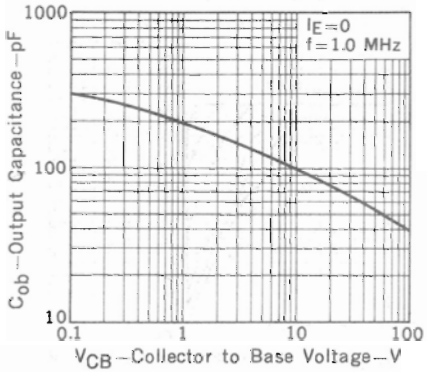
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



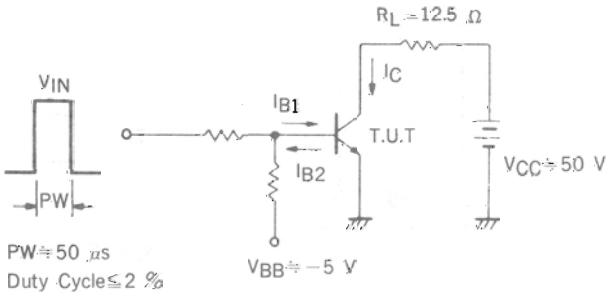
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

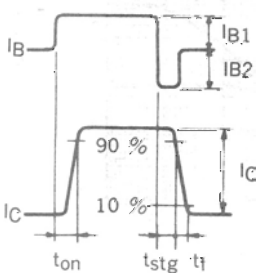


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

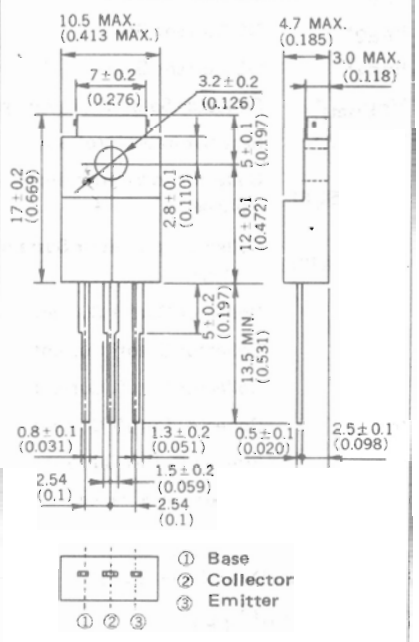
NPN SILICON POWER TRANSISTOR
2SC3693

DESCRIPTION The 2SC3693 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1443.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 Maximum	°C

Maximum Power Dissipation (T_C = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	10	A
$I_{C(pulse)}$	Collector Current (pulse)*	20	A
$I_{B(DC)}$	Base Current (DC)	5.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = 6.0 A, I_{B1} = −I_{B2} = 0.3 A R_L = 8.3 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = 2.0 V, I_C = 1.0 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = 2.0 V, I_C = 2.0 A
h_{FE3}*	DC Current Gain	100			—	V_{CE} = 2.0 V, I_C = 6.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			0.3	V	I_C = 6.0 A, I_B = 0.3 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 6.0 A, I_B = 0.3 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 6.0 A, I_B = 0.6 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 6.0 A, I_{B1} = −I_{B2} = 0.6 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0
C_{ob}	Output Capacitance		150		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		140		MHz	V_{CE} = 10 V, I_C = 1.0 A

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

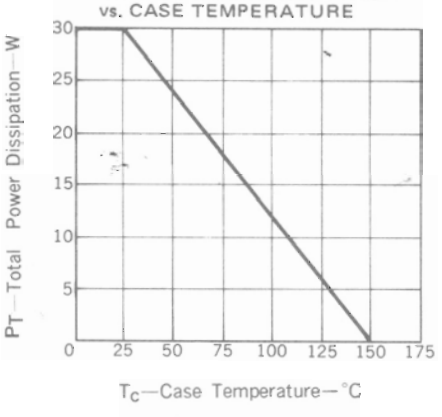
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

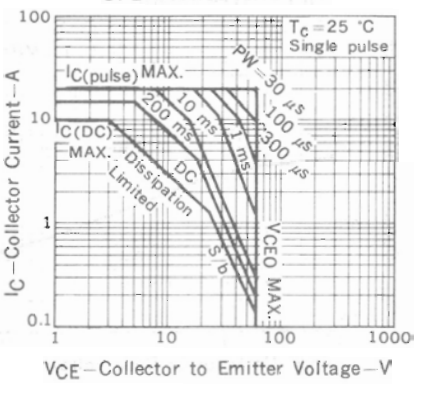
Test Conditions: V_{CE} = 2.0 V, I_C = 2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

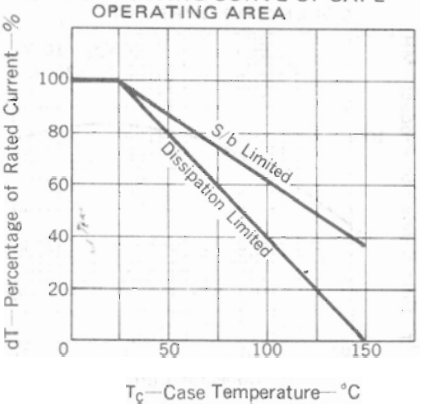
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



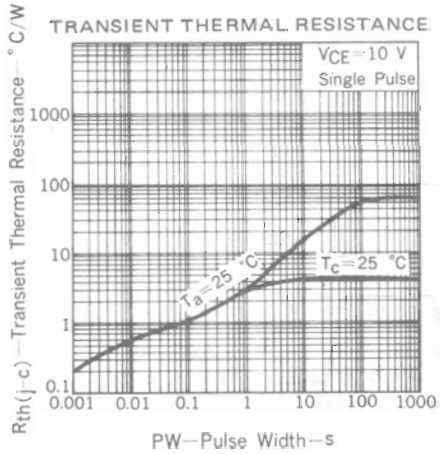
FORWARD BIAS SAFE OPERATING AREA



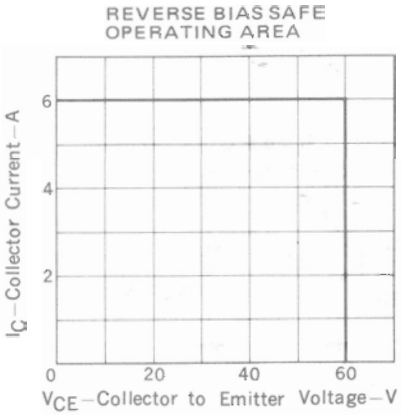
DERATING CURVE OF SAFE OPERATING AREA



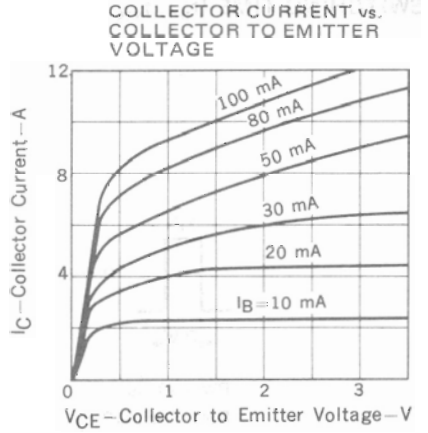
TRANSIENT THERMAL RESISTANCE



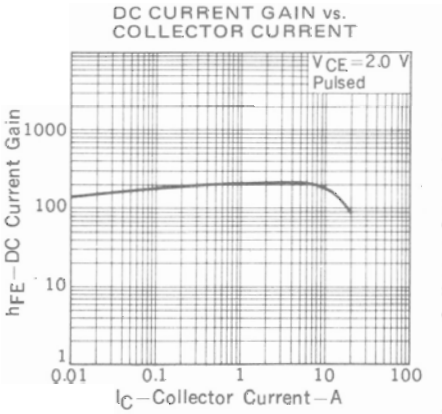
REVERSE BIAS SAFE OPERATING AREA



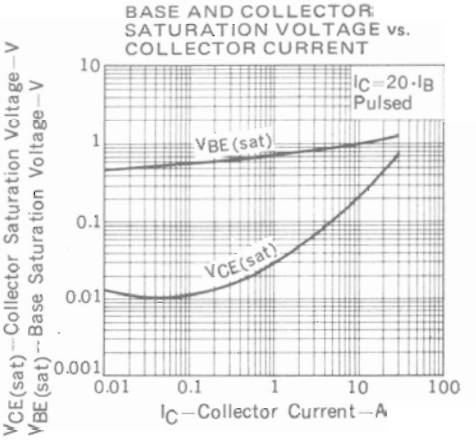
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



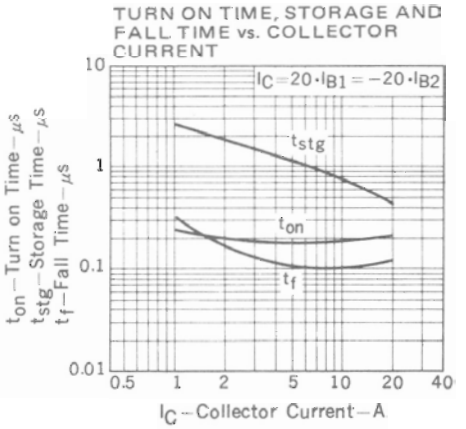
DC CURRENT GAIN vs. COLLECTOR CURRENT



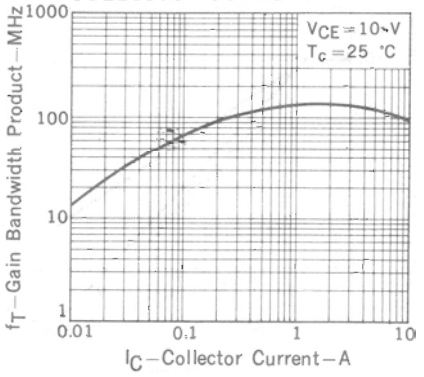
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



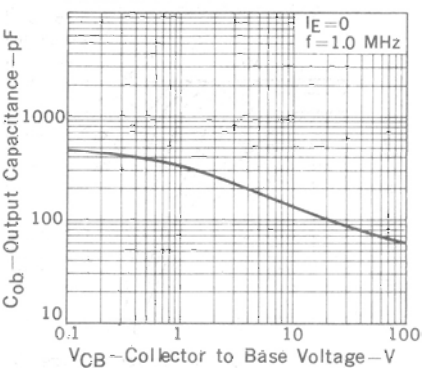
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



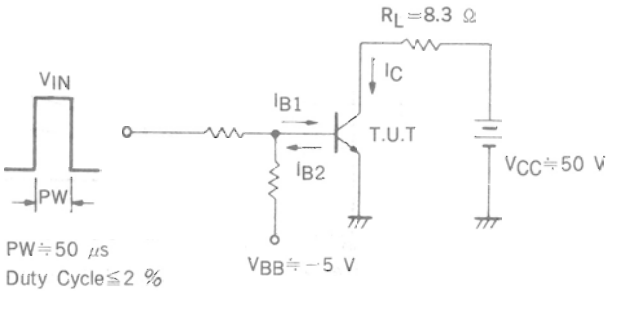
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

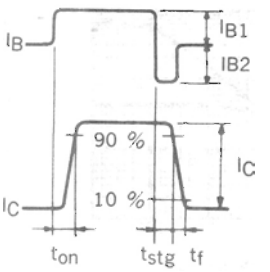


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

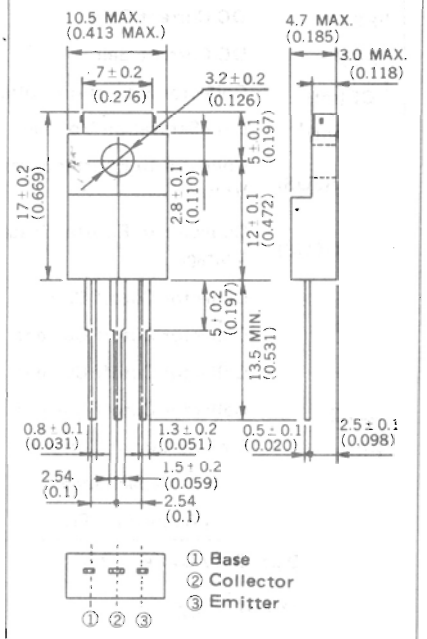
NPN SILICON POWER TRANSISTOR
2SC3694

DESCRIPTION The 2SC3694 is NPN silicon epitaxial transistor designed for switching regulator, DC-DC converter and high frequency power amplifier application.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Low Collector Saturation Voltage.
- High Switching Speed.
- Complementary to 2SA1444.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 Maximum	°C

Maximum Power Dissipation (T_c = 25 °C)

	Total Power Dissipation	30	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	15	A
$I_{C(pulse)}$	Collector Current (pulse)*	30	A
$I_{B(DC)}$	Base Current (DC)	7.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			0.3	μs	I_C = 8.0 A, I_{B1} = −I_{B2} = 0.4 A R_L = 6.3 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time			1.5	μs	
t_f	Fall Time			0.3	μs	
h_{FE1}*	DC Current Gain	100			—	V_{CE} = 2.0 V, I_C = 1.5 A
h_{FE2}*	DC Current Gain	100		400	—	V_{CE} = 2.0 V, I_C = 3.0 A
h_{FE3}*	DC Current Gain	60			—	V_{CE} = 2.0 V, I_C = 8.0 A
$V_{CE(sat)}$*	Collector Saturation Voltage			0.3	V	I_C = 8.0 A, I_B = 0.4 A
$V_{BE(sat)}$*	Base Saturation Voltage			1.2	V	I_C = 8.0 A, I_B = 0.4 A
$V_{CEO(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 8.0 A, I_B = 0.8 A, L = 1 mH
$V_{CEX(SUS)}$	Collector to Emitter Sustaining Voltage	60			V	I_C = 8.0 A, I_{B1} = −I_{B2} = 0.8 A, L = 180 μH, Clamped
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, R_{BE} = 50 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 60 V, $V_{BE(OFF)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0
C_{ob}	Output Capacitance		180		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product		120		MHz	V_{CE} = 10 V, I_C = 1.5 A

* PW ≤ 350 μs, Duty Cycle ≤ 2 %

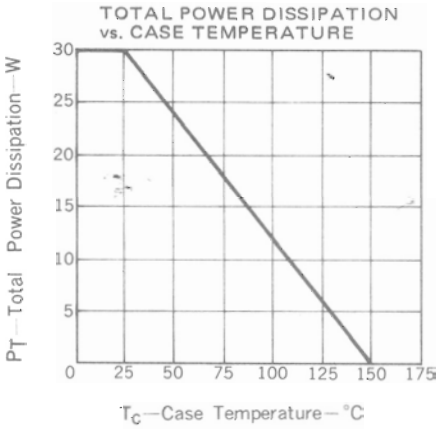
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	150 to 300	200 to 400

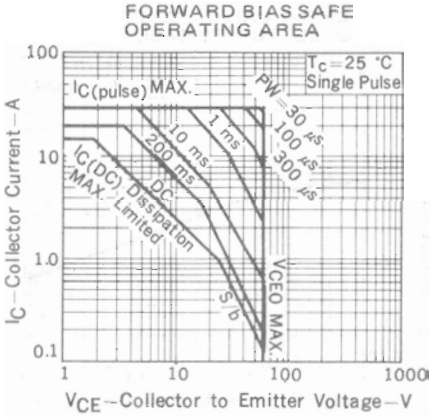
Test Conditions: V_{CE} = 2.0 V, I_C = 3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

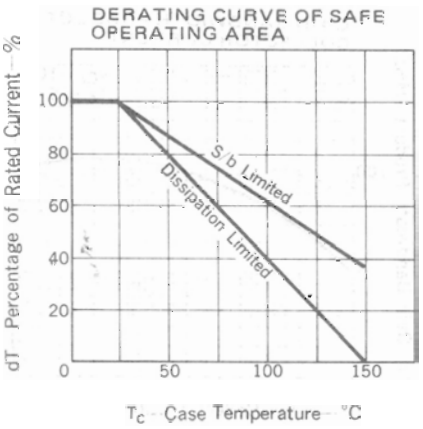
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



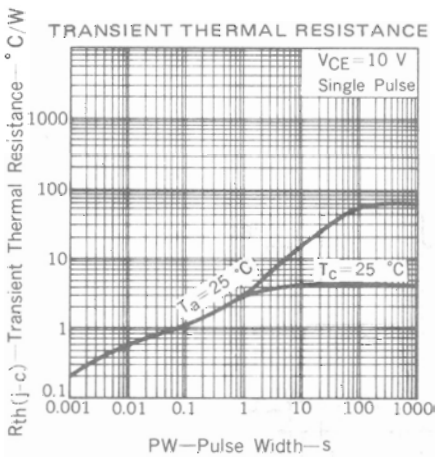
FORWARD BIAS SAFE OPERATING AREA



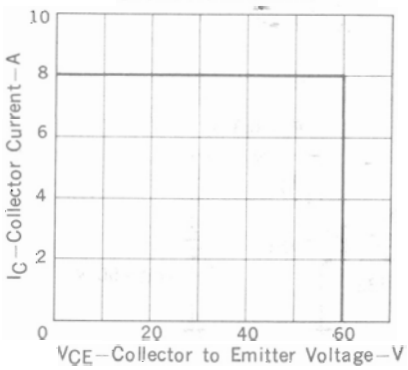
DERATING CURVE OF SAFE OPERATING AREA



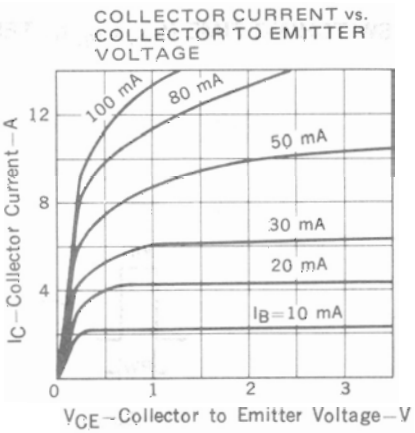
TRANSIENT THERMAL RESISTANCE



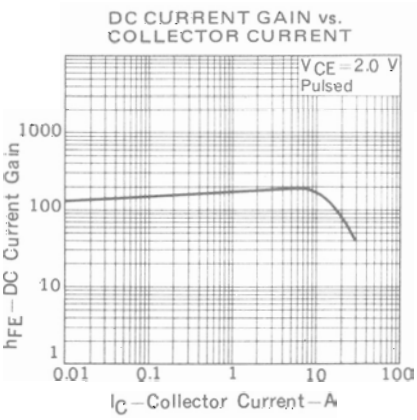
REVERSE BIAS SAFE OPERATING AREA



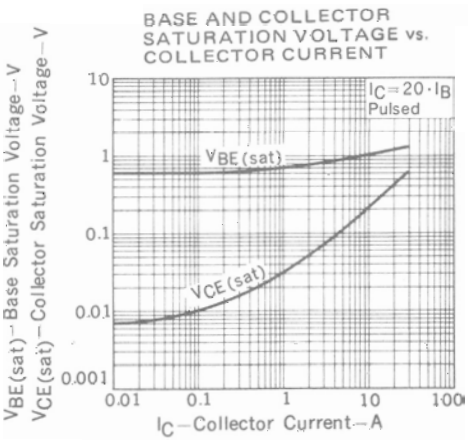
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



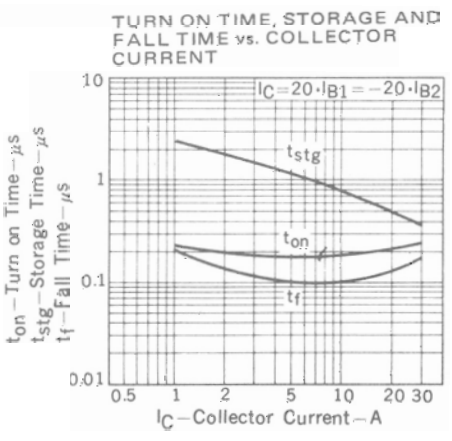
DC CURRENT GAIN vs. COLLECTOR CURRENT

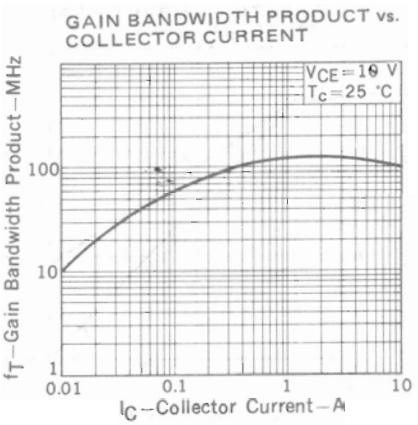


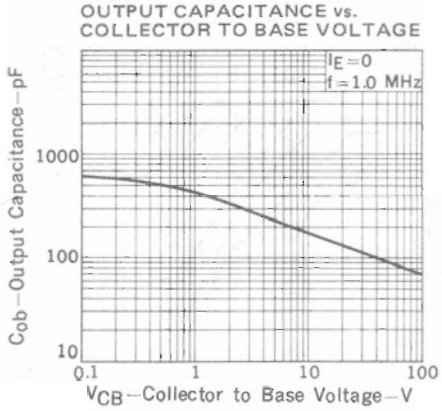
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



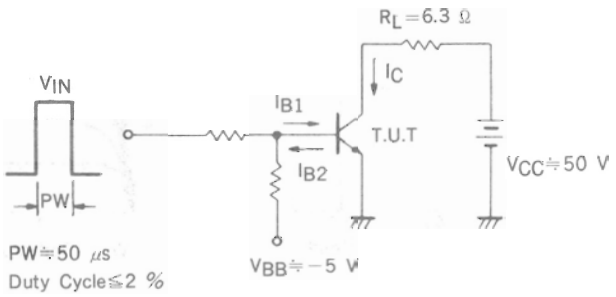
TURN ON TIME, STORAGE AND FALL TIME vs. COLLECTOR CURRENT

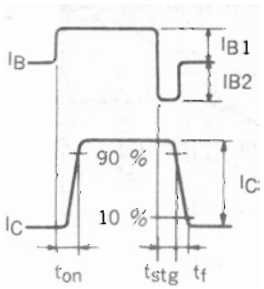






SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

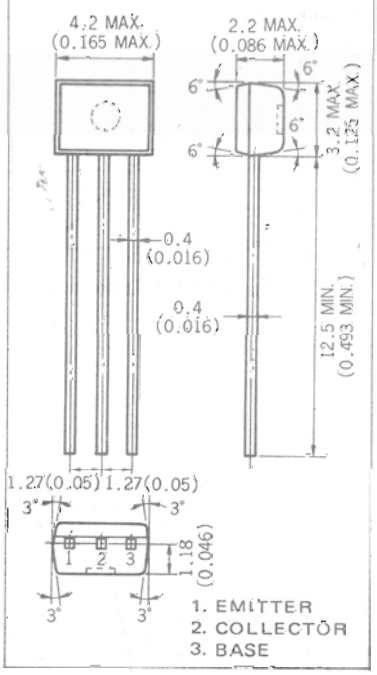
NPN SILICON TRANSISTOR
2SC3731

DESCRIPTION The 2SC3731 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.
- Complementary to the NEC 2SA1458 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	40	V
V_{EBO}	Emitter to Base Voltage	6.0	V
I_C	Collector Current	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			70	ns	See Test Circuit.
t_{stg}	Storage Time		100	200	ns	See Test Circuit.
t_{off}	Turn-off Time			250	ns	See Test Circuit.
f_T	Gain Bandwidth Product	300	510		MHz	V_{CE} = 20 V, I_E = −10 mA, f = 100 MHz
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB} = 5.0 V, I_E = 0, f = 1 MHz
h_{FE1}*	DC Current Gain	75	200	300	—	V_{CE} = 1.0 V, I_C = 10 mA
h_{FE2}*	DC Current Gain	25	80		—	V_{CE} = 1.0 V, I_C = 100 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.12	0.30	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.80	0.95	V	I_C = 50 mA, I_B = 5.0 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB} = 3.0 V, I_C = 0

* Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

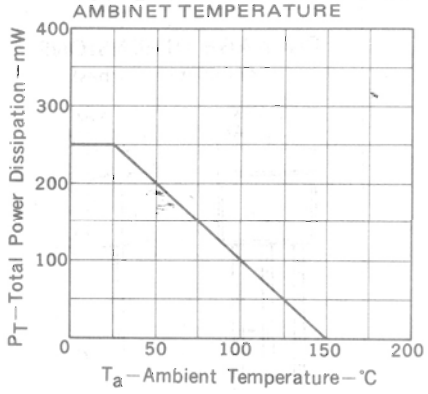
Classification of h_{FE1}

Rank	M	L	K
Range	75 to 150	100 to 200	150 to 300

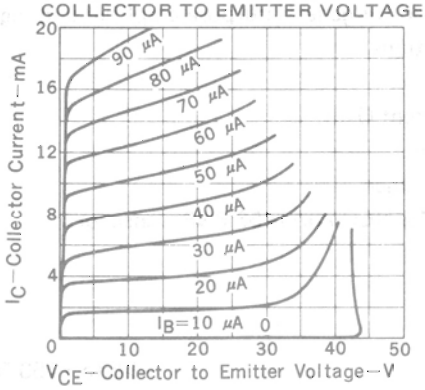
Test Conditions : V_{CE} = 1.0 V, I_C = 10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

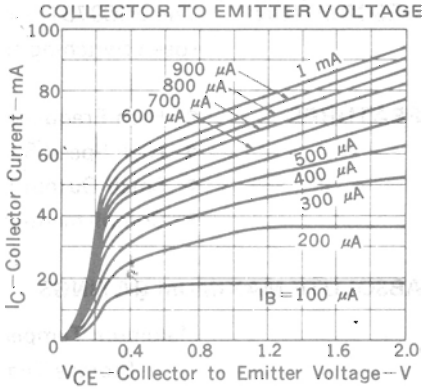
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



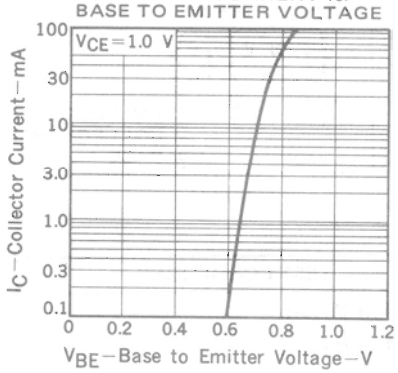
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



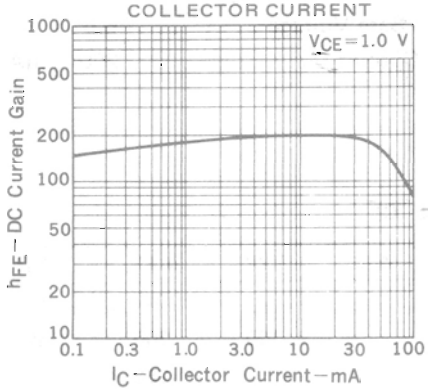
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



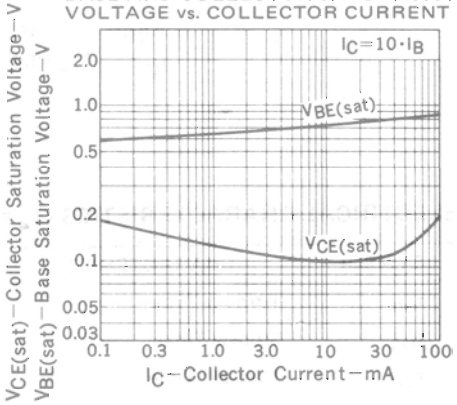
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



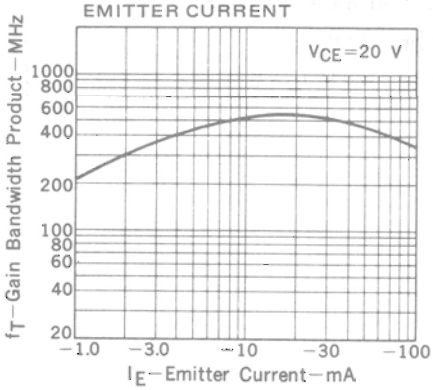
DC CURRENT GAIN vs. COLLECTOR CURRENT



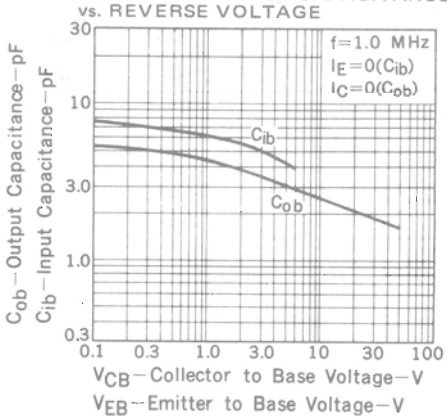
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



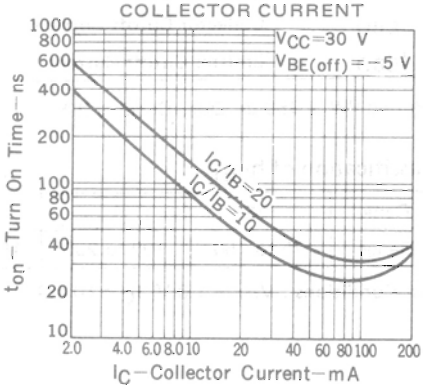
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



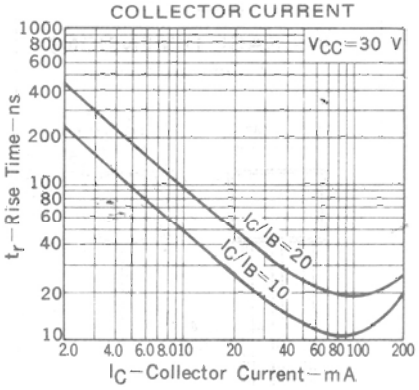
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



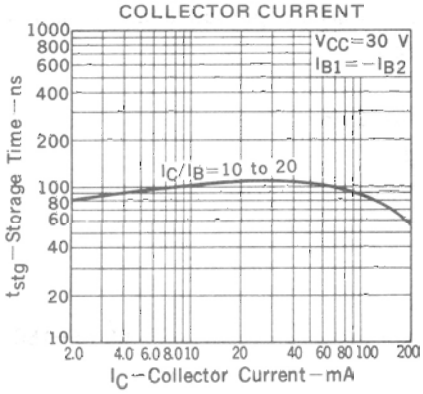
TURN ON TIME vs. COLLECTOR CURRENT



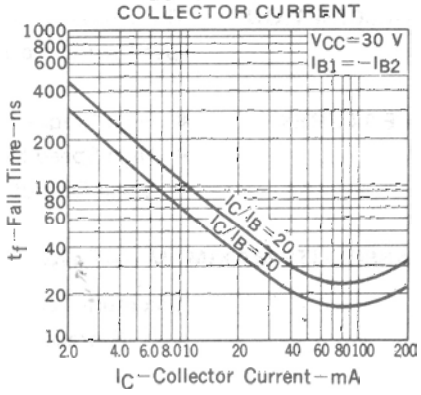
RISE TIME vs. COLLECTOR CURRENT



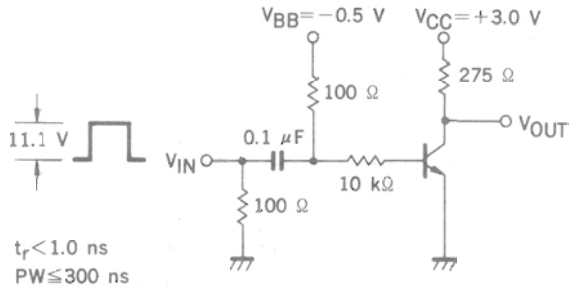
STORAGE TIME vs. COLLECTOR CURRENT



FALL TIME vs. COLLECTOR CURRENT

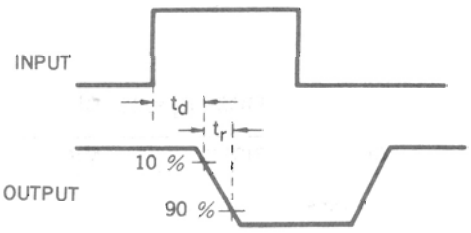


SWITCHING TIME TEST CIRCUIT

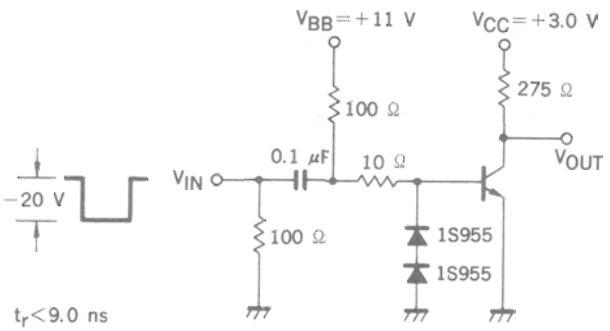


t_r<1.0 ns
PW≦300 ns
Duty Cycle=2 %

t_{on} SWITCHING

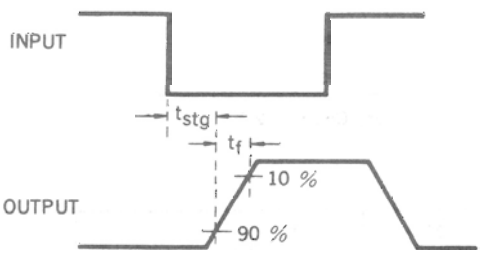


$t_{on}=t_d+t_r$



t_r<9.0 ns
PW≦300 ns
Duty Cycle=2 %

t_{off} SWITCHING



$t_{off}=t_{stg}+t_f$

NEC
ELECTRON DEVICE

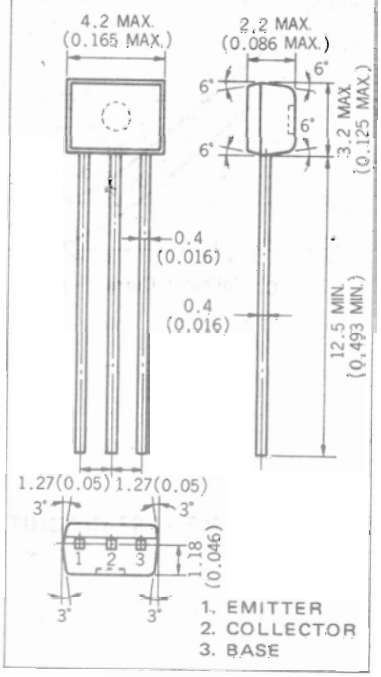
NPN SILICON TRANSISTOR
2SC3732

DESCRIPTION The 2SC3732 is designed for general purpose amplifier and high speed switching applications.

FEATURES

- High Frequency Current Gain.
- High Speed Switching.
- Small Output Capacitance.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

	Storage Temperature	−55 to +150	°C
	Junction Temperature	150 °C Maximum	

Maximum Power Dissipation (T_a = 25 °C)

	Total Power Dissipation	250	mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	40	V
V_{CES}	Collector to Emitter Voltage	40	V
V_{CEO}	Collector to Emitter Voltage	15	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	200	mA
I_C	Collector Current (10 μs pulse)	500	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time		8.0	12	ns	V_{CC} = 3.0 V, I_C = 10 mA, I_{B1} = 3.0 mA, V_{BE} = −1.5 V
t_{off}	Turn-off Time		12	18	ns	V_{CC} = 3.0 V, I_C = 10 mA, I_{B1} = 3.0 mA, I_{B2} = −1.5 mA
t_{stg}	Storage Time		6.0	13	ns	I_C = 10 mA, I_{B1} = $-I_{B2}$ = 10 mA
f_T	Gain Bandwith Product	500	750		MHz	V_{CE} = 10 V, I_E = −10 mA, f = 100 MHz
C_{ob}	Output Capacitance		1.8	4.0	pF	V_{CB} = 5.0 V, I_E = 0, f = 1 MHz
h_{FE}*	DC Current Gain	40	90	200	—	V_{CE} = 1.0 V, I_C = 10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.15	0.25	V	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.80	0.85	V	I_C = 10 mA, I_B = 1.0 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 20 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB} = 3.0 V, I_C = 0

* Pulsed PW ≤ 350 μs, Duty Cycle ≤ 2 %

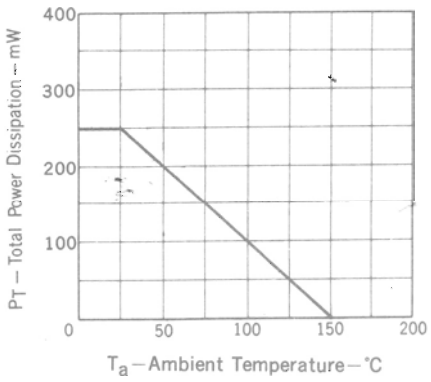
Classification of h_{FE}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

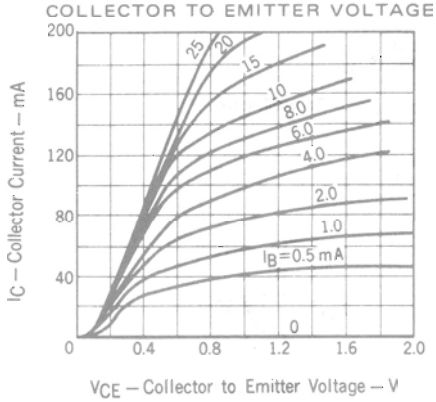
Test Conditions : V_{CE} = 1.0 V, I_C = 10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

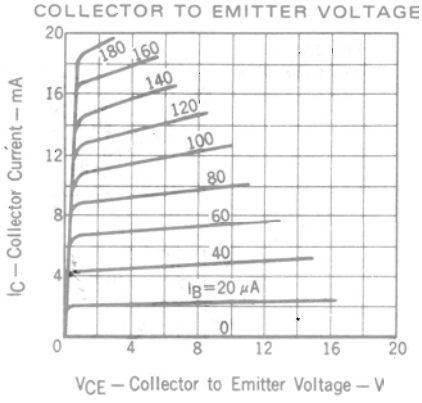
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



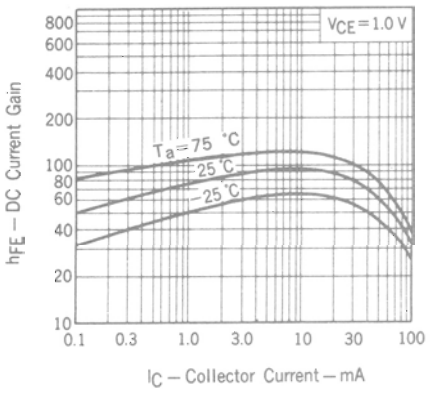
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



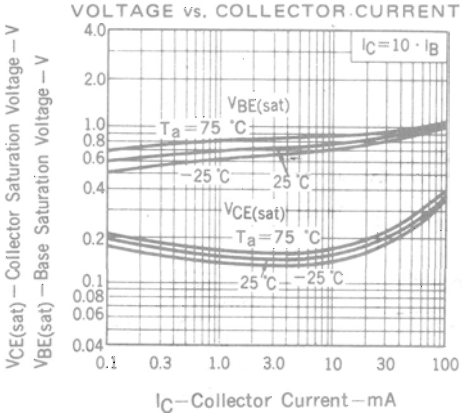
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



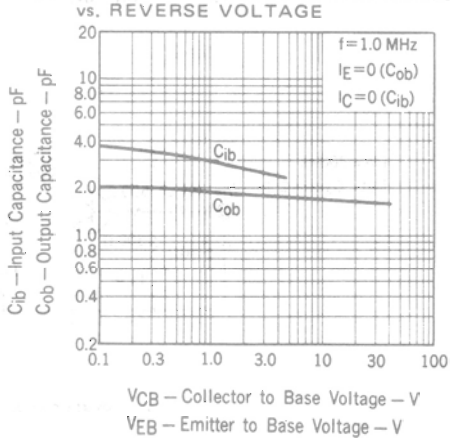
DC CURRENT GAIN vs. COLLECTOR CURRENT



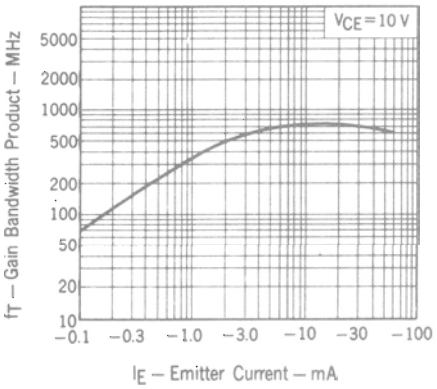
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



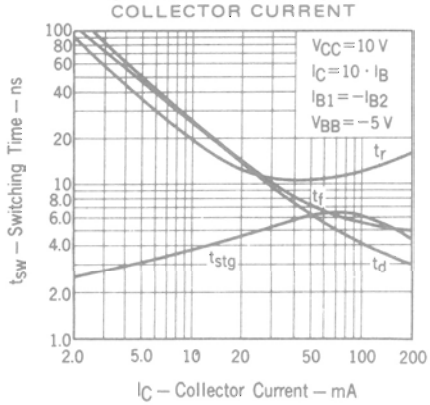
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



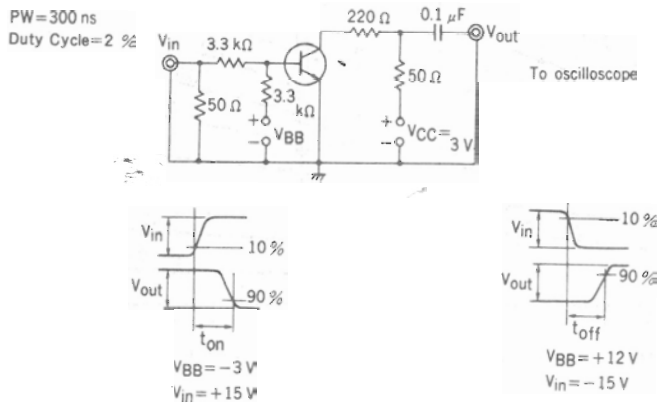
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



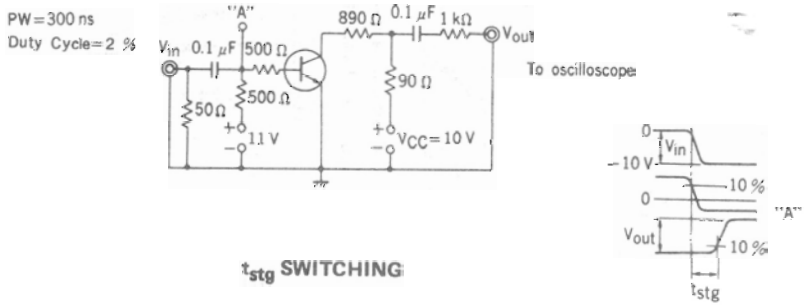
SWITCHING TIME vs. COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT



t_{on}, t_{off} SWITCHING



t_{stg} SWITCHING

Voltage waveforms

NEC
ELECTRON DEVICE

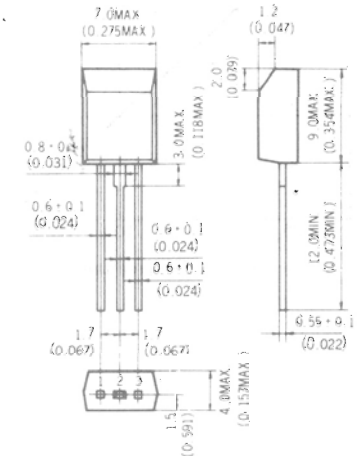
NPN SILICON TRANSISTOR
2SC3733

DESCRIPTION The 2SC3733 is designed for power amplifier and high speed switching applications.

FEATURES

- High speed, high voltage switching.
- Low Collector Saturation Voltage.
- Complementary to the NEC 2SA1460 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage . . .	80	V
V_{CEO}	Collector to Emitter Voltage .	45	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	1.0	A
$I_{C(pulse)}$	Collector Current (pulse)* . .	2.0	A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time		20	40	ns	V_{CC} = 10 V I_C = 500 mA $I_{B1} = -I_{B2} \fallingdotseq$ 50 mA
t_{off}	Turn-off Time		72	110	ns	
t_{stg}	Storage Time		55	80	ns	
f_T	Gain Bandwidth Product	300	380		MHz	V_{CE} = 10 V, I_E = −100 mA
C_{ob}	Output Capacitance		1.8	10	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz
h_{FE1}**	DC Current Gain	60	120	200	—	V_{CE} = 10 V, I_C = 50 mA
h_{FE2}**	DC Current Gain	60	150		—	V_{CE} = 10 V, I_C = 500 mA
$V_{CE(sat)}$**	Collector Saturation Voltage		0.17	0.40	V	I_C = 500 mA, I_B = 50 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.90	1.20	V	I_C = 500 mA, I_B = 50 mA
I_{CES}	Collector Cutoff Current			0.1	μA	V_{CE} = 45 V, R_{BE} = 0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB} = 4.0 V, I_C = 0

** Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

Classification of h_{FE1}

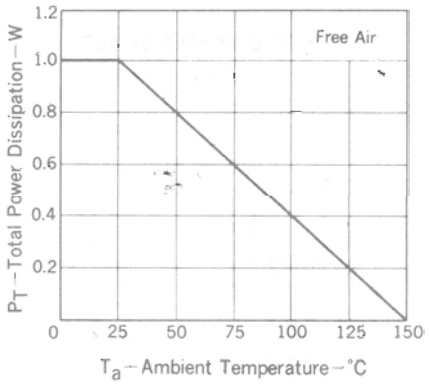
Rank	L	K
Range	60 to 120	100 to 200

Test Conditions : V_{CE} = 10 V, I_C = 50 mA

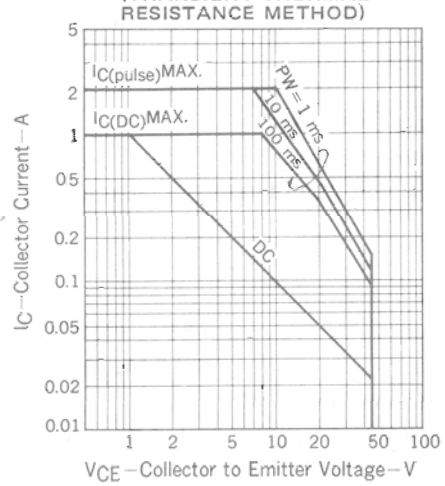
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

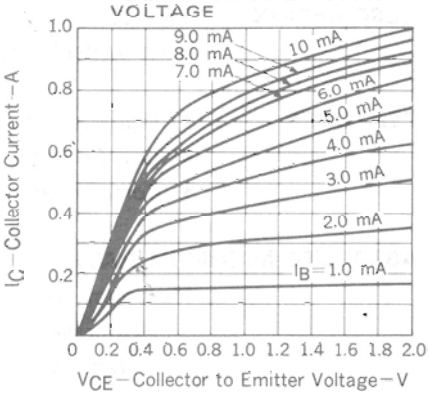
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



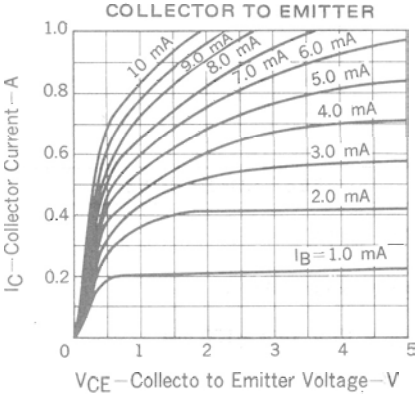
SAFE OPERATING AREA (TRANSIENT THERMAL RESISTANCE METHOD)



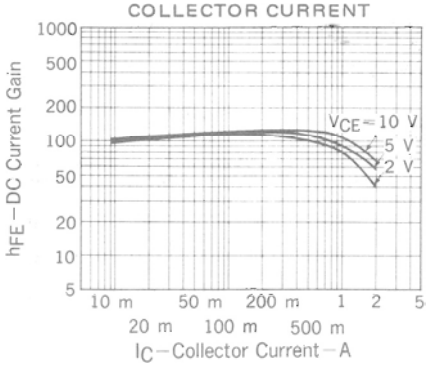
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



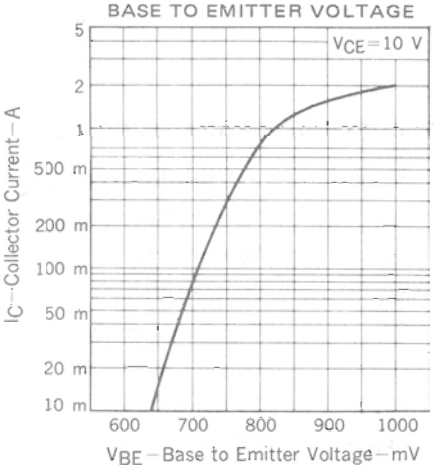
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER



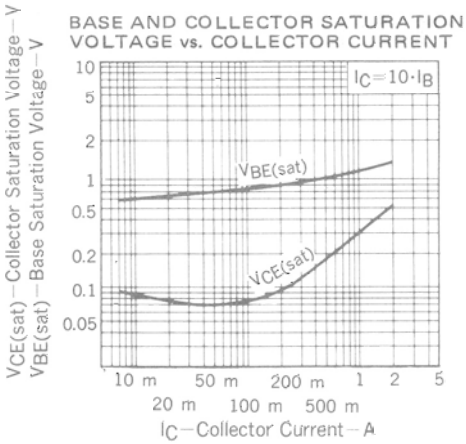
DC CURRENT GAIN vs. COLLECTOR CURRENT



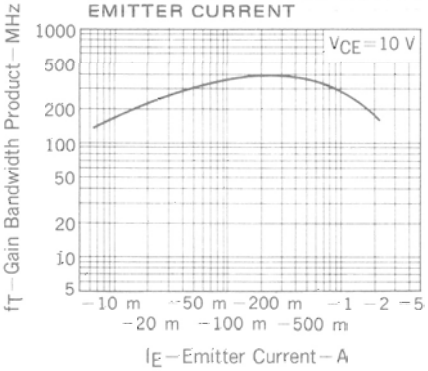
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



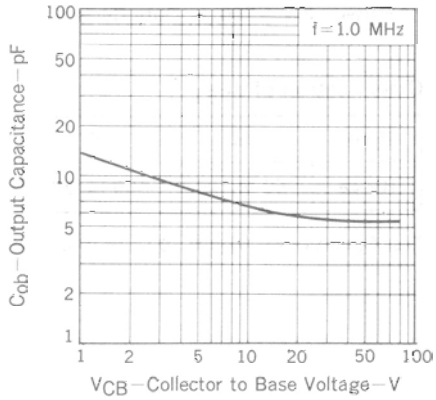
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



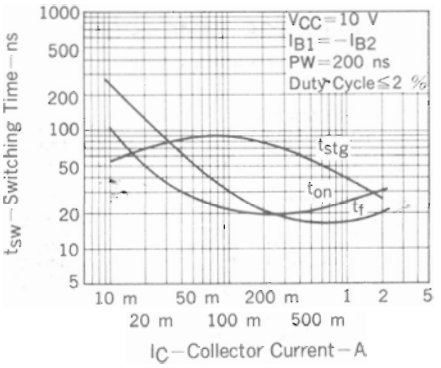
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



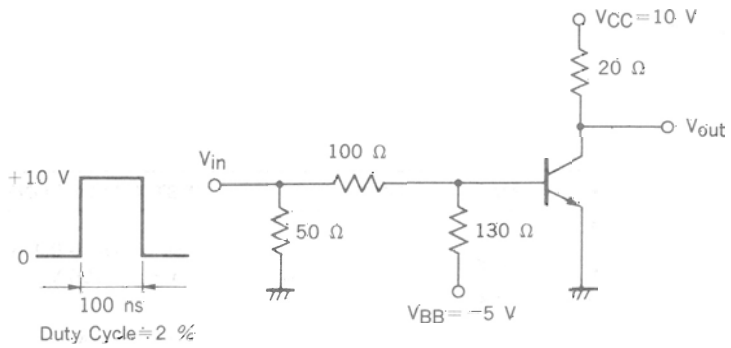
OUTPUT CAPACITANCE vs. REVERSE VOLTAGE

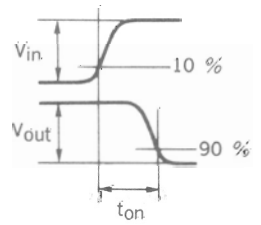


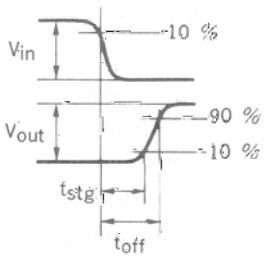
SWITCHING TIME vs. COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT







NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SC3840

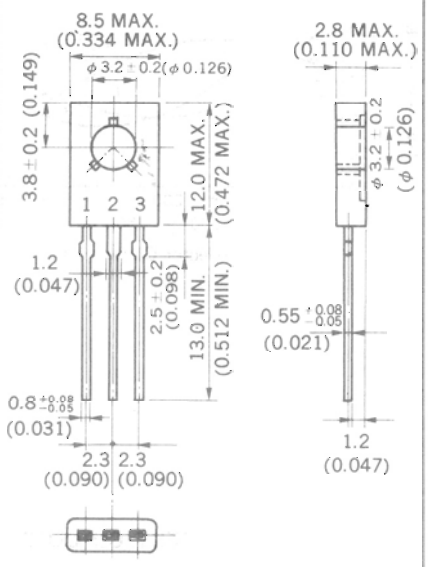
NEW DEVICE

DESCRIPTION The 2SC3840 is designed for use in high speed and high voltage. It is suitable for switching regulators, DC-DC converters and ultrasonic appliance applications.

FEATURES

- High speed switching
- High Voltage

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane.
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	600	V
V_{CEO}	Collector to Emitter Voltage . .	600	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	1.0	A
$I_{C(pulse)}$	Collector Current (Pulse)* . . .	2.0	A

*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-On Time		0.1	0.5	μs	I_C = 0.5 A, I_{B1} = −I_{B2} = 0.1 A R_L = 500 Ω, V_{CC} ≒ 250 V
t_{stg}	Storage Time		4.0	5.0	μs	
t_f	Fall Time		0.2	0.5	μs	
h_{FE1}**	DC Current Gain	30		120	—	V_{CE} = 5.0 V, I_C = 0.1 A
h_{FE2}**	DC Current Gain	5			—	V_{CE} = 5.0 V, I_C = 0.5 A
$V_{CE(sat)}$**	Collector Saturation Voltage			1.0	V	I_C = 0.4 A, I_B = 0.08 A
$V_{BE(sat)}$**	Base Saturation Voltage			1.2	V	I_C = 0.4 A, I_B = 0.08 A
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 600 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0

**Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

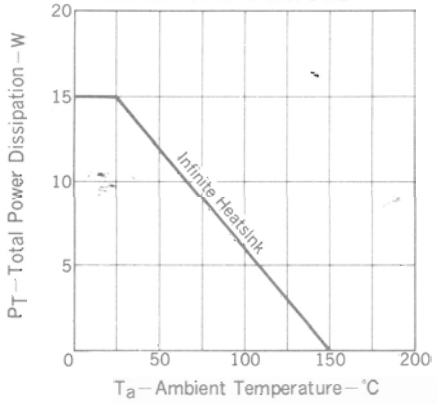
Classification of h_{FE1}

Rank	M	L	K
Range	30 to 60	40 to 80	60 to 120

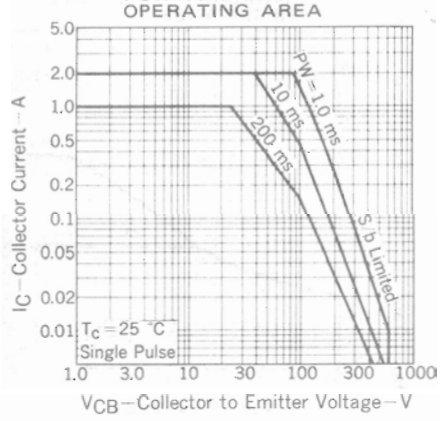
Test Conditions: V_{CE} = 5.0 V, I_C = 0.1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

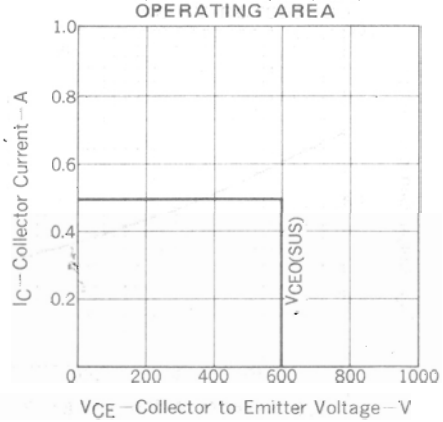
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



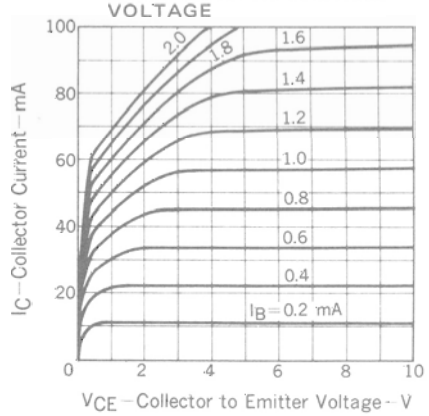
FORWARD BIAS SAFE OPERATING AREA



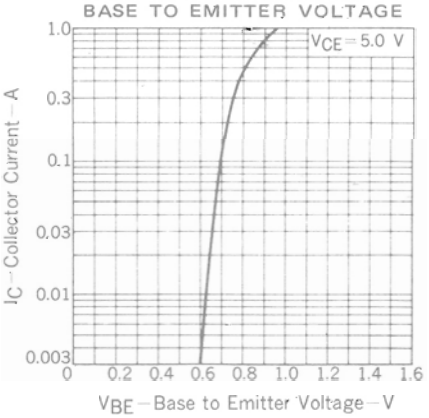
REVERSE BIAS SAFE OPERATING AREA



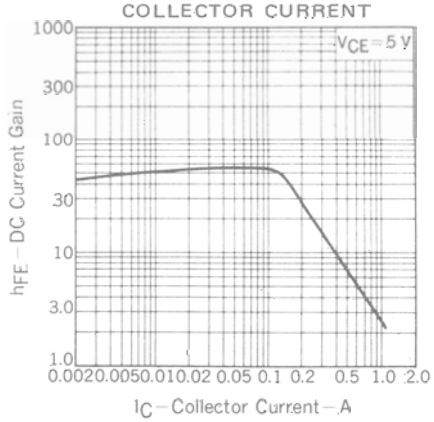
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



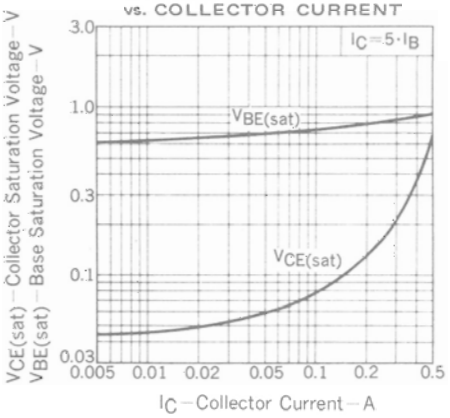
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



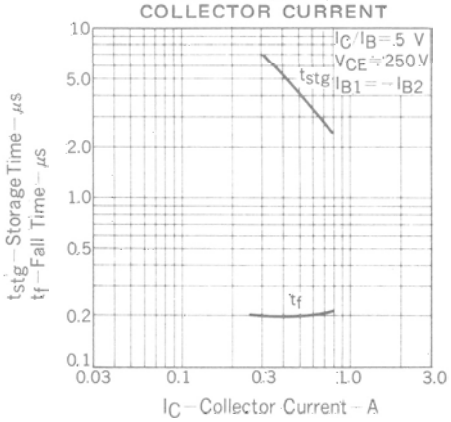
DC CURRENT GAIN vs. COLLECTOR CURRENT



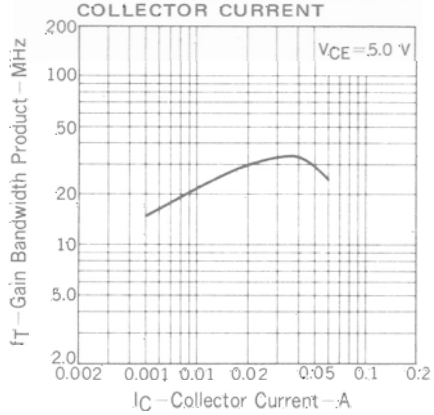
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



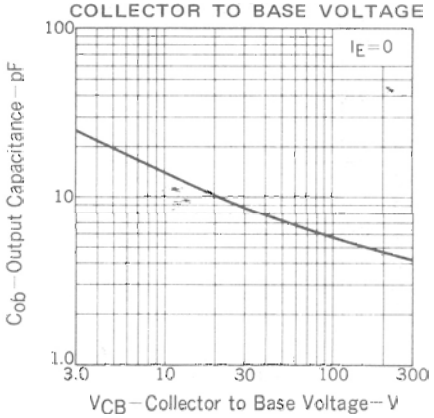
TURN OFF TIME vs. COLLECTOR CURRENT



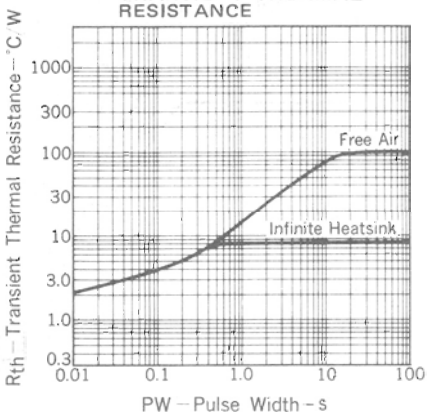
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



TRANSIENT THERMAL
RESISTANCE



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SC3999

DESCRIPTION The 2SC3999 is designed for uses of high-resolution monitor TV applications. This makes it possible to raise the video band of high-resolution monitor TVs to 50 MHz.

FEATURES

- High f_T : f_T = 300 MHz TYP. (@V_{CE} = 30 V, I_E = –30 mA)
- Low C_{ob} : C_{ob} = 2.8 pF (@V_{CB} = 30 V)
- High Voltage : V_{CBO} = 300 V, V_{CEO} = 250 V
- High Total Power Dissipation : P_T = 0.75 W
- Complementary to 2SA1544

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . –55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

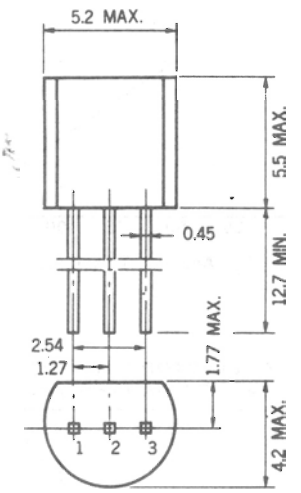
Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 750 mW

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	300	V
V_{CEO}	Collector to Emitter Voltage	250	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	100	mA

PACKAGE DIMENSIONS
in millimeters



1. Emitter EIAJ : SC-43B
2. Collector JEDEC : TO-92
3. Base IEC : PA33

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	200	320		V_{CE} = 10 V, I_C = 10 mA*
f_T	Gain Bandwidth Product	200	300		MHz	V_{CE} = 30 V, I_E = –30 mA
C_{ob}	Output Capacitance		2.8	3.5	pF	V_{CB} = 30 V, I_E = 0, f = 1 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		0.08	0.3	V	I_C = 10 mA, I_B = 1.0 mA*
$V_{BE(sat)}$	Base Saturation Voltage		0.72	1.2	V	I_C = 10 mA, I_B = 1.0 mA*
V_{ESDR}	Electrostatic Discharge-Resistant		1 000		V	C = 1 000 pF, E-B Reverse Bias

* Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

Classification of h_{FE}

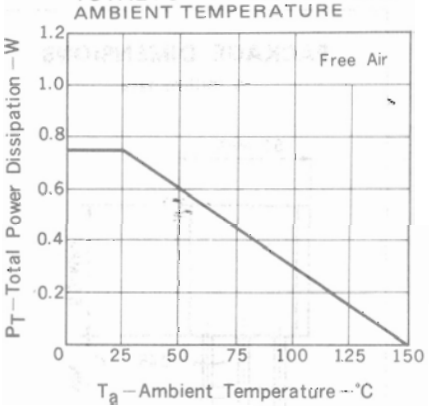
Rank	M	L	K
Range	60 to 120	100 to 200	160 to 320

Test Conditions: V_{CE} = 10 V, I_C = 10 mA

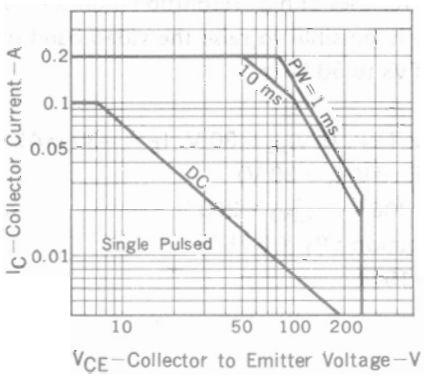
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

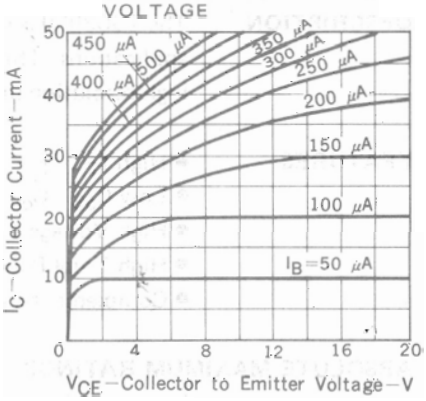
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



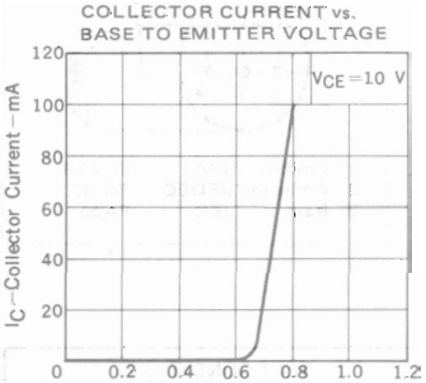
FORWARD BIAS SAFE OPERATING AREA



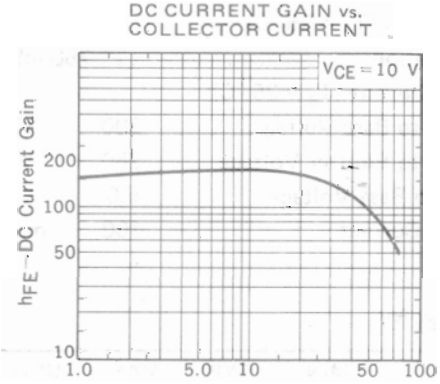
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



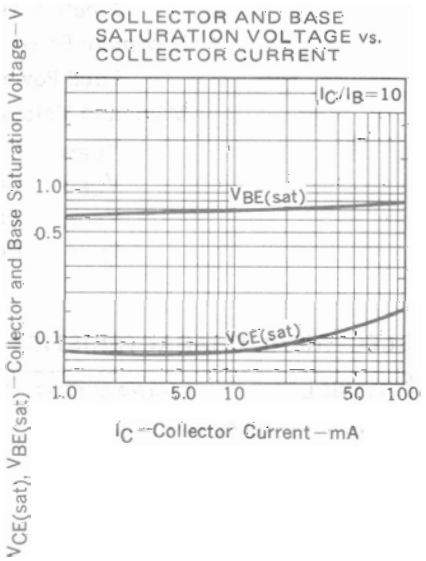
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



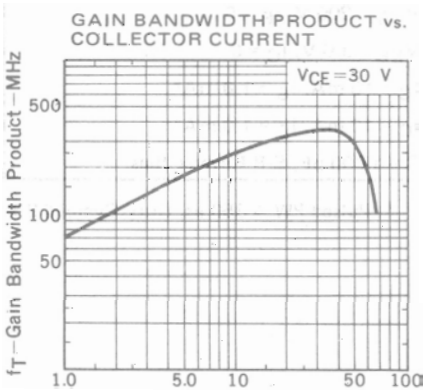
DC CURRENT GAIN vs. COLLECTOR CURRENT



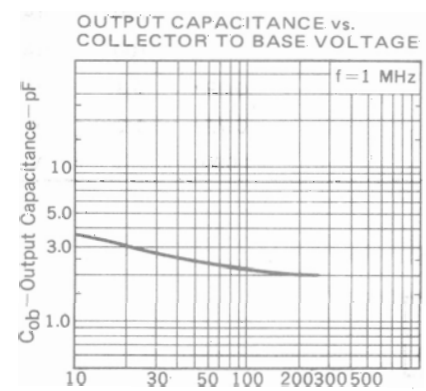
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

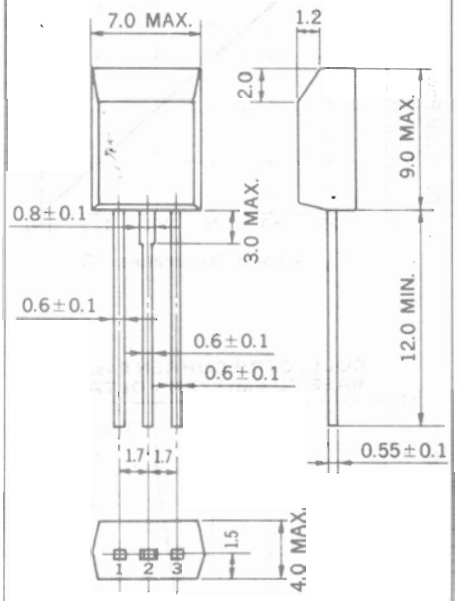
NPN SILICON TRANSISTOR
2SC4000

DESCRIPTION The 2SC4000 is designed for uses of high-resolution monitor TV applications. This makes it possible to raise the video band of high-resolution monitor TVs to 50 MHz.

FEATURES

- High f_T: f_T = 300 MHz TYP. (@V_{CE} = 30 V, I_E = –30 mA)
- Low C_{ob}: C_{ob} = 2.8 pF (@V_{CB} = 30 V)
- High Voltage: V_{CBO} = 300 V, V_{CEO} = 250 V
- High Total Power Dissipation: P_T = 1.0 W
- Complementary to 2SA1545

PACKAGE DIMENSIONS
in millimeters



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . –55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	300	V
V_{CEO}	Collector to Emitter Voltage	250	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	100	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	200	320	–	V_{CE} = 10 V, I_C = 10 mA*
f_T	Gain Bandwidth Product	200	300		MHz	V_{CE} = 30 V, I_E = –30 mA
C_{ob}	Output Capacitance		2.8	3.5	pF	V_{CB} = 30 V, I_E = 0, f = 1 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		0.08	0.3	V	I_C = 10 mA, I_B = 1.0 mA*
$V_{BE(sat)}$	Base Saturation Voltage		0.72	1.2	V	I_C = 10 mA, I_B = 1.0 mA*
V_{ESDR}	Electrostatic Discharge-Resistant		1 000		V	C = 1 000 pF, E-B Reverse Bias

* Pulsed PW < 350 μs, Duty Cycle < 2 %

Classification of h_{FE}

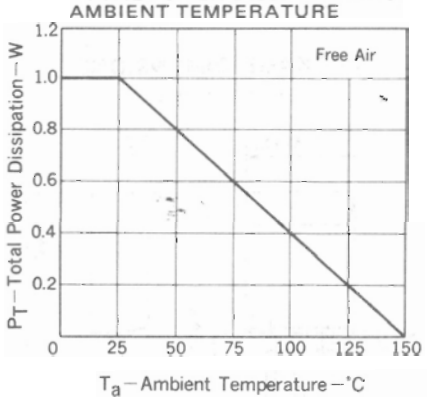
Rank	M	L	K
Range	60 to 120	100 to 200	160 to 320

Test Conditions: V_{CE} = 10 V, I_C = 10 mA

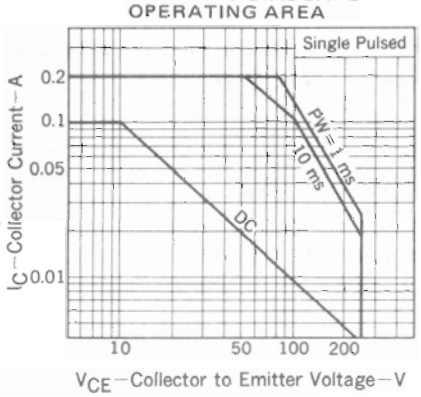
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

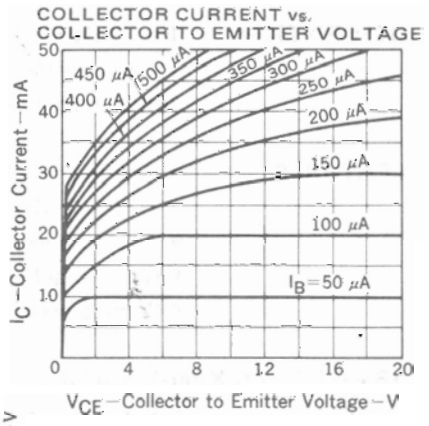
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



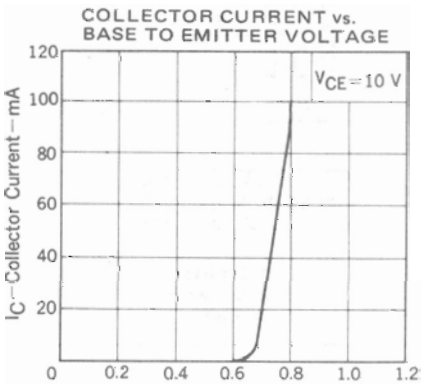
FORWARD BIAS SAFE OPERATING AREA



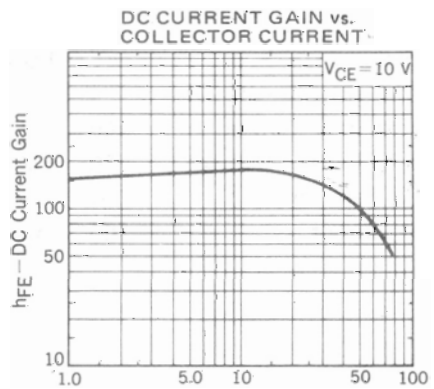
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



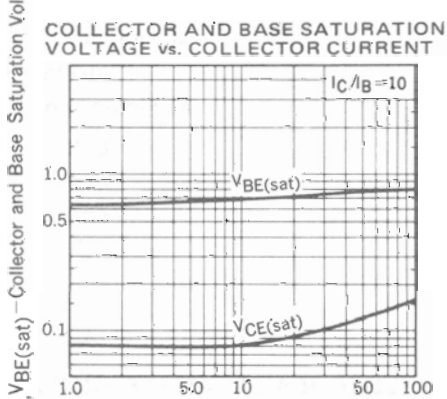
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



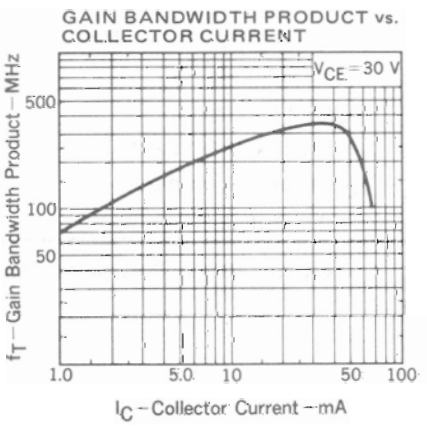
DC CURRENT GAIN vs. COLLECTOR CURRENT



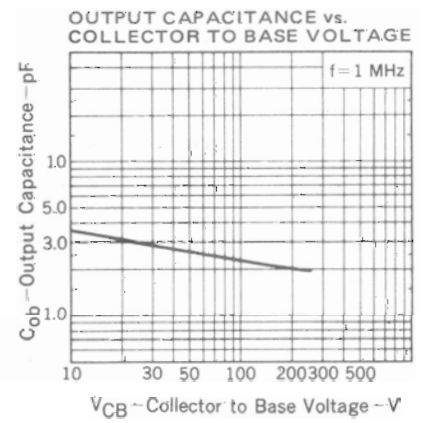
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

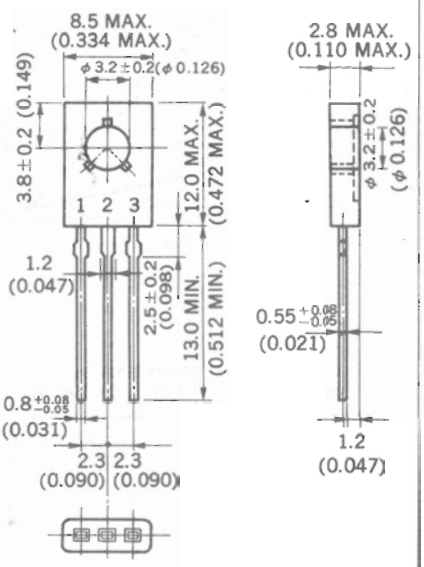
NPN SILICON POWER TRANSISTOR
2SC4001

DESCRIPTION The 2SC4001 is designed for uses of high-resolution monitor TV applications. This makes it possible to raise the video band of high-resolution monitor TVs to 50 MHz.

FEATURES

- High f_T : f_T = 300 MHz TYP. (@V_{CE} = 30 V, I_E = –30 mA)
- Low C_{ob} : C_{ob} = 2.8 pF (@V_{CB} = 30 V)
- High Voltage : V_{CBO} = 300 V, V_{CEO} = 250 V
- High Total Power Dissipation :
  P_T (T_a/T_C = 25 °C) = 1.3 W/7 W
- Complementary to 2SA1546

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . –55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation
- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 7.0 W

Maximum Voltages and Current (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	300	V
V_{CEO}	Collector to Emitter Voltage	250	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	100	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	200	320		V_{CE} = 10 V, I_C = 10 mA*
f_T	Gain Bandwidth Product	200	300		MHz	V_{CE} = 30 V, I_E = –30 mA
C_{ob}	Output Capacitance		2.8	3.5	pF	V_{CB} = 30 V, I_E = 0, f = 1 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 200 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		0.08	0.3	V	I_C = 10 mA, I_B = 1.0 mA*
$V_{BE(sat)}$	Base Saturation Voltage		0.72	1.2	V	I_C = 10 mA, I_B = 1.0 mA*
V_{ESDR}	Electrostatic Discharge-Resistant		1 000		V	C = 1 000 pF, E-B Reverse Bias

* Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

Classification of h_{FE}

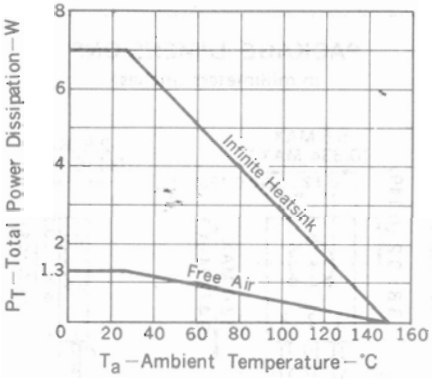
Rank	M	L	K
Range	60 to 120	100 to 200	160 to 300

Test Conditions: V_{CE} = 10 V, I_C = 10 mA

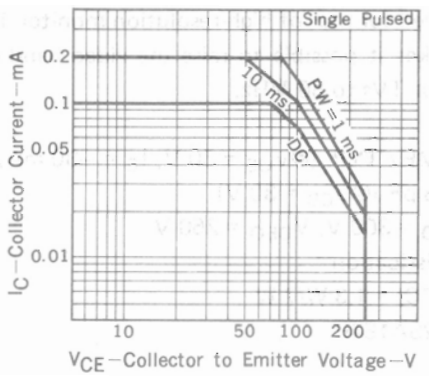
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

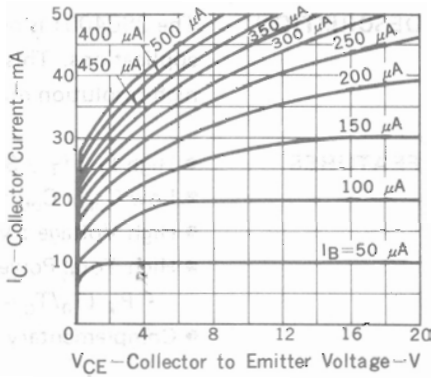
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



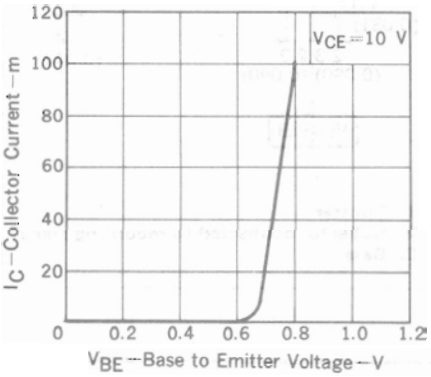
FORWARD BIAS SAFE OPERATING AREA



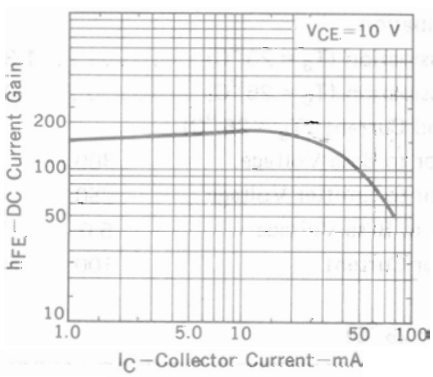
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



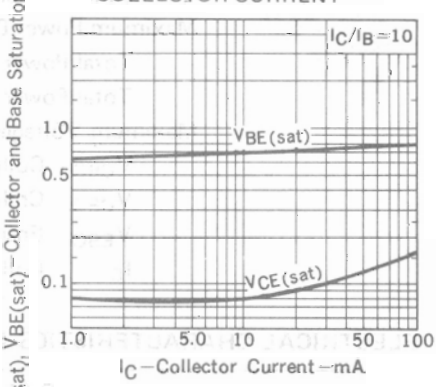
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



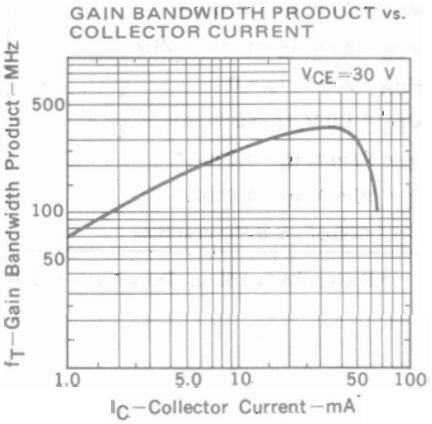
DC CURRENT GAIN vs. COLLECTOR CURRENT



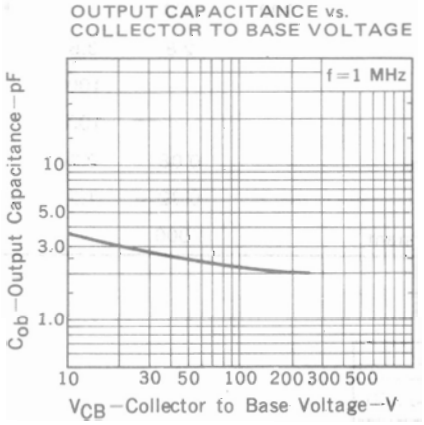
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

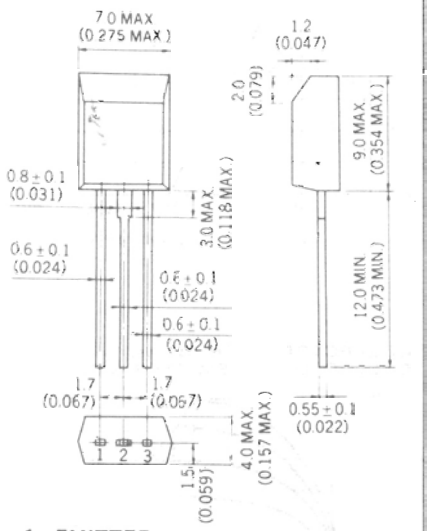
NPN SILICON TRANSISTOR
2SD471

DESCRIPTION The 2SD471 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation:
  1.0 W at 25 °C Ambient Temperature.
- Complementary to the NEC 2SB564 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 1.0 W
- Thermal Resistance (Junction to Ambient) . . . . . 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . . 25 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- I_C Collector Current . . . . . 1.0 A
- I_B Base Current . . . . . 0.1 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400		V_{CE}=1.0 V, I_C=0.1 A
h_{FE2}	DC Current Gain	50	140			V_{CE}=1.0 V, I_C=1.0 A
f_T	Gain Bandwidth Product		100		MHz	V_{CE}=6.0 V, I_E=10 mA
C_{ob}	Collector to Base Capacitance		22		pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	600	630	700	mV	V_{CE}=6.0 V, I_C=10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.21	0.35	V	I_C=1.0 A, I_B=0.1 A
$V_{BE(sat)}$	Base Saturation Voltage		1.0	1.2	V	I_C=1.0 A, I_B=0.1 A

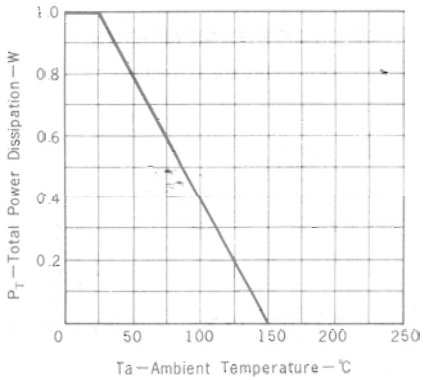
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

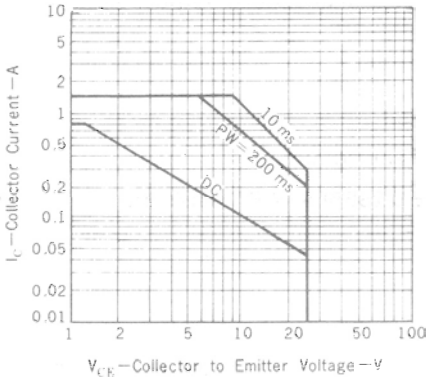
h_{FE1} Test Conditions: V_{CE} = 1.0V, I_C = 0.1A

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

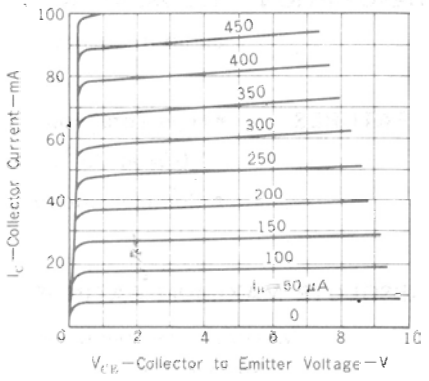
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



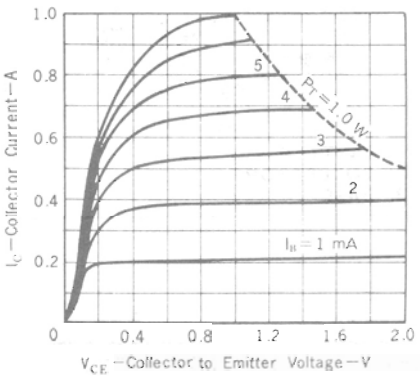
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



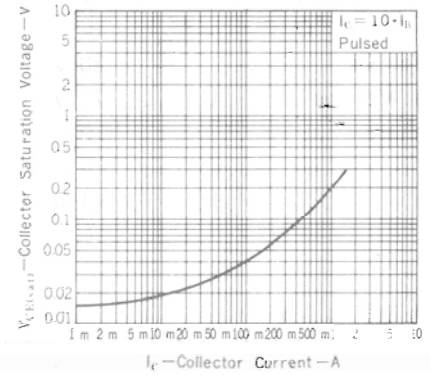
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



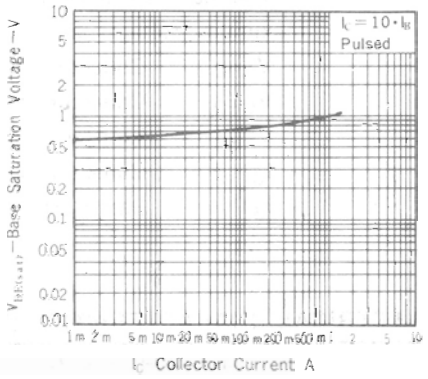
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



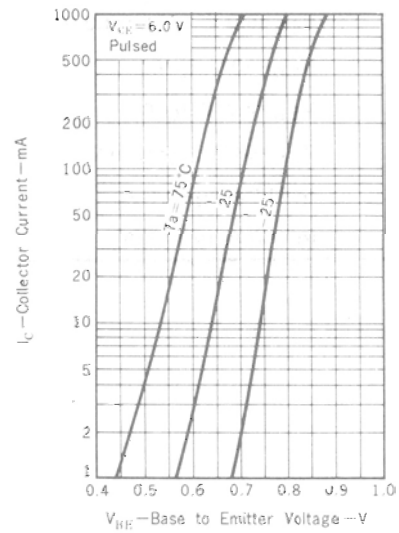
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



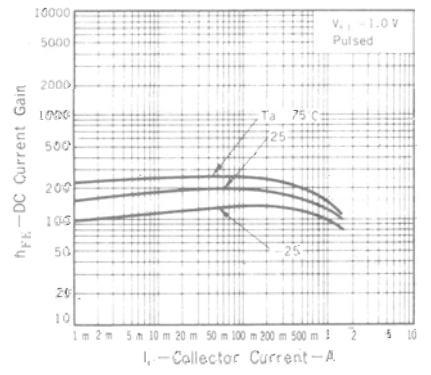
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



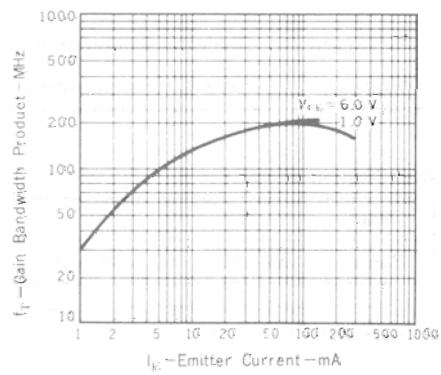
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



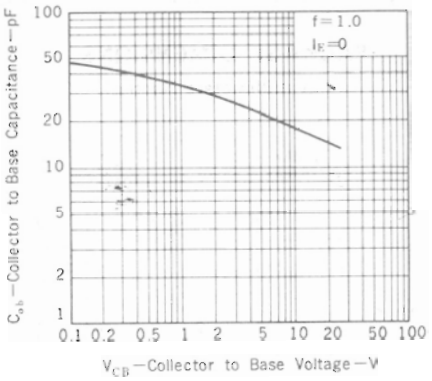
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



COLLECTOR TO BASE CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

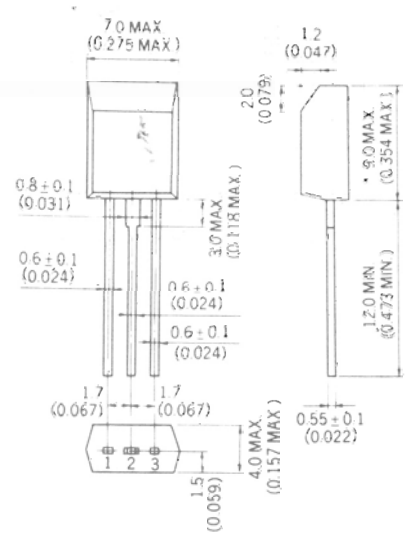
NPN SILICON TRANSISTOR
2SD571

DESCRIPTION The 2SD571 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High total power dissipation and high breakdown voltage: 1.0 W at 25 °C Ambient temperature/V_{CEO} = 50 V
- Complementary to the NEC 2SB605 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 1.0 W
- Thermal Resistance (Junction to Ambient) . . 125 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	0.7	A
I_B	Base Current	0.1	A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	90	200	400	—	V_{CE}=1.0 V, I_C=0.1 A
h_{FE2}	DC Current Gain	50	150		—	V_{CE}=1.0 V, I_C=0.5 A
f_T	Gain Bandwidth Product		110		MHz	V_{CE}=6.0 V, I_E=10 mA
C_{ob}	Output Capacitance		13		pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=60 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	600	635	700	mV	V_{CE}=6.0 V, I_C=10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.12	0.35	V	I_C=0.5 A, I_B=0.05 A
$V_{BE(sat)}$	Base Saturation Voltage		0.90	1.2	V	I_C=0.5 A, I_B=0.05 A

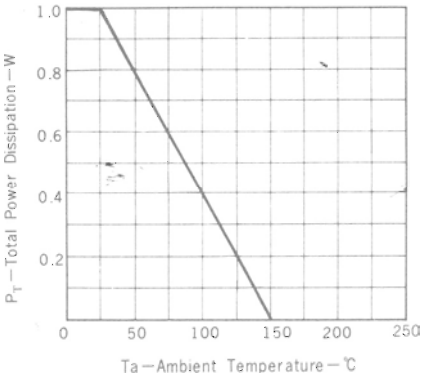
Classification of h_{FE1}

Rank	M	L	K
Range	90 – 180	135 – 270	200 – 400

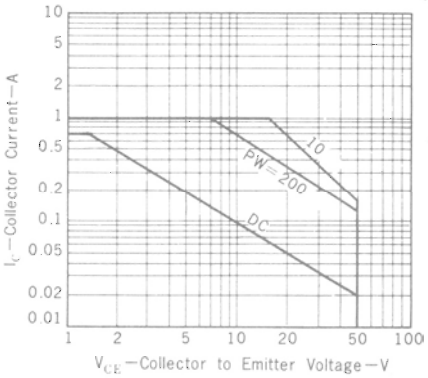
h_{FE1} Test Conditions: V_{CE}=1.0 V, I_C=0.1 A

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

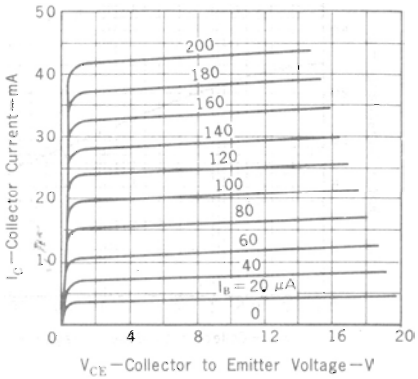
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



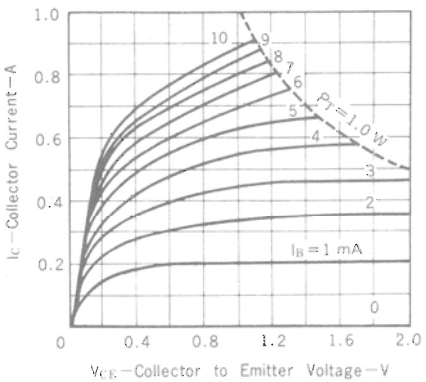
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE)



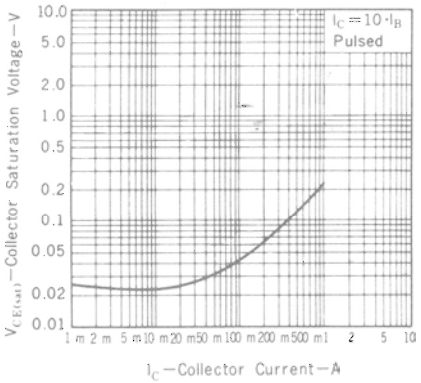
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



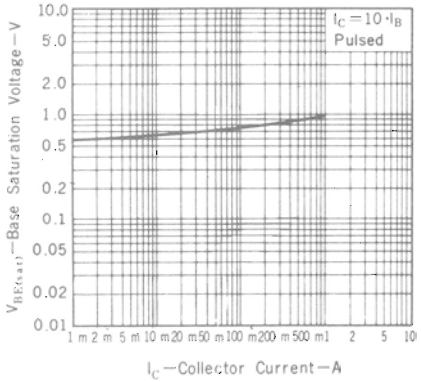
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



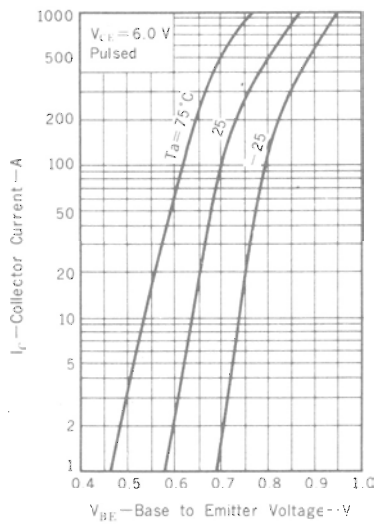
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



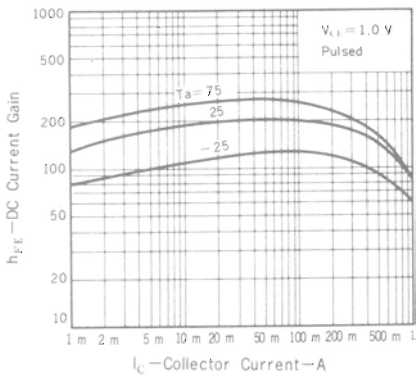
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



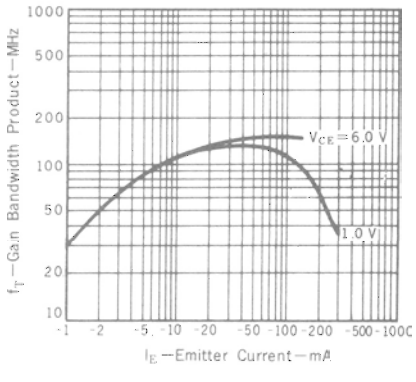
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



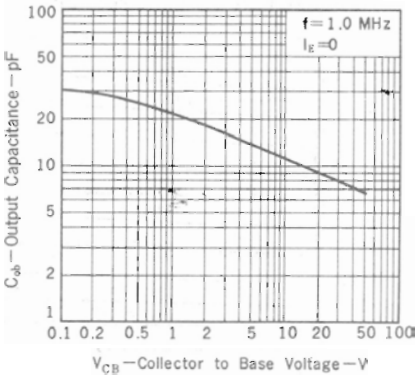
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

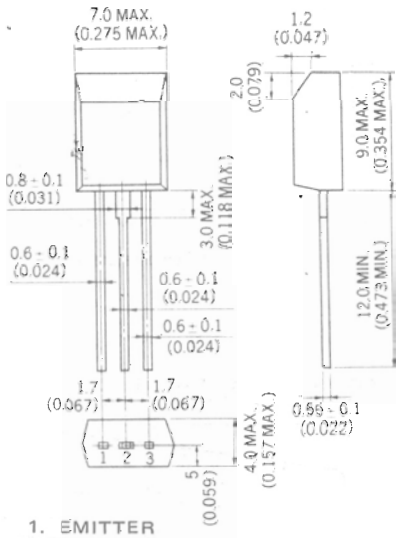
NPN SILICON TRANSISTOR
2SD773

DESCRIPTION The 2SD773 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation P_T : 1.0 W (Ta = 25 °C)
- High DC Current Gain h_{FE} : 250 TYP. (I_C = 100 mA)
- Low Collector Saturation Voltage
  $V_{CE(sat)}$: 0.2 V TYP. (I_C = 1.0A)
- Complementary to the NEC 2SB733 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Current (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 20 V
- V_{CEO} Collector to Emitter Voltage . . . . . 16 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current . . . . . 2.0 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135	250	600	—	V_{CE} = 2.0 V, I_C = 100 mA
h_{FE2}	DC Current Gain	100			—	V_{CE} = 1.0 V, I_C = 1.0 A
f_T	Gain Bandwidth Product	50	110		MHz	V_{CE} = 2.0 V, I_E = −10 mA
C_{ob}	Output Capacitance		16	35	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 16 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.55	0.60	0.65	V	V_{CE} = 6.0 V, I_C = 5.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.20	0.30	V	I_C = 1.0 A, I_B = 50 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.93	1.20	V	I_C = 1.0 A, I_B = 50 mA

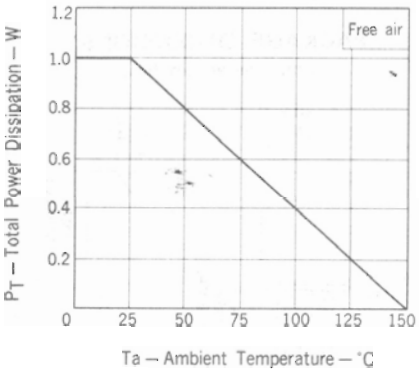
Classification of h_{FE1}

Rank	L_2	K_3	K_4	U_4	U_5
Range	135 – 270	200 – 320	250 – 400	300 – 480	360 – 600

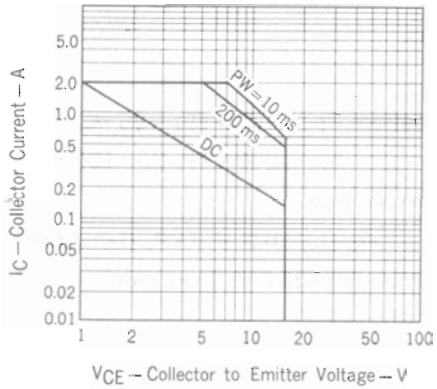
Test Conditions : V_{CE} = 2.0 V, I_C = 100 mA.

TYPICAL CHARACTERISTICS (Ta=25 °C)

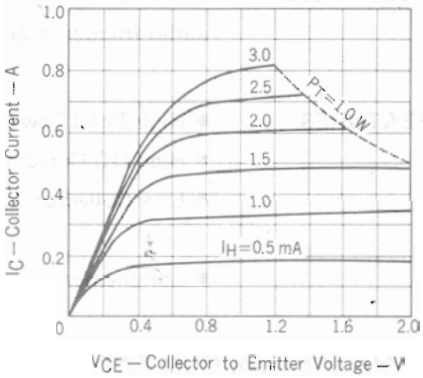
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



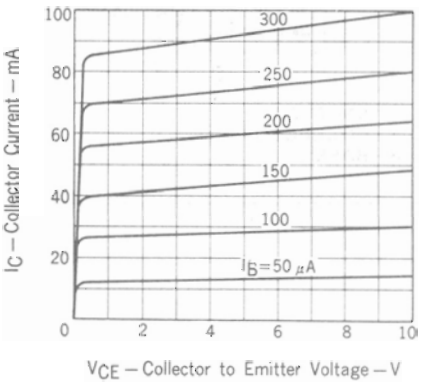
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



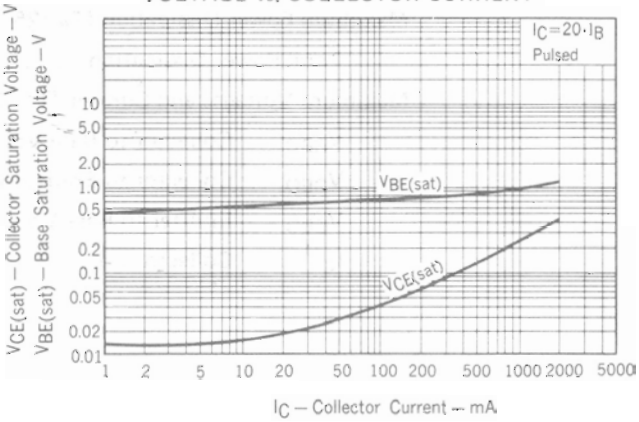
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



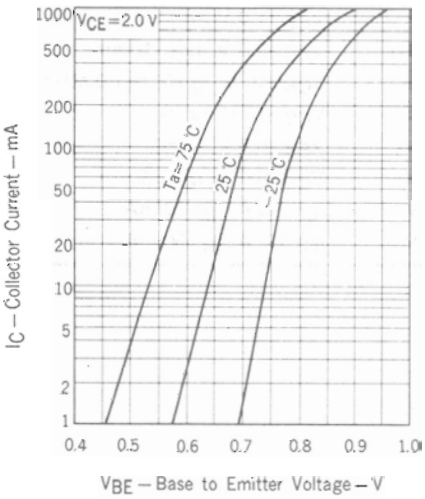
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



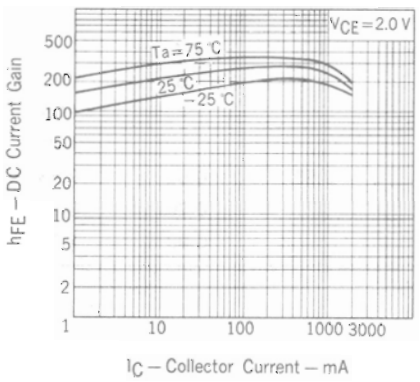
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



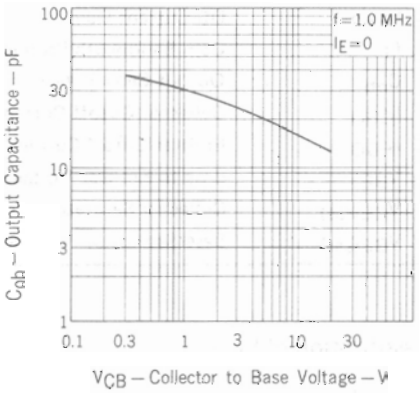
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



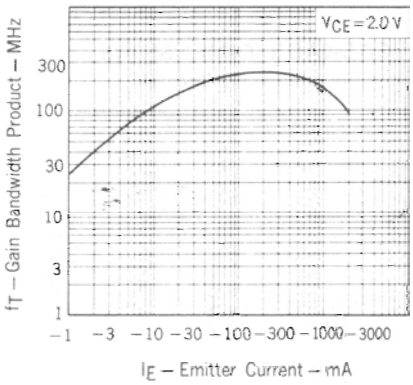
DC CURRENT GAIN vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



GAIN BANDWIDTH PRODUCT vs.
EMITTER CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR

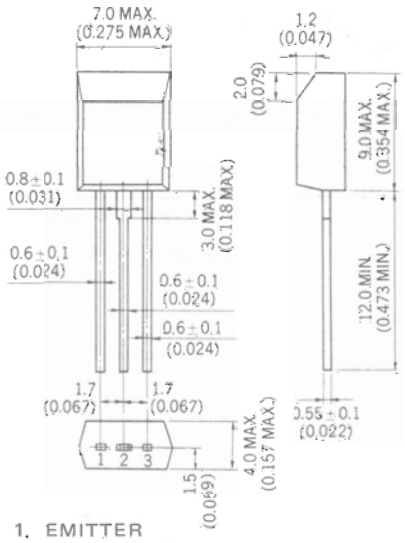
2SD774

DESCRIPTION The 2SD774 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High Total Power Dissipation P_T : 1.0 W (Ta = 25 °C)
- High Voltage V_{CE} : 50 V MIN.
- Complementary to the NEC 2SB734 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 100 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current . . . . . 1.0 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135	300	600	—	V_{CE}=2.0 V, I_C=100 mA
h_{FE2}	DC Current Gain	70			—	V_{CE}=1.0 V, I_C=1.0 A
f_T	Gain Bandwidth Product	50	95		MHz	V_{CE}=2.0 V, I_E=−10 mA
C_{ob}	Output Capacitance		16	35	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=6.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55	0.60	0.65	V	V_{CE}=6.0 V, I_C=5.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.23	0.30	V	I_C=1.0 A, I_B=50 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.92	1.20	V	I_C=1.0 A, I_B=50 mA

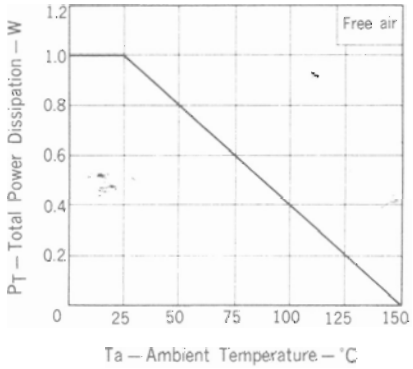
Classification of h_{FE1}

Rank	L_2	K_3	K_4	U_4	U_5
Range	135 – 270	200 – 320	250 – 400	300 – 480	360 – 600

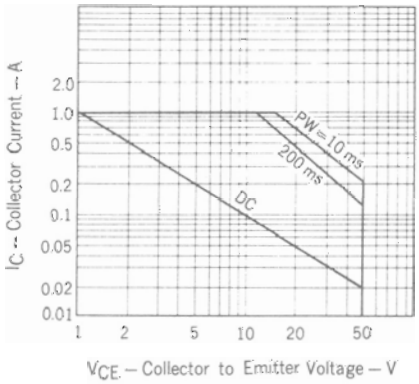
Test Conditions : V_{CE}=2.0 V, I_C=100 mA.

TYPICAL CHARACTERISTICS (Ta=25 °C)

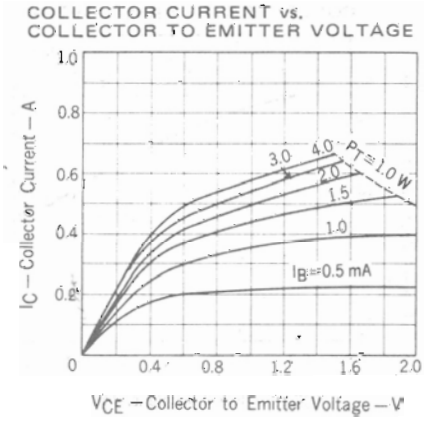
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



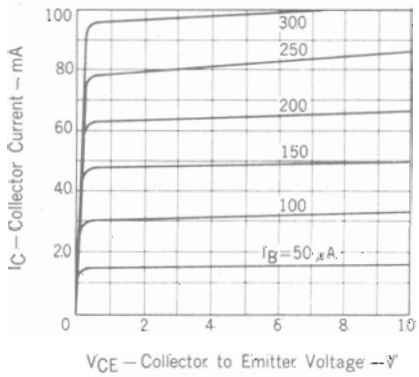
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



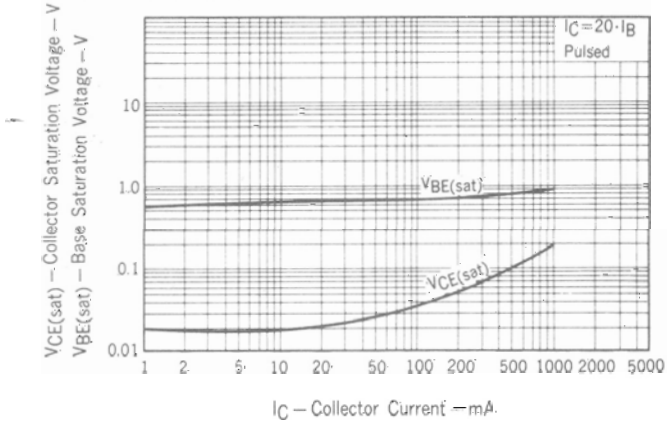
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



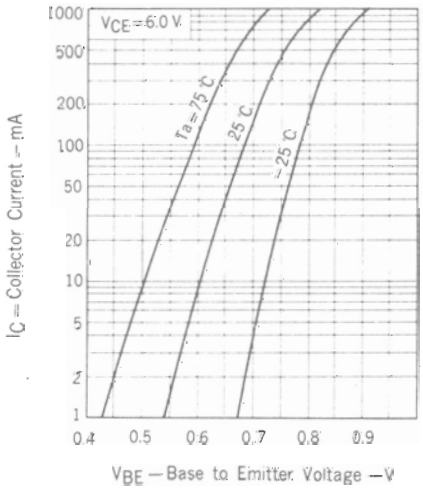
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



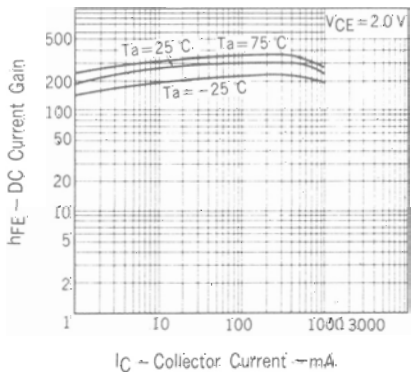
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



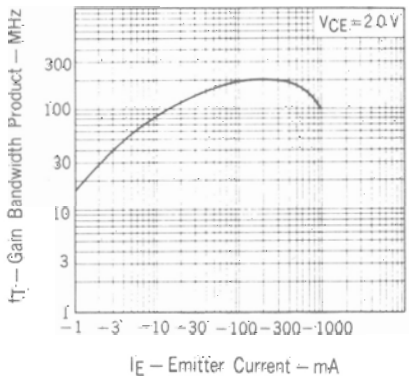
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



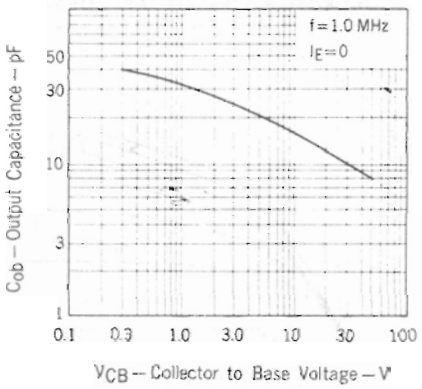
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

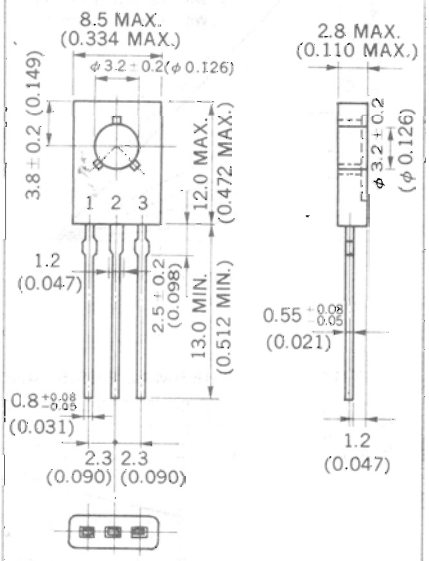
NPN SILICON POWER TRANSISTORS
2SD794,2SD794A

DESCRIPTION The 2SD794, 2SD794A is an NPN general purpose transistor designed for use in Audio frequency amplifier.

FEATURES

- High Voltage and Large Current capacity.
- Complementary to NEC 2SB744, 2SB744A PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SD794	2SD794A	
V_{CBO}	Collector to Base Voltage	70	70	V
V_{CEO}	Collector to Emitter Voltage	45	60	V
V_{EBO}	Emitter to Base Voltage	5.0	5.0	V
$I_{C(DC)}$	Collector Current (DC)	3.0	3.0	A
$I_{C(pulse)}$	Collector Current (pulse)	5.0	5.0	A

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	30	70			V_{CE} = 5.0 V, I_C = 20 mA*
h_{FE2}	DC Current Gain	60	100	320		V_{CE} = 5.0 V, I_C = 0.5 A*
f_T	Gain Bandwidth Product		60		MHz	V_{CE} = 5.0 V, I_C = 0.1 A
C_{ob}	Output Capacitance		40		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 45 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		0.3	2.0	V	I_C = 1.5 A, I_B = 0.15 A*
$V_{BE(sat)}$	Base Saturation Voltage		0.8	2.0	V	I_C = 1.5 A, I_B = 0.15 A*

*Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %

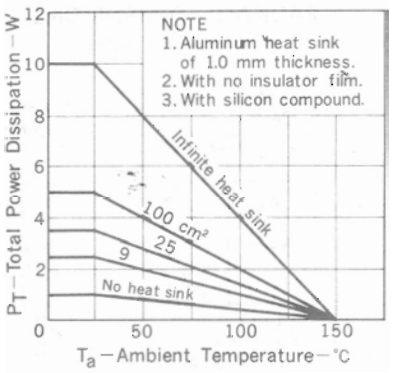
Classification of h_{FE2}

Rank	R	Q	P
Range	60 to 120	100 to 200	160 to 320

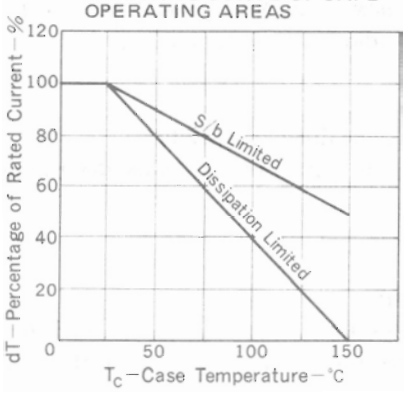
Test Conditions : V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

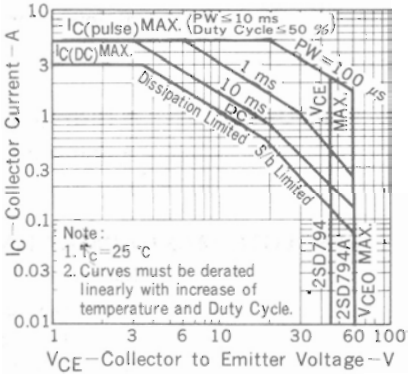
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



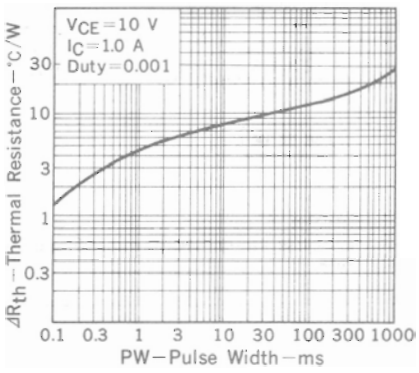
DERATING CURVE OF SAFE OPERATING AREAS



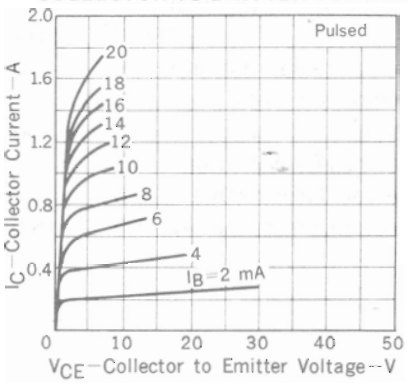
SAFE OPERATING AREAS



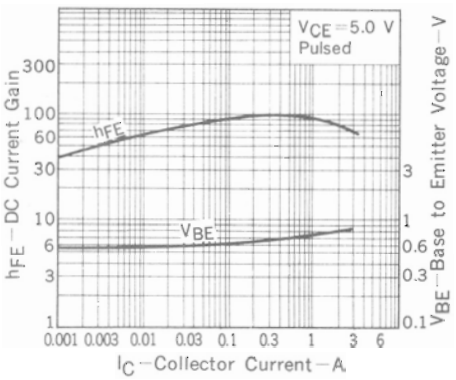
TRANSIENT THERMAL RESISTANCE



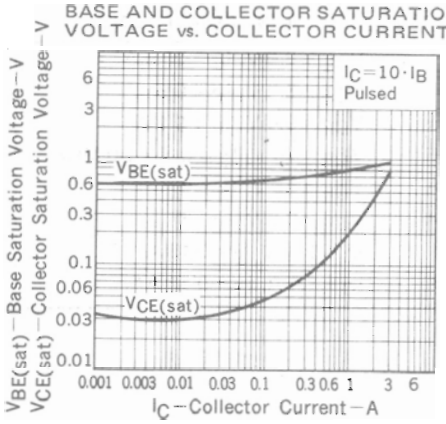
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



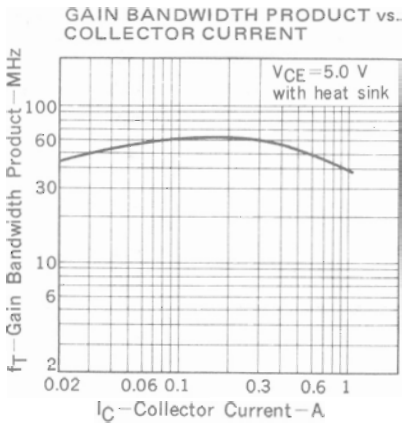
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



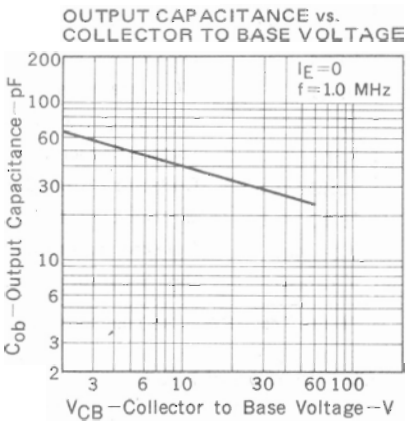
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

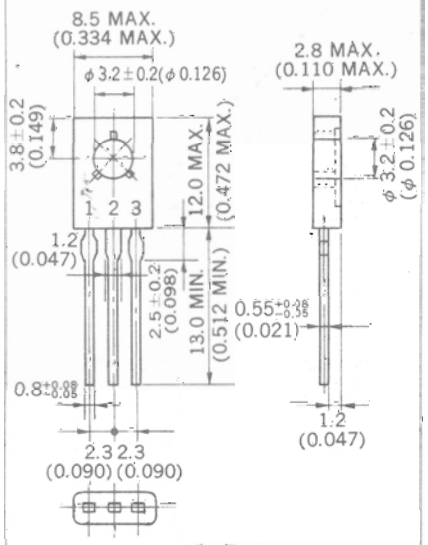
NPN SILICON POWER TRANSISTOR
2SD809(1)

DESCRIPTION The 2SD809(1) is designed for use in driver and output stages of audio frequency amplifier, and low speed switching.

FEATURES

- Suitable for general driving use, such as lamp, relay or motor.
- Low Collector Saturation Voltage.
- High h_{FE} and Excellent h_{FE} Linearity.
- Complementary to the NEC 2SB731 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

P_T	Total Power Dissipation (T_a = 25 °C)	1.0	W
P_T	Total Power Dissipation (T_C = 25 °C)	10	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage . . .	50	V
V_{EBO}	Emitter to Base Voltage	6.0	V
$I_{C(DC)}$	Collector Current	1.0	A
$I_{C(pulse)}$ *	Collector Current	2.0	A
$I_{B(DC)}$	Base Current.	0.5	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	135	250	600	—	V_{CE} = 2.0 V, I_C = 0.1 A
h_{FE2} **	DC Current Gain	70			—	V_{CE} = 1.0 V, I_C = 1.0 A
f_T	Gain Bandwidth Product		85		MHz	V_{CE} = −2.0 V, I_E = −10 mA
C_{ob}	Output Capacitance		15		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			0.1	μA	V_{EB} = 6.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage		0.3	0.6	V	I_C = 1.0 A, I_B = 50 mA
$V_{BE(sat)}$ **	Base Saturation Voltage		1.0	1.2	V	I_C = 1.0 A, I_B = 50 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

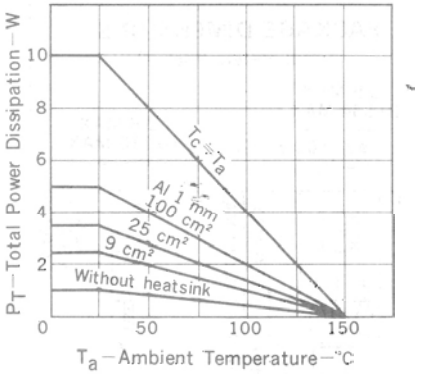
Classification of h_{FE1}

Rank	L	K	F	E
Range	135 to 270	200 to 400	300 to 480	360 to 600

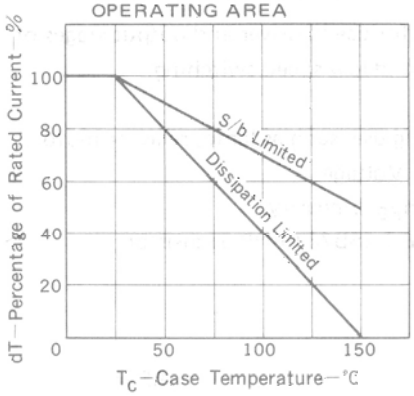
Test Conditions: V_{CE} = 2.0 V, I_C = 0.1 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

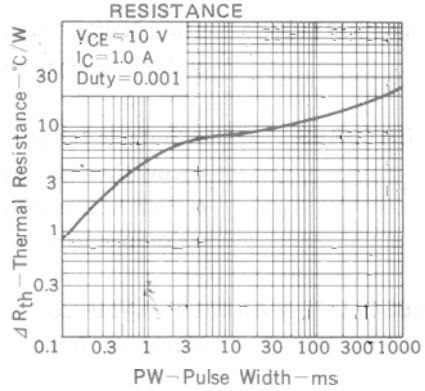
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



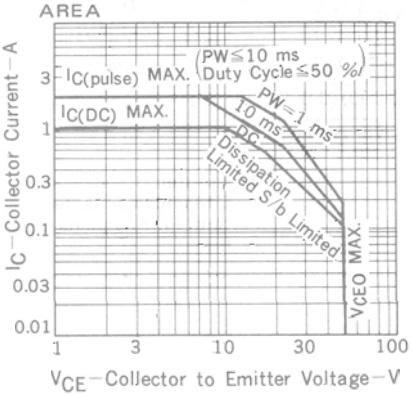
DERATING CURVE OF SAFE OPERATING AREA



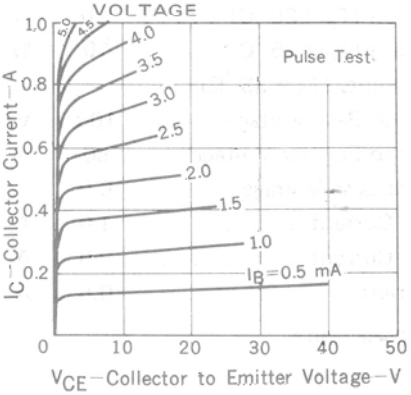
TRANSIENT THERMAL RESISTANCE



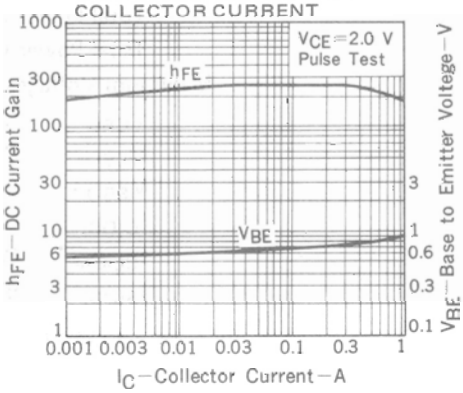
FORWARD BIAS SAFE OPERATING AREA



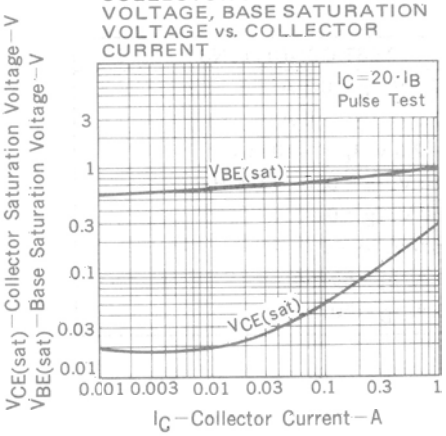
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



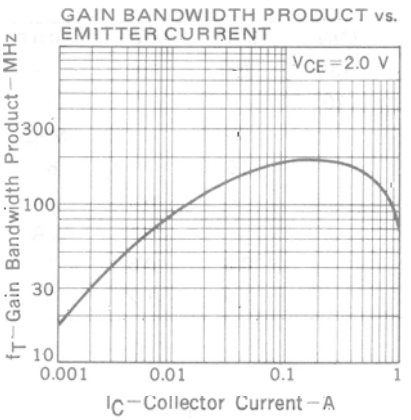
DC CURRENT GAIN AND BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



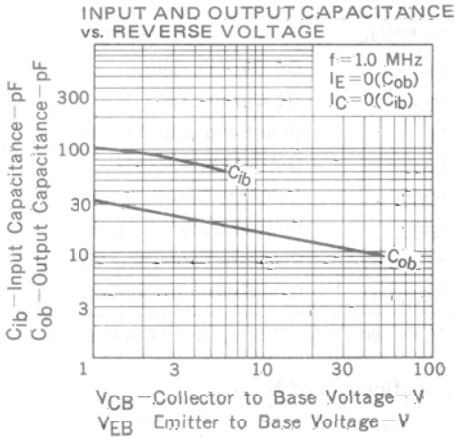
COLLECTOR SATURATION VOLTAGE, BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

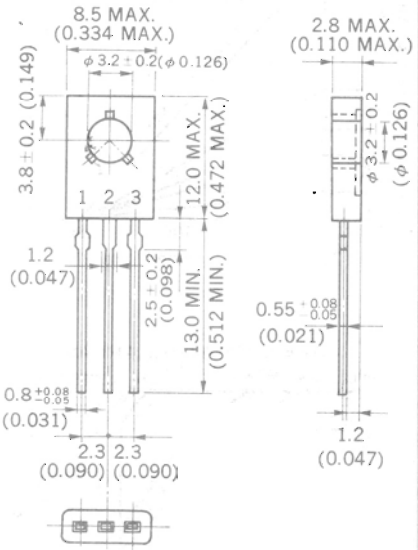
NPN SILICON POWER TRANSISTOR
2SD882

DESCRIPTION The 2SD882 is NPN silicon transistor suited for the output stage of 3 watts audio amplifier, voltage regulator, DC-DC converter and relay driver.

FEATURES

- Low saturation voltage.
  $V_{CE(sat)} \leq 0.5$ V (@ I_C = 2 A, I_B = 0.2 A)
- Excellent h_{FE} linearity and high h_{FE}.
  h_{FE} : 60 to 400 (@ V_{CE} = 2 V, I_C = 1 A)
- Less cramping space required due to small and thin package and reducing the trouble for attachment to a radiator.
  No insulator bushing required.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	40	V
V_{CEO}	Collector to Emitter Voltage	30	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (D.C)	3.0	A
$I_{C(pulse)}$*	Collector Current (pulse)	7.0	A

*Pulse Test PW ≤ 350 μs, Duty Cycle ≤ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	30	150			V_{CE} = 2.0 V, I_C = 20 mA**
h_{FE2}	DC Current Gain	60	160	400		V_{CE} = 2.0 V, I_C = 1.0 A**
f_T	Gain Bandwidth Product		90		MHz	V_{CE} = 5.0 V, I_C = 0.1 A
C_{ob}	Output Capacitance		45		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 3.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage		0.3	0.5	V	I_C = 2.0 A, I_B = 0.2 A**
$V_{BE(sat)}$	Base Saturation Voltage		1.0	2.0	V	I_C = 2.0 A, I_B = 0.2 A**

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %

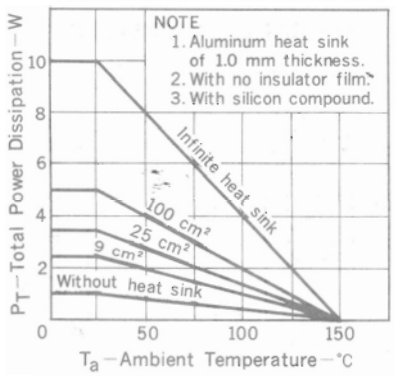
Classification of h_{FE}

Rank	R	Q	P	E
Range	60 to 120	100 to 200	160 to 320	200 to 400

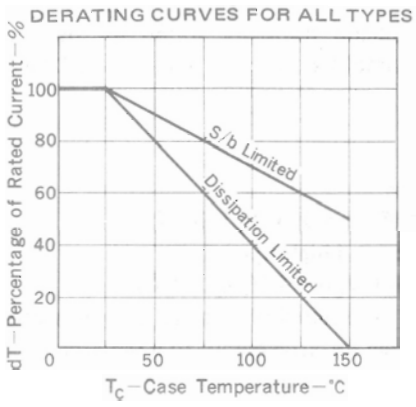
Test Conditions : V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

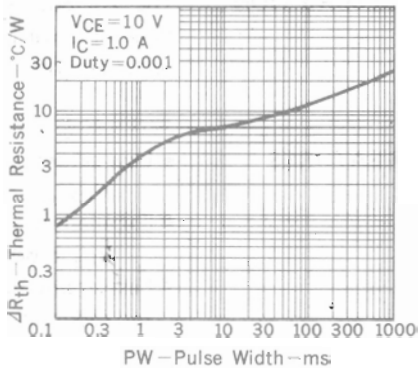
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



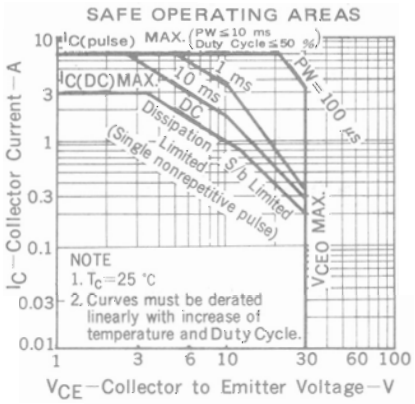
DERATING CURVES FOR ALL TYPES



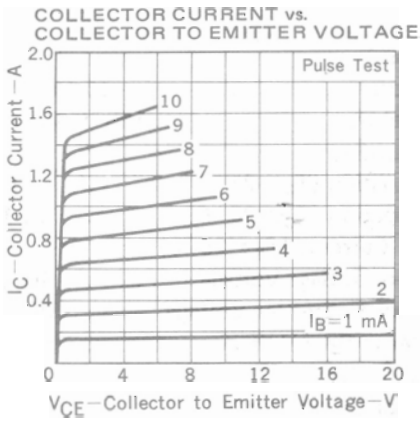
THERMAL RESISTANCE vs. PULSE WIDTH



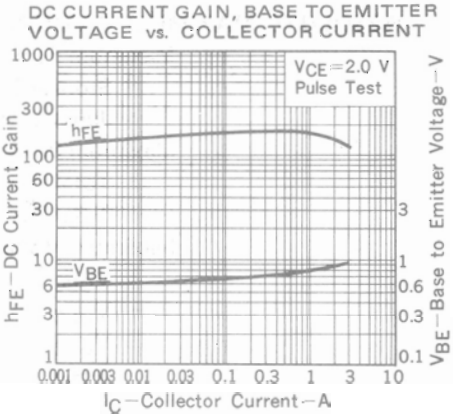
SAFE OPERATING AREAS



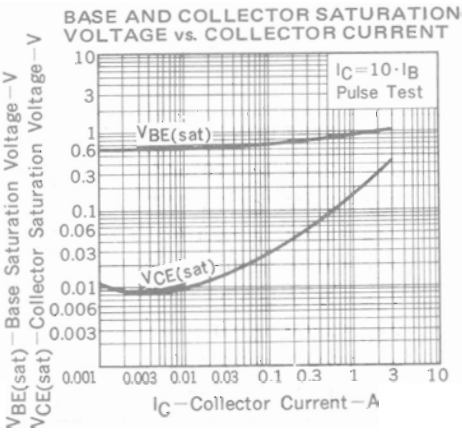
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



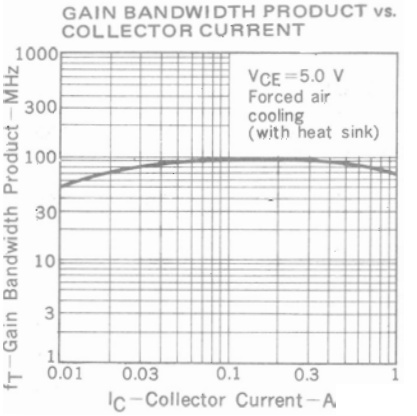
DC CURRENT GAIN, BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



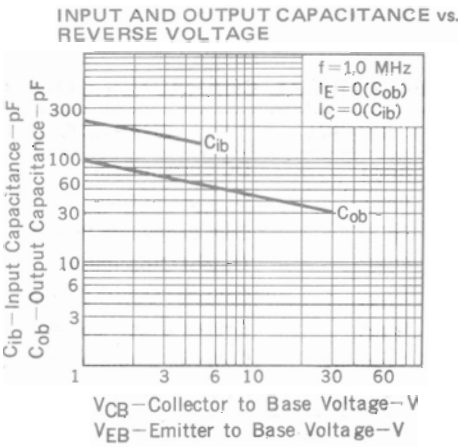
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTORS
2SD985,2SD986

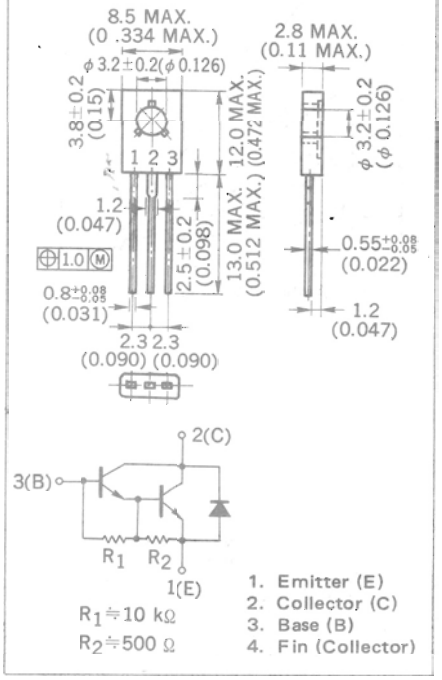
DESCRIPTION

The 2SD985, 2SD986 are darlington transistors built-in dumper diodes at E-C.
They are suitable for use to operate from IC without predriver such as hammer driver.

FEATURES

- High DC Current Gain.
- Low Collector Saturation Voltage.
- Built-in a dumper diode at E-C.
- Complementary to the NEC 2SB794, 2SB795 PNP Transistors.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)

		2SD985	2SD986	
V_{CBO}	Collector to Base Voltage. . .	150	150	V
V_{CEO}	Collector to Emitter Voltage.	60	80	V
V_{EBO}	Emitter to Base Voltage. . . .	8.0		V
$I_{C(DC)}$	Collector Current.	±1.5		A
$I_{C(pulse)}$ *	Collector Current.	±3.0		A
$I_{B(DC)}$	Base Current.	0.15		A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	1000			−	V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2} **	DC Current Gain	2000		30000	−	V_{CE} = 2.0 V, I_C = 1.0 A
t_{on}	Turn On Time		0.5		μs	I_C = 1.0 A, R_L = 50 Ω
t_{stg}	Storage Time		1.0		μs	I_{B1} = −I_{B2} = 1.0 mA, V_{CC} = 50 V
t_f	Fall Time		1.0		μs	See Test Circuit
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60/80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage			1.5	V	I_C = 1.0 A, I_B = 1.0 mA
$V_{BE(sat)}$ **	Base Saturation Voltage			2.0	V	I_C = 1.0 A, I_B = 1.0 mA

** Pulsed / PW ≦ 350 μs, Duty Cycle ≦ 2 %

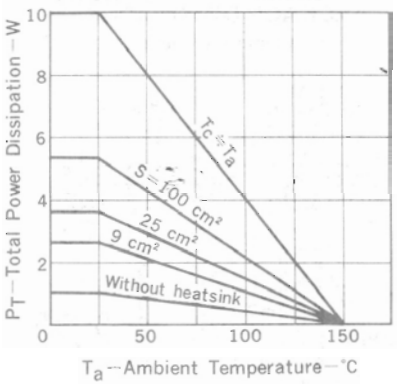
Classification of h_{FE2}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 30000

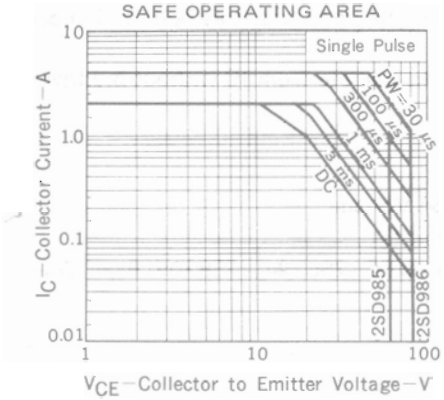
Test Conditions: V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

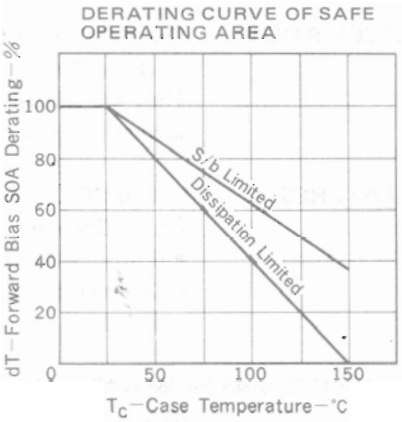
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



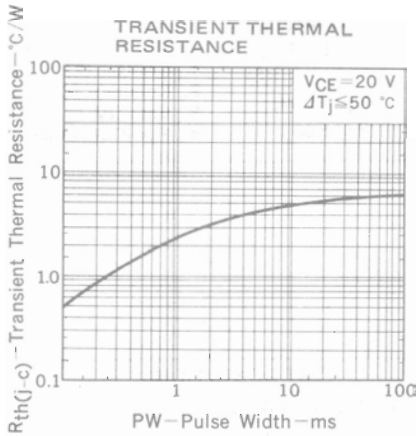
SAFE OPERATING AREA



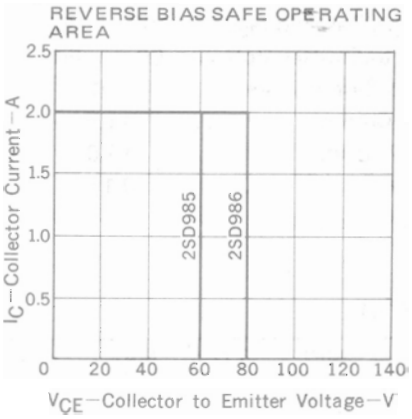
DERATING CURVE OF SAFE OPERATING AREA



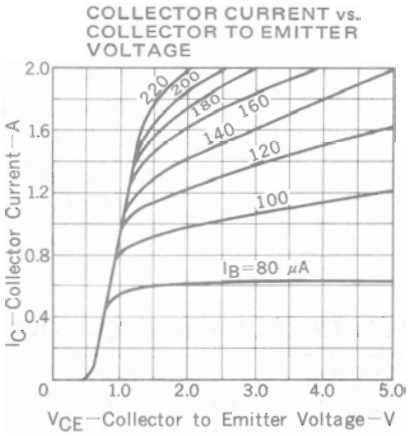
TRANSIENT THERMAL RESISTANCE



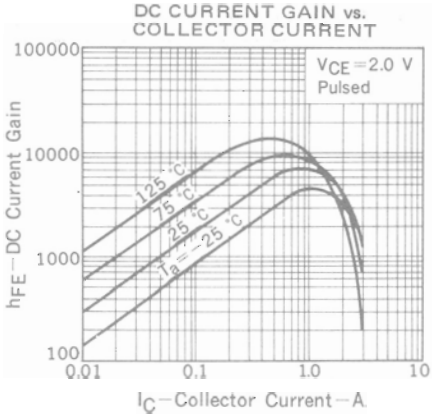
REVERSE BIAS SAFE OPERATING AREA



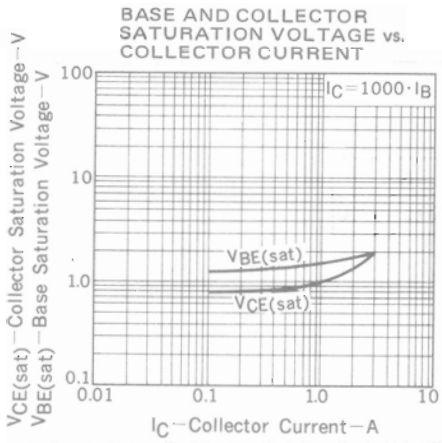
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



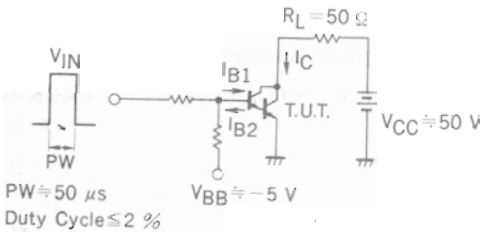
DC CURRENT GAIN vs. COLLECTOR CURRENT

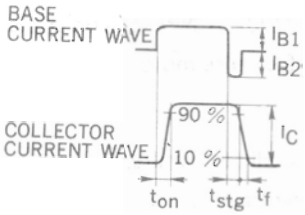


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





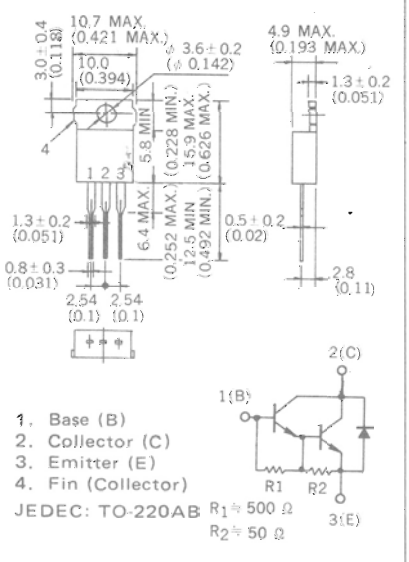
NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR
2SD987

DESCRIPTION The 2SD987 is NPN silicon triple diffused darlington transistor designed for pulse motor driver, relay driver and ignitor applications.

FEATURES
- Low collector saturation voltage.
- High voltage rating.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base (B)
2. Collector (C)
3. Emitter (E)
4. Fin (Collector)

JEDEC: TO-220AB

$R_1 \fallingdotseq 500\ \Omega$
$R_2 \fallingdotseq 50\ \Omega$

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	150 °C Maximum	

Maximum Power Dissipation ($T_c = 25$ °C)

Total Power Dissipation	40	W

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{CBO}	Collector to Base Voltage	500	V
V_{CEO}	Collector to Emitter Voltage	400	V
V_{EBO}	Emitter to Base Voltage	8.0	V
$I_{C(DC)}$	Collector Current (DC)	±5.0	A
$I_{C(pulse)}$	Collector Current (Pulse)*	±10	A
$I_{B(DC)}$	Base Current (DC)	0.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	200			–	$V_{CE} = 2.0$ V, $I_C = 1.0$ A
h_{FE2}	DC Current Gain**	100			–	$V_{CE} = 2.0$ V, $I_C = 3.0$ A
t_{on}	Turn-on Time		1.0		μs	$I_C = 3.0$ A, $I_{B1} = -I_{B2} = 30$ mA
t_{stg}	Storage Time		9.0		μs	$R_L = 50\ \Omega$, $V_{CC} \fallingdotseq 150$ V
t_f	Fall Time		4.0		μs	See Test Circuit.
$V_{CE(sat)}$	Collector Saturation Voltage**		1.0	1.5	V	$I_C = 3.0$ A, $I_B = 30$ mA
$V_{BE(sat)}$	Base Saturation Voltage**		1.6	2.0	V	$I_C = 3.0$ A, $I_B = 30$ mA
I_{CBO}	Collector Cutoff Current			10	μA	$V_{CB} = 400$ V, $I_E = 0$

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

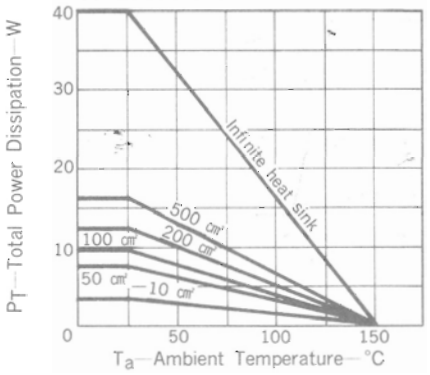
Classification of h_{FE1}

Rank	M	L	K
Range	200 to 500	400 to 1000	800 to 2000

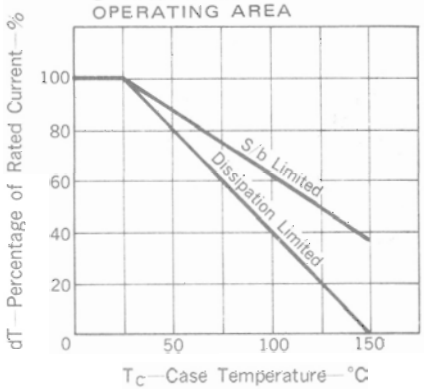
Test Conditions : $V_{CE} = 2.0$ V, $I_C = 1.0$ A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

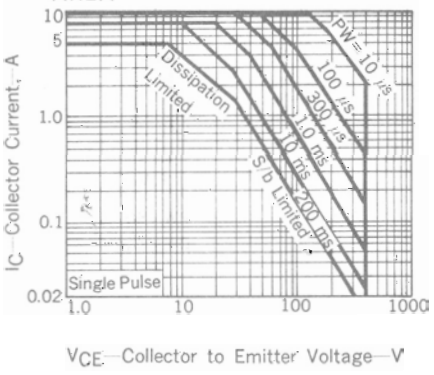
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



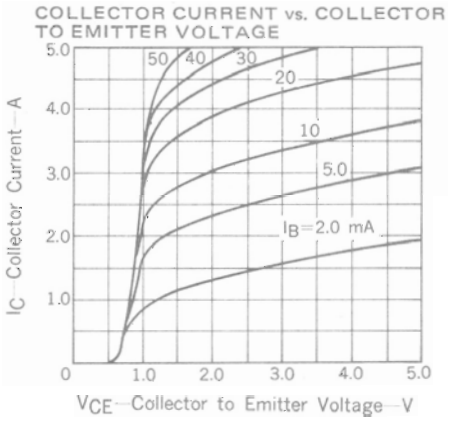
DERATING CURVE OF SAFE OPERATING AREA



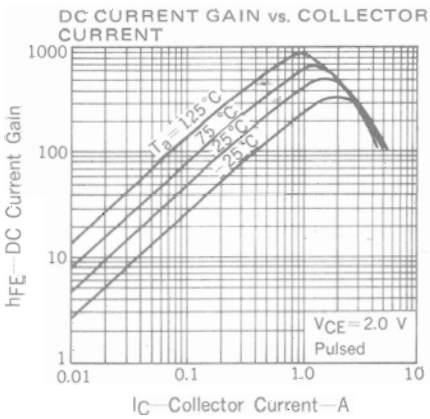
FORWARD BIAS SAFE OPERATING AREA



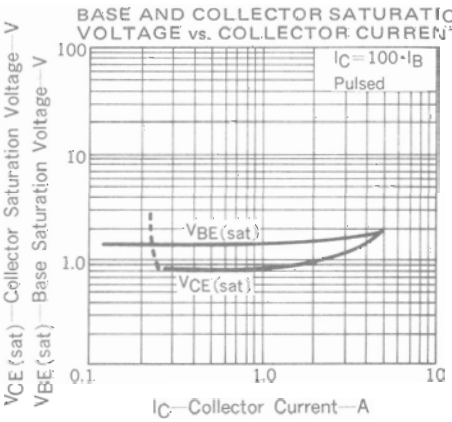
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



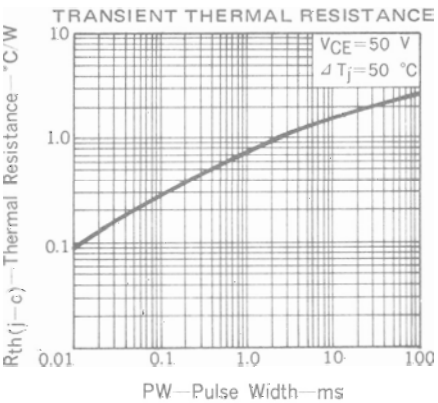
DC CURRENT GAIN vs. COLLECTOR CURRENT



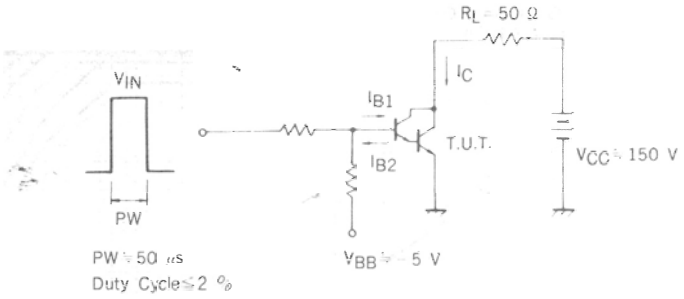
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

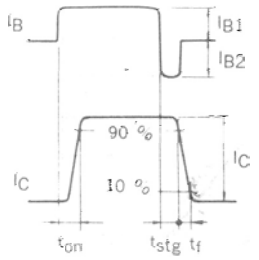


TRANSIENT THERMAL RESISTANCE



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

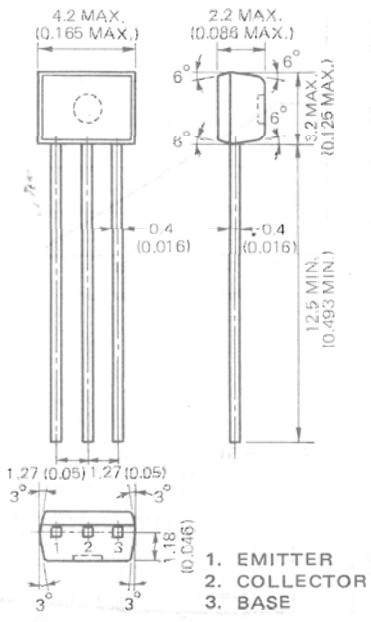
NPN SILICON TRANSISTOR
2SD1020

DESCRIPTION The 2SD1020 is designed for use in output stage of portable RADIO and cassette type tape recorder, general purpose applications.

FEATURES

- High total power dissipation.
  P_T = 350 mW
- High h_{FE} and low $V_{CE(sat)}$
  h_{FE} (I_C = 100 mA) : 200 TYP.
  $V_{CE(sat)}$ (700 mA) : 0.20 V TYP.
- Complementary to the NEC 2SB810 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to + 150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 350 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... 30 V
- V_{CEO} Collector to Emitter Voltage ..... 25 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 700 mA
- I_B Base Current ..... 150 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}*	DC Current Gain	110	200	400	–	V_{CE}=1.0 V, I_C=100 mA
h_{FE2}*	DC Current Gain	50	140		–	V_{CE}=1.0 V, I_C=700 mA
C_{ob}	Collector to Base Capacitance		13	25	pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
f_T	Gain Bandwidth Product	50	170		MHz	V_{CE}=6.0 V, I_E=10 mA
V_{BE}*	Base to Emitter Voltage	600	640	700	mV	V_{CE}=6.0 V, I_C=10 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.2	0.4	V	I_C=700 mA, I_B=70 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.95	1.2	V	I_C=700 mA, I_B=70 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0

*Pulsed PW ≤ 350 μs, duty cycle ≤ 2.0 %

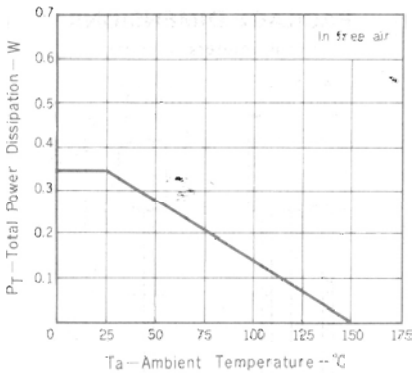
Classification of h_{FE1}

Rank	M	J	H	F	E
Range	110 – 180	135 – 220	170 – 270	200 – 320	250 – 400

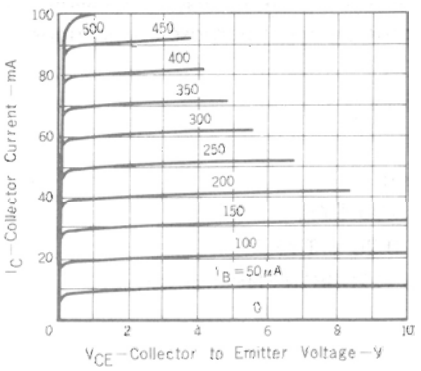
h_{FE1} Test Conditions : V_{CE} = 1.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C unless otherwise noted)

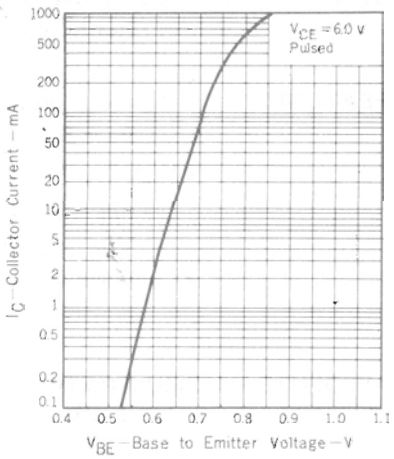
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



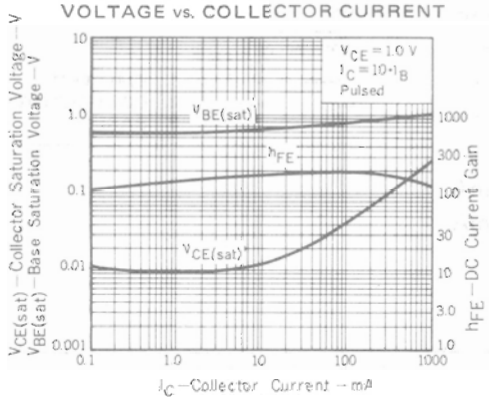
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



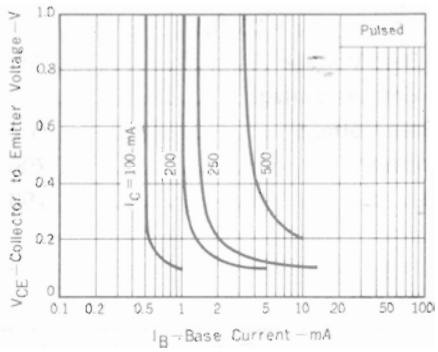
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



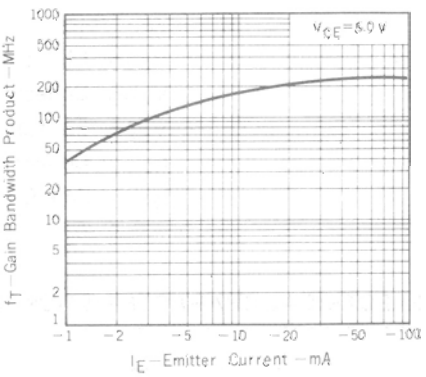
DC CURRENT GAIN, BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



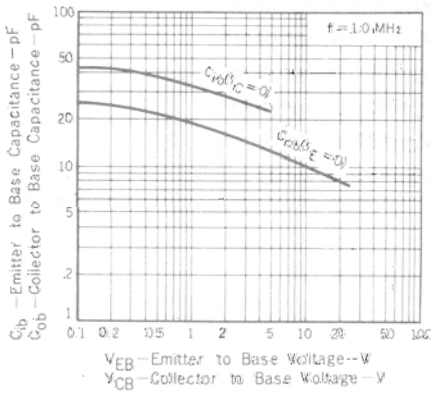
COLLECTOR TO EMITTER VOLTAGE vs. BASE CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



EMITTER TO BASE AND COLLECTOR TO BASE CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

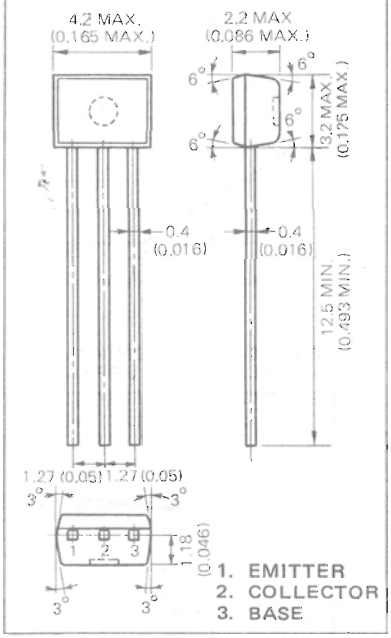
NPN SILICON TRANSISTOR
2SD1021

DESCRIPTION The 2SD1021 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High total power dissipation:
  350 mW at 25 °C Ambient Temperature.
- Complementary to the NEC 2SB811 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −55 to + 150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation ..... 350 mW
- Thermal Resistance (Junction to Ambient) ..... 429 °C/W

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage ..... 30 V
- V_{CEO} Collector to Emitter Voltage ..... 25 V
- V_{EBO} Emitter to Base Voltage ..... 5.0 V
- I_C Collector Current ..... 1.0 A
- I_B Base Current ..... 0.1 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	110	200	400	–	V_{CE}=1.0 V, I_C=0.1 A
h_{FE2}	DC Current Gain	50	140		–	V_{CE}=1.0 V, I_C=1.0 A
f_T	Gain Bandwidth Product		100		MHz	V_{CE}=6.0 V, I_E=10 mA
C_{ob}	Collector to Base Capacitance		22		pF	V_{CB}=6.0 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=30 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=5.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	600	630	700	mV	V_{CE}=6.0 V, I_C=10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.21	0.35	V	I_C=1.0 A, I_B=0.1 A
$V_{BE(sat)}$	Base Saturation Voltage		1.0	1.2	V	I_C=1.0 A, I_B=0.1 A

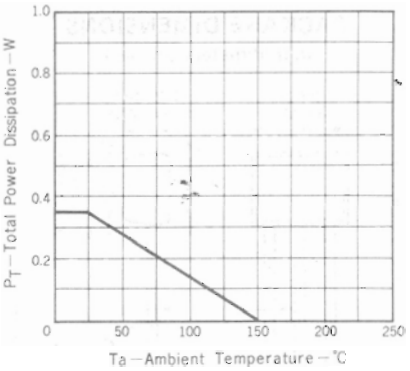
Classification of h_{FE1}

Rank	M	J	H	F	E
Range	110 – 180	135 – 220	170 – 270	200 – 320	250 – 400

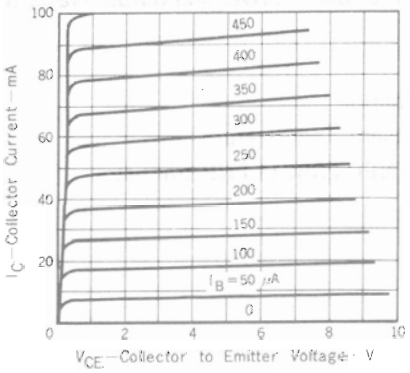
h_{FE1} Test Conditions : V_{CE}=1.0 V, I_C=0.1 A

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

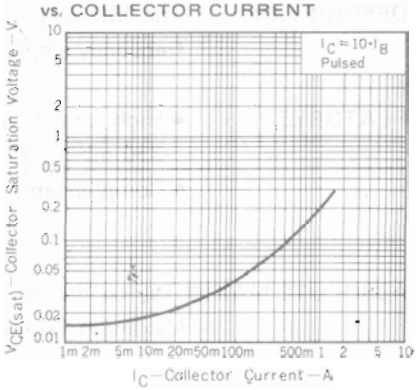
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



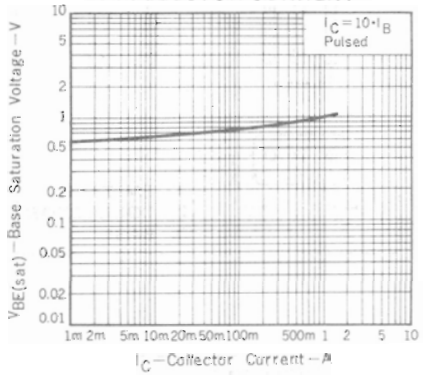
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



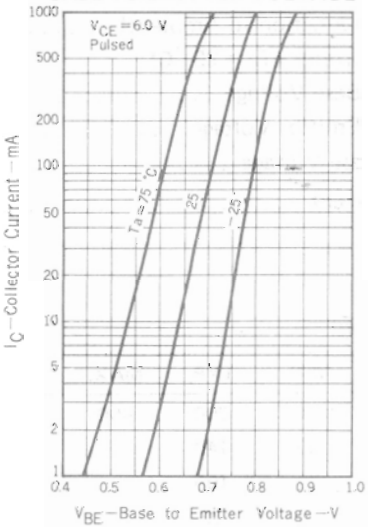
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



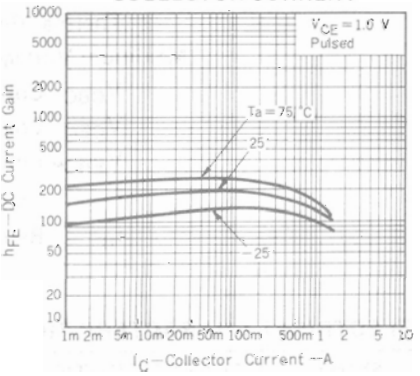
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



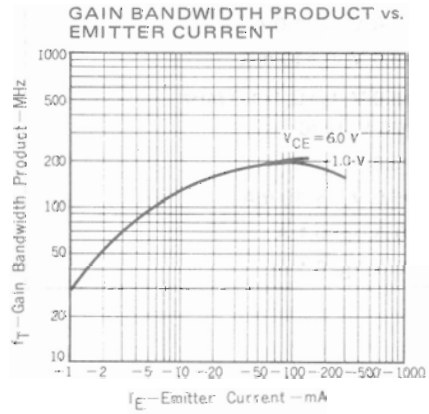
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



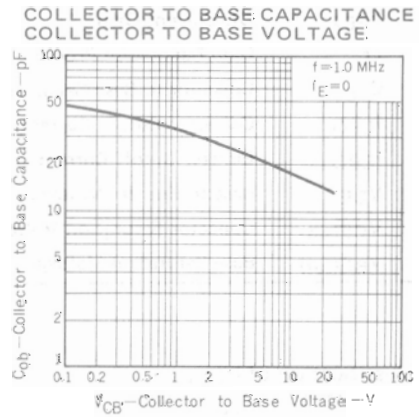
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



COLLECTOR TO BASE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

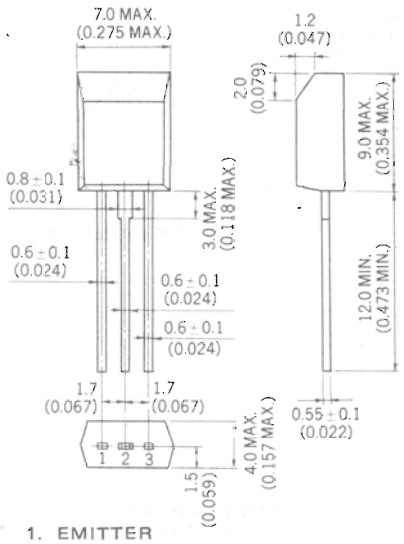
NPN SILICON TRANSISTOR
2SD1312

DESCRIPTION The 2SD1312 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- High total power dissipation and high breakdown voltage: 1.0 W at 25 °C ambient temperature /V_{CEO} = 80 V
- Complementary to the NEC 2SB984 PNP transistor.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 120 V
- V_{CEO} Collector to Emitter Voltage . . . . . 80 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- $I_{C(DC)}$ Collector Current . . . . . 1.0 A
- $I_{C(pulse)}$* Collector Current . . . . . 2.0 A

* PW ≦ 10 ms, duty cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135		600		V_{CE} = 1.0 V, I_C = 200 mA
h_{FE2}	DC Current Gain	75				V_{CE} = 1.0 V, I_C = 500 mA
f_T	Gain Bandwidth Product	50	120		MHz	V_{CE} = 6.0 V, I_E = −200 mA
C_{ob}	Output Capacitance		13	30	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	550	610	650	mV	V_{CE} = 6.0 V, I_C = 10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.25	0.5	V	I_C = 1.0 A, I_B = 100 mA
$V_{BE(sat)}$	Base Saturation Voltage		1.0	1.2	V	I_C = 1.0 A, I_B = 100 mA

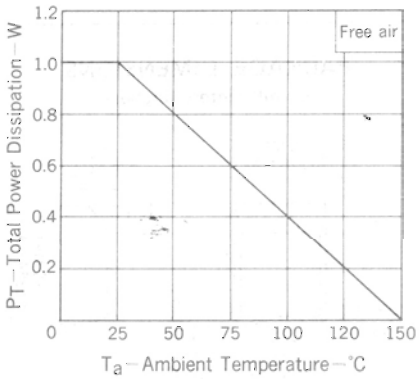
Classification of h_{FE1}

Rank	L	K	U
Range	135−270	200−400	300−600

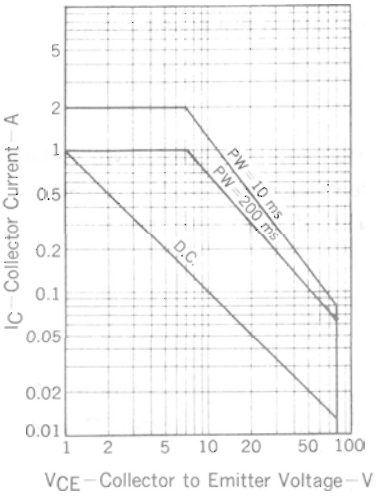
Test Conditions: V_{CE} = 1.0 V, I_C = 200 mA.

TYPICAL CHARACTERISTICS (T_a = 25 °C)

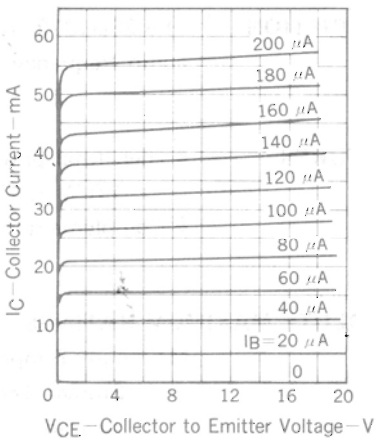
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



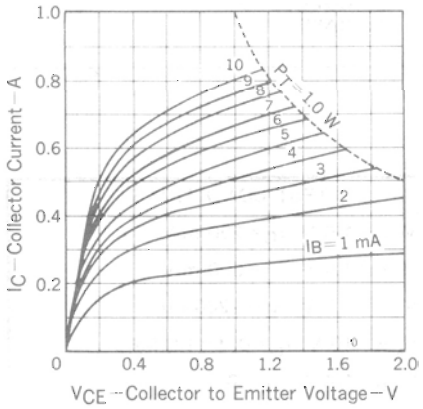
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



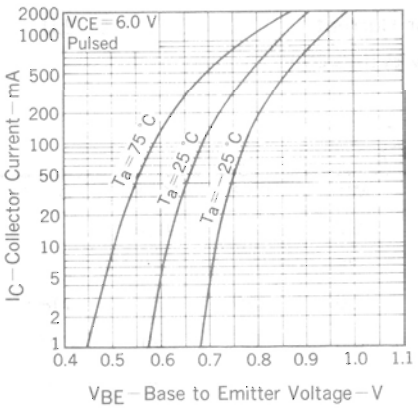
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



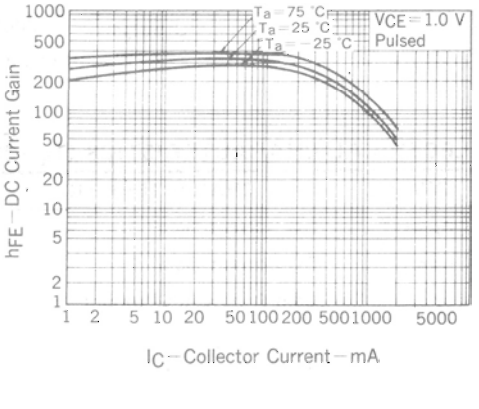
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



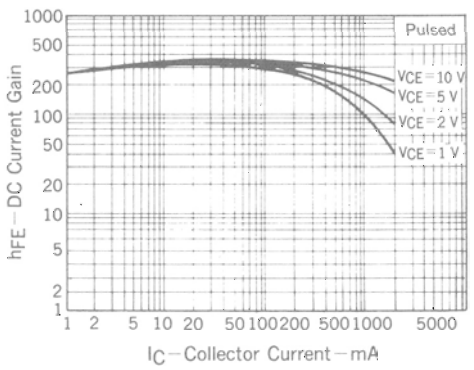
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



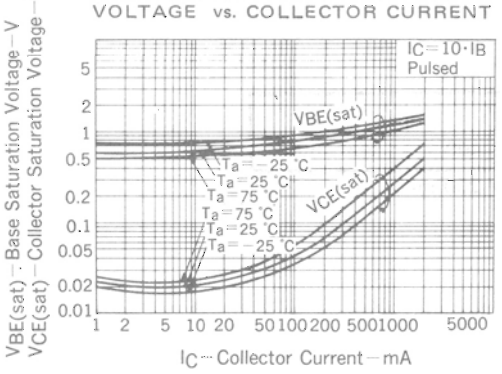
DC CURRENT GAIN vs. COLLECTOR CURRENT



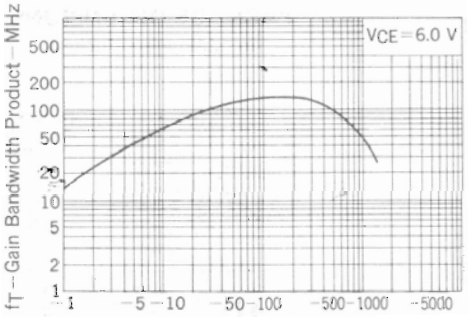
DC CURRENT GAIN vs. COLLECTOR CURRENT



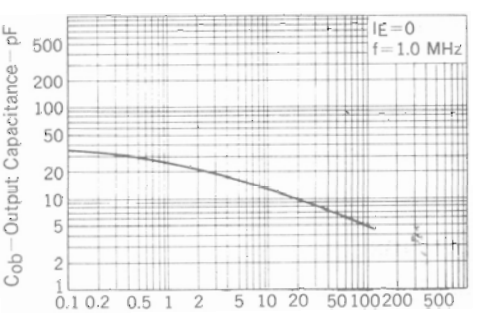
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs.
EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR

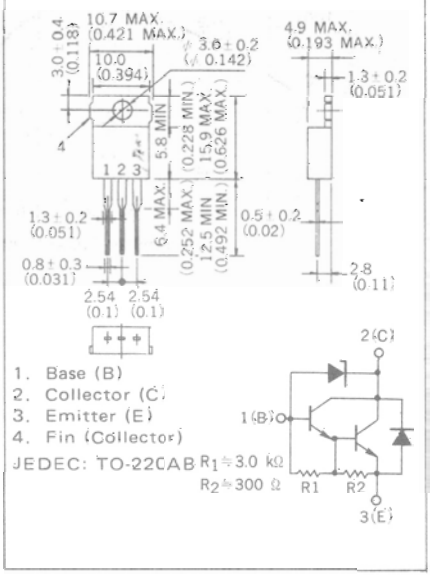
2SD1481

DESCRIPTION The 2SD1481 is NPN silicon epitaxial transistor designed for motor driver and relay driver applications.

FEATURES

- Low collector saturation voltage.
- Operates from IC without predriver.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_c = 25 °C)

- Total Power Dissipation . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60±10 V
V_{CEO}	Collector to Emitter Voltage	60±10 V
V_{EBO}	Emitter to Base Voltage	7.0 V
$I_{C(DC)}$	Collector Current (DC)	2.0 A
$I_{C(pulse)}$	Collector Current (Pulse)*	4.0 A
$I_{B(DC)}$	Base Current (DC)	0.2 A

*PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	2000		20000	—	V_{CE} = 2.0 V, I_C = 1.0 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = 2.0 V, I_C = 3.0 A
t_{on}	Turn On Time		0.5		μs	I_C = 1.0 A, I_{B1} = −I_{B2} = 10 mA
t_{stg}	Storage Time		2.0		μs	R_L = 50 Ω, V_{CC} ≒ 50 V
t_f	Fall Time		1.0		μs	See Test Circuit.
$V_{CE(sat)}$	Collector Saturation Voltage**			1.5	V	I_C = 1.0 A, I_B = 1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage**			2.0	V	I_C = 1.0 A, I_B = 1.0 mA
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 40 V, I_E = 0

**Pulse Test : PW ≤ 350 μs, Duty Cycle ≤ 2 %/Pulsed

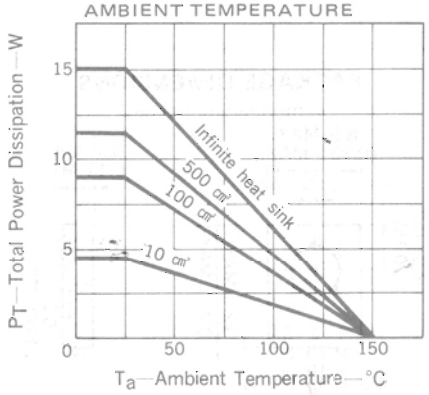
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 20000

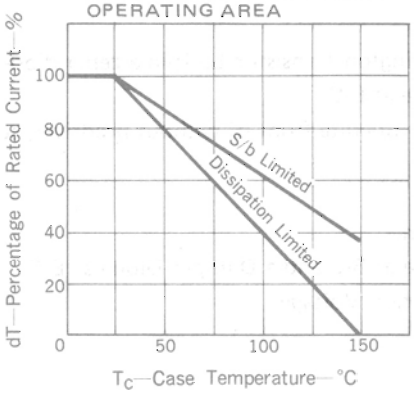
Test Conditions : V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

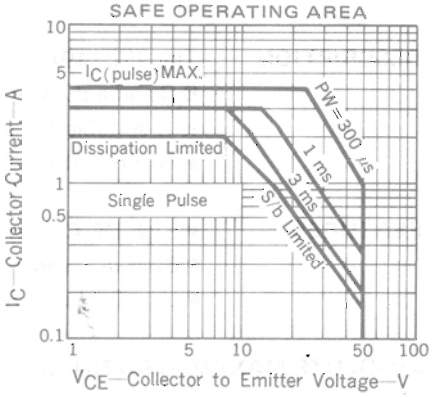
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



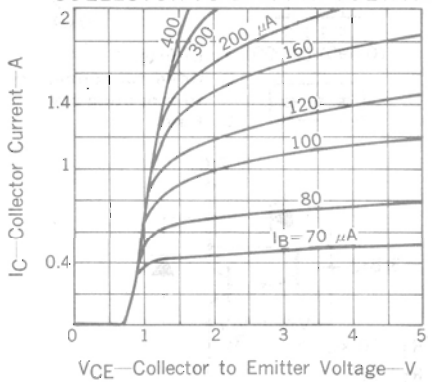
DERATING CURVE OF SAFE OPERATING AREA



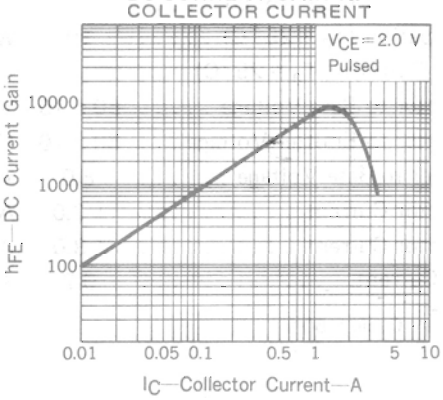
SAFE OPERATING AREA



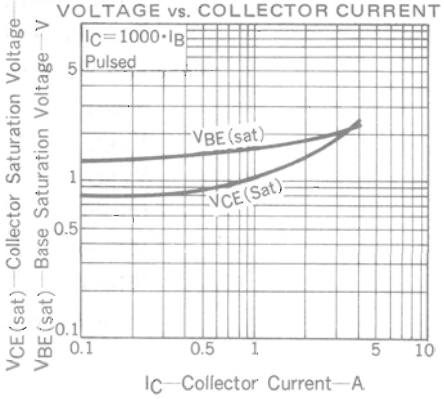
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



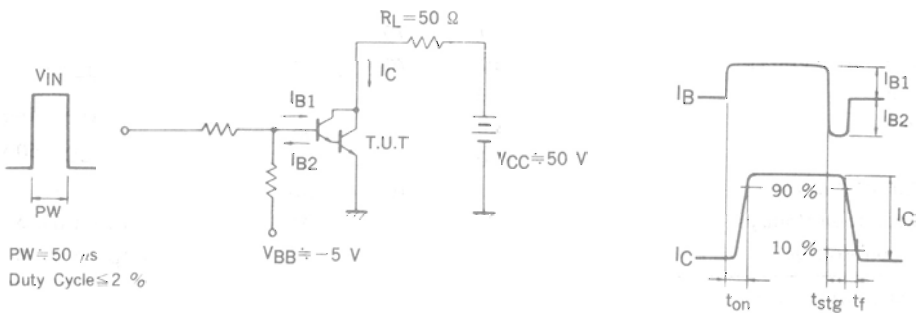
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



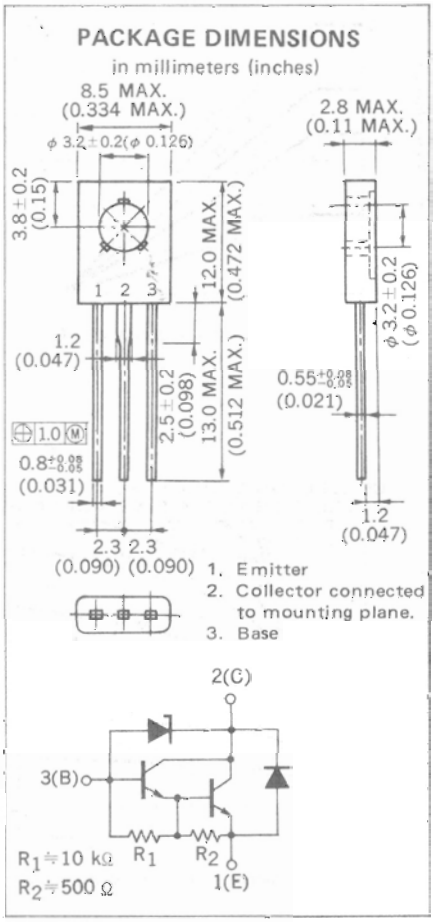
NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR
2SD1491

DESCRIPTION The 2SD1491 is a darlington transistor built-in a zener diode at B-C and a dumper diode at E-C.
It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES
- High DC Current Gain.
- Built-in a Zener Diode at B-C and a Dumper Diode at E-C.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	+150 Maximum	°C

Maximum Power Dissipations

Total Power Dissipation (T_a = 25 °C)	1.0	W
Total Power Dissipation (T_c = 25 °C)	10	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60 ± 10	V
V_{CEO}	Collector to Emitter Voltage	60 ± 10	V
V_{EBO}	Emitter to Base Voltage	8.0	V
$I_{C(DC)}$	Collector Current	± 2.0	A
$I_{C(pulse)}$*	Collector Current	± 3.0	A
$I_{B(DC)}$	Base Current	0.2	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	1000			—	V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2} **	DC Current Gain	2000		20000	—	V_{CE} = 2.0 V, I_C = 1.0 A
V_{CBO}	Collector to Base Voltage	50	60	70	V	I_C = 1.0 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 10 mA, R_{BE} = ∞
t_{on}	Turn On Time		0.5		μs	I_C = 1.0 A, I_{B1} = −I_{B2} = 1.0 mA, R_L = 50 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time		3.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 40 V, I_E = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage			1.5	V	I_C = 1.0 A, I_B = 1.0 mA
$V_{BE(sat)}$ **	Base Saturation Voltage			2.0	V	I_C = 1.0 A, I_B = 1.0 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

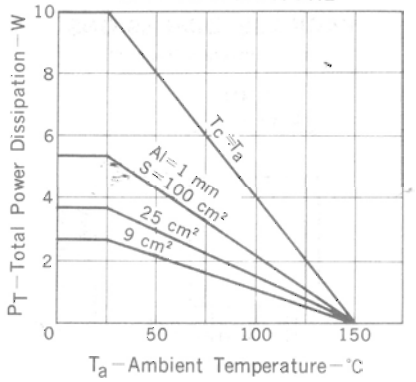
Classification of h_{FE2}

Rank	M	L	K
Range	2000 to 6000	4000 to 12000	10000 to 20000

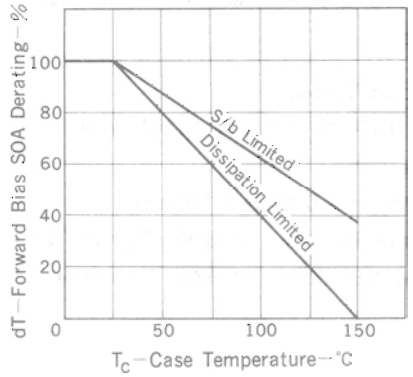
Test Conditions: V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

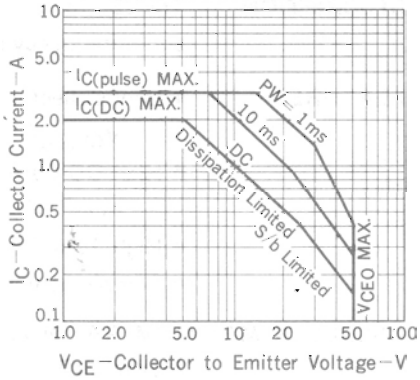
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



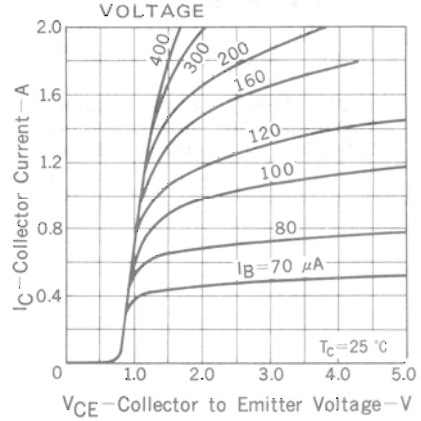
DERATING CURVE OF SAFE OPERATING AREA



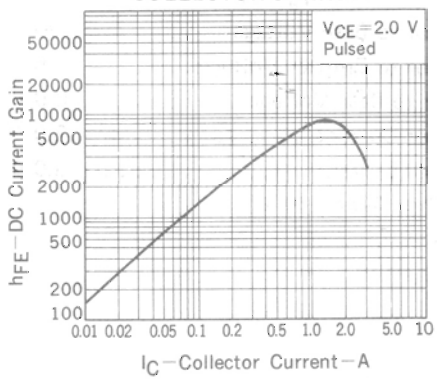
SAFE OPERATING AREA



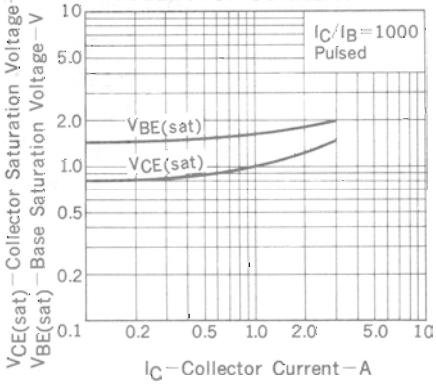
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



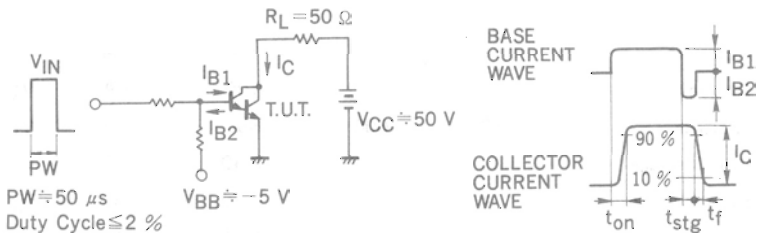
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

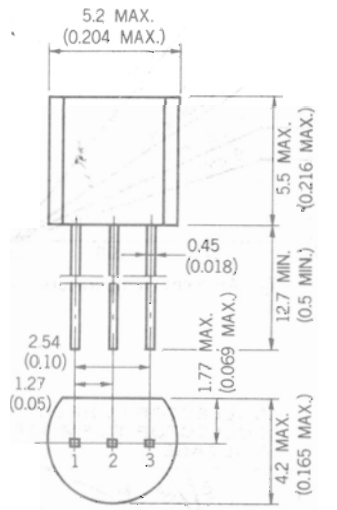
NPN SILICON TRANSISTOR
2SD1513

DESCRIPTION The 2SD1513 is designed for use in driver and output stages of audio frequency amplifiers.

FEATURES

- Low Collector Saturation Voltage
  $V_{CE(sat)}$: 0.20 V TYP. (I_C = 1.0 A, I_B = 10 mA)
- High DC Current Gain
  h_{FE} : 350 TYP. (V_{CE} = 2.0 V, I_C = 100 mA)
- High Total Power Dissipation P_T : 0.75 W (T_a = 25 °C)
- Complementary to The NEC 2SB1068 PNP Transistor

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 20 V
- V_{CEO} Collector to Emitter Voltage . . . . . 16 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- $I_{C(DC)}$ Collector Current . . . . . 2.0 A
- $I_{C(pulse)}$* Collector Current . . . . . 3.0 A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	135	350	650	–	V_{CE} = 2.0 V, I_C = 100 mA
h_{FE2}	DC Current Gain	100			–	V_{CE} = 2.0 V, I_C = 1.5 A
f_T	Gain Bandwidth Product	100	200		MHz	V_{CE} = 10 V, I_E = 50 mA
C_{ob}	Output Capacitance		28		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 16 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	550	600	650	mV	V_{CE} = 6.0 V, I_C = 5.0 mA
$V_{CE(sat)1}$	Collector Saturation Voltage		0.20	0.40	V	I_C = 1.0 A, I_B = 10 mA
$V_{CE(sat)2}$	Collector Saturation Voltage		0.23	0.50	V	I_C = 1.5 A, I_B = 75 mA
$V_{CE(sat)3}$	Collector Saturation Voltage		0.26	0.50	V	I_C = 1.5 A, I_B = 20 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.95	1.2	V	I_C = 1.5 A, I_B = 75 mA

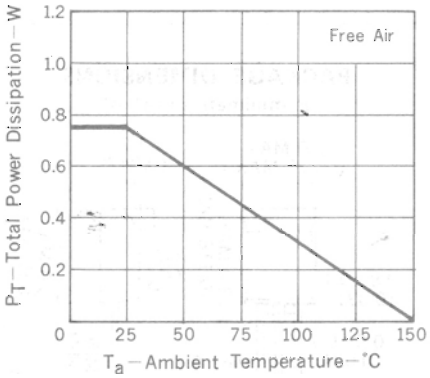
Classification of h_{FE}

Rank	L	K	U
Range	135 – 270	200 – 400	300 – 650

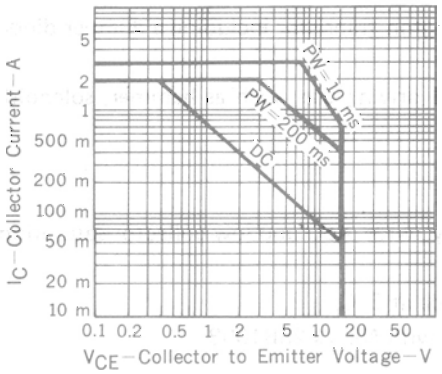
Test Conditions : V_{CE} = 2.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

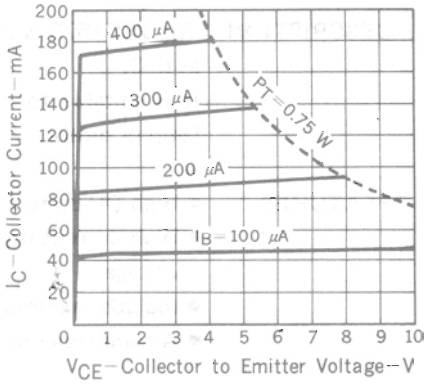
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



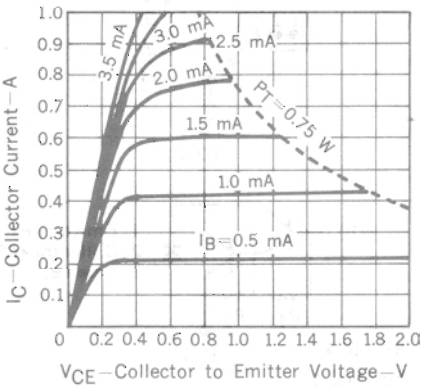
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



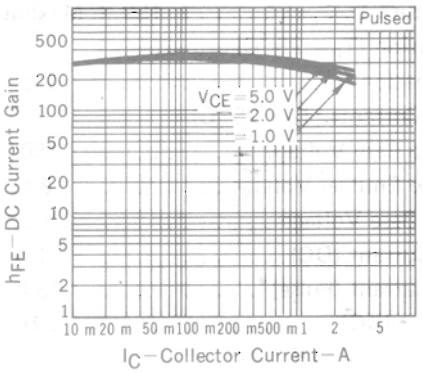
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



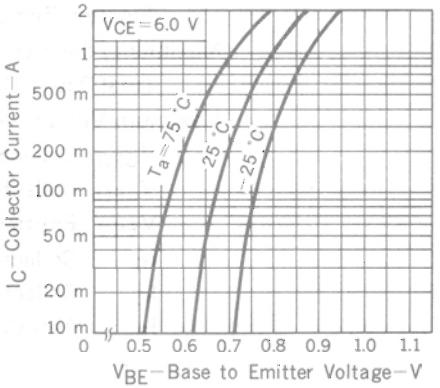
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



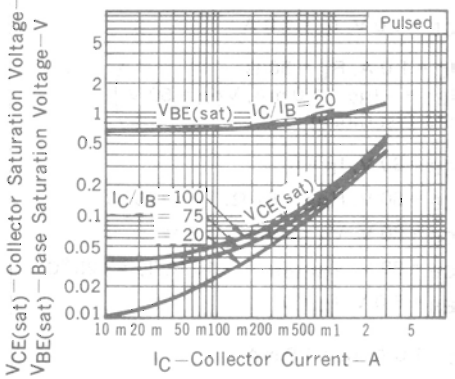
DC CURRENT GAIN vs. COLLECTOR CURRENT



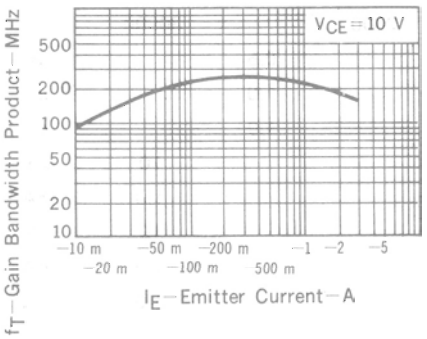
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



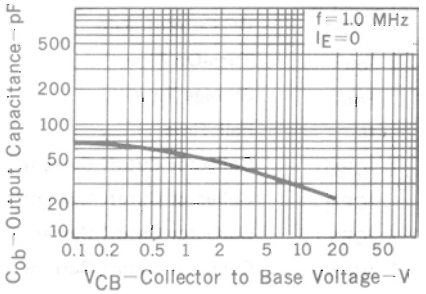
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



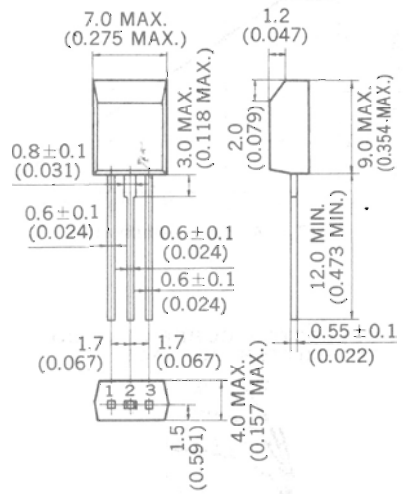
NEC
ELECTRON DEVICE

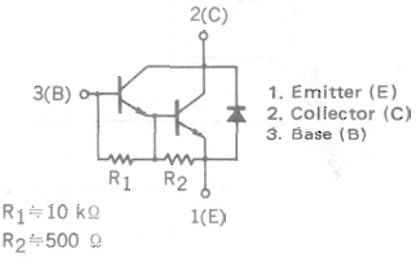
NPN SILICON DARLINGTON TRANSISTOR
2SD1579

DESCRIPTION The 2SD1579 is a darlington transistor including a dumper diode at E-C.
It is suitable for general driving use, such as hammer, solenoid, lamp or motor.

FEATURES
- High DC current gain.
- High current capability, wide ASO and low collector saturation voltage.
- Includes a dumper diode at E-C.
- A complementary pair with NEC's 2SB1093.

PACKAGE DIMENSIONS
in millimeters (inches)





ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	150 Maximum	°C

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation	1.0	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	80	V
V_{EBO}	Emitter to Base Voltage	8.0	V
I_C	Collector Current (DC)	±1.5	A
I_C	Collector Current (Pulse)*	±3.0	A
I_B	Base Current (DC)	0.15	A

*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	1000			—	V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2}	DC Current Gain	2000		30000	—	V_{CE} = 2.0 V, I_C = 1.0 A
t_{on}	Turn-On Time		0.5		μs	(I_C = 1.0 A, R_L = 50 Ω, I_{B1} = −I_{B2} = 1.0 mA, V_{CC} = 50 V, See Test Circuit)
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 80 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 80 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 80 V, $V_{BE(off)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 80 V, $V_{BE(off)}$ = −1.5 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			1.5	V	I_C = 1.0 A, I_B = 1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage			2.0	V	
f_T	Gain Bandwidth Product		60		MHz	V_{CE} = 10 V, I_E = −1.0 A

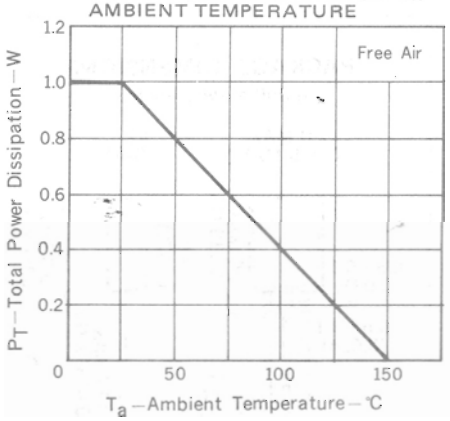
Classification of h_{FE2}

Rank	M	L	K
Range	2000 – 5000	4000 – 10000	8000 – 30000

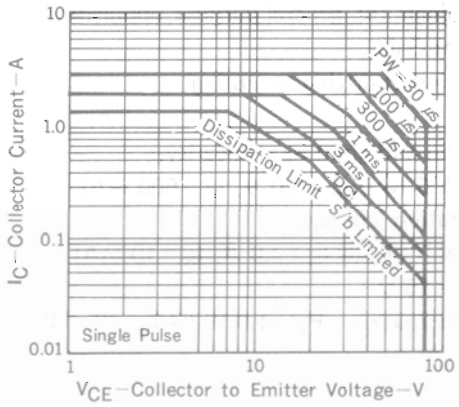
Test Conditions: V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

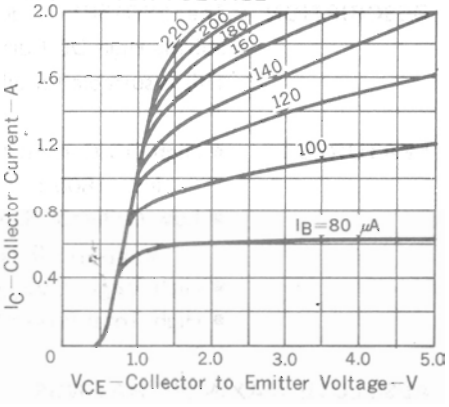
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



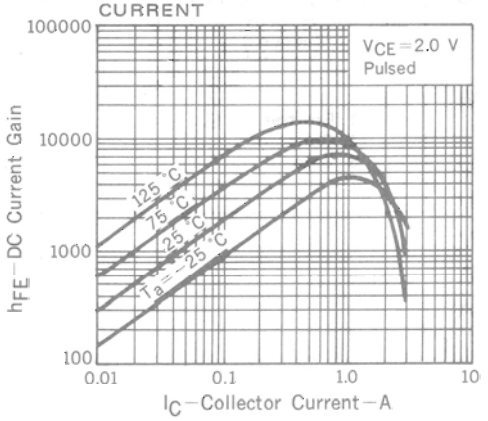
SAFE OPERATING AREAS



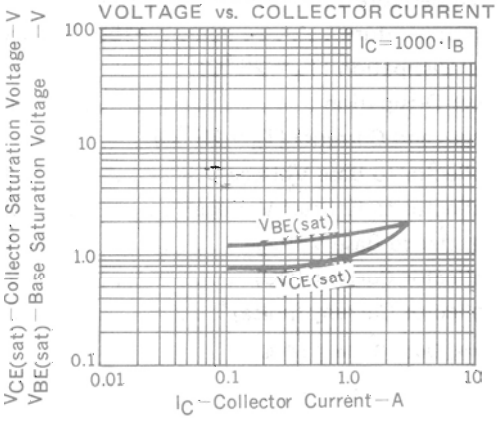
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



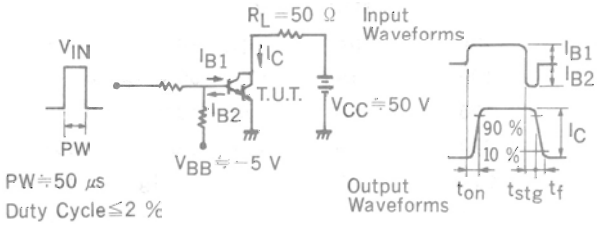
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CURCUIT



NEC
ELECTRON DEVICE

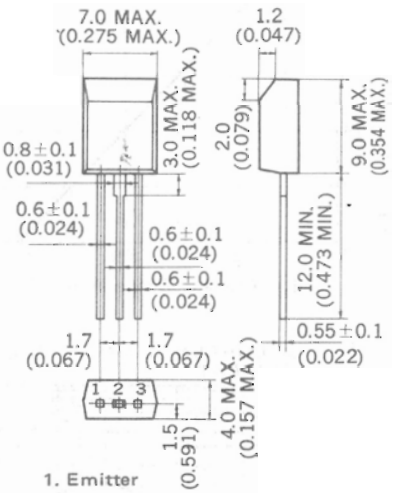
NPN SILICON TRANSISTOR
2SD1581

DESCRIPTION The 2SD1581 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving or muting.

FEATURES

- High DC Current Gain and good h_{FE} linearity.
  h_{FE} = 800 to 3 200 (@ V_{CE} = 5.0 V, I_C = 500 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.22 V TYP. (@ I_C = 1.0 A, I_B = 10 mA)
- High V_{EBO} : V_{EBO} = 15 V
- High Total Power Dissipation : P_T = 1.0 W, (@ T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	+150	°C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation	1.0	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	30	V
V_{CEO}	Collector to Emitter Voltage	25	V
V_{EBO}	Emitter to Base Voltage	15	V
I_C	Collector Current (DC)	2.0	A
I_C	Collector Current (pulse)*	3.0	A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	800	1500	3200	–	V_{CE} = 5.0 V, I_C = 500 mA
h_{FE2}	DC Current Gain	400			–	V_{CE} = 5.0 V, I_C = 2.0 A
f_T	Gain Bandwidth Product	150	350		MHz	V_{CE} = 10 V, I_E = −500 mA
C_{ob}	Output Capacitance		26	35	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600	630	700	mV	V_{CE} = 5.0 V, I_C = 100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.22	0.30	V	I_C = 1.0 A, I_B = 10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.90	1.2	V	I_C = 1.0 A, I_B = 10 mA

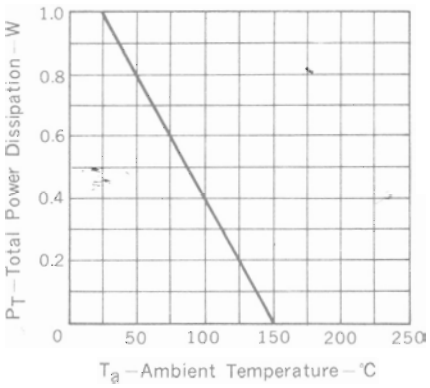
Classification of h_{FE1}

Rank	M	L	K
Range	800 – 1600	1200 – 2400	2000 – 3200

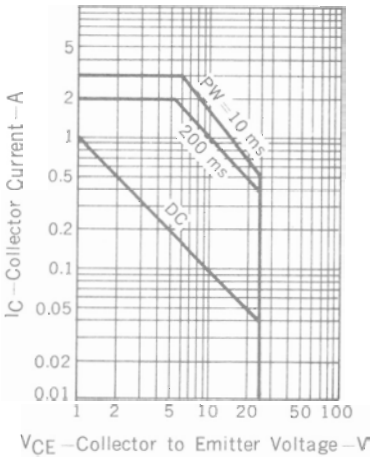
Test Conditions: V_{CE} = 5.0 V, I_C = 500 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

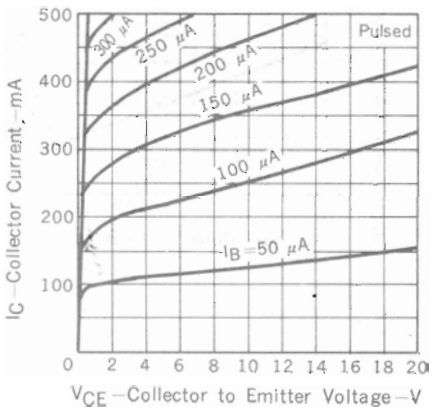
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



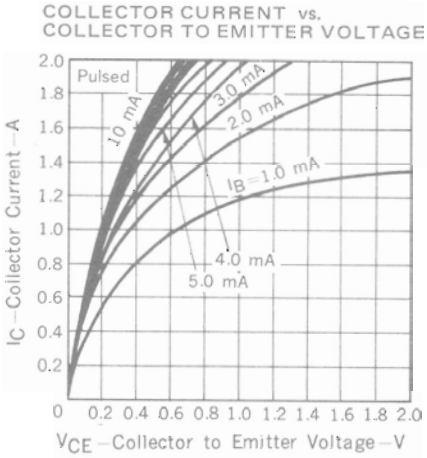
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



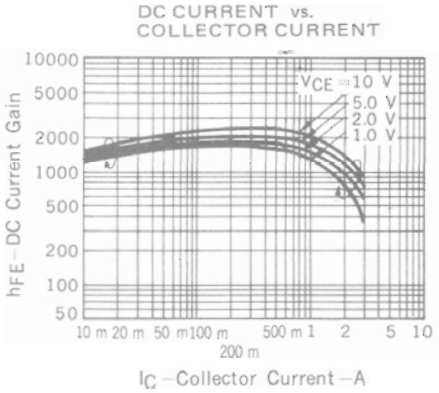
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



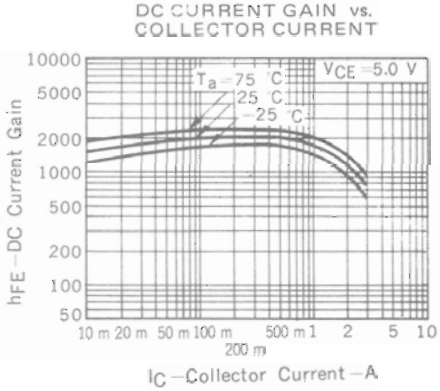
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



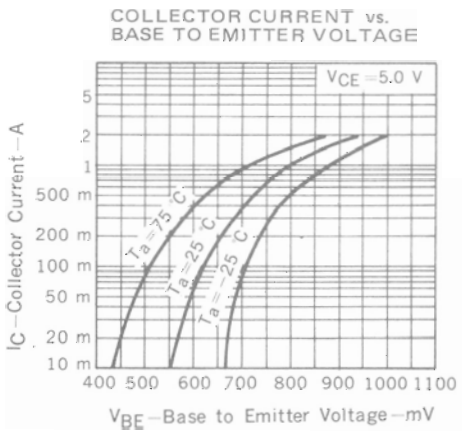
DC CURRENT vs. COLLECTOR CURRENT



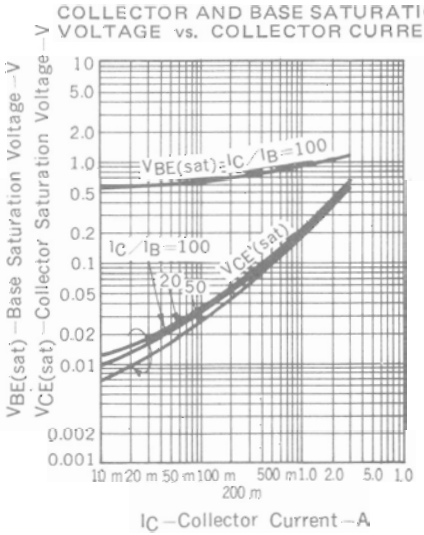
DC CURRENT GAIN vs. COLLECTOR CURRENT



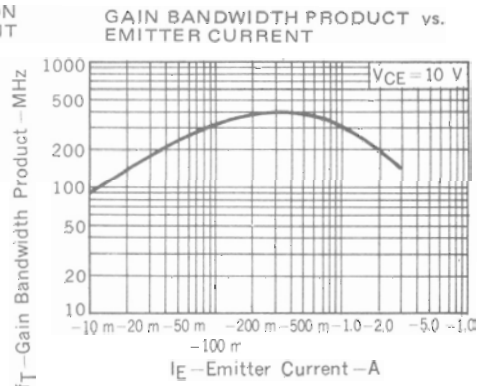
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



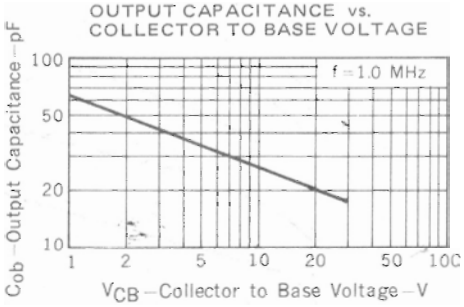
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

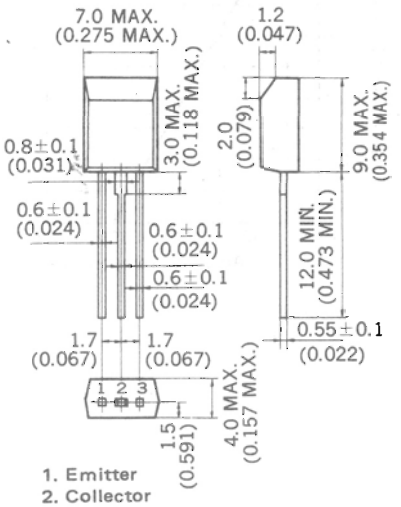
NPN SILICON TRANSISTOR
2SD1582

DESCRIPTION The 2SD1582 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving or muting.

FEATURES

- High DC Current Gain and good h_{FE} linearity.
  h_{FE} = 800 to 3200 (@ V_{CE} = 5.0 V, I_C = 300 mA)
- High Voltage and Wide "SOA".
  V_{CEO} = 50 V, V_{EBO} = 15 V
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.17 V TYP. (@ I_C = 500 mA, I_B = 5.0 mA)
- High Total Power Dissipation : P_T = 1.0 W (@ T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 15 V
- I_C Collector Current (DC) . . . . . 1.0 A
- I_C Collector Current (pulse)* . . . . . 1.5 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	800	1500	3200	—	V_{CE} = 5.0 V, I_C = 300 mA
h_{FE2}	DC Current Gain	400			—	V_{CE} = 5.0 V, I_C = 1.0 A
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 10 V, I_E = −500 mA
C_{ob}	Output Capacitance		18	30	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600	630	700	mV	V_{CE} = 5.0 V, I_C = 100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.17	0.30	V	I_C = 500 mA, I_B = 5.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.80	1.2	V	I_C = 500 mA, I_B = 5.0 mA

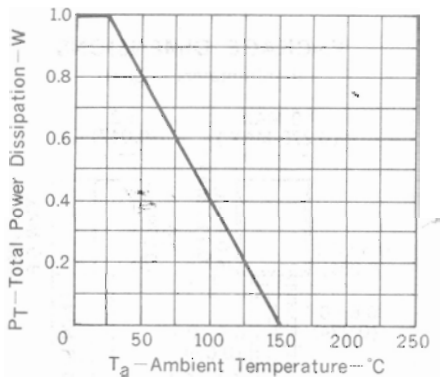
Classification of h_{FE1}

Rank	M	L	K
Range	800 – 1600	1200 – 2400	2000 – 3200

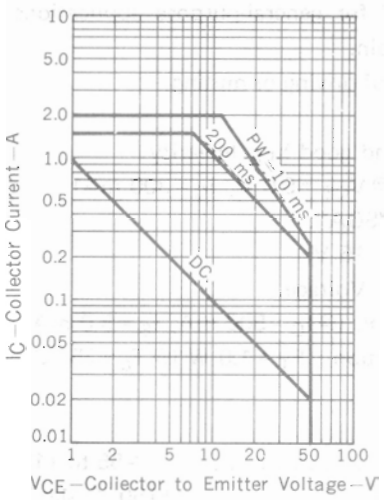
Test Conditions: V_{CE} = 5.0 V, I_C = 300 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

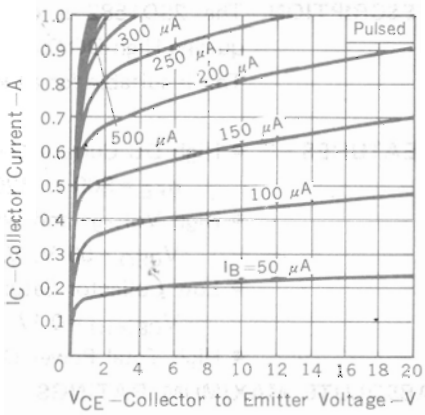
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



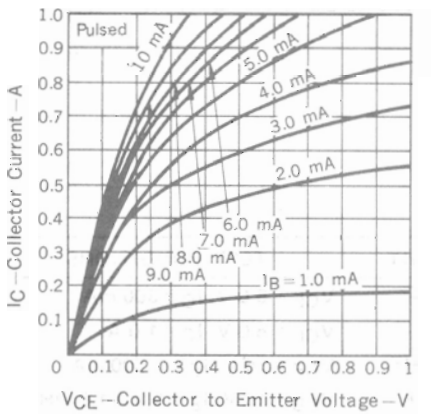
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



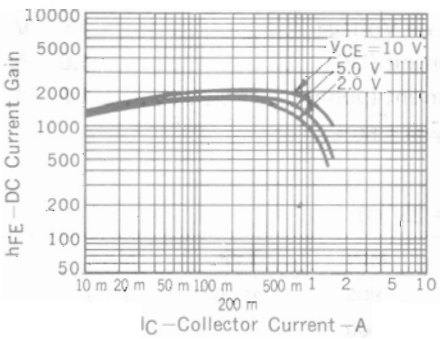
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



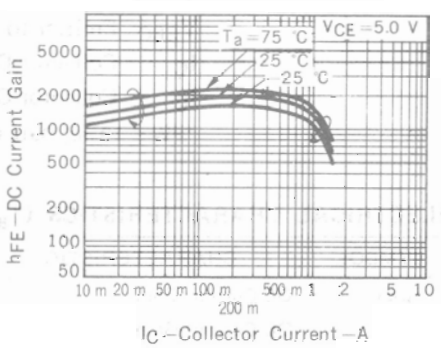
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



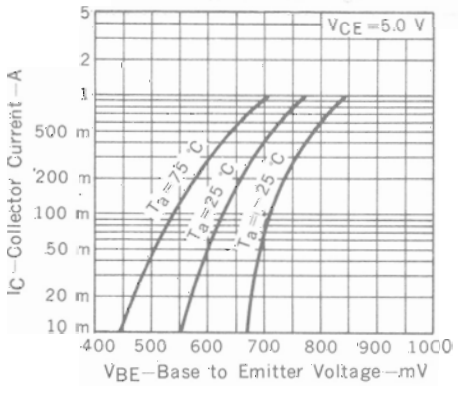
DC CURRENT GAIN vs. COLLECTOR CURRENT



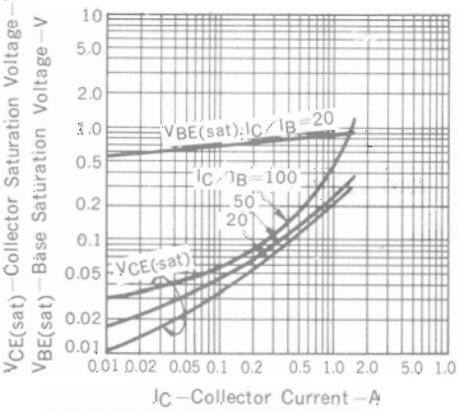
DC CURRENT GAIN vs. COLLECTOR CURRENT



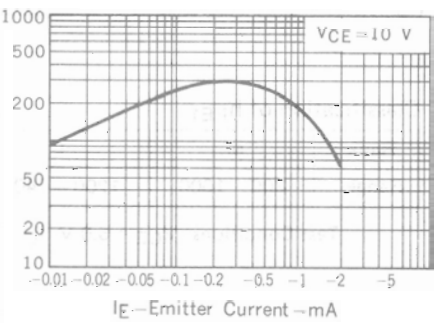
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



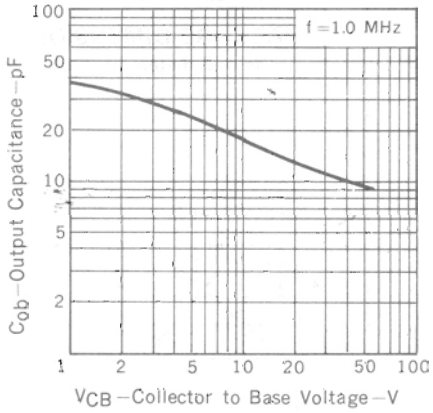
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SD1585

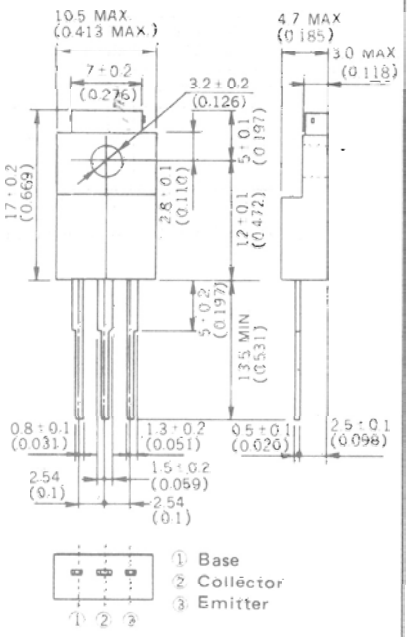
NEW DEVICE

DESCRIPTION The 2SD1585 is an NPN general purpose transistor designed for use in audio frequency power amplifier.

FEATURES

- Easy mount by eliminating Sheet and Bushing.
- Complementary to the 2SB1094.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation (T_a = 25 °C)		2.0	W
Total Power Dissipation (T_C = 25 °C)		15	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage . . .	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	3.0	A
$I_{C(pulse)}$	Collector Current (Pulse)*	5.0	A
$I_{B(pulse)}$	Base Current (DC)	0.6	A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	20				V_{CE} = 5.0 V, I_C = 50 mA
h_{FE2}**	DC Current Gain	40		200		V_{CE} = 5.0 V, I_C = 0.5 A
f_T	Gain Bandwidth Product		16		MHz	V_{CE} = 5.0 V, I_C = 0.1 A
C_{ob}	Output Capacitance		48		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage			1.5	V	I_C = 2.0 A, I_B = 0.2 A
$V_{BE(sat)}$**	Base Saturation Voltage			2.0	V	I_C = 2.0 A, I_B = 0.2 A

**Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

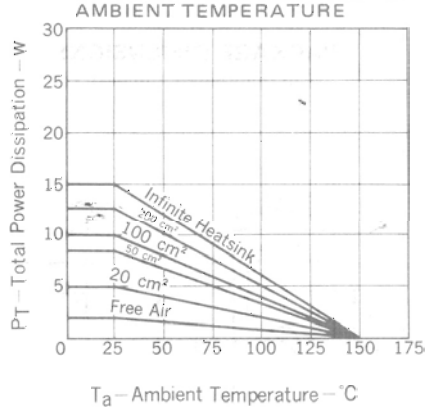
Classification of h_{FE2}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

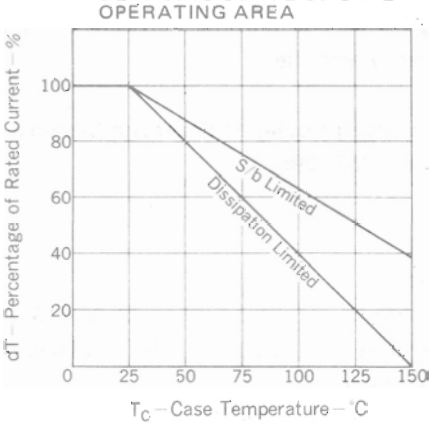
Test Conditions: V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

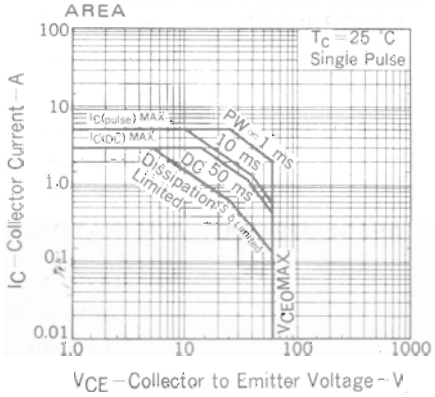
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



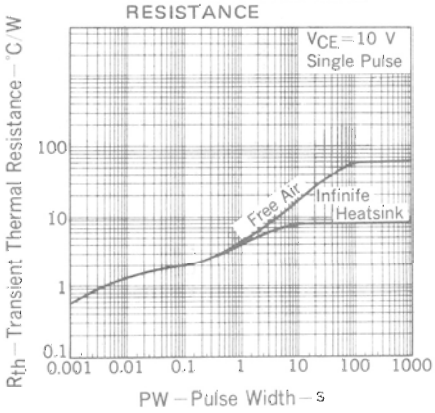
DERATING CURVE OF SAFE OPERATING AREA



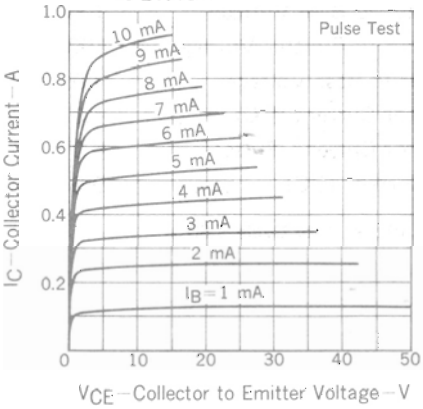
FORWARD BIAS SAFE OPERATING AREA



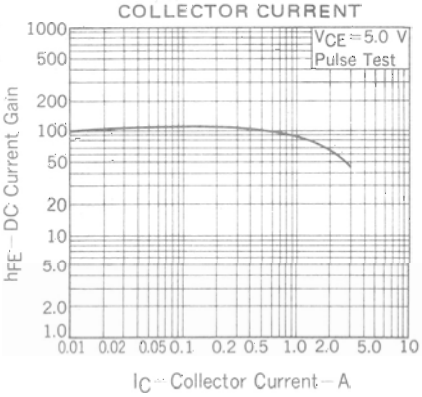
TRANSIENT THERMAL RESISTANCE



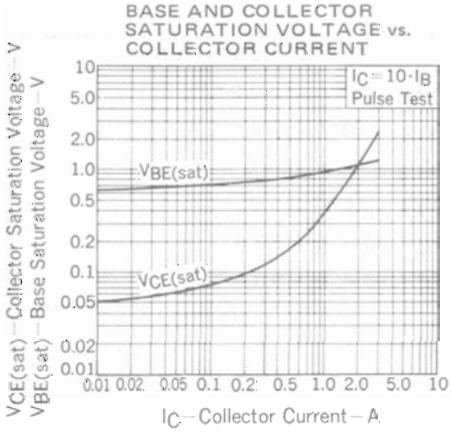
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



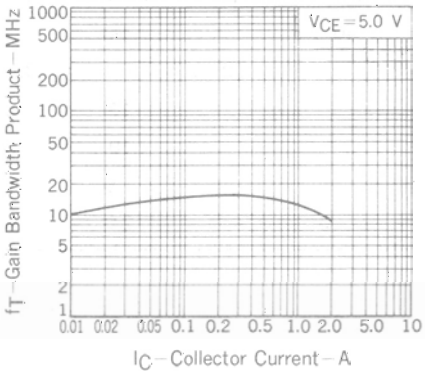
DC CURRENT GAIN vs. COLLECTOR CURRENT



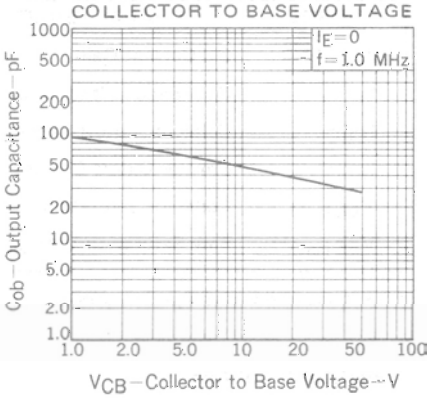
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

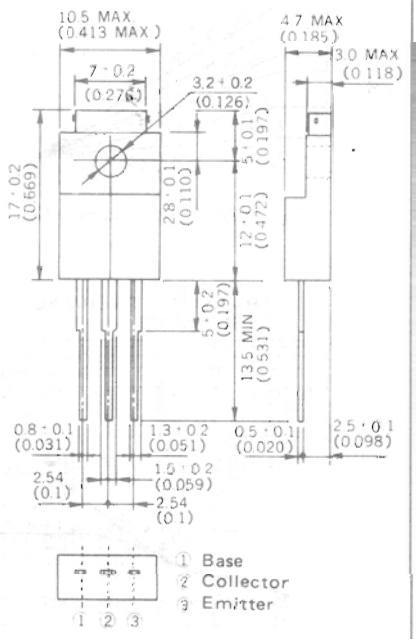
NPN SILICON POWER TRANSISTOR
2SD1586

DESCRIPTION The 2SD1586 is an NPN general purpose transistor designed for use in Audio frequency amplifier.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Complementary to the 2SB1095.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . 2.0 W
- Total Power Dissipation (T_C = 25 °C) . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 100 V
- V_{CEO} Collector to Emitter Voltage . . . 100 V
- V_{EBO} Emitter to Base Voltage . . . . . 7.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 4.0 A
- $I_{C(pulse)}$ Collector Current (Pulse)* . . . . 6.0 A
- $I_{B(DC)}$ Base Current (DC) . . . . . 0.6 A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}**	DC Current Gain	40		200		V_{CE} = 5.0 V, I_C = 0.5 A
f_T	Gain Bandwidth Product		20		MHz	V_{CE} = 5.0 V, I_C = 0.1 A
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage			1.5	V	I_C = 3.0 A, I_B = 0.3 A
$V_{BE(sat)}$**	Base Saturation Voltage			2.0	V	I_C = 3.0 A, I_B = 0.3 A

**Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

Classification of h_{FE}

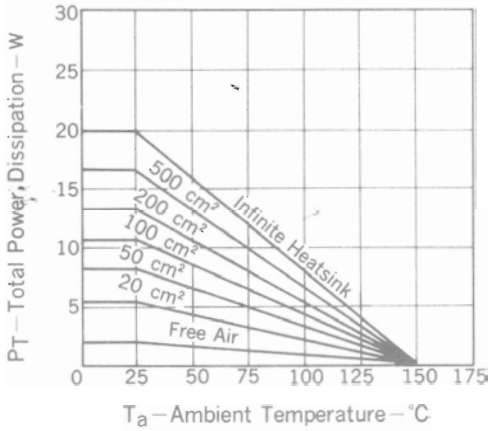
Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

Test Conditions: V_{CE} = 5.0 V, I_C = 0.5 A

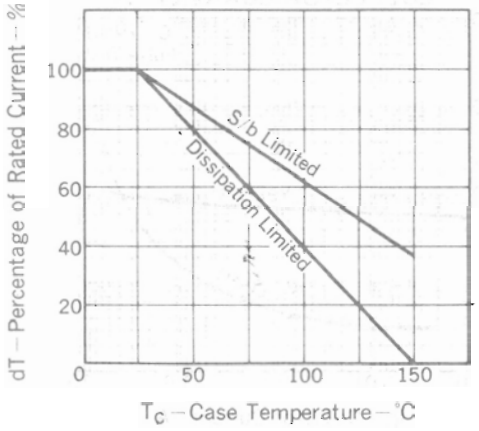
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

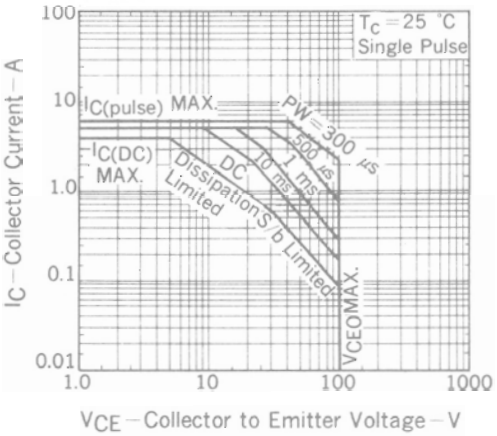
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



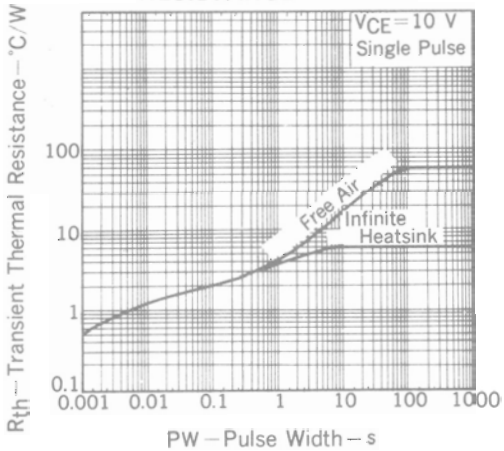
DERATING CURVE OF SAFE OPERATING AREA



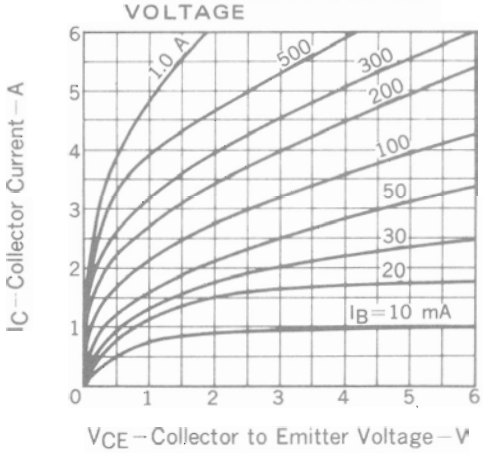
FORWARD BIAS SAFE OPERATING AREA



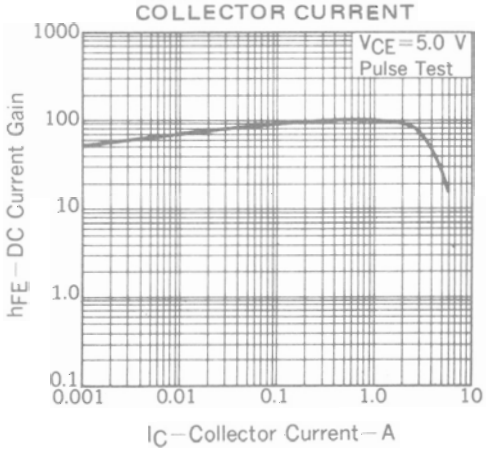
TRANSIENT THERMAL RESISTANCE



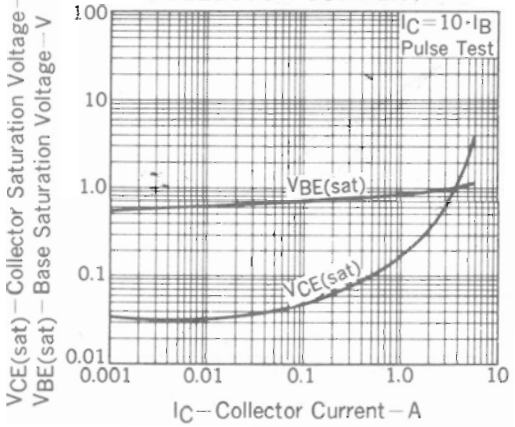
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



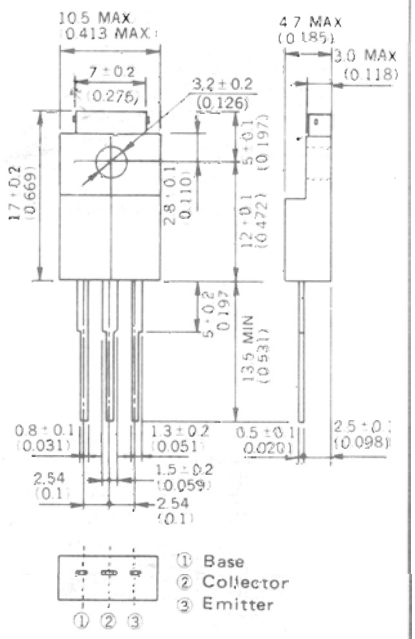
NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SD1587

DESCRIPTION The 2SD1587 is an NPN general purpose transistor designed for use in audio frequency amplifier.

FEATURES
- Easy mount by eliminating Insulation Sheet and Bushing.
- Complementary to the 2SB1096.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations
- Total Power Dissipation (T_a = 25 °C) . . . . 2.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	200	V
V_{CEO}	Collector to Emitter Voltage . . .	150	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	2.0	A
$I_{C(pulse)}$	Collector Current (Pulse)*	3.0	A
$I_{B(DC)}$	Base Current (DC)	1.0	A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

NEW DEVICE

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}**	DC Current Gain	40				V_{CE} = 10 V, I_C = 0.4 A
f_T	Gain Bandwidth Product		5		MHz	V_{CE} = 10 V, I_C = 0.4 A
I_{CBO}	Collector Cutoff Current			50	μA	V_{CB} = 150 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			50	μA	V_{EB} = 4.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage			1.0	V	I_C = 500 mA, I_B = 50 mA

**Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

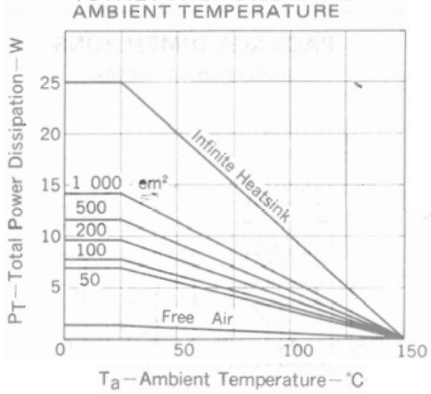
Classification of h_{FE}

Rank	M	L	K
Range	40 to 80	60 to 120	100 to 200

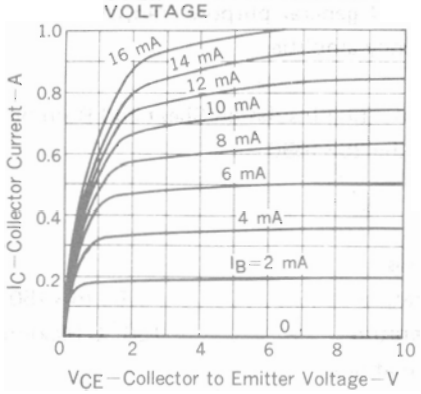
Test Conditions: V_{CE} = 10 V, I_C = 0.4 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

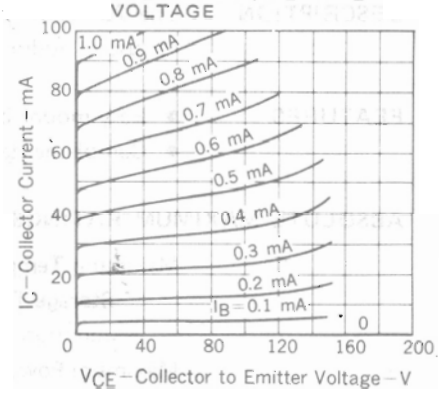
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



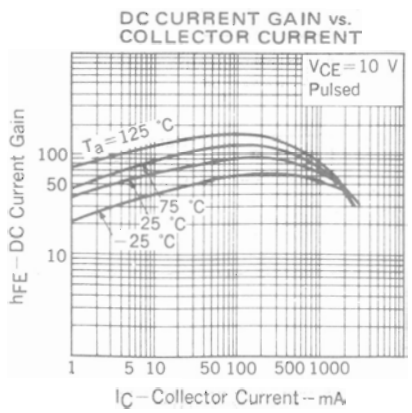
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



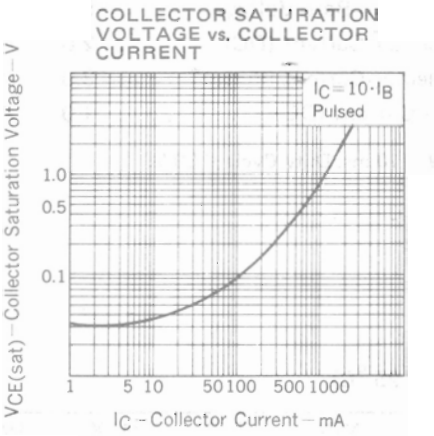
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



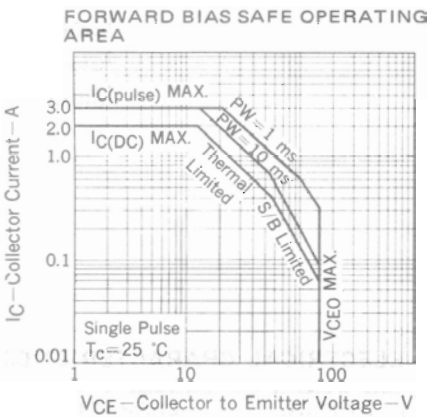
DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



FORWARD BIAS SAFE OPERATING AREA



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR

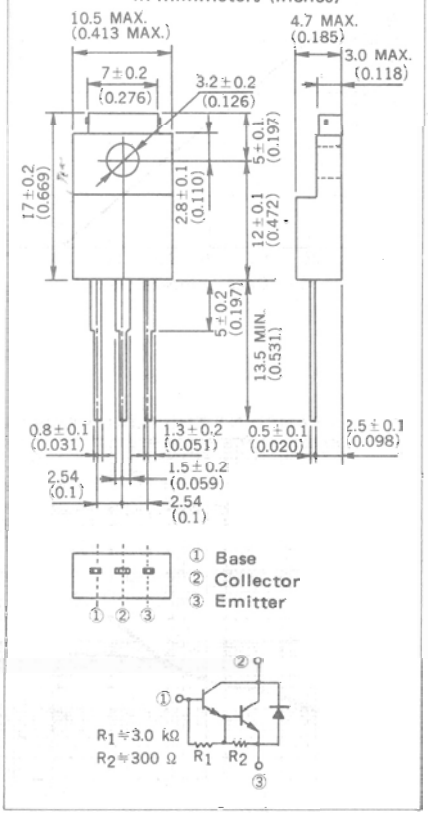
2SD1589

DESCRIPTION The 2SD1589 is NPN silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Collector to Emitter Reverse Diode is built-in.
- Low Collector Saturation Voltage.
- Complementary to 2SB1098.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	±5.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	±10	A
$I_{B(DC)}$	Base Current (DC)	0.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	2000	8000	20000	—	V_{CE} = 2.0 V, I_C = 2.0 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = 2.0 V, I_C = 4.0 A
t_{on}	Turn on Time		1.0		μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 2.0 mA, R_L = 25 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time		3.5		μs	
t_f	Fall Time		1.2		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**			1.5	V	I_C = 2.0 A, I_B = 2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage**			2.0	V	I_C = 2.0 A, I_B = 2.0 mA
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 100 V, I_E = 0

**PW ≤ 350 μs, Duty Cycle ≤ 2 %

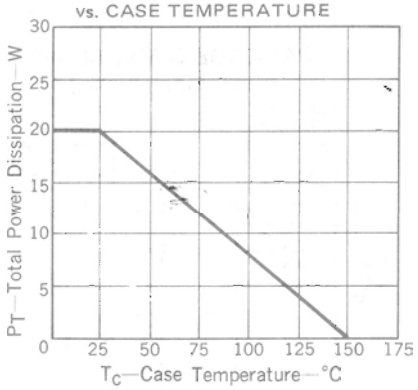
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 20000

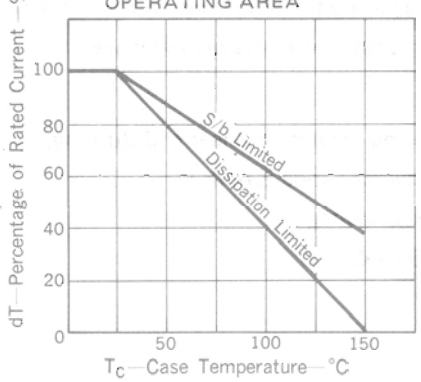
Test Conditions: V_{CE} = 2.0 V, I_C = 2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

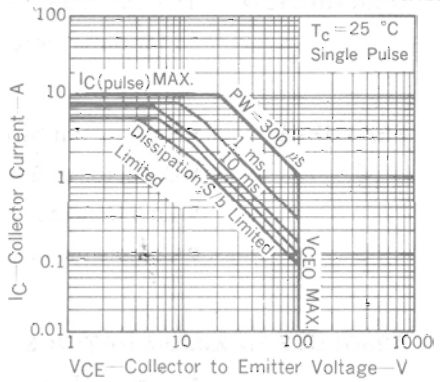
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



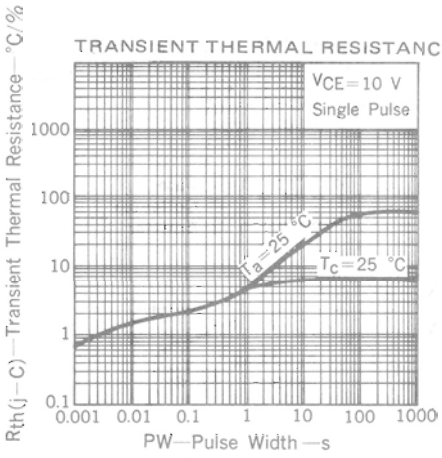
DERATING CURVE OF SAFE OPERATING AREA



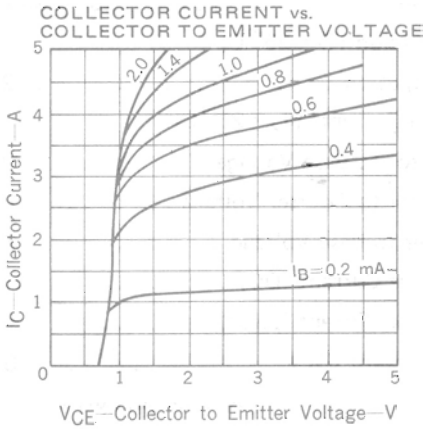
FORWARD BIAS SAFE OPERATING AREA



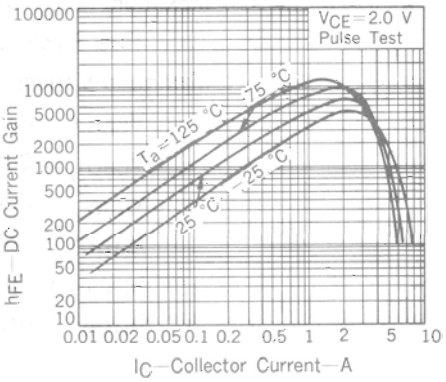
TRANSIENT THERMAL RESISTANCE



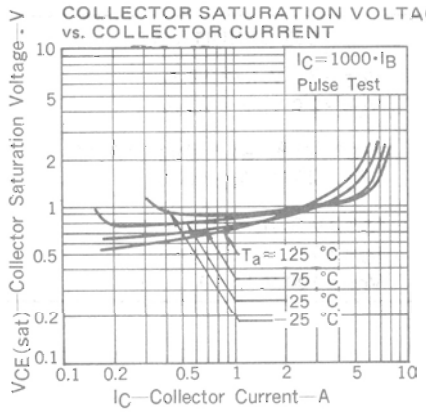
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



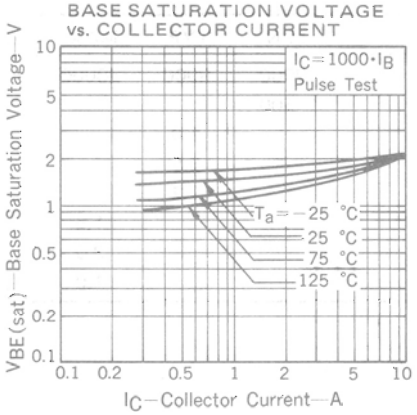
DC CURRENT GAIN vs. COLLECTOR CURRENT



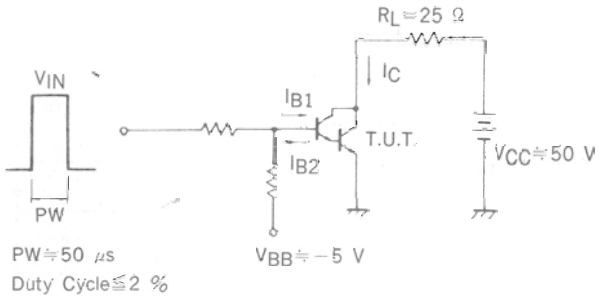
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



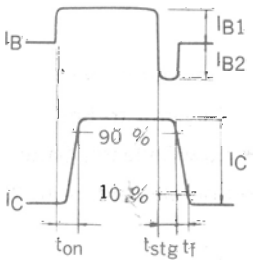
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



PW ≒ 50 μs
Duty Cycle ≦ 2 %



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR

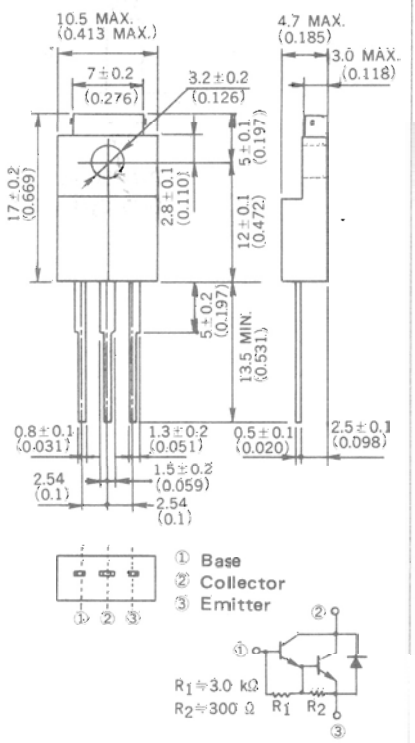
2SD1590

DESCRIPTION The 2SD1590 is NPN silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Collector to Emitter Reverse Diode is built-in.
- Low Collector Saturation Voltage.
- Complementary to 2SB1099.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 25 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	+8.0, −5.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	+12, −8.0	A
$I_{B(DC)}$	Base Current (DC)	0.8	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	2000		15000	—	V_{CE} = 2.0 V, I_C = 3.0 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = 2.0 V, I_C = 5.0 A
t_{on}	Turn-on Time		1.0		μs	I_C = 3.0 A, I_{B1} = −I_{B2} = 3.0 mA, R_L = 16.7 Ω, V_{CC} = 50 V
t_{stg}	Storage Time		3.5		μs	
t_f	Fall Time		1.2		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**		0.9	1.5	V	I_C = 3.0 A, I_B = 3.0 mA
$V_{BE(sat)}$	Base Saturation Voltage**		1.6	2.0	V	I_C = 3.0 A, I_B = 3.0 mA
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 100 V, I_E = 0

**PW ≤ 350 μs, Duty Cycle ≤ 2 %

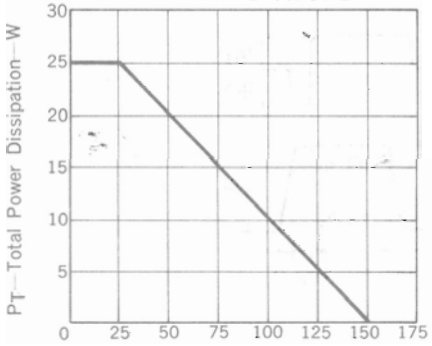
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	3000 to 7000	5000 to 15000

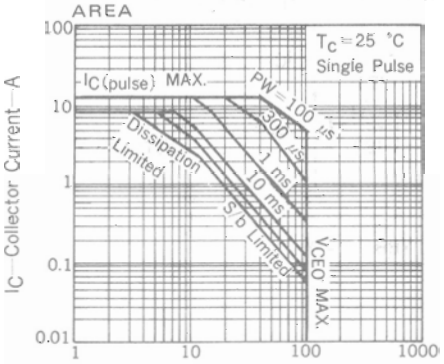
Test Conditions: V_{CE} = 2.0 V, I_C = 3.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

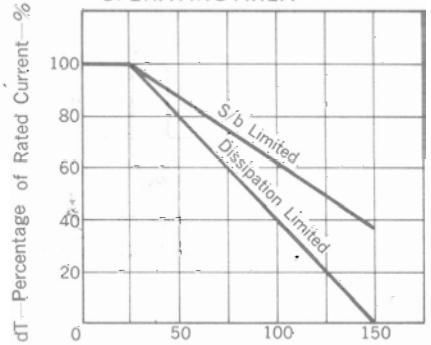
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



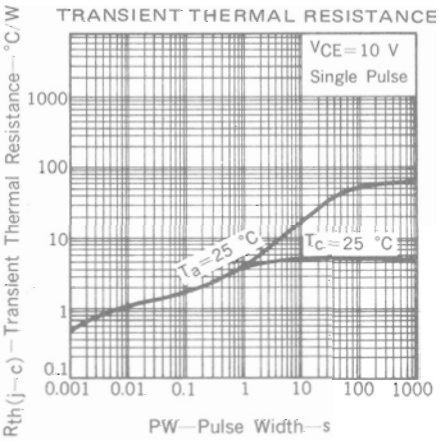
FORWARD BIAS SAFE OPERATING AREA



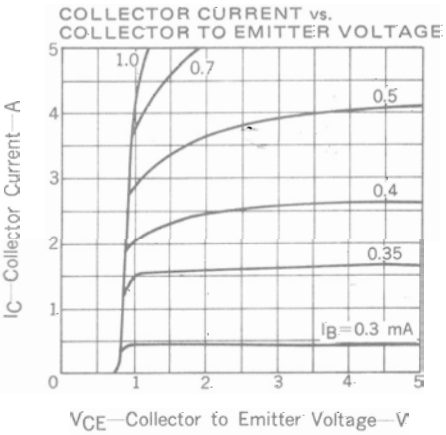
DERATING CURVE OF SAFE OPERATING AREA



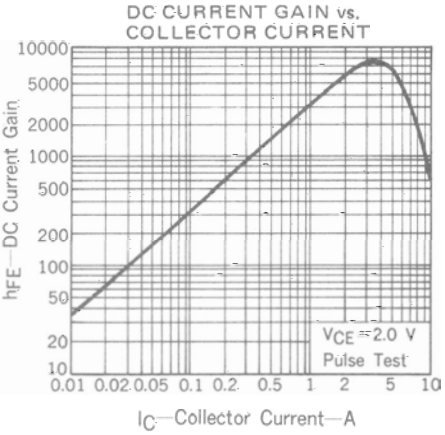
TRANSIENT THERMAL RESISTANCE



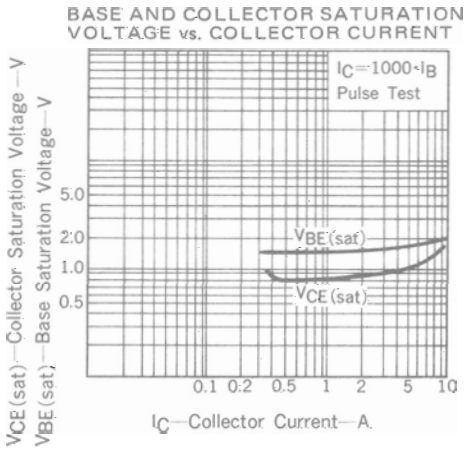
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



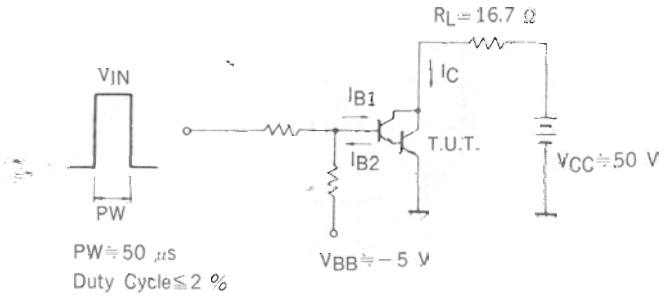
DC CURRENT GAIN vs. COLLECTOR CURRENT

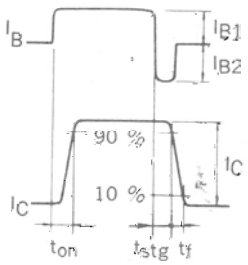


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

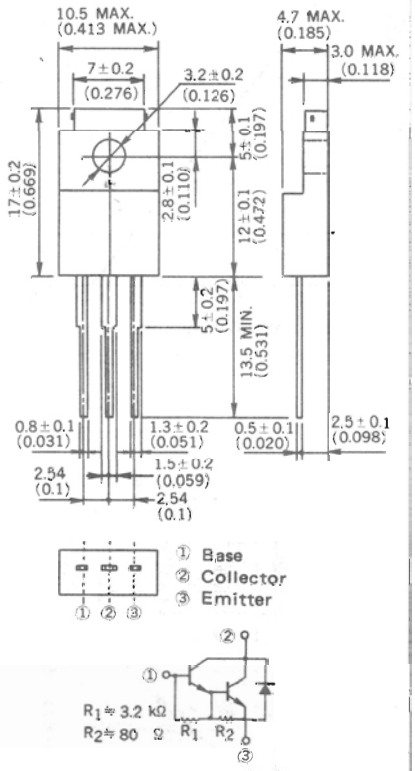
NPN SILICON DARLINGTON POWER TRANSISTOR
2SD1591

DESCRIPTION The 2SD1591 is NPN silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, and solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- High DC Current Gain.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	150	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	8.0	V
$I_{C(DC)}$	Collector Current (DC)	±10	A
$I_{C(pulse)}$	Collector Current (pulse)*	±20	A
$I_{B(DC)}$	Base Current (DC)	1.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain**	1000	9000	30000	—	V_{CE} = 2.0 V, I_C = 10 A
t_{on}	Turn on Time		1.0		μs	I_C = 10 A, I_{B1} = −I_{B2} = 25 mA, R_L = 5.0 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time		5.0		μs	
t_f	Fall Time		2.0		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**		1.1	1.5	V	I_C = 10 A, I_B = 25 mA
$V_{BE(sat)}$	Base Saturation Voltage**		1.8	2.0	V	
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0

**PW ≤ 350 μs, Duty Cycle ≤ 2 %

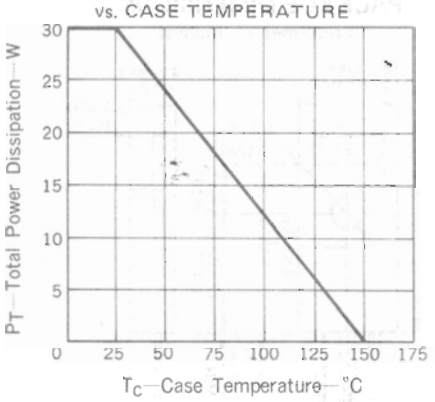
Classification of h_{FE}

Rank	M	L	K	J
Range	1000 to 3000	2000 to 5000	4000 to 10000	8000 to 30000

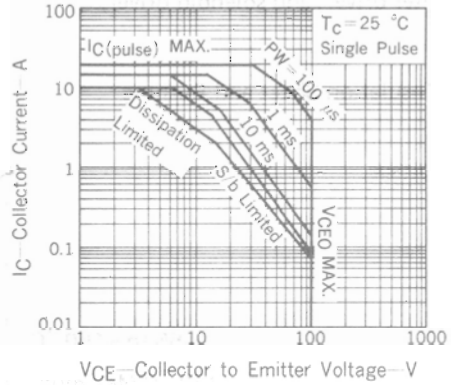
Test Conditions: V_{CE} = 2.0 V, I_C = 10 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

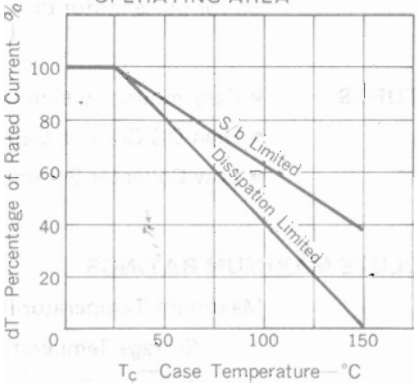
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



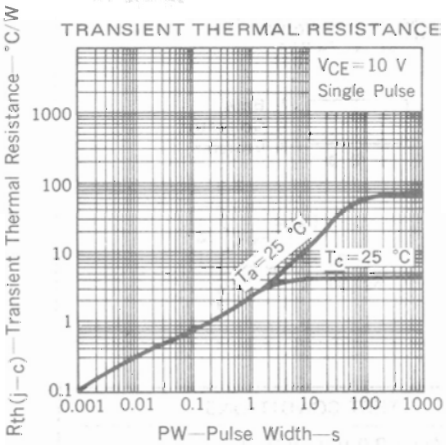
FORWARD BIAS SAFE OPERATING AREA



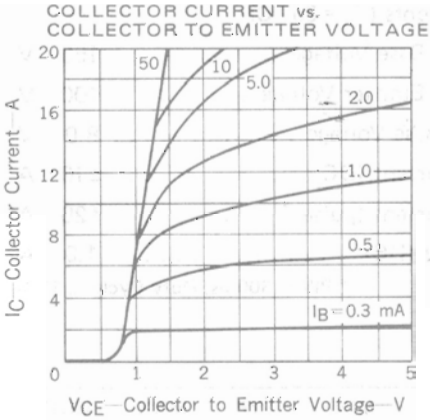
DERATING CURVE OF SAFE OPERATING AREA



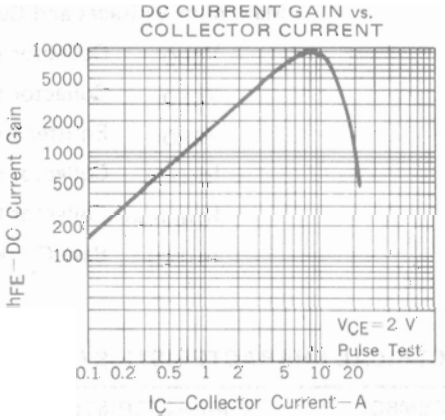
TRANSIENT THERMAL RESISTANCE



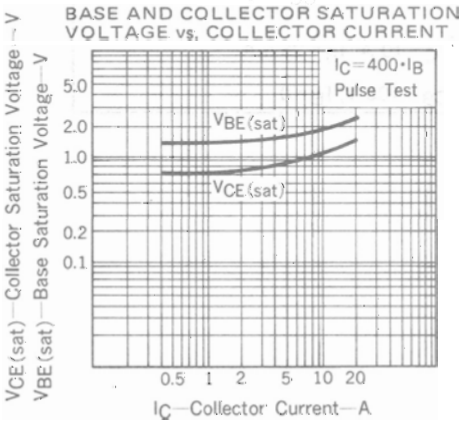
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



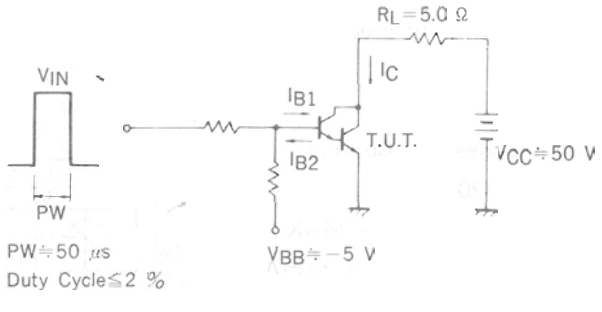
DC CURRENT GAIN vs. COLLECTOR CURRENT

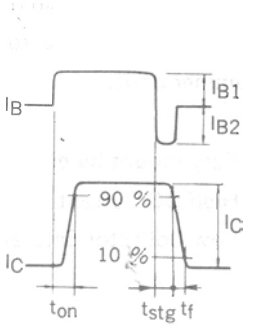


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





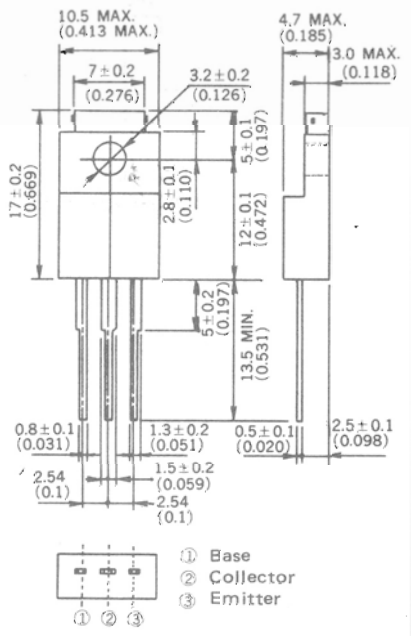
NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SD1593

DESCRIPTION The 2SD1593 is High h_{FE} and Low $V_{CE(sat)}$ transistor.
It is suitable for use to operate from IC without predriver such as hammer driver.

FEATURES
- Easy mount by eliminating Insulation Sheet and Bushing.
- High DC Current Gain : h_{FE} = 800 to 3200
- Low Collector Saturation Voltage : $V_{CE(sat)}$ = 0.5 V MAX. (@ I_C/I_B = 2.0 A/20 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)
- Total Power Dissipation . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	3.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	5.0	A
$I_{B(DC)}$	Base Current (DC)	0.5	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	800		3200	—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = 5.0 V, I_C = 3.0 A
f_T	Gain Bandwidth Product		110		MHz	V_{CE} = 5.0 V, I_C = 0.1 A
C_{ob}	Output Capacitance		50		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
$V_{CE(sat)}$	Collector Saturation Voltage**			0.5	V	I_C = 2.0 A, I_B = 20 mA
$V_{BE(sat)}$	Base Saturation Voltage**			1.2	V	I_C = 2.0 A, I_B = 20 mA
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

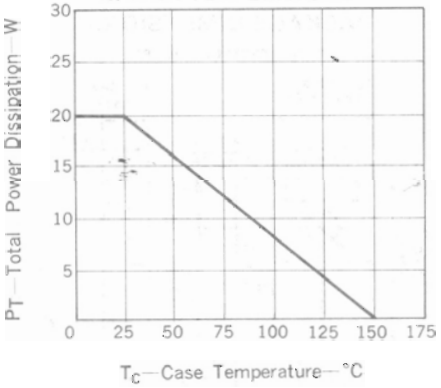
Classification of h_{FE1}

Rank	M	L	K
Range	800 to 1600	1000 to 2000	1600 to 3200

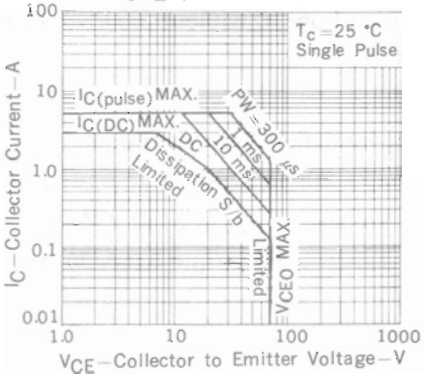
Test Conditions: V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

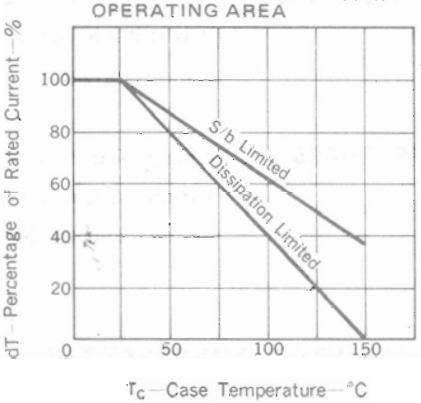
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



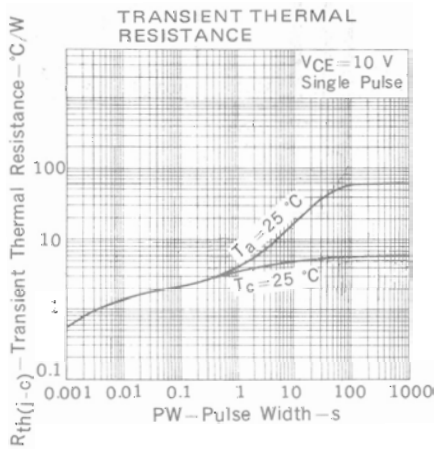
FORWARD BIAS SAFE OPERATING AREA



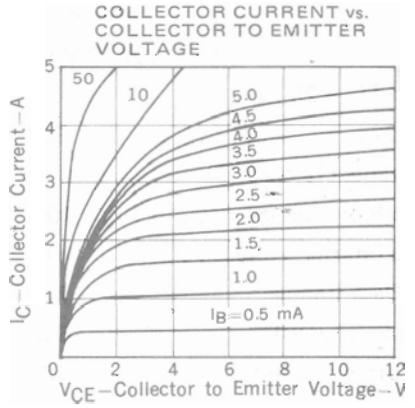
DERATING CURVE OF SAFE OPERATING AREA



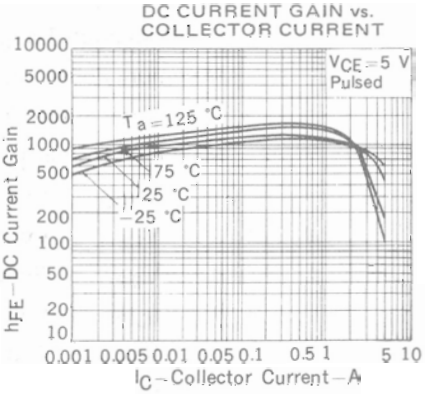
TRANSIENT THERMAL RESISTANCE



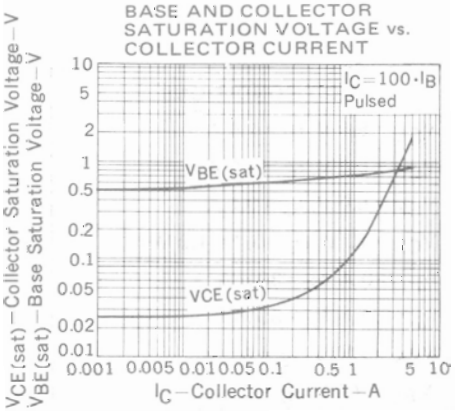
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



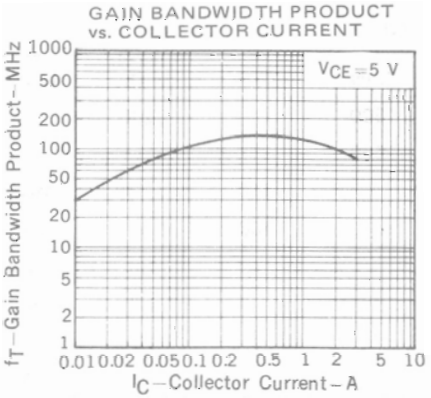
DC CURRENT GAIN vs. COLLECTOR CURRENT



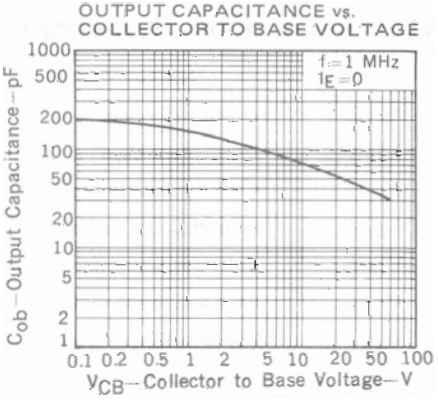
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

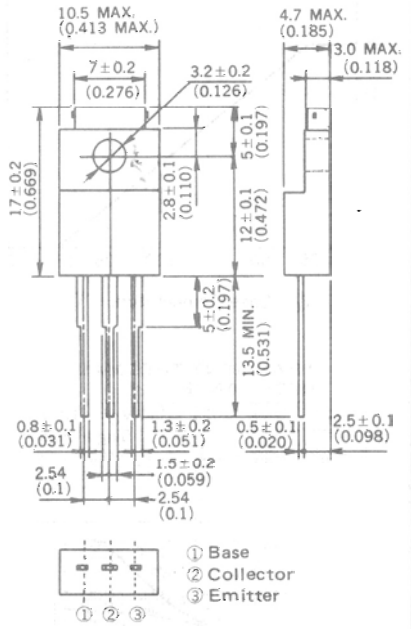
NPN SILICON POWER TRANSISTOR
2SD1594

DESCRIPTION The 2SD1594 is High h_{FE} and Low $V_{CE(sat)}$ transistor.
It is suitable for use to operate from IC without predriver such as hammer driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- High DC Current Gain : h_{FE} = 800 to 3200
- Low Collector Saturation Voltage : $V_{CE(sat)}$ = 1.0 V MAX.
  (@ I_C/I_B = 3.0 A/30 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 30 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	100	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	6.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	10	A
$I_{B(DC)}$	Base Current (DC)	1.0	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	800		3200	—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE2}**	DC Current Gain	500			—	V_{CE} = 5.0 V, I_C = 3.0 A
f_T	Gain Bandwidth Product		110		MHz	V_{CE} = 5.0 V, I_C = 0.1 A
C_{ob}	Output Capacitance		100		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
$V_{CE(sat)}$**	Collector Saturation Voltage			1.0	V	I_C = 3.0 A, I_B = 30 mA
$V_{BE(sat)}$**	Base Saturation Voltage			1.2	V	I_C = 3.0 A, I_B = 30 mA
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

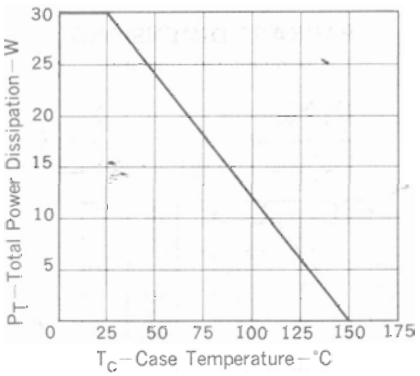
Classification of h_{FE1}

Rank	M	L	K
Range	800 to 1600	1000 to 2000	1600 to 3200

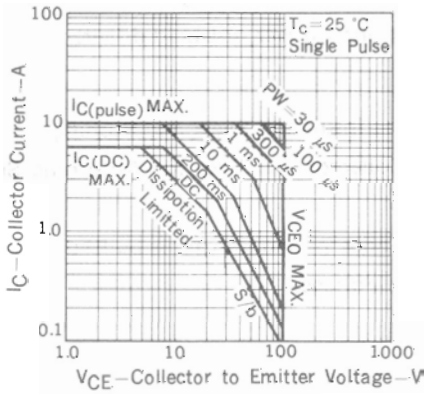
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

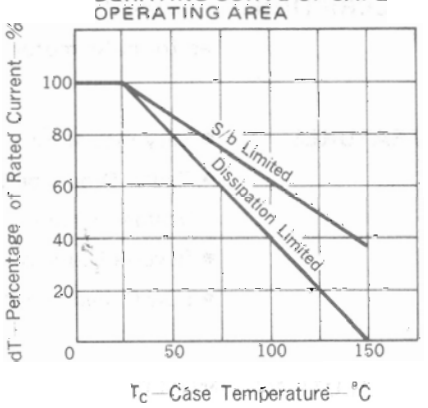
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



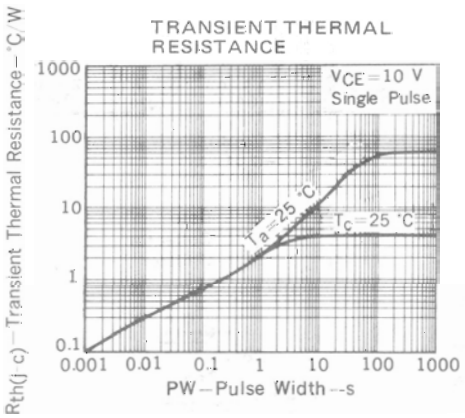
FORWARD BIAS SAFE OPERATING AREA



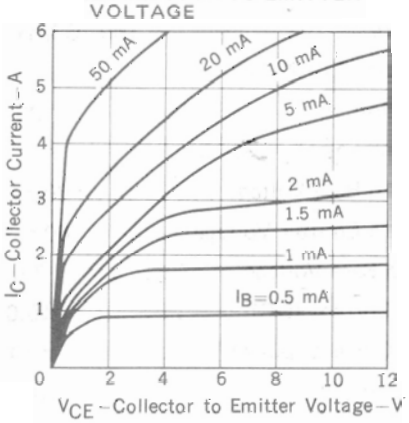
DERATING CURVE OF SAFE OPERATING AREA



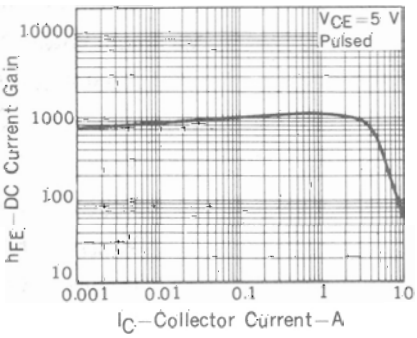
TRANSIENT THERMAL RESISTANCE



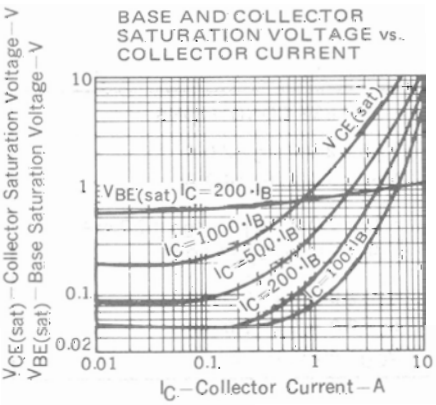
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



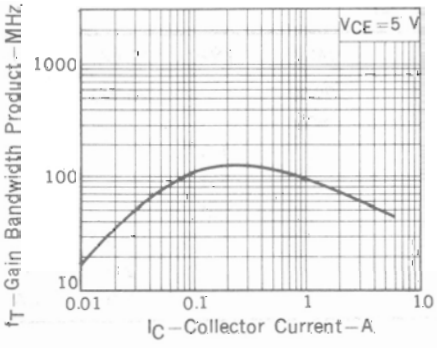
DC CURRENT GAIN vs. COLLECTOR CURRENT



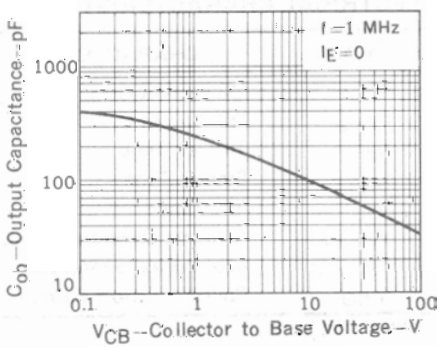
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR

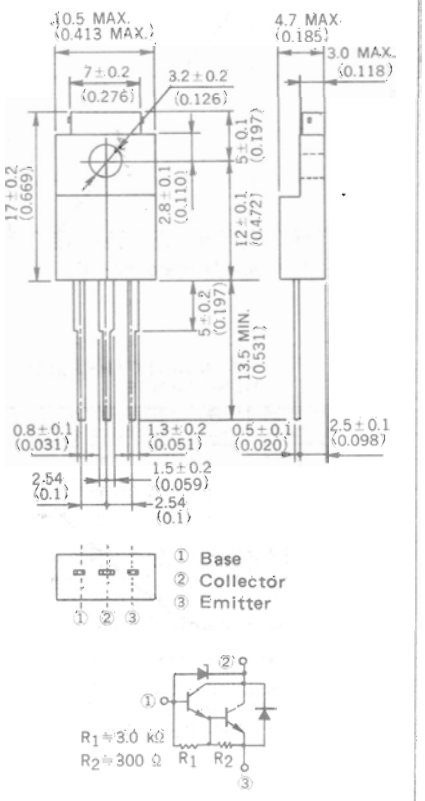
2SD1595

DESCRIPTION The 2SD1595 is NPN silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- Easy mount by eliminating Insulation Sheet and Bushing.
- Zener Diode between Collector and Base for Absorbing Surge Voltage is built-in.
- Reverse Diode between Collector and Emitter is built-in.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60 ± 10	V
V_{CEO}	Collector to Emitter Voltage	60 ± 10	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current (DC)	±5.0	A
$I_{C(pulse)}$	Collector Current (pulse)*	±10	A
$I_{B(DC)}$	Base Current (DC)	0.5	A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain**	2000		20000	—	V_{CE} = 2.0 V, I_C = 2.0 A
h_{FE2}	DC Current Gain**	500			—	V_{CE} = 2.0 V, I_C = 4.0 A
t_{on}	Turn-on Time		1.0		μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 2.0 mA, R_L = 25 Ω, V_{CC} ≒ 50 V
t_{stg}	Storage Time		7.0		μs	
t_f	Fall Time		2.0		μs	
$V_{CE(sat)}$	Collector Saturation Voltage**			1.5	V	I_C = 2.0 A, I_B = 2.0 mA
$V_{BE(sat)}$	Base Saturation Voltage**			2.0	V	I_C = 2.0 A, I_B = 2.0 mA
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 40 V, I_E = 0

**PW ≦ 350 μs, Duty Cycle ≦ 2 %

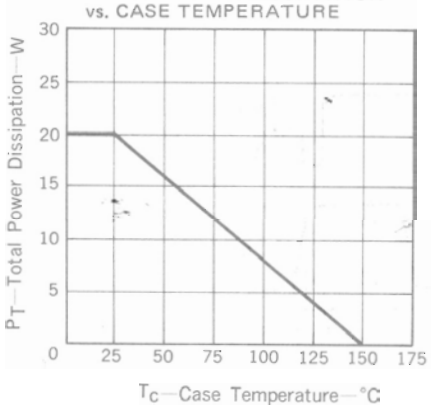
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 20000

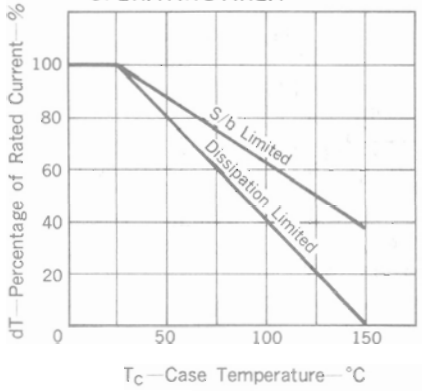
Test Conditions: V_{CE} = 2.0 A, I_C = 2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

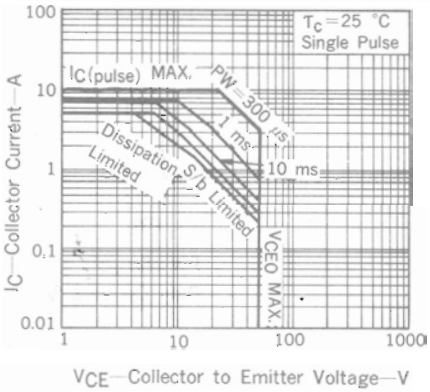
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



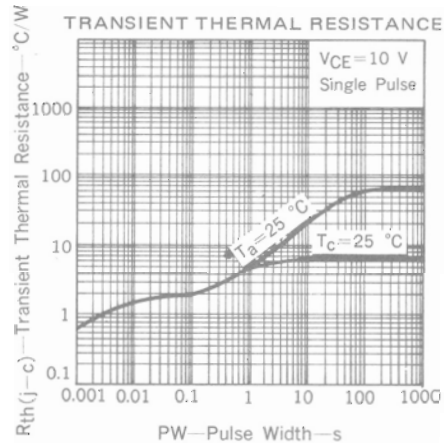
DERATING CURVE OF SAFE OPERATING AREA



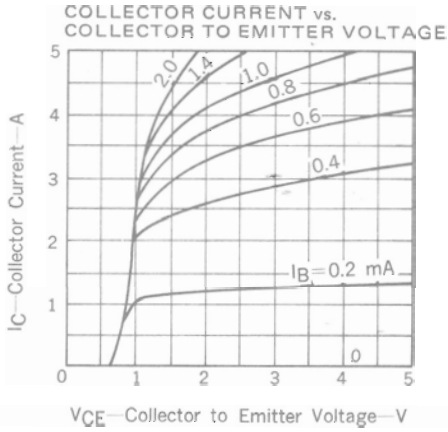
FORWARD BIAS SAFE OPERATING AREA



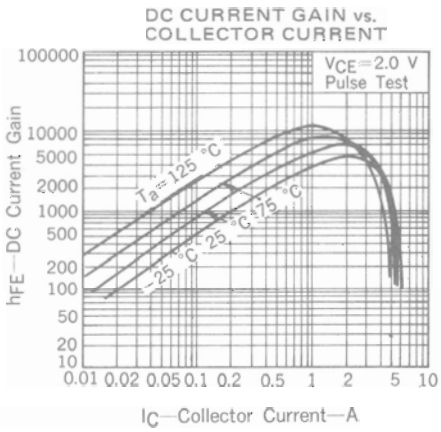
TRANSIENT THERMAL RESISTANCE



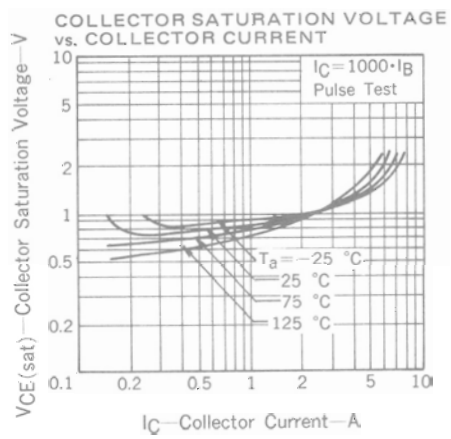
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



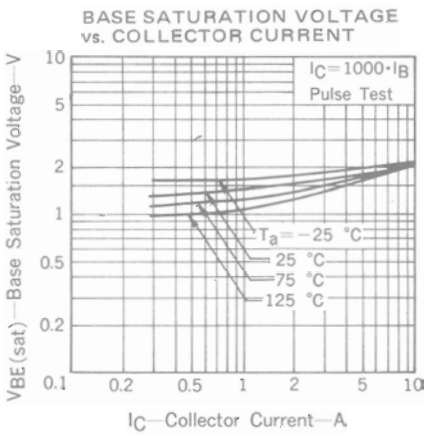
DC CURRENT GAIN vs. COLLECTOR CURRENT



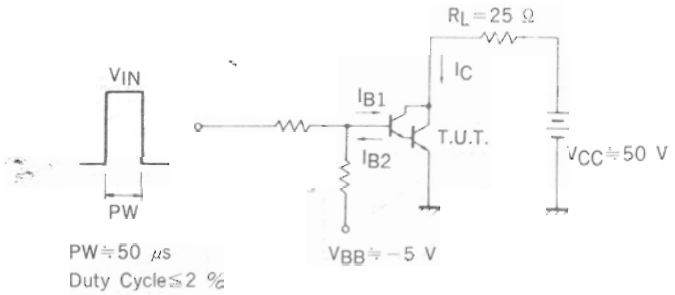
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

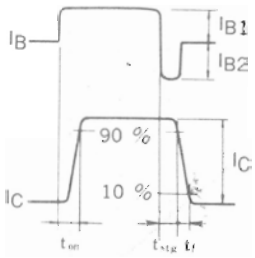


BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

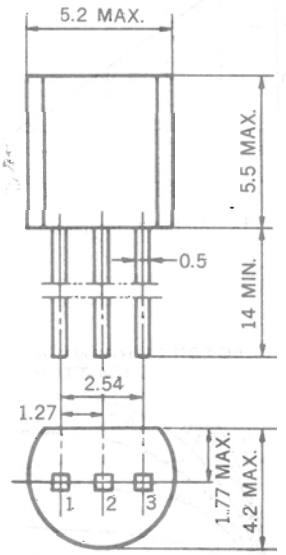
NPN SILICON TRANSISTORS
2SD1616, 2SD1616A

DESCRIPTION The 2SD1616/2SD1616A are designed for use in driver and output stages of AF amplifier, general purpose application.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.15 V TYP. (@ I_C = 1.0 A, I_B = 50 mA)
- High Break Down Voltage.
  V_{CEO} = 50 V/60 V (2SD1616/2SD1616A)
- High Total Power Dissipation. : P_T = 0.75 W (T_a = 25 °C)
- Complementary to the NEC 2SB1116/2SB1116A PNP Transistor.

PACKAGE DIMENSIONS
in millimeters



1. Emitter EIAJ : SC-43B
2. Collector JEDEC : TO-92
3. Base IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C) 2SD1616/2SD1616A
- V_{CBO} Collector to Base Voltage . . . . . 60 V/120 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V/60 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current (DC) . . . . . 1.0 A
- I_C Collector Current (pulse)* . . . . . 2.0 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

2SD1616/2SD1616A

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	135		600	–	V_{CE} = 2.0 V, I_C = 100 mA
h_{FE2}**	DC Current Gain	81			–	V_{CE} = 2.0 V, I_C = 1.0 A
f_T	Gain Bandwidth Product	100	160		MHz	V_{CE} = 2.0 V, I_C = 100 mA
C_{ob}	Output Capacitance		19		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 60 V/120 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 6.0 V, I_C = 0
V_{BE}**	Base to Emitter Voltage	600		700	mV	V_{CE} = 2.0 V, I_C = 50 mA
$V_{CE(sat)}$**	Collector Saturation Voltage		0.15	0.3	V	I_C = 1.0 A, I_B = 50 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.9	1.2	V	I_C = 1.0 A, I_B = 50 mA
t_{on}	Turn-On Time		0.07		μs	V_{CC} = 10 V, I_C = 100 mA
t_{stg}	Storage Time		0.95		μs	I_{B1} = −I_{B2} = 10 mA
t_f	Fall Time		0.07		μs	$V_{BE(off)}$ = −2 to 3 V

**Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

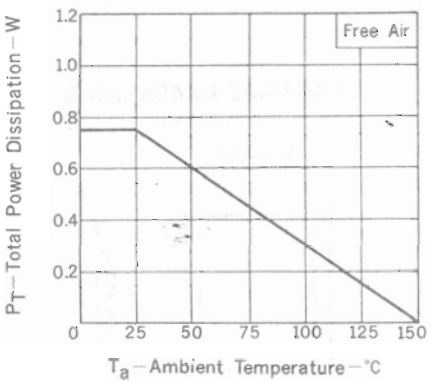
Classification of h_{FE1}

Rank	L	K	U
Range	135 to 270	200 to 400	300 to 600

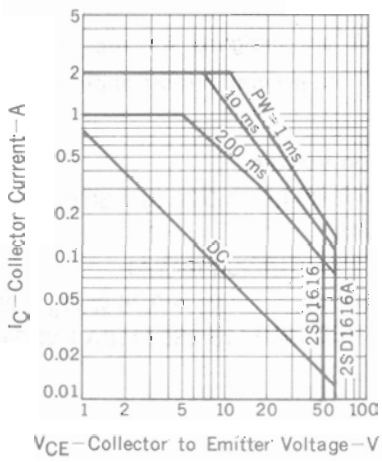
Test Conditions: V_{CE} = 2.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

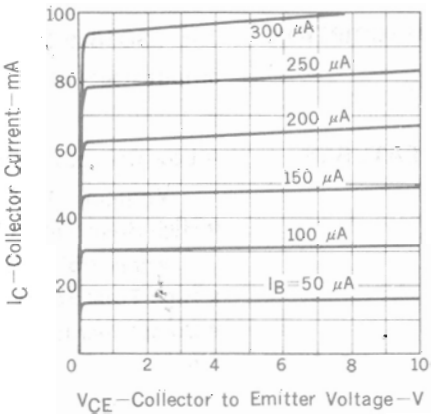
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



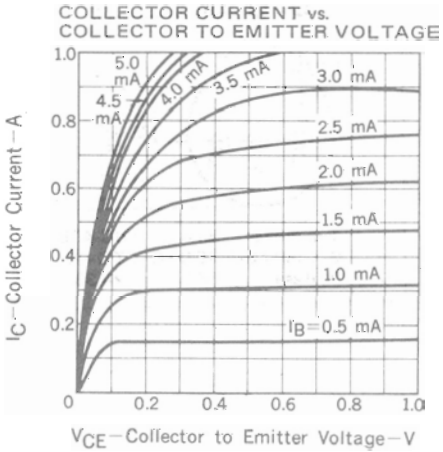
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



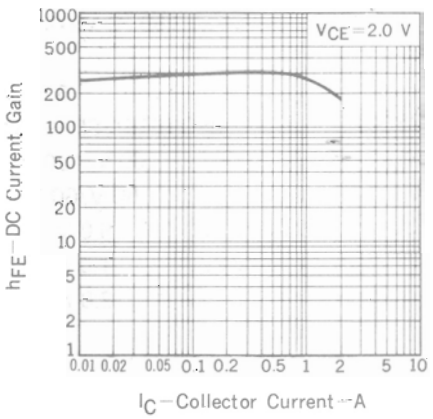
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



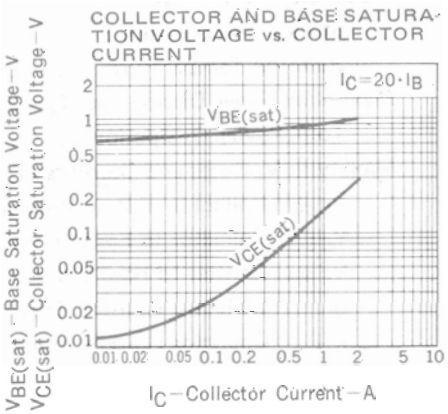
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



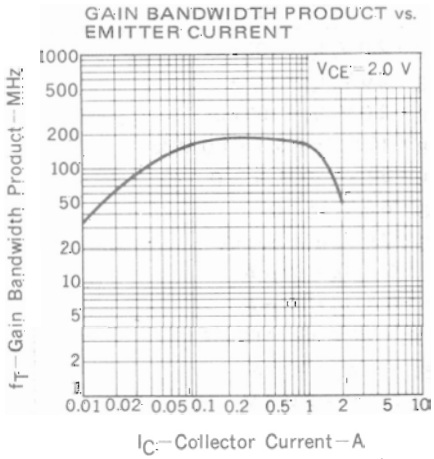
DC CURRENT GAIN vs. COLLECTOR CURRENT



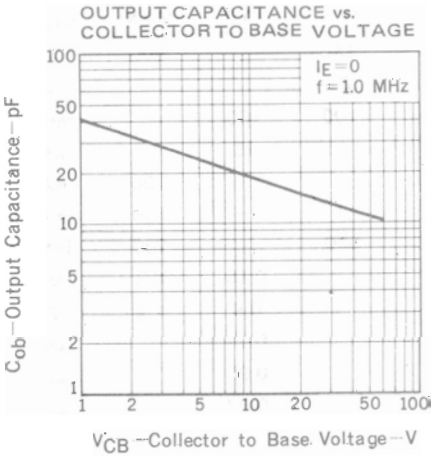
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



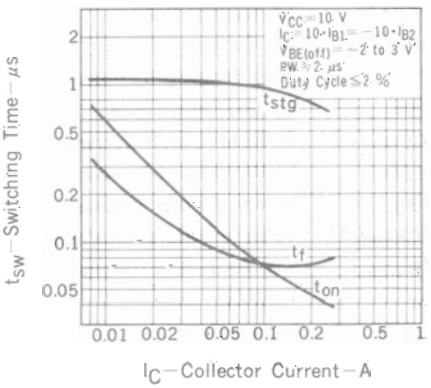
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

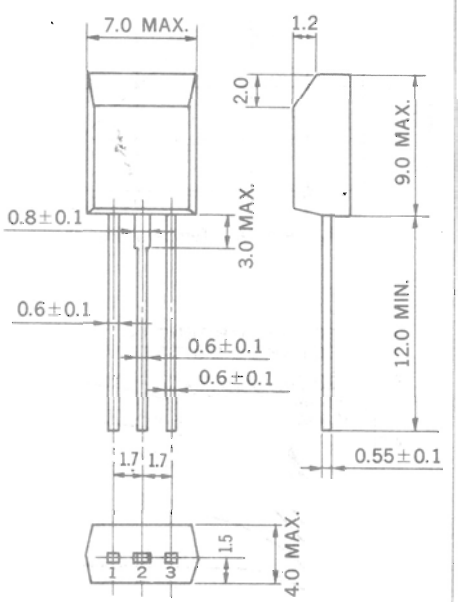
NPN SILICON TRANSISTOR
2SD1617

DESCRIPTION The 2SD1617 is a Low $V_{CE(sat)}$ transistor which has a large Current Capability and Wide ASO.
It is suitable for driver of solenoid or motor, or electronic flash.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.20 V TYP. (@ I_C/I_B = 2.0 A/0.2 A)
- Large Current.
  $I_{C(DC)}$ = 3.0 A, $I_{C(pulse)}$ = 5.0 A
- High DC Current Gain. :
  h_{FE} = 300 TYP. (@ V_{CE} = 2.0 V, I_C = 1.0 A)
- High Total Power Dissipation. : P_T = 1.0 W
- Complementary to the NEC 2SB1117 PNP Transistor.

PACKAGE DIMENSIONS
in millimeters



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 40 V
- V_{CEO} Collector to Emitter Voltage . . . . . 25 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current (DC) . . . . . 3.0 A
- I_C Collector Current (pulse)* . . . . . 5.0 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	135	300	600	—	V_{CE} = 2.0 V, I_C = 1.0 A
h_{FE2}**	DC Current Gain	81			—	V_{CE} = 2.0 V, I_C = 2.0 A
f_T	Gain Bandwidth Product	100	200		MHz	V_{CE} = 5.0 V, I_E = −1.0 A
C_{ob}	Output Capacitance		40		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 6.0 V, I_C = 0
V_{BE}**	Base to Emitter Voltage	600	630	700	mV	V_{CE} = 2.0 V, I_B = 0.1 A
$V_{CE(sat)1}$**	Collector Saturation Voltage		0.2	0.3	V	I_C = 2.0 A, I_B = 0.2 A
$V_{CE(sat)2}$**	Collector Saturation Voltage		0.3	0.5	V	I_C = 3.0 A, I_B = 0.3 A
$V_{BE(sat)}$**	Base Saturation Voltage		1.0	1.2	V	I_C = 2.0 A, I_B = 0.2 A
t_{on}	Turn-On Time		70		ns	(V_{CC} = 10 V, I_C = 500 mA
t_{stg}	Storage Time		420		ns	I_{B1} = −I_{B2} = 50 mA
t_f	Fall Time		60		ns	$V_{BE(off)}$ = −2 to 3 V)

**Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

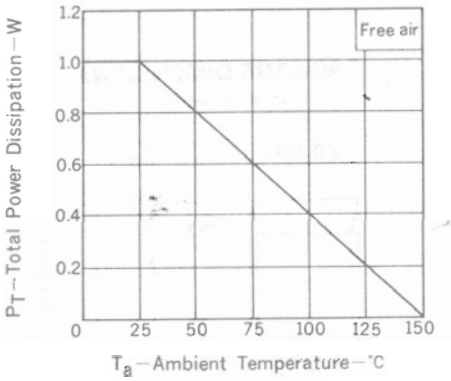
Classification of h_{FE1}

Rank	L	K	U
Range	135 to 270	200 to 400	300 to 600

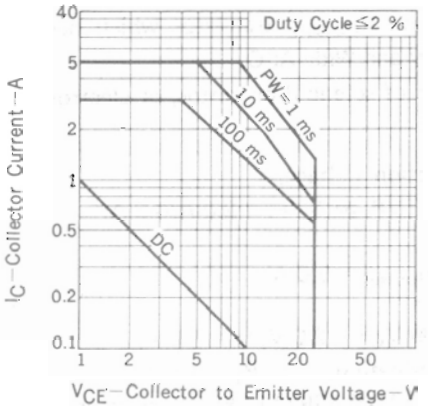
Test Conditions: V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

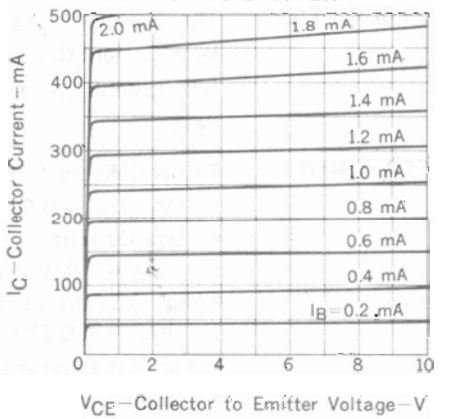
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



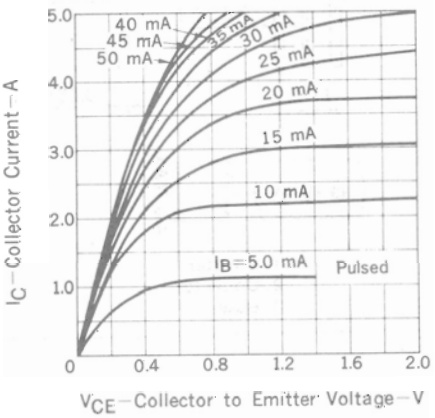
SAFE OPERATING AREAS (TRANSIENT THERMAL RESITANCE METHOD)



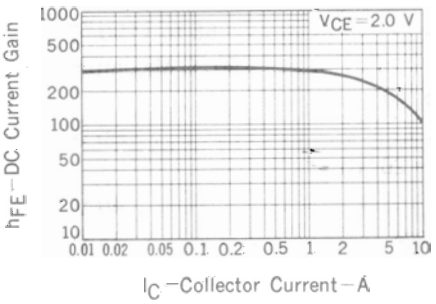
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



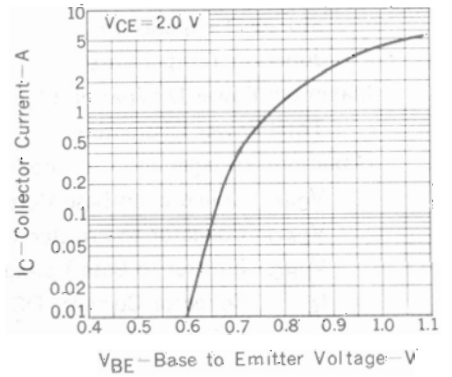
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



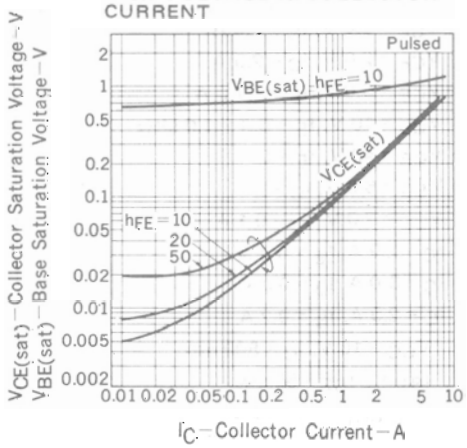
DC CURRENT GAIN vs. COLLECTOR CURRENT



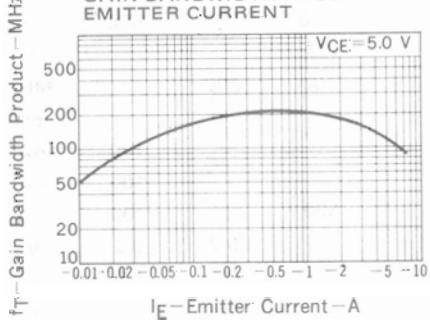
BASE TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



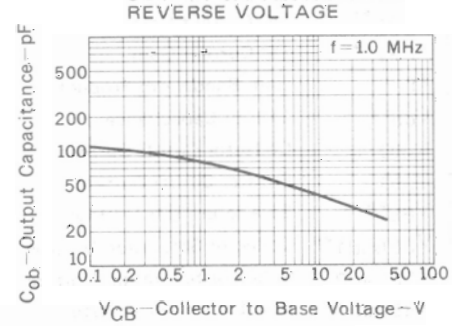
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



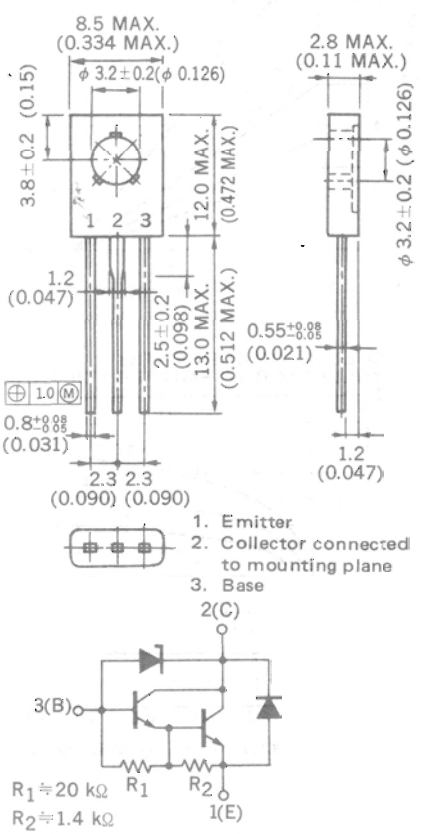
NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON POWER TRANSISTOR
2SD1630

DESCRIPTION The 2SD1630 is a darlington transistor built-in a zener diode at B-C and a dumper diode at E-C.
It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES
- High DC Current Gain.
- Built-in a Zener Diode at B-C and a Dumper Diode at E-C.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations
- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 10 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 60 ± 10 V
- V_{CEO} Collector to Emitter Voltage . . . . 60 ± 10 V
- V_{EBO} Emitter to Base Voltage . . . . . 7.0 V
- $I_{C(DC)}$ Collector Current . . . . . ± 1.0 A
- $I_{C(pulse)}$* Collector Current . . . . . ± 2.0 A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	1000			—	V_{CE} = 2.0 V, I_C = 0.2 A
h_{FE2} **	DC Current Gain	2000		30000	—	V_{CE} = 2.0 V, I_C = 0.5 A
V_{CBO}	Collector to Base Voltage	50	60	70	V	I_C = 1.0 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 10 mA, R_{BE} = ∞
t_{on}	Turn On Time		0.5		μs	I_C = 0.5 A, R_L = 100 Ω I_{B1} = −I_{B2} = 0.5 mA, V_{CC} = 50 V
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			0.5	μA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage			1.5	V	I_C = 0.5 A, I_B = 0.5 mA
$V_{BE(sat)}$ **	Base Saturation Voltage			2.0	V	I_C = 0.5 A, I_B = 0.5 mA

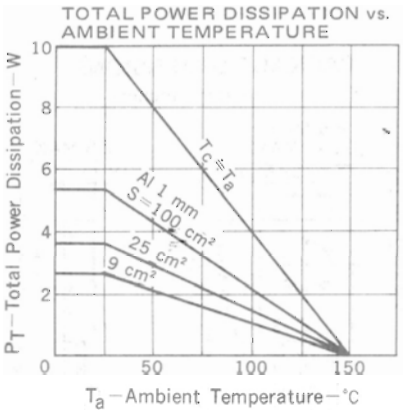
** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

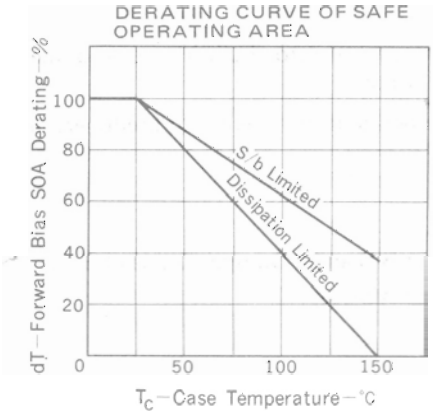
Classification of h_{FE2}

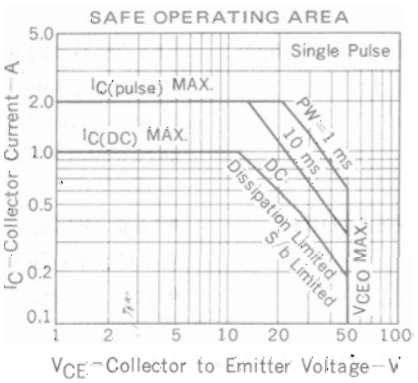
Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 30000

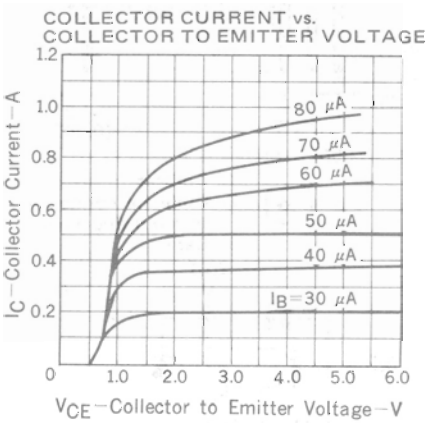
Test Conditions: V_{CE} = 2.0 V, I_C = 0.5 A

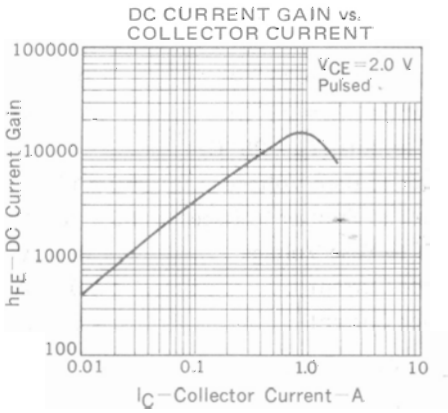
TYPICAL CHARACTERISTICS (T_a = 25 °C)

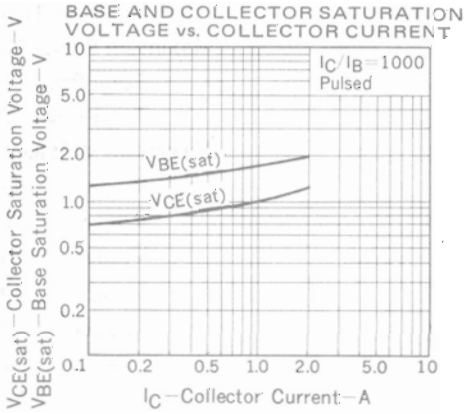




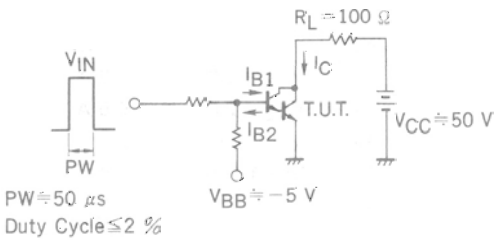


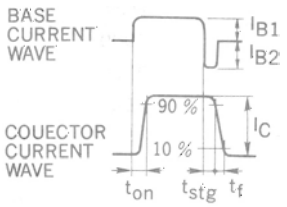






SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

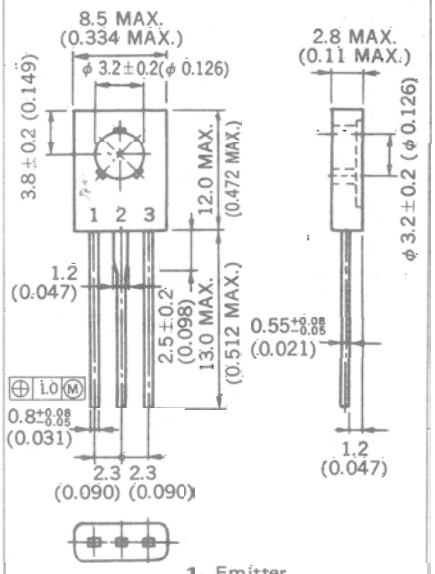
NPN SILICON POWER TRANSISTOR
2SD1691

DESCRIPTION The 2SD1691 is a Low $V_{CE(sat)}$ transistor which has a large current capability and wide SOA.
It is suitable for DC-DC converter, or driver of solenoid or motor.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.1 V TYP. (@ I_C/I_B = 2.0 A/0.2 A)
- Large Current.
  $I_{C(DC)}$ = 5.0 A, $I_{C(pulse)}$ = 8.0 A
- High Total Power Dissipation : P_T = 1.3 W
- Complementary to 2SB1151.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 20 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 60 V
- V_{EBO} Emitter to Base Voltage . . . . . 7.0 V
- $I_{C(DC)}$ Collector Current . . . . . 5.0 A
- $I_{C(pulse)}$ Collector Current* . . . . . 8.0 A
- $I_{B(DC)}$ Base Current . . . . . 1.0 A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$V_{CE(sat)}$**	Collector Saturation Voltage		0.1	0.3	V	I_C = 2.0 A, I_B = 0.2 A
$V_{BE(sat)}$**	Base Saturation Voltage		0.9	1.2	V	I_C = 2.0 A, I_B = 0.2 A
h_{FE1}**	DC Current Gain	60			—	V_{CE} = 1.0 V, I_C = 0.1 A
h_{FE2}**	DC Current Gain	100		400	—	V_{CE} = 1.0 V, I_C = 2.0 A
h_{FE3}**	DC Current Gain	50			—	V_{CE} = 1.0 V, I_C = 5.0 A
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0
t_{on}	Turn On Time		0.2	1.0	μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.2 A, R_L = 5.0 Ω, V_{CC} ≒ 10 V
t_{stg}	Storage Time		1.1	2.5	μs	
t_f	Fall Time		0.2	1.0	μs	

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

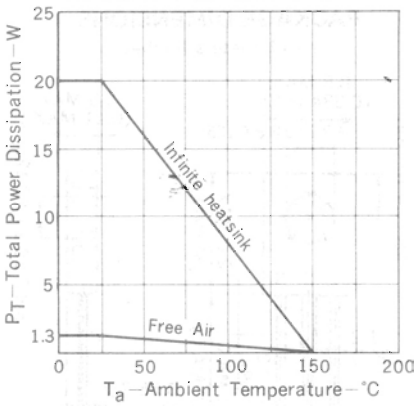
Classification of h_{FE2}

Rank	M	L	K
Range	100 to 200	160 to 320	200 to 400

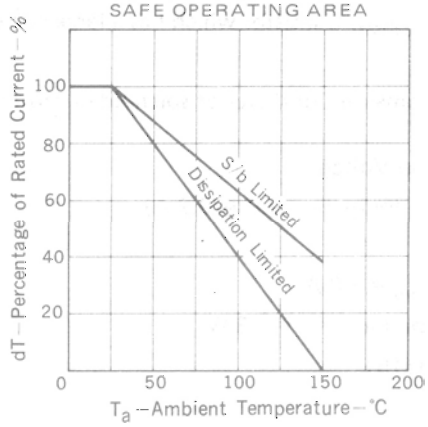
Test Conditions: V_{CE} = 1.0 V, I_C = 2.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

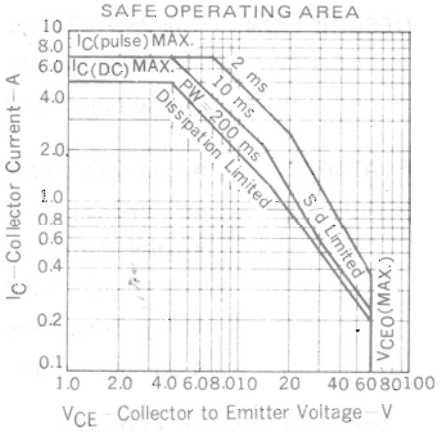
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



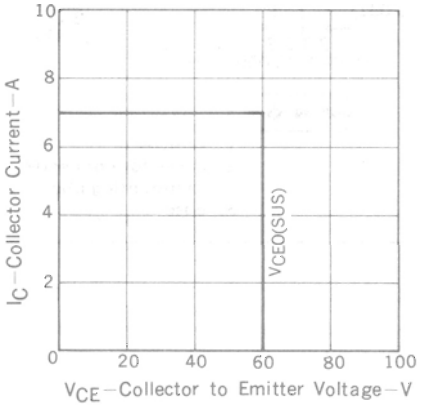
DERATING CURVE OF SAFE OPERATING AREA



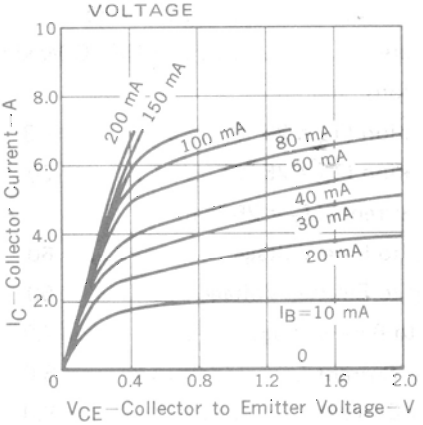
SAFE OPERATING AREA



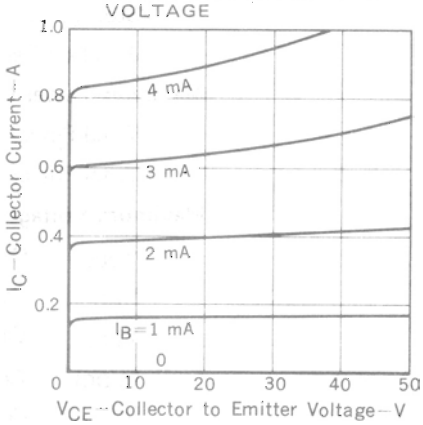
REVERSE BIAS SAFE OPERATING AREA



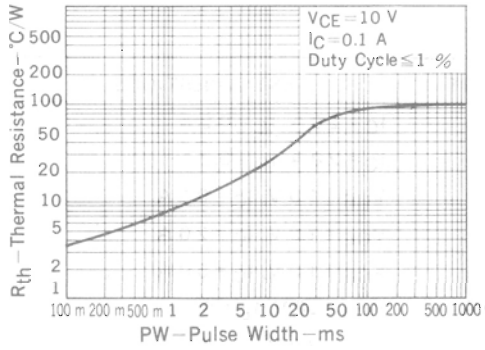
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



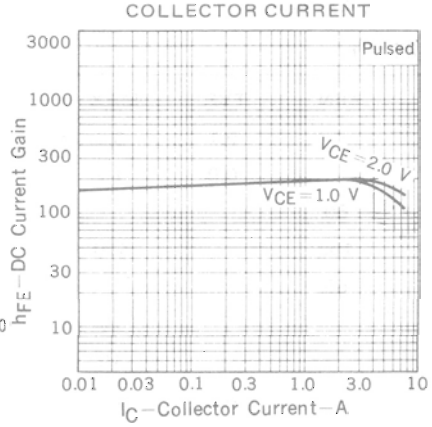
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



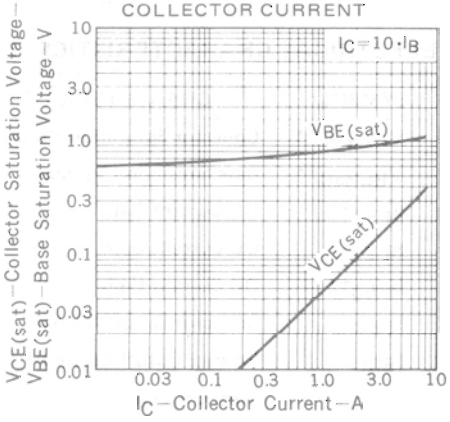
TRANSIENT THERMAL RESISTANCE



DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON TRANSISTOR
2SD1692

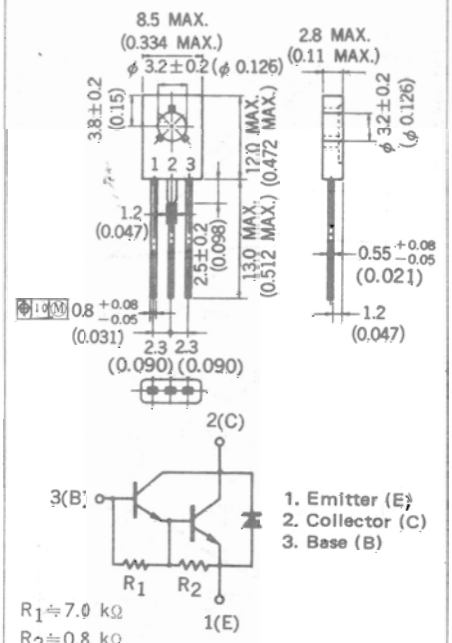
DESCRIPTION The 2SD1692 is a darlington transistor built-in dumper diode at E-C.

It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES

- High DC Current Gain.
- Low Collector Saturation Voltage.
- Built-in a dumper diode at E-C.
- High Power Dissipation: P_T = 1.3 W (at T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 150 V
- V_{CEO} Collector to Emitter Voltage . . . . . 100 V
- V_{EBO} Emitter to Base Voltage . . . . . 8.0 V
- $I_{C(DC)}$ Collector Current . . . . . ±3.0 A
- $I_{C(pulse)}$* Collector Current . . . . . ±5.0 A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	2000		20000	—	V_{CE} = 2.0 V, I_C = 1.5 A
h_{FE2}**	DC Current Gain	1000			—	V_{CE} = 2.0 V, I_C = 3.0 A
t_{on}	Turn On Time		0.5		μs	I_C = 1.5 A, R_L = 27 Ω
t_{stg}	Storage Time		2.0		μs	I_{B1} = −I_{B2} = 1.5 mA, V_{CC} ≒ 40 V
t_f	Fall Time		1.0		μs	See Test Circuit.
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 100 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage		0.9	1.2	V	I_C = 1.5 A, I_B = 1.5 mA
$V_{BE(sat)}$**	Base Saturation Voltage		1.5	2.0	V	I_C = 1.5 A, I_B = 1.5 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

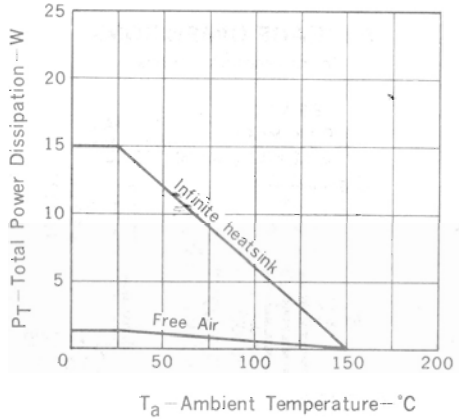
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 20000

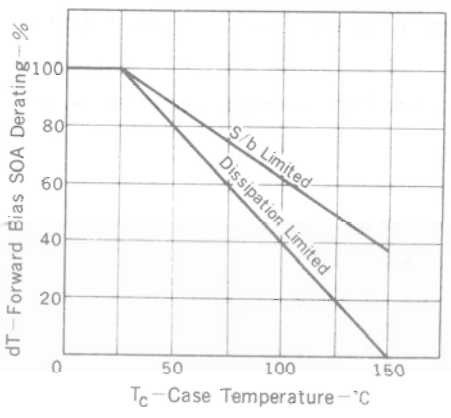
Test Conditions: V_{CE} = 2.0 V, I_C = 1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

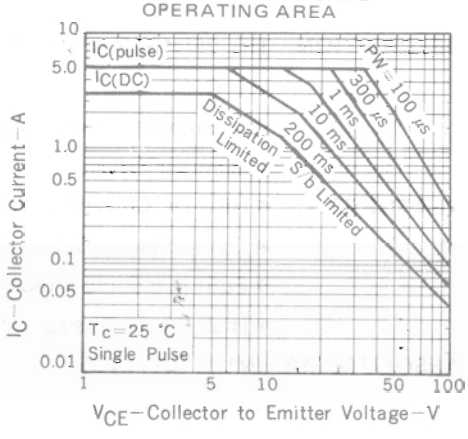
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



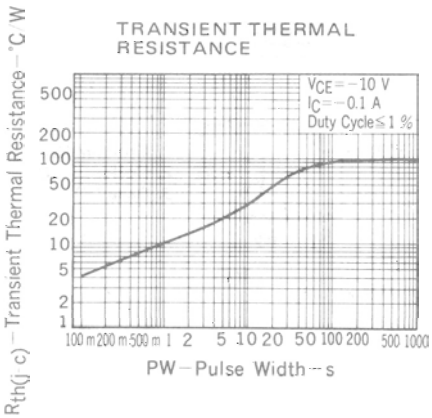
DERATING CURVE OF SAFE OPERATING AREA



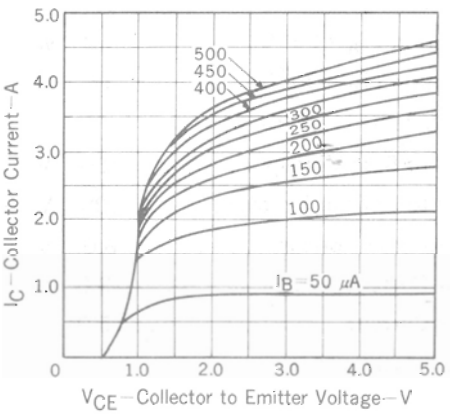
FORWARD BIAS SAFE OPERATING AREA



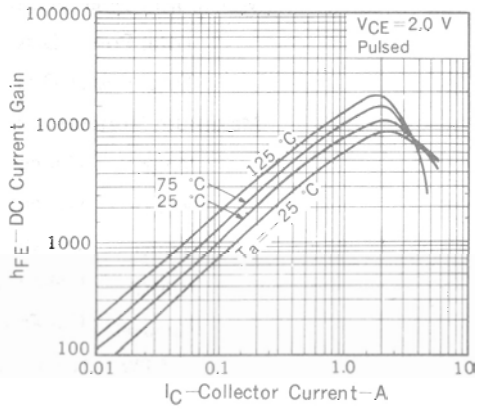
TRANSIENT THERMAL RESISTANCE



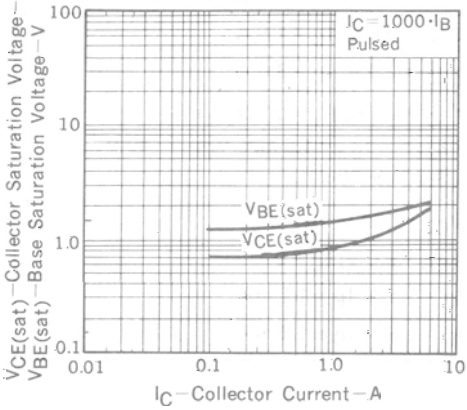
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



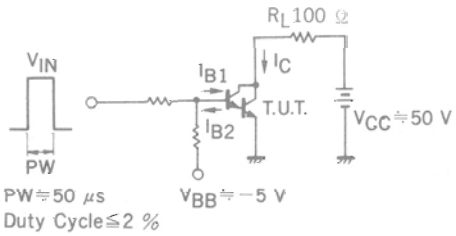
DC CURRENT GAIN vs. COLLECTOR CURRENT

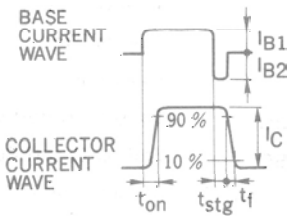


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON TRANSISTOR

2SD1693

DESCRIPTION The 2SD1693 is a darlington transistor built-in a zener diode at B-C and a dumper diode at E-C.

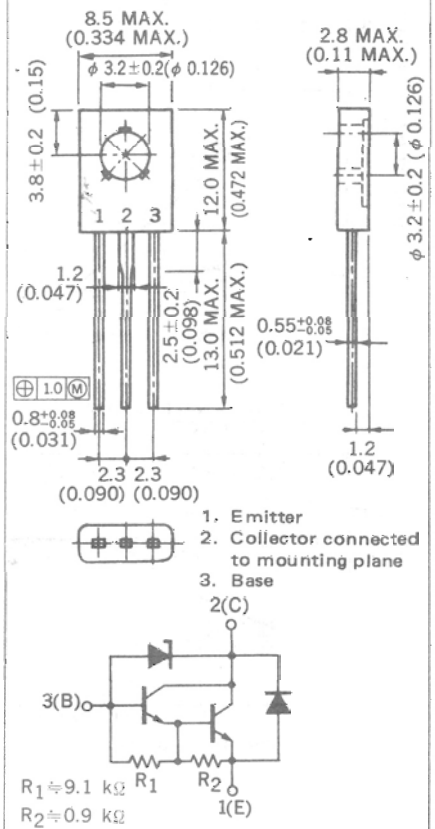
It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES

- High DC Current Gain.
- Built-in a Zener Diode at B-C and a Dumper Diode at E-C.
- Low Collector Saturation Voltage.
- High Power Dissipation: P_T = 1.3 W (at T_a = 25 °C)

PACKAGE DIMENSIONS

in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.3 W
- Total Power Dissipation (T_c = 25 °C) . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60±10 V
- V_{CEO} Collector to Emitter Voltage . . . . . 60±10 V
- V_{EBO} Emitter to Base Voltage . . . . . 8.0 V
- $I_{C(DC)}$ Collector Current . . . . . ±3.0 A
- $I_{C(pulse)}$* Collector Current . . . . . ±5.0 A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	2000		20000	—	V_{CE} = 2.0 V, I_C = 1.5 A
h_{FE2}**	DC Current Gain	1000			—	V_{CE} = 2.0 V, I_C = 3.0 A
V_{CBO}	Collector to Base Voltage	50	60	70	V	I_C = 1.0 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 10 mA, R_{BE} = ∞
t_{on}	Turn On Time		0.5		μs	I_C = 1.5 A, R_L = 27 Ω I_{B1} = −I_{B2} = 1.5 mA, V_{CC} ≒ 40 V
t_{stg}	Storage Time		2.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$**	Collector Saturation Voltage		0.9	1.2	V	I_C = 1.5 A, I_B = 1.5 mA
$V_{BE(sat)}$**	Base Saturation Voltage		1.5	2.0	V	I_C = 1.5 A, I_B = 1.5 mA

** Pulsed / PW ≦ 350 μs, Duty Cycle ≦ 2 %

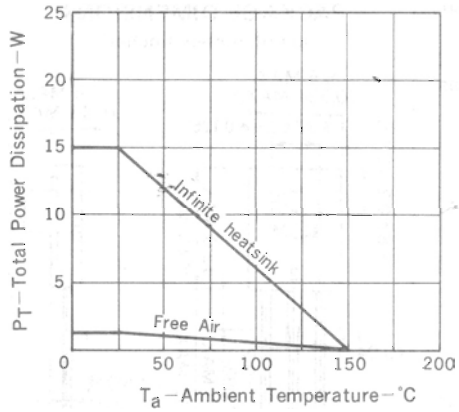
Classification of h_{FE1}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 20000

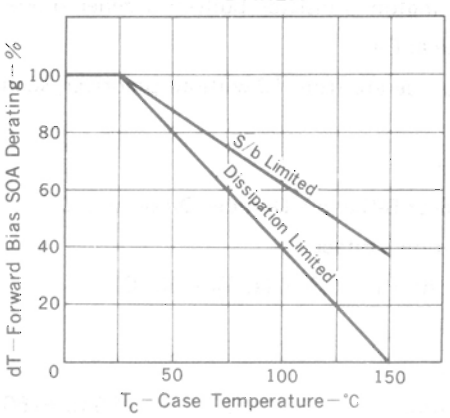
Test Conditions: V_{CE} = 2.0 V, I_C = 1.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

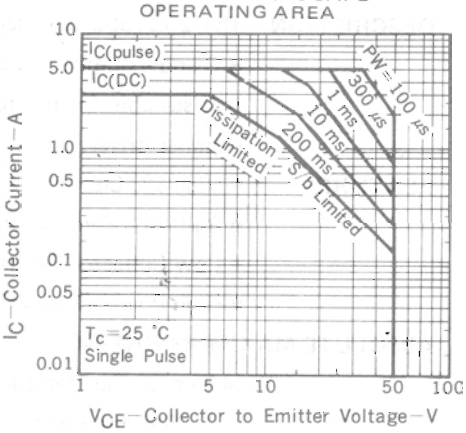
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



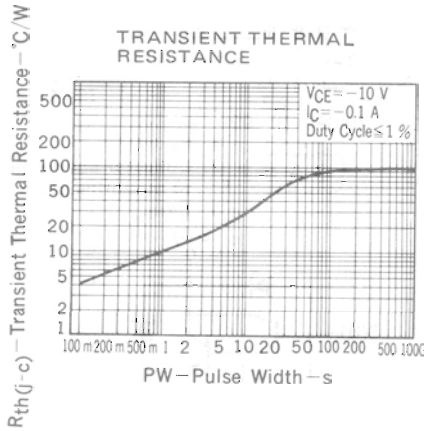
DERATING CURVE OF SAFE OPERATING AREA



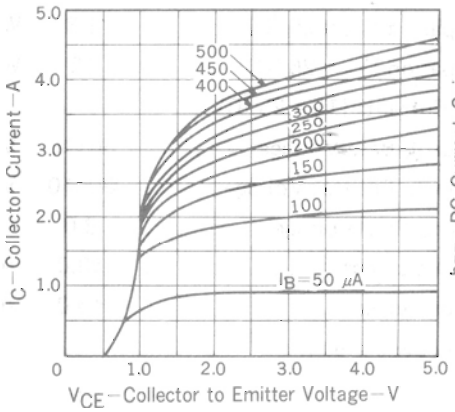
FORWARD BIAS SAFE OPERATING AREA



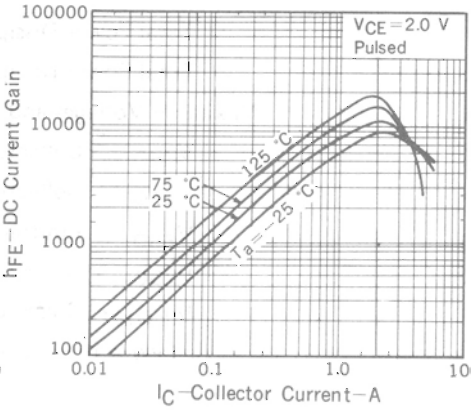
TRANSIENT THERMAL RESISTANCE



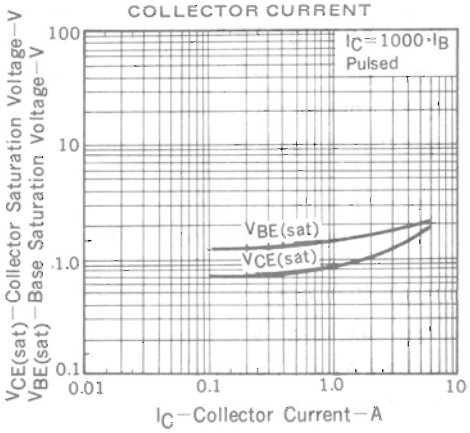
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



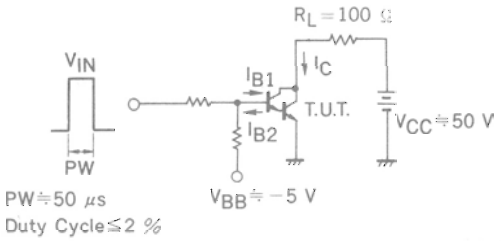
DC CURRENT GAIN vs. COLLECTOR CURRENT

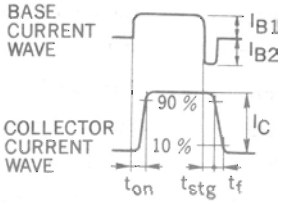


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





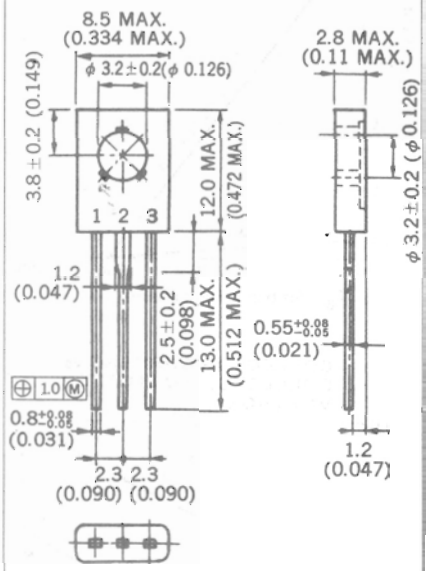
NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SD1694

DESCRIPTION The 2SD1694 is High h_{FE} and Low $V_{CE(sat)}$ transistor.
It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES
- High DC Current Gain : h_{FE} = 800 to 3200.
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.4 V MAX. (@ I_C/I_B = 2.0 A/20 mA)
- High Total Power Dissipation : P_T = 1.3 W

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Junction Temperature	+150 Maximum	°C

Maximum Power Dissipations

Total Power Dissipation (T_a = 25 °C)	1.3	W
Total Power Dissipation (T_C = 25 °C)	20	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current	3.0	A
$I_{C(pulse)}$*	Collector Current	5.0	A
$I_{B(DC)}$	Base Current	0.5	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	700	1400		—	V_{CE} = 5.0 V, I_C = 50 mA
h_{FE2}**	DC Current Gain	800	1500	3200	—	V_{CE} = 5.0 V, I_C = 0.5 A
h_{FE3}**	DC Current Gain	500	1200		—	V_{CE} = 5.0 V, I_C = 3.0 A
t_{on}	Turn-On Time		0.9	2.0	μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 20 mA, R_L = 5 Ω, V_{CC} ≒ 10 V
t_{stg}	Storage Time		2.6	4.0	μs	
t_f	Fall Time		1.0	2.0	μs	
$V_{CE(sat)}$**	Collector Saturation Voltage		0.2	0.4	V	I_C = 2.0 A, I_B = 20 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.85	1.2	V	I_C = 2.0 A, I_B = 20 mA
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 5.0 V, I_C = 0
f_T	Gain Bandwidth Product	100	250		MHz	V_{CE} = 5.0 V, I_C = 1.0 A
C_{ob}	Output Capacitance		50	60	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

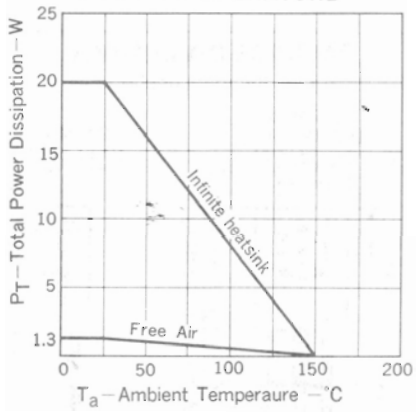
Classification of h_{FE2}

Rank	M	L	K
Range	800 to 1600	1000 to 2000	1600 to 3200

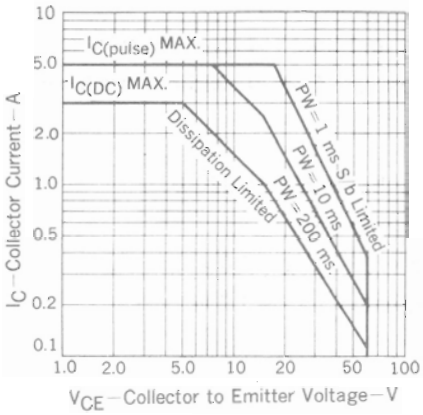
Test Conditions: V_{CE} = 5.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

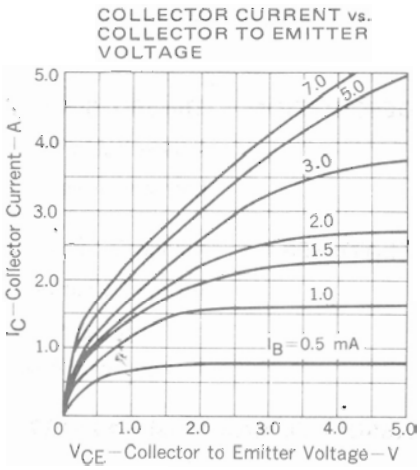
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



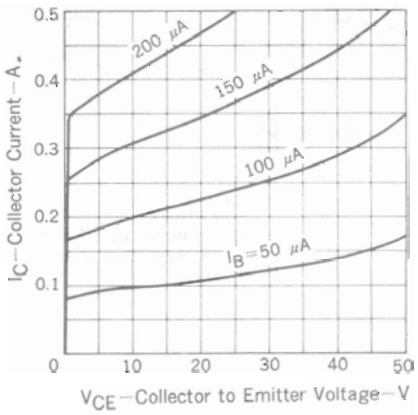
SAFE OPERATING AREA



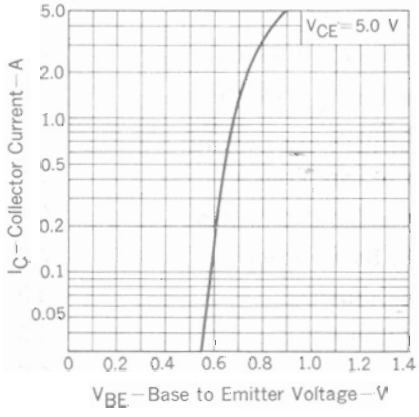
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



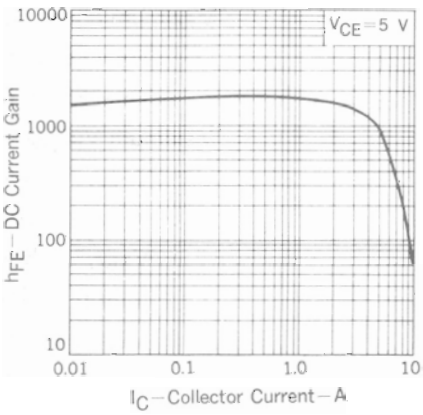
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



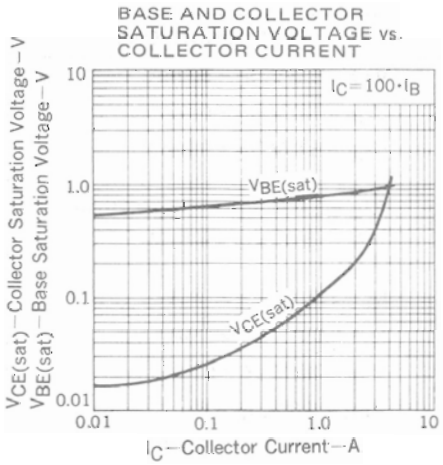
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



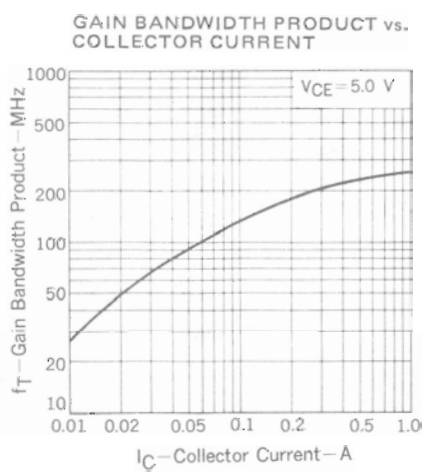
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SD1697

DESCRIPTION The 2SD1697 is NPN silicon epitaxial darlington transistor designed for pulse motor, printer driver, solenoid driver.

FEATURES

- High DC current gain
- Includes a dumper diode of E-C.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

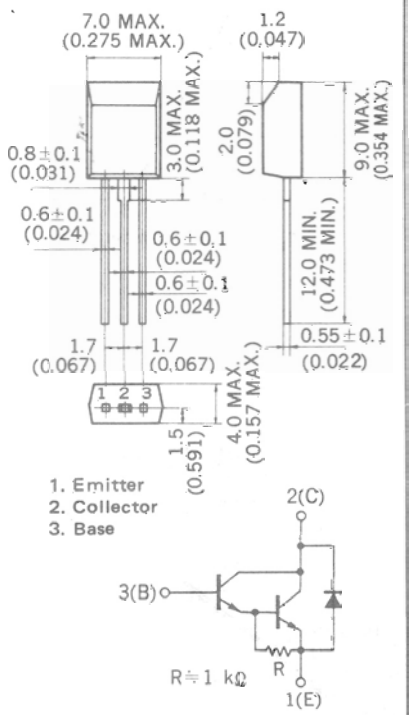
Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage . . .	80	V
V_{EBO}	Emitter to Base Voltage	8.0	V
I_C	Collector Current (DC)	±0.8	A
I_C	Collector Current (pulse)*	±1.2	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector
3. Base

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	4000		50000		V_{CE} = 2.0 V, I_C = 0.3 A
h_{FE2}**	DC Current Gain	1000				V_{CE} = 2.0 V, I_C = 0.8 A
t_{on}	Turn-on Time		0.5		μs	I_C = 0.5 A I_{B1} = −I_{B2} = 1.0 mA V_{CC} = 40 V, R_L = 80 Ω
t_{stg}	Storage Time		2.5		μs	
t_f	Fall Time		1.0		μs	
$V_{CE(sat)}$**	Collector Saturation Voltage		0.9	1.2	V	I_C = 0.5 A, I_B = 1.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		1.5	2.0	V	I_C = 0.5 A, I_B = 1.0 mA
V_{CBO}	Collector to Base Voltage	100			V	I_C = 0.1 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	80			V	I_C = 5.0 mA, I_B = 0
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 5.0 V, I_C = 0

** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE1}

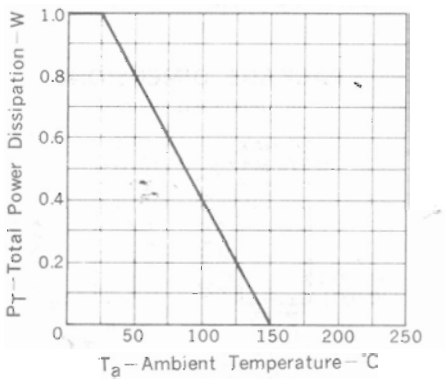
Rank	L	K
Range	4000 to 12000	8000 to 50000

Test Conditions: V_{CE} = 2.0 V, I_C = 0.3 A

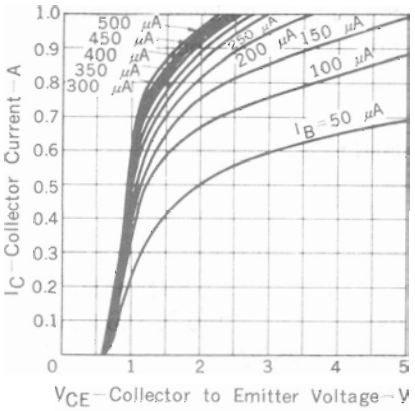
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

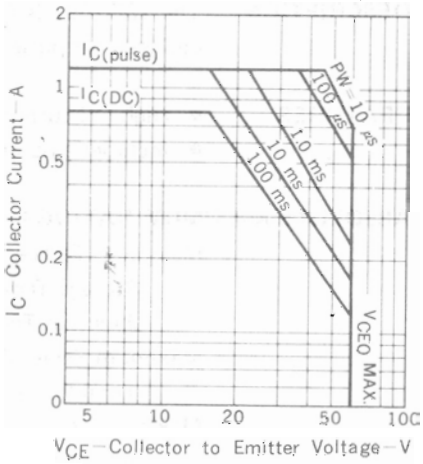
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



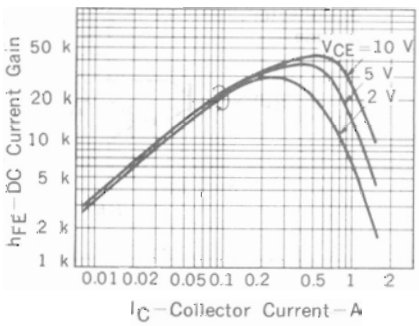
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



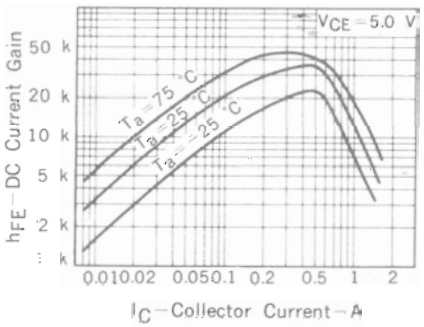
SAFE OPERATING AREA (TRANSIENT THERMAL RESISTANCE METHOD)



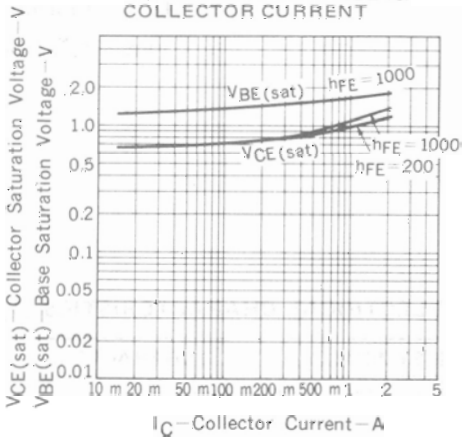
DC CURRENT GAIN vs. COLLECTOR CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

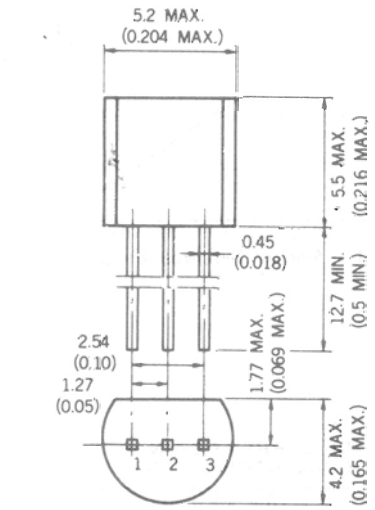
NPN SILICON TRANSISTOR
2SD1698

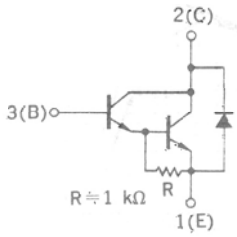
DESCRIPTION The 2SD1698 is NPN silicon epitaxial darlington transistor designed for pulse motor, printer driver, solenoid driver.

FEATURES

- High DC Current gain.
- Includes a dumper diode at E-C.

PACKAGE DIMENSIONS
in millimeters (inches)





1. Emitter
2. Collector
3. Base

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 750 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	100	V
V_{CEO}	Collector to Emitter Voltage	80	V
V_{EBO}	Emitter to Base Voltage	8.0	V
$I_{C(DC)}$	Collector Current	±0.8	A
$I_{C(pulse)}$*	Collector Current	±1.2	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	4000		50000		V_{CE} = 2.0 V, I_C = 0.3 A
h_{FE2}**	DC Current Gain	1000				V_{CE} = 2.0 V, I_C = 0.8 A
t_{on}	Turn-on Time		0.5		μs	I_C = 0.5 A I_{B1} = −I_{B2} = 1.0 mA V_{CC} = 40 V, R_L = 80 Ω
t_{stg}	Storage Time		2.5		μs	
t_f	Fall Time		1.0		μs	
$V_{CE(sat)}$**	Collector Saturation Voltage		0.9	1.2	V	I_C = 0.5 A, I_B = 1.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		1.5	2.0	V	I_C = 0.5 A, I_B = 1.0 mA
V_{CBO}	Collector to Base Voltage	100			V	I_C = 0.1 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	80			V	I_C = 5.0 mA, I_B = 0
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 80 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 5.0 V, I_C = 0

** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE1}

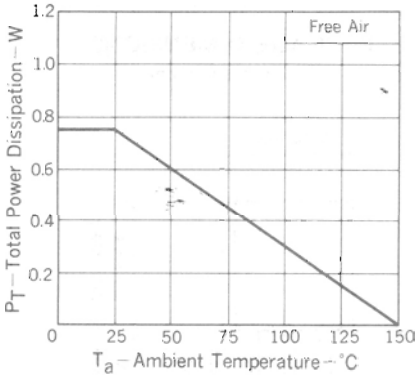
Rank	L	K
Range	4000 to 12000	8000 to 50000

Test Conditions: V_{CE} = 2.0 V, I_C = 0.3 A

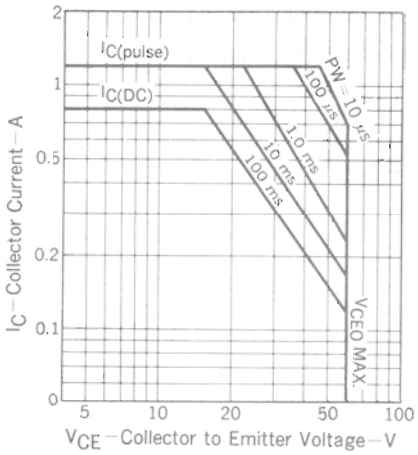
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

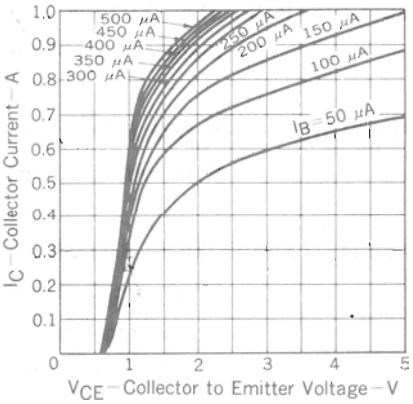
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



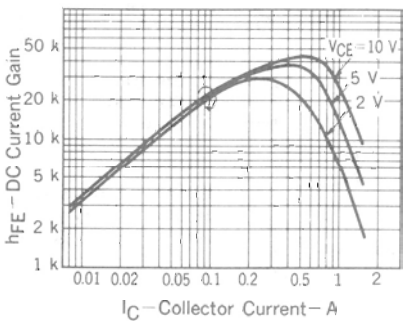
SAFE OPERATING AREAS (TRANSIENT THERMAL RESRISTANCE METHOD)



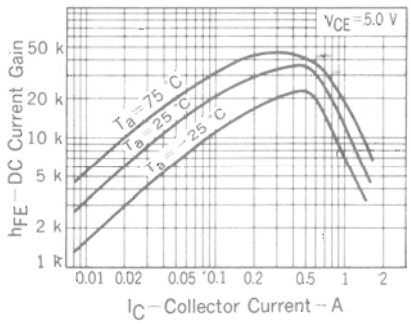
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



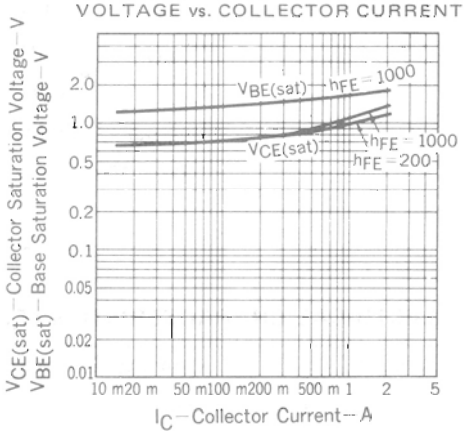
DC CURRENT GAIN vs. COLLECTOR CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

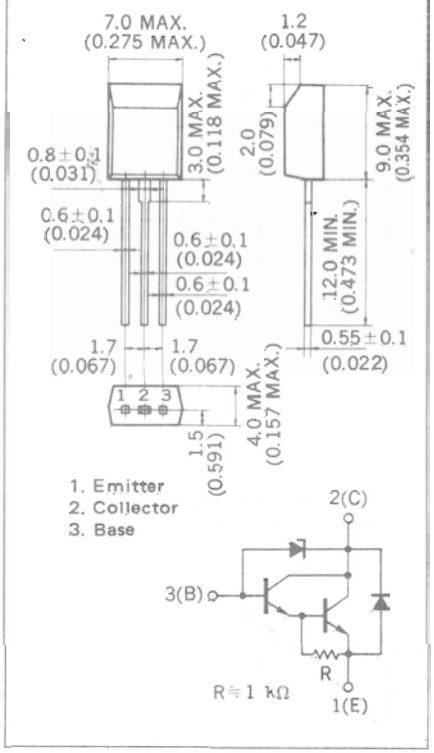
NPN SILICON TRANSISTOR
2SD1700

DESCRIPTION The 2SD1700 is NPN silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- High DC Current Gain
- Zener Diode between Collector and Base for Absorbing Surge Voltage is built-in.
- Reverse Diode between Collector and Emitter is built-in.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60±10	V
V_{CEO}	Collector to Emitter Voltage	60±10	V
V_{EBO}	Emitter to Base Voltage	8.0	V
I_C	Collector Current (DC)	±0.8	A
I_C	Collector Current (pulse)*	±1.2	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	4000		50000		V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2}**	DC Current Gain	1000				V_{CE} = 2.0 V, I_C = 0.8 A
t_{on}	Turn-on Time		0.5		μs	I_C = 0.5 A I_{B1} = −I_{B2} = 1.0 mA V_{CC} = 40 V, R_L = 80 Ω
t_{stg}	Storage Time		2.5		μs	
t_f	Fall-Time		1.0		μs	
$V_{CE(sat)}$**	Collector Saturation Voltage		0.9	1.2	V	I_C = 0.5 A, I_B = 1.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		1.5	2.0	V	I_C = 0.5 A, I_B = 1.0 mA
V_{CBO}	Collector to Base Voltage	50	60	70	V	I_C = 0.1 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 5.0 mA, I_B = 0
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 5.0 V, I_C = 0

** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE1}

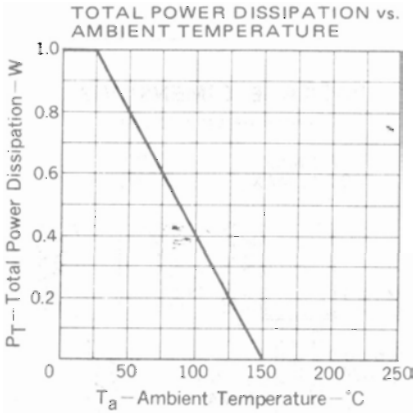
Rank	L	K
Range	4000 to 12000	8000 to 50000

Test Conditions: V_{CE} = 2.0 V, I_C = 0.5 A

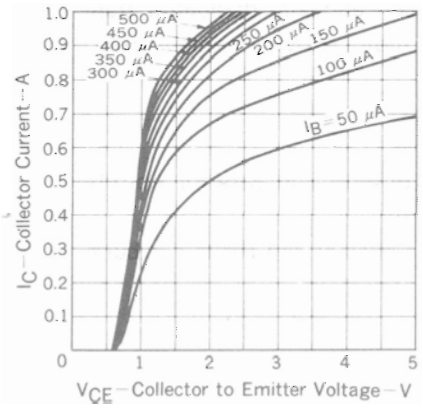
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

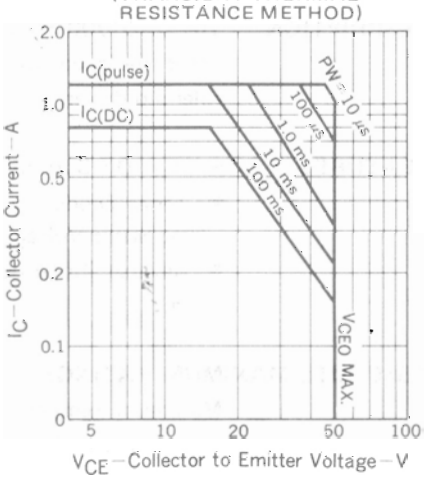
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



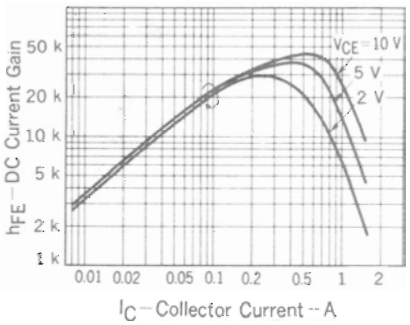
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



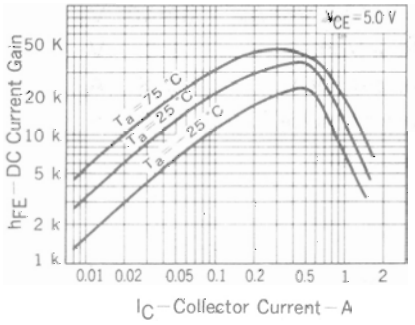
SAFE OPERATING AREA (TRANSIENT THERMAL RESISTANCE METHOD)



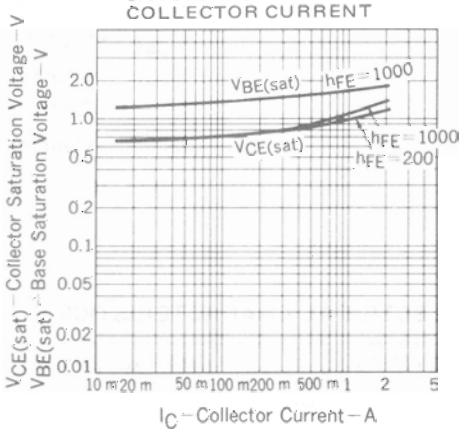
DC CURRENT GAIN vs. COLLECTOR CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

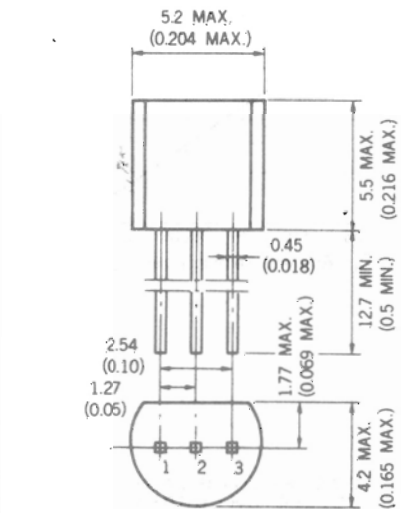
NPN SILICON TRANSISTOR
2SD1701

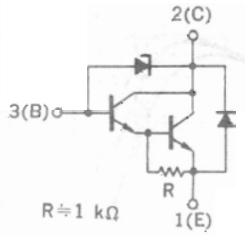
DESCRIPTION The 2SD1701 is NPN silicon epitaxial darlington transistor designed for pulse motor driver, printer driver, solenoid driver.

FEATURES

- High DC Current gain.
- Zener Diode between Collector and Base for Absorbing Surge Voltage is built-in.
- Reverse Diode between Collector and Emitter is built-in.

PACKAGE DIMENSIONS
in millimeters (inches)





1. Emitter
2. Collector
3. Base

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 750 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60±10	V
V_{CEO}	Collector to Emitter Voltage	60±10	V
V_{EBO}	Emitter to Base Voltage	8.0	V
$I_{C(DC)}$	Collector Current	±0.8	A
$I_{C(pulse)}$*	Collector Current	±1.2	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	4000		50000		V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2}**	DC Current Gain	1000				V_{CE} = 2.0 V, I_C = 0.8 A
t_{on}	Turn-on Time		0.5		μs	I_C = 0.5 A I_{B1} = −I_{B2} = 1.0 mA V_{CC} = 40 V, R_L = 80 Ω
t_{stg}	Storage Time		2.5		μs	
t_f	Fall-Time		1.0		μs	
$V_{CE(sat)}$**	Collector Saturation Voltage		0.9	1.2	V	I_C = 0.5 A, I_B = 1.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		1.5	2.0	V	I_C = 0.5 A, I_B = 1.0 mA
V_{CBO}	Collector Base Voltage	50	60	70	V	I_C = 0.1 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 5.0 mA, I_B = 0
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 5.0 V, I_C = 0

** Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE1}

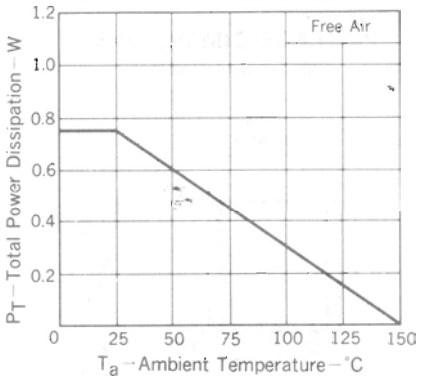
Rank	L	K
Range	4000 to 12000	8000 to 50000

Test Conditions: V_{CE} = 2.0 V, I_C = 0.5 A

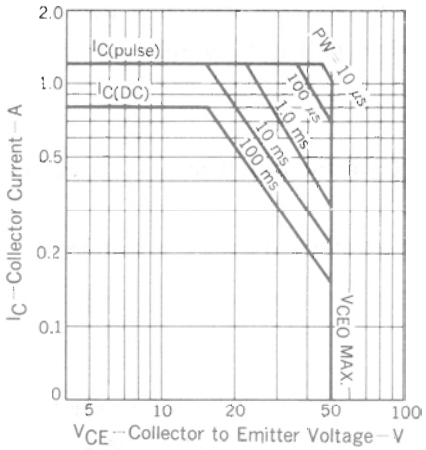
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

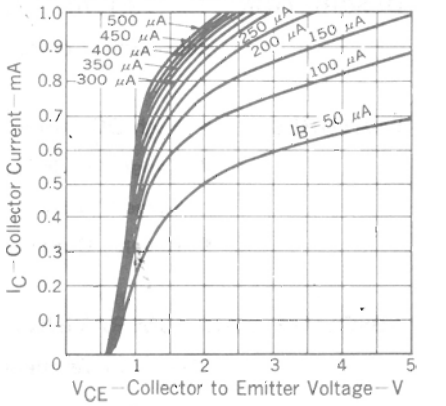
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



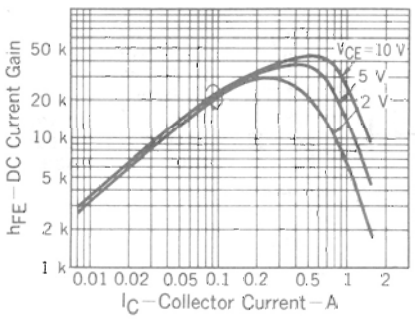
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



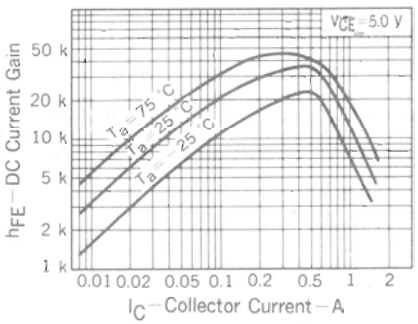
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



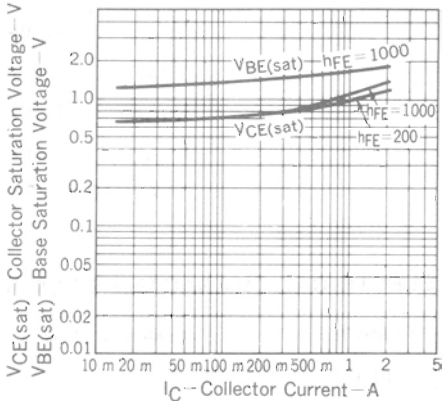
DC CURRENT GAIN vs. COLLECTOR CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
2SD1779

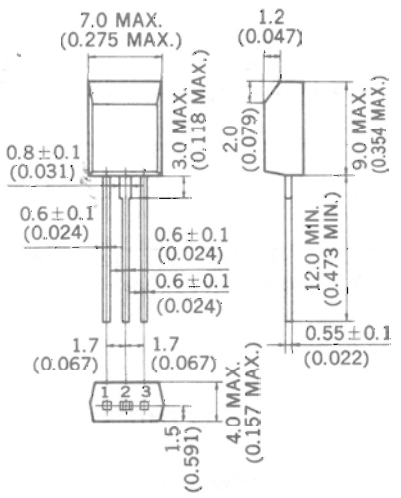
NEW DEVICE

DESCRIPTION The 2SD1779 is high h_{FE} transistor.
It is suitable for use to operate from IC without predriver, such as hammer or motor driver.

FEATURES

- High DC Current Gain.
  h_{FE} = 800 to 3200 (@V_{CE} = 5.0 V, I_C = 1.0 A)
- Wide "SOA".
  V_{CEO} = 60 V, $I_{C(DC)}$ = 2.0 A
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.20 V TYP. (@I_C = 1.0 A, I_B = 10 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 60 V
- V_{EBO} Emitter to Base Voltage . . . . . 15 V
- I_C Collector Current (DC) . . . . . 2.0 A
- I_C^* Collector Current (pulse) . . . . . 3.0 A

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	800	1500	3200	—	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE2}**	DC Current Gain	500			—	V_{CE} = 5.0 V, I_C = 2.0 A
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 12 V, I_C = 0
$V_{CE(sat)1}$**	Collector Saturation Voltage		0.1	0.2	V	I_C = 0.5 A, I_B = 5.0 mA
$V_{CE(sat)2}$**	Collector Saturation Voltage		0.2	0.3	V	I_C = 1.0 A, I_B = 10 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.8	1.2	V	I_C = 1.0 A, I_B = 10 mA
t_{on}	Turn On Time		0.8		μs	I_C = 1.0 A
t_{stg}	Storage Time		2.0		μs	I_{B1} = −I_{B2} = 10 mA
t_f	Fall Time		1.2		μs	R_L = 20 Ω, V_{CC} = 20 V

** PW ≦ 350 μs, Duty Cycle ≦ 2 %

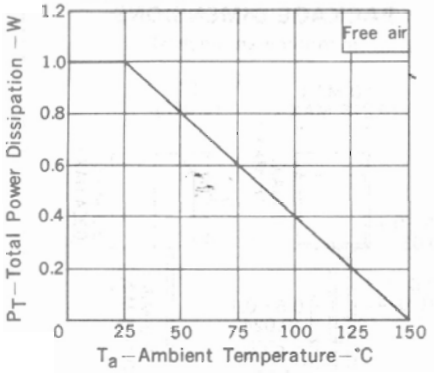
Classification of h_{FE1}

Rank	M	L	K
Range	800 to 1600	1200 to 2400	2000 to 3200

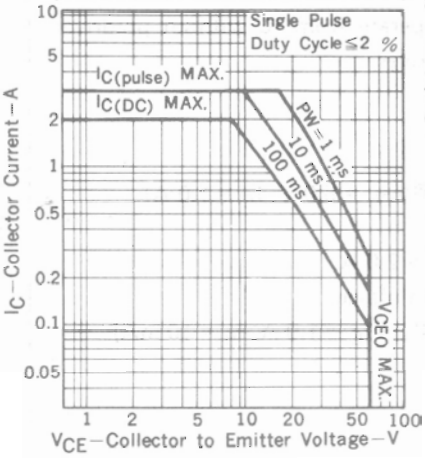
Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

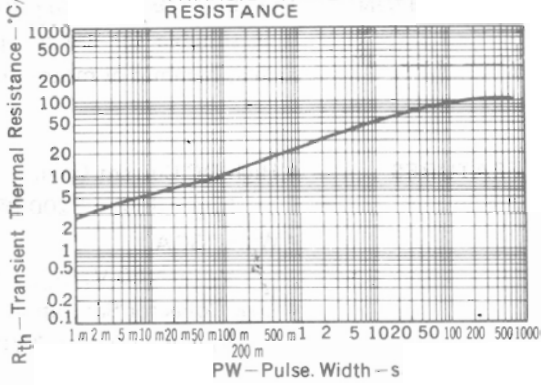
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



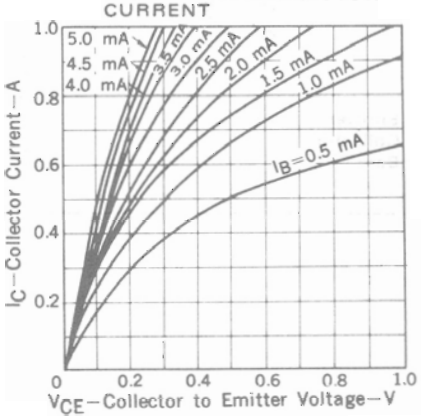
SAFE OPERATING AREA (TRANSIENT THERMAL METHOD)



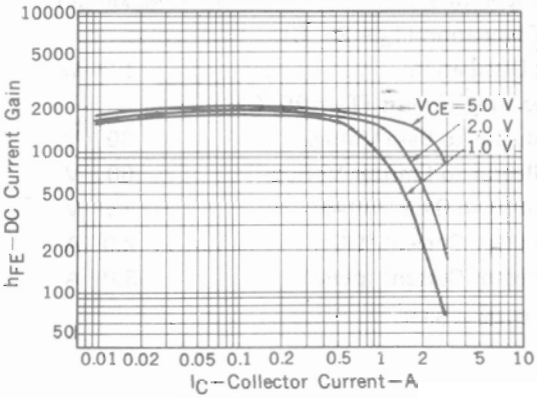
TRANSIENT THERMAL RESISTANCE



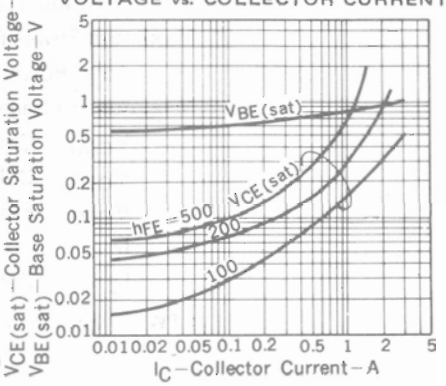
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SICICON TRANSISTOR
2SD1780

DESCRIPTION

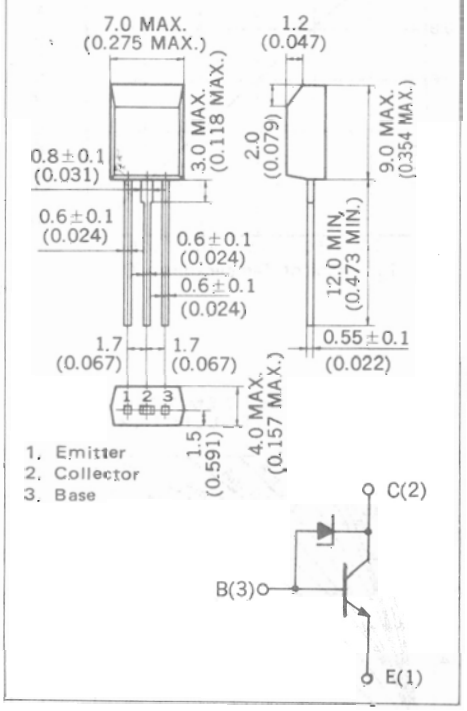
The 2SD1780 is high h_{FE} transistor, built-in a zener diode at B-C.

It is suitable for use to operate from IC without predriver, such as hammer or motor driver.

FEATURES

- Built in 60 V Zener Diode at B-C.
- High DC Current Gain.
  h_{FE} = 800 to 3200 (@V_{CE} = 5.0 V, I_C = 1.0 A)
- Wide "SOA".
  V_{CEO} = 60 ± 10 V, $I_{C(DC)}$ = 2.0 A
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.20 TYP. (@I_C = 1.0 A, I_B = 10 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60 ± 10	V
V_{CEO}	Collector to Emitter Voltage	60 ± 10	V
V_{EBO}	Emitter to Base Voltage	15	V
I_C	Collector Current (DC)	2.0	A
I_C*	Collector Current (pulse)	3.0	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{CBO}	Collector to Base Voltage	50	60	70	V	I_C = 1.0 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 10 mA, R_{BE} = ∞
h_{FE1}**	DC Current Gain	800	1500	3200	–	V_{CE} = 5.0 V, I_C = 1.0 A
h_{FE2}**	DC Current Gain	500			–	V_{CE} = 5.0 V, I_C = 2.0 A
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Base Cutoff Current			100	nA	V_{EB} = 12 V, I_C = 0
$V_{CE(sat)1}$**	Collector Saturation Voltage		0.1	0.2	V	I_C = 0.5 A, I_B = 5.0 mA
$V_{CE(sat)2}$**	Collector Saturation Voltage		0.2	0.3	V	I_C = 1.0 A, I_B = 10 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.8	1.2	V	I_C = 1.0 A, I_B = 10 mA
t_{on}	Turn On Time		0.8		μs	I_C = 1.0 A
t_{stg}	Storage Time		2.0		μs	I_{B1} = −I_{B2} = 10 mA
t_f	Fall Time		1.2		μs	R_L = 20 Ω, V_{CC} = 20 V

** PW ≤ 350 μs, Duty Cycle ≤ 2 %

Classification of h_{FE1}

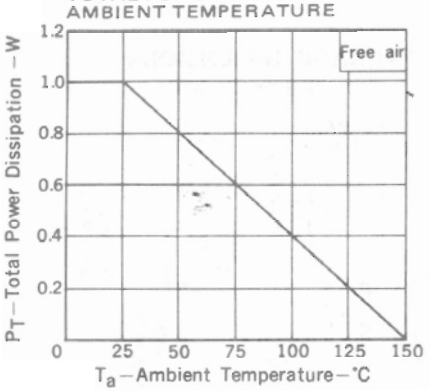
Rank	M	L	K
Range	800 to 1600	1200 to 2400	2000 to 3200

Test Conditions: V_{CE} = 5.0 V, I_C = 1.0 A

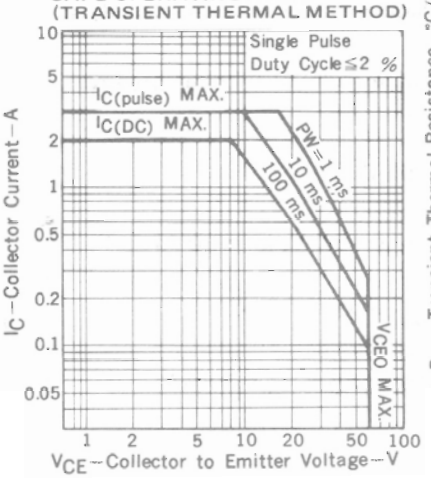
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

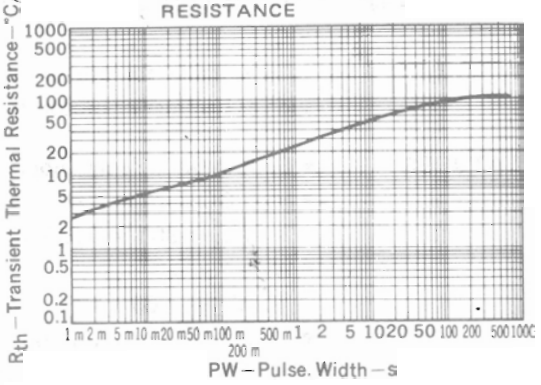
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



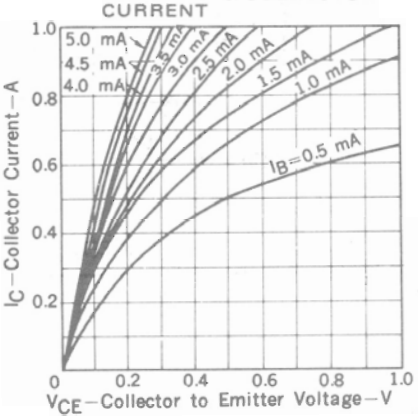
SAFE OPERATING AREA (TRANSIENT THERMAL METHOD)



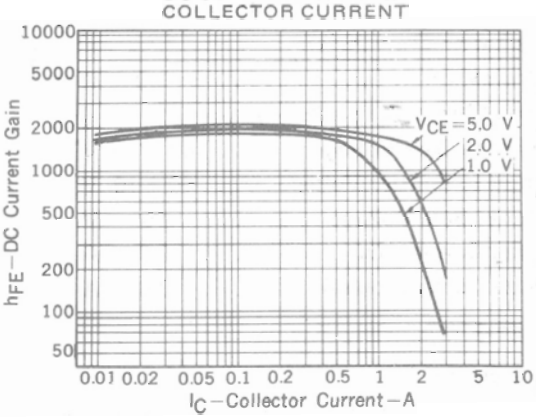
TRANSIENT THERMAL RESISTANCE



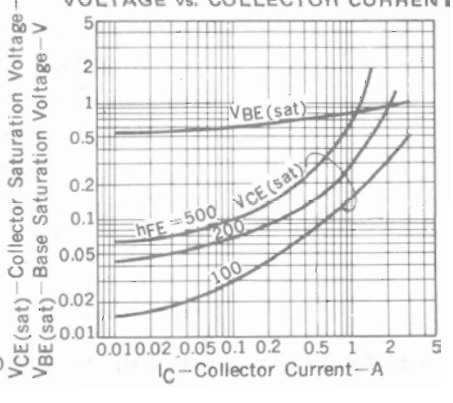
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON POWER TRANSISTOR
2SD1818

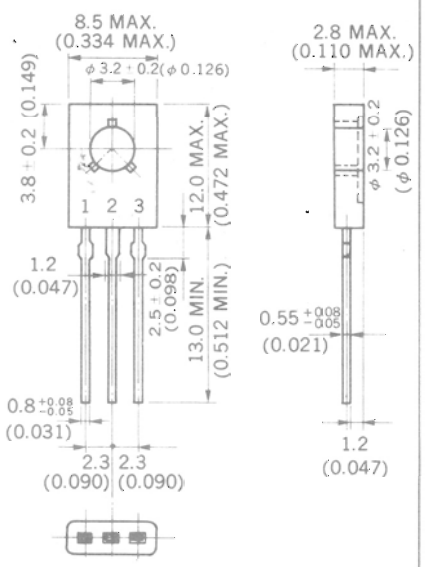
DESCRIPTION

The 2SD1818 is a Low $V_{CE(sat)}$ transistor which has a large current capability and wide SOA.
It is suitable for DC-DC converter, or driver of solenoid or motor.

FEATURES

- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.25 V MAX. (@ I_C/I_B = 1.5 A/0.15 A)
- Large Current
  $I_{C(DC)}$ = 3.0 A, $I_{C(pulse)}$ = 5.0 A
- High Total Power Dissipation: P_T = 1.3 W
- Complementary to 2SB1217

PACKAGE DIMENSIONS
in millimeters (inches)



1. Emitter
2. Collector connected to mounting plane
3. Base

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

	Total Power Dissipation (T_a = 25 °C) . . .	1.3	W
	Total Power Dissipation (T_C = 25 °C) . . .	10	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage . .	60	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current	3.0	A
$I_{C(pulse)}$	Collector Current*	5.0	A
$I_{B(DC)}$	Base Current	0.5	A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$V_{CE(sat)}$**	Collector Saturation Voltage		0.14	0.25	V	I_C = 1.5 A, I_B = 0.15 A
$V_{BE(sat)}$**	Base Saturation Voltage		0.9	1.2	V	I_C = 1.5 A, I_B = 0.15 A
h_{FE1}**	DC Current Gain	60			—	V_{CE} = 2.0 V, I_C = 0.2 A
h_{FE2}**	DC Current Gain	100		400	—	V_{CE} = 2.0 V, I_C = 0.6 A
h_{FE3}**	DC Current Gain	50			—	V_{CE} = 2.0 V, I_C = 2.0 A
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			10	μA	V_{EB} = 7.0 V, I_C = 0
t_{on}	Turn On Time		0.15	0.5	μs	I_C = 2.0 A, I_{B1} = −I_{B2} = 0.2 A R_L = 5.0 Ω, V_{CC} ≒ 10 V
t_{stg}	Storage Time		0.75	2.0	μs	
t_f	Fall Time		0.2	0.5	μs	

**PW ≦ 350 μs, Duty Cycle ≦ 2 %

Classification of h_{FE2}

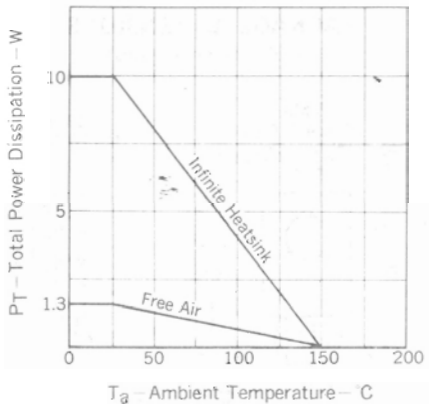
Rank	M	L	K
Range	100 to 200	160 to 320	200 to 400

Test Conditions: V_{CE} = 2.0 V, I_C = 0.6 A

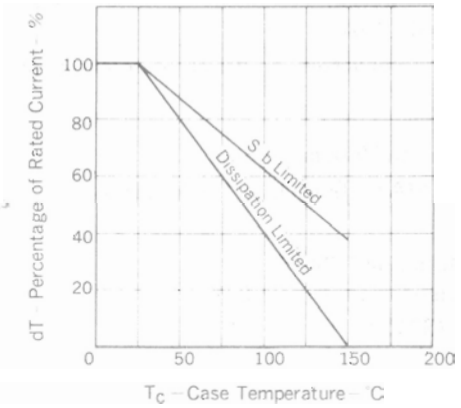
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

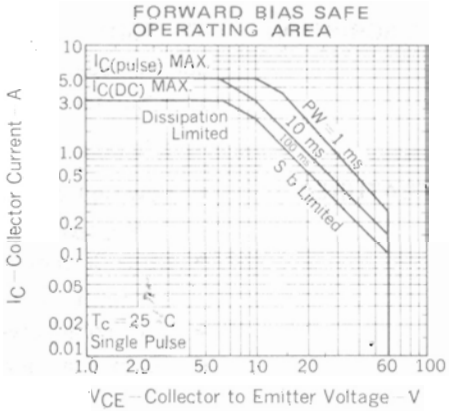
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



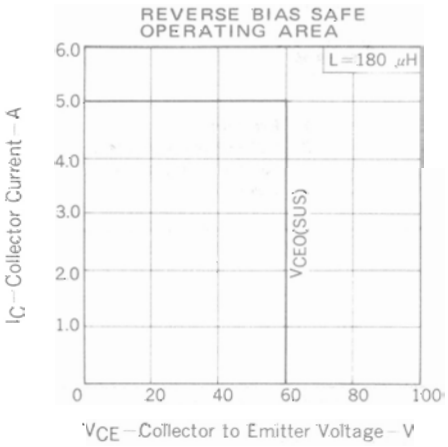
DERATING CURVE OF SAFE OPERATING AREA



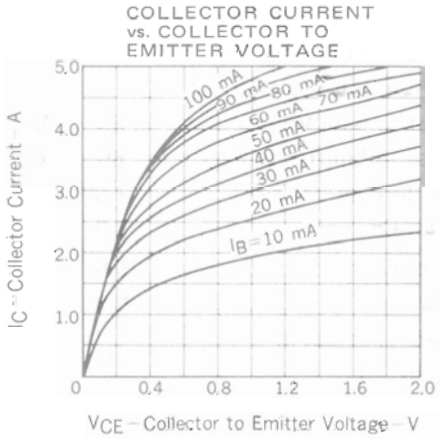
FORWARD BIAS SAFE OPERATING AREA



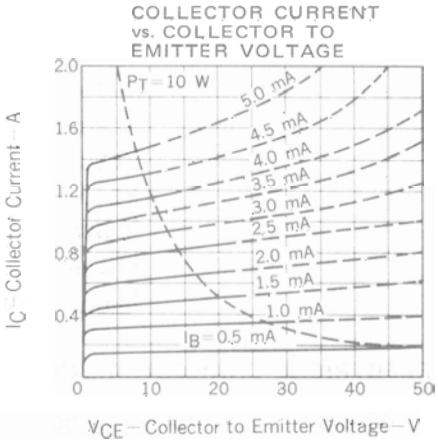
REVERSE BIAS SAFE OPERATING AREA



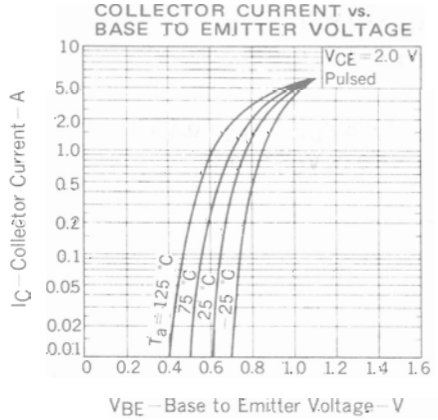
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



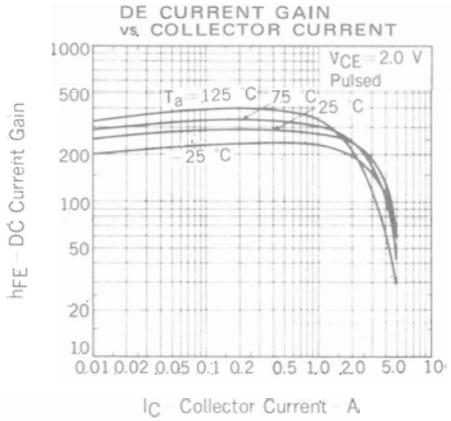
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



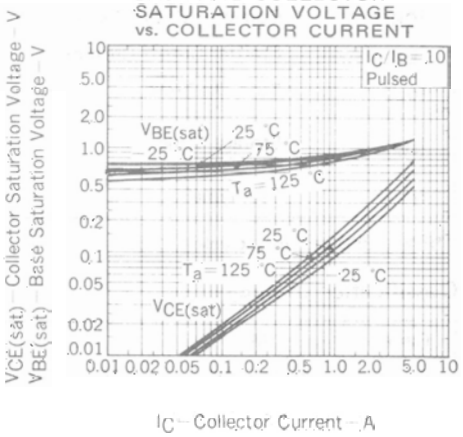
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



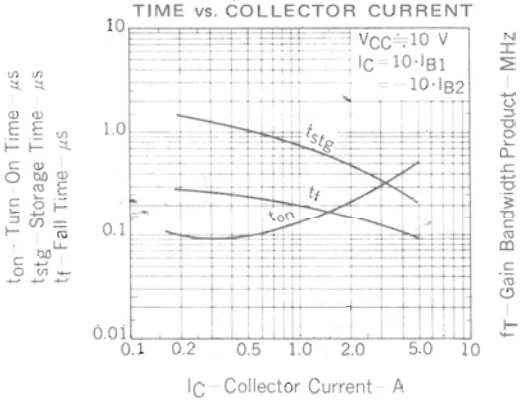
DE CURRENT GAIN vs. COLLECTOR CURRENT



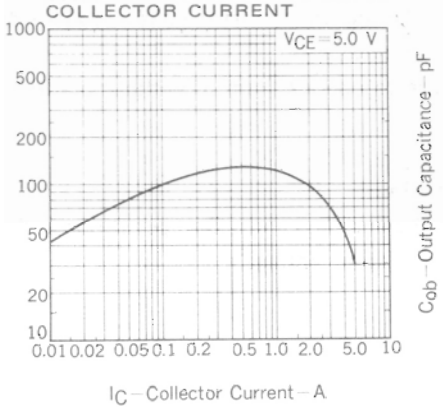
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



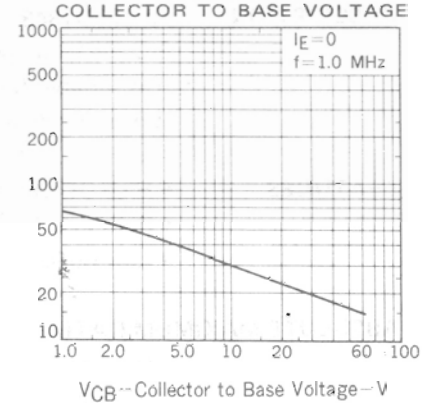
TURN-ON, STORAGE AND FALL TIME vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON DARLINGTON TRANSISTOR
2SD1843

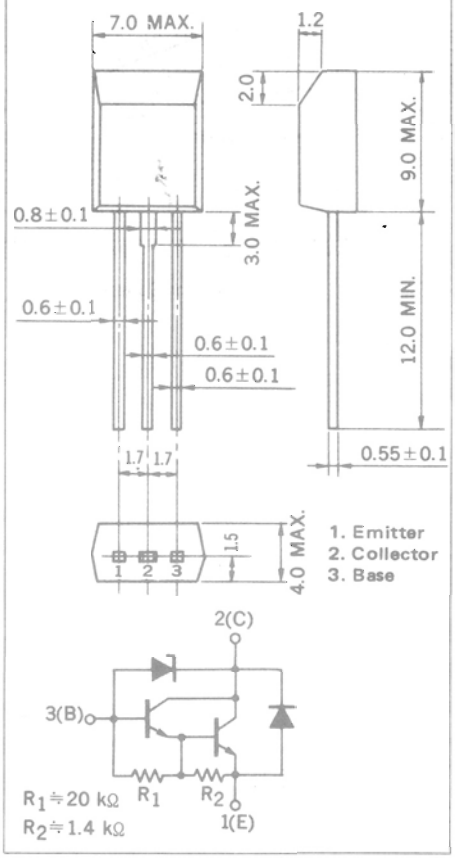
NEW DEVICE

DESCRIPTION The 2SD1843 is a darlington transistor built-in a zener diode at B-C and a dumper diode at E-C.
It is suitable for use to operate from IC without predriver, such as hammer driver.

FEATURES

- High DC Current Gain.
- Built-in a Zener Diode at B-C and a Dumper Diode at E-C.
- Low Collector Saturation Voltage.

PACKAGE DIMENSIONS
in millimeters



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation

- Total Power Dissipation (T_a = 25 °C) . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	60 ± 10	V
V_{CEO}	Collector to Emitter Voltage	60 ± 10	V
V_{EBO}	Emitter to Base Voltage	7.0	V
$I_{C(DC)}$	Collector Current	± 1.0	A
$I_{C(pulse)}$ *	Collector Current	± 2.0	A

* PW ≤ 10 ms, Duty Cycle ≤ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1} **	DC Current Gain	1000			—	V_{CE} = 2.0 V, I_C = 0.2 A
h_{FE2} **	DC Current Gain	2000		30000	—	V_{CE} = 2.0 V, I_C = 0.5 A
V_{CBO}	Collector to Base Voltage	50	60	70	V	I_C = 1.0 mA, I_E = 0
V_{CEO}	Collector to Emitter Voltage	50	60	70	V	I_C = 10 mA, R_{BE} = ∞
t_{on}	Turn On Time		0.5		μs	I_C = 0.5 A, R_L = 100 Ω I_{B1} = −I_{B2} = 0.5 mA, V_{CC} = 50 V
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			0.5	μA	V_{CB} = 40 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$ **	Collector Saturation Voltage			1.5	V	I_C = 0.5 A, I_B = 0.5 mA
$V_{BE(sat)}$ **	Base Saturation Voltage			2.0	V	I_C = 0.5 A, I_B = 0.5 mA

** Pulsed / PW ≤ 350 μs, Duty Cycle ≤ 2 %

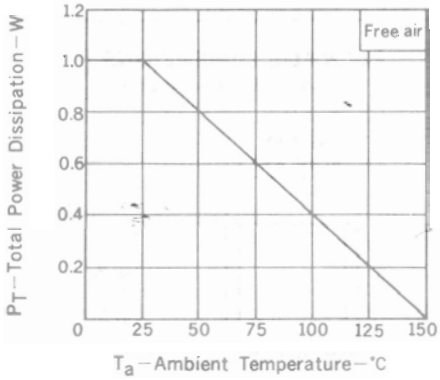
Classification of h_{FE2}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 30000

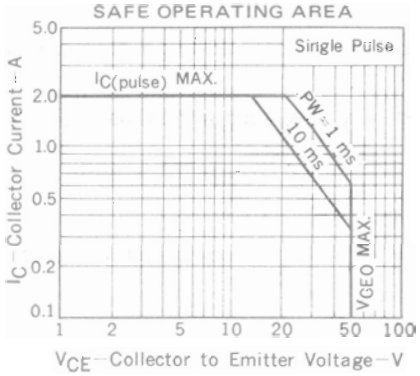
Test Conditions: V_{CE} = 2.0 V, I_C = 0.5 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

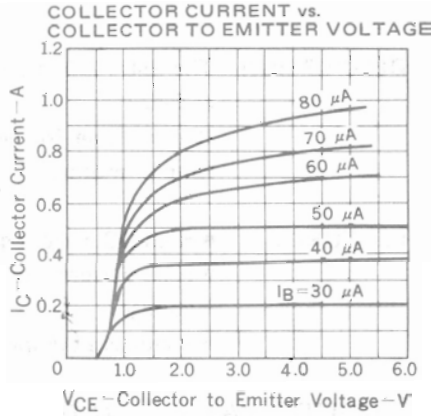
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



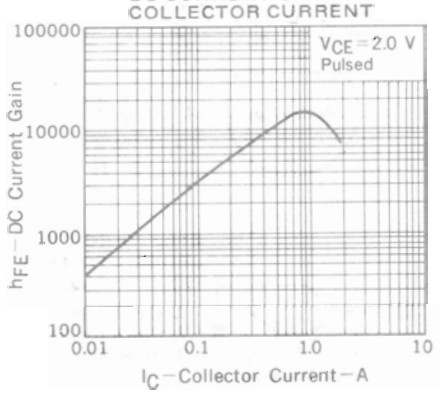
SAFE OPERATING AREA



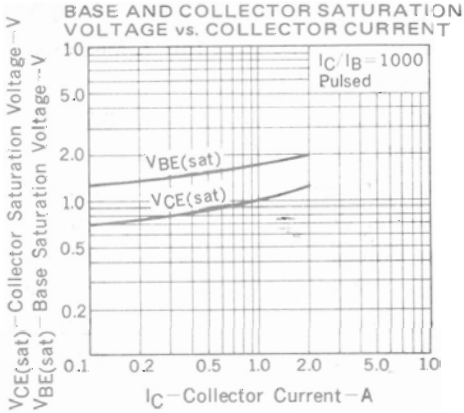
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



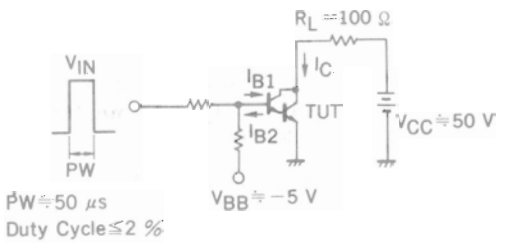
DC CURRENT GAIN vs. COLLECTOR CURRENT

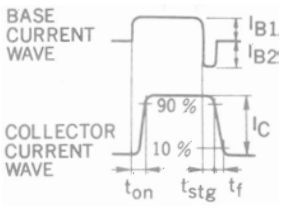


BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT





NEC
ELECTRON DEVICE

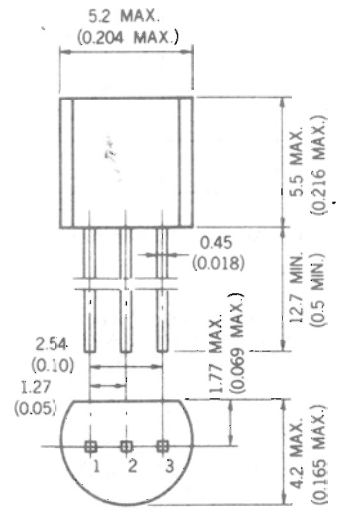
NPN SILICON DARLINGTON TRANSISTOR
2SD1939

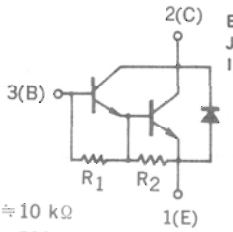
NEW DEVICE

DESCRIPTION The 2SD1939 is a darlington transistor including a dumper diode at E-C.
It is suitable for general driving use, such as hammer, solenoid, lamp or motor.

FEATURES
- High DC current gain.
- High current capability, wide ASO and low collector saturation voltage.
- Includes a dumper diode at E-C.

PACKAGE DIMENSIONS
in millimeters (inches)





EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33
1. Emitter (E)
2. Collector (C)
3. Base (B)

$R_1 \fallingdotseq 10\ k\Omega$
$R_2 \fallingdotseq 500\ \Omega$

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 150 V
- V_{CEO} Collector to Emitter Voltage . . . . . 80 V
- V_{EBO} Emitter to Base Voltage . . . . . 8.0 V
- I_C Collector Current (DC) . . . . . ±1.5 A
- I_C Collector Current (Pulse)* . . . . . ±3.0 A
- I_B Base Current (DC) . . . . . 0.15 A

*PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	1000			–	V_{CE} = 2.0 V, I_C = 0.5 A
h_{FE2}	DC Current Gain	2000		30000	–	V_{CE} = 2.0 V, I_C = 1.0 A
t_{on}	Turn-On Time		0.5		μs	(I_C = 1.0 A, R_L = 50 Ω, $I_{B1} = -I_{B2}$ = 1.0 mA, V_{CC} = 50 V, See Test Circuit)
t_{stg}	Storage Time		1.0		μs	
t_f	Fall Time		1.0		μs	
I_{CBO}	Collector Cutoff Current			10	μA	V_{CB} = 80 V, I_E = 0
I_{CER}	Collector Cutoff Current			1.0	mA	V_{CE} = 80 V, R_{BE} = 51 Ω, T_a = 125 °C
I_{CEX1}	Collector Cutoff Current			10	μA	V_{CE} = 80 V, $V_{BE(off)}$ = −1.5 V
I_{CEX2}	Collector Cutoff Current			1.0	mA	V_{CE} = 80 V, $V_{BE(off)}$ = −15 V, T_a = 125 °C
I_{EBO}	Emitter Cutoff Current			1.0	mA	V_{EB} = 5.0 V, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			1.5	V	I_C = 1.0 A, I_B = 1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage			2.0	V	
f_T	Gain Bandwidth Product		60		MHz	V_{CE} = 10 V, I_E = −1.0 A

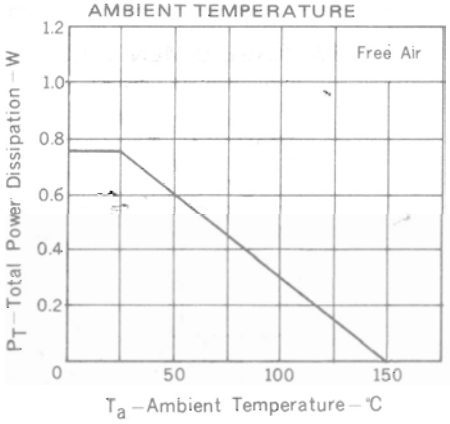
Classification of h_{FE2}

Rank	M	L	K
Range	2000 to 5000	4000 to 10000	8000 to 30000

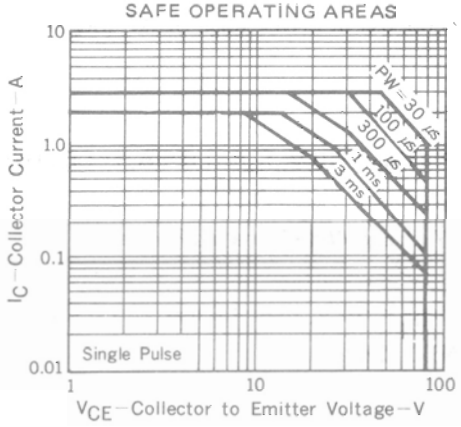
Test Conditions: V_{CE} = 2.0 V, I_C = 1.0 A

TYPICAL CHARACTERISTICS (T_a = 25 °C)

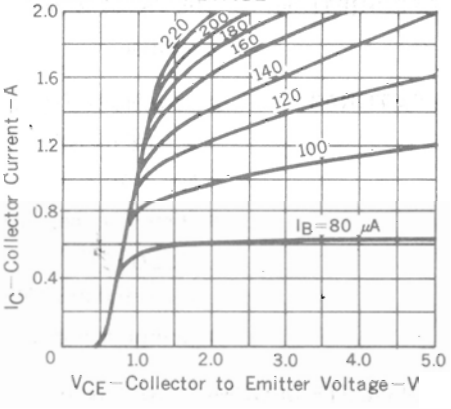
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



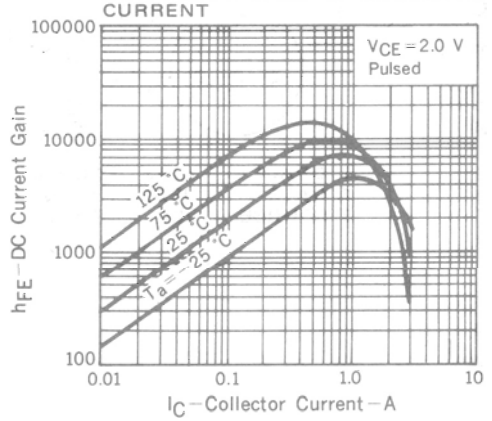
SAFE OPERATING AREAS



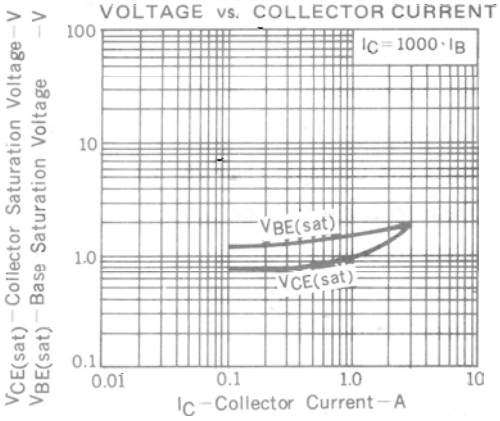
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



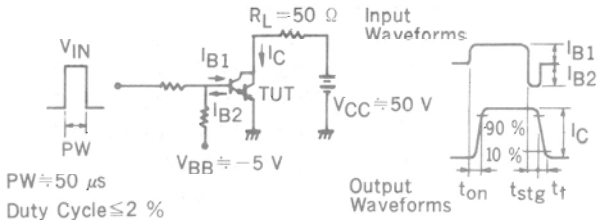
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



NEC
ELECTRON DEVICE

P-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

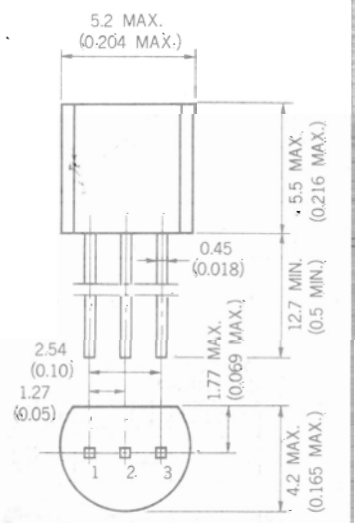
2SJ44

DESCRIPTION The 2SJ44 is designed for use in driver stage of AF low noise amplifier.

FEATURES

- Low Noise Figure
  e_n=1.5 nV/$\sqrt{Hz}$ TYP. (V_{DS}=−10 V, I_D=−1.0 mA, f=1.0 kHz)
  NV ≦ 20 mV
- High Voltage, High $|Y_{fs}|$, and Wide Dynamic Range
  V_{GDO} ≧ 40 V
  $|Y_{fs}|$=9.0 mS TYP. (V_{DS}=−10 V, I_D=−1.0 mA, f=1.0 kHz)
- Complementary to NEC 2SK163

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	40	V
V_{GSO}	Gate to Source Voltage	40	V
V_{DSX} *	Drain to Source Voltage	−40	V
I_D	Drain Current	−30	mA
I_G	Gate Current	−10	mA

* V_{GS} = −2.0 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	−1.0	−9.0	−18	mA	V_{DS} = −10 V, V_{GS} = 0
$\|Y_{fs}\|_1$	Forward Transfer Admittance	7.0	9.0		mS	V_{DS} = −10 V, I_D = −1.0 mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	7.0			mS	V_{DS} = −10 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		50		pF	V_{DS} = −10 V, V_{GS} = 0, f = 1.0 MHz
C_{rss}	Feedback Capacitance		10		pF	V_{DS} = −10 V, V_{GS} = 0, f = 1.0 MHz
NV	Noise Voltage		16	20	mV	See test circuit
I_{GSS}	Gate Cutoff Current			1.0	nA	V_{GS} = 20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	0.2		1.5	V	V_{DS} = −10 V, I_D = −10 μA

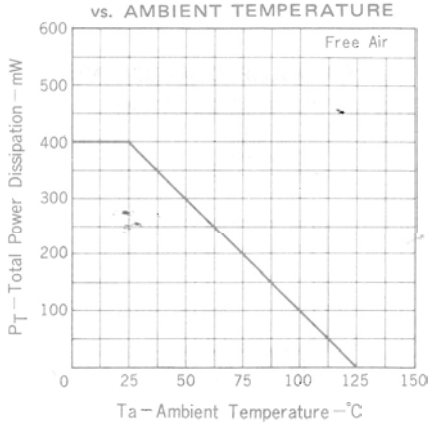
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	−1.0 — −6.0	−5.0 — −10	−9.0 — −14	−13 — −18

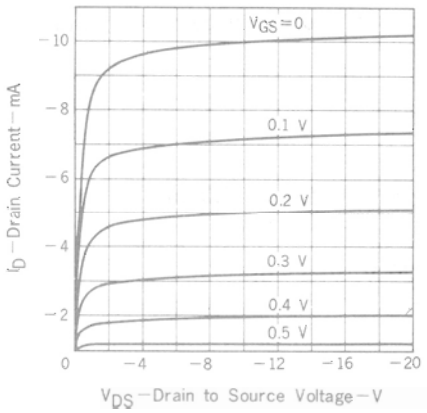
I_{DSS} Test Conditions : V_{DS} = −10 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

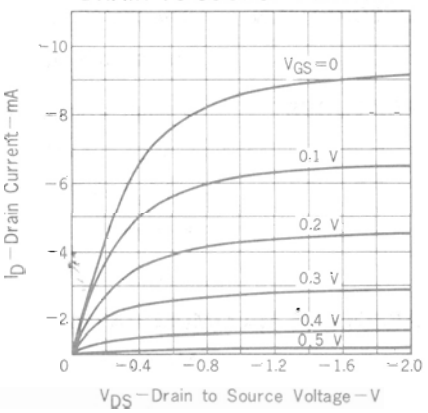
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



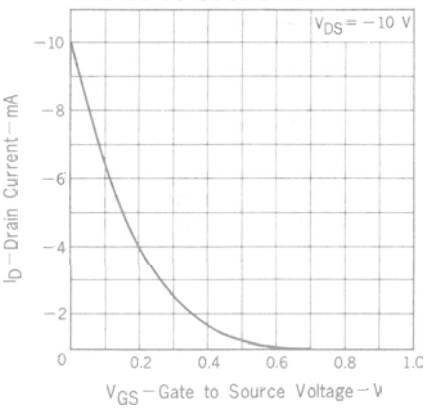
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



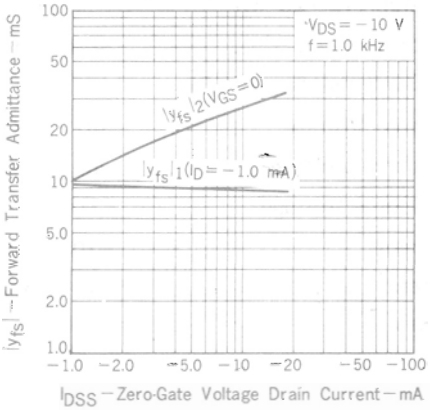
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



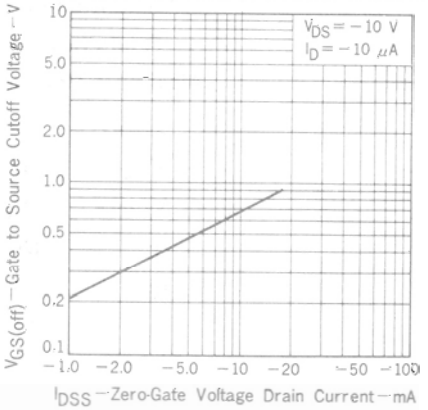
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



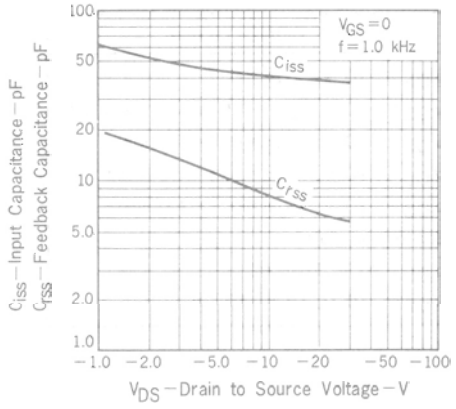
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



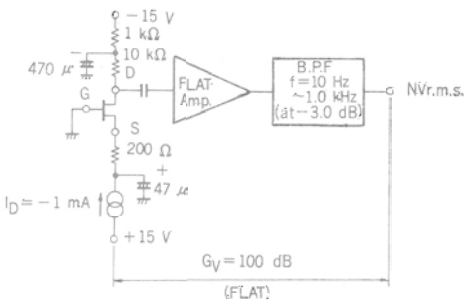
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE VOLTAGE TEST CIRCUIT



$V_{DS} \fallingdotseq -4$ V, $I_D = -1.0$ mA, $R_G = 0$, $G_V = 100$ dB,
f = 10 Hz – 1.0 kHz (at −3.0 dB)

NEC
ELECTRON DEVICE

P-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

2SJ45

DESCRIPTION The 2SJ45 is designed for use in driver stage of AF amplifier and switching circuit.

FEATURES

- High Voltage, High $|Y_{fs}|$
  $V_{GDO} \geqq 40$ V
  $|Y_{fs}| = 9.0$ mS TYP. ($V_{DS} = -10$ V, $I_D = -1.0$ mA, f = 1.0 kHz)
- High Input impedance
  $I_{GSS} \leqq 1.0$ nA ($V_{GS} = 20$ V, $V_{DS} = 0$)

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

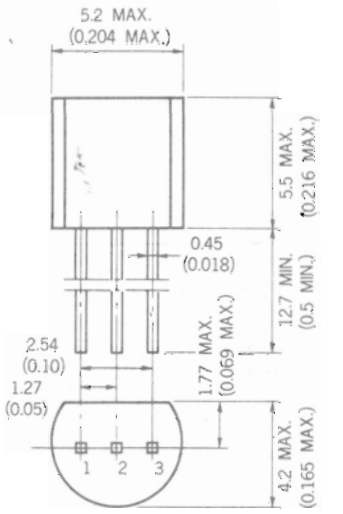
Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	40	V
V_{GSO}	Gate to Source Voltage	40	V
V_{DSX}*	Drain to Source Voltage	−40	V
I_D	Drain Current	−30	mA
I_G	Gate Current	−10	mA

* $V_{GS} = 2.0$ V

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	−1.0	−9.0	−18	mA	$V_{DS} = -10$ V, $V_{GS} = 0$
$\|Y_{fs}\|_1$	Forward Transfer Admittance	7.0	9.0		mS	$V_{DS} = -10$ V, $I_D = -1.0$ mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	7.0			mS	$V_{DS} = -10$ V, $V_{GS} = 0$, f = 1.0 kHz
C_{iss}	Input Capacitance		50		pF	$V_{DS} = -10$ V, $V_{GS} = 0$, f = 1.0 MHz
C_{rss}	Feedback Capacitance		10		pF	$V_{DS} = -10$ V, $V_{GS} = 0$, f = 1.0 MHz
NV	Noise Voltage			50	mV	See test circuit
I_{GSS}	Gate Cutoff Current			1.0	nA	$V_{GS} = 20$ V, $V_{DS} = 0$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	0.2		1.5	V	$V_{DS} = -10$ V, $I_D = -10$ μA

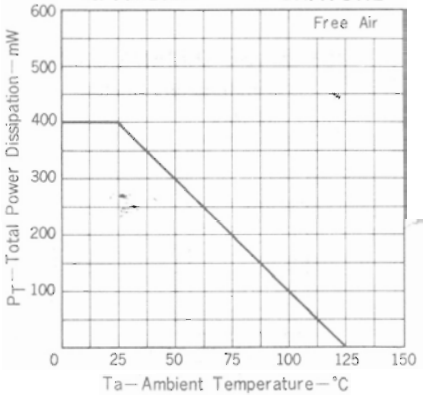
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	−1.0 — −6.0	−5.0 — −10	−9.0 — −14	−13 — −18

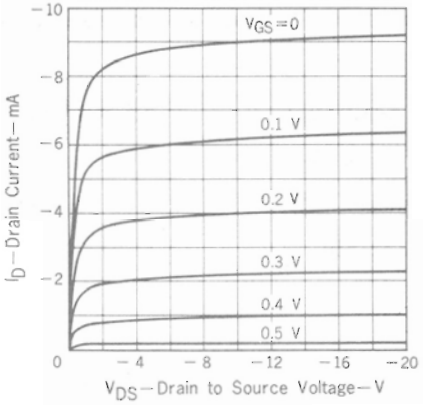
I_{DSS} Test Conditions : $V_{DS} = -10$ V, $V_{GS} = 0$

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

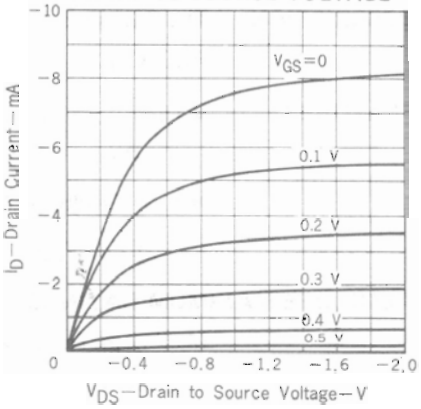
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



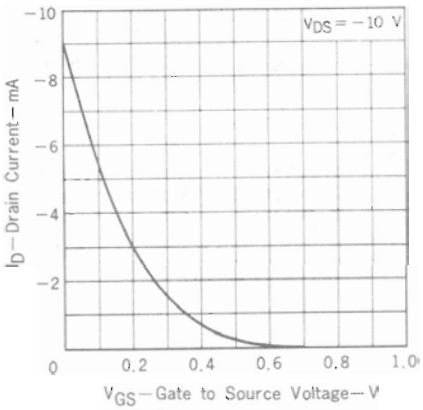
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



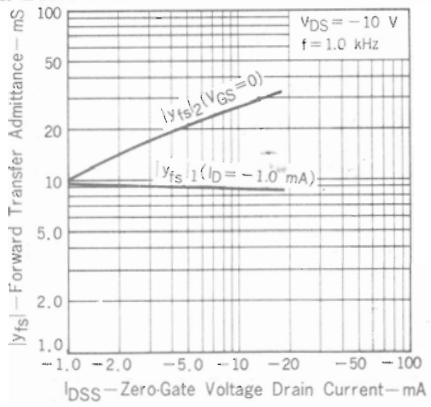
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



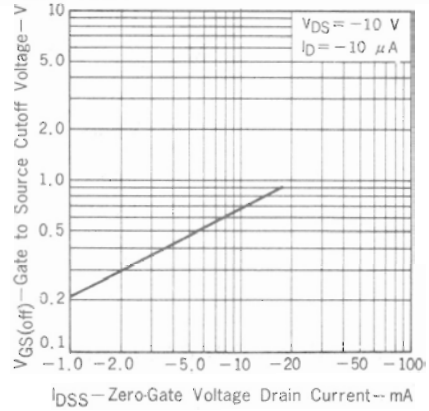
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



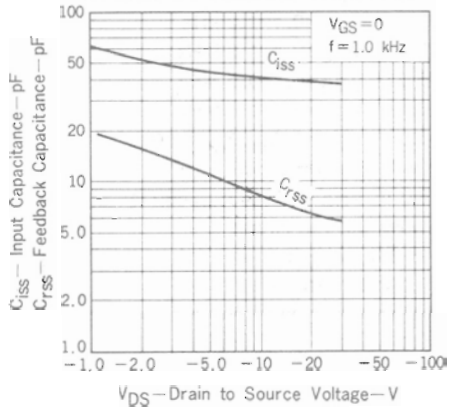
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



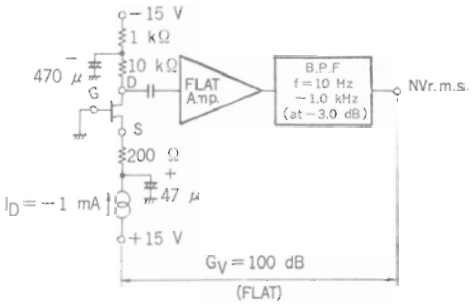
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE VOLTAGE TEST CIRCUIT



$V_{DS} \fallingdotseq -4$ V, $I_D = -1.0$ mA, $R_G = 0$, $G_V = 100$ dB,
f = 10 Hz – 1.0 kHz (at −3 dB)

NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK49

DESCRIPTION The 2SK49 is designed for use in FM tuner of a potable RADIO RECIVER.

FEATURES

- High Forward Transfer Admittance. : 5.5 mS TYP.
  $|Yfs|_2$ (V_{DS} = 5.0 V, V_{GS} = 0)
- Low Feedback Capacitance. : 0.07 pF TYP.
  C_{rss} (V_{DS} = 5.0 V, V_{GS} = 0)

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +80 °C Maximum

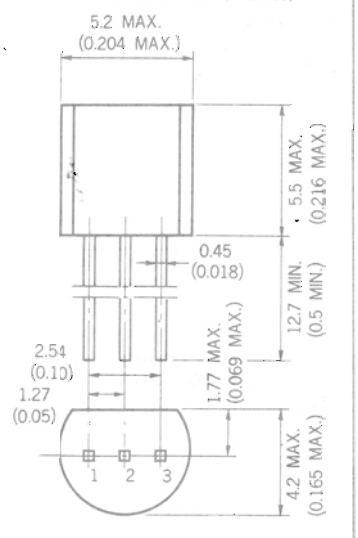
Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 72 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−20 V
V_{GSO}	Gate to Source Voltage	−1.0 V
V_{DSX}	Drain to Source Voltage	20 V
I_D	Drain Current	10 mA
I_G	Gate Current	10 mA

PACKAGE DIMENSIONS
in millimeters (inches)



1. GATE
2. SOURCE
3. DRAIN

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	2.0	6.0	mA	V_{DS}=5.0 V, V_{GS}=0
$\|Yfs\|_1$	Forward Transfer Admittance	1.9	2.8		mS	V_{DS}=5.0 V, I_D=0.5 mA, f=1.0 kHz
$\|Yfs\|_2$	Forward Transfer Admittance	1.9	5.5		mS	V_{DS}=5.0 V, V_{GS}=0, f=1.0 kHz
C_{iss}	Input Capacitance		5.0	6.5	pF	V_{DS}=5.0 V, V_{GS}=0, f=1.0 MHz
C_{rss}	Feedback Capacitance		0.07	0.25	pF	V_{DS}=5.0 V, V_{GS}=0, f=1.0 MHz
C_{oss}	Output Capacitance		3.8	4.5	pF	V_{DS}=5.0 V, V_{GS}=0, f=1.0 MHz
G_{ps}	Power Gain	9.0	18		dB	V_{DS}=5.0 V, V_{GS}=0, Z_{in}, Z_{out}=50 Ω f=100 MHz, See test circuit
NF	Noise Figure		3.5	6.0	dB	V_{DS}=5.0 V, V_{GS}=0, Z_{in}, Z_{out}=50 Ω f=100 MHz, See test circuit
I_{GSS}	Gate Cutoff Current			−50	nA	V_{GS}=−0.5 V, V_{DS}=0
$V_{GS(off)}$	Gate to Source Cutoff Voltage		−0.8	−2.5	V	V_{DS}=5.0 V, I_D=10 μA

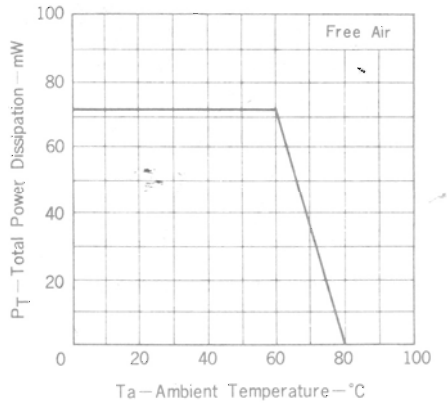
Classification of I_{DSS}

Rank	E	F	H
I_{DSS}(mA)	0.5 −1.5	1.0 − 3.0	2.0 − 6.0

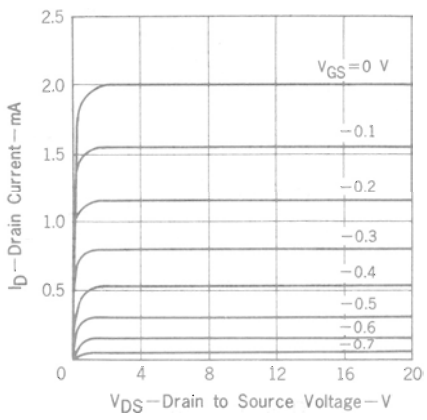
I_{DSS} Test Conditions : V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C unless otherwise noted)

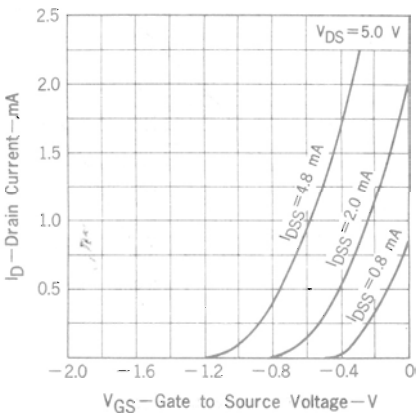
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



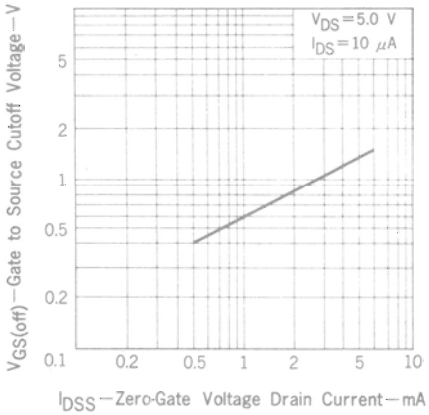
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



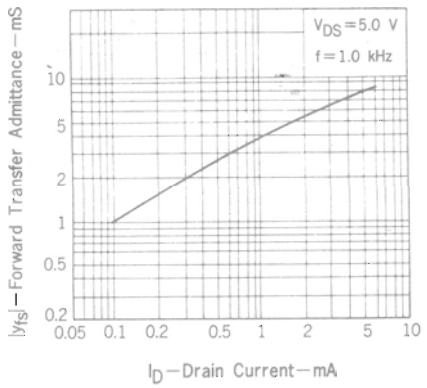
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



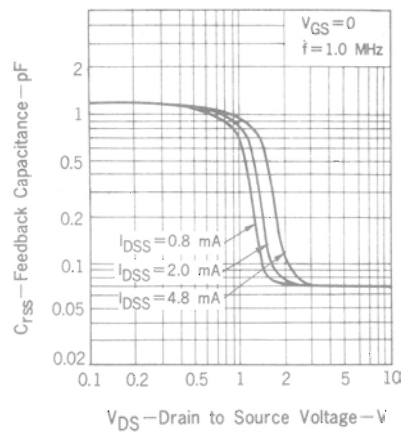
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



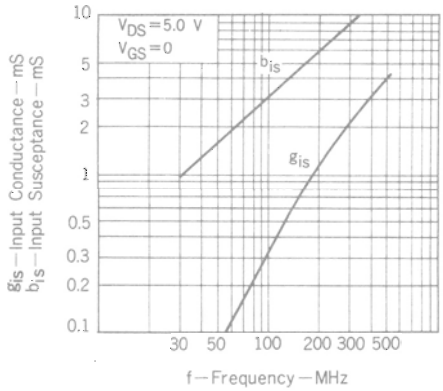
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



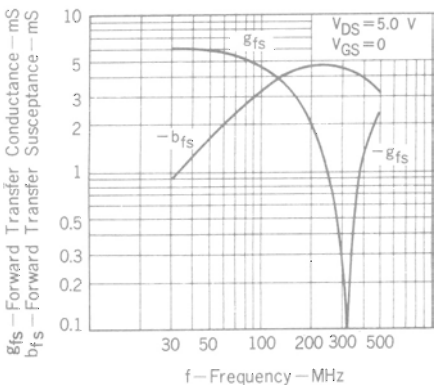
FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



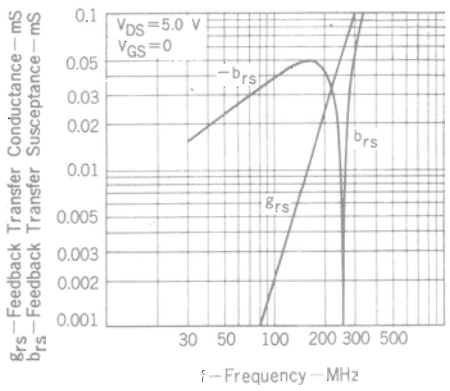
INPUT ADMITTANCE vs. FREQUENCY



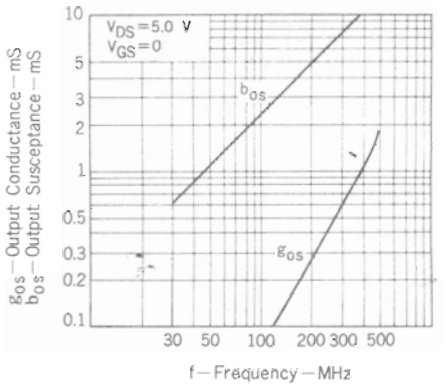
FORWARD TRANSFER ADMITTANCE vs. FREQUENCY



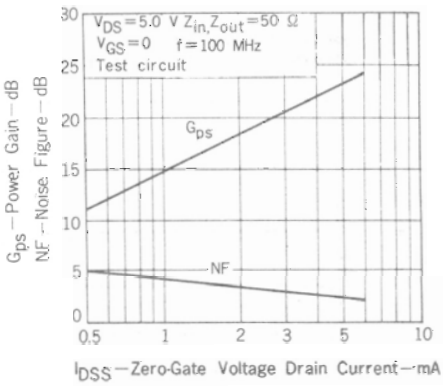
FEEDBACK TRANSFER ADMITTANCE vs. FREQUENCY



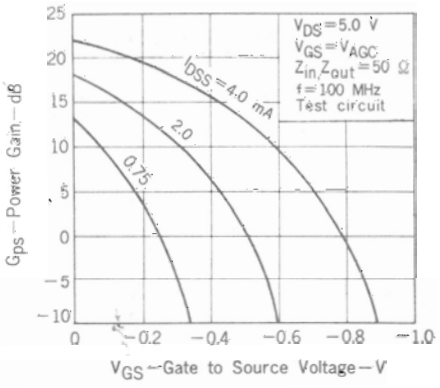
OUTPUT ADMITTANCE vs. FREQUENCY



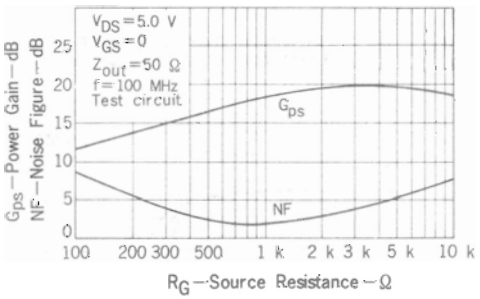
POWER GAIN AND NOISE FIGURE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



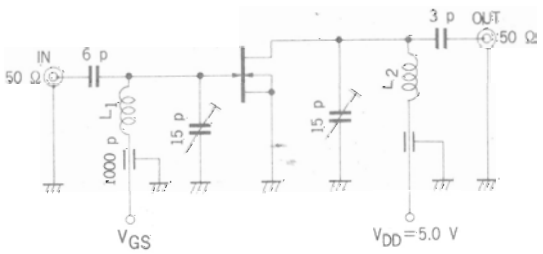
POWER GAIN vs. GATE TO SOURCE VOLTAGE



POWER GAIN AND NOISE FIGURE vs. SOURCE RESISTANCE



NOISE FIGURE and POWER GAIN TEST CIRCUIT (f = 100 MHz)



NEC
ELECTRON DEVICE

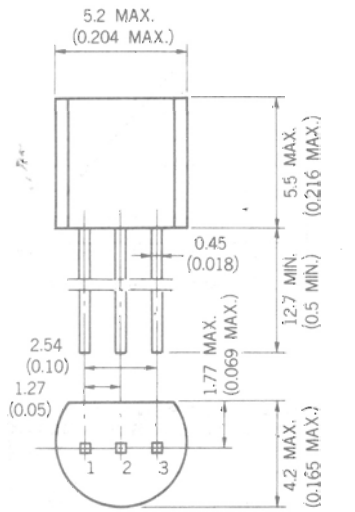
N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK68A

DESCRIPTION The 2SK68A is designed for use in driver stage of AF low noise amplifier.

FEATURES

- Low Noise Figure
  NF (V_{DS} = 10 V, V_{GS} = 0, R_G = 10 kΩ, f = 10 Hz) : 1.0 dB TYP.
- High Voltage, High $|y_{fs}|$, and Wide Dynamic Range
  V_{GDO} > −50 V, $|y_{fs}|$ (V_{DS} = 10 V, V_{GS} = 0) : 12 mS TYP.
- Low Leakage Current
  I_{GSS} < −1.0 nA (V_{GS} = −20 V)

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−50 V
V_{GSO}	Gate to Source Voltage	−50 V
V_{DSX}*	Drain to Source Voltage	50 V
I_D	Drain Current	20 mA
I_G	Gate Current	10 mA

*V_{GS} = −2.0 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	3.0	12	mA	V_{DS} = 10 V, V_{GS} = 0
$\|y_{fs}\|_1$	Forward Transfer Admittance	4.0	5.2		mS	V_{DS} = 10 V, I_D = 0.5 mA, f = 1.0 kHz
$\|y_{fs}\|_2$	Forward Transfer Admittance	4.0	12		mS	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		13		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
C_{rss}	Feedback Capacitance		2.6		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
NF_1	Noise Figure		5.0	10	dB	V_{DS} = 10 V, V_{GS} = 0, R_G = 1.0 kΩ, f = 10 Hz
NF_2	Noise Figure		1.0	3.0	dB	V_{DS} = 10 V, V_{GS} = 0, R_G = 1.0 kΩ, f = 100 Hz
NF_3	Noise Figure		0.6	1.5	dB	V_{DS} = 10 V, V_{GS} = 0, R_G = 1.0 kΩ, f = 1.0 kHz
NV	Noise Voltage		15	20	mV	See test circuit
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS} = −20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.13	−0.5	−1.5	V	V_{DS} = 10 V, I_D = 10 μA

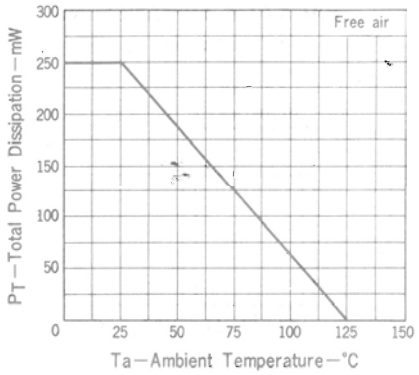
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	0.5 – 1.5	1.0 – 3.0	2.0 – 6.0	4.0 – 12

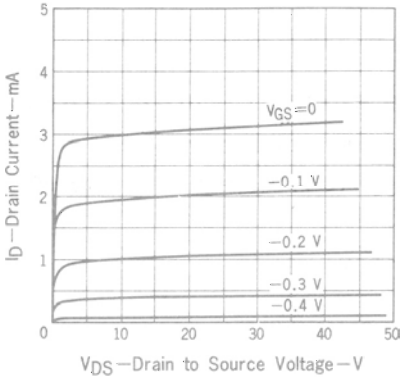
I_{DSS} Test Conditions : V_{DS} = 10 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

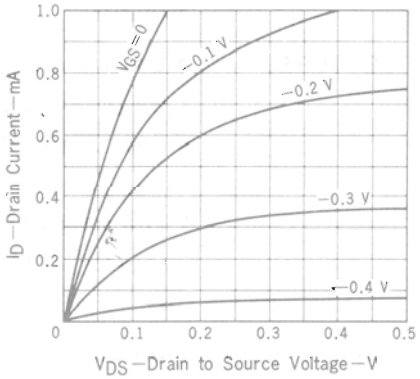
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



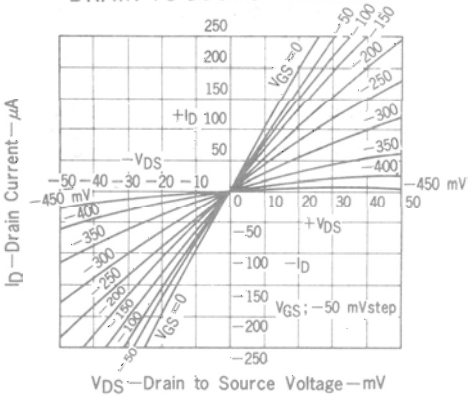
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



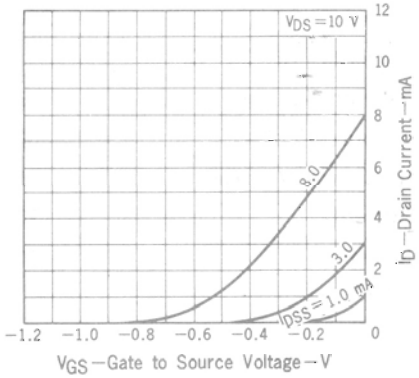
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



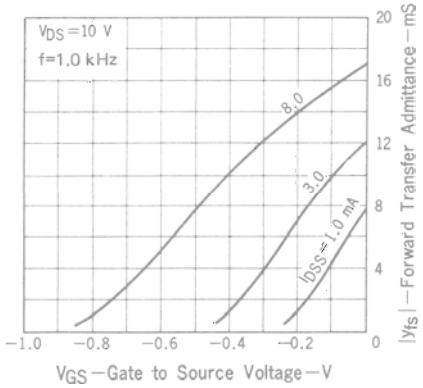
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



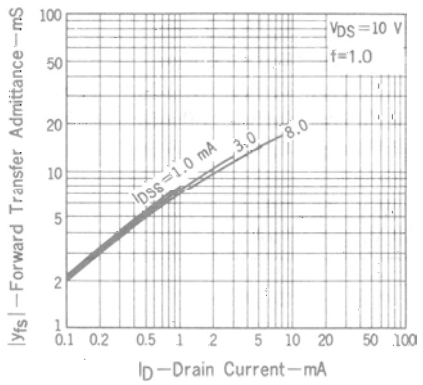
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



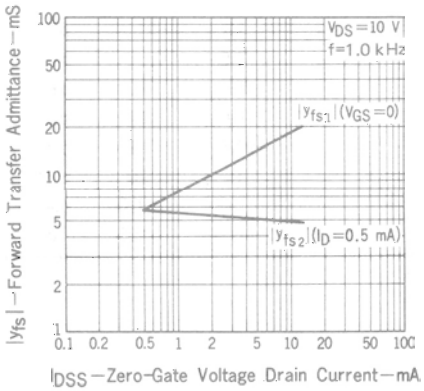
FORWARD TRANSFER ADMITTANCE vs. GATE TO SOURCE VOLTAGE



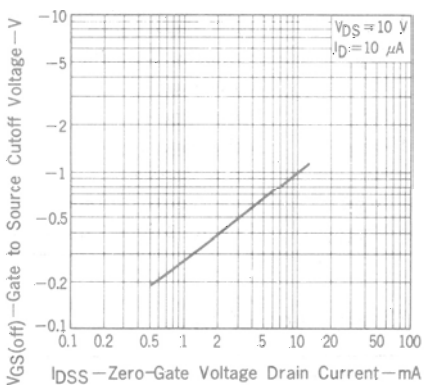
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



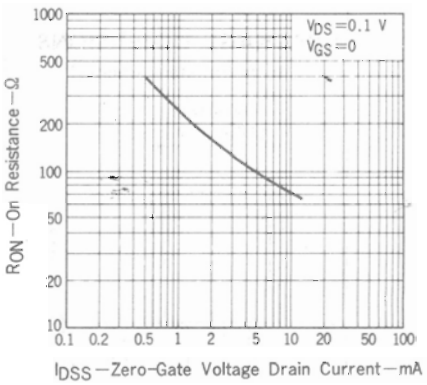
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



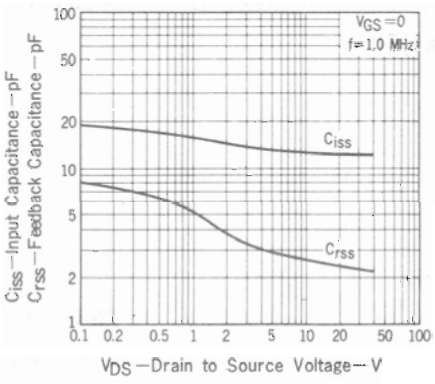
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



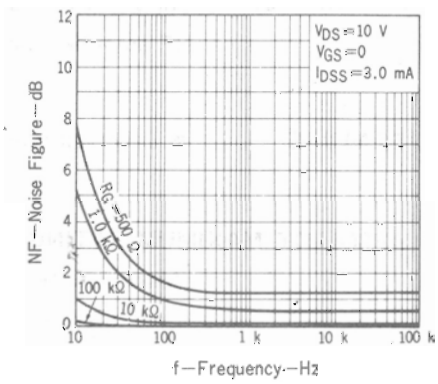
ON RESISTANCE
vs. ZERO-GATE VOLTAGE DRAIN CURRENT



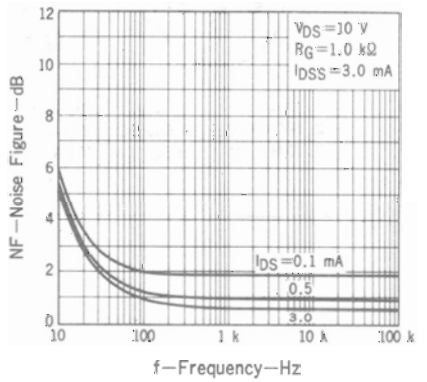
INPUT AND FEEDBACK CAPACITANCE
vs. DRAIN TO SOURCE VOLTAGE



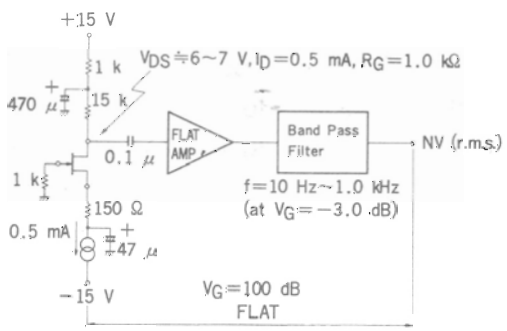
NOISE FIGURE vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



NOISE VOLTAGE TEST CIRCUIT



NEC
ELECTRON DEVICE

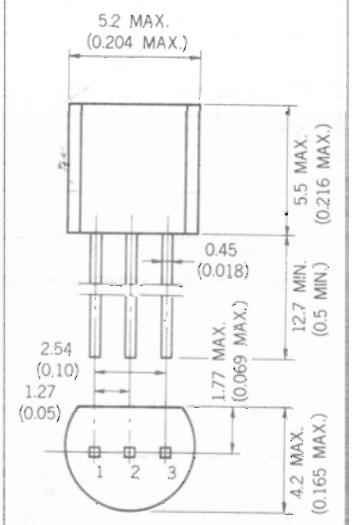
N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK104

DESCRIPTION The 2SK104 is designed for use in analog-switch, variable-resistor, RF amplifier and AF amplifier.

FEATURE

- Low Cost type FET

PACKAGE DIMENSIONS
in millimeters (inches)



1. GATE
2. SOURCE
3. DRAIN

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- Gate to Drain Voltage V_{GDO} . . . . . −30 V
- Gate to Source Voltage V_{GSO} . . . . . −30 V
- Drain to Source Voltage V_{DSX}* . . . . . 30 V
- Drain Current I_D . . . . . 20 mA
- Gate Current I_G . . . . . 10 mA

*V_{GS} = −5.0 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Cutoff Current			−10	nA	V_{GS} = −30 V, V_{DS} = 0
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	2.5	12	mA	V_{DS} = 5.0 V, V_{GS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.25	−1.1	−4.5	V	V_{DS} = 5.0 V, I_D = 10 μA
$\|Y_{fs}\|_1$	Forward Transfer Admittance	1.5	2.1		mS	V_{DS} = 5.0 V, I_D = 0.5 mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	1.5	4.1		mS	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz
Ciss	Input Capacitance		4.1	6.0	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
Crss	Feedback Capacitance		0.9	1.3	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz

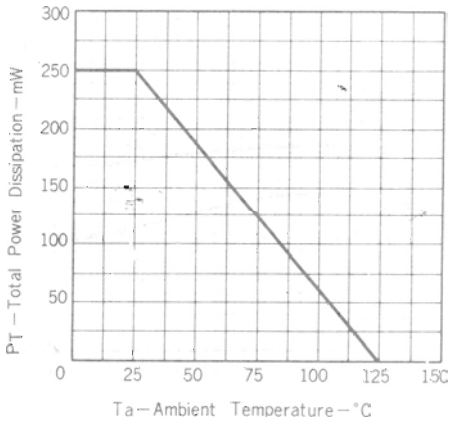
Classification of I_{DSS}

Rank	E	F	H	J
I_{DSS}(mA)	0.5 – 1.5	1.0 – 3.0	2.0 – 6.0	4.0 – 12

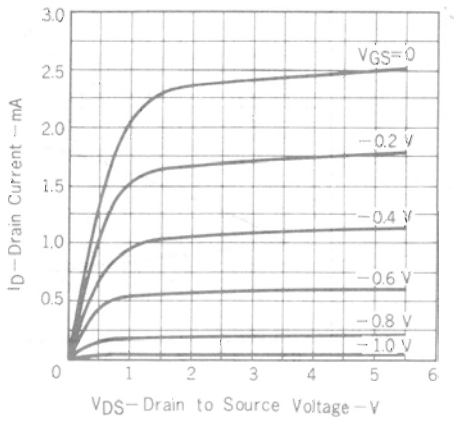
I_{DSS} Test Conditions : V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

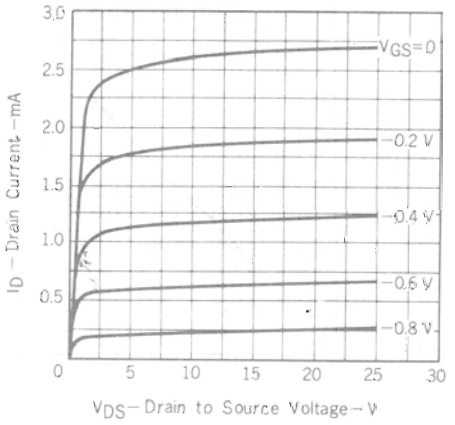
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



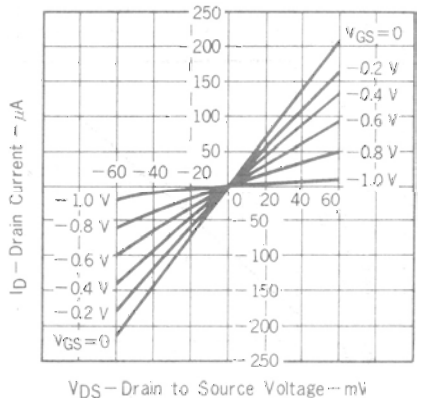
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



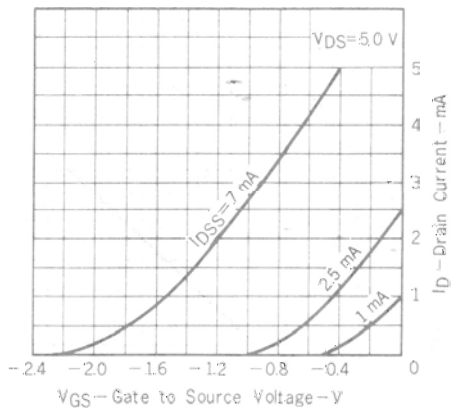
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



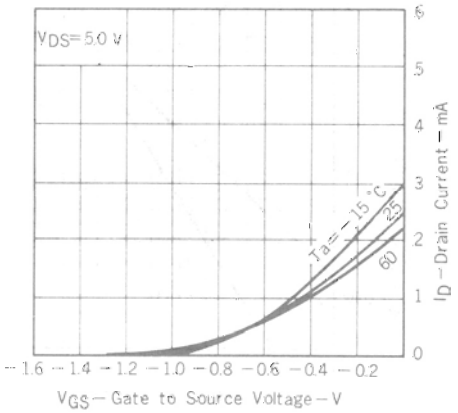
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



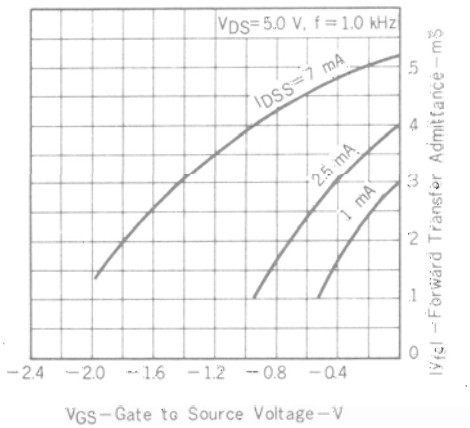
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



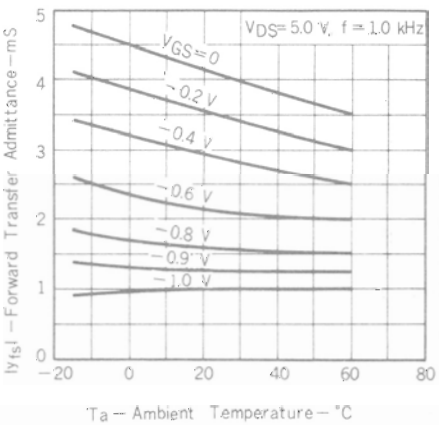
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



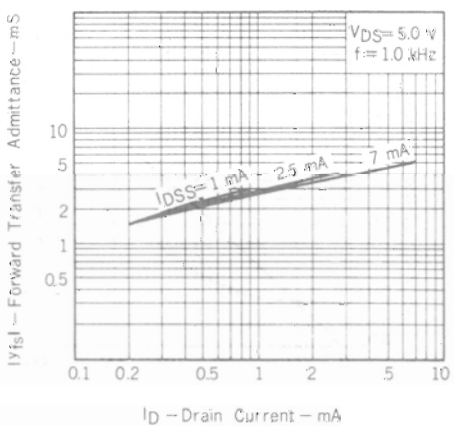
FORWARD TRANSFER ADMITTANCE vs. GATE TO SOURCE VOLTAGE



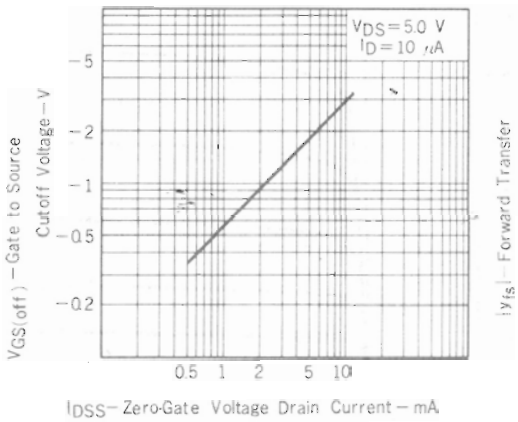
FORWARD TRANSFER ADMITTANCE vs. AMBIENT TEMPERATURE



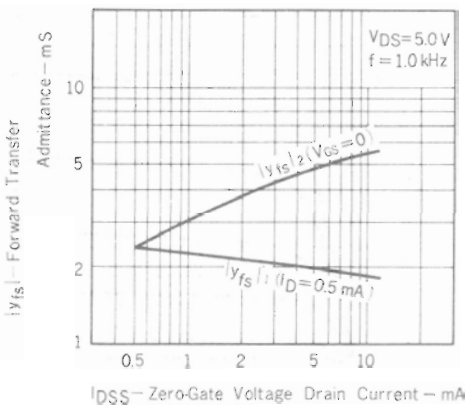
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



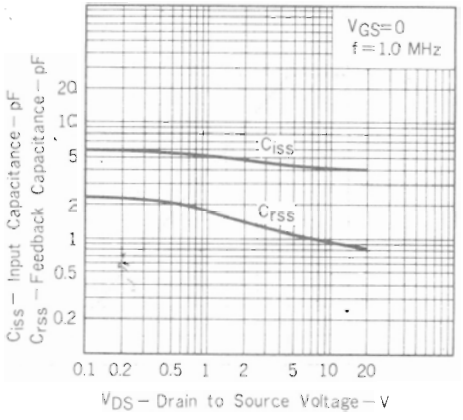
GATE TO SOURCE CUTOFF VOLTAGE
vs. ZERO-GATE VOLTAGE DRAIN CURRENT



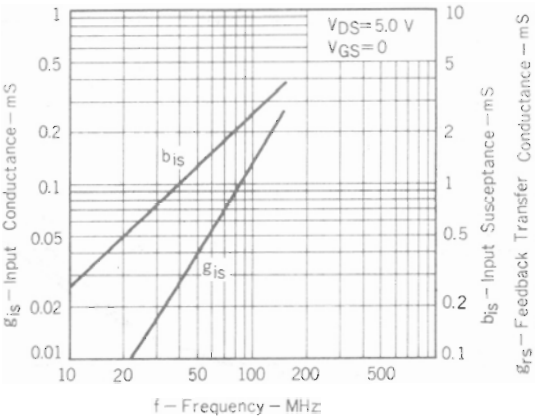
FORWARD TRANSFER ADMITTANCE
vs. ZERO-GATE VOLTAGE DRAIN CURRENT



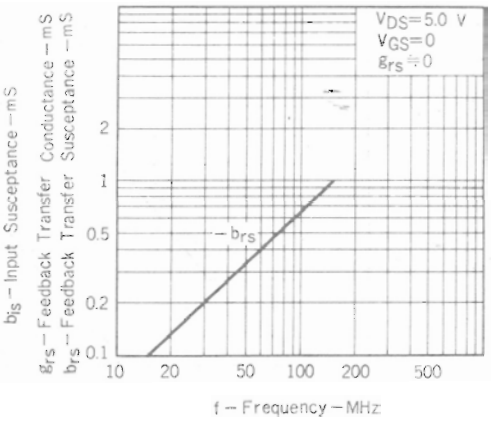
INPUT AND FEEDBACK CAPACITANCE
vs. DRAIN TO SOURCE VOLTAGE



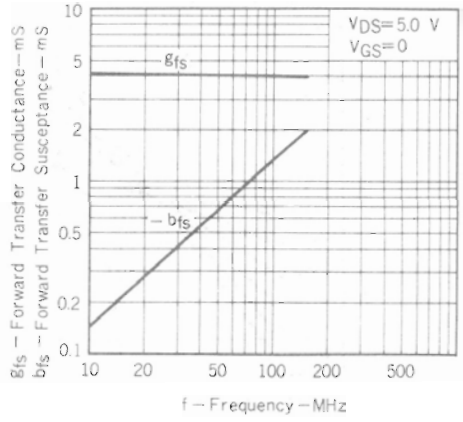
INPUT ADMITTANCE
vs. FREQUENCY



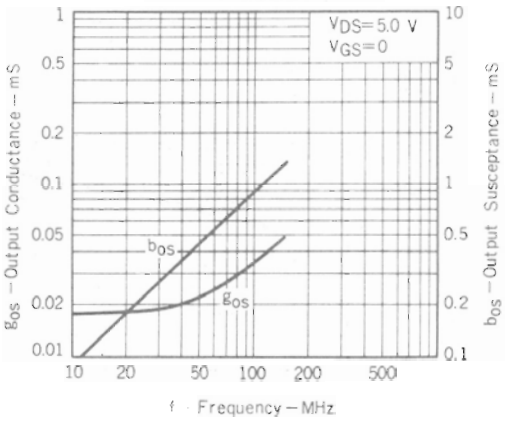
FEEDBACK TRANSFER ADMITTANCE
vs. FREQUENCY



FORWARD TRANSFER ADMITTANCE
vs. FREQUENCY



OUTPUT ADMITTANCE
vs. FREQUENCY



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

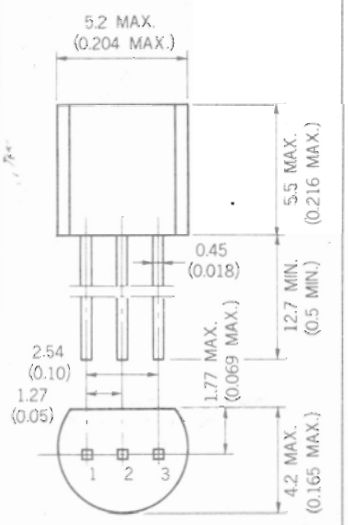
2SK105

DESCRIPTION The 2SK105 is designed for use in analog-switch, variable-resistor and AF amplifier.

FEATURES

- Low cost type FET.

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

- Gate to Drain Voltage V_{GDO} . . . . . −50 V
- Gate to Source Voltage V_{GSO} . . . . . −50 V
- Drain to Source Voltage V_{DSX}* . . . . . 50 V
- Drain Current I_D . . . . . 20 mA
- Gate Current I_G . . . . . 10 mA

*V_{GS} = −5.0 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS} = −30 V, V_{DS} = 0
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	2.5	12	mA	V_{DS} = 5.0 V, V_{GS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.25	−1.1	−4.5	V	V_{DS} = 5.0 V, I_D = 10 μA
$\lvert Y_{fs} \rvert_1$	Forward Transfer Admittance	1.5	2.1		mS	V_{DS} = 5.0 V, I_D = 0.5 mA, f = 1.0 kHz
$\lvert Y_{fs} \rvert_2$	Forward Transfer Admittance	1.5	4.1		mS	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz
Ciss	Input Capacitance		4.1	6.0	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
Crss	Feedback Capacitance		0.9	1.3	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz

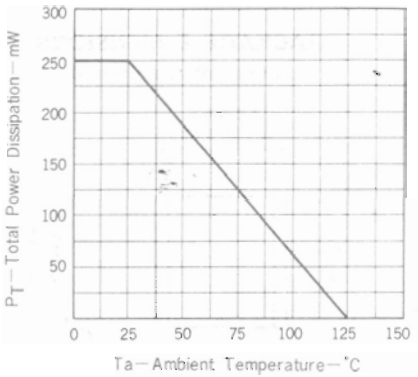
Classification of I_{DSS}

Rank	E	F	H	J
I_{DSS}(mA)	0.5 – 1.5	1.0 – 3.0	2.0 – 6.0	4.0 – 12

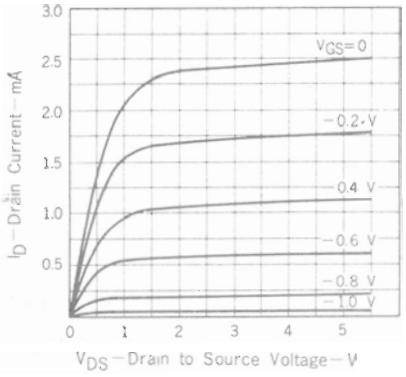
I_{DSS} Test Conditions : V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

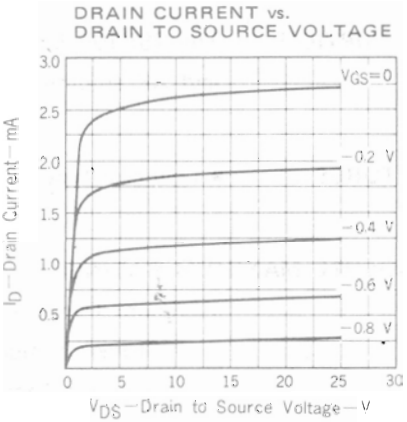
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



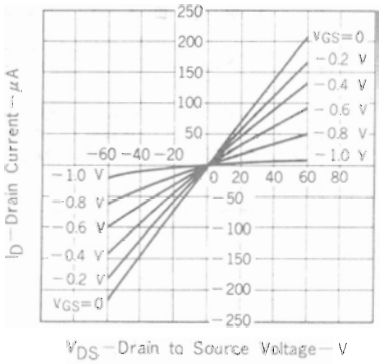
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



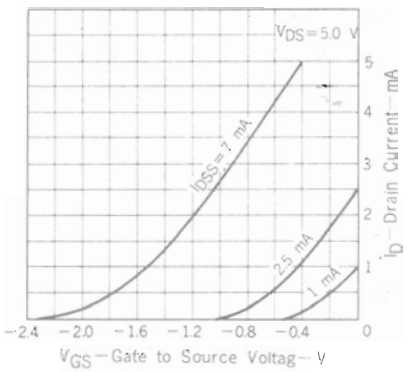
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



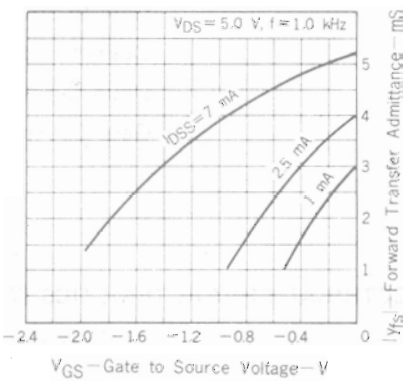
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



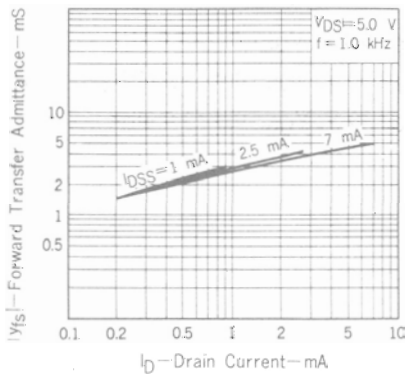
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



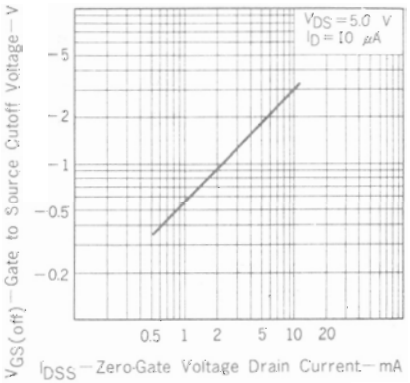
FORWARD TRANSFER ADMITTANCE vs. GATE TO SOURCE VOLTAGE



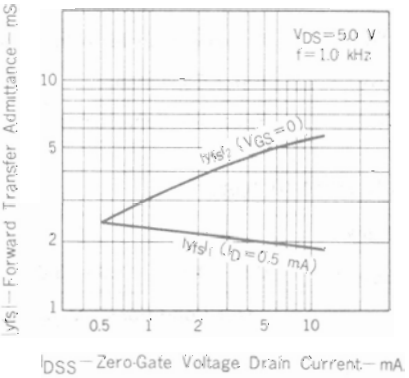
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



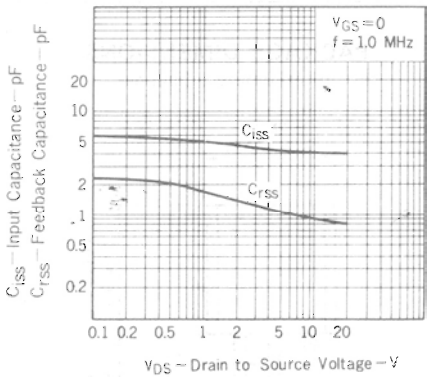
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



INPUT AND FEEDBACK CAPACITANCE
vs. DRAIN TO SOURCE VOLTAGE



NEC
ELECTRON DEVICE

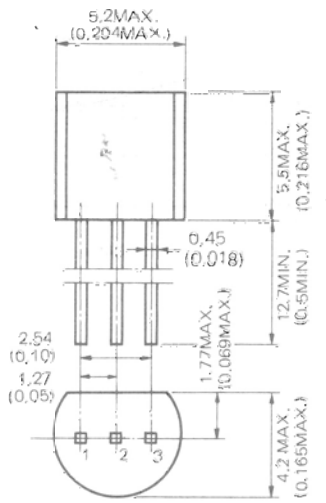
N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK162

DESCRIPTION The 2SK162 is designed for use in the first stage for Low Noise Amplifier.

FEATURES

- High $|Y_{fs}|$
  $|Y_{fs}| = 45$ mS TYP. @ $V_{DS} = 5.0$ V, $I_D = 5.0$ mA, $f = 1.0$ kHz
- Low Noise
  $e_n = 0.65\ nV/\sqrt{Hz}$ @ $V_{DS} = 5.0$ V, $I_D = 5.0$ mA, $f = 1.0$ kHz

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−40	V
V_{GSO}	Gate to Source Voltage	−40	V
V_{DSX}*	Drain to Source Voltage	40	V
I_D	Drain Current	50	mA
I_G	Gate Current	10	mA

*$V_{GS} = -2.0$ V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	5.0	18	30	mA	V_{DS}=5.0 V, V_{GS}=0
NF	Noise Figure		1.1	2.5	dB	V_{DS}=5.0 V, I_D=5.0 mA, R_G=100 Ω, f=100 Hz
$\|Y_{fs}\|_1$	Forward Transfer Admittance	40	45		mS	V_{DS}=5.0 V, I_D=5.0 mA, f=1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	40			mS	V_{DS}=5.0 V, V_{GS}=0, f=1.0 kHz
NV	Noise Voltage			35	mV	See Test Circuit
C_{iss}	Input Capacitance		55		pF	V_{DS}=10 V, V_{GS}=0, f=1.0 MHz
C_{rss}	Feedback Capacitance		10		pF	V_{DS}=10 V, V_{GS}=0, f=1.0 MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS}=−20 V, V_{DS}=0
$V_{GS(off)}$	Gate to Source Cutoff Voltage			−1.2	V	V_{DS}=5.0 V, I_D=1.0 μA

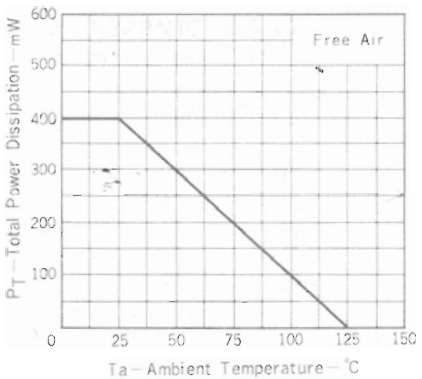
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	5.0 – 12	11 – 18	17 – 24	23 – 30

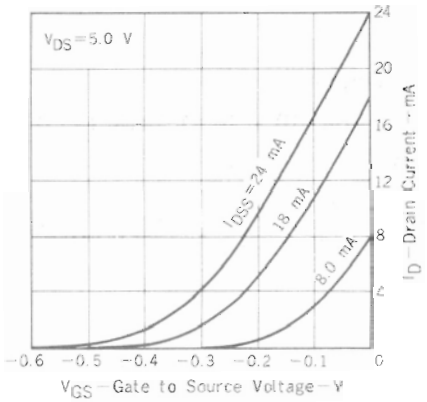
I_{DSS} Test Conditions: V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

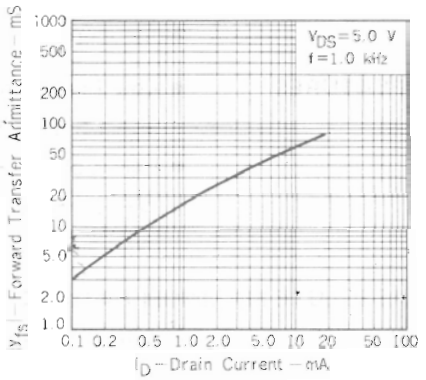
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



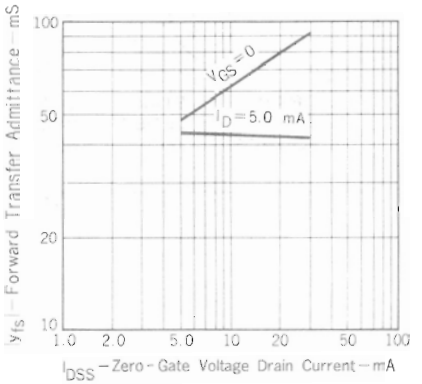
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



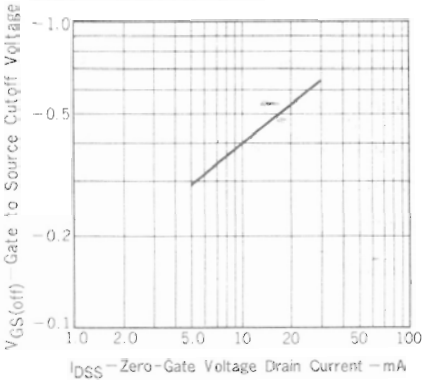
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



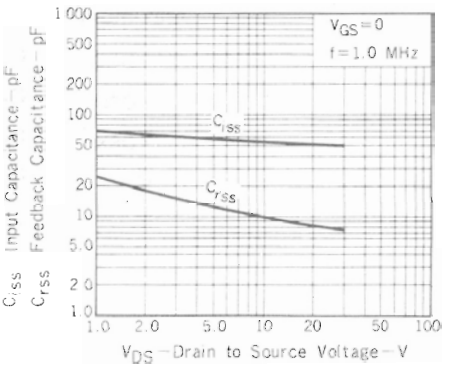
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



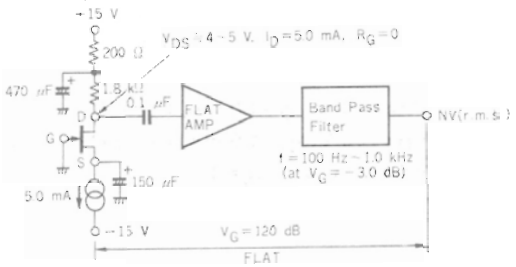
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE VOLTAGE TEST CIRCUIT



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

2SK163

DESCRIPTION The 2SK163 is designed for use in the first stage for AF Low Noise amplifier.

FEATURES

- Low Equivalent Noise Voltage.
  $e_n = 1.3\ nV/\sqrt{Hz}$ TYP. ($V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz)
- High Voltage and High $|Y_{fs}|$
  $V_{DSX} > 50$ V ($V_{GS} = -2.0$ V)
  $|Y_{fs}| > 7.0$ mS ($V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz)

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

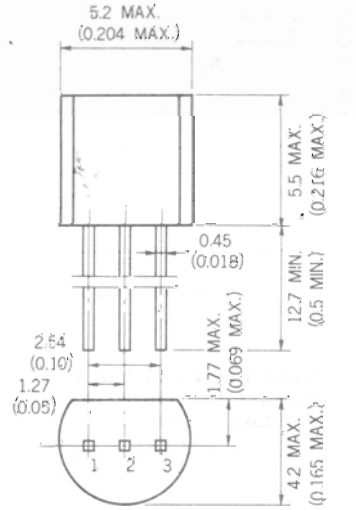
Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−50	V
V_{GSO}	Gate to Source Voltage	−50	V
V_{DSX} *	Drain to Source Voltage	50	V
I_D	Drain Current	30	mA
I_G	Gate Current	10	mA

* $V_{GS} = -2.0$ V

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	1.0	8.0	18	mA	$V_{DS} = 10$ V, $V_{GS} = 0$
e_n	Equivalent Noise Voltage		1.3		$nV/\sqrt{Hz}$	$V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz
$\|Y_{fs}\|_1$	Forward Transfer Admittance	7.0	9.0		mS	$V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	7.0			mS	$V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz
NV	Noise Voltage			20	mV	See test circuit
C_{iss}	Input Capacitance		15		pF	$V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ MHz
C_{rss}	Feedback Capacitance		6.0		pF	$V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	$V_{GS} = -20$ V, $V_{DS} = 0$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.2		−1.2	V	$V_{DS} = 10$ V, $I_D = 10$ μA

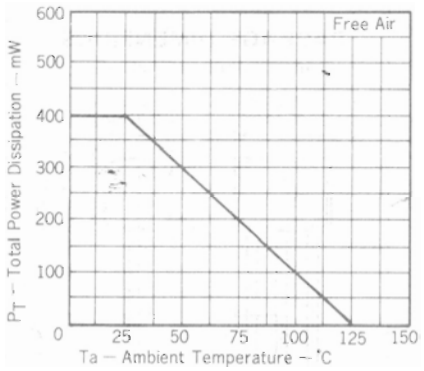
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	1.0 – 6.0	5.0 – 10	9.0 – 14	13 – 18

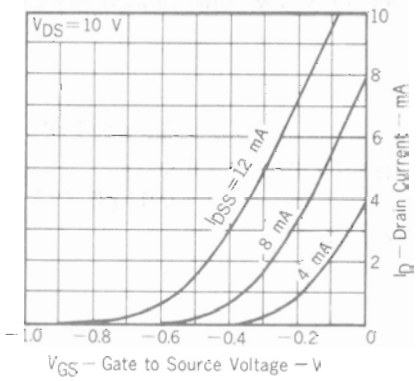
I_{DSS} Test Conditions: $V_{DS} = 10$ V, $V_{GS} = 0$

TYPICAL CHARACTERISTICS (Ta = 25 °C)

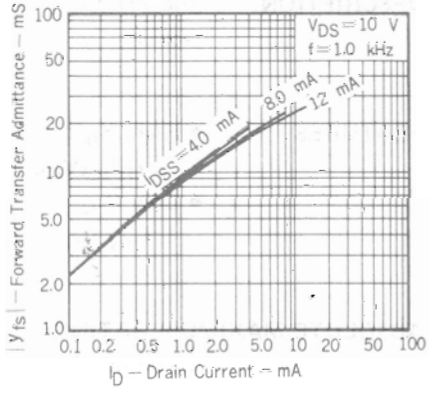
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



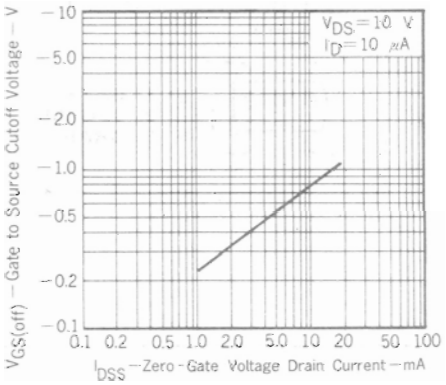
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



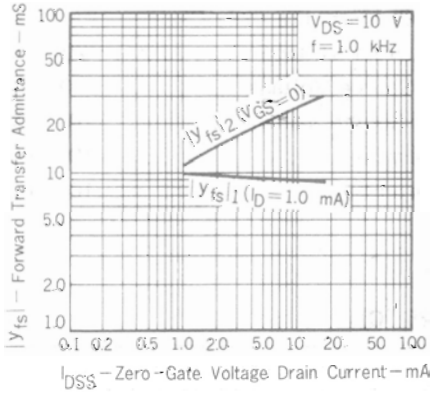
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



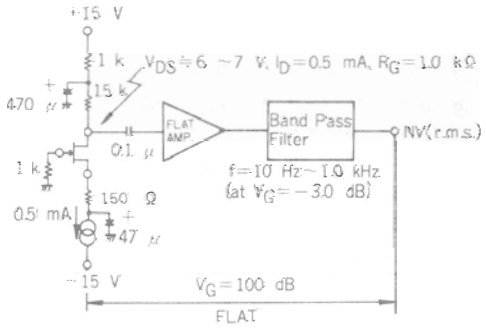
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



NOISE VOLTAGE TEST CIRCUIT



NEC
ELECTRON DEVICE

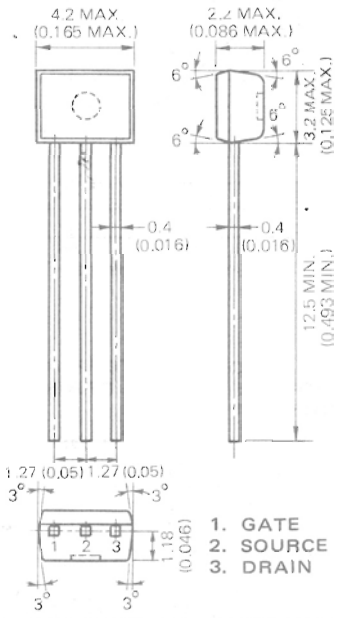
N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK193

DESCRIPTION The 2SK193 is designed for use in FM tuner of a potable radio receiver.

FEATURES

- High $|Y_{fs}|_1$: 3.5 mS TYP.
  $|Y_{fs}|_1$ (V_{DS} = 5.0 V, I_D = 0.5 mA, f = 1.0 kHz)
- Low C_{rss} : 0.07 pF TYP.
  C_{rss} (V_{DS} = 5.0 V, V_{GS} = 0)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−20	V
V_{GSO}	Gate to Source Voltage	−1.0	V
V_{DSX}*	Drain to Source Voltage	20	V
I_D	Drain Current	10	mA
I_G	Gate Current	10	mA

* V_{GS} = −2.5 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	2.5	8.0	mA	V_{DS} = 5.0 V, V_{GS} = 0
$\|Y_{fs}\|_1$	Forward Transfer Admittance	2.3	3.5		mS	V_{DS} = 5.0 V, I_D = 0.5 mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	2.3	8.5		mS	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		5.0	6.5	pF	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 MHz
C_{rss}	Feedback Capacitance		0.07	0.25	pF	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 MHz
C_{oss}	Output Capacitance		4.5	6.0	pF	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 MHz
G_{ps}	Power Gain	13	21		dB	V_{DS} = 5.0 V, V_{GS} = 0, Z_{in}, Z_{out} = 50 Ω f = 100 MHz, See test circuit
NF	Noise Figure		3.0	6.0	dB	V_{DS} = 5.0 V, V_{GS} = 0, Z_{in}, Z_{out} = 50 Ω f = 100 MHz, See test circuit
I_{GSS}	Gate Cutoff Current			−100	nA	V_{GS} = −0.5 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage			−2.5	V	V_{DS} = 5.0 V, I_D = 10 μA

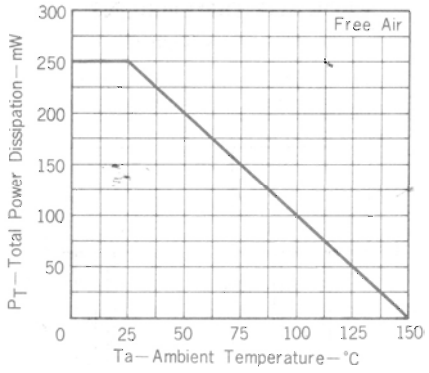
Classification of I_{DSS}

Rank	UF	EF	FF	PF	KF	LF	MF
I_{DSS}(mA)	0.5 – 1.0	0.75 – 1.5	1.0 – 2.0	1.5 – 3.0	2.0 – 4.0	3.0 – 6.0	4.0 – 8.0

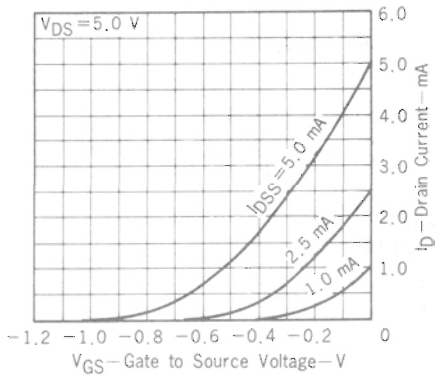
I_{DSS} Test Conditions: V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

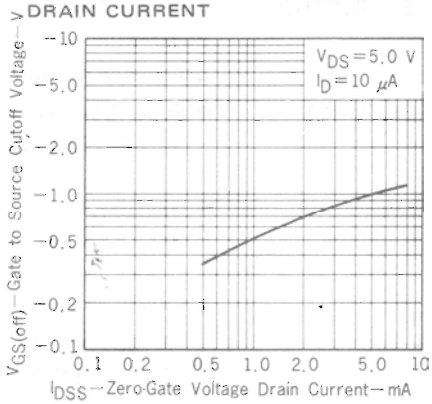
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



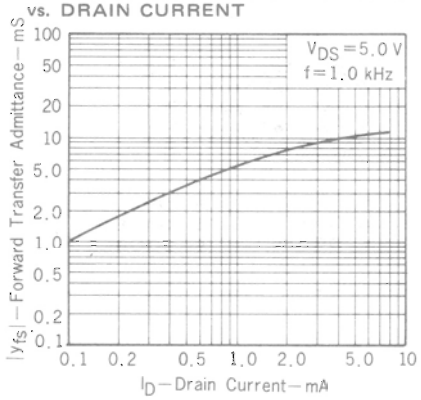
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



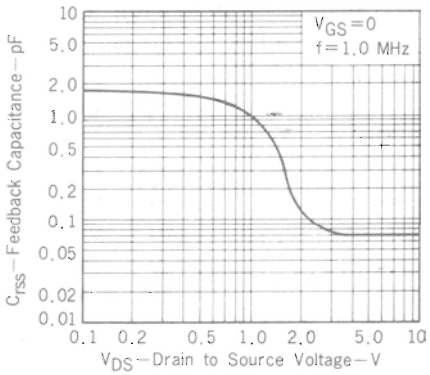
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



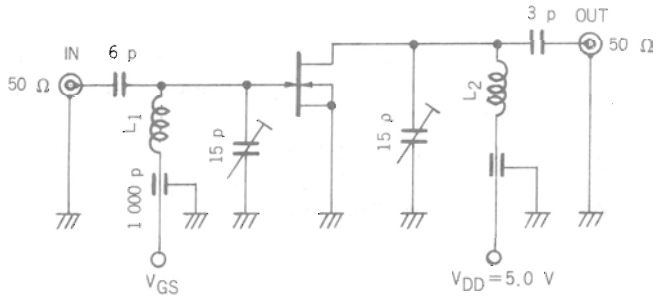
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE FIGURE and POWER GAIN TEST CIRCUIT (f = 100 MHz)



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

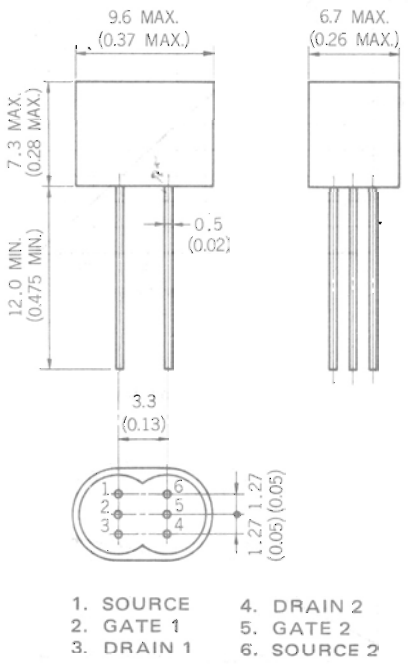
2SK194

DESCRIPTION The 2SK194 is designed for use in the first stage for differential amplifier.
Especially recommended Hi-Fi STEREO SETS.

FEATURES

- Super-Low Noise
  $e_n = 0.65\ nV/\sqrt{Hz}$ TYP. @ $V_{DS} = 5.0$ V, $I_D = 5.0$ mA, f = 1.0 kHz
- High $|Y_{fs}|$
  $|Y_{fs}| = 45$ mS @ $V_{DS} = 5.0$ V, $I_D = 5.0$ mA, f = 1.0 kHz
- Excellent pair balance
  $\Delta V_{GS} = 20$ mV MAX.
  $|Y_{fs}|$ Ratio = 0.95 MAX.
  @ $V_{DS} = 5.0$ V, $I_D = 5.0$ mA

PACKAGE DIMENSIONS
in millimeters (inches)



1. SOURCE
2. GATE 1
3. DRAIN 1
4. DRAIN 2
5. GATE 2
6. SOURCE 2

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation . . . . . 400 mW/Unit

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−40	V
V_{GSO}	Gate to Source Voltage	−40	V
V_{DSX}*	Drain to Source Voltage	40	V
I_D	Drain Current	50	mA
I_G	Gate Current	10	mA

*$V_{GS} = -3.0$ V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	5.0		24	mA	$V_{DS} = 5.0$ V, $V_{GS} = 0$
$\frac{I_{DSS(S)}}{I_{DSS(L)}}$	Zero-Gate Voltage Drain Current Ratio	0.9		1.0		$V_{DS} = 5.0$ V, $V_{GS} = 0$ $I_{DSS(S)}/I_{DSS(L)}$*
$\lvert Y_{fs}\rvert$	Forward Transfer Admittance	40	45		mS	$V_{DS} = 5.0$ V, $I_D = 5.0$ mA, f = 1.0 kHz
$\frac{\lvert Y_{fs}\rvert_{(S)}}{\lvert Y_{fs}\rvert_{(L)}}$	Forward Transfer Admittance Ratio	0.95		1.0		$V_{DS} = 5.0$ V, $I_D = 5.0$ mA, f = 1.0 kHz $\lvert Y_{fs}\rvert_{(S)}/\lvert Y_{fs}\rvert_{(L)}$*
ΔV_{GS}	Gate to Source Voltage Difference		3.0	20	mV	$V_{DS} = 5.0$ V, $I_D = 5.0$ mA $\Delta V_{GS} = V_{GS(L)} - V_{GS(S)}$*
NV	Noise Voltage		25	35	mV	See Test Circuit
C_{iss}	Input Capacitance		55		pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz
C_{rss}	Feedback Capacitance		10		pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz
$V_{GS(off)}$	Gate to Source Cutoff Voltage			−1.2	V	$V_{DS} = 5.0$ V, $I_D = 10\ \mu A$
I_{GSS}	Gate Cutoff Current			−1.0	nA	$V_{GS} = -20$ V, $V_{DS} = 0$

*(S) : The Smaller Value, (L) : The Larger of pair

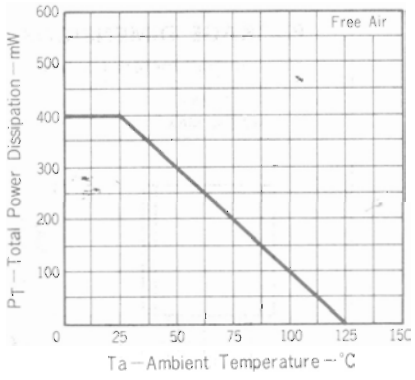
Classification of I_{DSS}

Rank	K	L	M
I_{DSS}(mA)	5.0 – 12	11 – 18	17 – 24

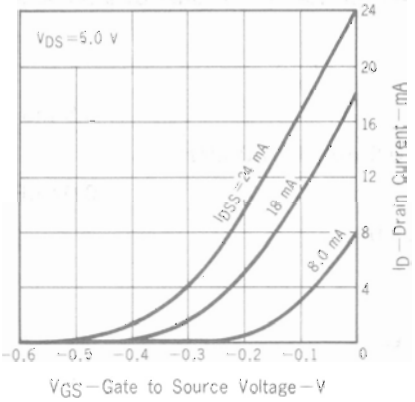
I_{DSS} Test Conditions : $V_{DS} = 5.0$ V, $V_{GS} = 0$

TYPICAL CHARACTERISTICS (Ta = 25 °C)

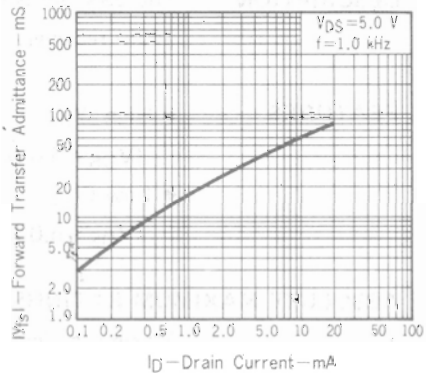
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



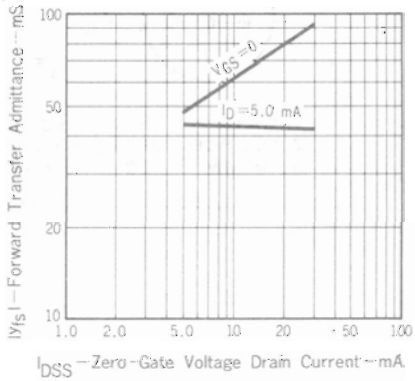
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



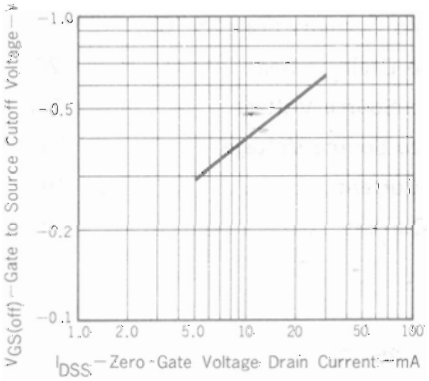
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



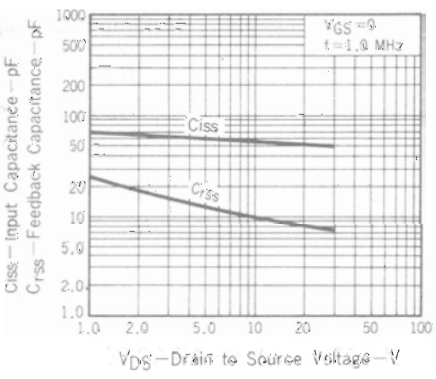
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



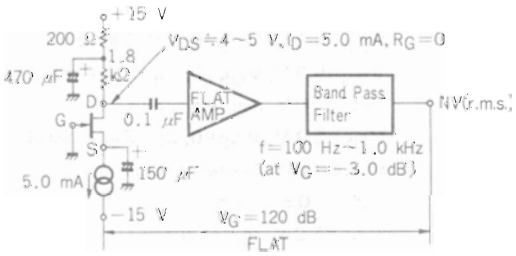
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE VOLTAGE TEST CIRCUIT



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

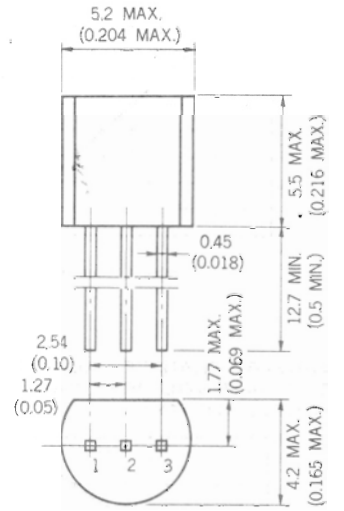
2SK195

DESCRIPTION The 2SK195 is designed for use in FM tuner of a potable radio receiver.

FEATURES

- High $|Y_{fs}|_1$: 3.5 mS TYP.
  (V_{DS} = 5.0 V, I_D = 0.5 mA, f = 1.0 kHz)
- Low C_{rss} : 0.07 pF TYP.
  (V_{DS} = 5.0 V, V_{GS} = 0)

PACKAGE DIMENSIONS
in millimeters (inches)



1. GATE
2. SOURCE
3. DRAIN

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−20	V
V_{GSO}	Gate to Source Voltage	−1.0	V
V_{DSX}	Drain to Source Voltage	20	V
I_D	Drain Current	10	mA
I_G	Gate Current	10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	2.5	8.0	mA	V_{DS}=5.0 V, V_{GS}=0
$\|Y_{fs}\|_1$	Forward Transfer Admittance	2.3	3.5		mS	V_{DS}=5.0 V, I_D=0.5 mA, f=1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	2.3			mS	V_{DS}=5.0 V, V_{GS}=0, f=1.0 kHz
C_{iss}	Input Capacitance		5.0	6.5	pF	V_{DS}=5.0 V, V_{GS}=0, f=1.0 MHz
C_{rss}	Feedback Capacitance		0.07	0.25	pF	V_{DS}=5.0 V, V_{GS}=0, f=1.0 MHz
C_{oss}	Output Capacitance		4.5	6.0	pF	V_{DS}=5.0 V, V_{GS}=0, f=1.0 MHz
G_{ps}	Power Gain	13	21		dB	V_{DS}=5.0 V, V_{GS}=0, Z_{in}, Z_{out}=50 Ω f=100 MHz, See test circuit
NF	Noise Figure		3.0	6.0	dB	V_{DS}=5.0 V, V_{GS}=0, Z_{in}, Z_{out}=50 Ω f=100 MHz, See test circuit
I_{GSS}	Gate Cutoff Current			−100	nA	V_{GS}=−0.5 V, V_{DS}=0
$V_{GS(off)}$	Gate to Source Cutoff Voltage			−2.5	V	V_{DS}=5.0 V, I_D=10 μA

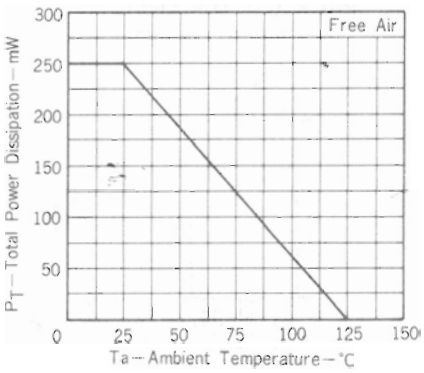
Classification of I_{DSS}

Rank	E	F	H	J
I_{DSS}(mA)	0.5 – 1.5	1.0 – 3.0	2.0 – 6.0	4.0 – 8.0

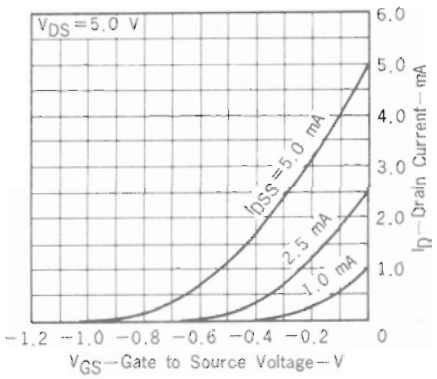
I_{DSS} Test Conditions: V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

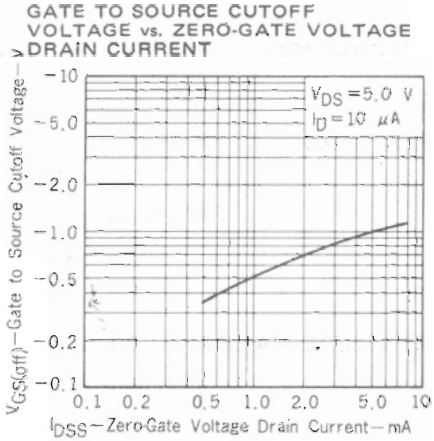
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



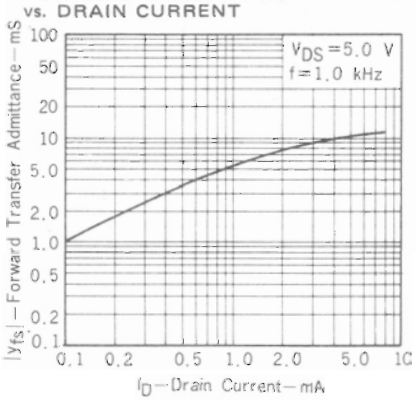
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



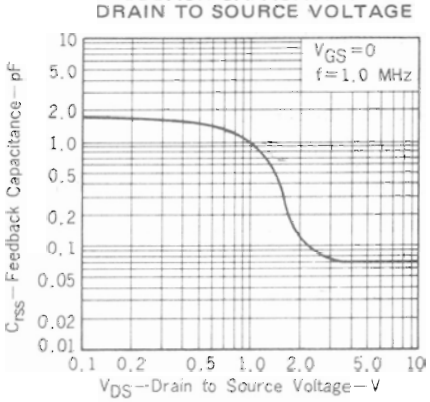
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



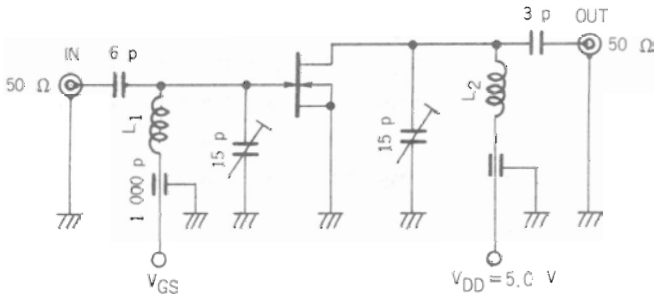
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE FIGURE and POWER GAIN TEST CIRCUIT (f = 100 MHz)



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

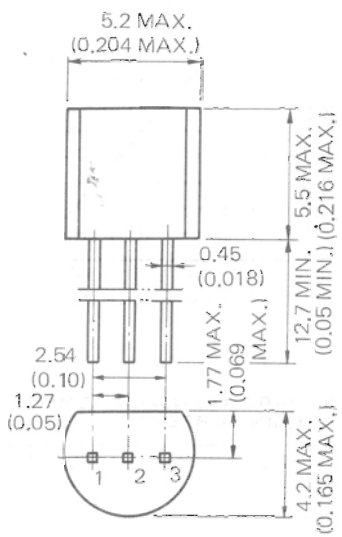
2SK505

DESCRIPTION The 2SK505 is designed for use in VIDEO stage Low Noise amplifier.

FEATURES

- High $|Y_{fs}|$
  $|Y_{fs}|$ = 26 mS TYP. (V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz)
- Low C_{iss}
  C_{iss} = 4.8 pF TYP. (V_{DS} = 5.0 V, I_D = 10 mA, f = 1.0 MHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN EIAJ : SC-43B
2. SOURCE JEDEC : TO-92
3. GATE IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −65 to 150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation ..... 400 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{GDO} Gate to Drain Voltage ..... −15 V
- V_{GSO} Gate to Source Voltage ..... −15 V
- V_{DXS}* Drain to Source Voltage ..... 15 V
- I_D Drain Current ..... 50 mA
- I_G Gate Current ..... 5 mA

* V_{GS} = −4.0 V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Current	10	20	40	mA	V_{DS} = 5.0 V, V_{GS} = 0
$\|Y_{fs}\|_1$	Forward Transfer Admittance	14	19		mS	V_{DS} = 5.0 V, I_D = 10 mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	14	26		mS	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		4.8		pF	V_{DS} = 5.0 V, I_D = 10 mA, f = 1.0 MHz
C_{rss}	Feedback Capacitance		1.6		pF	V_{DS} = 5.0 V, I_D = 10 mA, f = 1.0 MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS} = −10 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.6	−1.4	−3.0	V	V_{DS} = 5.0 V, I_D = 10 μA

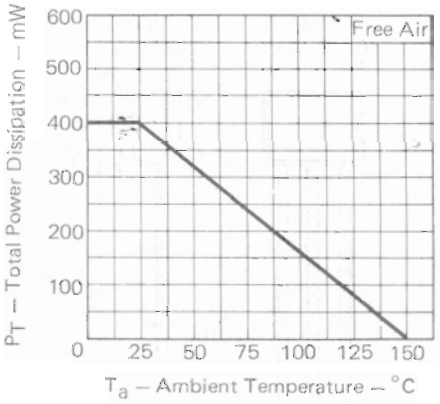
Classification of I_{DSS}

Rank	E	F	H
I_{DSS}(mA)	10 − 20	15 − 30	25 − 40

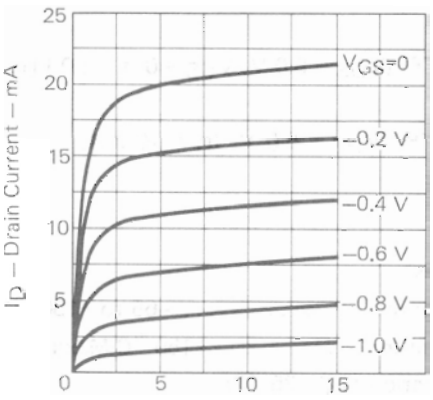
I_{DSS} Test Conditions : V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

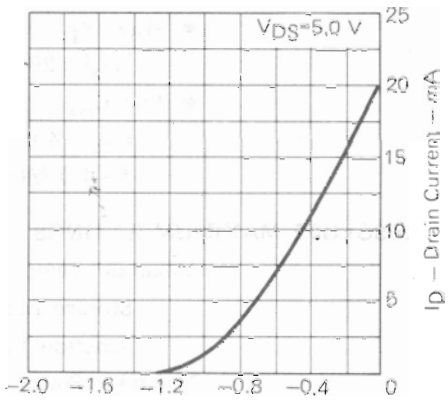
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



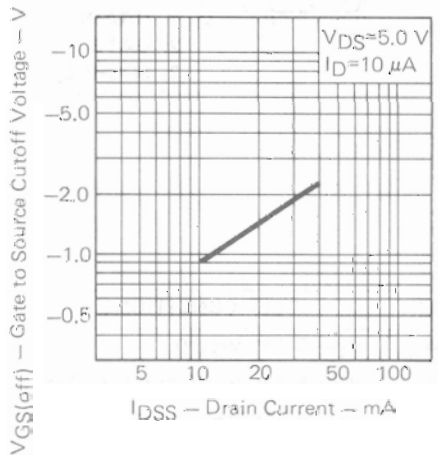
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



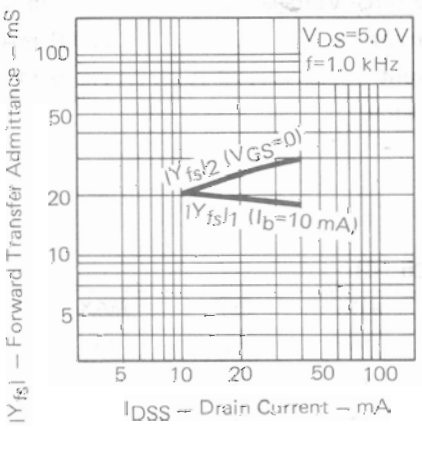
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



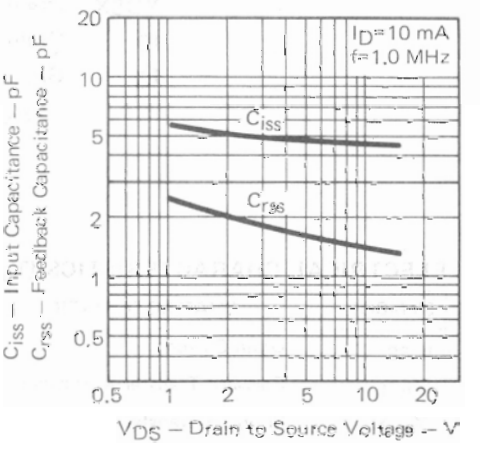
GATE TO SOURCE CUTOFF VOLTAGE vs. DRAIN CURRENT (CORRELATIVITY)



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT (CORRELATIVITY)



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



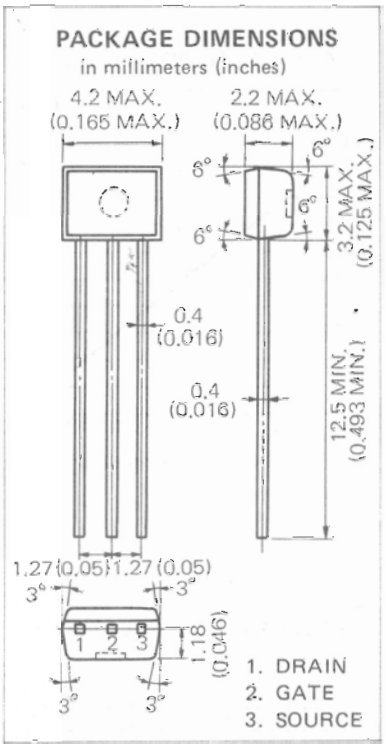
NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFFCT TRANSISTOR

2SK507

DESCRIPTION The 2SK507 is designed for use in VIDEO stage Low Noise amplifier.

- High $|Y_{fs}|$
  $|Y_{fs}|$ = 26 mS TYP. (V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz)
- Low C_{iss}
  C_{iss} = 4.8 pF TYP. (V_{DS} = 5.0 V, I_D = 10 mA, f = 1.0 MHz)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −65 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation ..... 350 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{GDO} Gate to Drain Voltage ..... −15 V
- V_{GSO} Gate to Source Voltage ..... −15 V
- V_{DSX}* Drain to Source Voltage ..... 15 V
- I_D Drain Current ..... 50 mA
- I_G Gate Current ..... 5 mA

* V_{GS} = −4.0 V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Current	10	20	40	mA	V_{DS}=5.0 V, V_{GS}=0
$\|Y_{fs}\|1$	Forward Transfer Admittance	14	19		mS	V_{DS}=5.0 V, I_D=10 mA, f=1.0 kHz
$\|Y_{fs}\|2$	Forward Transfer Admittance	14	26		mS	V_{DS}=5.0 V, V_{GS}=0, f=1.0 kHz
C_{iss}	Input Capacitance		4.8		pF	V_{DS}=5.0 V, I_D=10 mA, f=1.0 MHz
C_{rss}	Feedback Capacitance		1.6		pF	V_{DS}=5.0 V, I_D=10 mA, f=1.0 MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS}=−10 V, V_{DS}=0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.6	−1.4	−3.0	V	V_{DS}=5.0 V, I_D=10 μA

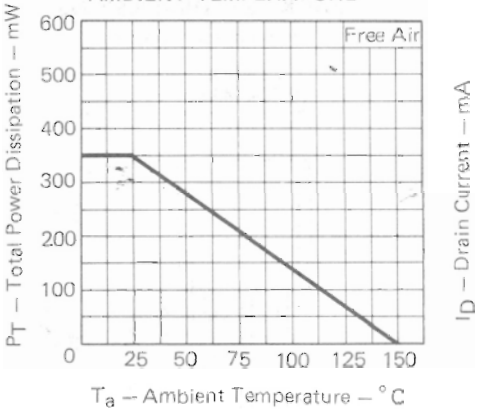
Classification of I_{DSS}

Rank	E	F	H
I_{DSS}(mA)	10 − 20	15 − 30	25 − 40

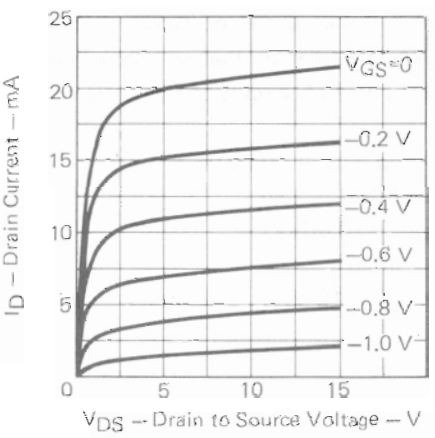
I_{DSS} Test Conditions: V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

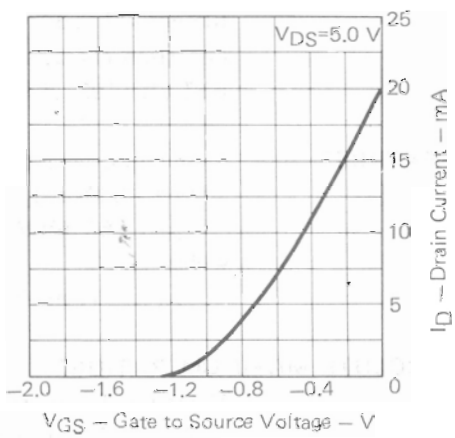
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



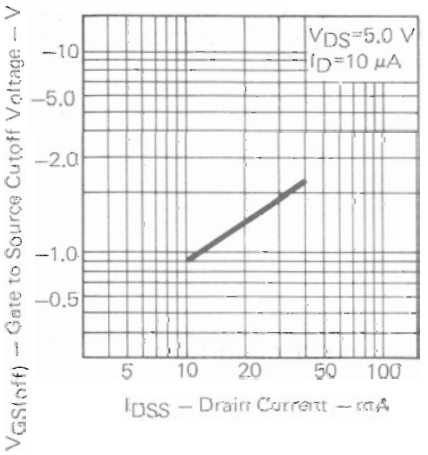
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



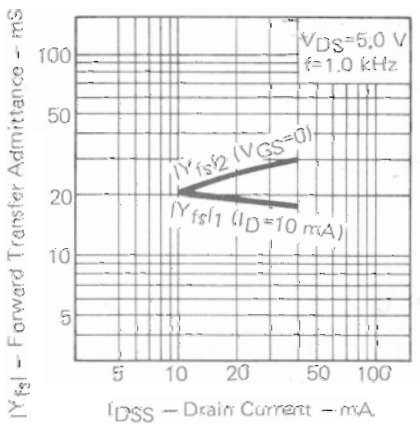
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



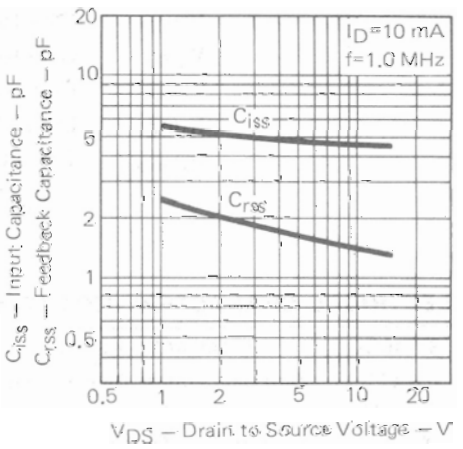
GATE TO SOURCE CUTOFF VOLTAGE vs. DRAIN CURRENT (CORRELATIVITY)



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT (CORRELATIVITY)



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

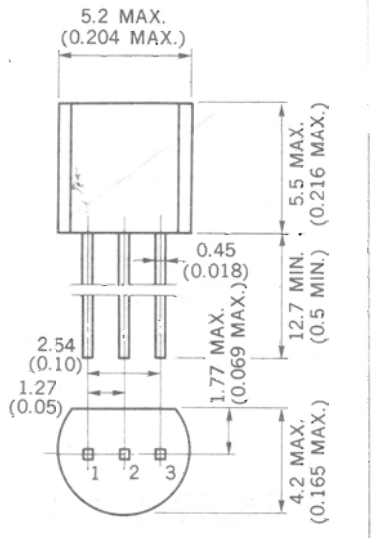
2SK518

DESCRIPTION The 2SK518 is designed for use in RF amplifier of an electronic tuning AM radio receiver. It has excellent cross modulation distortion characteristic compared with that of a conventional FET (2SK193, 2SK163 etc.) at AGC circuit of a cascade type.

FEATURES

- An improvement of X-mod. (19 to 20 dB).
  (f_d = 1.0 MHz, f_u = 1.04 MHz
  $v_{in(d)}$ = 60 dBμV, $v_{in(u)}$ = 120 dBμV)
- High $|y_{fs}|_1$
  $|y_{fs}|_1$ = 17 mS TYP. (V_{DS} = 10 V, I_D = 30 mA, f = 1.0 kHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. GATE
3. SOURCE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{GDO}	Gate to Drain Voltage	−30	V
V_{GSO}	Gate to Source Voltage	−30	V
V_{DSX} *	Drain to Source Voltage	30	V
$I_{D(DC)}$	Drain Current	50	mA
$I_{D(pulse)}$	Drain Current	110	mA

* V_{GS} = −10 V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}**	Zero-Gate Voltage Drain Current	30	60	110	mA	V_{DS} = 10 V, V_{GS} = 0
$\|y_{fs}\|_1$ **	Forward Transfer Admittance		17		mS	V_{DS} = 10 V, I_D = 30 mA, f = 1.0 kHz
$\|y_{fs}\|_2$ **	Forward Transfer Admittance		22		mS	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		6.0		pF	V_{DS} = 10 V, I_D = 10 mA, f = 1.0 MHz
C_{rss}	Feedback Capacitance		2.0		pF	V_{DS} = 10 V, I_D = 10 mA, f = 1.0 MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS} = −20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−1.5	−4.0	−9.0	V	V_{DS} = 10 V, I_D = 10 μA

** Pulsed: Pulse Width ≦ 1 ms, Duty Cycle ≦ 1 %

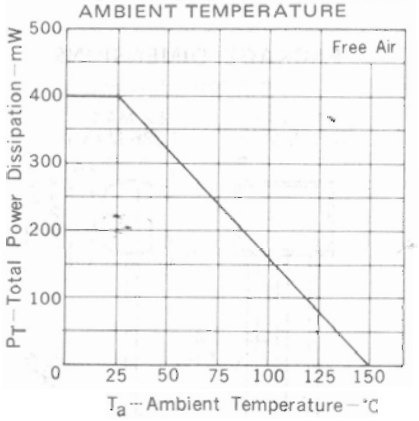
Classification of I_{DSS}

Rank	E	F	H	J	K
I_{DSS}(mA)	30 to 50	45 to 65	60 to 80	75 to 95	90 to 110

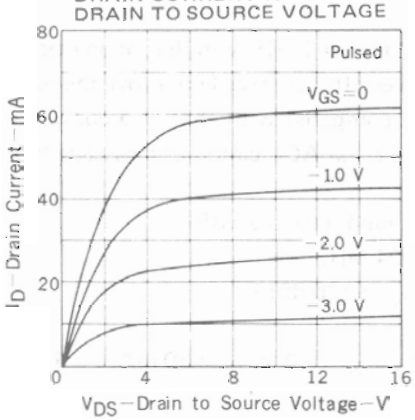
Test Conditions: V_{DS} = 10 V, V_{GS} = 0 (Pulsed: Pulse Width ≦ 1 ms, Duty Cycle ≦ 1 %)

TYPICAL CHARACTERISTICS (T_a = 25 °C)

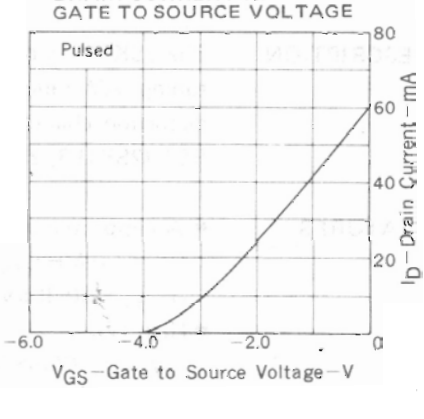
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



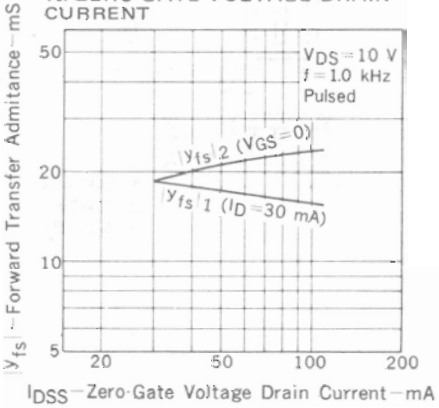
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



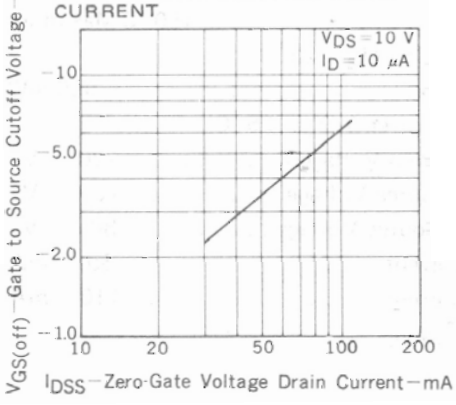
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



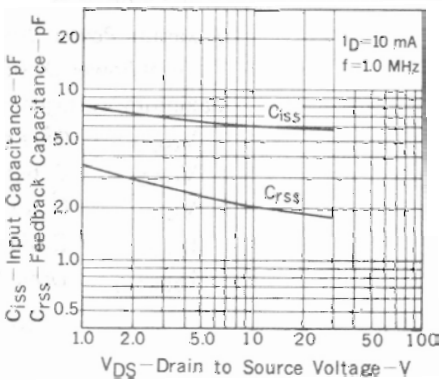
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



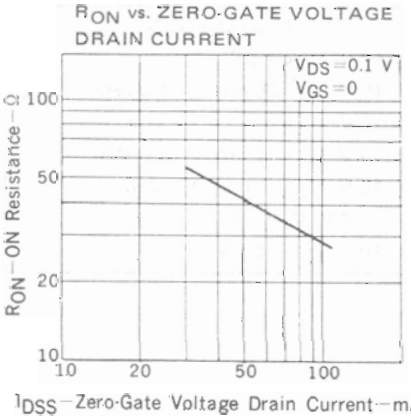
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



R_{ON} vs. ZERO-GATE VOLTAGE DRAIN CURRENT



NEC
ELECTRON DEVICE

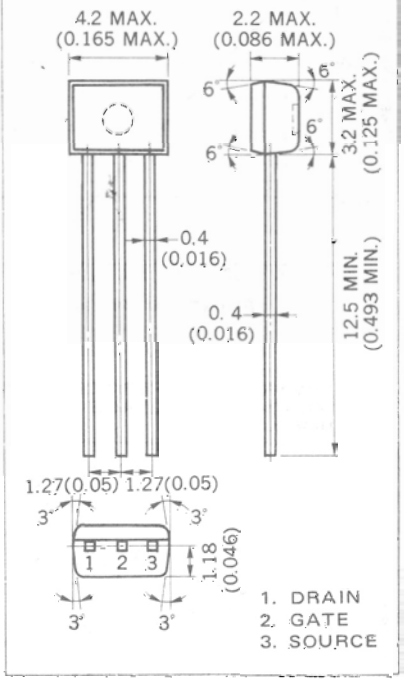
N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK519

DESCRIPTION The 2SK519 is designed for use in RF amplifier of an electronic tuning AM radio receiver. It has excellent cross modulation distortion characteristic compared with that of a conventional FET (2SK193, 2SK163 etc.) at AGC circuit of a cascade type.

FEATURES

- An improvement of X-mod. (19 to 20 dB).
  (f_d = 1.0 MHz, f_u = 1.04 MHz
  $v_{in(d)}$ = 60 dBμV, $v_{in(u)}$ = 120 dBμV)
- High $|y_{fs}|_1$
  $|y_{fs}|_1$ = 17 mS TYP. (V_{DS} = 10 V, I_D = 30 mA, f = 1.0 kHz)

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 350 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{GDO}	Gate to Drain Voltage	−30	V
V_{GSO}	Gate to Source Voltage	−30	V
V_{DSX} *	Drain to Source Voltage	30	V
$I_{D(DC)}$	Drain Current	50	mA
$I_{D(pulse)}$	Drain Current	110	mA

* V_{GS} = −10 V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}**	Zero-Gate Voltage Drain Current	30	60	110	mA	V_{DS} = 10 V, V_{GS} = 0
$\|y_{fs}\|_1$**	Forward Transfer Admittance		17		mS	V_{DS} = 10 V, I_D = 30 mA, f = 1.0 kHz
$\|y_{fs}\|_2$**	Forward Transfer Admittance		22		mS	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		6.0		pF	V_{DS} = 10 V, I_D = 10 mA, f = 1.0 MHz
C_{rss}	Feedback Capacitance		2.0		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS} = −20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−1.5	−4.0	−9.0	V	V_{DS} = 10 V, I_D = 10 μA

** Pulse Width ≤ 1 ms, Duty Cycle ≤ 1 %

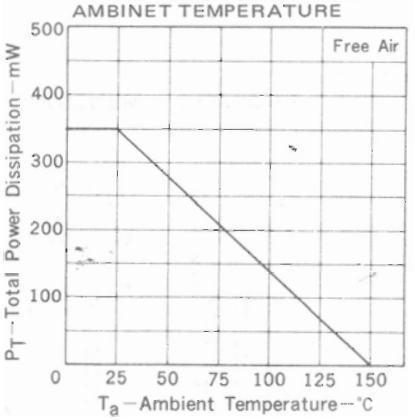
Classification of I_{DSS}

Rank	E	F	H	J	K
I_{DSS}(mA)	30 to 50	45 to 65	60 to 80	75 to 95	90 to 110

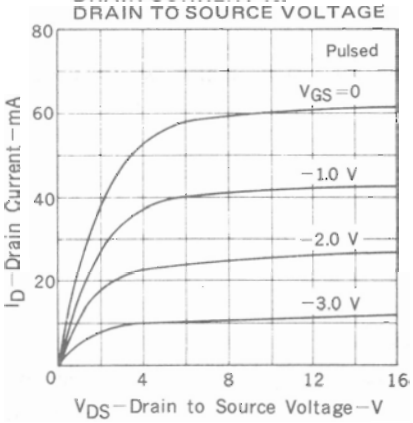
Test Conditions: V_{DS} = 10 V, V_{GS} = 0 (Pulsed: Pulse Width ≤ 1 ms, Duty Cycle ≤ 1 %)

TYPICAL CHARACTERISTICS (T_a = 25 °C)

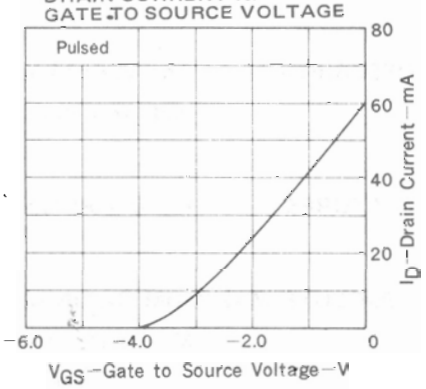
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



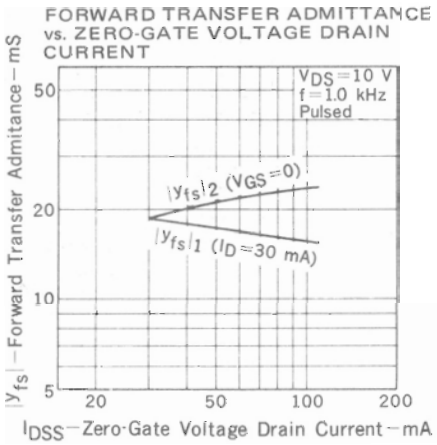
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



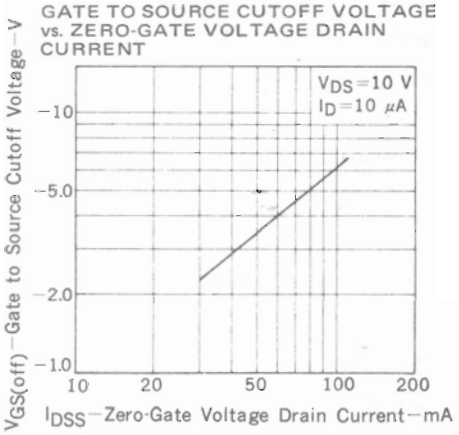
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



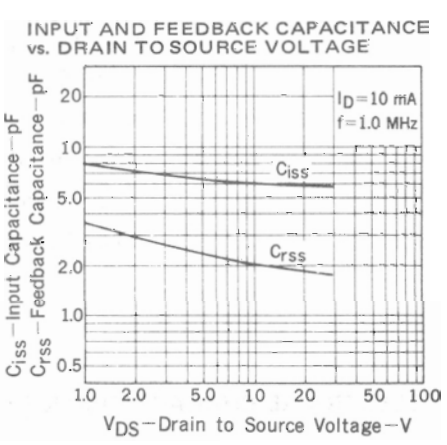
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



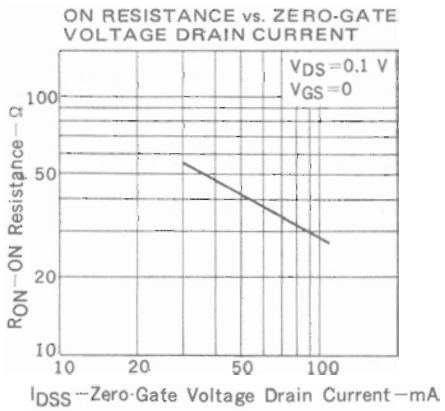
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



ON RESISTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

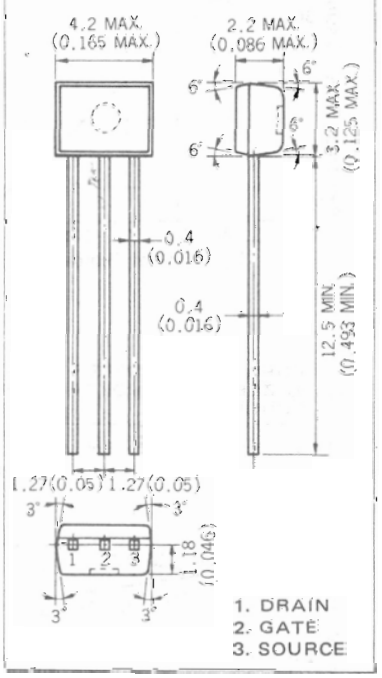
2SK514

DESCRIPTION The 2SK514 is designed for use in analog-switch, variable-resistor and AF amplifier.

FEATURES

- Low cost type FET.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

- Gate to Drain Voltage V_{GDO} . . . . . −50 V
- Gate to Source Voltage V_{GSO} . . . . . −50 V
- Drain to Source Voltage V_{DSX}* . . . . . 50 V
- Drain Current I_D . . . . . 20 mA
- Gate Current I_G . . . . . 10 mA

*V_{GS} = −5.0 V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS} = −30 V, V_{DS} = 0
I_{DSS}	Zero-Gate Voltage Drain Current	1.0	3.5	12	mA	V_{DS} = 5.0 V, V_{GS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.5	−1.7	−4.5	V	V_{DS} = 5.0 V, I_D = 0.1 μA
$\|Y_{fs}\|_1$	Forward Transfer Admittance	1.2	1.8		mS	V_{DS} = 5.0 V, I_D = 0.5 mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	1.4	4.1		mS	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz
Ciss	Input Capacitance		6.0	8.0	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz
Crss	Feedback Capacitance		1.5	2.5	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz

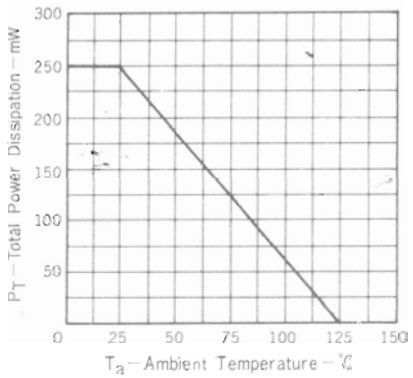
Classification of I_{DSS}

Rank	E	F	H	J	K
I_{DSS}(mA)	1.0 – 2.0	1.5 – 3.0	2.5 – 5.0	4.0 – 8.0	6.0 – 12.0

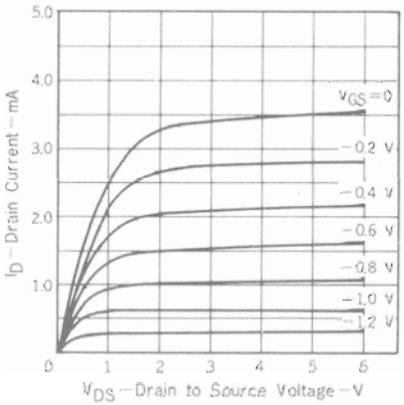
I_{DSS} Test Conditions : V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C unless otherwise noted)

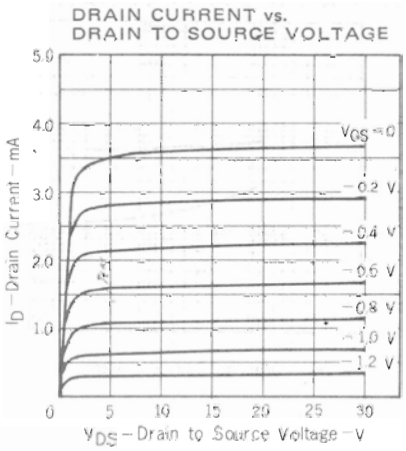
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



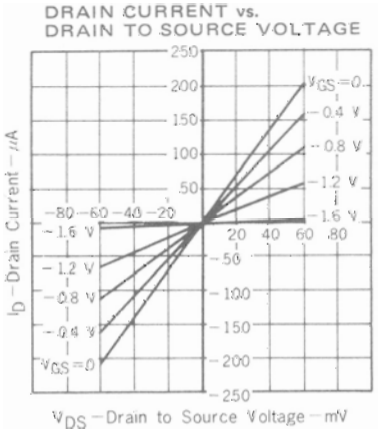
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



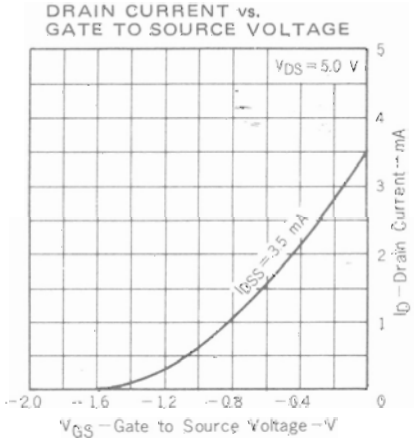
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



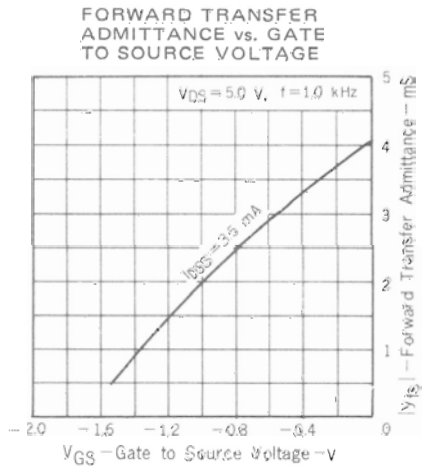
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



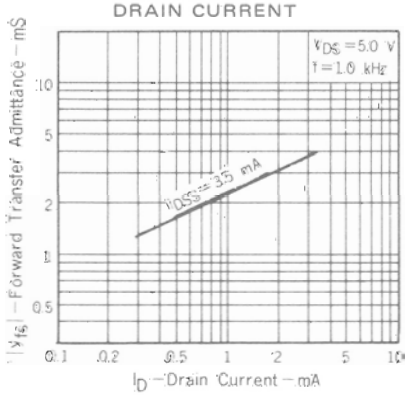
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



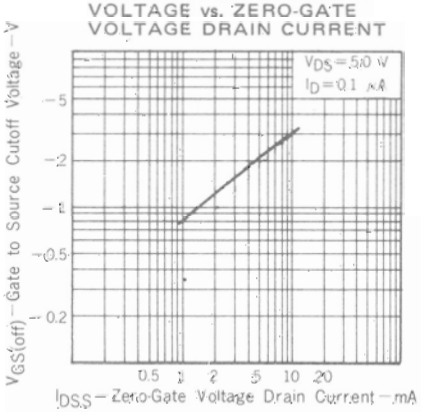
FORWARD TRANSFER ADMITTANCE vs. GATE TO SOURCE VOLTAGE



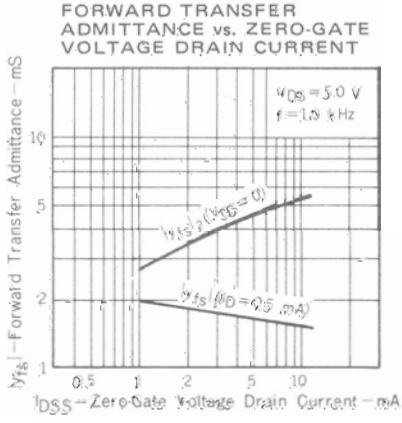
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



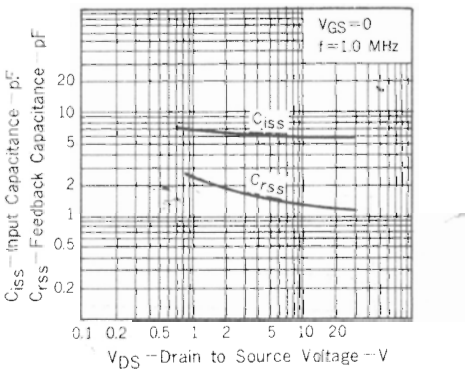
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



INPUT AND FEEDBACK CAPACITANCE
vs. DRAIN TO SOURCE VOLTAGE



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

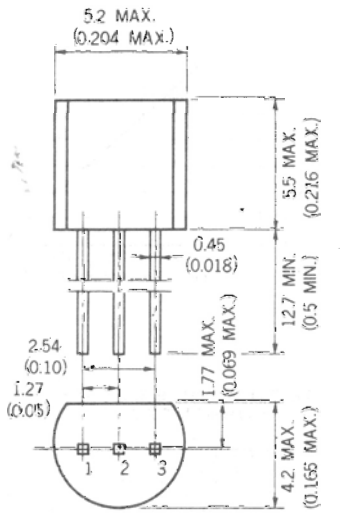
2SK523

DESCRIPTION The 2SK523 is designed for use in the first stage for AF Low Noise amplifier.

FEATURES

- Low Equivalent Noise Voltage.
  $e_n = 1.3\ nV/\sqrt{Hz}$ TYP. ($V_{DS} = 10$ V, $I_D = 1.0$ mA, f = 1.0 kHz)
- High Voltage and High $|Y_{fs}|$
  $V_{DSX} > 50$ V ($V_{GS} = -2.0$ V)
  $|Y_{fs}| > 7.0$ mS ($V_{DS} = 10$ V, $I_D = 1.0$ mA, f = 1.0 kHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. SOURCE
3. GATE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation ($T_a = 25$ °C)

Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{GDO}	Gate to Drain Voltage	−50	V
V_{GSO}	Gate to Source Voltage	−50	V
V_{DSX} *	Drain to Source Voltage	50	V
I_D	Drain Current	30	mA
I_G	Gate Current	10	mA

* $V_{GS} = -2.0$ V

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Current	1.0	8.0	18	mA	$V_{DS} = 10$ V, $V_{GS} = 0$
e_n	Equivalent Noise Voltage		1.3		$nV/\sqrt{Hz}$	$V_{DS} = 10$ V, $I_D = 1.0$ mA, f = 1.0 kHz
$\|Y_{fs}\|_1$	Forward Transfer Admittance	7.0	9.0		mS	$V_{DS} = 10$ V, $I_D = 1.0$ mA, f = 1.0 kHz
$\|Y_{fs}\|_2$	Forward Transfer Admittance	7.0			mS	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 kHz
NV	Noise Voltage			20	mV	See test circuit
C_{iss}	Input Capacitance		13		pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz
C_{rss}	Feedback Capacitance		3.2		pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1.0 MHz
I_{GSS}	Gate Cutoff Current			−1.0	nA	$V_{GS} = -20$ V, $V_{DS} = 0$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.2		−1.2	V	$V_{DS} = 10$ V, $I_D = 10$ μA

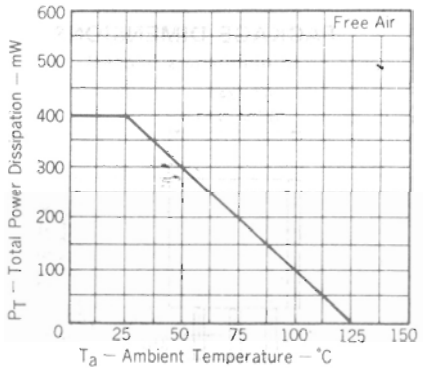
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	1.0 – 5.5	4.5 – 9.5	8.5 – 14	13 – 18

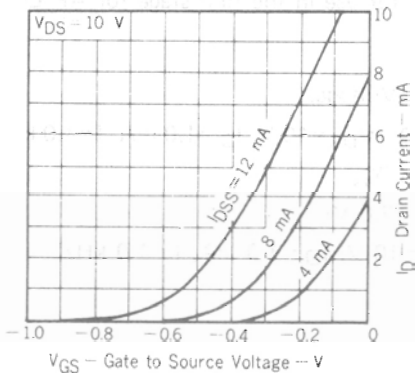
I_{DSS} Test Conditions: $V_{DS} = 10$ V, $V_{GS} = 0$

TYPICAL CHARACTERISTICS (Ta = 25 °C)

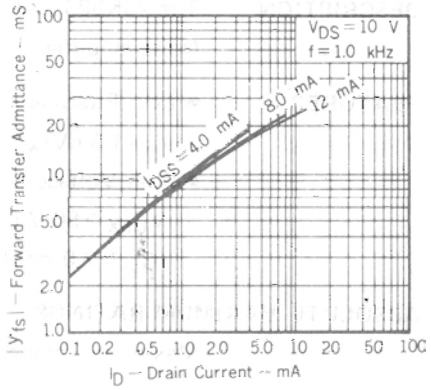
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



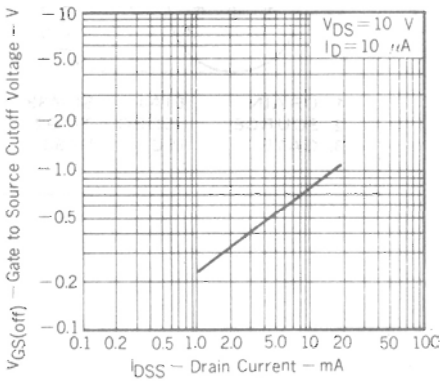
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



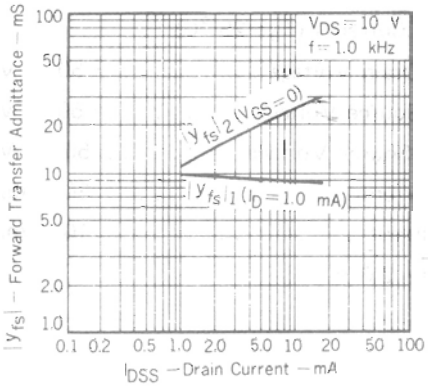
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



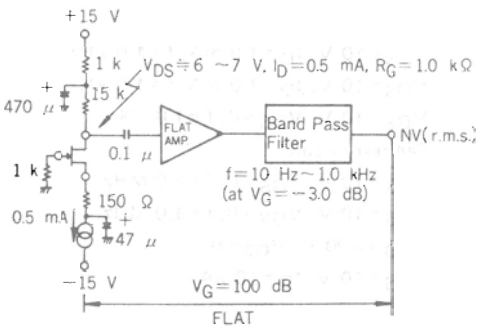
GATE TO SOURCE CUTOFF VOLTAGE vs. DRAIN CURRENT (CORRELATIVITY)



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT (CORRELATIVITY)



NOISE VOLTAGE TEST CIRCUIT



NEC
ELECTRON DEVICE

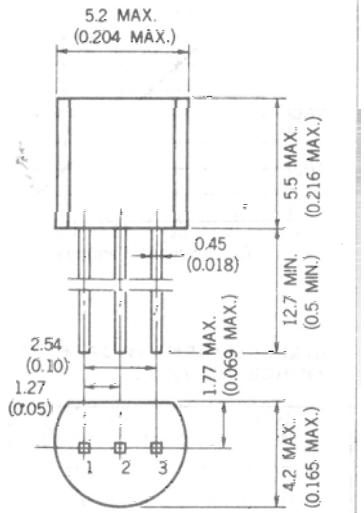
N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR
2SK533

DESCRIPTION The 2SK533 is designed for use in the first stage for AF Low Noise amplifier.

FEATURES

- Low Leak Current
  $I_{GSS} \leqq -100$ pA
- Low Equivalent Noise Voltage.
  $e_n = 1.3\ nV/\sqrt{Hz}$ TYP. ($V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz)
- High Voltage and High $|y_{fs}|$
  $V_{DSX} > 50$ V ($V_{GS} = -2.0$ V)
  $|y_{fs}| > 7.0$ mS ($V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz)

PACKAGE DIMENSIONS
in millimeters (inches)



1. DRAIN
2. SOURCE
3. GATE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation ($T_a = 25$ °C)

- Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{GDO}	Gate to Drain Voltage	−50	V
V_{GSO}	Gate to Source Voltage	−50	V
V_{DSX}*	Drain to Source Voltage	50	V
I_D	Drain Current	30	mA
I_G	Gate Current	10	mA

* $V_{GS} = -2.0$ V

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	1.0	8.0	18	mA	$V_{DS} = 10$ V, $V_{GS} = 0$
e_n	Equivalent Noise Voltage		1.3		$nV/\sqrt{Hz}$	$V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz
$\|y_{fs}\|_1$	Forward Transfer Admittance	7.0	9.0		mS	$V_{DS} = 10$ V, $I_D = 1.0$ mA, $f = 1.0$ kHz
$\|y_{fs}\|_2$	Forward Transfer Admittance	7.0			mS	$V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ kHz
NV	Noise Voltage			20	mV	See Test Circuit
C_{iss}	Input Capacitance		13		pF	$V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz
C_{rss}	Feedback Capacitance		3.2		pF	$V_{DS} = 10$ V, $V_{GS} = 0$, $f = 1.0$ MHz
I_{GSS}	Gate Cutoff Current			−100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.2		−1.2	V	$V_{DS} = 10$ V, $I_D = 10$ μA

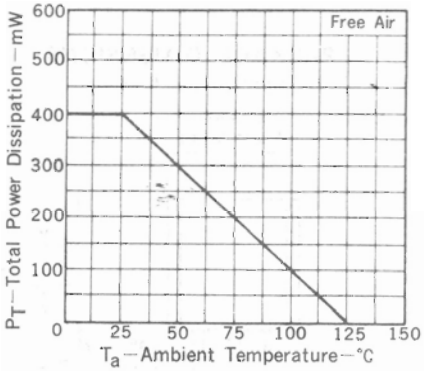
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	1.0 to 5.5	4.5 to 9.5	8.5 to 14	13 to 18

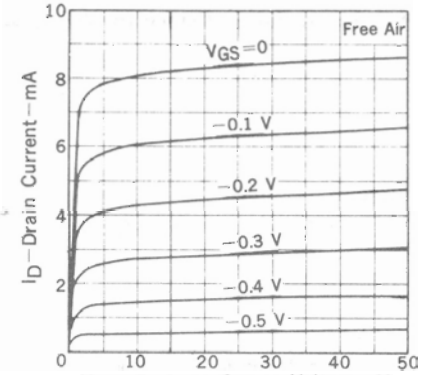
I_{DSS} Test Conditions: $V_{DS} = 10$ V, $V_{GS} = 0$

TYPICAL CHARACTERISTICS (T_a = 25 °C)

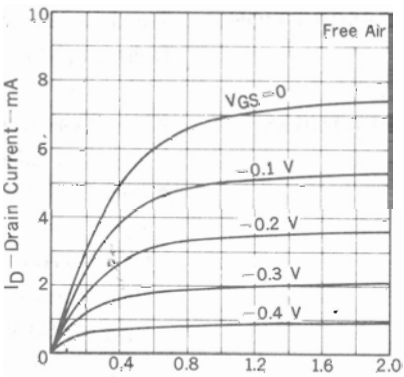
TOTAL POWER DISSIPATION vs. AMBINET TEMPERATURE



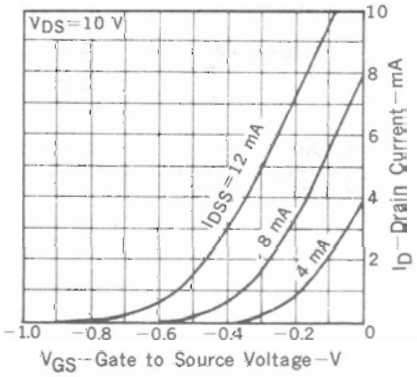
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



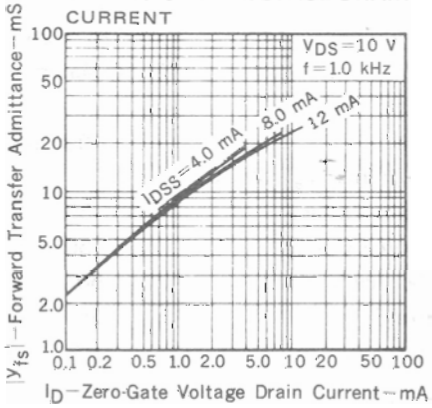
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



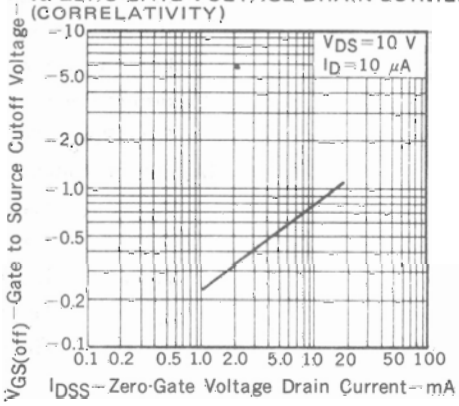
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



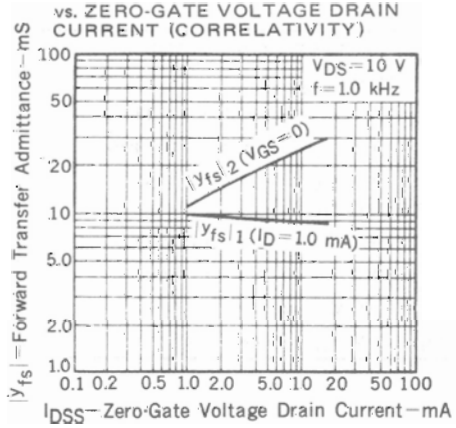
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



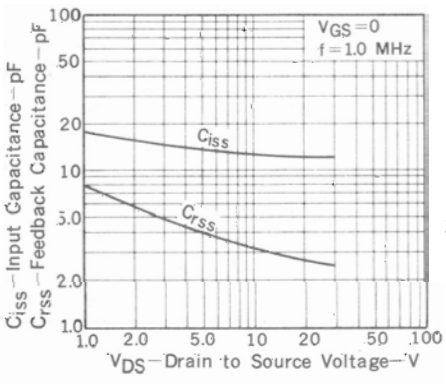
GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



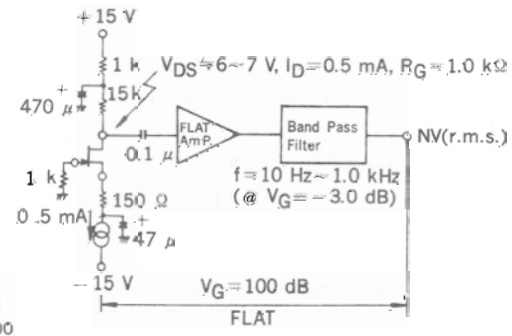
FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT (CORRELATIVITY)



INPUT AND FEEDBACK CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE VOLTAGE TEST CIRCUIT



NEC
ELECTRON DEVICE

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

2SK540

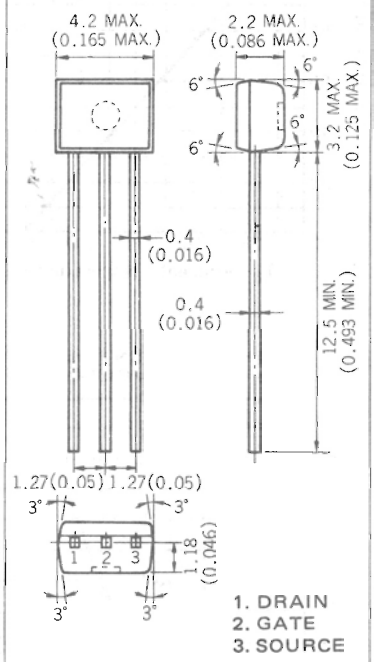
DESCRIPTION The 2SK540 is designed for use in ECM Impedance Converter.

FEATURES

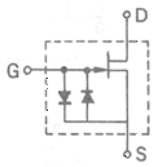
- High $|y_{fs}|$ and Low Conversion Loss
  $|y_{fs}|$ = 1.5 mS TYP. (V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz)
- Gate Bias Diode built-in

NEW DEVICE

PACKAGE DIMENSIONS
in millimeters (inches)



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 100 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{GDO}	Gate to Drain Voltage	−20	V
V_{DSX}*	Drain to Source Voltage	20	V
I_D	Drain Current	10	mA
I_G	Gate Current	−10	mA

*V_{GS} = −1.0 V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Current	20		540	μA	V_{DS} = 5.0 V, V_{GS} = 0
$\|y_{fs}\|_1$	Forward Transfer Admittance	350			μS	V_{DS} = 5.0 V, I_D = 30 μA, f = 1.0 kHz
$\|y_{fs}\|_2$	Forward Transfer Admittance		1500		μS	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 kHz
C_{iss}	Input Capacitance		5.5		pF	V_{DS} = 5.0 V, f = 1.0 MHz
C_{oss}	Output Capacitance		2.7		pF	V_{DS} = 5.0 V, V_{GS} = 0, f = 1.0 MHz
$V_{GS(off)}$	Gate to Source Cutoff Voltage			−0.8	V	V_{DS} = 5.0 V, I_D = 1.0 μA

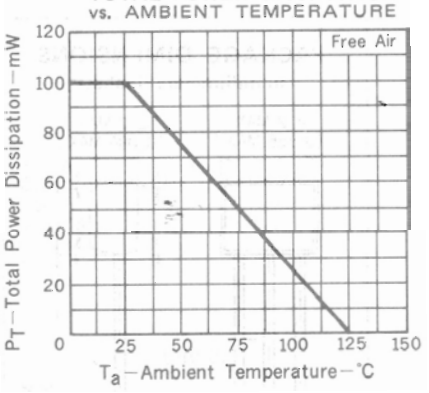
Classification of I_{DSS}

Rank	E	F	H	J	K	L
I_{DSS} (mA)	20 – 40	35 – 70	60 – 120	100 – 200	150 – 300	270 – 540

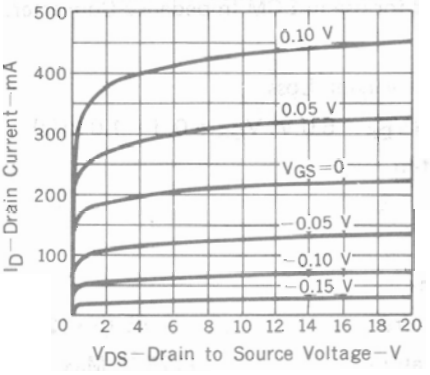
I_{DSS} Test Conditions: V_{DS} = 5.0 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

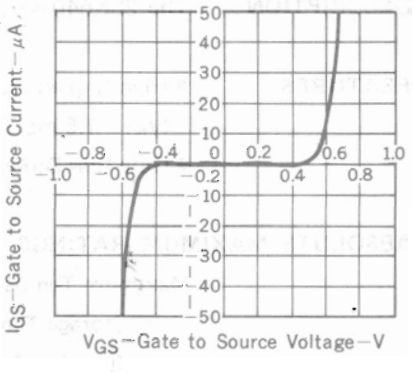
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



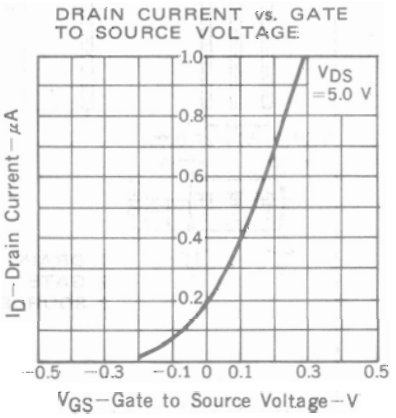
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



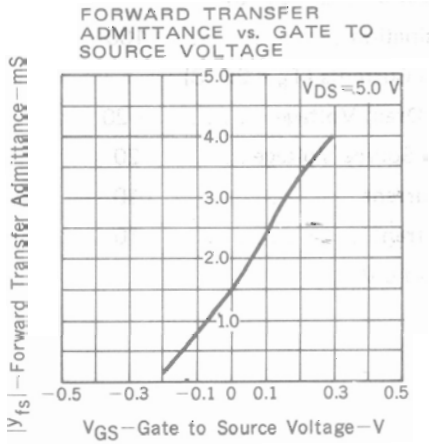
GATE TO SOURCE CURRENT vs. GATE TO SOURCE VOLTAGE



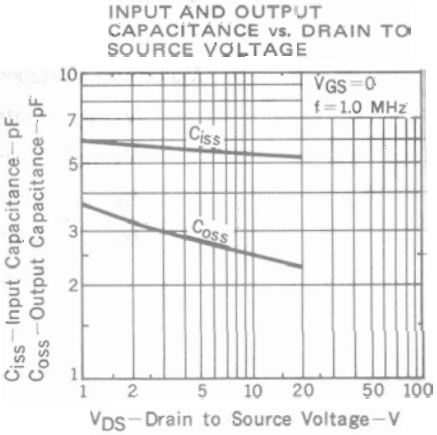
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



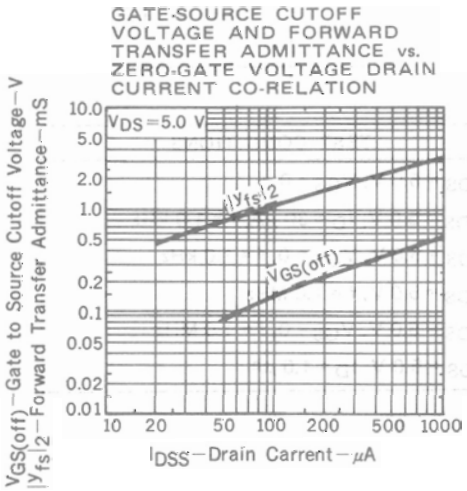
FORWARD TRANSFER ADMITTANCE vs. GATE TO SOURCE VOLTAGE



INPUT AND OUTPUT CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



GATE-SOURCE CUTOFF VOLTAGE AND FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT CO-RELATION



NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK591

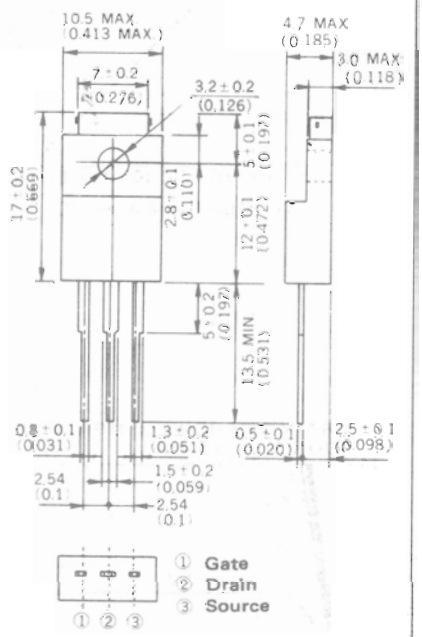
NEW DEVICE

DESCRIPTION The 2SK591 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Secondary Breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

	Total Power Dissipation (T_a = 25 °C) . . .	2.0	W
	Total Power Dissipation (T_c = 25 °C) . . .	35	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	60	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±15	A
$I_{D(pulse)}$	Drain Current (pulse)*	±60	A

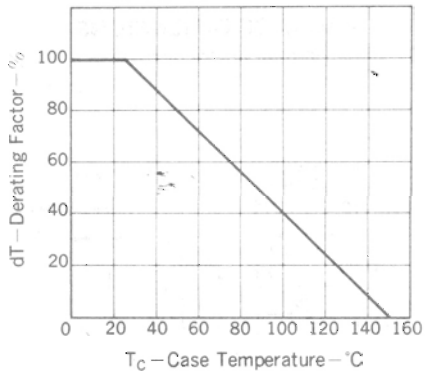
*PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

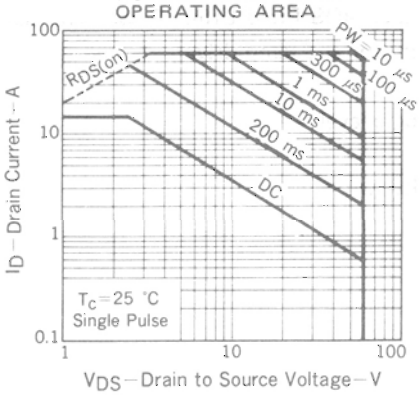
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance			0.055	Ω	V_{GS} = 10 V, I_D = 6 A
$R_{DS(on)}$	Drain to Source On-State Resistance			0.070	Ω	V_{GS} = 4 V, I_D = 6 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	5			S	V_{DS} = 10 V, I_D = 6 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 60 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		1800		pF	V_{DS} = 10V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		800		pF	
C_{rss}	Reverse Transfer Capacitance		350		pF	
$t_{d(on)}$	Turn On Delay Time		20		ns	I_D = 6 A, V_{CC} ≒ 30 V R_L = 5 Ω, $V_{GS(on)}$ = 10 V R_{in} = 10 Ω
t_r	Rise Time		85		ns	
$t_{d(off)}$	Turn Off Delay Time		240		ns	
t_f	Fall Time		230		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

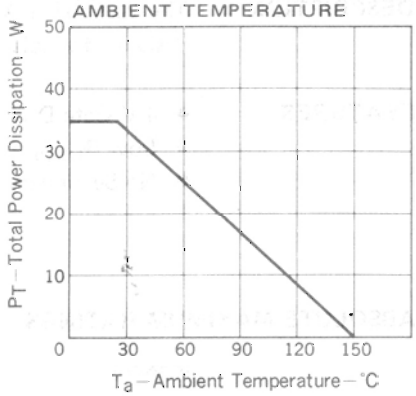
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



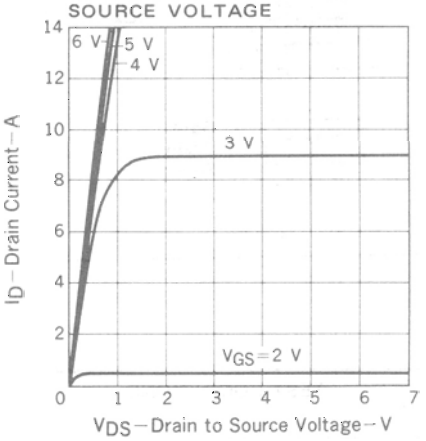
FORWARD BIAS SAFE OPERATING AREA



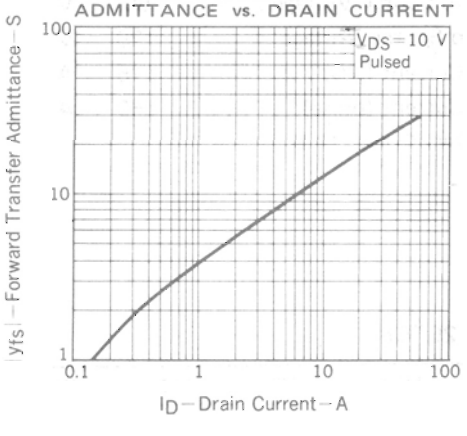
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



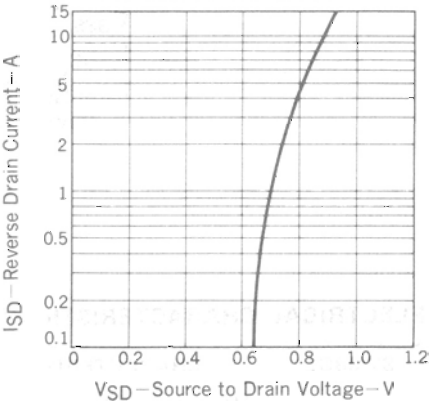
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



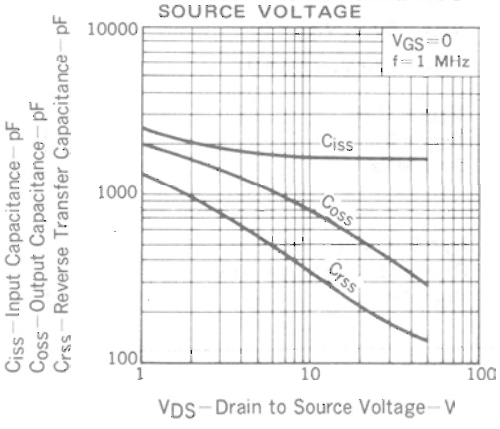
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



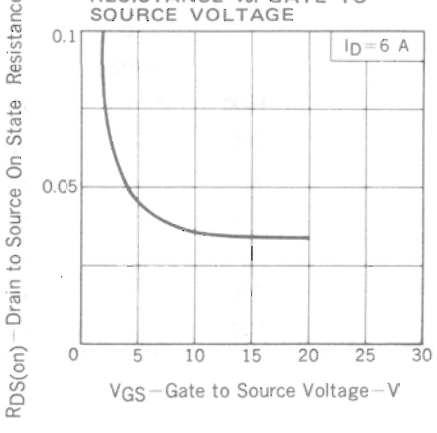
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



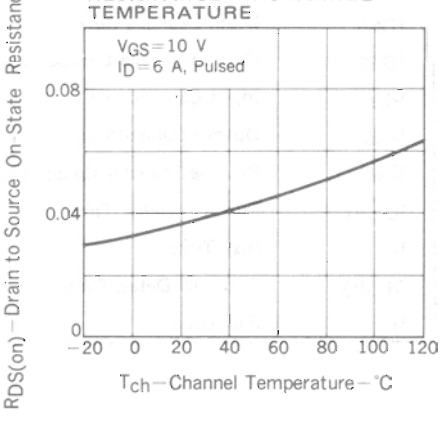
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

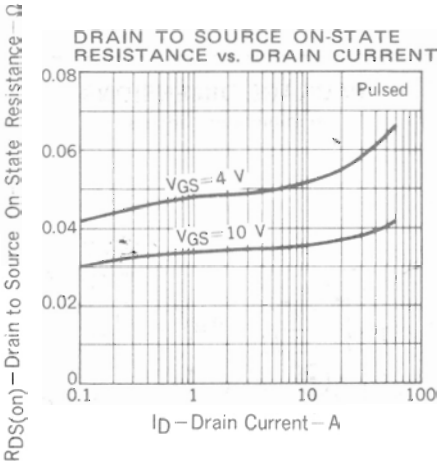


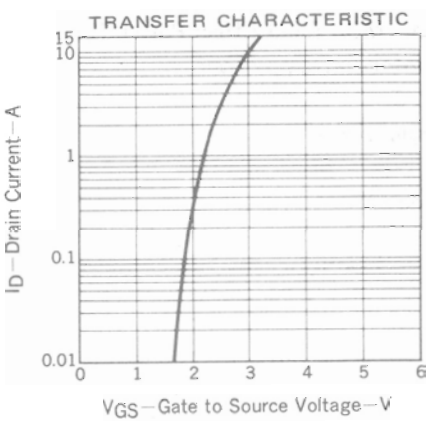
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

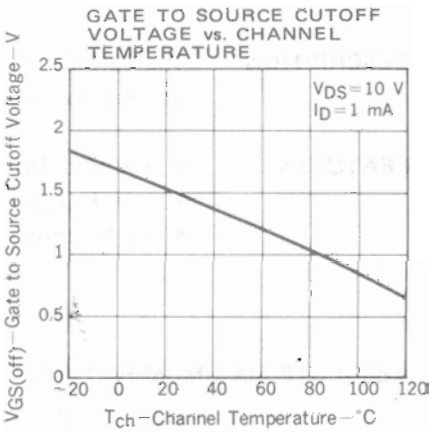


DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

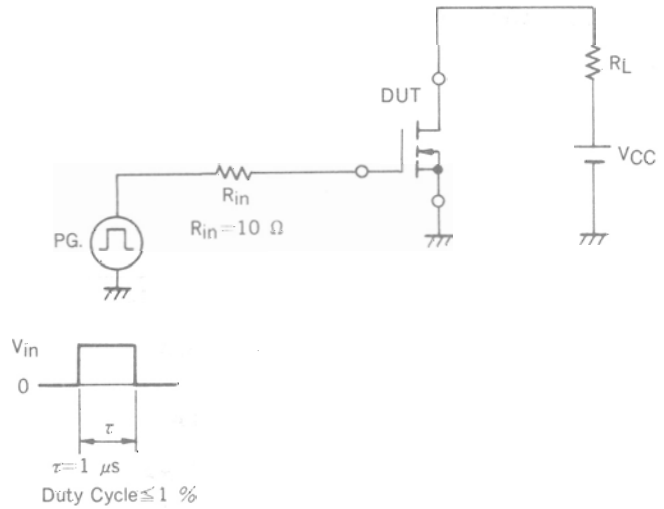


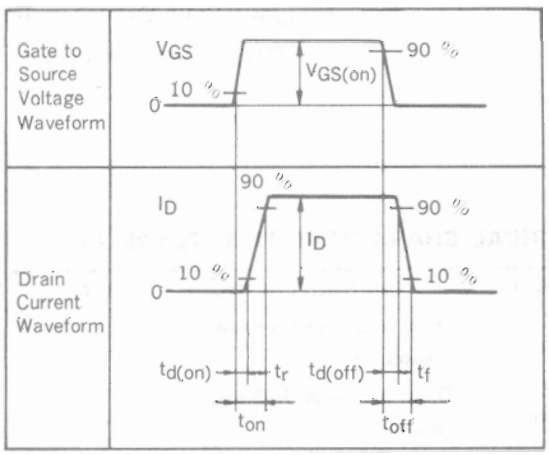






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK659

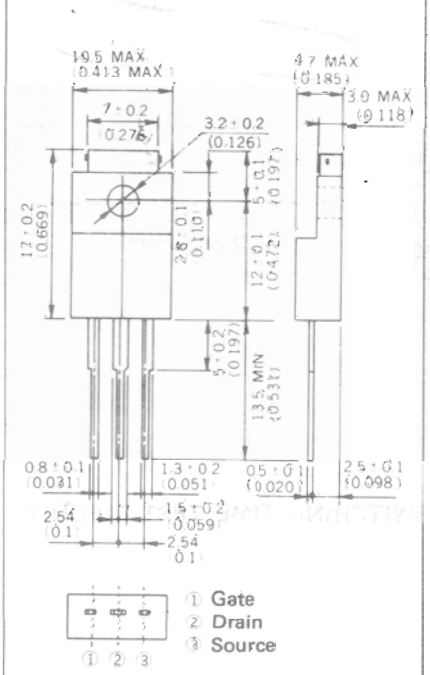
DESCRIPTION The 2SK659 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Secondary Breakdown

NEW DEVICE

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . 2.0 W
- Total Power Dissipation (T_C = 25 °C) . . . 35 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{DSS} Drain to Source Voltage . . . . . 60 V
- V_{GSS} Gate to Source Voltage . . . . . ±20 V
- $I_{D(DC)}$ Drain Current (DC) . . . . . ±12 A
- $I_{D(pulse)}$ Drain Current (pulse)* . . . . . ±60 A

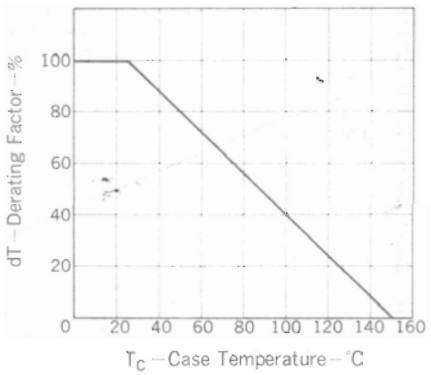
*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

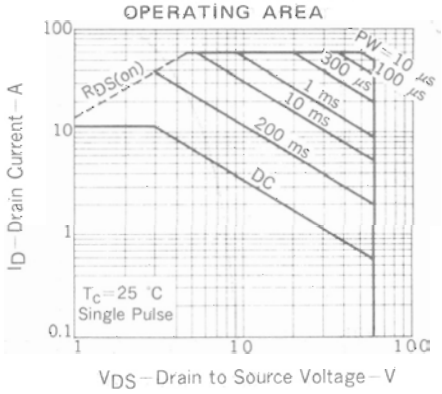
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance			0.075	Ω	V_{GS} = 10 V, I_D = 6 A
$R_{DS(on)}$	Drain to Source On-State Resistance			0.095	Ω	V_{GS} = 4 V, I_D = 6 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	5			S	V_{DS} = 10 V, I_D = 6 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 60 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		1300		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		600		pF	
C_{rss}	Reverse Transfer Capacitance		260		pF	
$t_{d(on)}$	Turn-On Delay Time		15		ns	I_D = 6 A, V_{CC} ≒ 30 V R_L = 5 Ω, $V_{GS(on)}$ = 10 V R_{in} = 10 Ω
t_r	Rise Time		75		ns	
$t_{d(off)}$	Turn-Off Delay Time		80		ns	
t_f	Fall Time		80		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

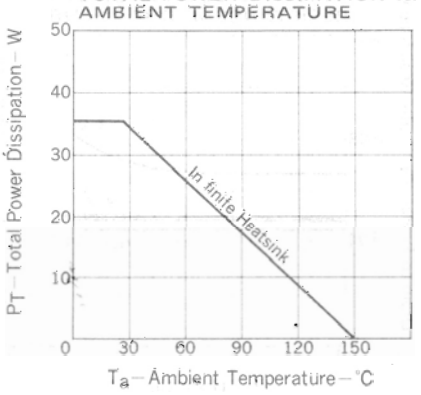
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



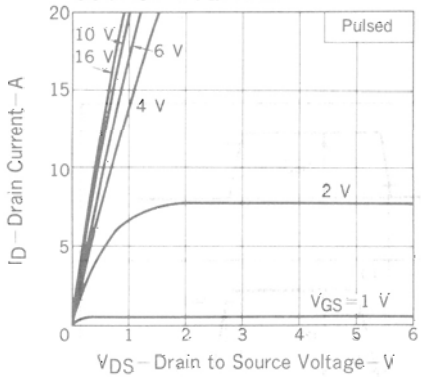
FORWARD BIAS SAFE OPERATING AREA



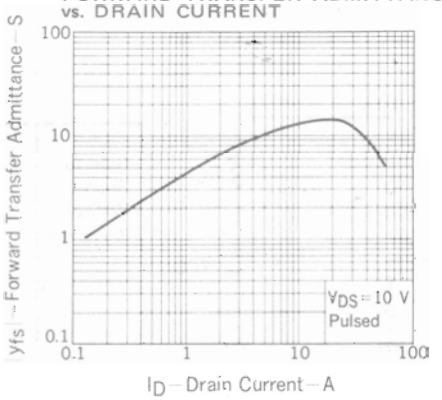
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



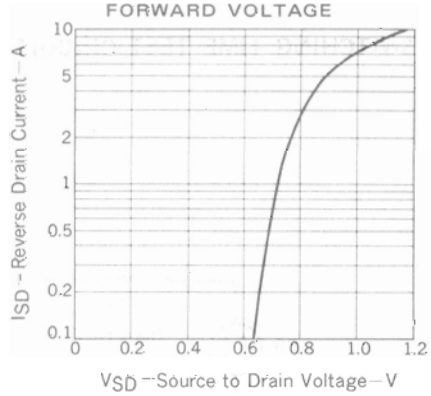
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



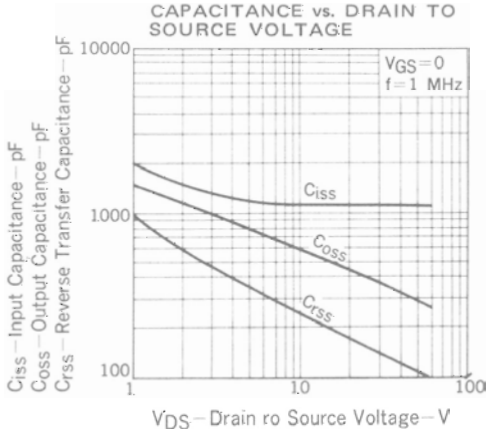
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



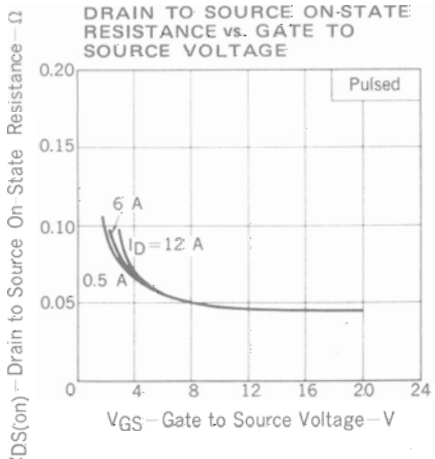
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



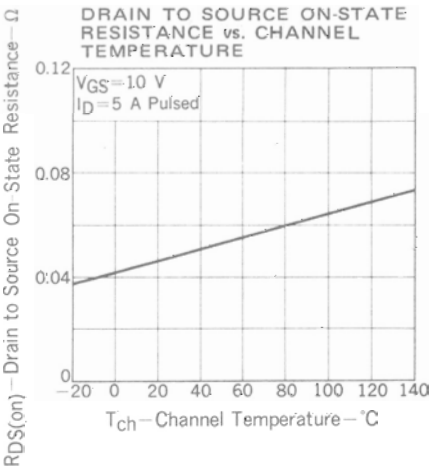
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

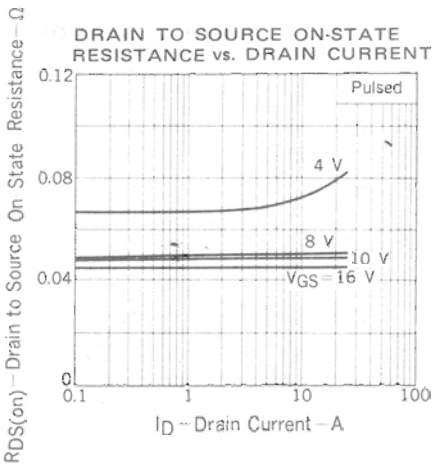


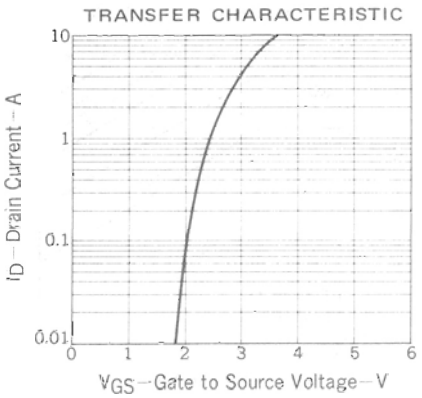
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

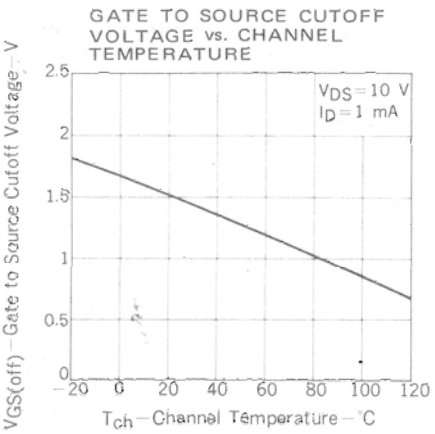


DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

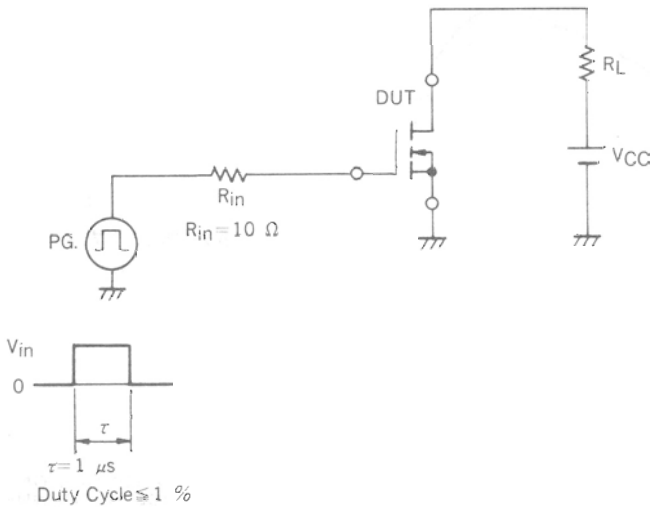


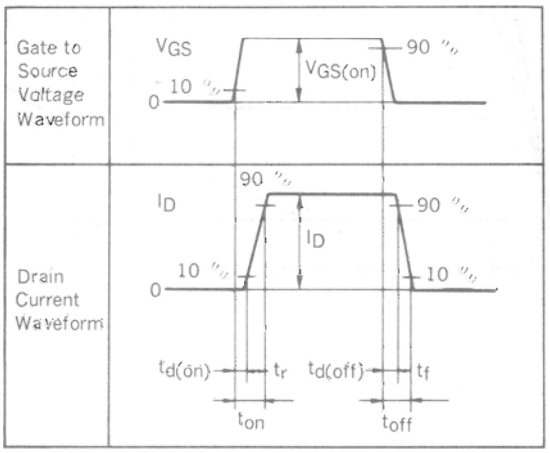






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK679

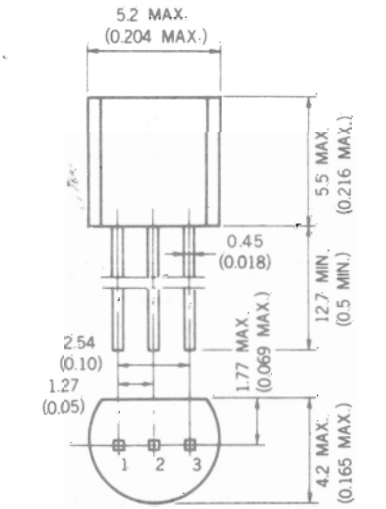
NEW DEVICE

FEATURES

- Suitable for switching power supplies, actuater controls, and pulse circuits
- Low $R_{DS(on)}$; $R_{DS(on)}$ = 0.95 Ω TYP. (V_{GS} = 4 V, I_D = 0.5 A)
- No second breakdown

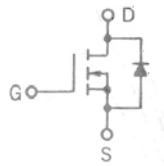
PACKAGE DIMENSIONS

in millimeters (inches)



1. Gate (G)
2. Drain (D)
3. Source (S)

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	30	V
V_{GSS}	Gate to Source Voltage.	±20	V
$I_{D(DC)}$	Drain Current (DC)	±1.0	A
$I_{D(pulse)}$	Drain Current (pulse)*	±2.0	A

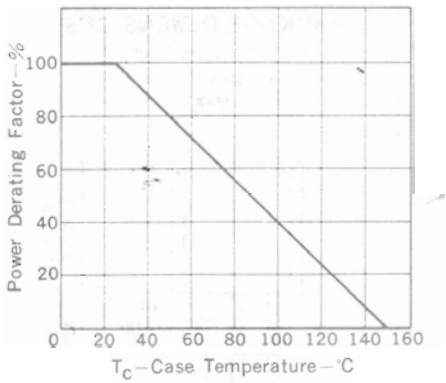
* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

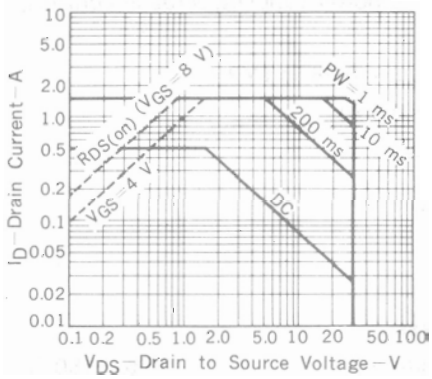
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 20 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1.0 mA
$\|y_{fs}\|$	Forward Transfer Admittance	0.4			S	V_{DS} = 10 V, I_D = 0.5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.5	1.0	Ω	V_{GS} = 10 V, I_D = 0.5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.95	1.5	Ω	V_{GS} = 4.0 V, I_D = 0.5 A
C_{iss}	Input Capacitance		40		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
C_{oss}	Output Capacitance		65		pF	
C_{rss}	Reverse Transfer Capacitance		10		pF	
$t_{d(on)}$	Turn-On Delay Time		60		ns	I_D = 0.5 A, V_{CC} = 25 V, $V_{GS(on)}$ = 10 V, R_L = 50 Ω, R_{in} = 10 Ω
t_r	Rise Time		180		ns	
$t_{d(off)}$	Turn-Off Delay Time		550		ns	
t_f	Fall Time		400		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

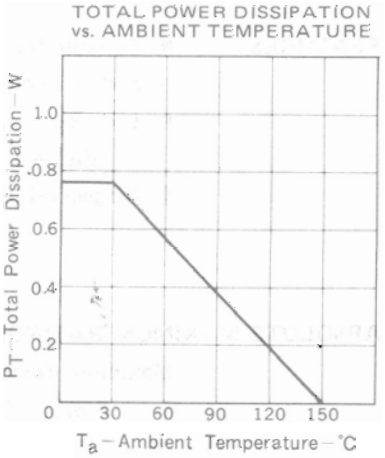
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



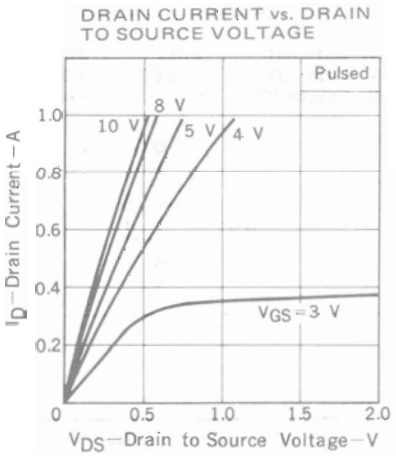
FORWARD BIAS SAFE OPERATING AREA



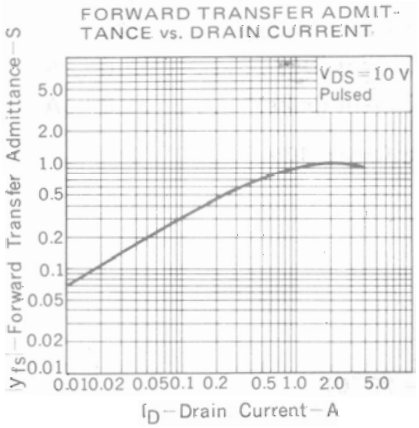
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



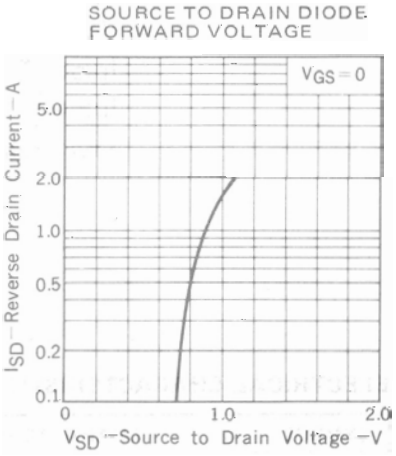
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



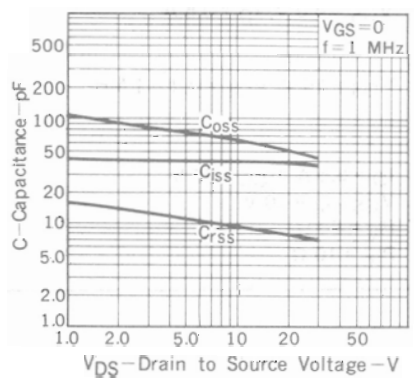
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



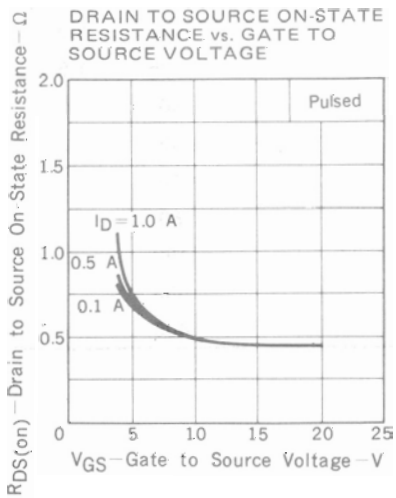
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



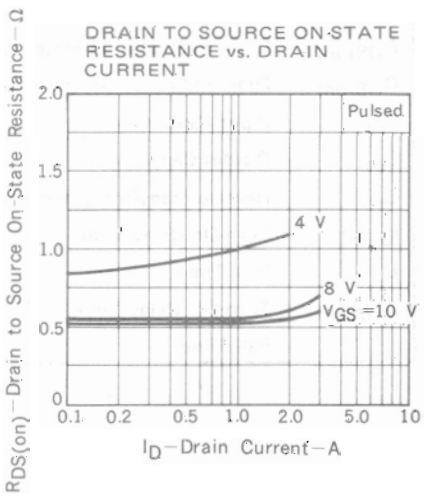
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



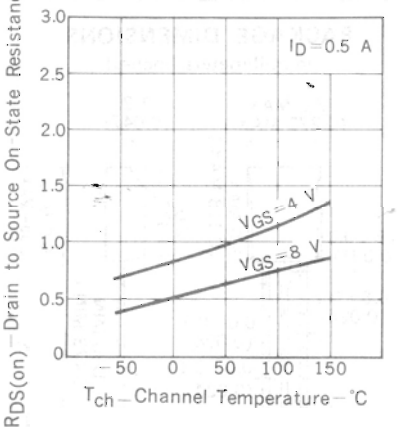
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



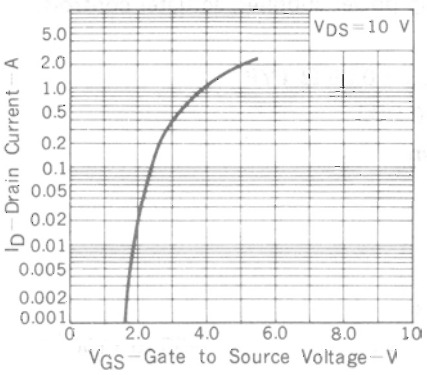
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



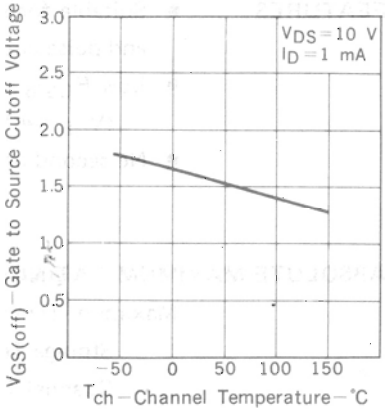
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



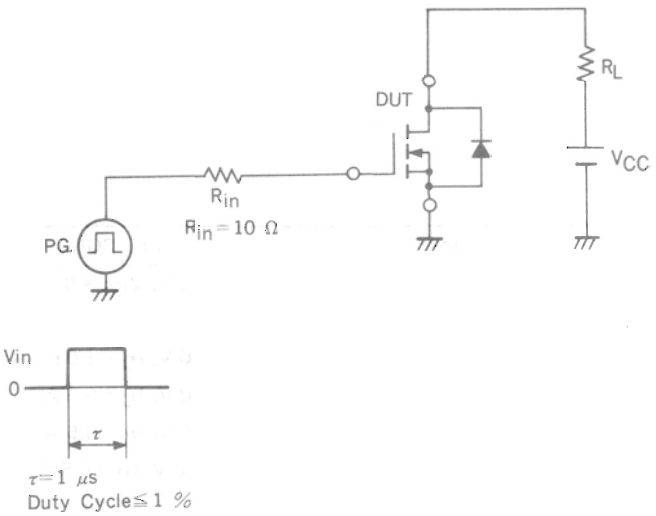
TRANSFER CHARACTERISTICS

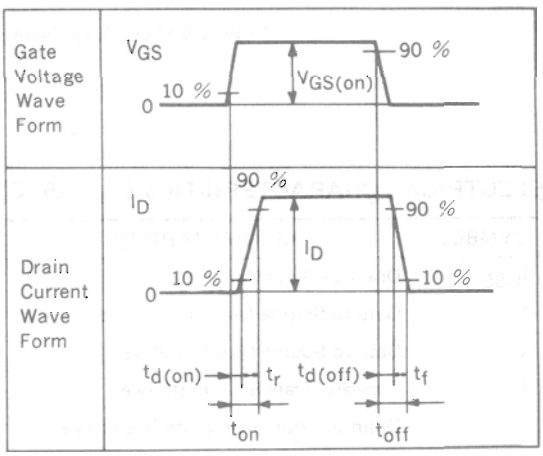


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



TURN-ON AND TURN-OFF TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK681

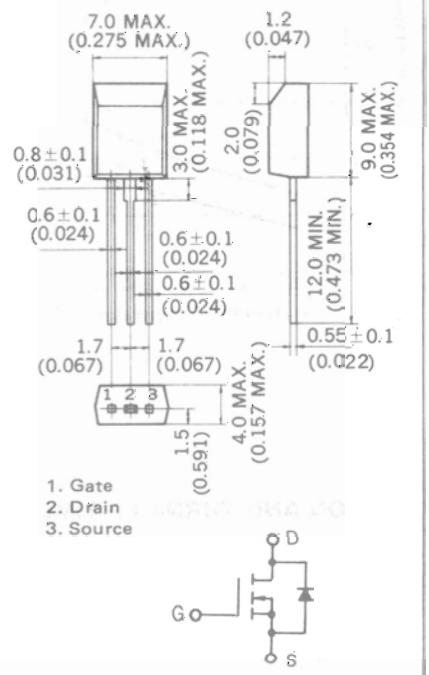
NEW DEVICE

FEATURES

- Suitable for switching power supplies, actuater controls, and pulse circuits
- Low $R_{DS(on)}$: $R_{DS(on)}$ = 0.95 Ω TYP. (V_{GS} = 4 V, I_D = 0.5 A)
- No second breakdown

PACKAGE DIMENSIONS

in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 1.0 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	30	V
V_{GSS}	Gate to Source Voltage.	±20	V
$I_{D(DC)}$	Drain Current (DC)	±1.0	A
$I_{D(pulse)}$	Drain Current (pulse)*	±2.0	A

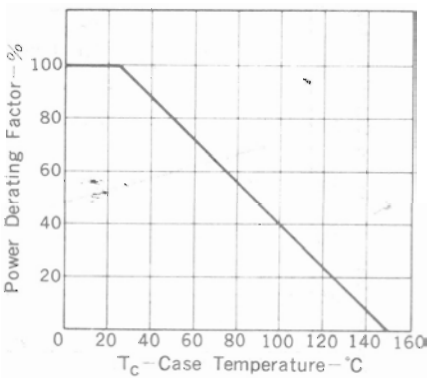
* PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

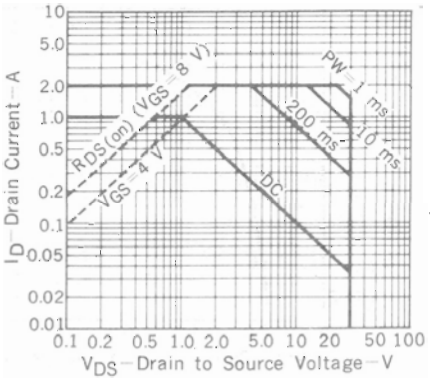
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 20 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1.0 mA
$\|y_{fs}\|$	Forward Transfer Admittance	0.4			S	V_{DS} = 10 V, I_D = 0.5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.5	1.0	Ω	V_{GS} = 10 V, I_D = 0.5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.95	1.5	Ω	V_{GS} = 4.0 V, I_D = 0.5 A
C_{iss}	Input Capacitance		40		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
C_{oss}	Output Capacitance		65		pF	
C_{rss}	Reverse Transfer Capacitance		10		pF	
$t_{d(on)}$	Turn-On Delay Time		60		ns	I_D = 0.5 A, V_{CC} = 25 V, $V_{GS(on)}$ = 10 V, R_L = 50 Ω, R_{in} = 10 Ω
t_r	Rise Time		180		ns	
$t_{d(off)}$	Turn-Off Delay Time		550		ns	
t_f	Fall Time		400		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

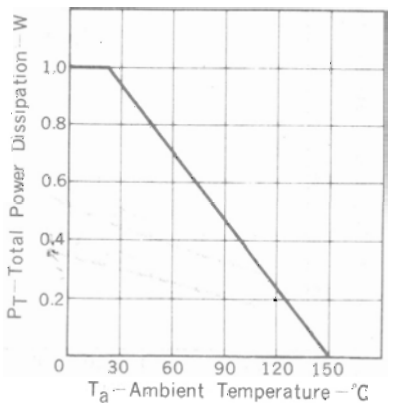
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



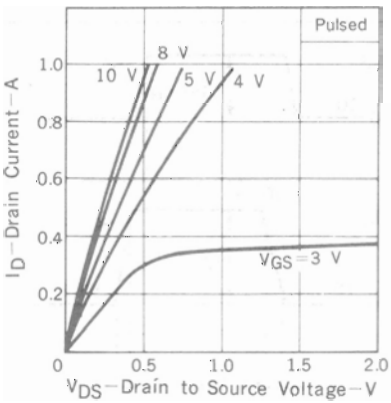
FORWARD BIAS SAFE OPERATING AREA



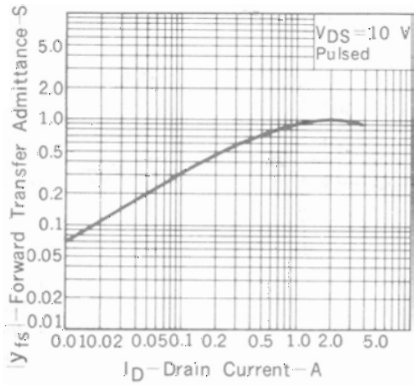
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



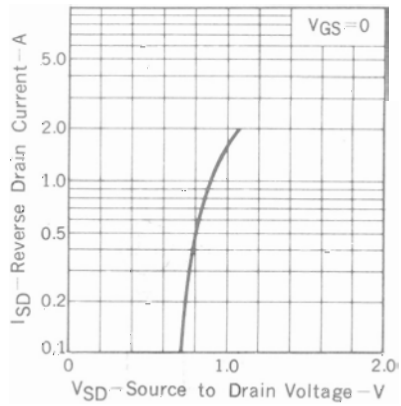
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



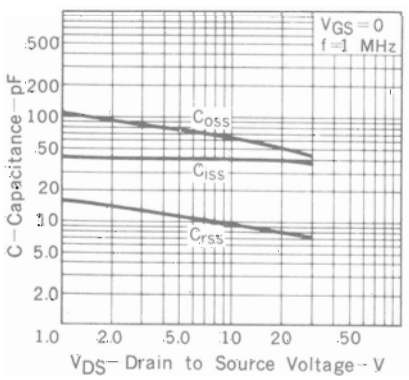
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



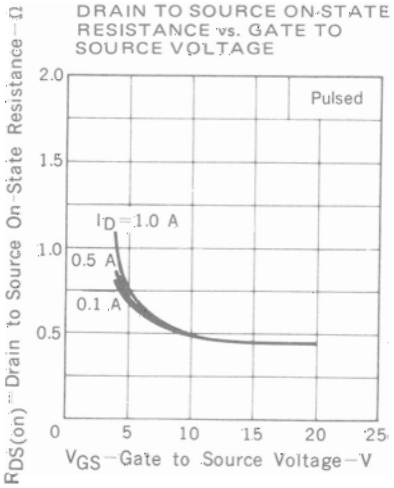
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



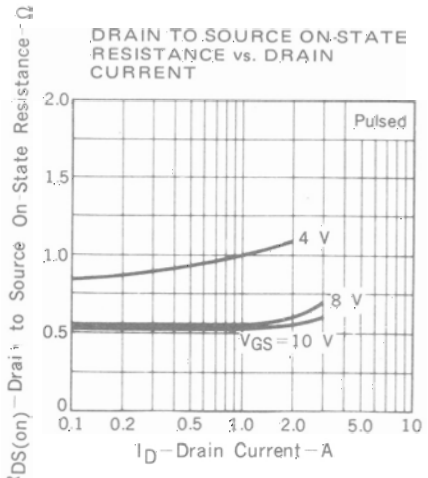
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



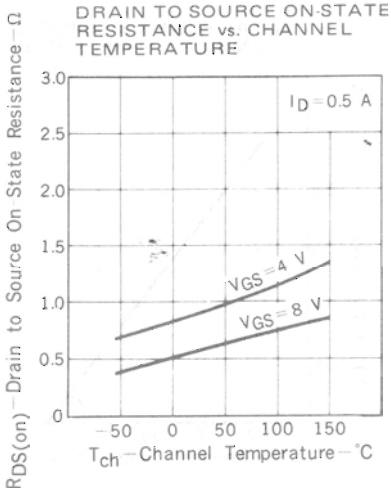
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



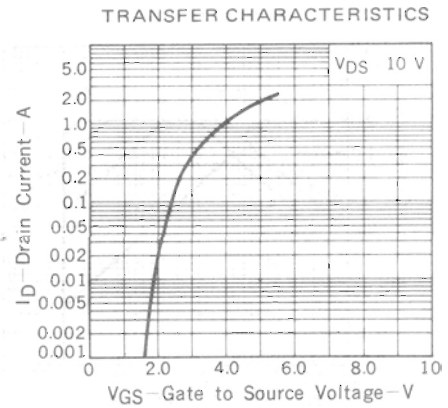
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



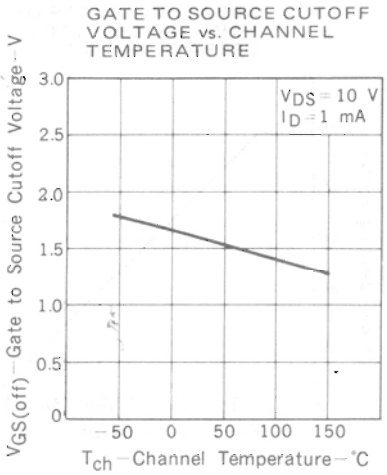
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



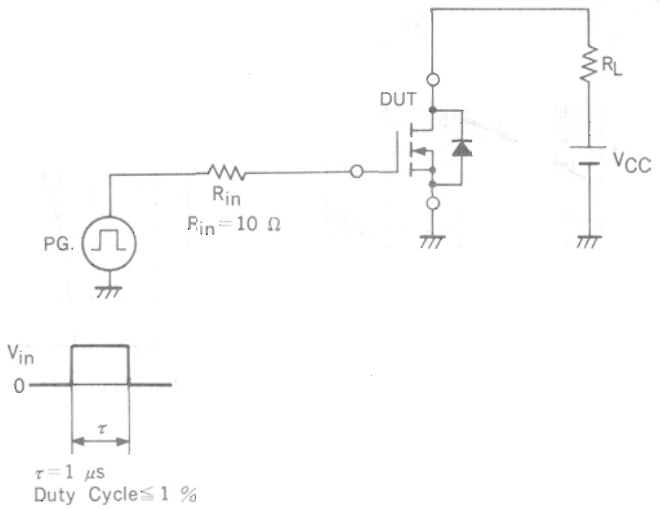
TRANSFER CHARACTERISTICS

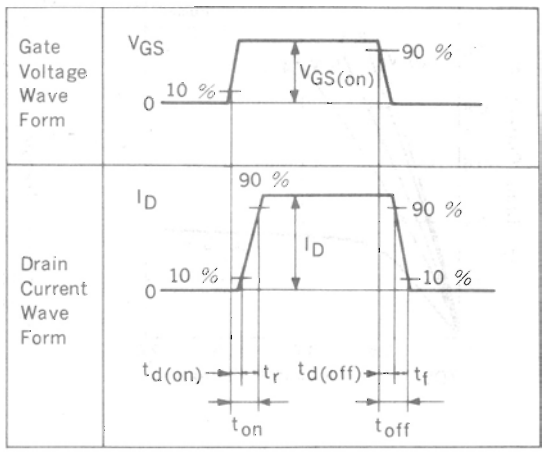


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



TURN-ON AND TURN-OFF TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

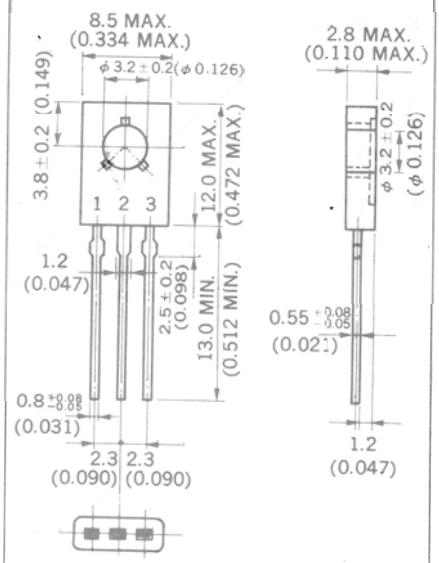
2SK699

DESCRIPTION The 2SK699 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Second Breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



1. Source
2. Drain connected to mounting plane
3. Gate

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation . . . . . 1.3 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage.	±20	V
$I_{D(DC)}$	Drain Current (DC)	±2	A
$I_{D(pulse)}$	Drain Current (pulse)*	±6	A

* PW ≤ 300 μs, Duty Cycle ≤ 10 %

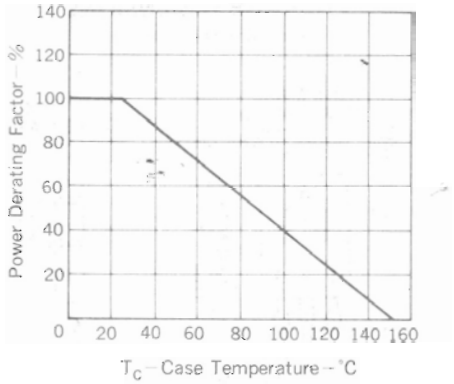
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.8	1.2	Ω	V_{GS} = 10 V, I_D = 1 A
$R_{DS(on)}$	Drain to Source On-State Resistance		1.0	1.5	Ω	V_{GS} = 4 V, I_D = 1 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{GS} = 10 V, I_D = 1 mA
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	0.5			S	V_{DS} = 10 V, I_D = 1 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		200		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		70		pF	
C_{rss}	Reverse Transfer Capacitance		15		pF	
$t_{d(on)}$	Turn-On Delay Time		45		ns	I_D = 1 A, V_{CC} = 50 V R_L = 50 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		450		ns	
t_f	Fall Time		110		ns	

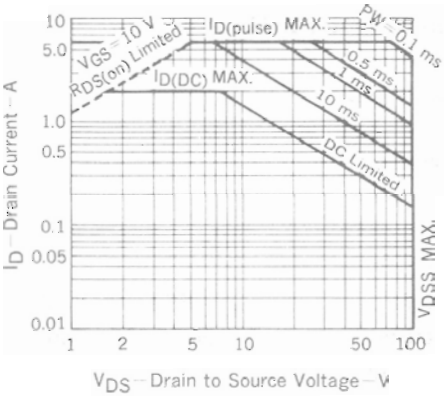
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

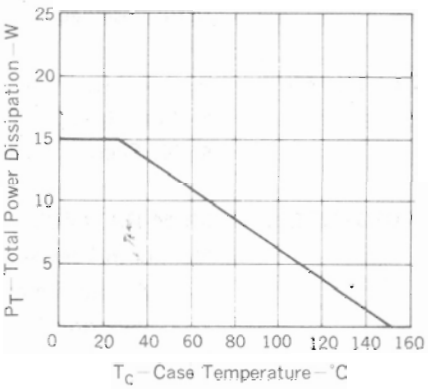
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



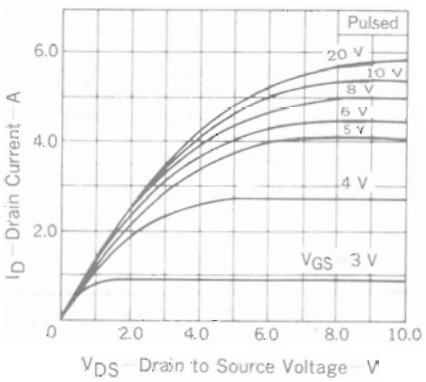
FORWARD BIAS SAFE OPERATING AREA



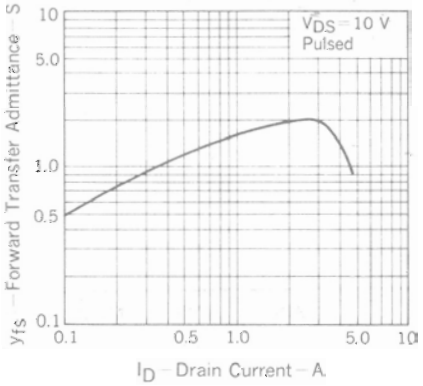
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



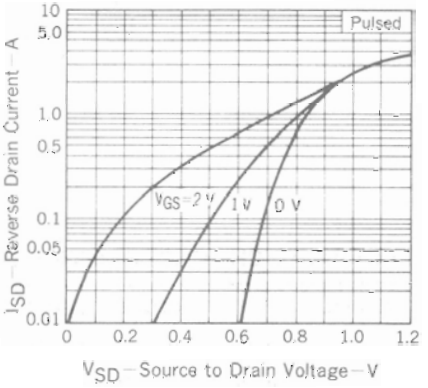
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



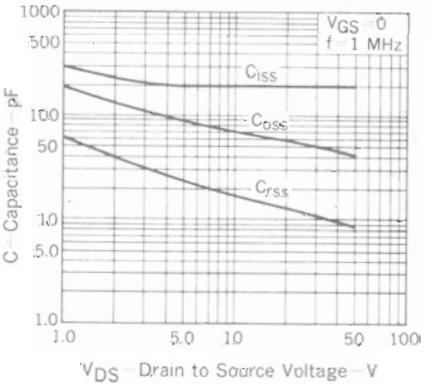
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



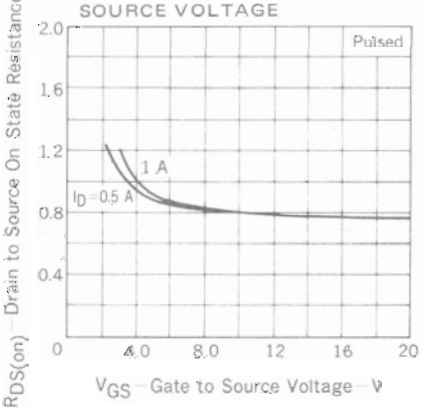
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



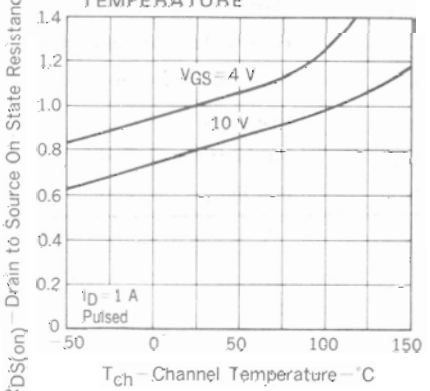
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

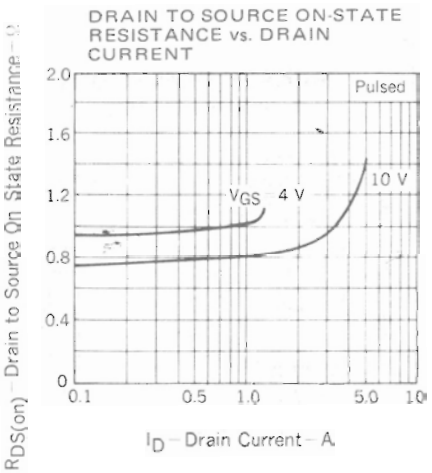


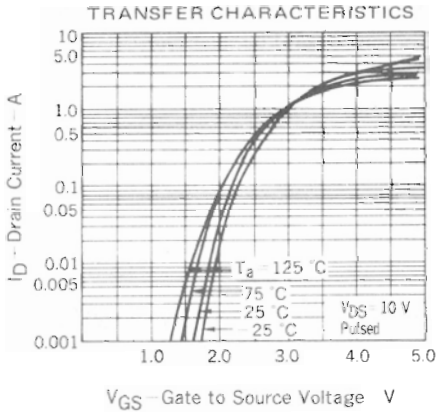
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

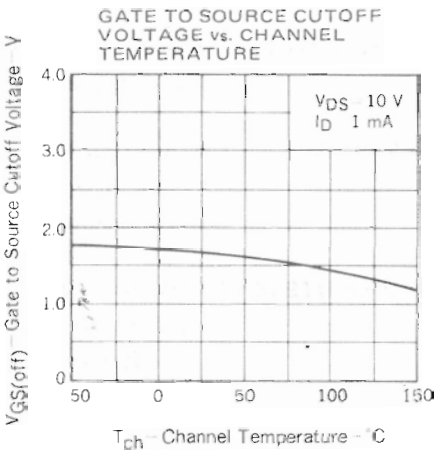


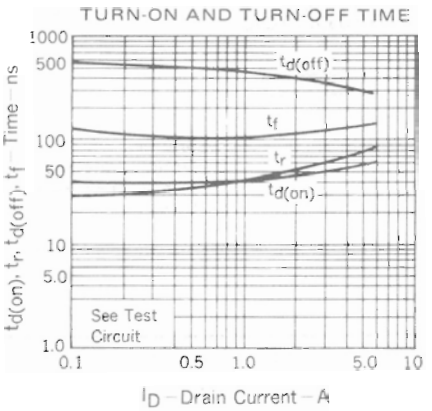
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



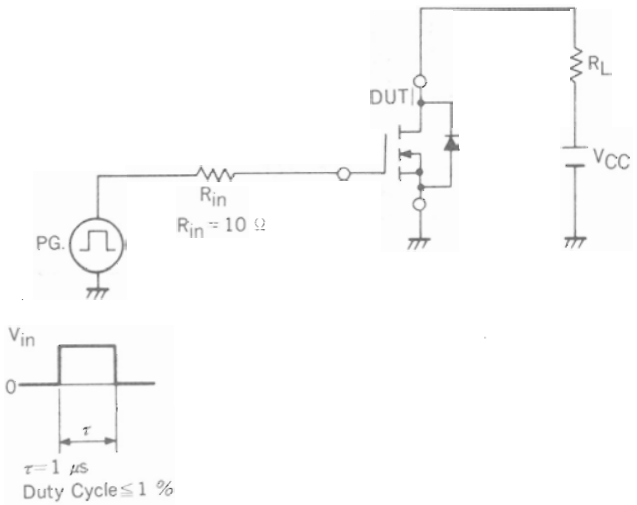


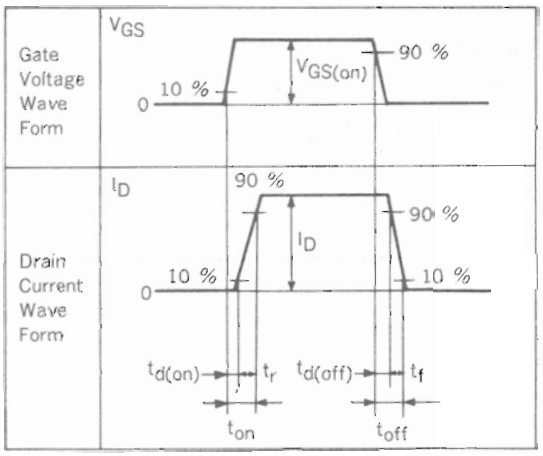






TURN-ON AND TURN-OFF TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK700

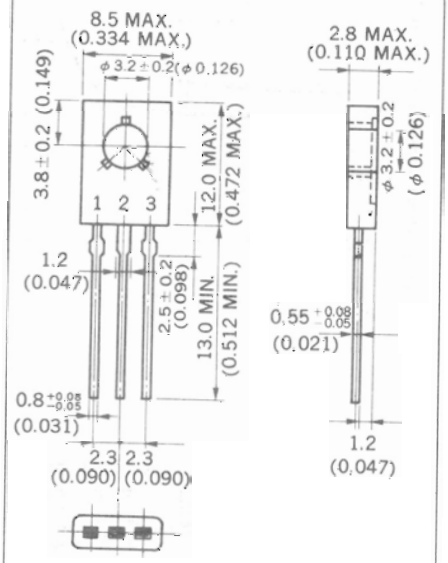
DESCRIPTION The 2SK700 is N-Channel MOS Field Effect Power Transistor designed for soleno id, motor and lamp driver.

FEATURES

- 4 V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Second Breakdown

NEW DEVICE

PACKAGE DIMENSIONS
in millimeters (inches)



1. Source
2. Drain connected to mounting plane
3. Gate

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation . . . . . 1.3 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	80	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±2	A
$I_{D(pulse)}$	Drain Current (pulse)*	±6	A

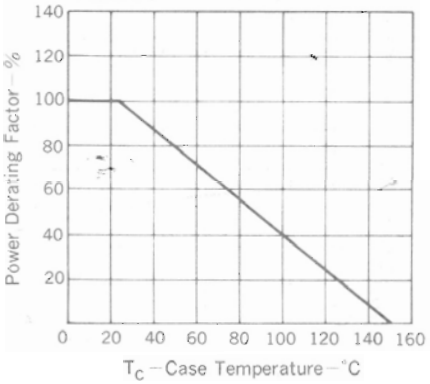
* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

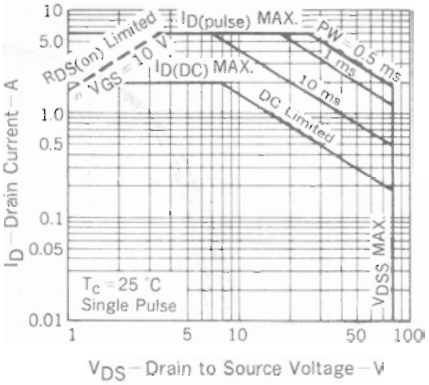
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.6	0.8	Ω	V_{GS} = 10 V, I_D = 1 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.8	1.0	Ω	V_{GS} = 4 V, I_D = 1 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = −1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	0.5			S	V_{DS} = 10 V, I_D = 1 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 80 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		200		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		70		pF	
C_{rss}	Reverse Transfer Capacitance		15		pF	
$t_{d(on)}$	Turn-On Delay Time		45		ns	I_D = 1 A, V_{CC} = 50 V R_L = 50 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		450		ns	
t_f	Fall Time		110		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

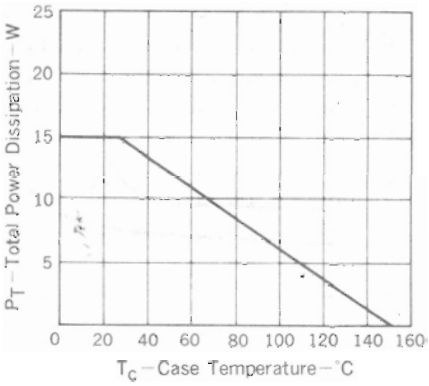
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



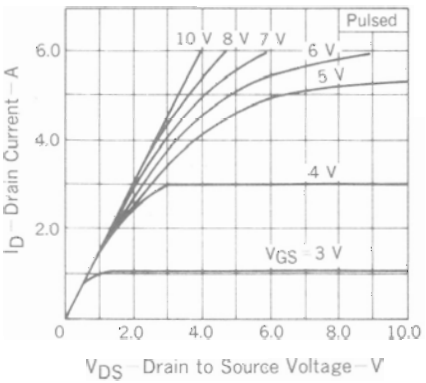
FORWARD BIAS SAFE OPERATING AREA



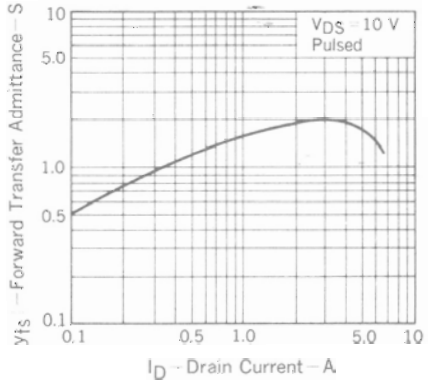
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



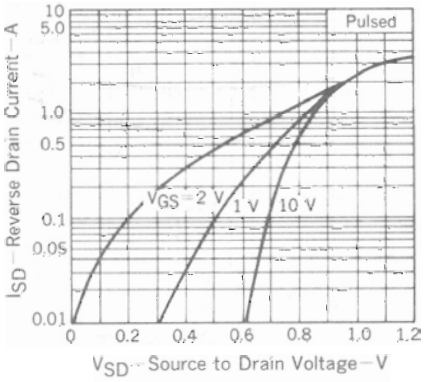
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



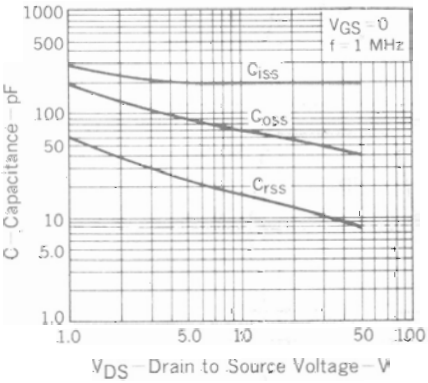
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



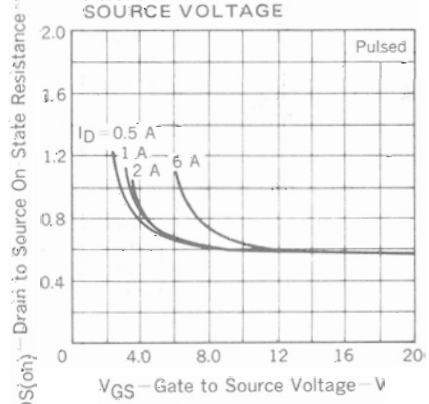
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



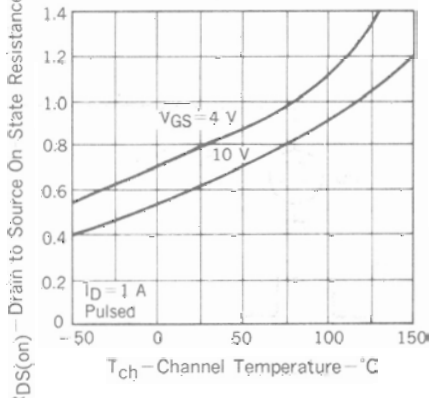
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

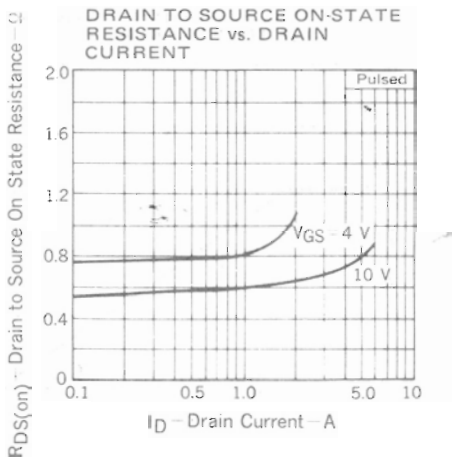


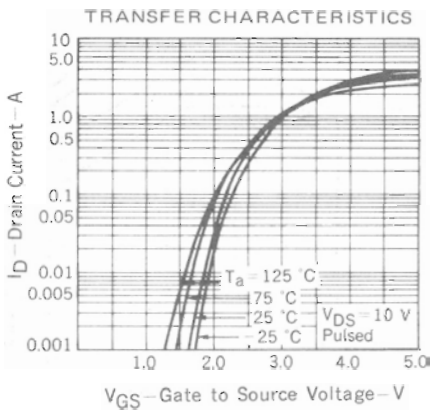
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

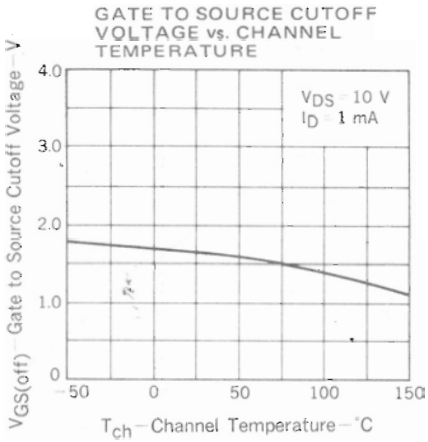


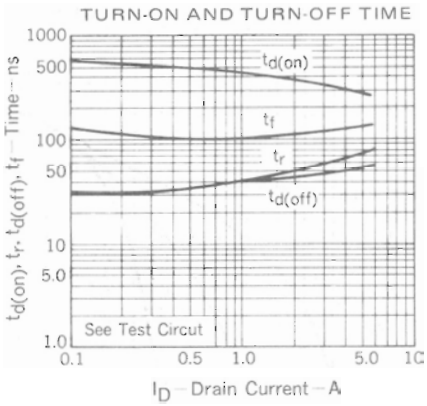
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



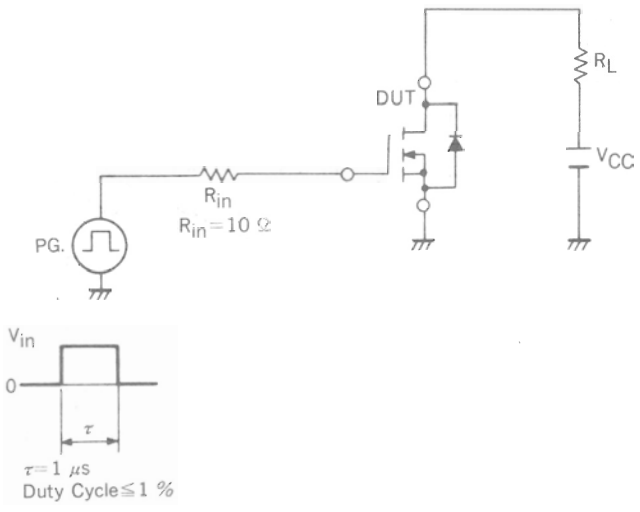


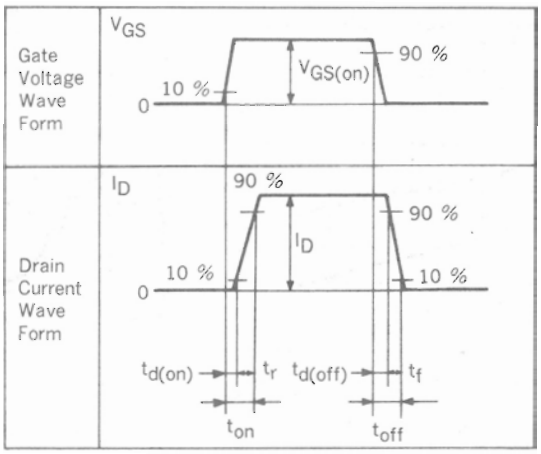






TURN-ON AND TURN-OFF TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK701

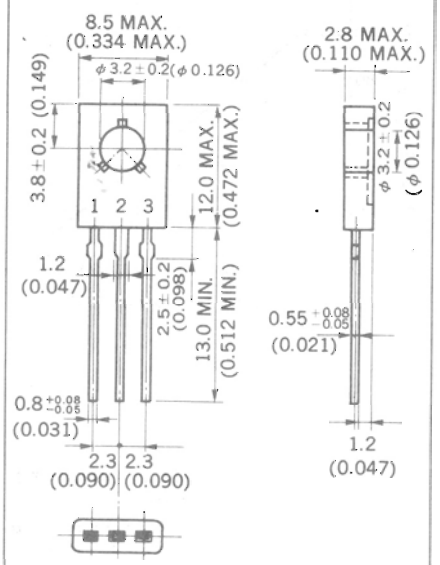
DESCRIPTION The 2SK701 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Second Breakdown

NEW DEVICE

PACKAGE DIMENSIONS
in millimeters (inches)



1. Source
2. Drain connected to mounting plane
3. Gate

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation . . . . . 1.3 W
- Total Power Dissipation (T_C = 25 °C) . . . . . 15 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{DSS} Drain to Source Voltage . . . . . 60 V
- V_{GSS} Gate to Source Voltage. . . . . ±20 V
- $I_{D(DC)}$ Drain Current (DC) . . . . . ±2 A
- $I_{D(pulse)}$ Drain Current (pulse)* . . . . . ±6 A

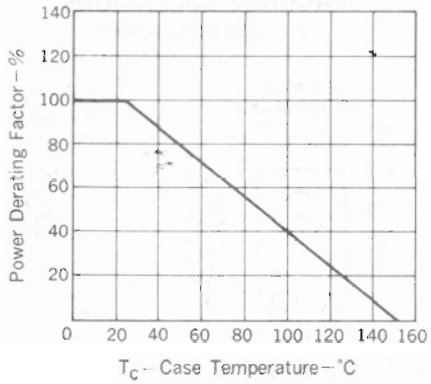
* PW ≤ 300 μs, Duty Cycle ≤ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

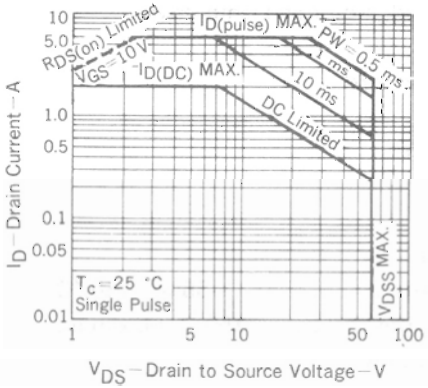
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.4	0.6	Ω	V_{GS} = 10 V, I_D = 1 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.6	0.85	Ω	V_{GS} = 4 V, I_D = 1 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	0.5			S	V_{DS} = 10 V, I_D = 1 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 60 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		200		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		70		pF	
C_{rss}	Reverse Transfer Capacitance		15		pF	
$t_{d(on)}$	Turn-On Delay Time		45		ns	I_D = 1 A, V_{CC} ≒ 50 V R_L = 50 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		450		ns	
t_f	Fall Time		110		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

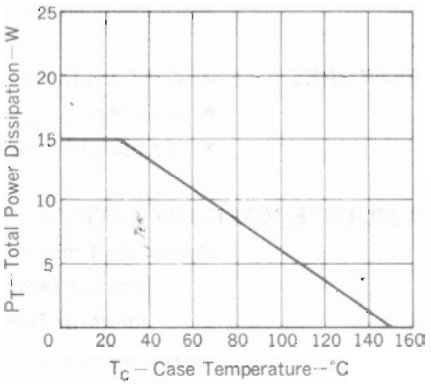
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



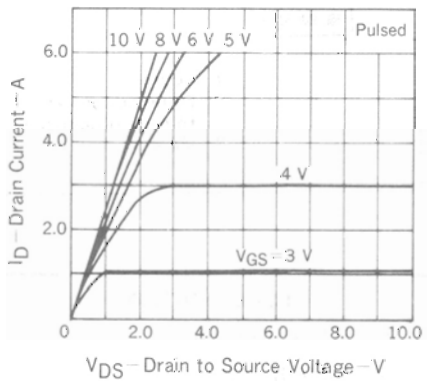
FORWARD BIAS SAFE OPERATING AREA



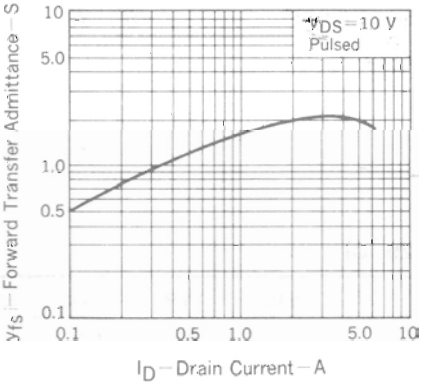
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



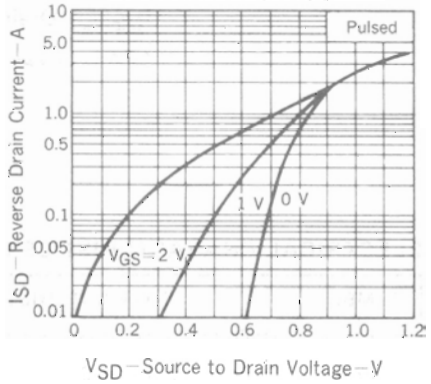
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



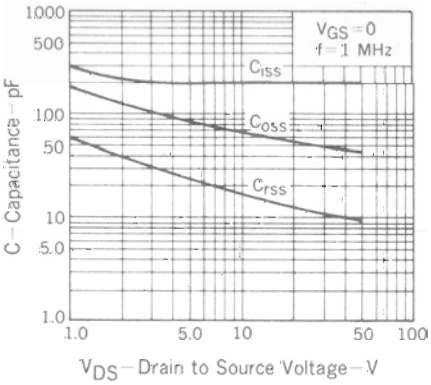
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



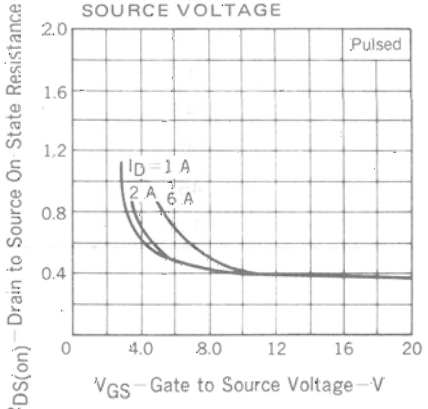
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



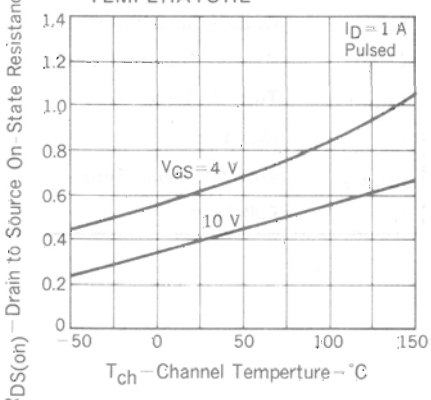
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



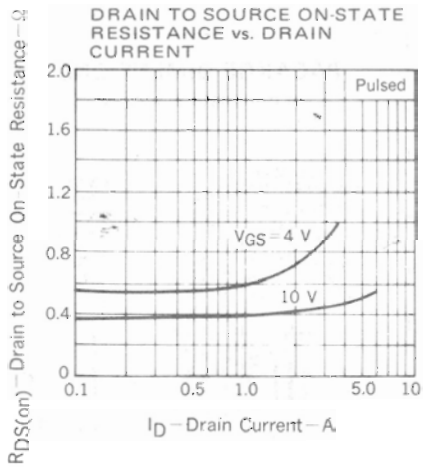
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



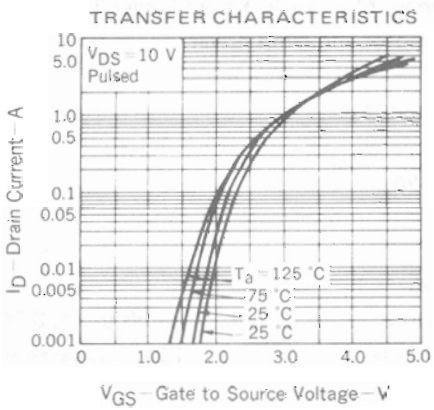
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



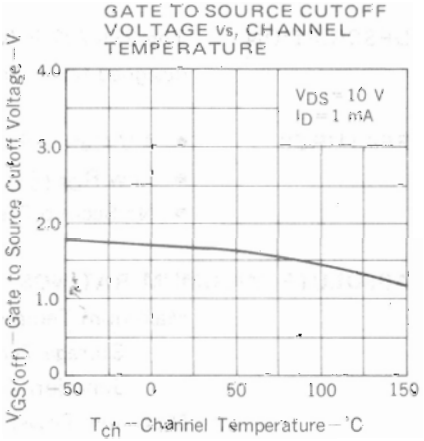
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



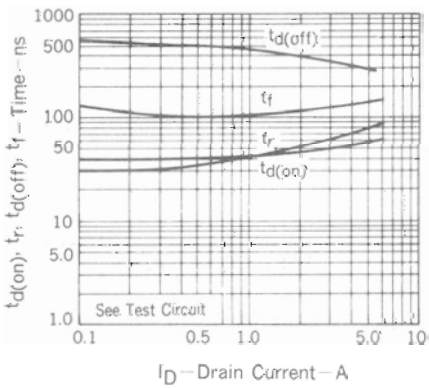
TRANSFER CHARACTERISTICS



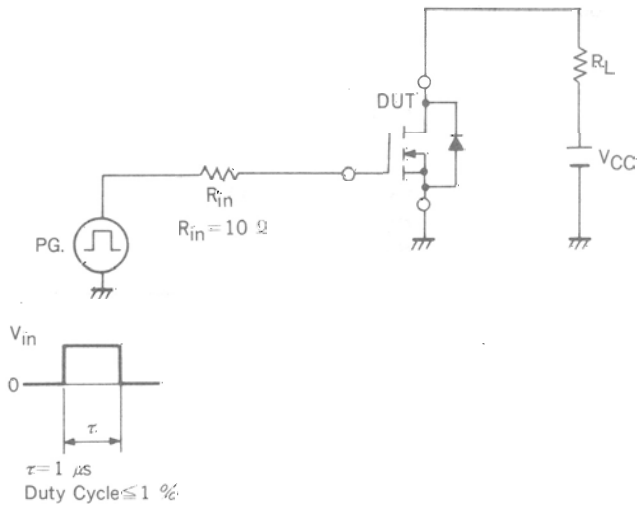
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

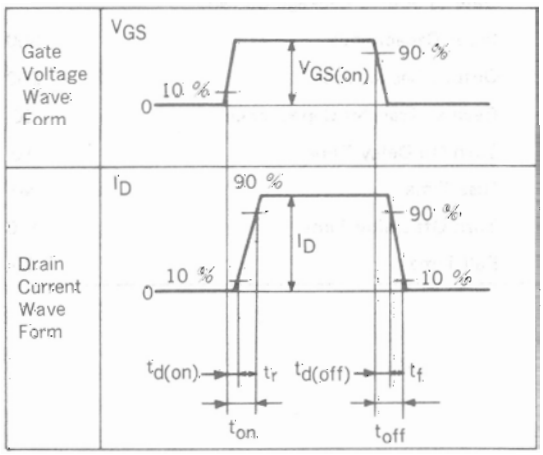


TURN-ON AND TURN-OFF TIME



TURN-ON AND TURN-OFF TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK702

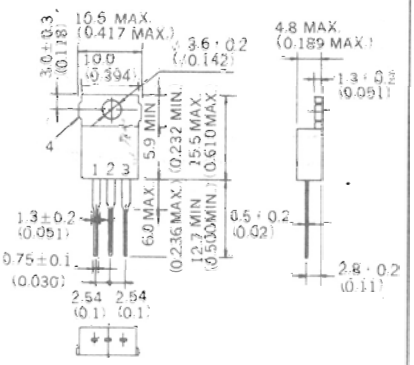
NEW DEVICE

DESCRIPTION The 2SK702 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Second Breakdown

PACAKGE DIMENSIONS
in millimeters (inches)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation . . . . . 1.5 W
- Total Power Dissipation (T_C = 25 °C) . . . 50 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{DSS} Drain to Source Voltage . . . . . 100 V
- V_{GSS} Gate to Source Voltage . . . . . ±20 V
- $I_{D(DC)}$ Drain Current (DC) . . . . . ±5 A
- $I_{D(pulse)}$ Drain Current (pulse)* . . . . . ±20 A

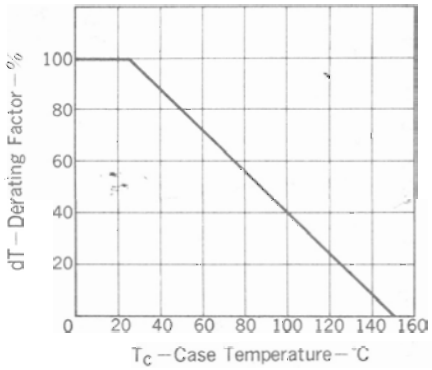
* PW ≦ 300 μs, Duty Cycle ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

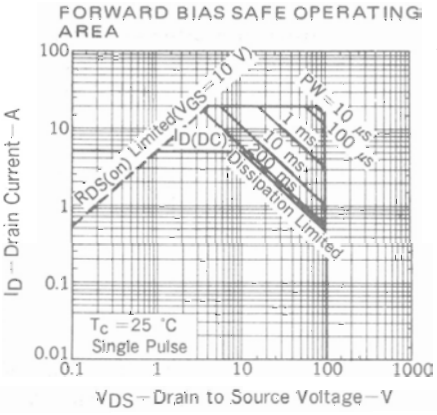
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.20	0.45	Ω	V_{GS} = 10 V, I_D = 5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.25	0.50	Ω	V_{GS} = 4 V, I_D = 5 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	4			S	V_{DS} = 10 V, I_D = 3 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		900		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		250		pF	
C_{rss}	Reverse Transfer Capacitance		50		pF	
$t_{d(on)}$	Turn On Delay Time		10		ns	I_D = 3 A, V_{CC} ≒ 50 V R_L = 17 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn Off Delay Time		110		ns	
t_f	Fall Time		30		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

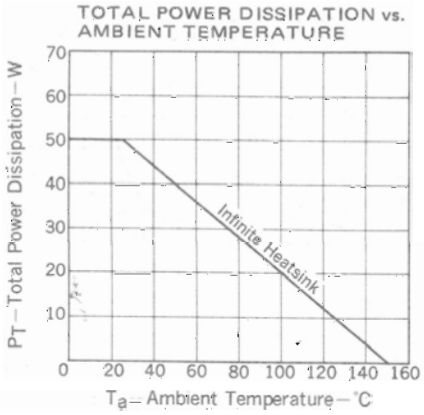
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



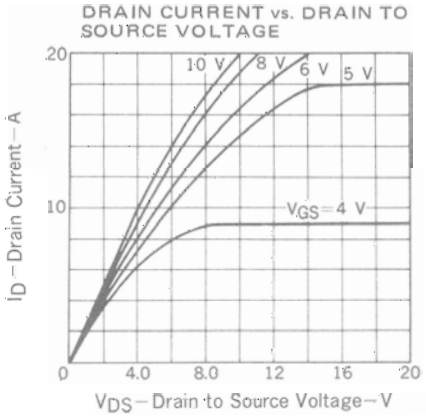
FORWARD BIAS SAFE OPERATING AREA



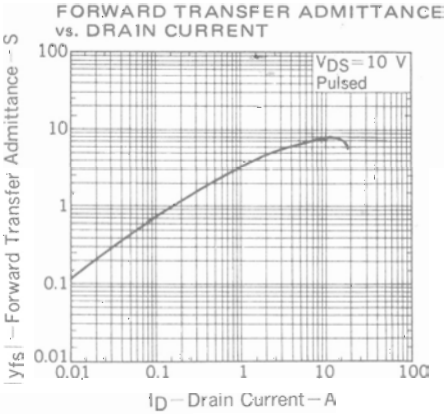
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



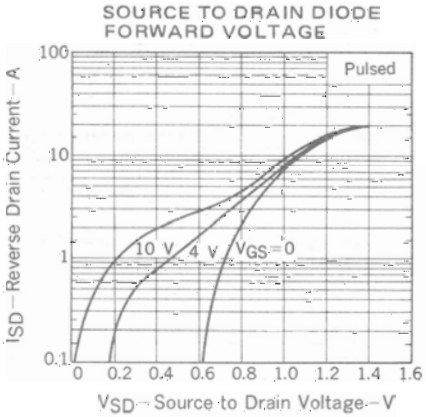
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



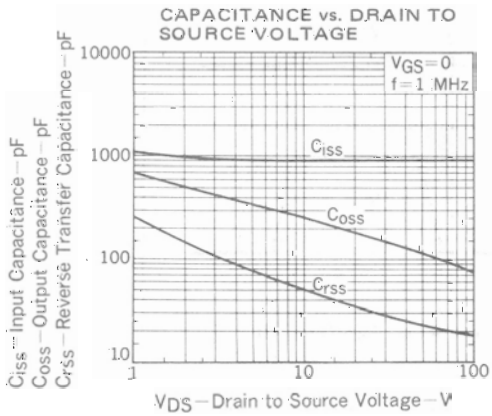
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



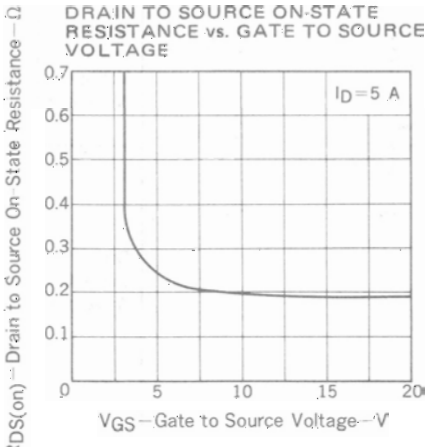
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



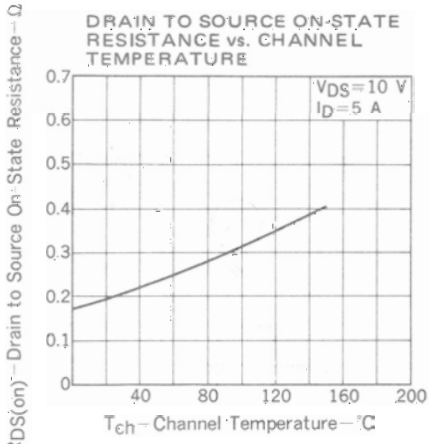
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



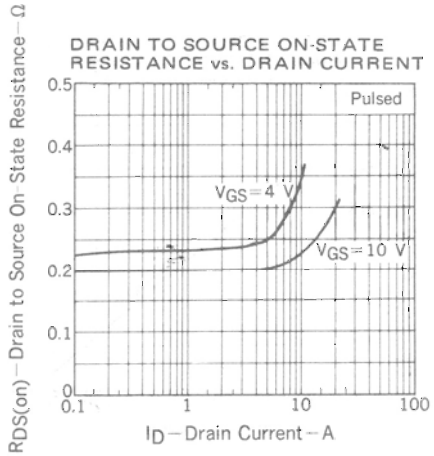
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



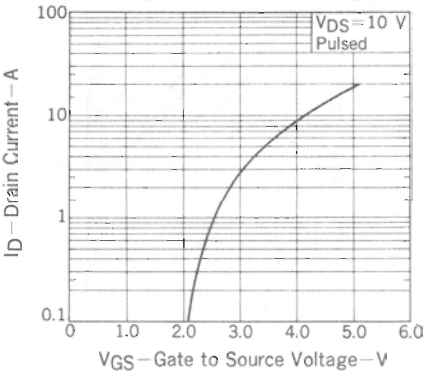
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



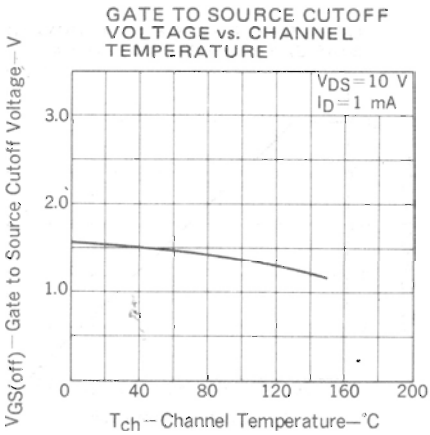
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



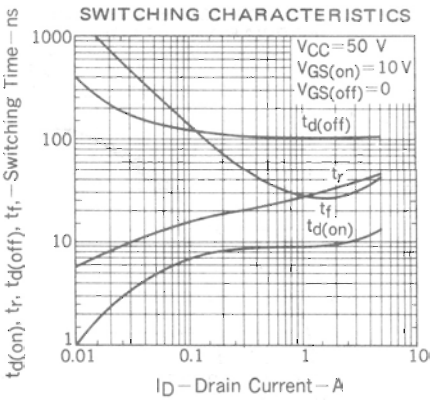
TRANSFER CHARACTERISTIC



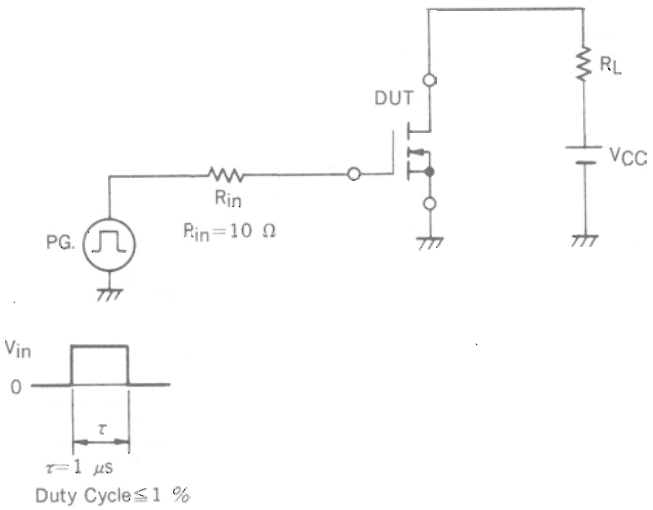
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

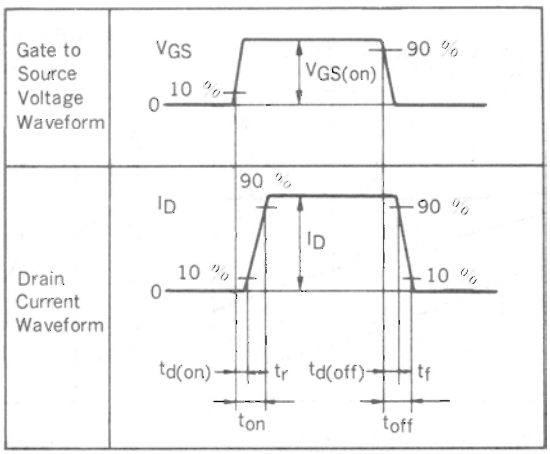


SWITCHING CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK703

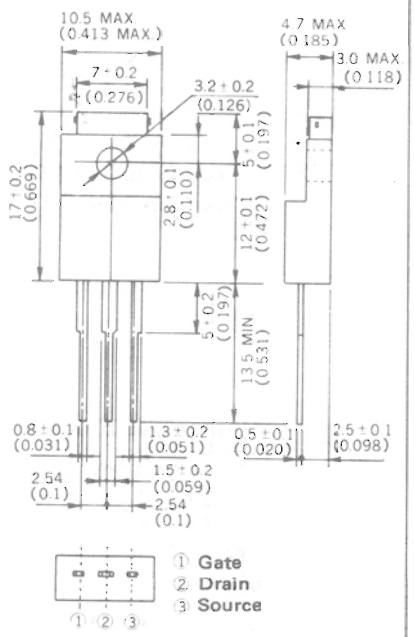
NEW DEVICE

DESCRIPTION The 2SK703 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Second Breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	–55 to +150	°C
Junction Temperature	150 °C Maximum	

Maximum Power Dissipations

Total Power Dissipation	2.0	W
Total Power Dissipation (T_C = 25 °C)	35	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±5	A
$I_{D(pulse)}$	Drain Current (pulse)*	±20	A

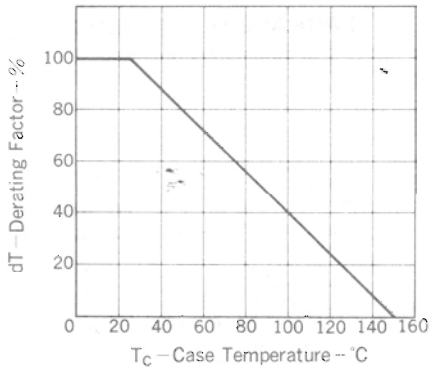
*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

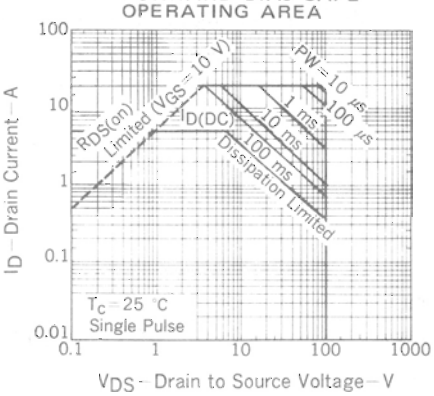
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.20	0.45	Ω	V_{GS} = 10 V, I_D = 5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.25	0.50	Ω	V_{GS} = 4 V, I_D = 5 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	4.0			S	V_{DS} = 10 V, I_D = 3 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		900		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		250		pF	
C_{rss}	Reverse Transfer Capacitance		45		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	I_D = 3 A, V_{CC} ≒ 50 V R_L = 17 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		110		ns	
t_f	Fall Time		30		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

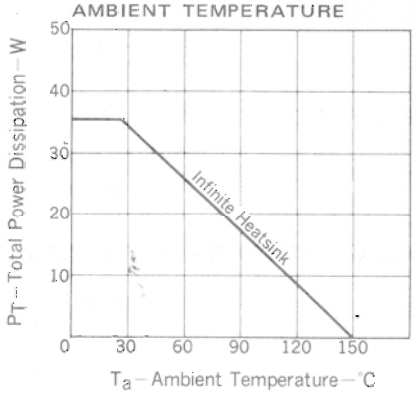
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



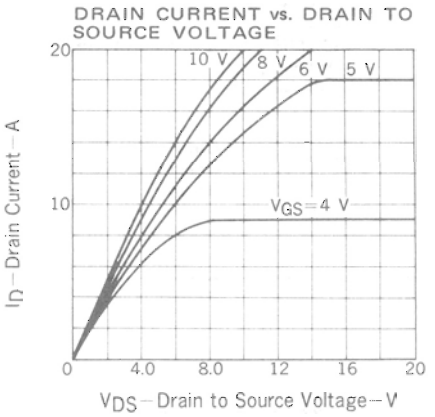
FORWARD BIAS SAFE OPERATING AREA



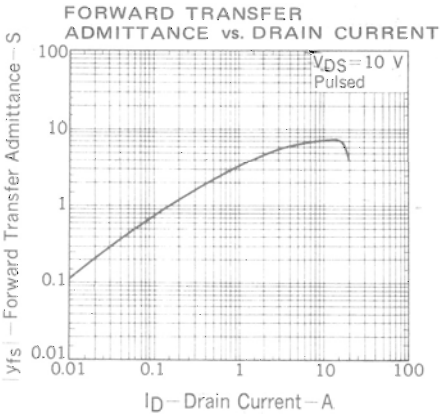
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



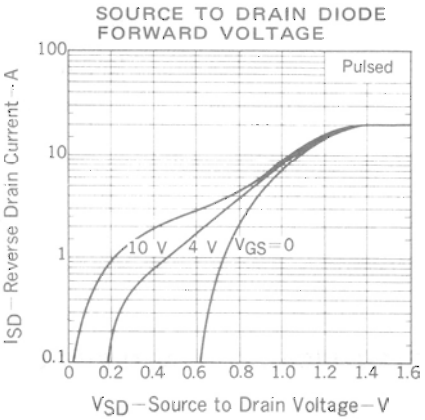
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



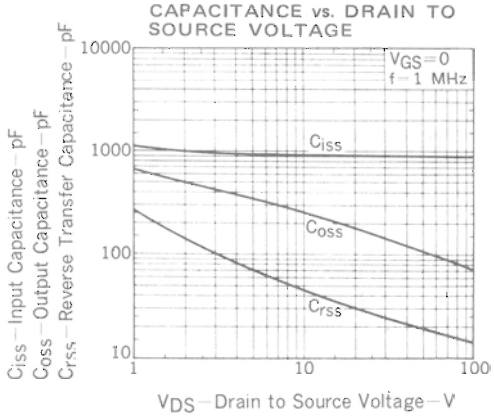
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



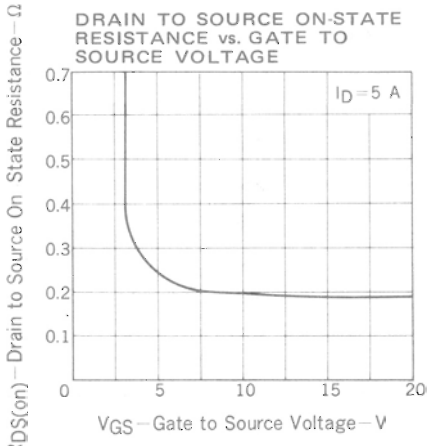
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



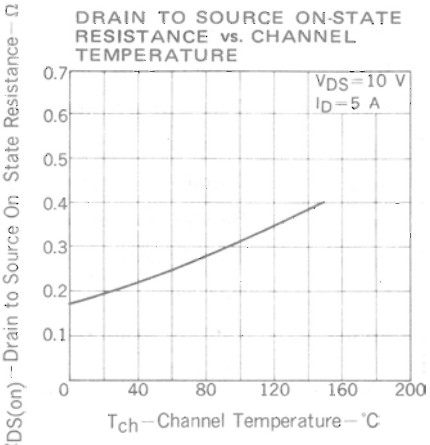
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

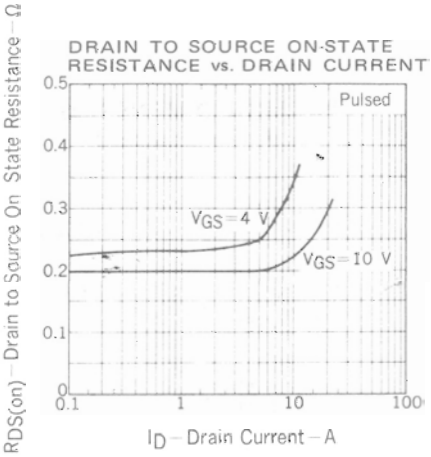


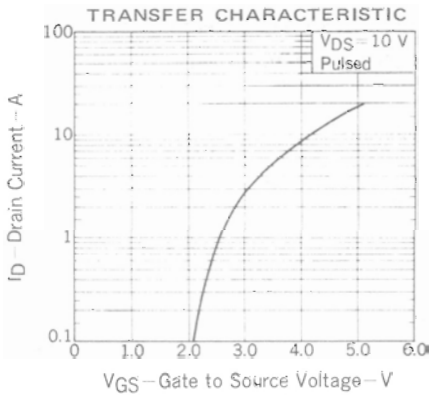
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

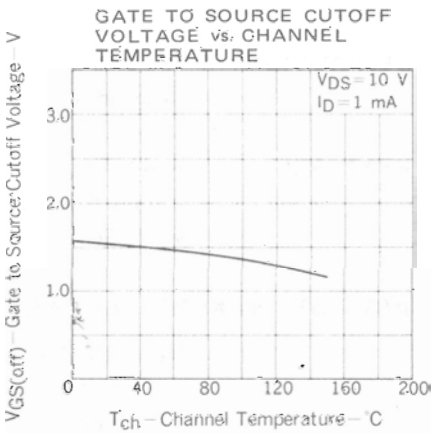


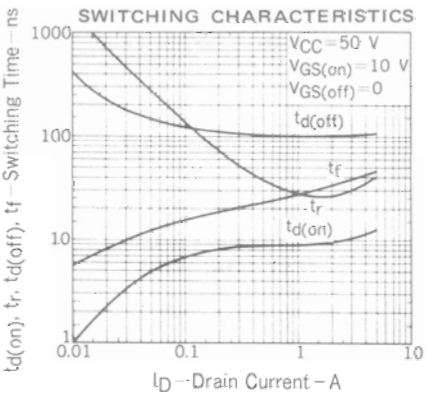
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



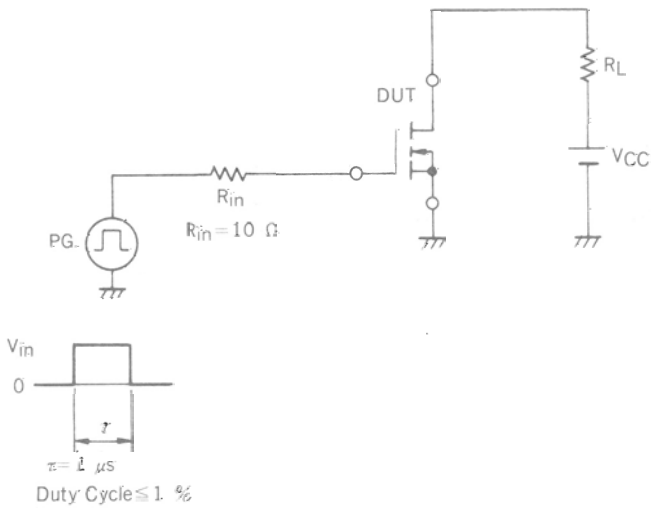


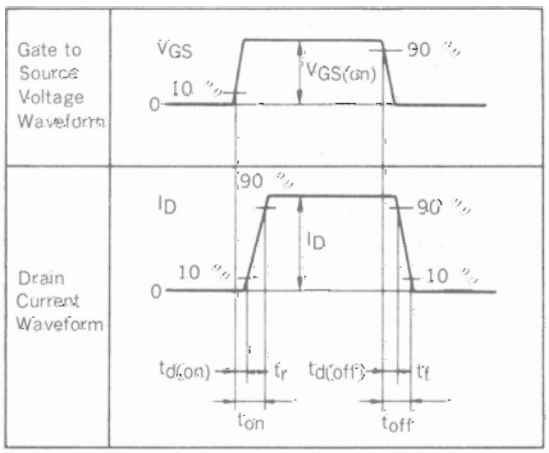






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK704

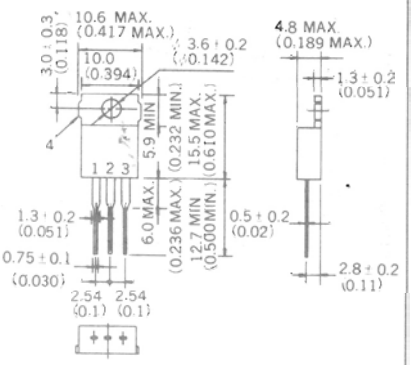
NEW DEVICE

DESCRIPTION The 2SK704 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Second Breakdown

PACAKGE DIMENSIONS
in millimeters (inches)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation . . . . . 1.5 W
- Total Power Dissipation (T_C = 25 °C) . . . 50 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{DSS} Drain to Source Voltage . . . . . 60 V
- V_{GSS} Gate to Source Voltage . . . . . ±20 V
- $I_{D(DC)}$ Drain Current (DC) . . . . . ±5 A
- $I_{D(pulse)}$ Drain Current (pulse)* . . . . . ±20 A

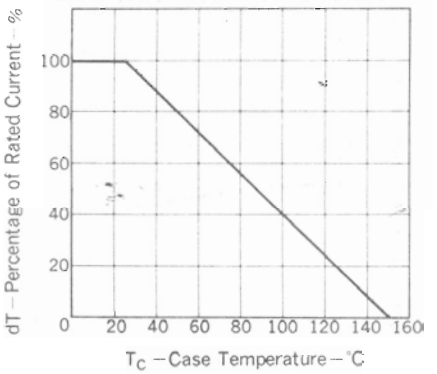
*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

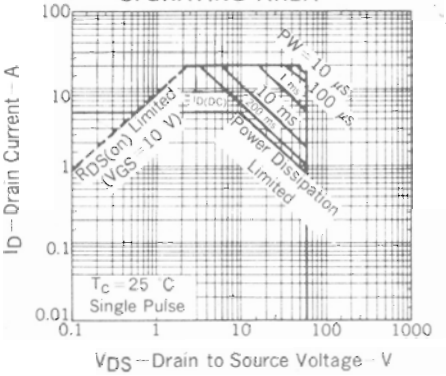
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.11	0.25	Ω	V_{GS} = 10 V, I_D = 5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.17	0.30	Ω	V_{GS} = 4 V, I_D = 5 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	4.0			S	V_{DS} = 10 V, I_D = 3 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 60 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		900		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		350		pF	
C_{rss}	Reverse Transfer Capacitance		100		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	I_D = 3 A, V_{CC} ≒ 10 V R_L = 17 Ω R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		110		ns	
t_f	Fall Time		30		ns	

TYPICAL CARACTERISTICS (T_a = 25 °C)

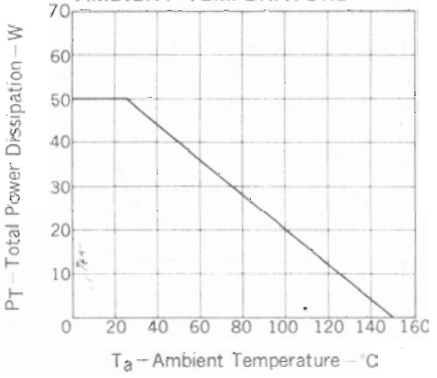
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



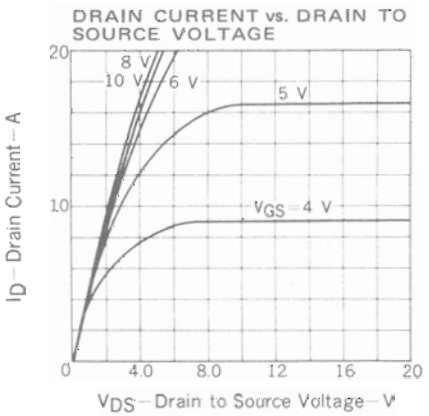
FORWARD BIAS SAFE OPERATING AREA



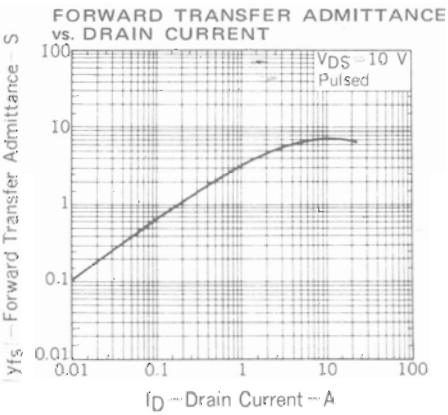
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



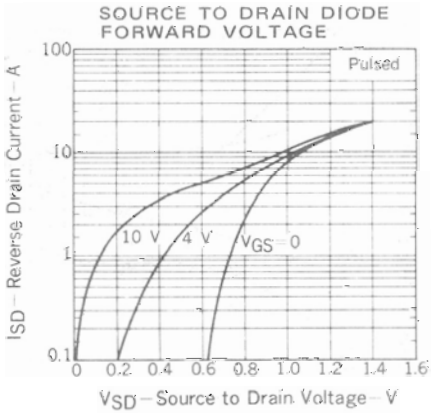
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



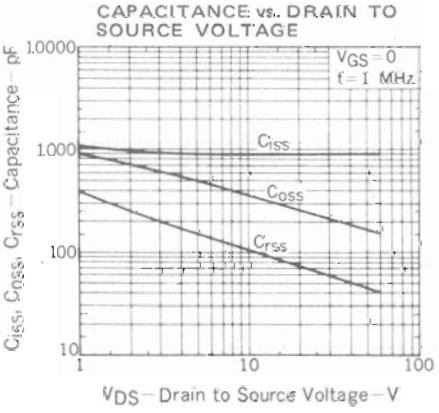
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



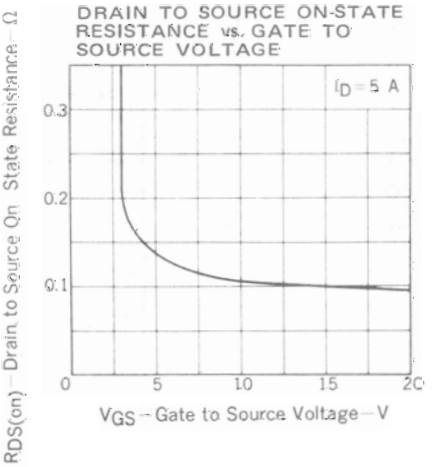
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



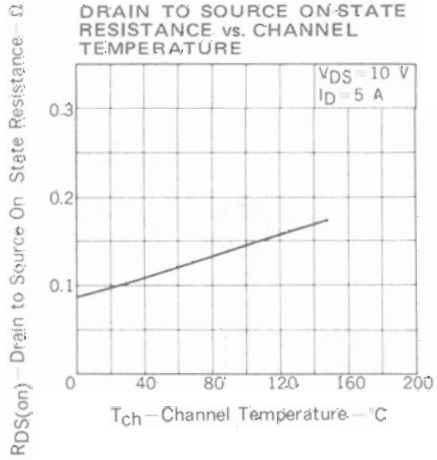
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

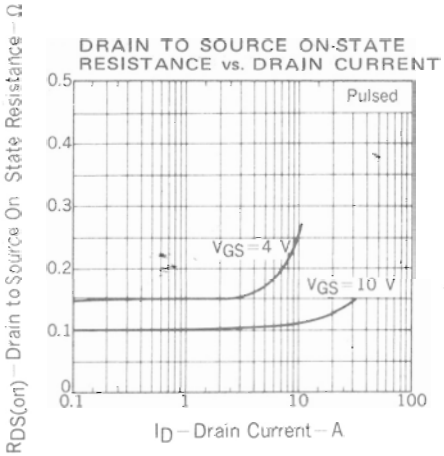


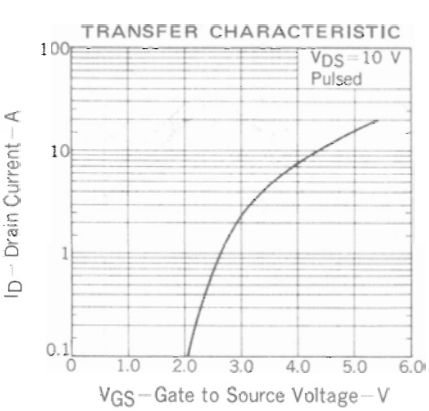
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

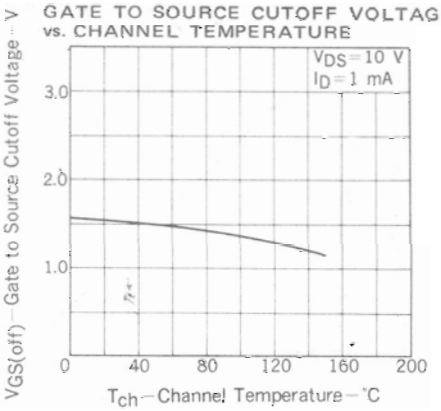


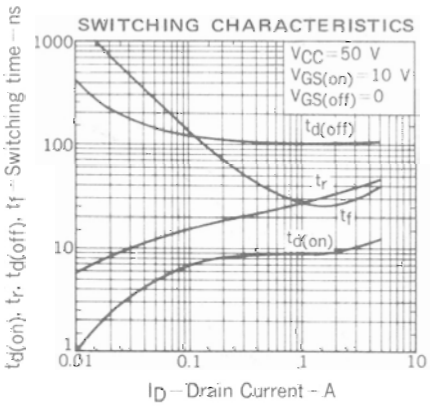
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



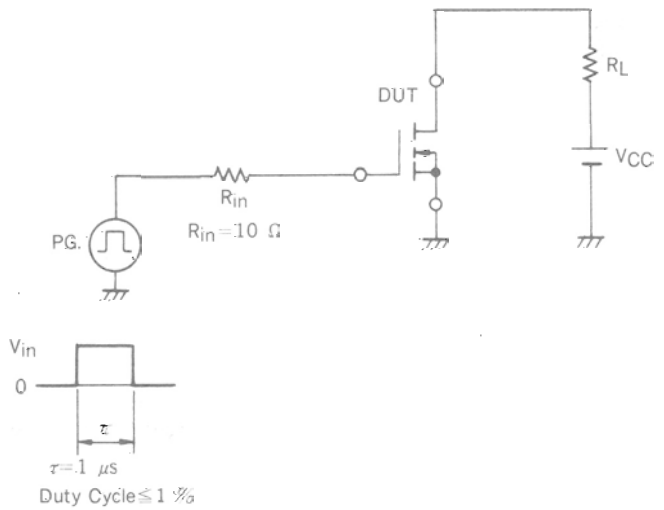


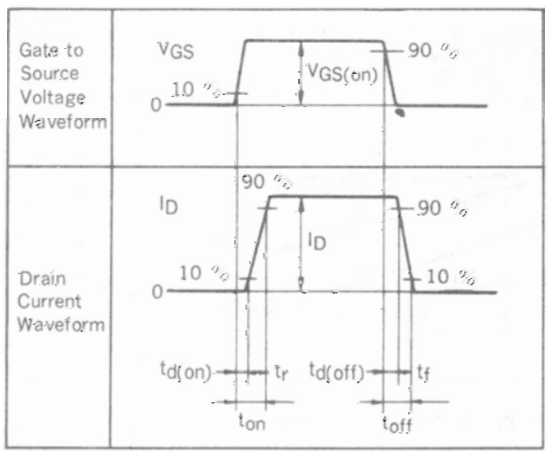






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK705

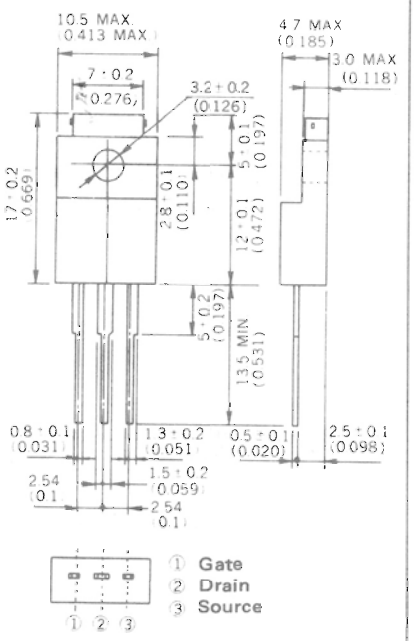
NEW DEVICE

DESCRIPTION The 2SK705 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Secondary Breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

	Total Power Dissipation (T_a = 25 °C) . . .	2.0	W
	Total Power Dissipation (T_c = 25 °C) . . .	35	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	60	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±5	A
$I_{D(pulse)}$	Drain Current (pulse)*	±20	A

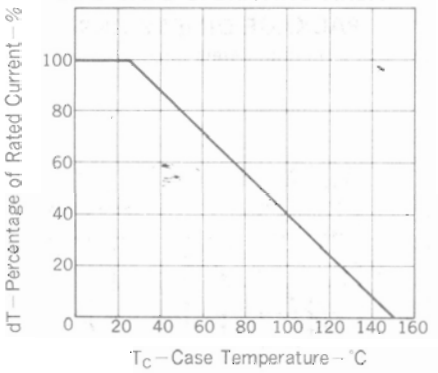
*PW ≦ 300 μs, Duty Cycles ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

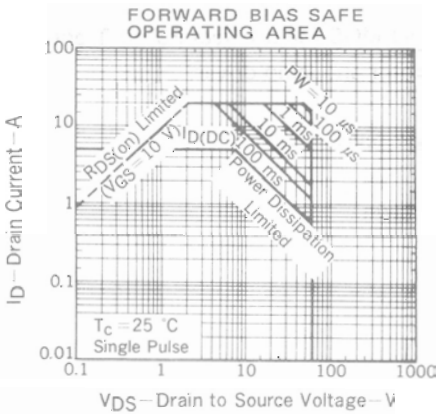
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.11	0.25	Ω	V_{GS} = 10 V, I_D = 5 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.17	0.30	Ω	V_{GS} = 4 V, I_D = 5 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	5.0			S	V_{DS} = 10 V, I_D = 3 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 60 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		900		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		350		pF	
C_{rss}	Reverse Transfer Capacitance		100		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	I_D = 3 A, V_{CC} ≒ 50 V R_L = 17 Ω, $V_{GS(on)}$ = 10 V R_{in} = 10 Ω
t_r	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		110		ns	
t_f	Fall Time		30		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

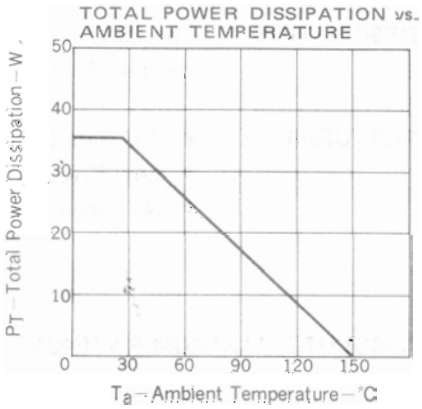
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



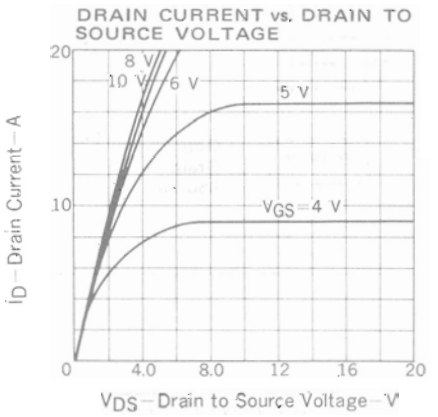
FORWARD BIAS SAFE OPERATING AREA



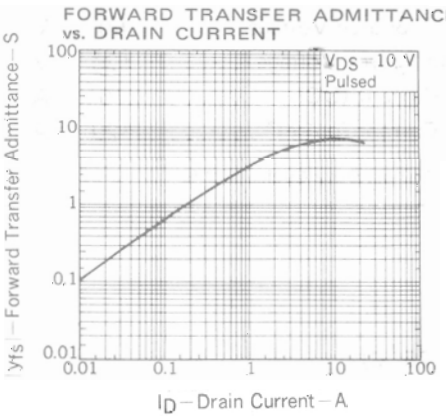
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



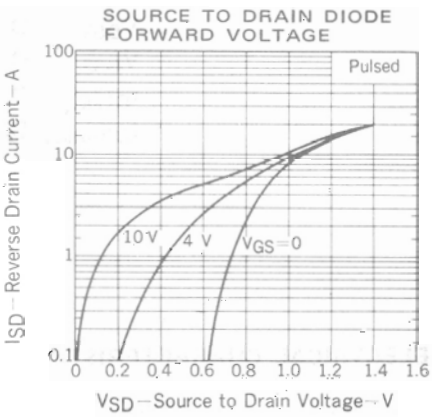
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



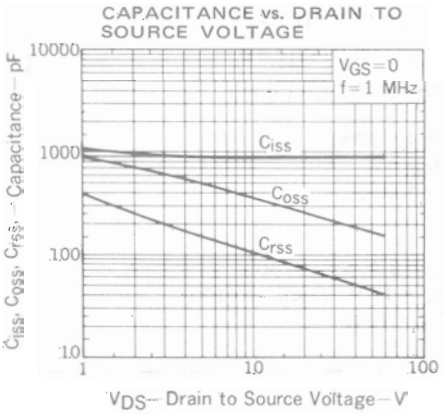
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



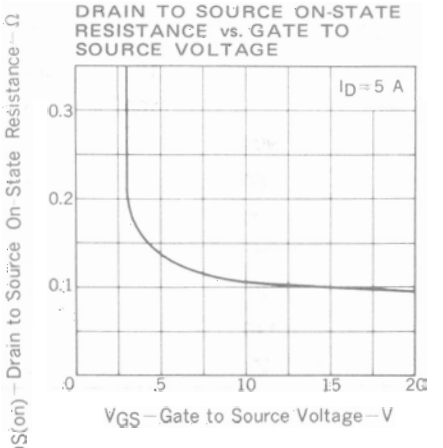
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



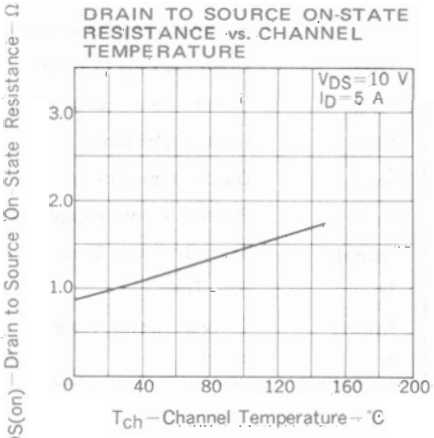
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

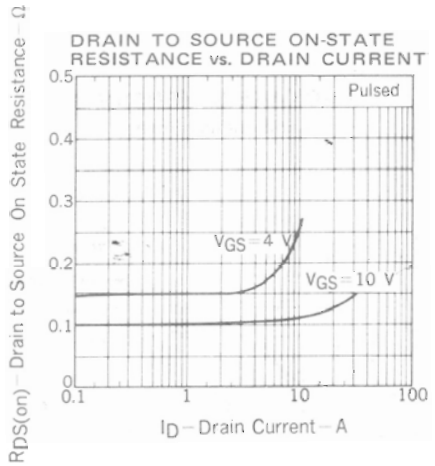


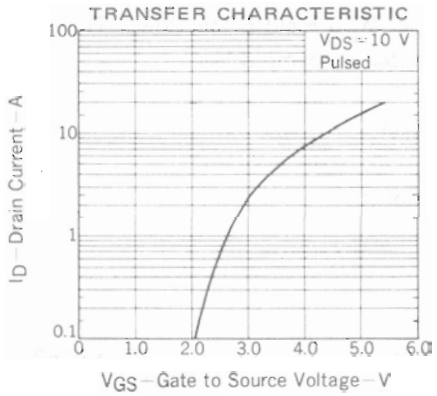
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

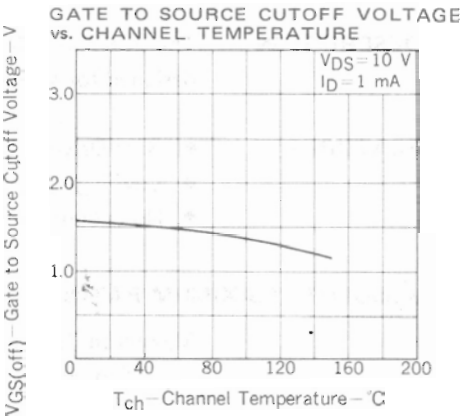


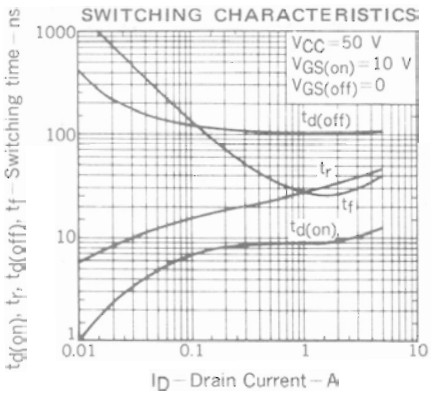
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



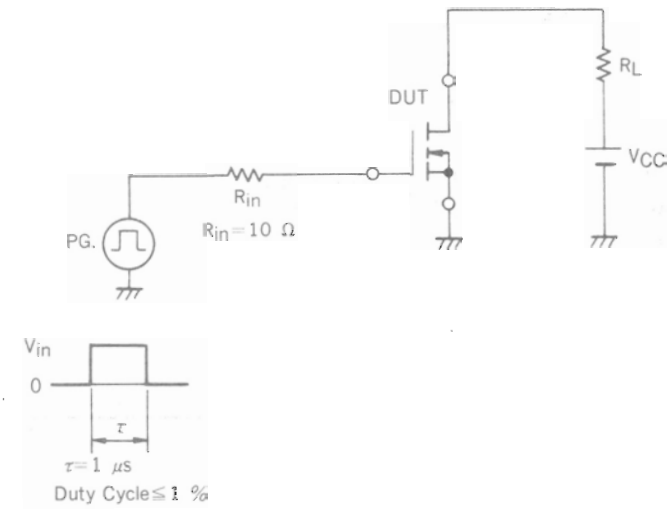


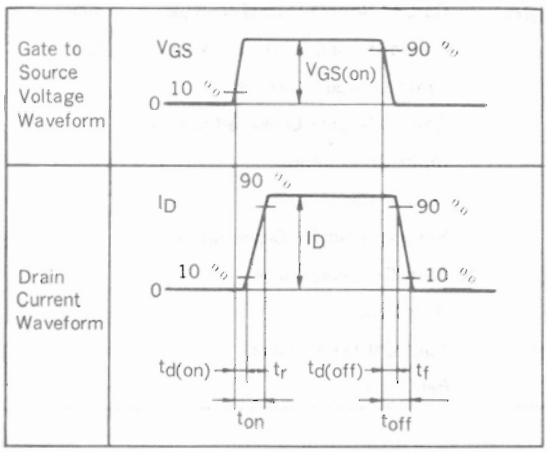






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK736

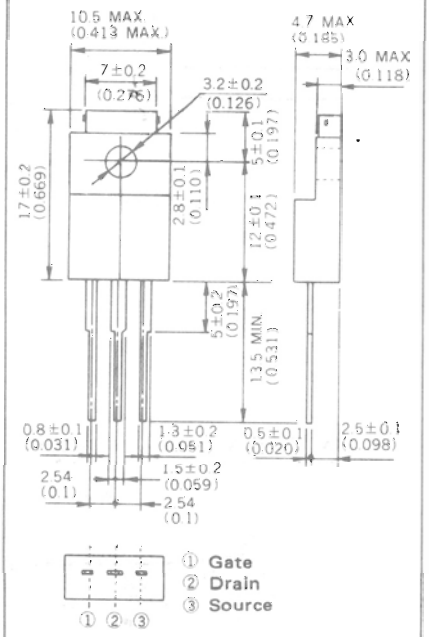
NEW DEVICE

DESCRIPTION The 2SK736 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Secondary Breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . 2.0 W
- Total Power Dissipation (T_c = 25 °C) . . . 35 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{DSS} Drain to Source Voltage . . . . . 100 V
- V_{GSS} Gate to Source Voltage . . . . . ±20 V
- $I_{D(DC)}$ Drain Current (DC) . . . . . ±15 A
- $I_{D(pulse)}$ Drain Current (pulse)* . . . . . ±60 A

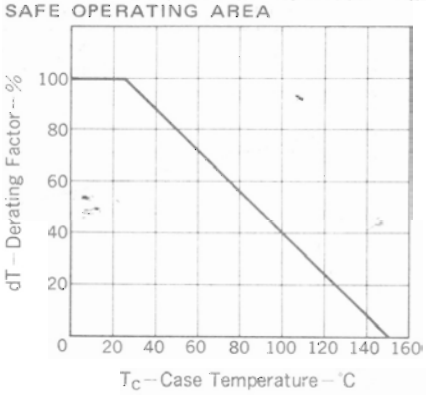
*PW ≦ 300 μs, Duty Cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

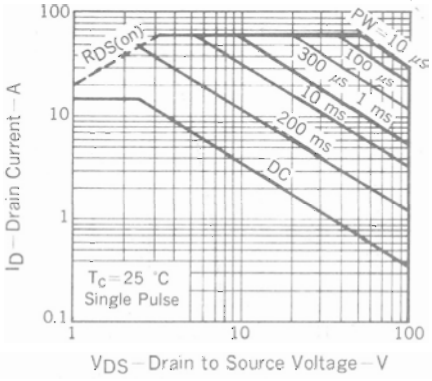
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance			0.08	Ω	V_{GS} = 10 V, I_D = 6 A
$R_{DS(on)}$	Drain to Source On-State Resistance			0.10	Ω	V_{GS} = 4 V, I_D = 6 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	5.0			S	V_{DS} = 10 V, I_D = 6 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		2400		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		600		pF	
C_{rss}	Reverse Transfer Capacitance		100		pF	
$t_{d(on)}$	Turn On Delay Time		15		ns	I_D = 6 A, V_{CC} ≒ 50 V R_L = 5 Ω R_{in} = 10 Ω
t_r	Rise Time		70		ns	
$t_{d(off)}$	Turn Off Delay Time		250		ns	
t_f	Fall Time		160		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

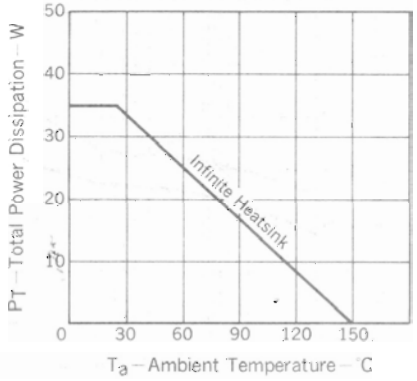
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



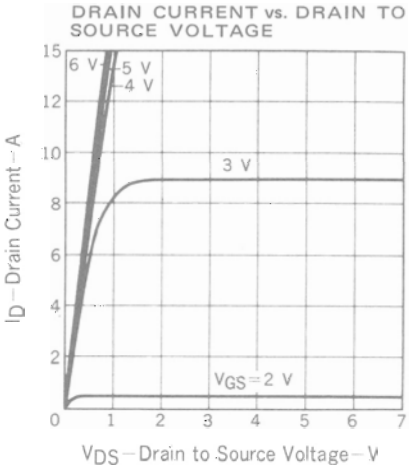
FORWARD BIAS SAFE OPERATING AREA



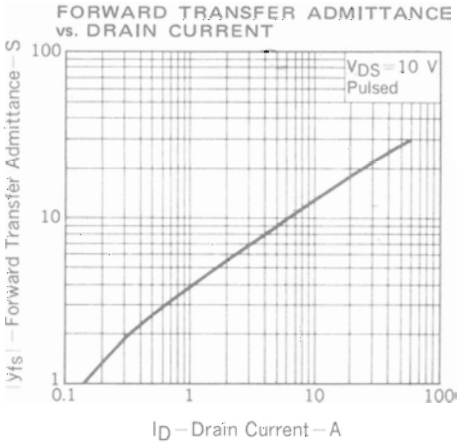
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



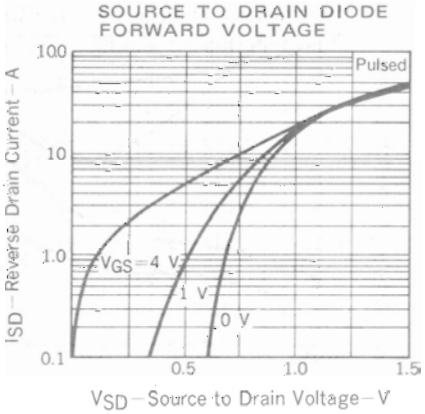
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



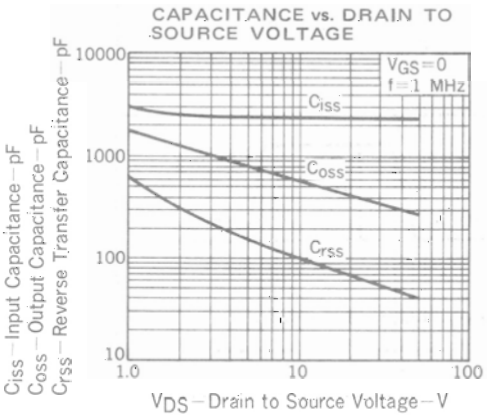
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



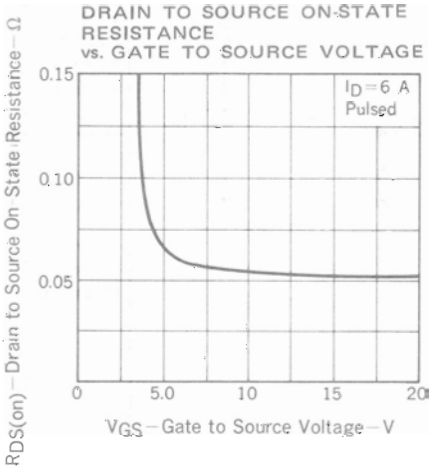
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



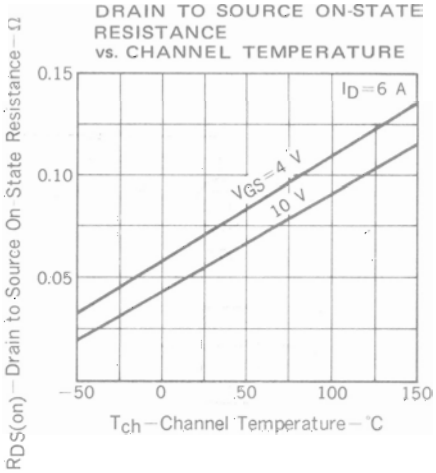
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



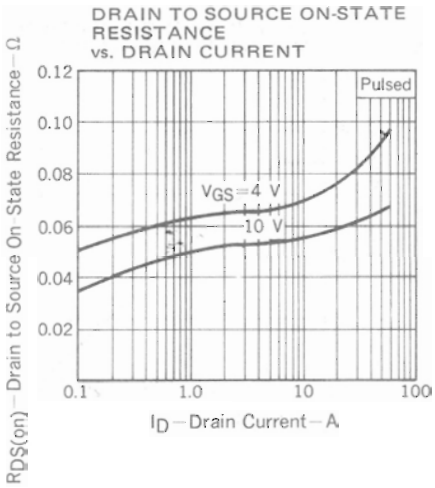
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



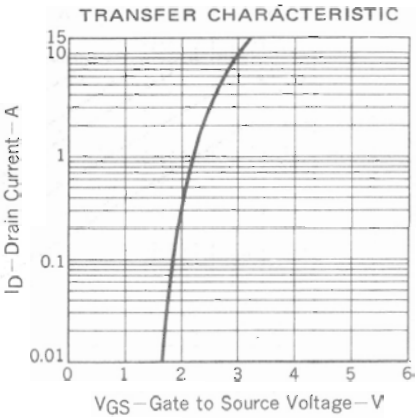
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



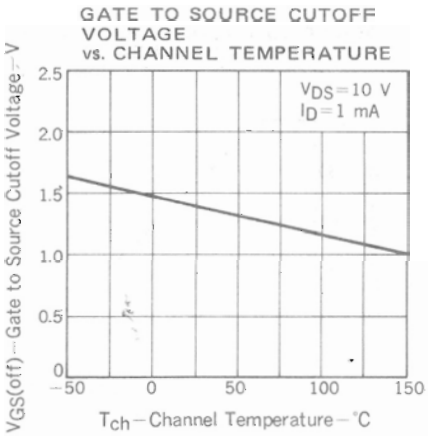
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



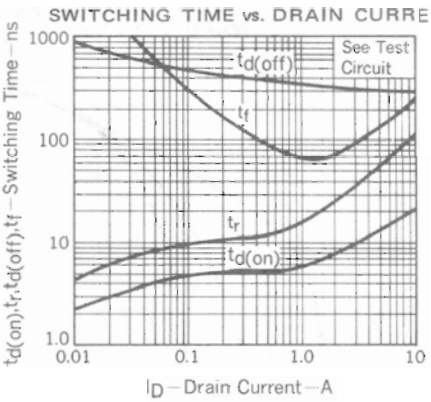
TRANSFER CHARACTERISTIC



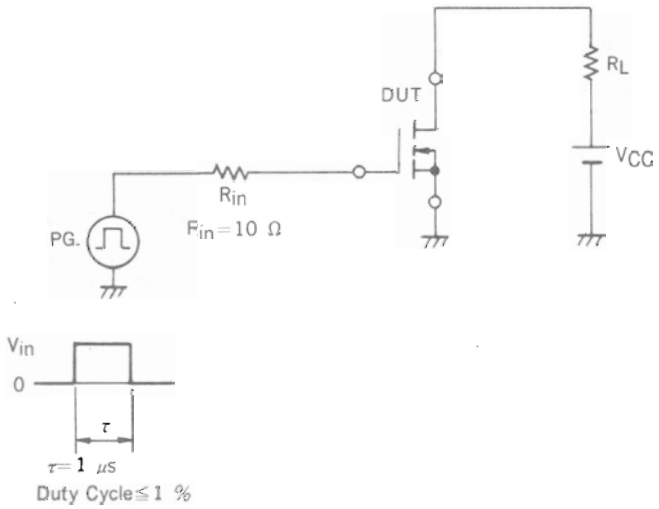
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

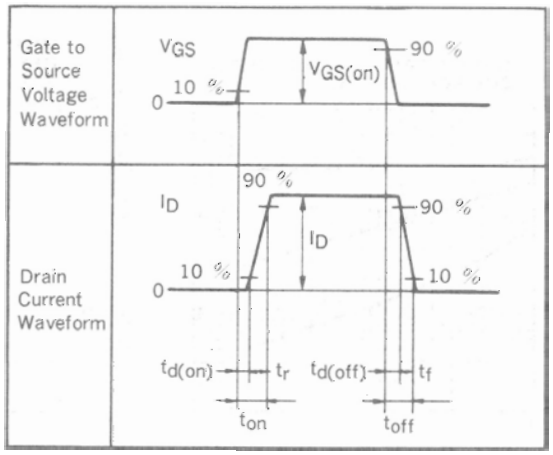


SWITCHING TIME vs. DRAIN CURRENT



SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

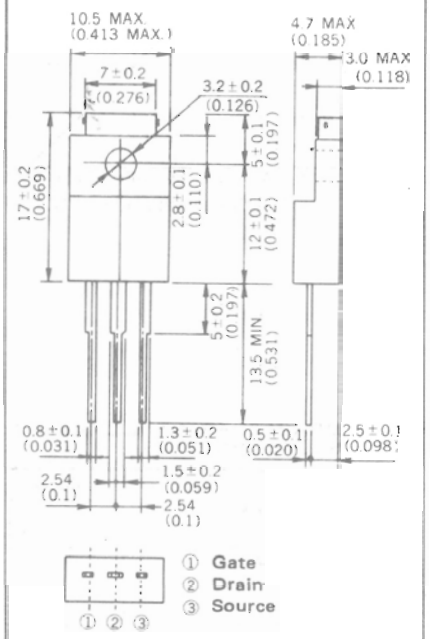
2SK737

DESCRIPTION The 2SK737 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4V Gate Drive — Logic level —
- Low $R_{DS(on)}$
- No Secondary Breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipations

- Total Power Dissipation (T_a = 25 °C) . . . 2.0 W
- Total Power Dissipation (T_c = 25 °C) . . . 35 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{DSS} Drain to Source Voltage . . . . 100 V
- V_{GSS} Gate to Source Voltage . . . . . ±20 V
- $I_{D(DC)}$ Drain Current (DC) . . . . . ±12 A
- $I_{D(pulse)}$ Drain Current (pulse)* . . . . . ±60 A

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

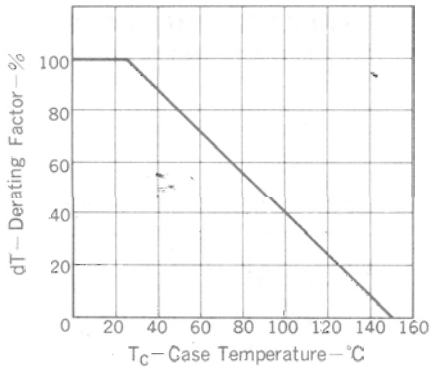
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance			0.15	Ω	V_{GS} = 10 V, I_D = 6 A
$R_{DS(on)}$	Drain to Source On-State Resistance			0.20	Ω	V_{GS} = 4 V, I_D = 6 A
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	5.0			S	V_{DS} = 10 V, I_D = 6 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 100 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20V, V_{DS} = 0
C_{iss}	Input Capacitance		1600		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		500		pF	
C_{rss}	Reverse Transfer Capacitance		150		pF	
$t_{d(on)}$	Turn On Delay Time		15		ns	I_D = 6 A, V_{CC} ≒ 50 V R_L = 5 Ω R_{in} = 10 Ω
t_r	Rise Time		60		ns	
$t_{d(off)}$	Turn Off Delay Time		100		ns	
t_f	Fall Time		50		ns	

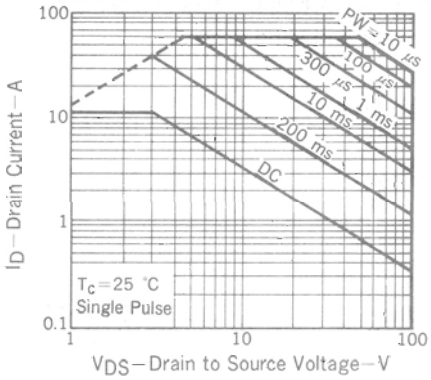
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

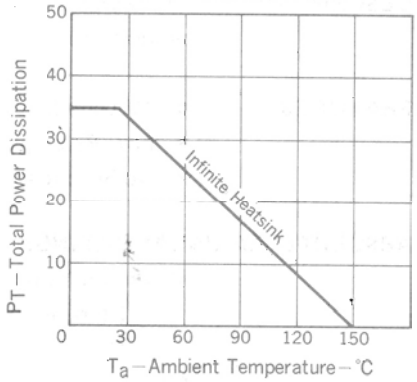
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



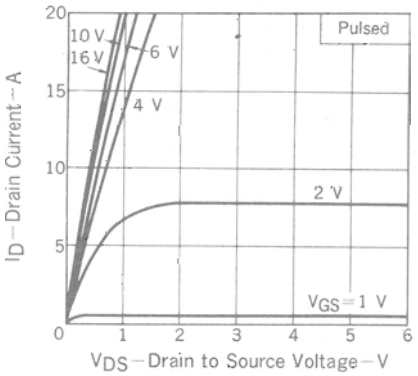
FORWARD BIAS SAFE OPERATING AREA



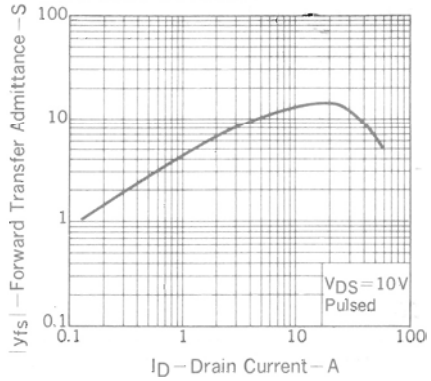
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



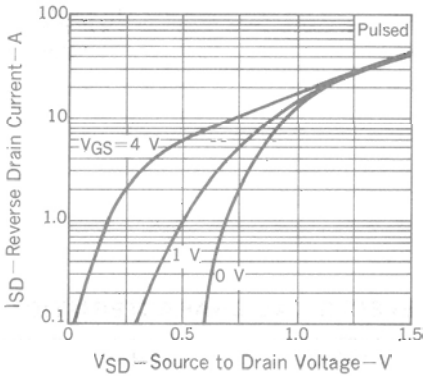
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



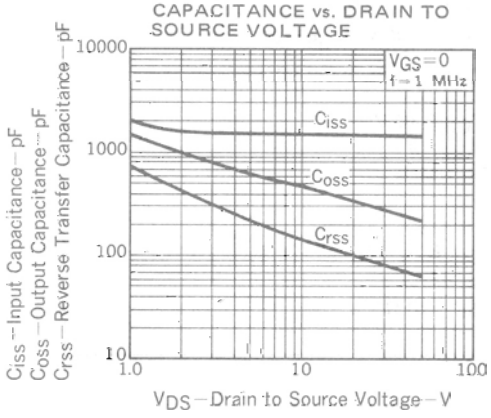
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



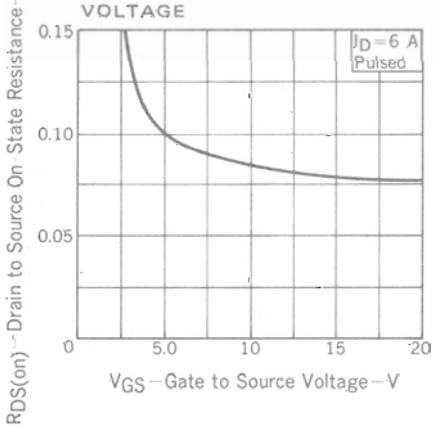
SOURCE TO DRAIN BODY DIODE FORWARD VOLTAGE



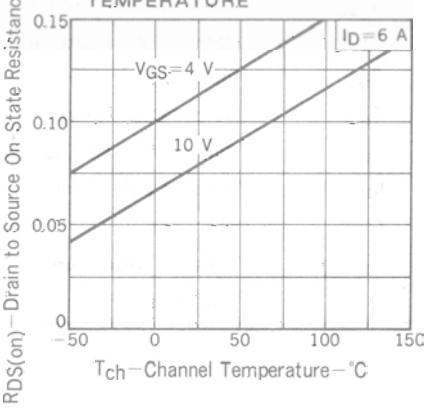
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

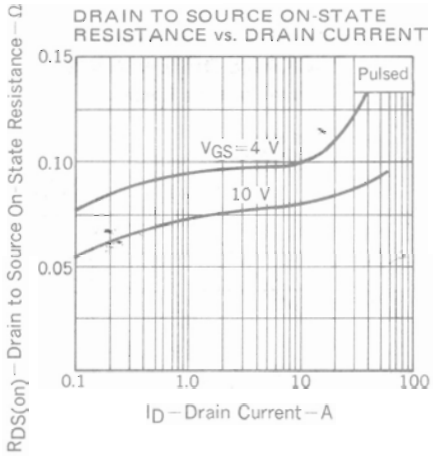


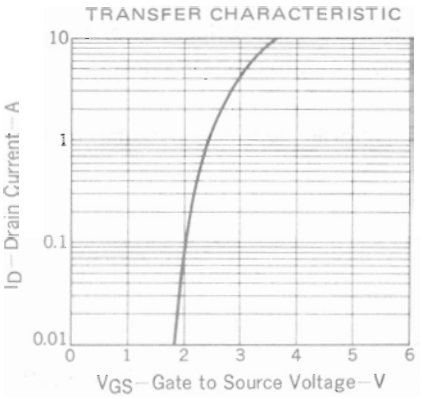
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

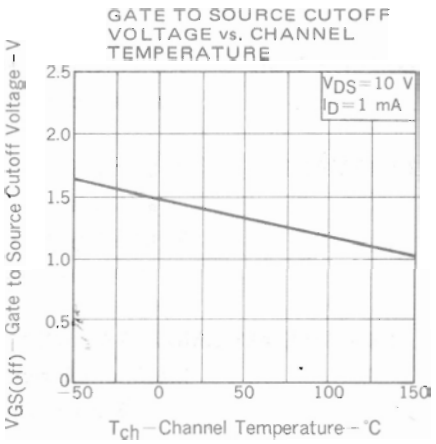


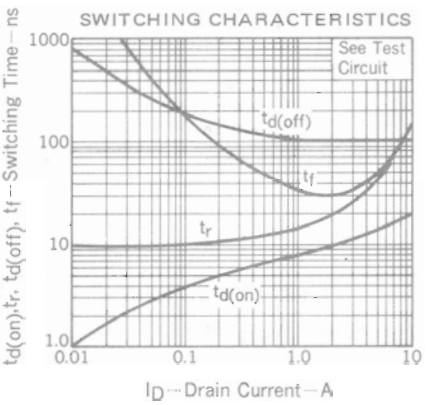
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



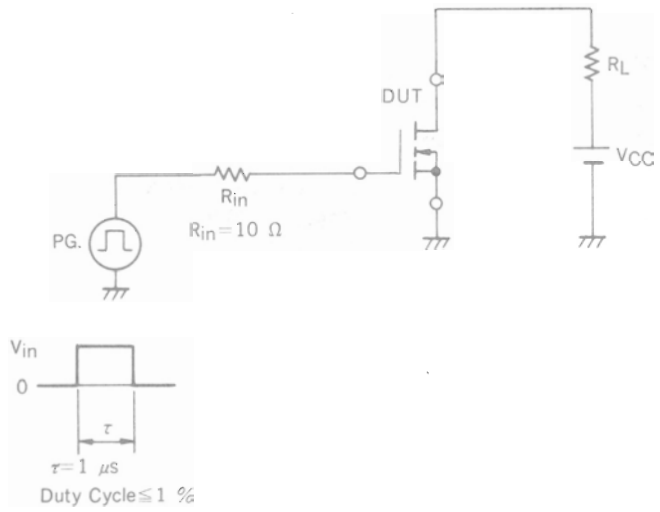


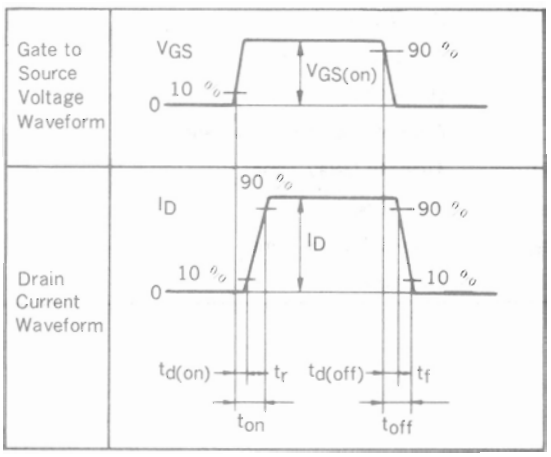






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK773

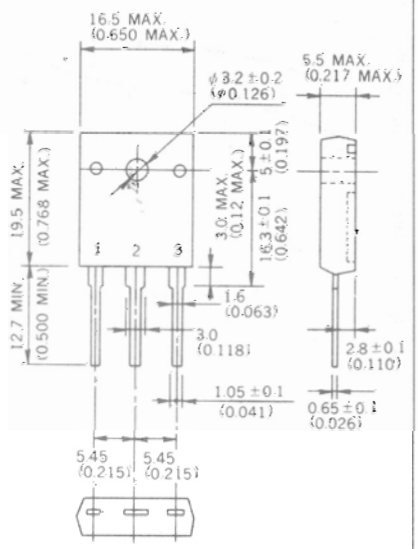
NEW DEVICE

DESCRIPTION The 2SK773 is N-channel MOD Field Effect Power Transistor designed for switching power supplies DC-DC converters.

FEATURES

- Suitable for switching power supplies, actuater controls, and pulse circuits.
- Low $R_{DS(on)}$
- No second breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



1. Gate
2. Drain (Fin)
3. Source

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±12	A
$I_{D(pulse)}$	Drain Current (pulse)*	±40	A

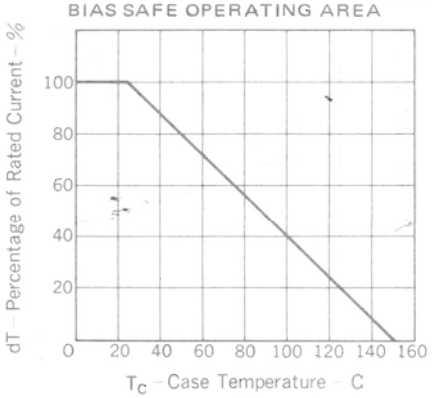
* PW ≦ 100 μs, Duty Cycle ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

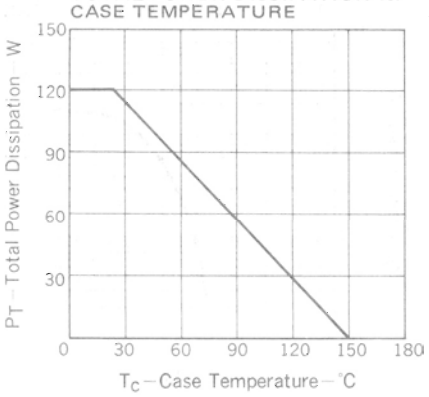
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Leakage Current			100	μA	V_{DS} = 500 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	5.0			S	V_{DS} = 10 V, I_D = 6 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.47	0.60	Ω	V_{GS} = 10 V, I_D = 6 A
C_{iss}	Input Capacitance		2200		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
C_{oss}	Output Capacitance		480		pF	
C_{rss}	Reverse Transfer Capacitance		130		pF	
$t_{d(on)}$	Turn-On Delay Time		30		ns	I_D = 6 A, V_{CC} ≒ 150 V $V_{GS(on)}$ = 10 V R_L = 25 Ω R_{in} = 10 Ω
t_r	Rise Time		45		ns	
$t_{d(off)}$	Turn-Off Delay Time		120		ns	
t_f	Fall Time		45		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

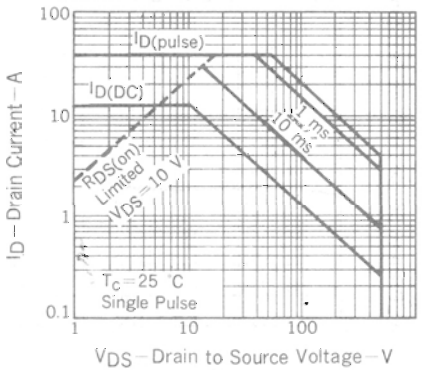
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



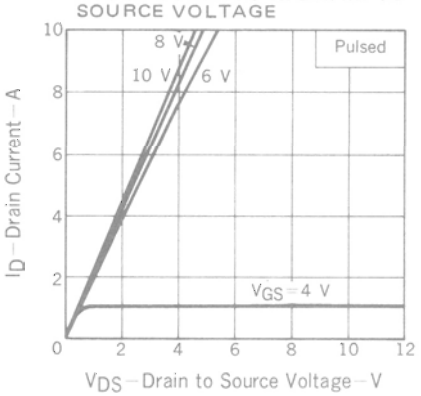
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



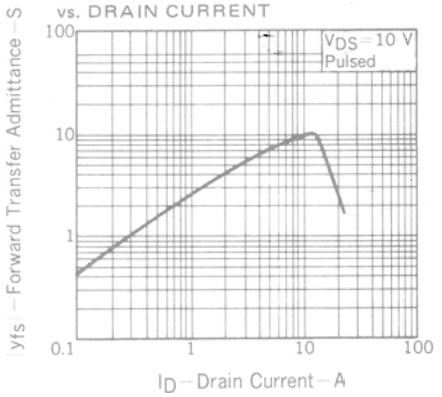
FORWARD BIAS SAFE OPERATING AREA



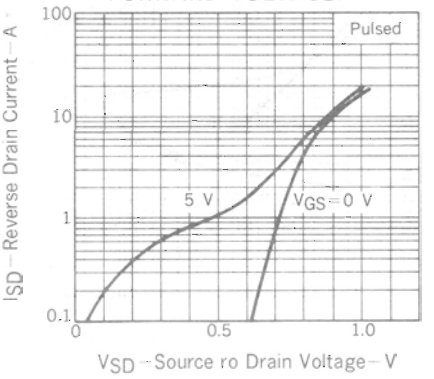
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



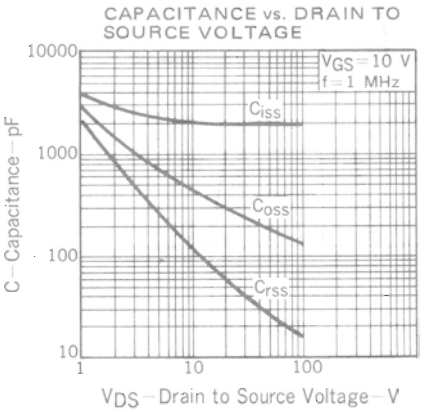
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



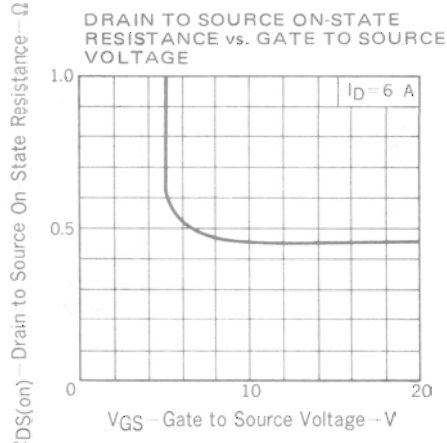
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



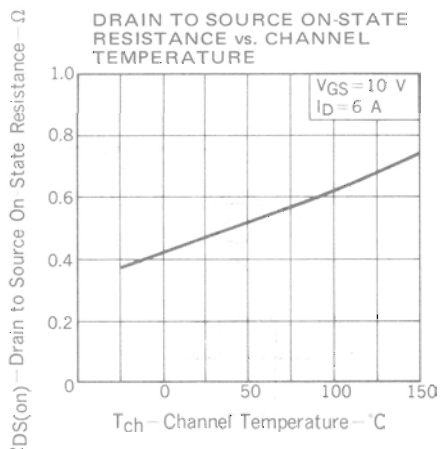
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

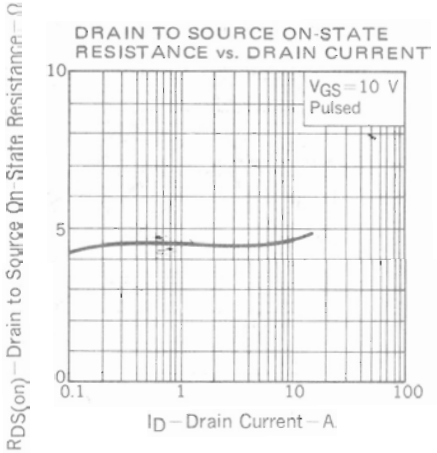


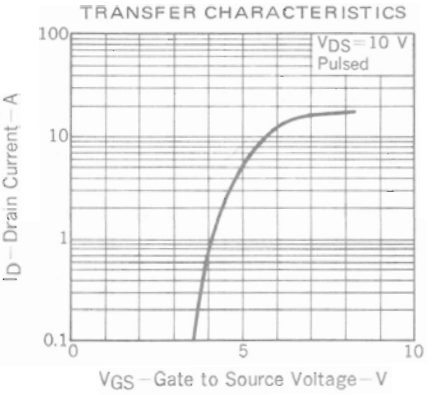
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

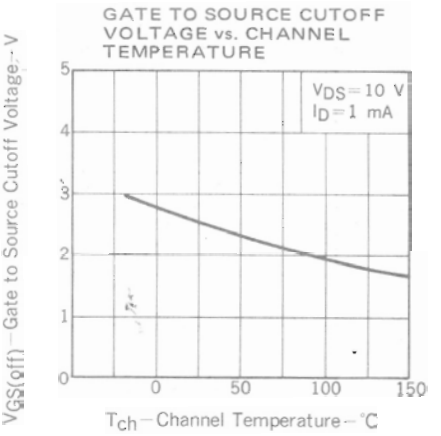


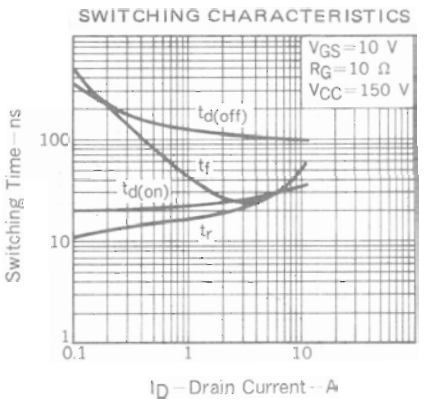
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



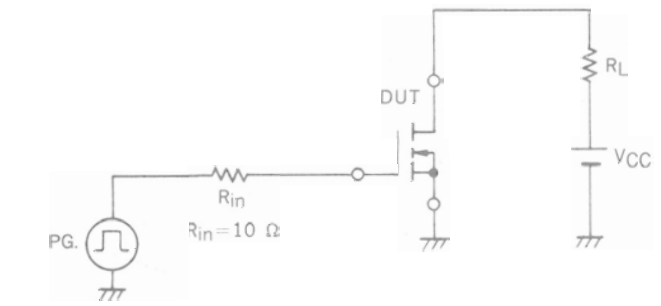


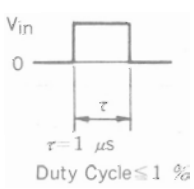


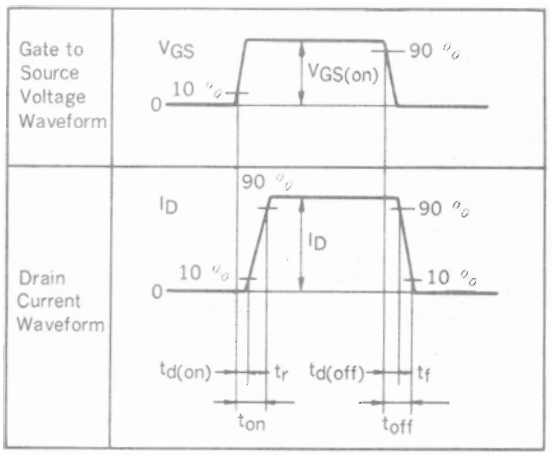




SWITCHING TIME TEST CIRCUIT







NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

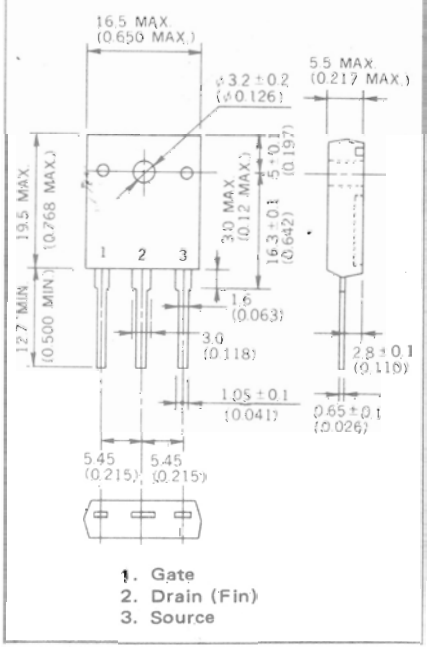
2SK774

DESCRIPTION The 2SK774 is N-channel MOS Field Effect Power Transistor designed for switching power supplies DC-DC converter.

FEATURES

- Suitable for switching power supplies, actuater controls, and pulse circuits
- Low $R_{DS(on)}$
- No second breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



1. Gate
2. Drain (Fin)
3. Source

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±18	A
$I_{D(pulse)}$	Drain Current (pulse)*	±60	A

* PW ≦ 300 μs, Duty Cycle ≦ 2 %

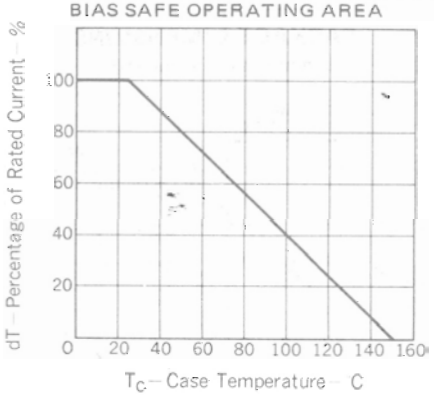
NEW DEVICE

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

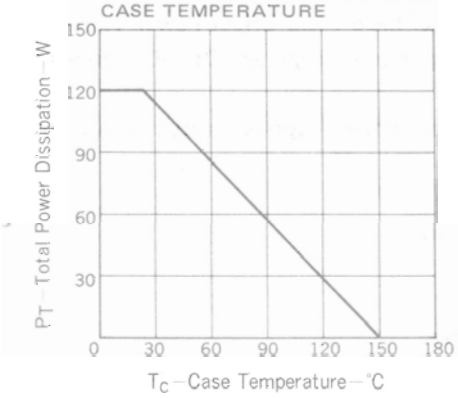
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Leakage Current			100	μA	V_{DS} = 500 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	8.0			S	V_{DS} = 10 V, I_D = 9 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.35	0.45	Ω	V_{GS} = 10 V, I_D = 9 A
C_{iss}	Input Capacitance		2600		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
C_{oss}	Output Capacitance		620		pF	
C_{rss}	Reverse Transfer Capacitance		170		pF	
$t_{d(on)}$	Turn-On Delay Time		35		ns	I_D = 9 A, V_{CC} ≒ 150 V $V_{GS(on)}$ = 10 V R_L = 16 Ω R_{in} = 10 Ω
t_r	Rise Time		55		ns	
$t_{d(off)}$	Turn-Off Delay Time		150		ns	
t_f	Fall Time		55		ns	

TYPICAL CHARACTERISTICS (T_a = 25 °C)

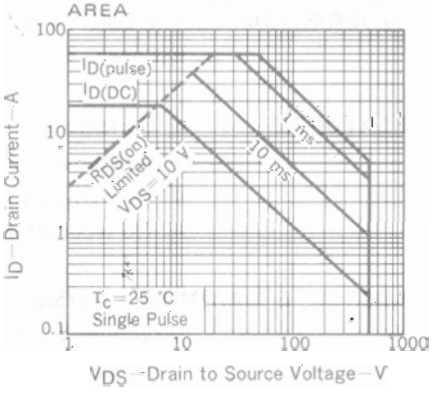
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



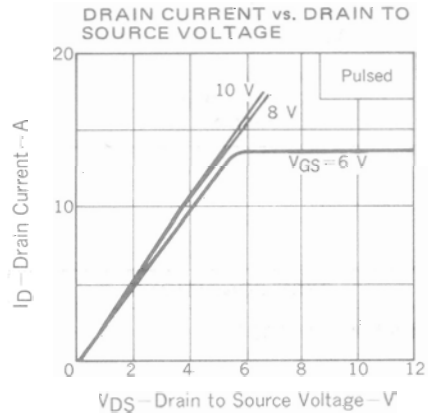
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



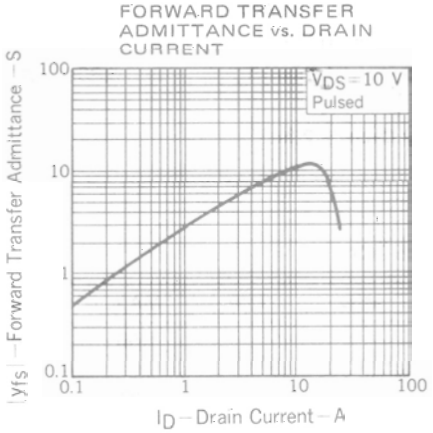
FORWARD BIAS SAFE OPERATING AREA



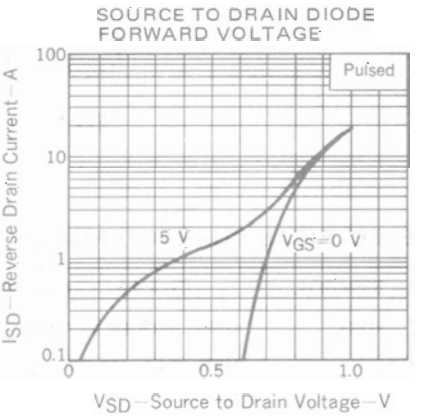
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



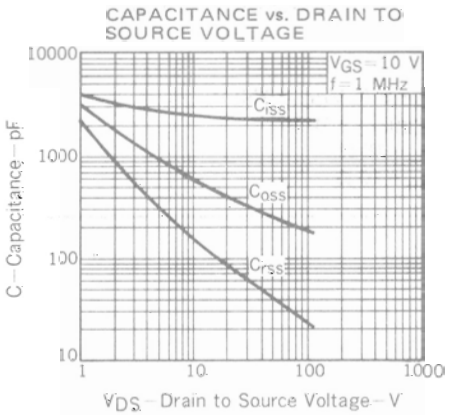
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



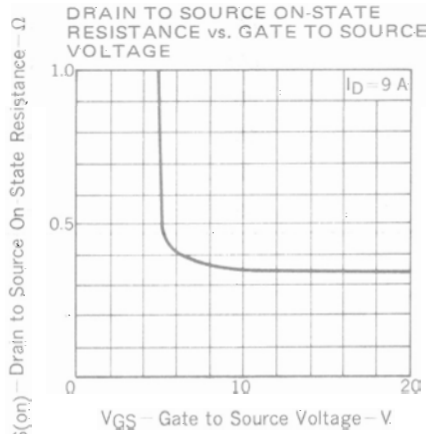
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



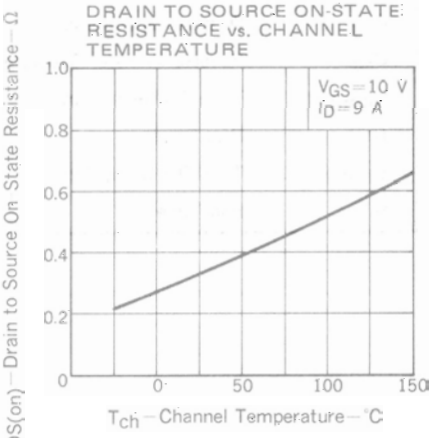
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

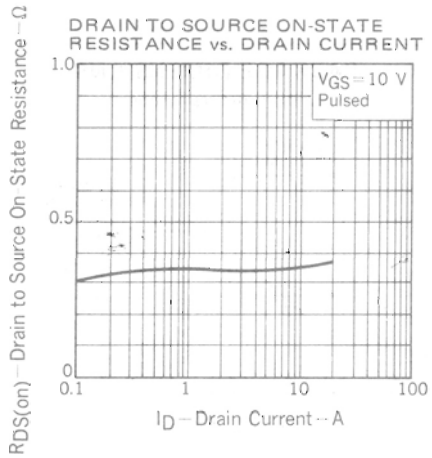


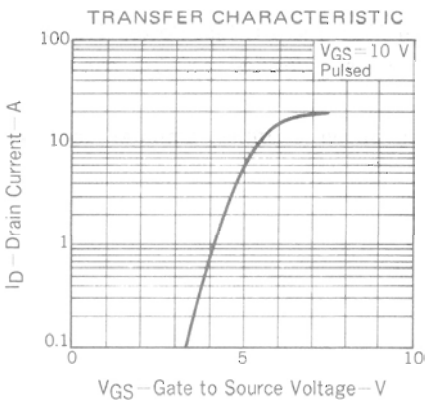
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

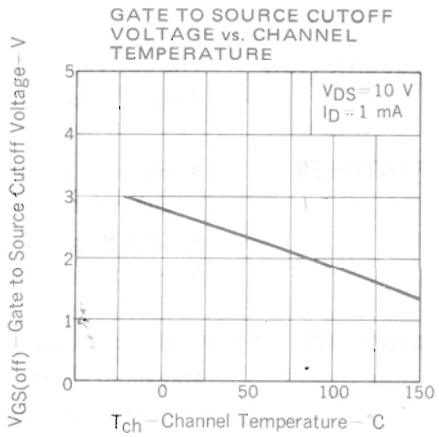


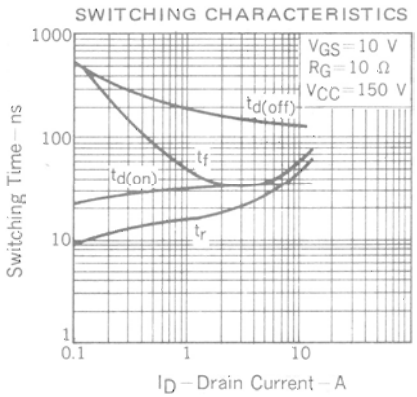
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



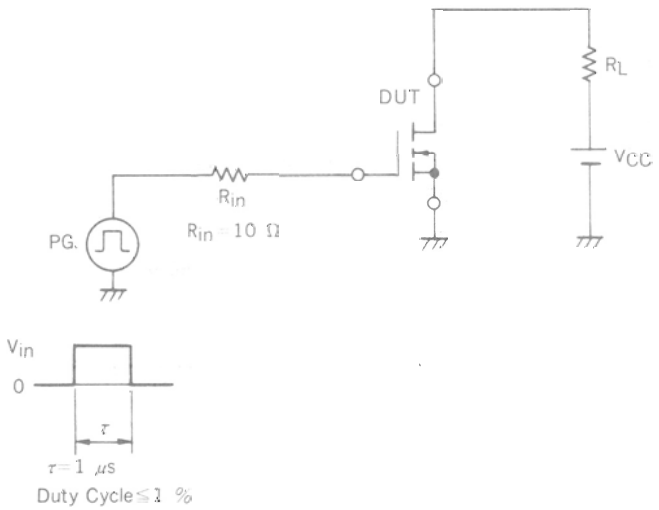


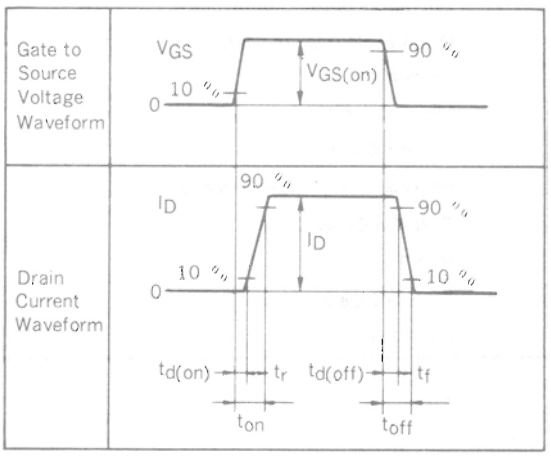






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK799

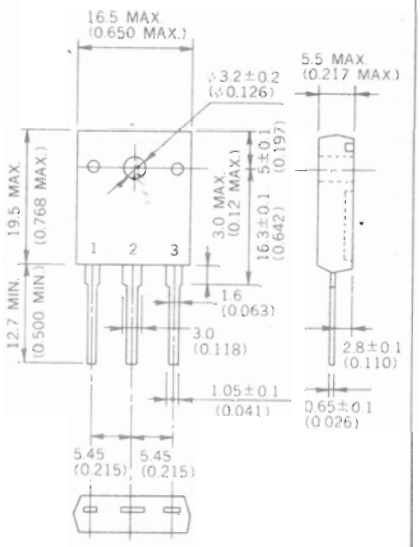
NEW DEVICE

DESCRIPTION The 2SK799 is N-channel MOS Field Effect Power Transistor designed for switching power supplies, DC-DC converters.

FEATURES

- Suitable for switching power supplies, actuater controls, and pulse circuits
- Low $R_{DS(on)}$
- No second breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



1. Base
2. Collector (Fin)
3. Emitter

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	450	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±12	A
$I_{D(pulse)}$	Drain Current (pulse)*	±40	A

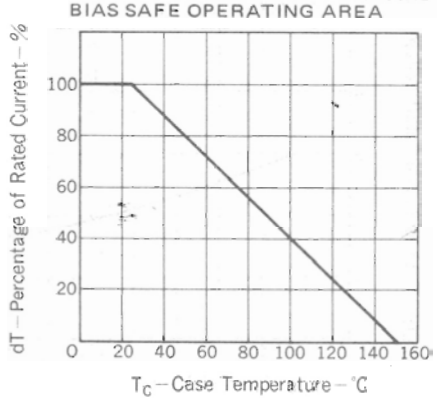
* PW ≦ 100 μs, Duty Cycle ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

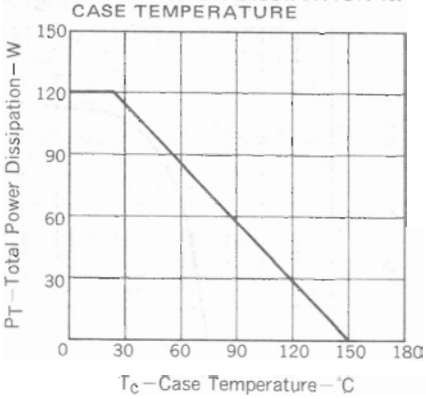
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Leakage Current			100	μA	V_{DS} = 450 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	5.0			S	V_{DS} = 10 V, ID = 6 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.40	0.50	Ω	V_{GS} = 10 V, I_D = 6 A
C_{iss}	Input Capacitance		2000		pF	
C_{oss}	Output Capacitance		500		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		140		pF	
$t_{d(on)}$	Turn-On Delay Time		20		ns	
t_r	Rise Time		35		ns	I_D = 6 A, V_{CC} = 150 V
$t_{d(off)}$	Turn-Off Delay Time		100		ns	$V_{GS(on)}$ = 10 V
t_f	Fall Time		35		ns	R_{in} = 10 Ω

TYPICAL CHARACTERISTICS (T_a = 25 °C)

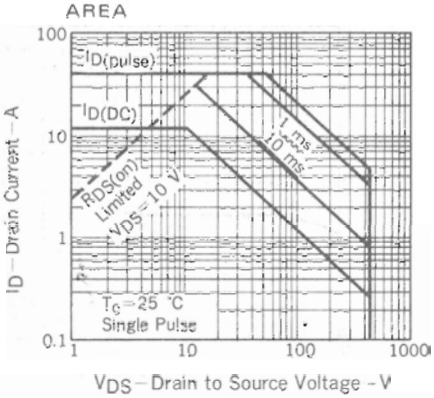
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



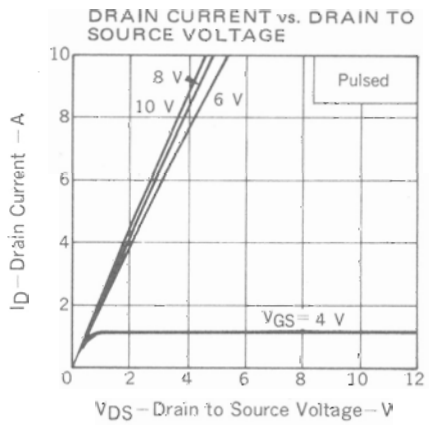
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



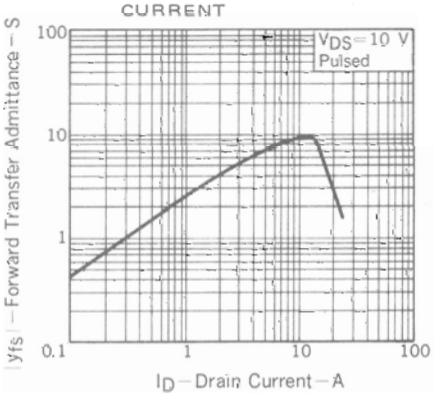
FORWARD BIAS SAFE OPERATING AREA



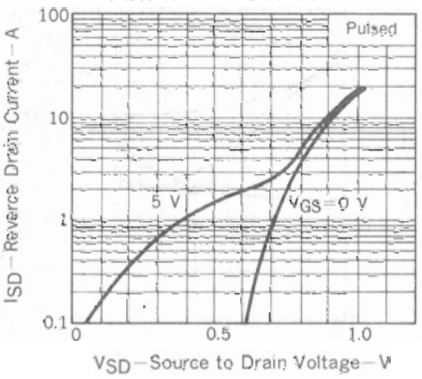
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



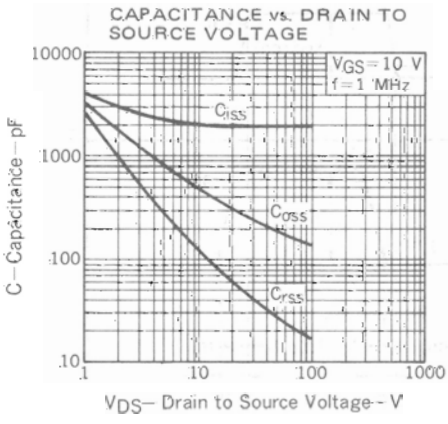
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



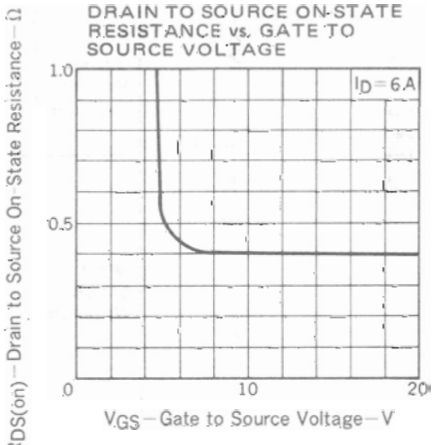
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



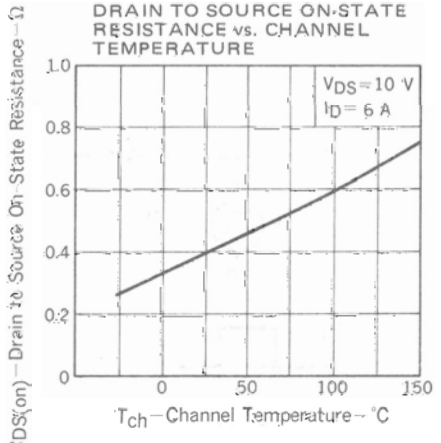
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

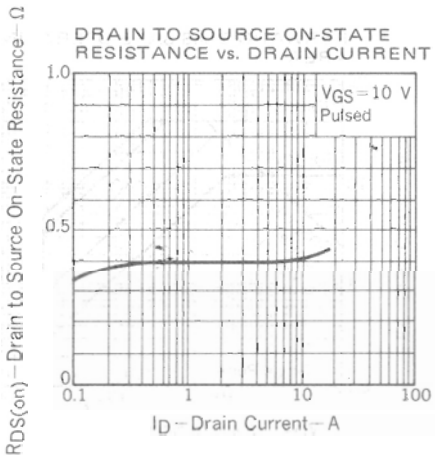


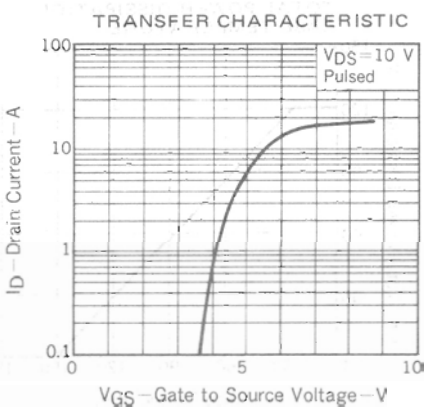
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

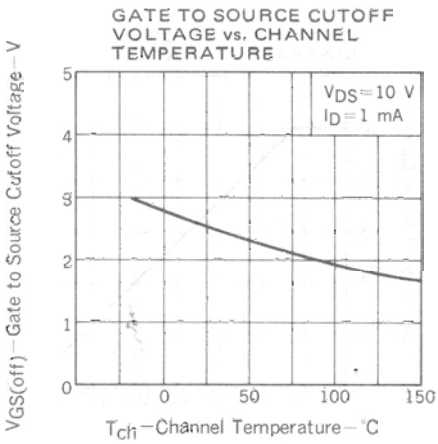


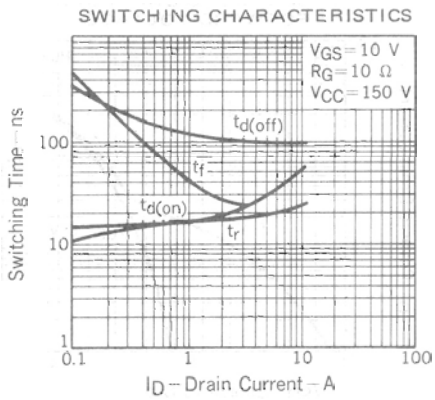
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



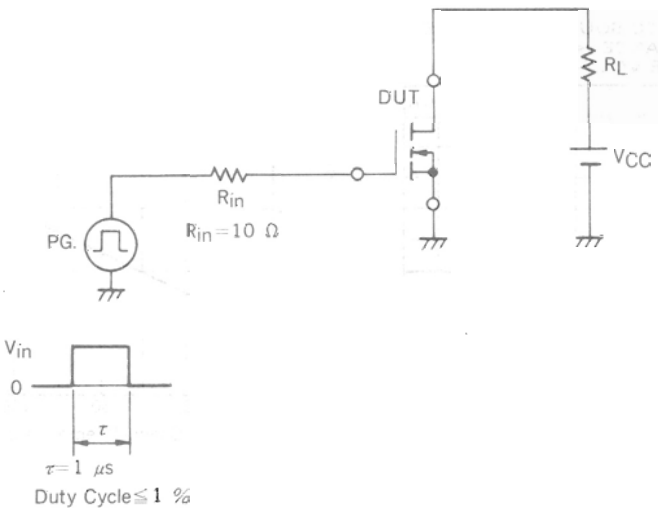


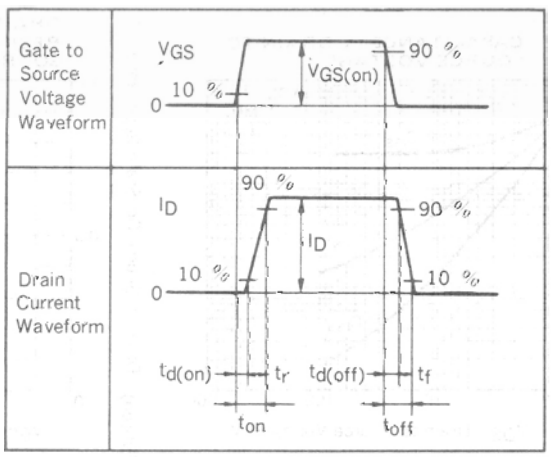






SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK800

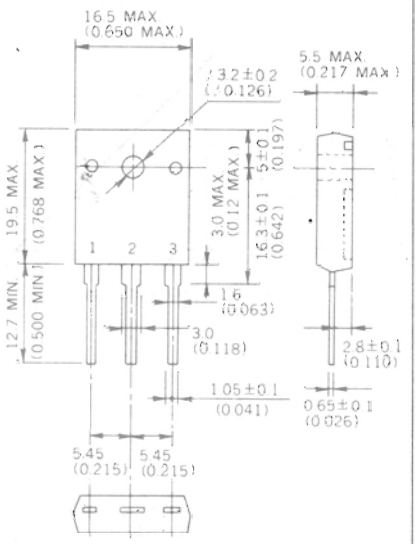
NEW DEVICE

DESCRIPTION The 2SK800 is N-channel MOS Field Effect Power Transistor designed for converters.

FEATURES

- Suitable for switching power supplies, actuater controls, and pulse circuits
- Low $R_{DS(on)}$
- No second breakdown

PACKAGE DIMENSIONS
in millimeters (inches)



1. Gate
2. Drain (Fin)
3. Source

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Channel Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_C = 25 °C)

- Total Power Dissipation . . . . . 120 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	450	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±18	A
$I_{D(pulse)}$	Drain Current (pulse)*	±60	A

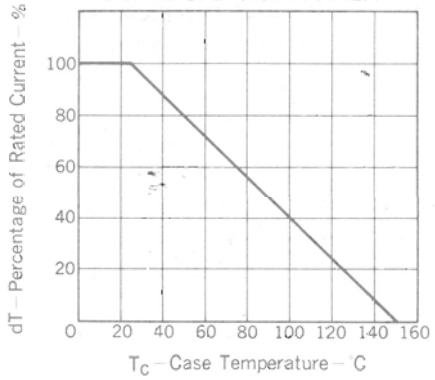
* PW ≦ 100 μs, Duty Cycle ≦ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

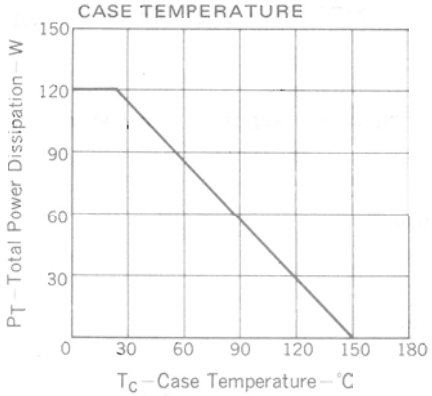
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Drain Leakage Current			100	μA	V_{DS} = 450 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|y_{fs}\|$	Forward Transfer Admittance	8.0			S	V_{DS} = 10 V, I_D = 9 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.32	0.38	Ω	V_{GS} = 10 V, I_D = 9 A
C_{iss}	Input Capacitance		2600		pF	
C_{oss}	Output Capacitance		610		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		140		pF	
$t_{d(on)}$	Turn-On Delay Time		20		ns	
t_r	Rise Time		40		ns	I_D = 9 A, V_{CC} = 150 V
$t_{d(off)}$	Turn-Off Delay Time		120		ns	$V_{GS(on)}$ = 10 V
t_f	Fall Time		55		ns	R_{in} = 10 Ω

TYPICAL CHARACTERISTICS (T_a = 25 °C)

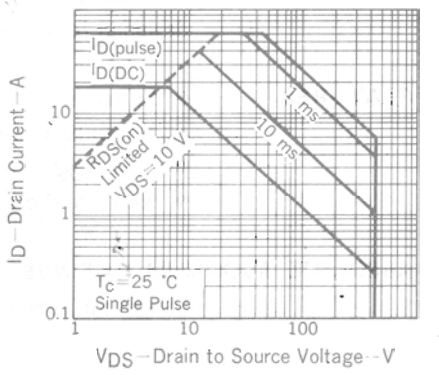
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



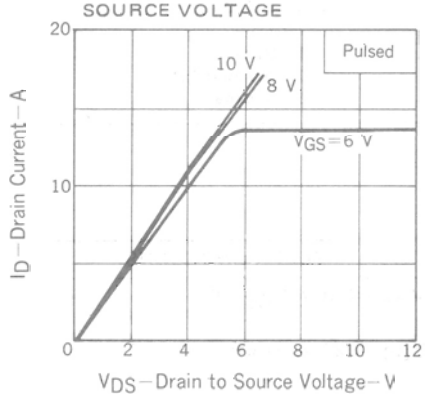
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



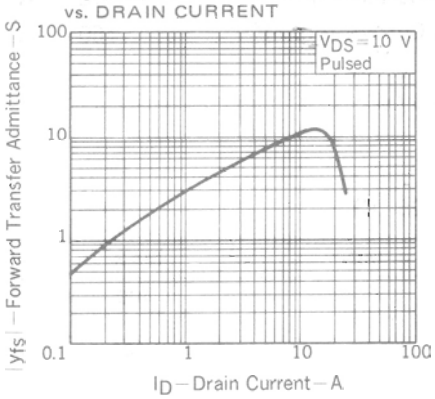
FORWARD BIAS SAFE OPERATING AREA



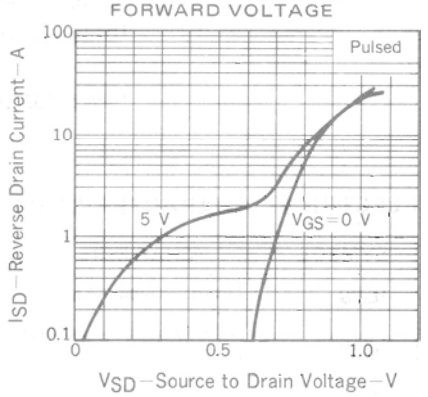
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



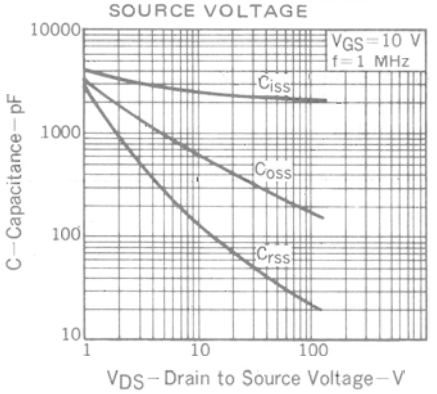
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



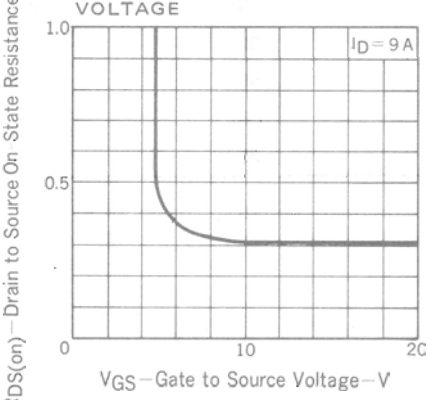
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



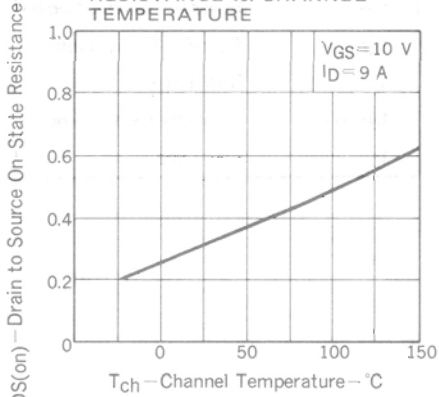
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



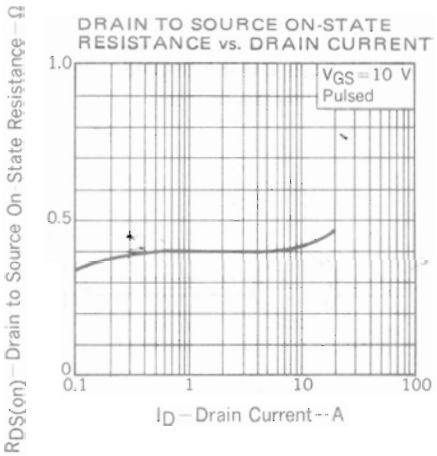
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



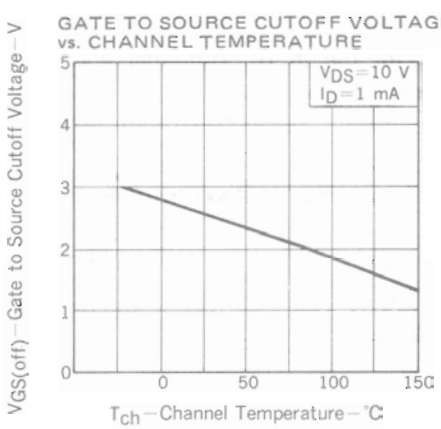
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



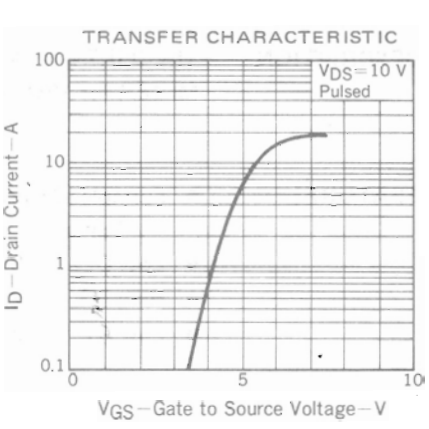
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



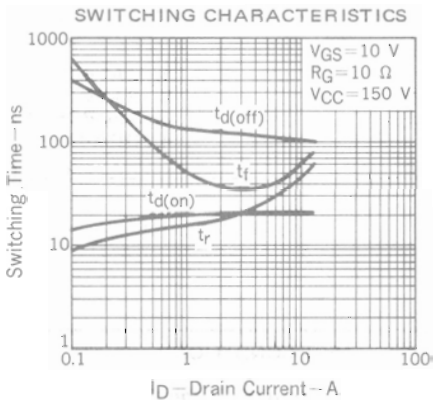
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



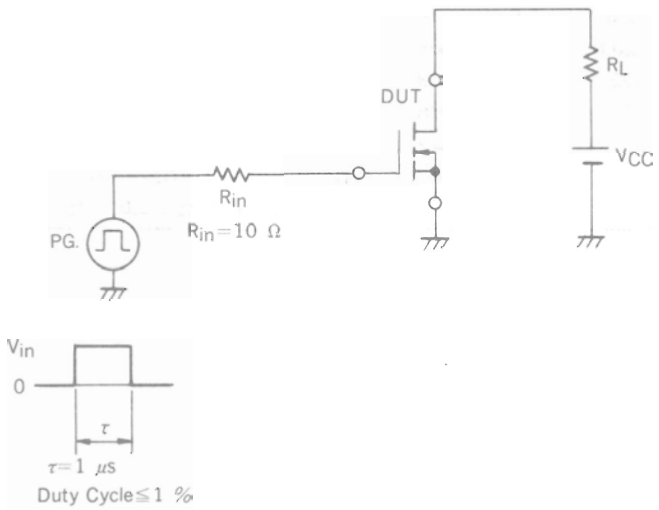
TRANSFER CHARACTERISTIC

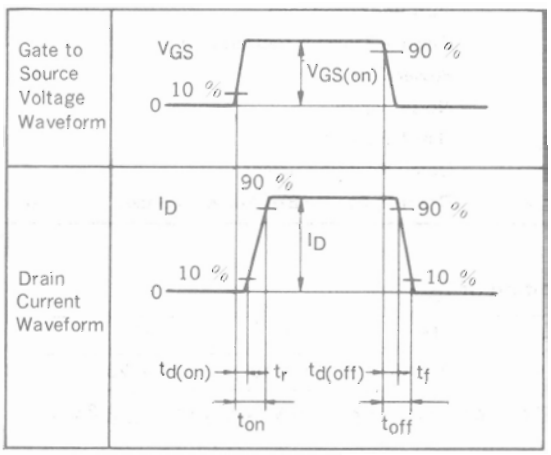


SWITCHING CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT





NEC
ELECTRON DEVICE

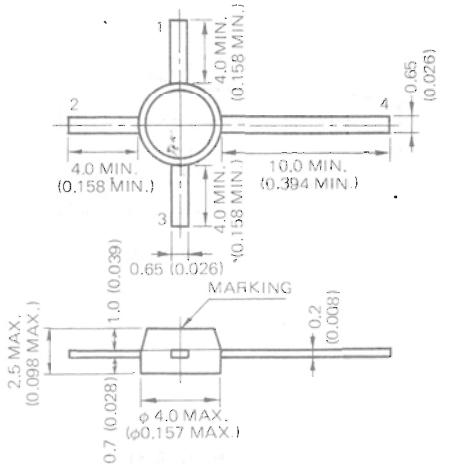
MOS FIELD EFFECT TRANSISTOR
3SK74

DESCRIPTION The 3SK74 is designed for use in RF Amplifier and MIXER for VHF TV Tuner.

FEATURES

- Suitable for use as RF Amplifier & Mixer in VHF TV Tuner.
- Low C_{rss} : 0.03 pF TYP.
- High PG : 22 dB TYP.
- Low NF : 2.0 dB TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. GATE 2
2. GATE 1
3. SOURCE
4. DRAIN

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +125 °C
- Channel Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Current (Ta=25 °C)

- V_{DSX} Drain to Source Voltage . . . . . 20 V
- V_{G1S} Gate1 to Source Voltage . . . . . ±10 V
- V_{G2S} Gate2 to Source Voltage . . . . . ±10 V
- I_D Drain Current . . . . . 25 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	7.0		25	mA	V_{DS}=6.0 V, V_{G1S}=0, V_{G2S}=3.0 V
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−3.0	V	V_{DS}=6.0 V, V_{G2S}=0, I_D=5.0 μA
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−3.0	V	V_{DS}=6.0 V, V_{G1S}=0, I_D=5.0 μA
$\lvert Y_{fs} \rvert$	Forward Transfer Admittance	17	20		mS	V_{DS}=6.0 V, I_D=10 mA, V_{G2S}=3.0 V f=1 kHz
C_{iss}	Input Capacitance		4.8	6.0	pF	V_{DS}=6.0 V, I_D=10 mA, V_{G2S}=3.0 V f=1 MHz
C_{oss}	Output Capacitance		2.5	3.5	pF	
C_{rss}	Reverse Transfer Capacitance		0.03	0.05	pF	
G_{ps}	Power Gain	20	22		dB	V_{DS}=10 V, I_D=10 mA, f=200 MHz V_{G2}=5.0 V (See Test Circuit)
NF	Noise Figure		2.0	3.0	dB	
I_{G1SS}	Gate1 Reverse Current			±0.1	μA	V_{DS}=0, V_{G1S}=±10 V, V_{G2S}=0
I_{G2SS}	Gate2 Reverse Current			±0.1	μA	V_{DS}=0, V_{G1S}=0, V_{G2S}=±10 V
BV_{DSX}	Drain to Source Breakdown Voltage	20			V	V_{G1S}=−3.0 V, V_{G2S}=3.0 V, I_D=500 nA

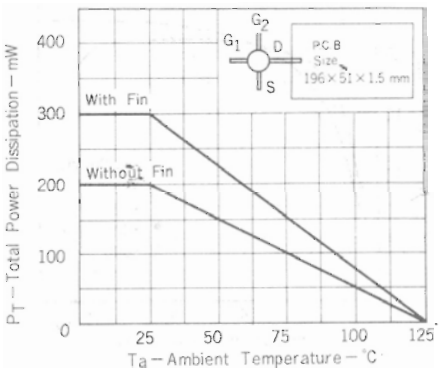
Classification of I_{DSS}

Rank	M	L	K
Range(mA)	7.0 – 13	11 – 19	17 – 25

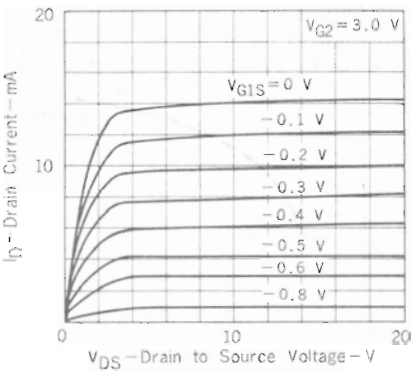
I_{DSS} Test Conditions : V_{DS}=6.0 V, V_{G1S}=0, V_{G2S}=3.0 V

TYPICAL CHARACTERISTICS (Ta = 25 °C)

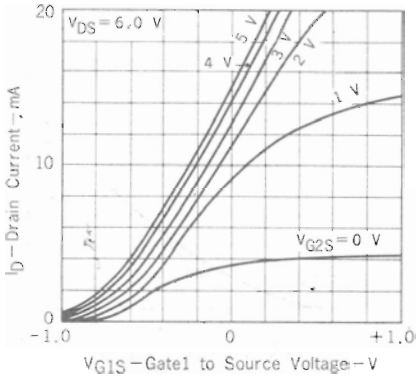
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



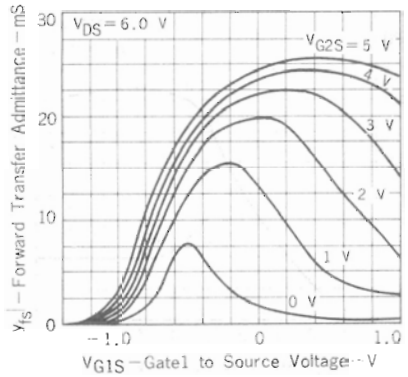
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



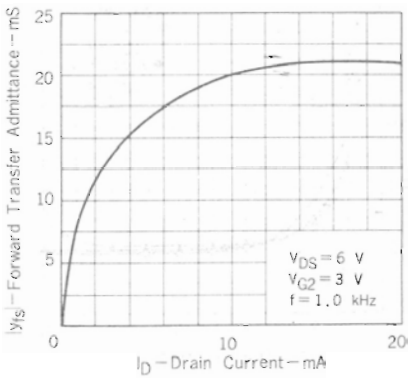
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



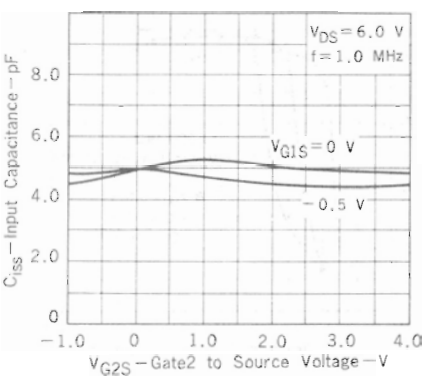
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

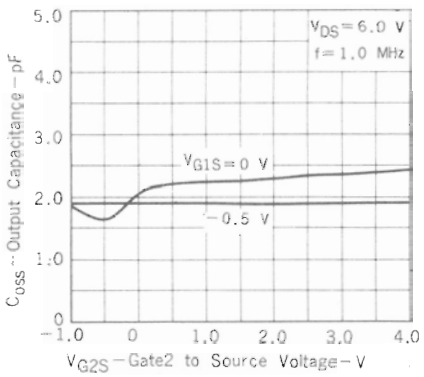


INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE

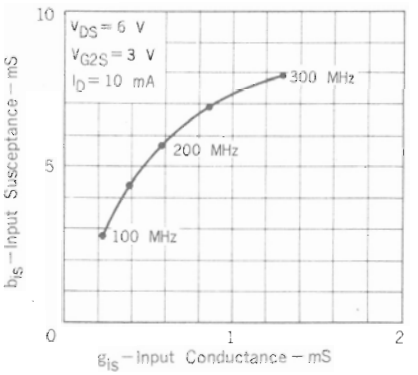


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

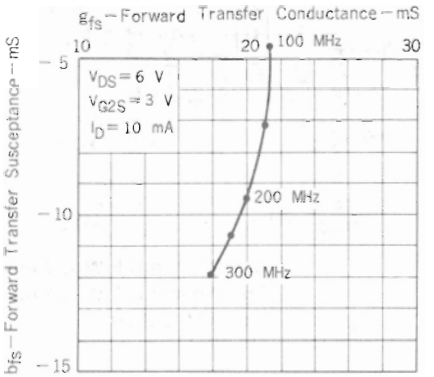
OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



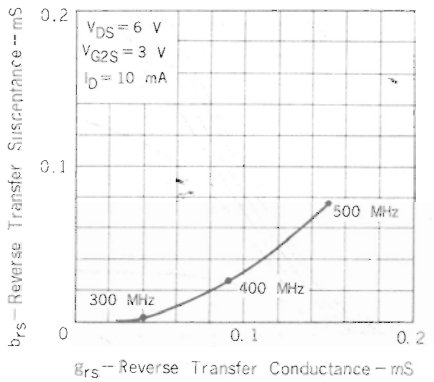
INPUT ADMITTANCE (y_{is}) vs. FREQUENCY



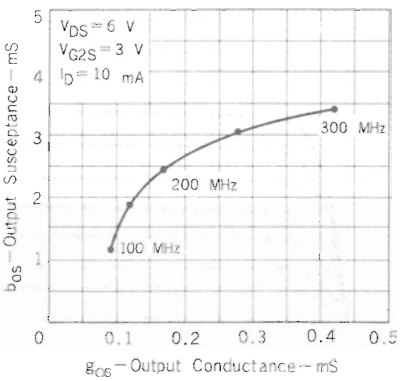
FORWARD TRANSFER ADMITTANCE (y_{fs}) vs. FREQUENCY



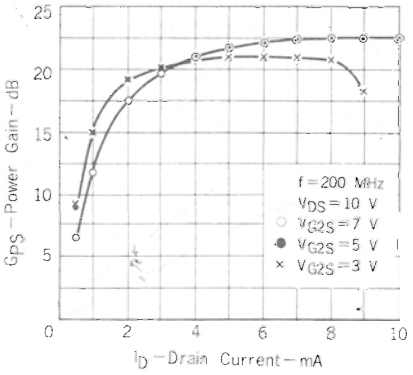
REVERSE TRANSFER ADMITTANCE (y_{rs}) vs. FREQUENCY



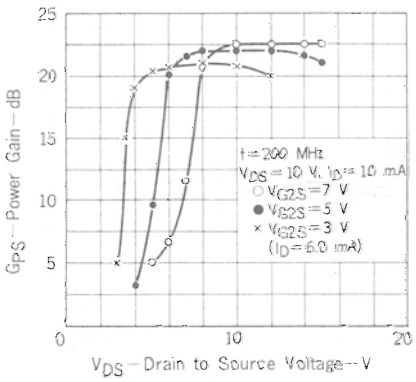
OUTPUT ADMITTANCE (y_{os}) vs. FREQUENCY



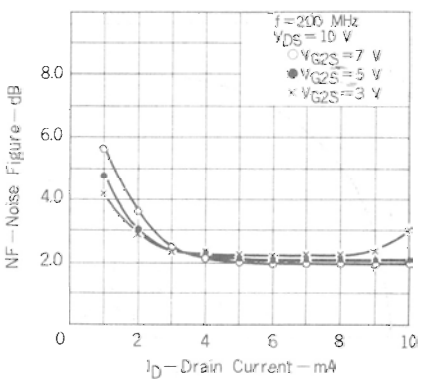
POWER GAIN vs. DRAIN CURRENT



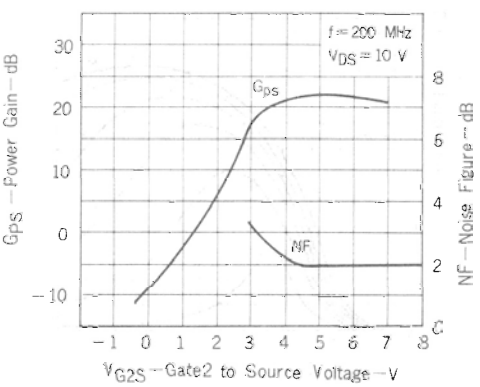
POWER GAIN vs. DRAIN TO SOURCE VOLTAGE



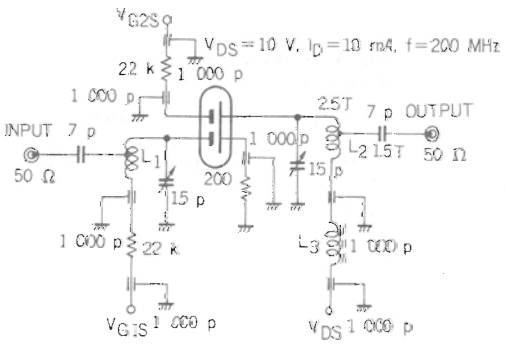
NOISE FIGURE vs. DRAIN CURRENT



NOISE FIGURE, POWER GAIN vs. GATE2 TO SOURCE VOLTAGE



200 MHz POWER GAIN & NOISE FIGURE TEST CIRCUIT



L_1 : 0.6 mm U.E.W. ϕ 7 mm 3T
L_2 : 0.6 mm U.E.W. ϕ 7 mm 3T
L_3 : RFC 2.2 μH

NEC
ELECTRON DEVICE

N-CHANNEL SILICON DUAL-GATE MOS FIELD EFFECT TRANSISTOR

3SK87

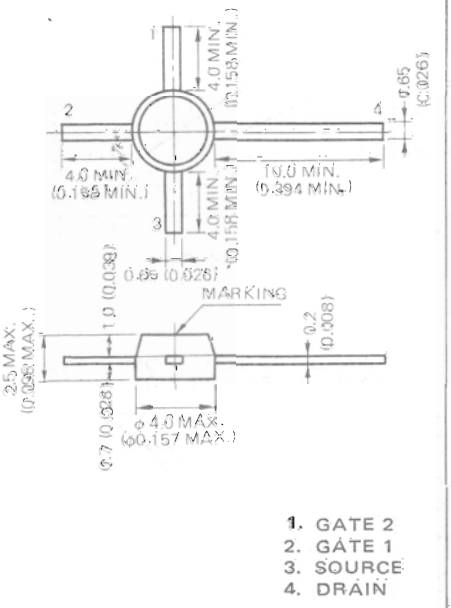
DISCONTINUED

DESCRIPTION The 3SK87 is designed for use as RF Amplifier in UHF TV Tuner.
Especially recommended for half wave length resonator type tuner (λ/2).

FEATURES

- Low C_{rss} : 0.02 pF TYP.
- High G_{ps} : 18 dB TYP.
- Low NF : 3.8 dB TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. GATE 2
2. GATE 1
3. SOURCE
4. DRAIN

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C
- Channel Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta=25 °C)
- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Current (Ta=25 °C)
- Drain to Source Voltage V_{DSX} . . . . . 20 V
- Gate1 to Source Voltage V_{G1S} . . . . . ±10 V
- Gate2 to Source Voltage V_{G2S} . . . . . ±10 V
- Drain Current I_D . . . . . 25 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Curre	0.5		8	mA	V_{DS}=10 V, V_{G2S}=4.0 V, V_{G1S}=0
$\|Y_{fs}\|$	Forward Transfer Admittance	18	22		mS	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 kHz
C_{iss}	Input Capacitance	1.5	2.0	3.5	pF	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 MHz
C_{oss}	Output Capacitance	0.5	1.1	1.5	pF	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 MHz
C_{rss}	Reverse Transfer Capacitance		0.02	0.03	pF	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 MHz
G_{ps}*	Power Gain	15	18	22	dB	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=900 MHz
NF*	Noise Figure		3.8	5.5	dB	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=900 MHz
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−2.0	V	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 μA
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−0.7	V	V_{DS}=10 V, V_{G1S}=4.0 V, I_D=10 μA
I_{G1SS}	Gate1 Reverse Current			±20	nA	V_{DS}=0, V_{G1S}=±10 V, V_{G2S}=0
I_{G2SS}	Gate2 Reverse Current			±20	nA	V_{DS}=0, V_{G2S}=±10 V, V_{G1S}=0
BV_{DSX}	Drain to Source Breakdown Voltage	20	24		V	V_{G1S}=V_{G2S}=−2.0 V, I_D=10 μA

* See Test Circuit

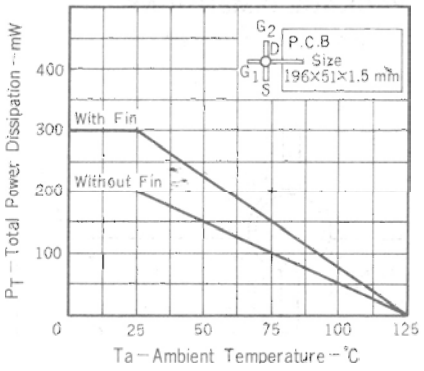
Classification of I_{DSS}

Rank	L	K
I_{DSS}(mA)	0.5 – 5.0	3.0 – 8.0

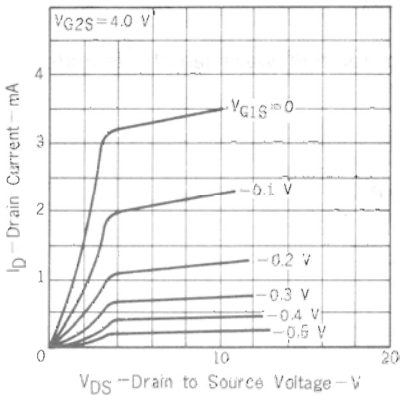
I_{DSS} Test Conditions: V_{DS}=10 V, V_{G2S}=4.0 V, V_{G1S}=0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

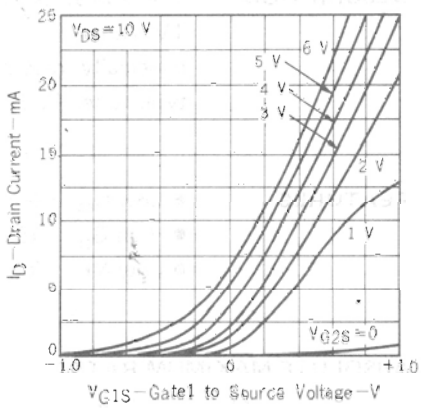
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



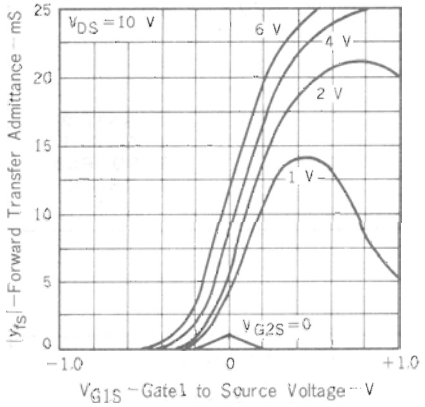
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



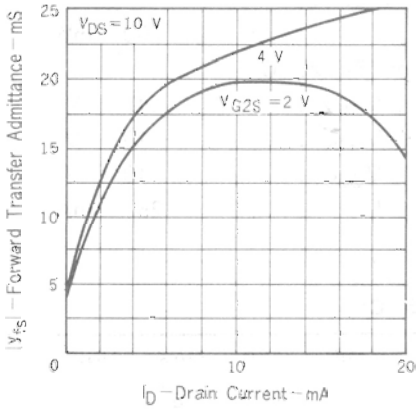
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



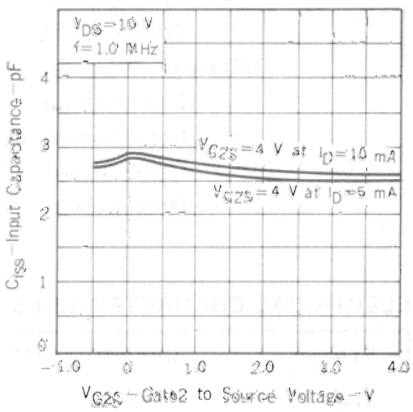
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

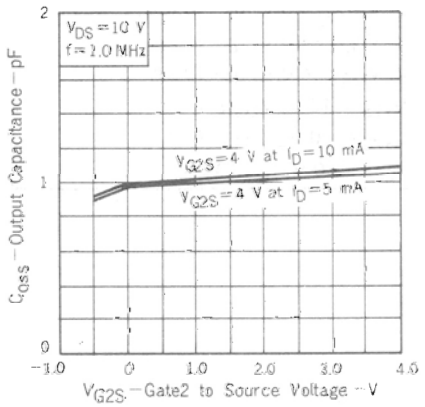


INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE

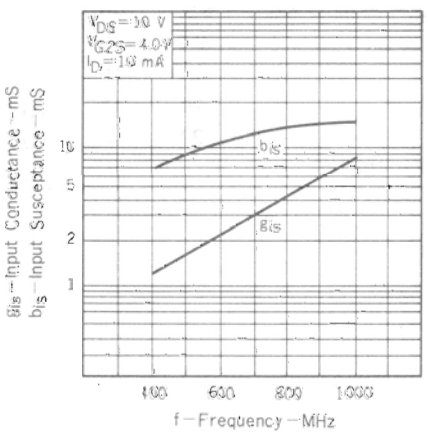


TYPICAL "Y" PARAMETERS

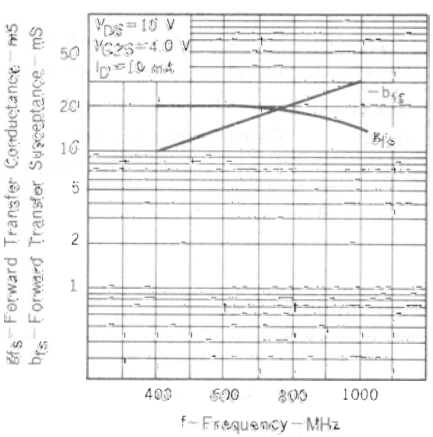
OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



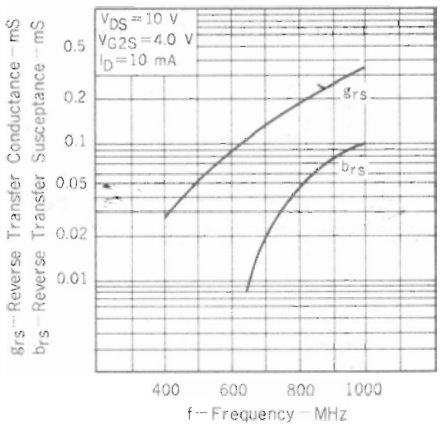
INPUT ADMITTANCE vs. FREQUENCY



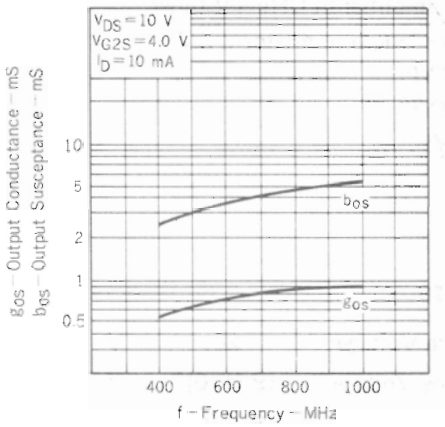
FORWARD TRANSFER ADMITTANCE vs. FREQUENCY



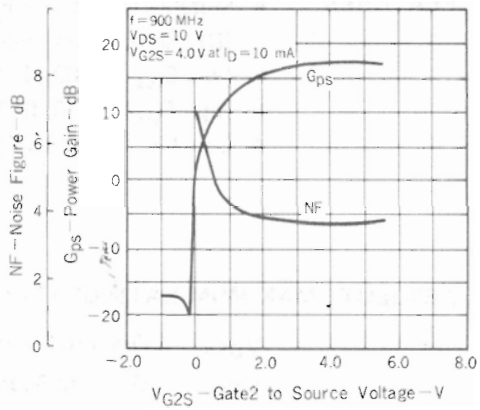
REVERSE TRANSFER ADMITTANCE vs. FREQUENCY



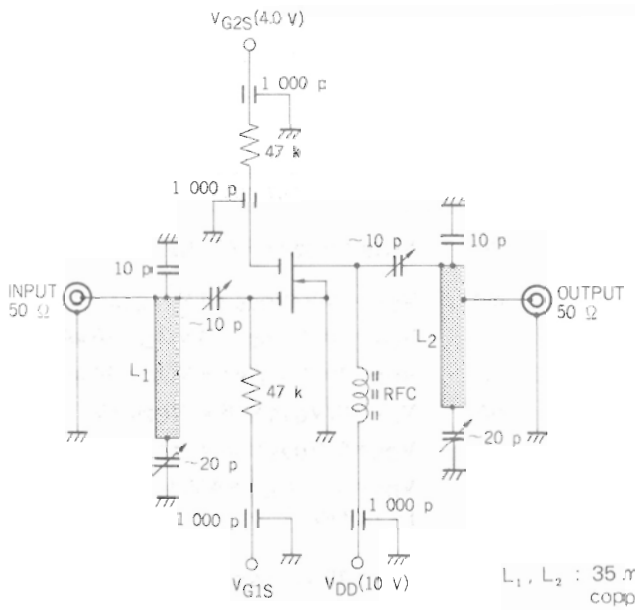
OUTPUT ADMITTANCE vs. FREQUENCY



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



900 MHz G_{ps} & NF TEST CIRCUIT



L_1, L_2 : 35 mm X 5.0 mm X 0.2 mm copper

NEC
ELECTRON DEVICE

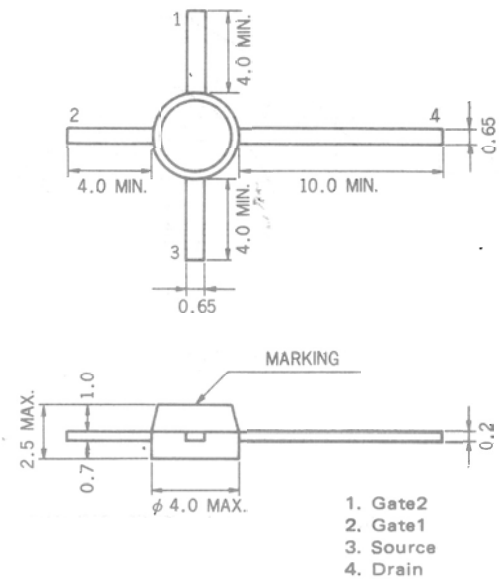
MOS FIELD EFFECT TRANSISTOR
3SK87A

FEATURES

- Suitable for use as RF amplifier in UHF TV tuner. (RF Amp. for half wave length resonator : λ/2)
- Low C_{rss} : 0.02 pF TYP.
- High G_{ps} : 20.0 dB TYP.
- Low NF : 3.0 dB TYP.

NEW DEVICE

PACKAGE DIMENSIONS (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

V_{DSX}	Drain to Source Voltage	20	V
V_{G1S}	Gate1 to Source Voltage	±8 (±10)*	V
V_{G2S}	Gate2 to Source Voltage	±8 (±10)*	V
I_D	Drain Current	25	mA
P_T	Total Power Dissipation	200	mW
T_{ch}	Channel Temperature	125	°C
T_{stg}	Storage Temperature	−55 to +125	°C

*$R_L \geqq 10$ kΩ

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
BV_{DSX}	Drain to Source Breakdown Voltage	20	24		V	$V_{G1S} = V_{G2S} = -2$ V, $I_D = 10$ μA
I_{DSS}	Drain Current	0.5		8	mA	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $V_{G1S} = 0$
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−2.0	V	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ μA
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−0.7	V	$V_{DS} = 10$ V, $V_{G1S} = 4$ V, $I_D = 10$ μA
I_{G1SS}	Gate1 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G1S} = \pm 8$ V, $V_{G2S} = 0$
I_{G2SS}	Gate2 Reverse Current			±20	A	$V_{DS} = 0$, $V_{G2S} = \pm 8$ V, $V_{G1S} = 0$
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	18	22		mS	$V_{DS} = 5$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1.0 kHz
C_{iss}	Input Capacitance	1.5	2.5	3.5	pF	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1 MHz
C_{oss}	Output Capacitance	0.5	1.1	1.5	pF	
C_{rss}	Reverse Transfer Capacitance		0.02	0.03	pF	
G_{ps}**	Power Gain	18	20		dB	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 900 MHz
NF**	Noise Figure		3.0	5.0	dB	

I_{DSS} Classification

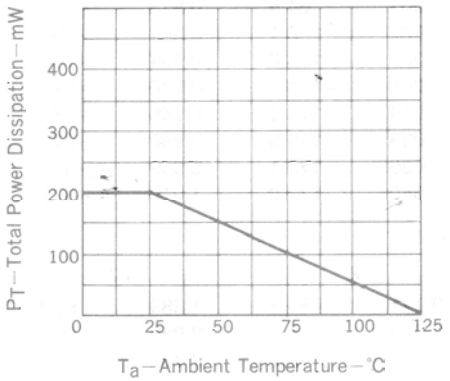
Marking	L	K
I_{DSS}	0.5 to 5	3 to 8

UNIT: mA

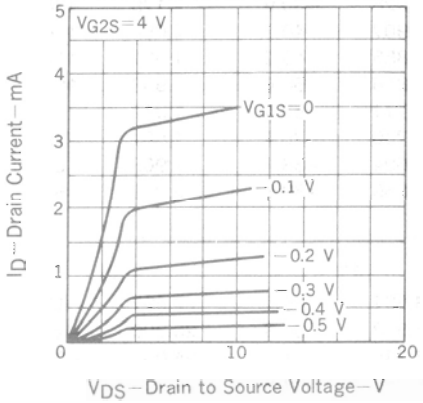
**See Test Circuit

TYPICAL CHARACTERISTICS (T_a = 25 °C)

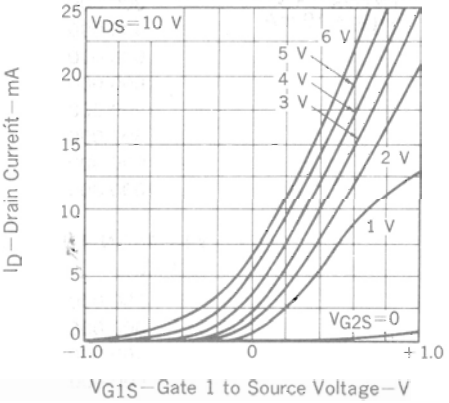
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



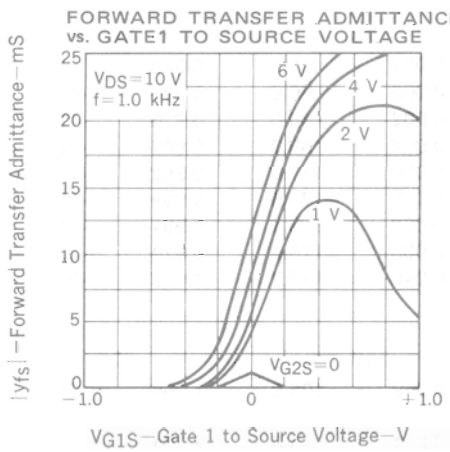
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



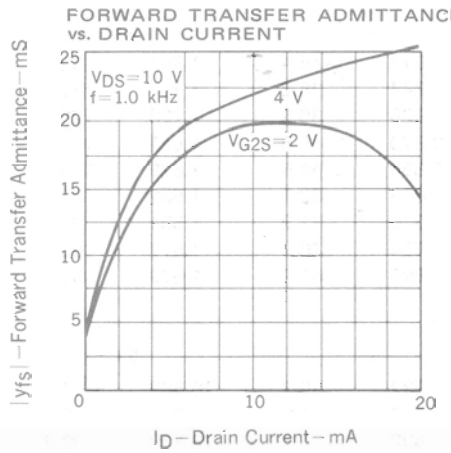
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



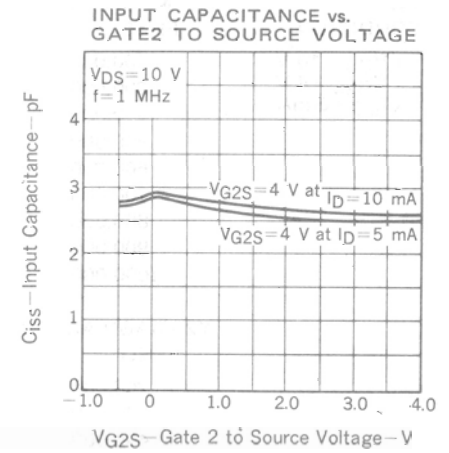
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



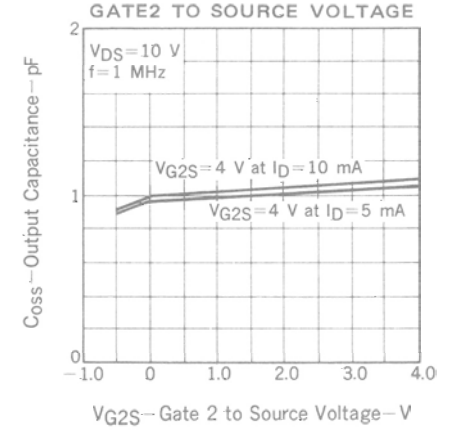
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



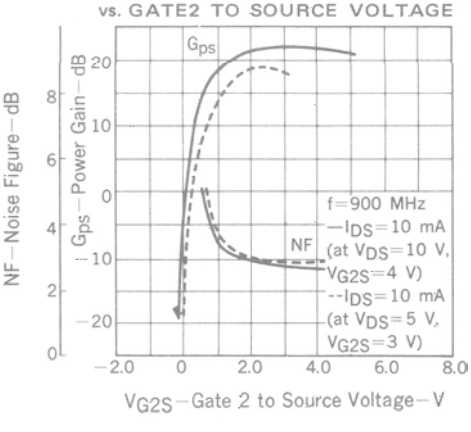
INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



S-PARAMETER, Y-PARAMETER

S1, Y1
CONDITION
(V_{DS} = 10 V, V_{G2S} = 4 V, I_{DS} = 10 mA)

S1–MAGN AND ANGLES :

FREQ.	11		21		12		22	
200.000	0.971	−20.4	2.178	152.9	0.002	88.8	0.983	−8.0
300.000	0.928	−30.9	2.129	138.2	0.003	64.4	0.973	−11.8
400.000	0.907	−40.1	2.094	126.0	0.002	156.1	0.961	−15.6
500.000	0.855	−49.2	1.987	114.2	0.004	−176.0	0.937	−18.9
600.000	0.826	−58.6	1.968	102.1	0.009	−173.6	0.940	−21.3
700.000	0.777	−67.4	1.917	91.3	0.014	−176.3	0.949	−25.0
800.000	0.740	−75.4	1.881	79.4	0.023	−176.5	0.948	−27.9
900.000	0.694	−83.1	1.908	66.0	0.029	179.1	0.969	−32.5
1000.000	0.659	−89.8	2.018	51.9	0.040	−179.0	1.019	−37.4

Y1–MAGN AND ANGLES :

FREQ.	11		21		12		22	
200.000	3.587	85.1	22.687	−13.1	0.021	−77.2	1.389	83.1
300.000	5.533	81.8	23.300	−21.2	0.032	−95.0	2.059	82.9
400.000	7.348	81.0	24.068	−27.4	0.021	2.7	2.752	81.1
500.000	9.286	77.9	24.720	−34.2	0.051	35.6	3.382	77.7
600.000	11.406	76.6	26.011	−41.5	0.112	42.8	3.784	78.7
700.000	13.532	73.4	27.351	−48.1	0.207	44.4	4.381	80.5
800.000	15.628	70.7	29.027	−56.7	0.348	47.3	4.815	80.0
900.000	17.717	67.0	31.774	−66.9	0.490	46.3	5.476	83.2
1000.000	19.559	63.5	35.530	−78.0	0.701	51.3	6.128	88.3

S2, Y2
CONDITION
(V_{DS} = 10 V, V_{G2S} = 4 V, I_{DS} = 5 mA)

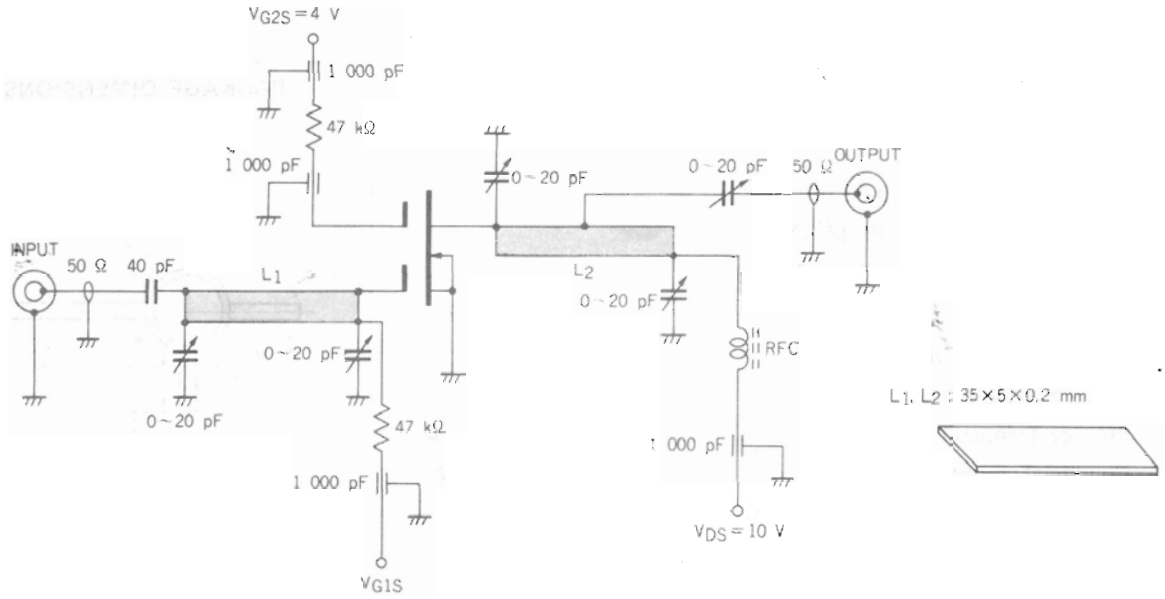
S2–MAGN AND ANGLES :

FREQ.	11		21		12		22	
200.000	0.976	−18.4	1.801	152.6	0.002	61.2	0.988	−7.8
300.000	0.944	−28.2	1.767	137.4	0.003	86.9	0.979	−11.6
400.000	0.920	−36.8	1.728	125.2	0.002	140.0	0.970	−15.7
500.000	0.879	−45.5	1.642	113.0	0.004	−159.0	0.947	−18.7
600.000	0.854	−54.5	1.629	100.5	0.008	−171.6	0.952	−21.5
700.000	0.808	−63.1	1.582	89.3	0.015	−173.5	0.959	−25.1
800.000	0.776	−71.2	1.551	77.4	0.022	−175.4	0.951	−28.1
900.000	0.734	−79.4	1.577	63.9	0.030	−178.6	0.974	−32.4
1000.000	0.695	−86.9	1.673	50.0	0.040	−179.7	1.013	−37.2

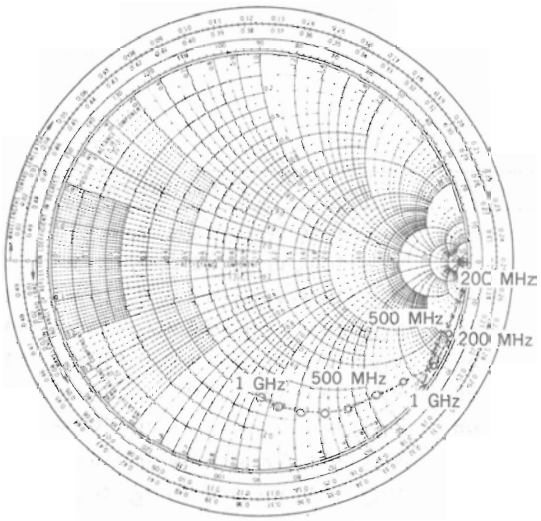
Y2–MAGN AND ANGLES :

FREQ.	11		21		12		22	
200.000	3.232	85.7	18.589	−14.5	0.019	−105.8	1.355	85.1
300.000	5.022	83.0	19.017	−23.3	0.028	−73.8	2.015	84.0
400.000	6.692	81.9	19.439	−29.6	0.021	−14.8	2.754	83.1
500.000	8.490	79.4	19.747	−36.8	0.050	51.2	3.340	79.6
600.000	10.398	78.4	20.652	−44.2	0.104	43.7	3.807	81.1
700.000	12.425	75.5	21.548	−50.9	0.210	46.2	4.407	82.2
800.000	14.458	73.5	22.769	−59.1	0.326	48.1	4.877	81.2
900.000	16.612	70.5	24.930	−68.6	0.468	48.8	5.534	84.5
1000.000	18.672	67.0	28.318	−79.2	0.684	51.2	6.221	88.5

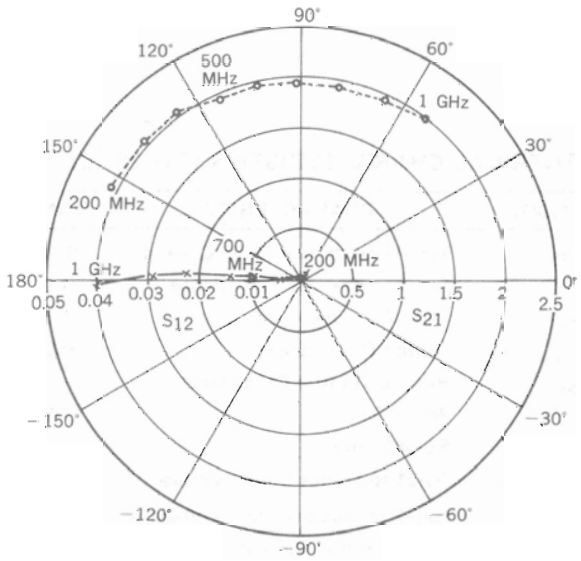
900 MHz G_{ps} & NF TEST CIRCUIT



V_{DS} = 10 V, V_{G2S} = 4 V, I_D = 10 mA



O:S_{11} ×:S_{22}



O:S_{21} ×:S_{12}

NEC
ELECTRON DEVICE

N-CHANNEL SILICON DUAL-GATE MOS FIELD EFFECT TRANSISTOR

3SK88

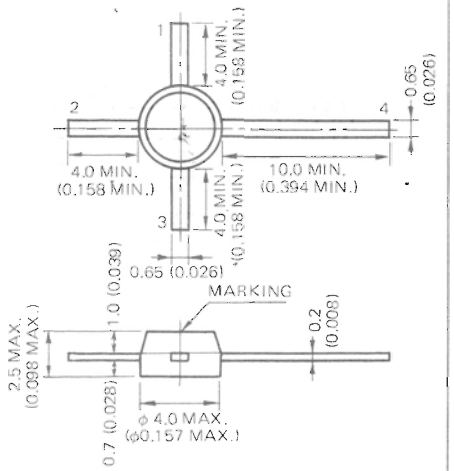
DISCONTINUED

DESCRIPTION The 3SK88 is designed for use in RF Amplifier for UHF TV Tuner.

FEATURES

- Low C_{rss} : 0.02 pF TYP.
- High G_{ps} : 16 dB TYP.
- Low NF : 3.8 dB TYP.

PACKAGE DIMENSIONS
in millimeters (inches)



1. GATE 2
2. GATE 1
3. SOURCE
4. DRAIN

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Channel Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 ° C)

- Total Power Dissipation . . . . . 200 mW

Maximum Voltages and Current (Ta = 25 °C)

- Drain to Source Voltage V_{DSX} . . . . . 20 V
- Gate1 to Source Voltage V_{G1S} . . . . . ±10 V
- Gate2 to Source Voltage V_{G2S} . . . . . ±10 V
- Drain Current I_D . . . . . 25 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	0.01		6.0	mA	V_{DS}=10 V, V_{G2S}=4.0 V, V_{G1S}=0
$\|y_{fs}\|$	Forward Transfer Admittance	14	17		mS	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 kHz
C_{iss}	Input Capacitance	1.5	2.0	2.5	pF	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 MHz
C_{oss}	Output Capacitance	0.5	1.0	1.3	pF	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 MHz
C_{rss}	Reverse Transfer Capacitance		0.02	0.03	pF	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=1.0 MHz
G_{ps}*	Power Gain	14	16	18	dB	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=900 MHz
NF*	Noise Figure		3.8	5.5	dB	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 mA, f=900 MHz
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−2.0	V	V_{DS}=10 V, V_{G2S}=4.0 V, I_D=10 μA
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−0.7	V	V_{DS}=10 V, V_{G1S}=4.0 V, I_D=10 μA
I_{G1SS}	Gate1 Reverse Current			20	nA	V_{DS}=0, V_{G1S}=±10 V, V_{G2S}=0
I_{G2SS}	Gate2 Reverse Current			20	nA	V_{DS}=0, V_{G2S}=±10 V, V_{G1S}=0
BV_{DSX}	Drain to Source Breakdown Voltage	20			V	V_{G1S}=V_{G2S}=−2.0 V, I_D=10 μA

* See Test Circuit

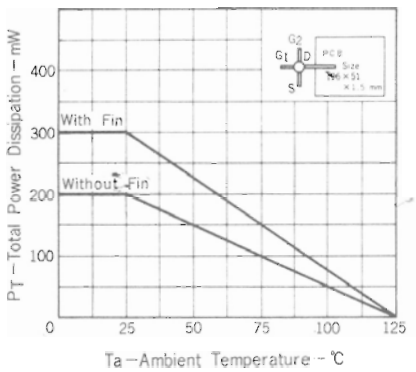
Classification of I_{DSS}

Rank	L	K
I_{DSS}(mA)	0.01 – 2.0	1.0 – 6.0

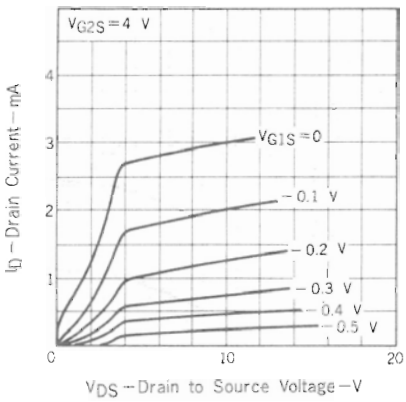
I_{DSS} Test Conditions: V_{DS} = 10 V, V_{G2S} = 4.0 V, V_{G1S} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

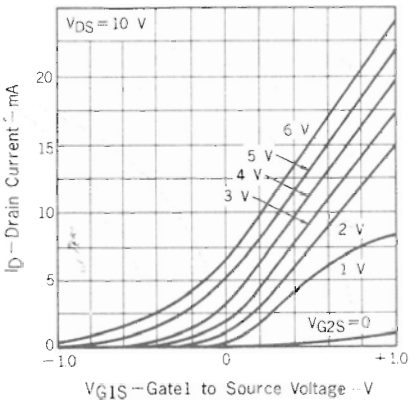
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



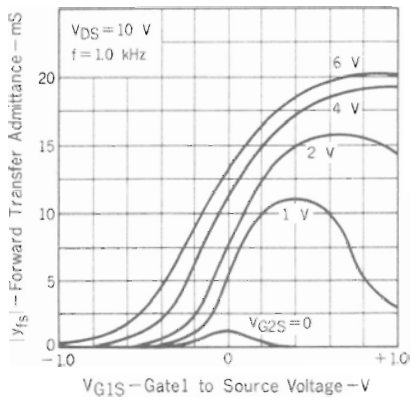
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



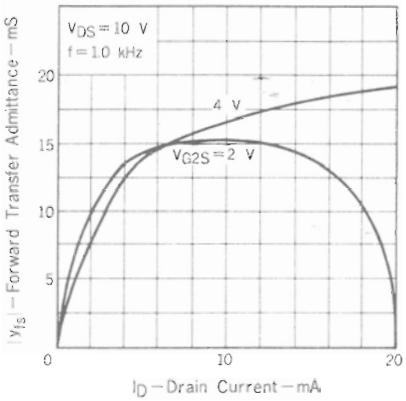
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



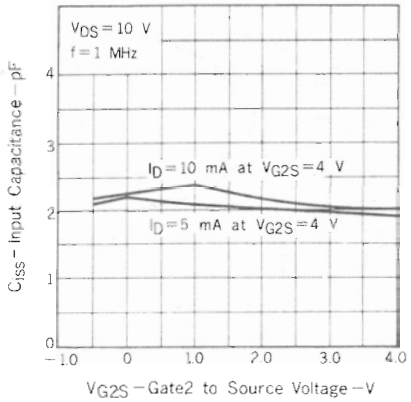
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



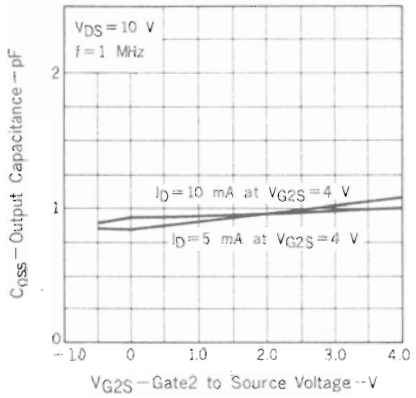
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE

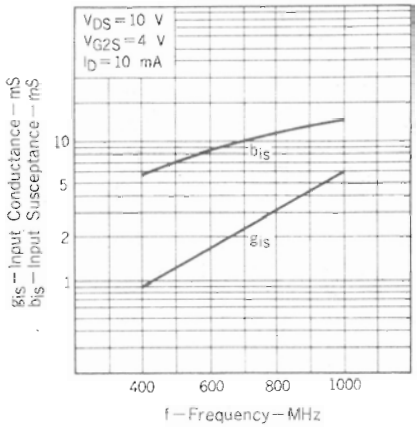


OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE

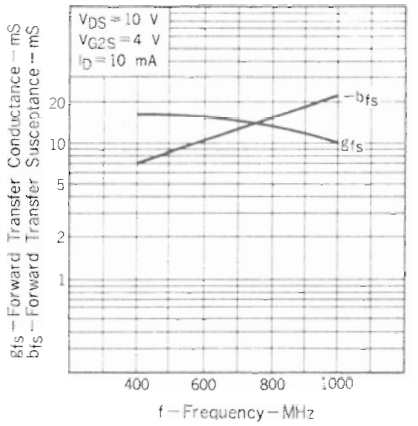


TYPICAL "Y" PARAMETERS

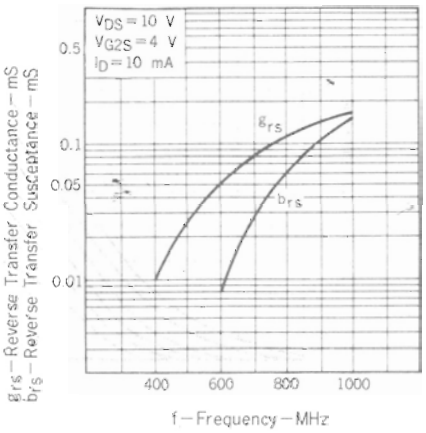
INPUT ADMITTANCE vs. FREQUENCY



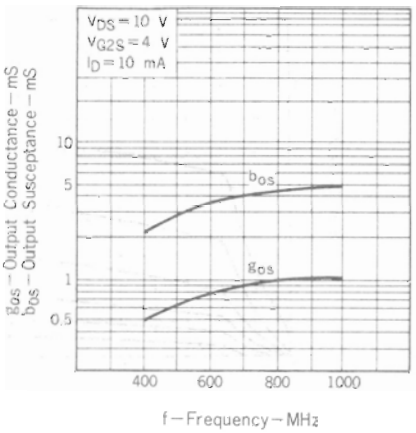
FORWARD TRANSFER ADMITTANCE vs. FREQUENCY



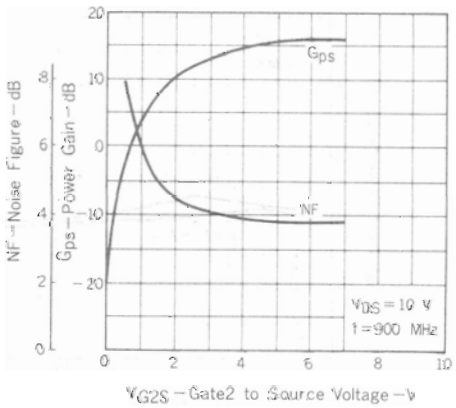
REVERSE TRANSFER ADMITTANCE vs. FREQUENCY



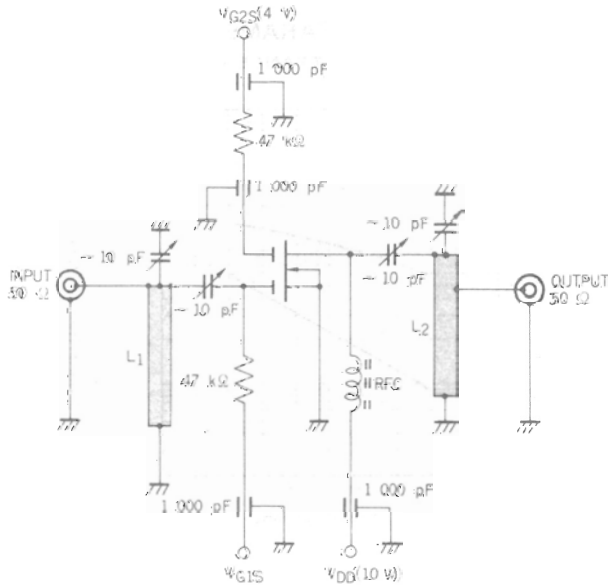
OUTPUT ADMITTANCE vs. FREQUENCY



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



900 MHz G_{ps} AND NF TEST CIRCUIT



L_1, L_2: .35 mm X 5.0 mm X 0.2 mm copper

NEC
ELECTRON DEVICE

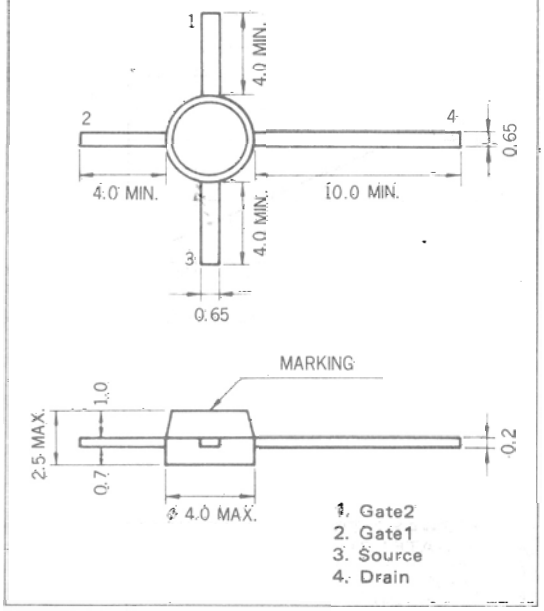
MOS FIELD EFFECT TRANSISTOR
3SK88A

FEATURES

- Suitable for use as RF amplifier in UHF TV tuner.
- Low C_{rss} : 0.02 pF TYP.
- High G_{ps} : 17.0 dB TYP.
- Low NF : 3.2 dB TYP.

NEW DEVICE

PACKAGE DIMENSIONS (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

V_{DSX}	Drain to Source Voltage	20	V
V_{G1S}	Gate1 to Source Voltage	±8 (±10)*	V
V_{G2S}	Gate2 to Source Voltage	±8 (±10)*	V
I_D	Drain Current	25	mA
P_T	Total Power Dissipation	200	mW
T_{ch}	Channel Temperature	125	°C
T_{stg}	Storage Temperature	−55 to +125	°C

*$R_L \geqq 10\ k\Omega$

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
BV_{DSX}	Drain to Source Breakdown Voltage	20			V	$V_{G1S} = V_{G2S} = -2$ V, $I_D = 10\ \mu A$
I_{DSS}	Drain Current	0.01		6	mA	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $V_{G1S} = 0$
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−2.0	V	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10\ \mu A$
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−0.7	V	$V_{DS} = 10$ V, $V_{G1S} = 4$ V, $I_D = 10\ \mu A$
I_{G1SS}	Gate1 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G1S} = \pm 10$ V, $V_{G2S} = 0$
I_{G2SS}	Gate2 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G2S} = \pm 10$ V, $V_{G1S} = 0$
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	14	17		mS	$V_{DS} = 5$ V, $V_{G2S} = 4$V, $I_D = 10$ mA, f = 1 kHz
C_{iss}	Input Capacitance	1.5	2.0	2.5	pF	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1 MHz
C_{oss}	Output Capacitance	0.5	1.0	1.5	pF	
C_{rss}	Reverse Transfer Capacitance		0.02	0.03	pF	
G_{ps}**	Power Gain	15.0	17.0		dB	$V_{DS} = 10$ V, $V_{G2S} = 4$ V $I_D = 10$ mA, f = 900 MHz
NF**	Noise Figure		3.2	5.0	dB	

I_{DSS} Classification

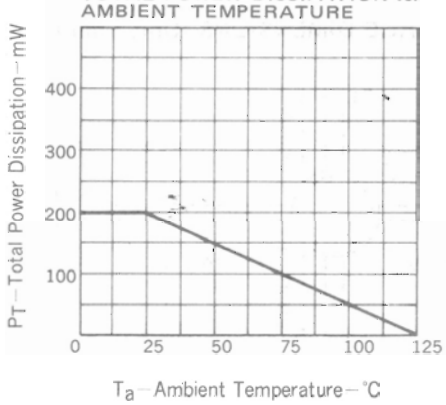
Marking	L	K
I_{DSS}	0.01 to 2	1 to 6

UNIT : mA

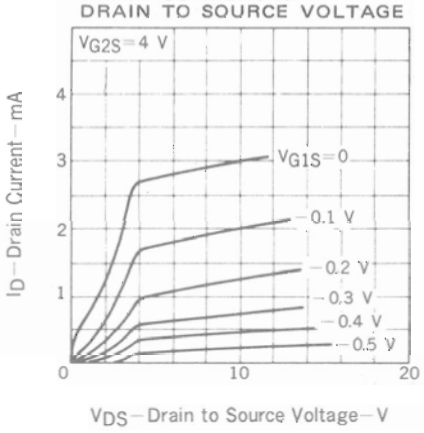
**See Test Circuit

TYPICAL CHARACTERISTICS (T_a = 25 °C)

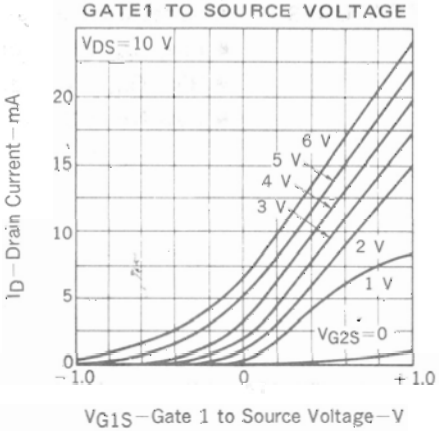
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



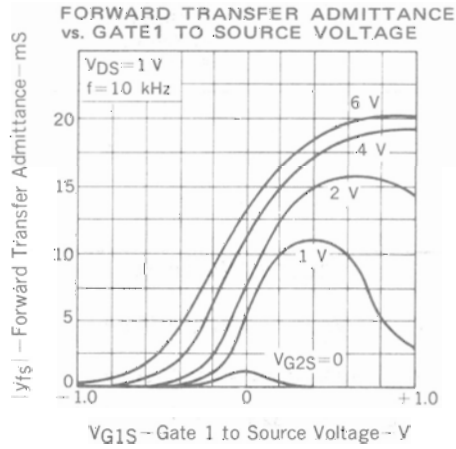
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



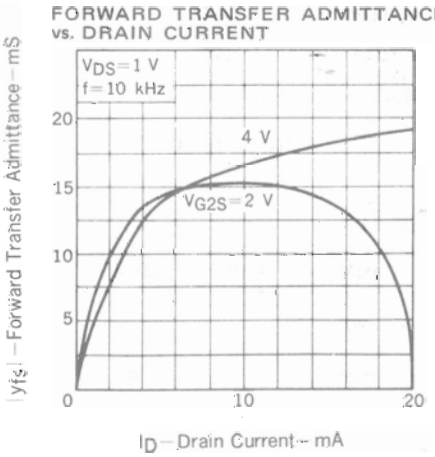
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



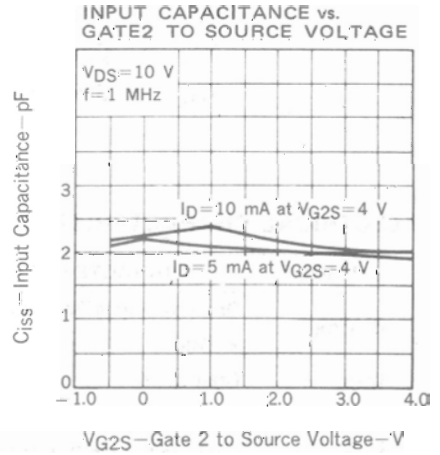
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



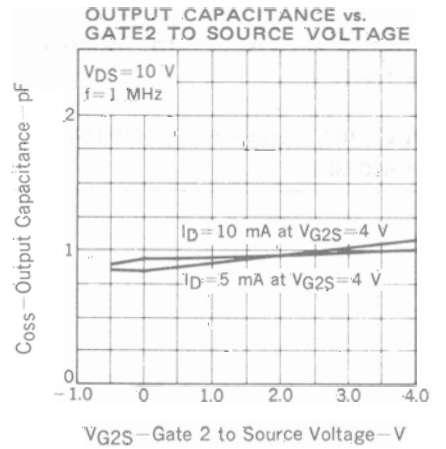
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



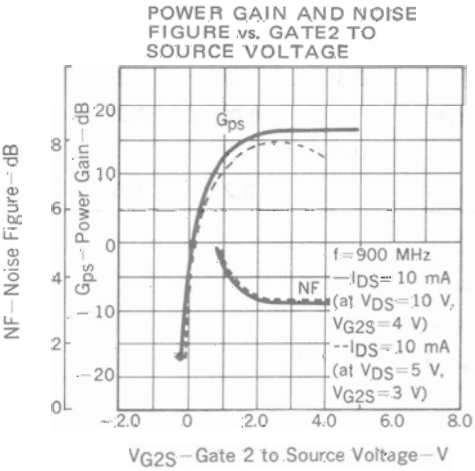
INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



S-PARAMETER, Y-PARAMETER

S1, Y1
CONDITION
(V_{DS} = 10 V, V_{G2S} = 4 V, I_{DS} = 10 mA)

S1–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	0.979	−14.4	1.616	159.1	0.002	74.5	0.990	−6.1
300.000	0.957	−22.0	1.602	147.3	0.003	80.9	0.977	−9.2
400.000	0.944	−28.7	1.603	138.1	0.002	102.8	0.971	−12.6
500.000	0.914	−35.5	1.536	128.9	0.002	142.8	0.946	−15.0
600.000	0.896	−42.6	1.539	119.0	0.004	168.2	0.949	−17.0
700.000	0.859	−49.6	1.510	110.3	0.006	−173.8	0.949	−20.2
800.000	0.830	−56.1	1.487	100.7	0.010	−174.9	0.934	−21.9
900.000	0.789	−63.0	1.481	90.5	0.015	−176.7	0.940	−25.2
1000.000	0.749	−69.8	1.516	81.5	0.020	−175.2	0.956	−28.2

Y1–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	2.517	85.0	16.573	−10.8	0.022	−95.4	1.059	84.5
300.000	3.877	83.4	16.936	−17.4	0.032	−83.9	1.609	81.6
400.000	5.123	83.1	17.403	−21.8	0.027	−57.2	2.208	82.1
500.000	6.439	81.0	17.463	−27.0	0.020	−13.0	2.682	77.7
600.000	7.866	80.5	18.104	−32.7	0.044	16.5	3.027	79.2
700.000	9.368	78.2	18.691	−37.2	0.078	38.7	3.582	80.4
800.000	10.825	76.6	19.451	−43.6	0.133	40.7	3.908	78.1
900.000	12.463	74.1	20.560	−50.3	0.203	42.6	4.444	79.9
1000.000	14.146	71.4	22.336	−56.1	0.299	47.2	4.921	82.1

S2, Y2
CONDITION
(V_{DS} = 10 V, V_{G2S} = 4 V, I_{DS} = 5 mA)

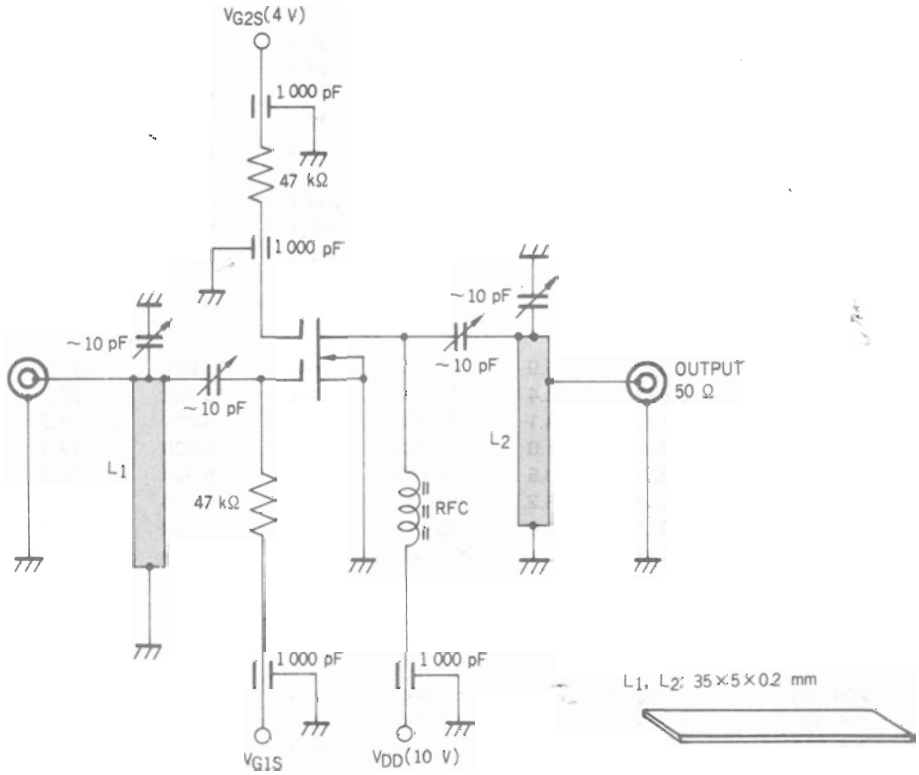
S2–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	0.982	−14.2	1.349	158.4	0.002	92.2	0.993	−6.0
300.000	0.959	−21.6	1.342	146.1	0.002	72.4	0.984	−8.9
400.000	0.947	−28.3	1.337	136.2	0.001	132.9	0.976	−12.3
500.000	0.915	−35.2	1.289	126.4	0.002	164.6	0.954	−14.8
600.000	0.897	−42.4	1.285	116.3	0.003	177.6	0.957	−16.8
700.000	0.858	−49.3	1.264	107.0	0.007	−172.7	0.957	−19.9
800.000	0.829	−56.1	1.237	96.9	0.012	−168.8	0.944	−21.8
900.000	0.786	−63.0	1.235	86.2	0.016	−177.6	0.949	−24.7
1000.000	0.746	−70.3	1.260	76.7	0.024	−176.7	0.964	−27.9

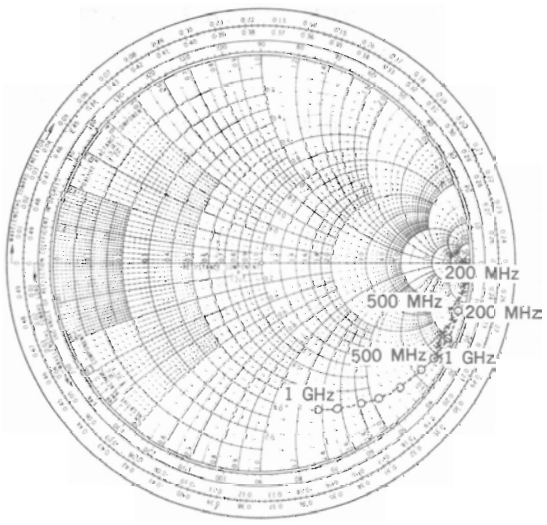
Y2–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	2.483	85.7	13.784	−11.7	0.017	−77.8	1.030	85.6
300.000	3.821	83.6	14.095	−19.0	0.023	−92.6	1.557	84.0
400.000	5.066	83.3	14.434	−24.0	0.015	−27.3	2.151	83.4
500.000	6.398	81.0	14.562	−29.6	0.026	8.6	2.628	79.3
600.000	7.803	80.5	14.991	−35.7	0.036	25.7	2.980	80.8
700.000	9.296	78.0	15.543	−40.8	0.086	39.5	3.521	81.7
800.000	10.811	76.6	16.102	−47.5	0.160	46.8	3.873	79.6
900.000	12.424	73.9	17.059	−54.7	0.223	41.4	4.338	81.4
1000.000	14.240	71.2	18.536	−60.8	0.346	45.7	4.845	83.4

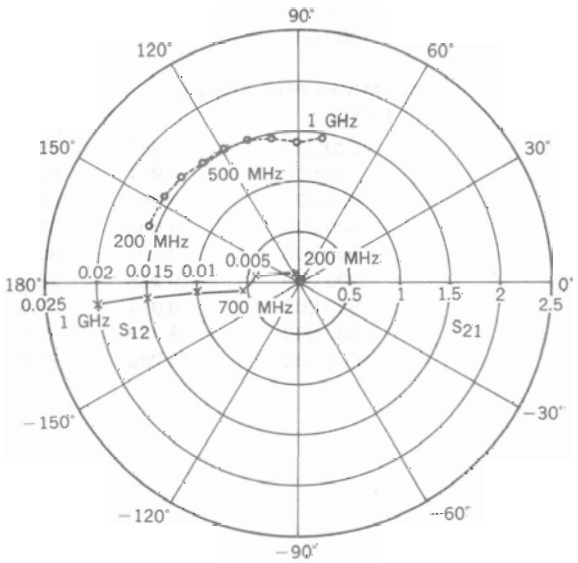
900 MHz G_{ps} AND NF TEST CIRCUIT



V_{DS}=10 V, V_{G2S}=4 V, I_D=10 mA



O:S_{11} ×:S_{22}



O:S_{21} ×:S_{12}

NEC
ELECTRON DEVICE

MOS FIELD EFFECT TRANSISTOR
3SK122

DESCRIPTION The 3SK122 is designed for use in RF Amplifier and MIXER for VHF TV Tuner.

FEATURES

- Suitable for Use as RF Amplifier & Mixer in VHF TV Tuner.
- High G_{PS} : 25 dB TYP. } at V_{DS} = 10 V, V_{G2} = 5.0 V,
- Low NF : 1.2 dB TYP. } I_D = 10 mA, f = 200 MHz
- High G_{PS} : 22 dB TYP. } at V_{DS} = 5 V, V_{G2} = 3 V,
- Low NF : 1.3 dB TYP. } I_D = 10 mA, f = 200 MHz

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +125 °C

Channel Temperature ..... +125 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation ..... 200 mW

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSX} Drain to Source Voltage ..... 20 V

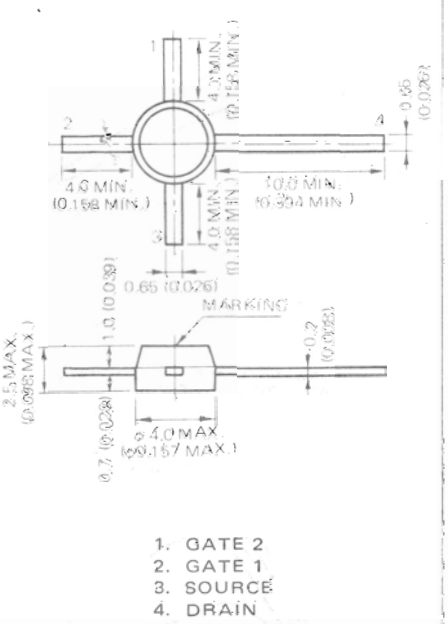
V_{G1S} Gate 1 to Source Voltage ..... ±8 V

V_{G2S} Gate 2 to Source Voltage ..... ±8 V

I_D Drain Current ..... 25 mA

PACKAGE DIMENSIONS

in millimeters (inches)



1. GATE 2
2. GATE 1
3. SOURCE
4. DRAIN

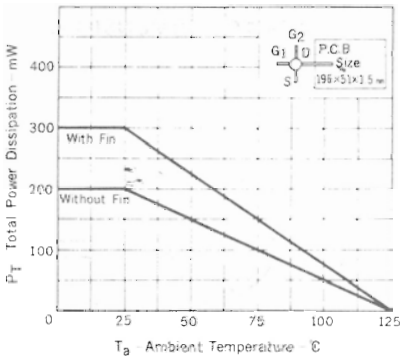
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
BV_{DSX}	Drain to Source Breakdown Voltage	20			V	V_{G1S} = −2 V, V_{G2S} = −2 V, I_D = 10 μA
I_{DSS}	Zero-Gate Voltage Drain Current	7.0		25	mA	V_{DS} = 6.0 V, V_{G1S} = 0, V_{G2S} = 3.0 V
$V_{G1S(off)}$	Gate 1 to Source Cutoff Voltage			−2.0	V	V_{DS} = 8.0 V, V_{G2S} = 0, I_D = 5.0 μA
$V_{G2S(off)}$	Gate 2 to Source Cutoff Voltage			−1.5	V	V_{DS} = 8.0 V, V_{G1S} = 0, I_D = 5.0 μA
I_{G1SS}	Gate 1 Reverse Current			±20	μA	V_{DS} = 0, V_{G1S} = 8 V, V_{G2S} = 0
I_{G2SS}	Gate 2 Reverse Current			±20	μA	V_{DS} = 0, V_{G1S} = 0, V_{G2S} = ±8 V
$\|Yfs\|$	Forward Transfer Admittance	22	28		mS	V_{DS} = 6.0 V, I_D = 10 mA, V_{G2S} = 3.0 V, f = 1 kHz
C_{iss}	Input Capacitance	4.0	5.0	6.5	pF	V_{DS} = 6.0 V, I_D = 10 mA, V_{G2S} = 3.0 V, f = 1 MHz
C_{oss}	Output Capacitance	2.2	2.9	3.7	pF	
C_{rss}	Reverse Transfer Capacitance		0.05	0.08	pF	
G_{PS}	Power Gain	20	25		dB	V_{DS} = 10 V, I_D = 10 mA, f = 200 MHz, V_{G2} = 5.0 V, See Test Circuit
NF	Noise Figure		1.2	2.5	dB	

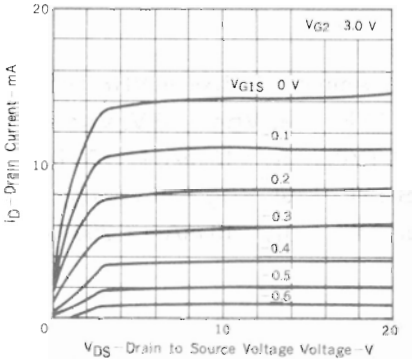
I_{DSS} Classification M : 7.0 − 13 mA L : 11 − 19 mA K : 17 − 25 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

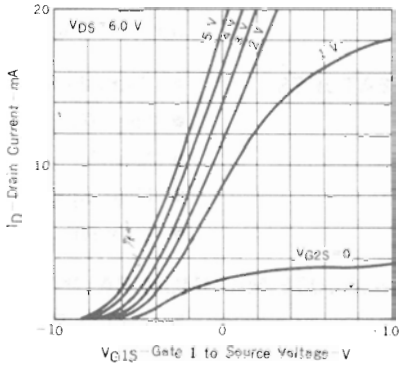
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



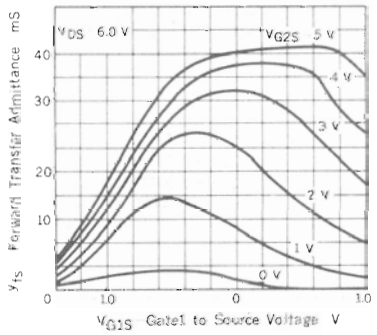
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



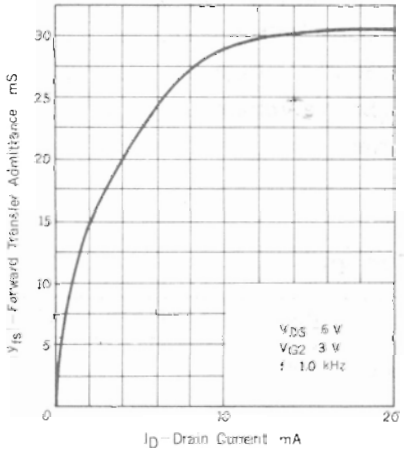
DRAIN CURRENT vs. GATE 1 TO SOURCE VOLTAGE



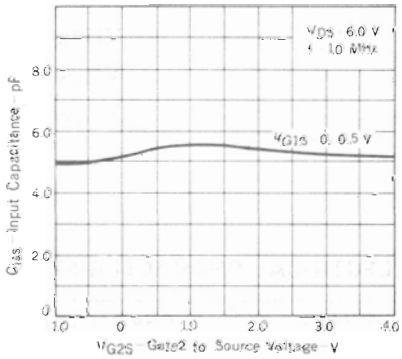
FORWARD TRANSFER ADMITTANCE vs. GATE 1 TO SOURCE VOLTAGE



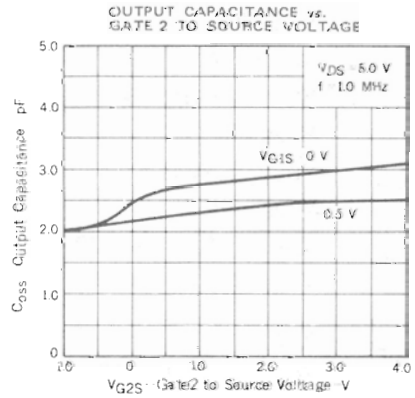
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



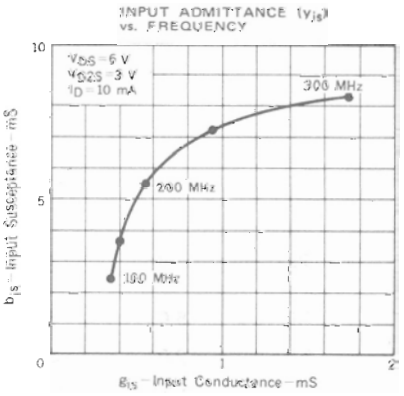
INPUT CAPACITANCE vs. GATE 2 TO SOURCE VOLTAGE



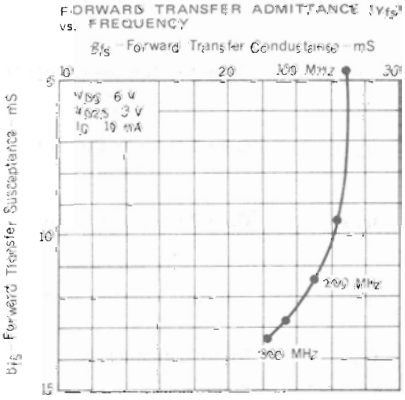
OUTPUT CAPACITANCE vs. GATE 2 TO SOURCE VOLTAGE



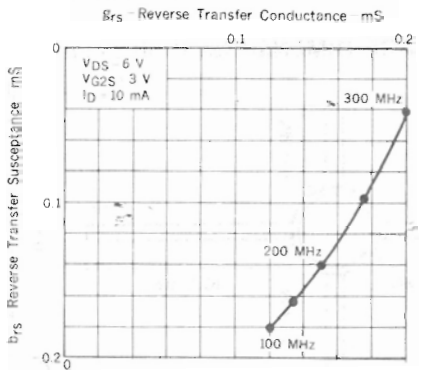
INPUT ADMITTANCE (y_{is}) vs. FREQUENCY



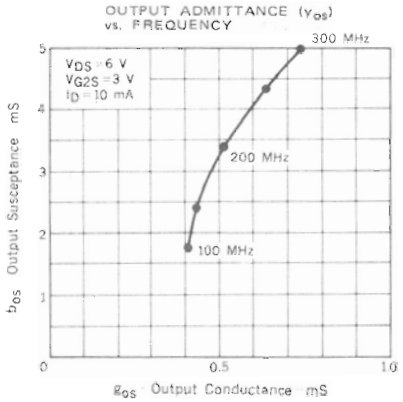
FORWARD TRANSFER ADMITTANCE (y_{fs}) vs. FREQUENCY



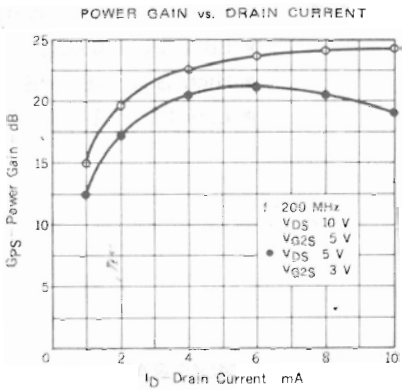
REVERSE TRANSFER ADMITTANCE (Y_{rs}) vs. FREQUENCY



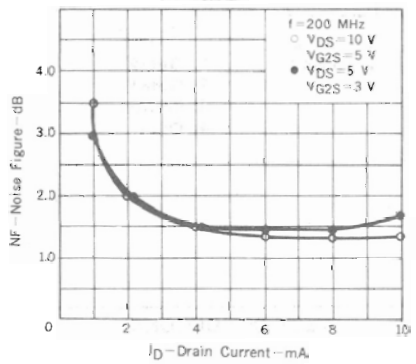
OUTPUT ADMITTANCE (Y_{os}) vs. FREQUENCY



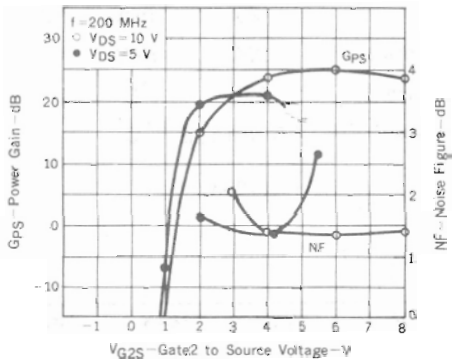
POWER GAIN vs. DRAIN CURRENT



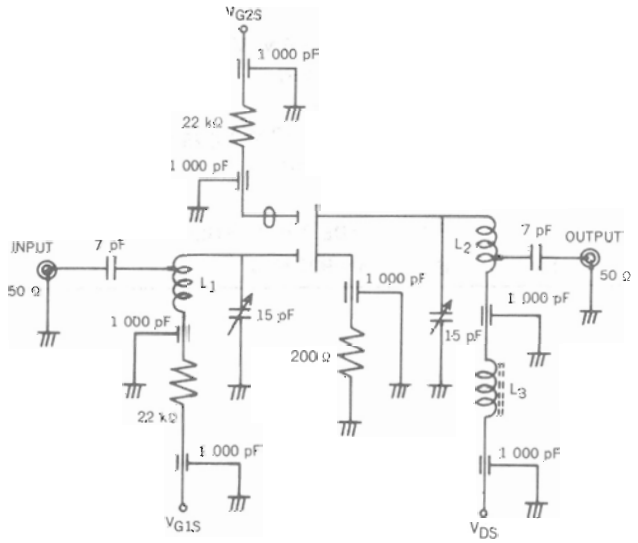
NOISE FIGURE vs DRAIN CURRENT



NOISE FIGURE, POWER GAIN vs. GATE 2 TO SOURCE VOLTAGE



200 MHz Power Gain & Noise Figure Test Circuit



TEST CONDITION

V_{DS} = 10 V, V_{G2S} = 5 V, I_D = 10 mA
f = 200 MHz
L_1 : φ 0.6 mm U.E.W. 7 mm 3T
L_2 : φ 0.6 mm U.E.W. 7 mm 3T
L_3 : RFC 2.2 μH

NEC
ELECTRON DEVICE

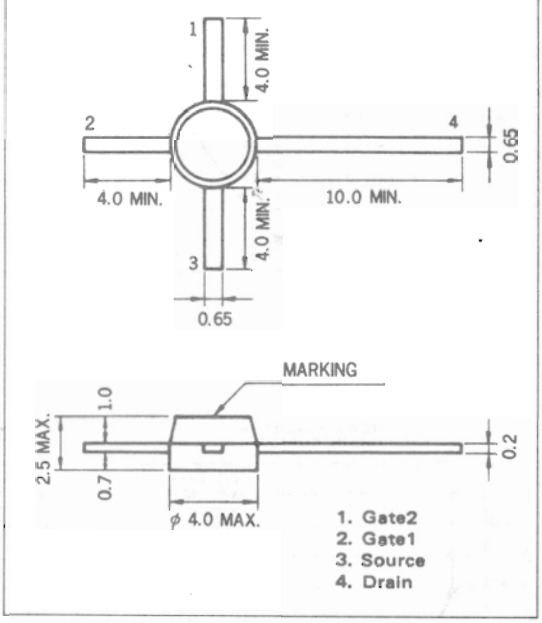
MOS FIELD EFFECT TRANSISTOR
3SK123A

FEATURES

- Suitable for use as RF amplifier in UHF TV tuner.
- Low C_{rss} : 0.02 pF TYP.
- High G_{ps} : 18.0 dB TYP.
- Low NF : 2.8 dB TYP.

NEW DEVICE

PACKAGE DIMENSIONS (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

V_{DSX}	Drain to Source Voltage	18	V
V_{G1S}	Gate1 to Source Voltage	±8 (±10)*	V
V_{G2S}	Gate2 to Source Voltage	±8 (±10)*	V
I_D	Drain Current	25	mA
P_T	Total Power Dissipation	200	mW
T_{ch}	Channel Temperature	125	°C
T_{stg}	Storage Temperature	−55 to +125	°C

*$R_L \geqq 10\ k\Omega$

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
BV_{DSX}	Drain to Source Breakdown Voltage	20			V	$V_{G1S} = V_{G2S} = -2$ V, $I_D = 10\ \mu A$
I_{DSS}	Drain Current	0.01		6	mA	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $V_{G1S} = 0$
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−2.0	V	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10\ \mu A$
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−0.7	V	$V_{DS} = 10$ V, $V_{G1S} = 4$ V, $I_D = 10\ \mu A$
I_{G1SS}	Gate1 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G1S} = \pm 8$ V, $V_{G2S} = 0$
I_{G2SS}	Gate2 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G2S} = \pm 8$ V, $V_{G1S} = 0$
$\|y_{fs}\|$	Forward Transfer Admittance	14	18		mS	$V_{DS} = 5$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1 kHz
C_{iss}	Input Capacitance	1.5		2.5	pF	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1 MHz
C_{oss}	Output Capacitance	0.5	1.0	1.5	pF	
C_{rss}	Reverse Transfer Capacitance		0.02	0.03	pF	
G_{ps}**	Power Gain	16.0	18.0		dB	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 900 MHz
NF**	Noise Figure		2.8	4.5	dB	

I_{DSS} Classification

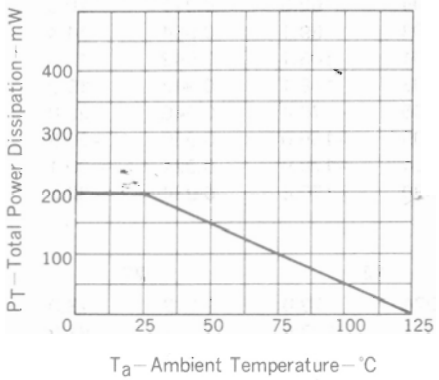
Marking	L	K
I_{DSS}	0.01 to 2	1 to 6

UNIT: mA

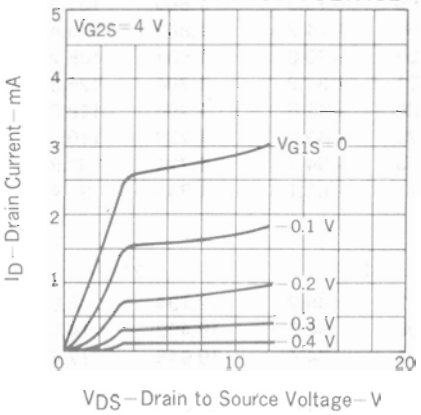
**See Test Circuit

TYPICAL CHARACTERISTICS (T_a = 25 °C)

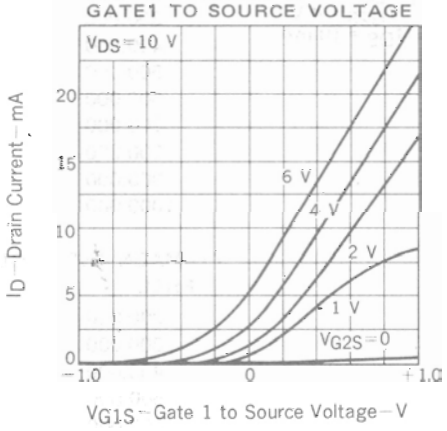
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



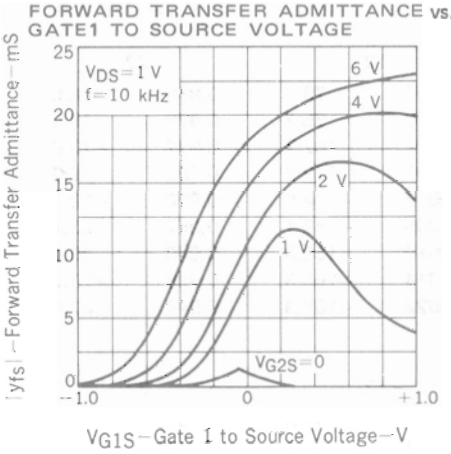
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



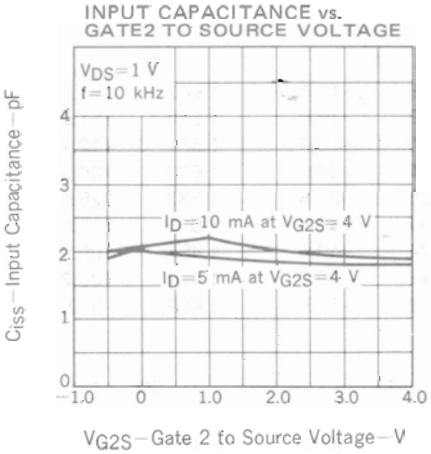
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



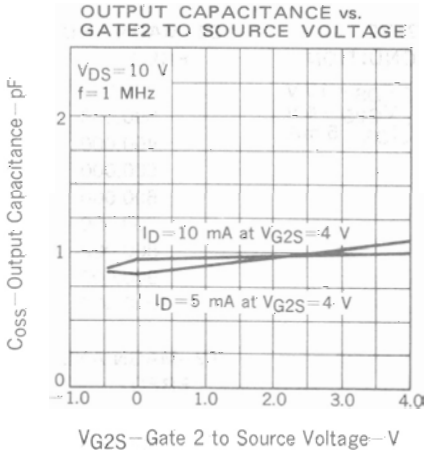
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



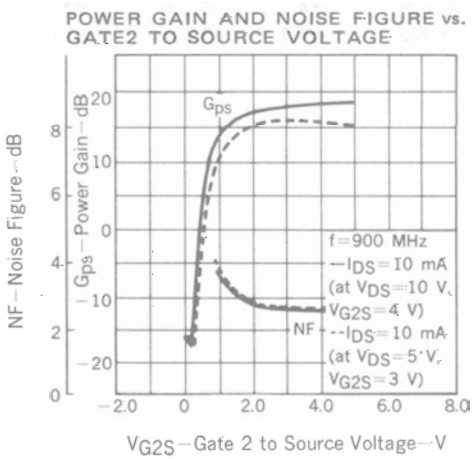
INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



S-PARAMETER, Y-PARAMETER

S1, Y1
CONDITION
V_{DS} = 10 V
V_{G2S} = 4 V
I_{DS} = 10 mA

S1–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	0.986	−12.5	1.868	161.7	0.002	92.4	0.975	−6.9
300.000	0.966	−18.9	1.860	151.3	0.004	62.3	0.971	−10.3
400.000	0.960	−24.9	1.863	143.4	0.003	89.1	0.964	−14.4
500.000	0.933	−30.6	1.801	135.2	0.001	103.1	0.942	−17.3
600.000	0.921	−37.2	1.794	126.3	0.003	148.1	0.943	−19.9
700.000	0.896	−42.8	1.766	118.8	0.005	−170.4	0.946	−23.8
800.000	0.870	−49.0	1.739	110.3	0.009	−165.0	0.930	−26.3
900.000	0.843	−54.7	1.724	101.8	0.014	−170.9	0.924	−30.1
1000.000	0.811	−61.1	1.748	95.4	0.020	−170.8	0.934	−33.5

Y1–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	2.173	86.2	19.194	−8.8	0.024	−78.0	1.212	78.0
300.000	3.306	84.2	19.492	−14.5	0.043	−103.5	1.793	81.2
400.000	4.404	84.4	19.945	−17.4	0.028	−71.7	2.531	81.6
500.000	5.496	82.2	20.116	−21.7	0.013	−53.9	3.093	78.5
600.000	6.769	82.0	20.593	−26.3	0.029	−4.5	3.552	79.8
700.000	7.925	80.3	21.067	−29.5	0.062	41.2	4.260	81.3
800.000	9.224	78.7	21.826	−34.4	0.110	50.2	4.746	79.3
900.000	10.472	77.0	22.764	−39.3	0.184	48.1	5.416	79.2
1000.000	12.012	74.8	24.431	−41.9	0.284	51.9	6.031	80.3

S2, Y2
CONDITION
V_{DS} = 10 V
V_{G2S} = 4 V
I_{DS} = 5 mA

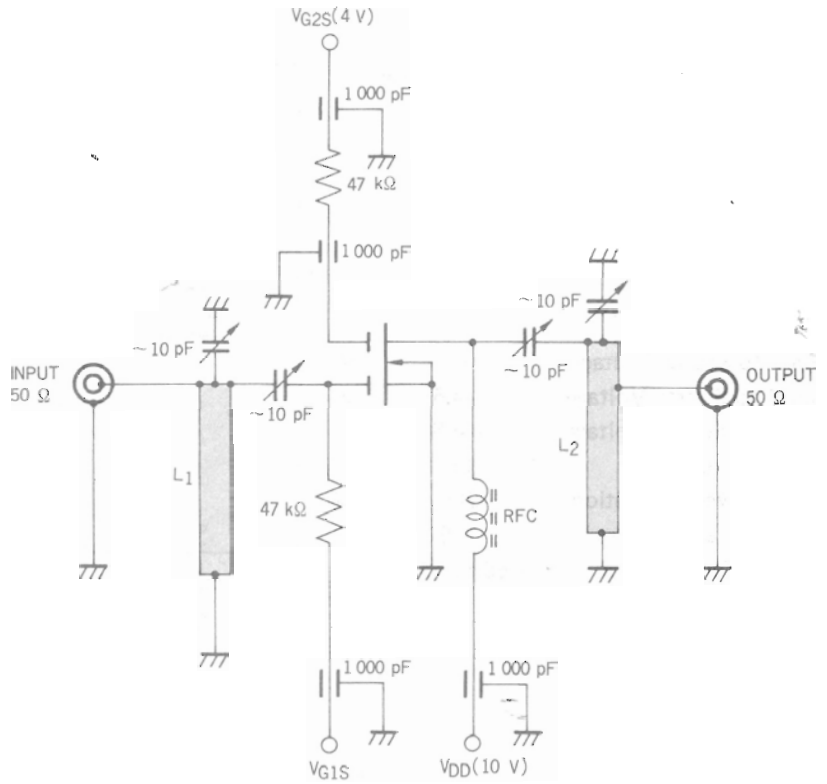
S2–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	0.986	−12.5	1.582	161.7	0.002	78.7	0.986	−6.6
300.000	0.968	−19.0	1.577	151.0	0.003	76.7	0.979	−10.0
400.000	0.960	−25.0	1.584	142.7	0.002	102.7	0.977	−13.8
500.000	0.934	−30.9	1.532	134.3	0.001	129.9	0.952	−16.9
600.000	0.925	−37.5	1.533	125.4	0.003	−164.5	0.956	−19.7
700.000	0.897	−43.7	1.510	117.5	0.005	−167.1	0.957	−23.1
800.000	0.874	−49.6	1.481	108.9	0.010	−159.9	0.940	−25.7
900.000	0.843	−56.0	1.470	100.2	0.014	−165.3	0.938	−29.2
1000.000	0.808	−62.5	1.489	93.5	0.022	−168.9	0.944	−32.6

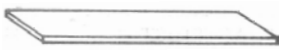
Y2–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	2.188	86.4	16.177	−8.9	0.021	−91.8	1.152	83.3
300.000	3.344	84.4	16.482	−14.8	0.034	−89.1	1.740	83.0
400.000	4.443	84.4	16.889	−18.3	0.022	−58.2	2.410	84.3
500.000	5.567	82.2	17.019	−22.5	0.013	−26.9	3.004	80.3
600.000	6.841	82.4	17.456	−27.0	0.031	43.0	3.507	82.0
700.000	8.100	80.6	17.927	−30.7	0.060	44.8	4.109	82.9
800.000	9.369	79.2	18.482	−35.7	0.119	55.4	4.608	80.6
900.000	10.792	77.4	19.349	−40.5	0.189	54.0	5.238	80.9
1000.000	12.372	75.1	20.835	−43.4	0.303	54.1	5.845	81.6

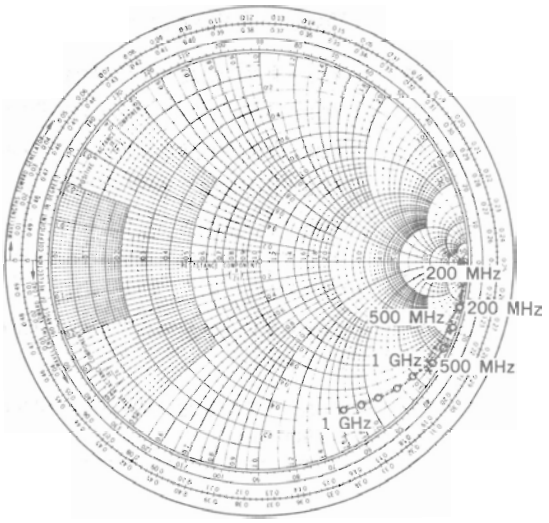
900 MHz G_{ps} AND NF TEST CIRCUIT



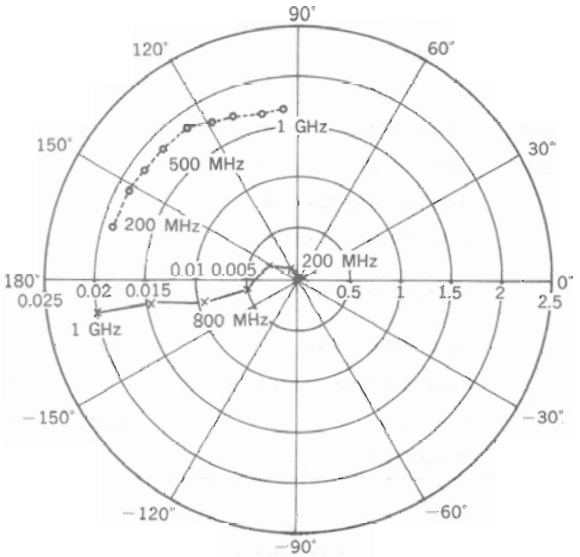
L1, L2: 35×5×0.2 mm



V_{DS} = 10 V, V_{G2S} = 4 V, I_D = 10 mA



O:S_{11} ×:S22



O:S_{21} ×:S_{12}

NEC
ELECTRON DEVICE

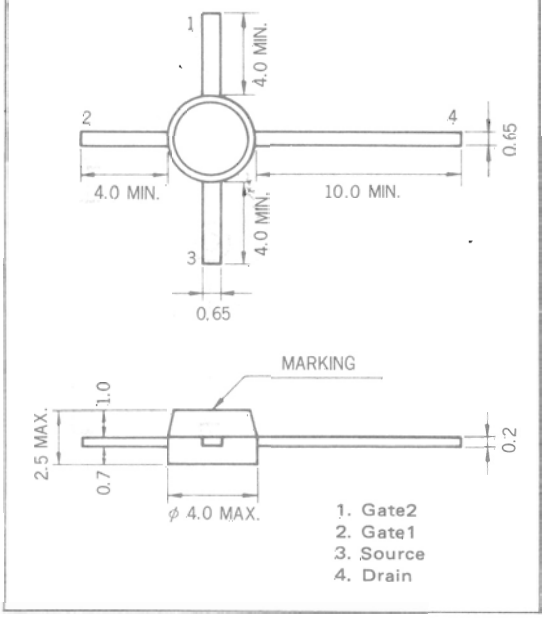
MES FIELD EFFECT TRANSISTOR
3SK124

NEW DEVICE

FEATURES

- Suitable for use as RF amplifier in UHF TV tuner.
- Low C_{rss} : 0.03 pF TYP.
- High G_{ps} : 20 dB TYP.
- Low NF : 1.3 dB TYP.

PACKAGE DIMENSIONS (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

V_{DSX}	Drain to Source Voltage	10	V
V_{G1S}	Gate1 to Source Voltage	−4.5	V
V_{G2S}	Gate2 to Source Voltage	−4.5	V
I_D	Drain Current	80	mA
P_T	Total Power Dissipation	200	mW
T_{ch}	Channel Temperature	125	°C
T_{stg}	Storage Temperature	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

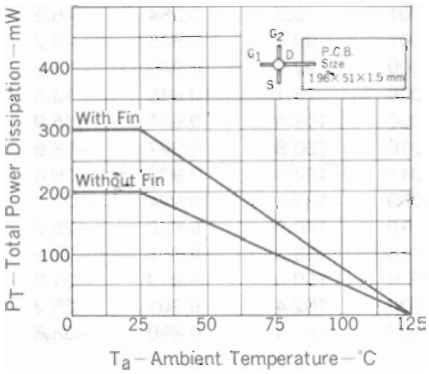
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
BV_{DSX}	Drain to Source Breakdown Voltage	10			V	V_{G1S} = −3 V, V_{G2S} = 0 V, I_D = 10 μA
I_{DSS}	Drain Current	10	40	80	mA	V_{DS} = 5 V, V_{G2S} = 0 V, V_{G1S} = 0
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−3.5	V	V_{DS} = 5 V, V_{G2S} = 0 V, I_D = 100 μA
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−3.5	V	V_{DS} = 5 V, V_{G1S} = 0 V, I_D = 100 μA
I_{G1SS}	Gate1 Reverse Current			20	A	V_{DS} = 0, V_{G1S} = −4 V, V_{G2S} = 0
I_{G2SS}	Gate2 Reverse Current			20	A	V_{DS} = 0, V_{G2S} = −4 V, V_{G1S} = 0
$\|Y_{fs}\|$	Forward Transfer Admittance	20	30		mS	V_{DS} = 5 V, V_{G2S} = 0 V, I_D = 10 mA f = 1 kHz
C_{iss}	Input Capacitance	1.5	2.0	2.5	pF	V_{DS} = 5 V, V_{G2S} = 0 V, I_D = 10 mA f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		0.03	0.04	pF	
G_{ps}	Power Gain	16.0	20.0		dB	V_{DS} = 5 V, V_{G2S} = 0 V, I_D = 10 mA f = 900 MHz
NF	Noise Figure		1.3	2.5	dB	

I_{DSS} Classification UNIT : mA

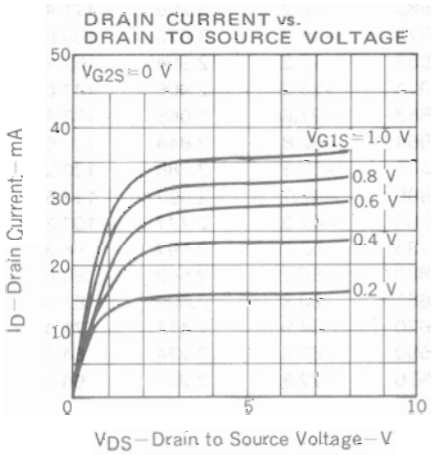
Marking	N	M	L	K
I_{DSS}	10 to 25	20 to 35	30 to 50	45 to 80

TYPICAL CHARACTERISTICS (T_a = 25 °C)

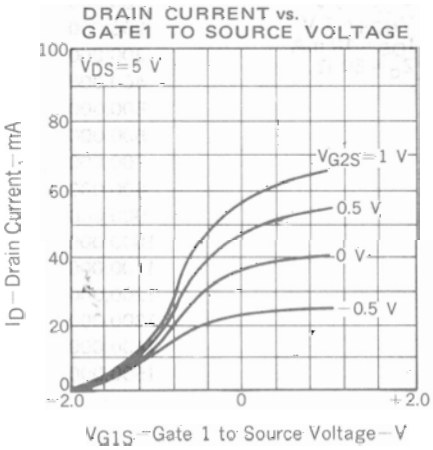
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



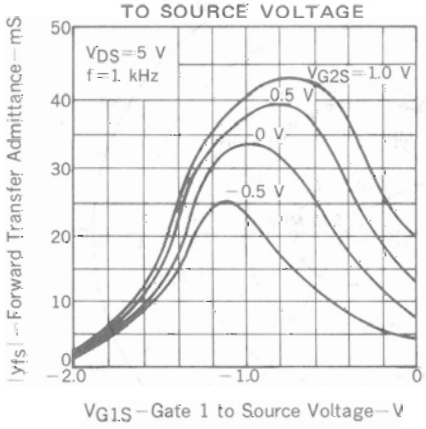
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



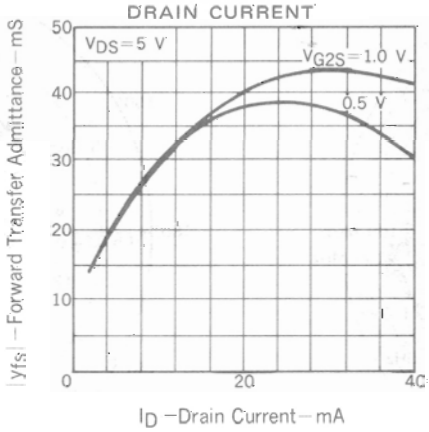
DRAIN CURRENT vs. GATE1 TO SOURCE VOLTAGE



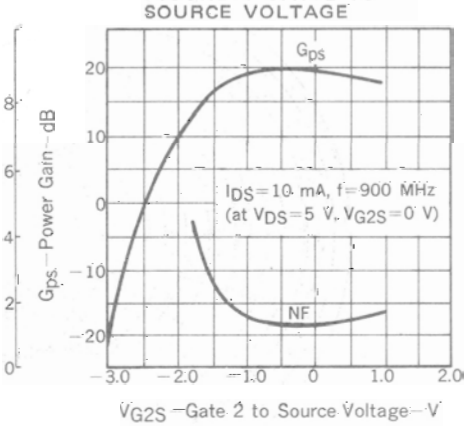
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



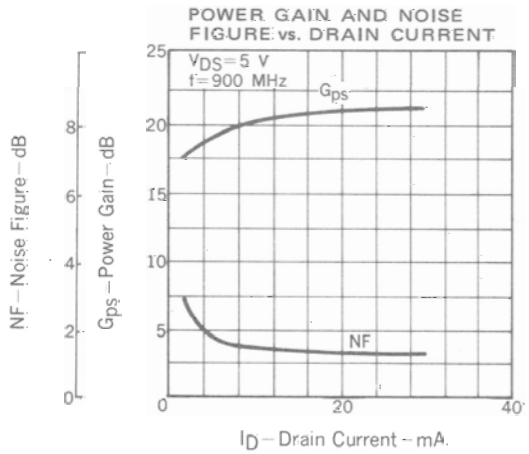
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



POWER GAIN AND NOISE FIGURE vs. DRAIN CURRENT

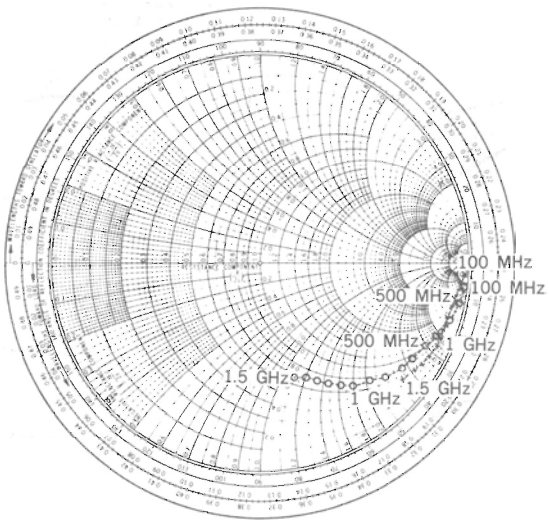


S-PARAMETER

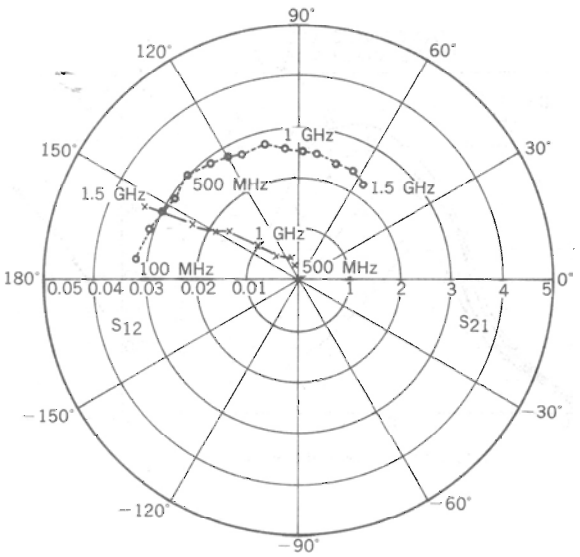
CONDITION: V_{DS} = 5 V, V_{G2S} = 1 V, I_{DS} = 10 mA, Z_o = 50 Ω

FREQ	S11		S21		S12		S22	
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100.000	0.988	−6.2	3.200	171.4	0.013	−108.1	0.987	−2.6
200.000	0.978	−11.7	3.073	160.6	0.012	18.6	0.954	−4.3
300.000	0.937	−17.2	2.994	152.9	0.001	9.9	0.954	−6.5
400.000	0.914	−23.3	2.906	147.0	0.007	98.2	0.945	−9.0
500.000	0.888	−27.6	3.066	137.4	0.009	92.2	0.949	−11.3
600.000	0.864	−32.8	2.844	127.6	0.006	75.1	0.945	−13.5
700.000	0.837	−37.3	2.789	120.0	0.008	102.4	0.931	−15.9
800.000	0.805	−42.7	2.697	114.5	0.010	100.8	0.927	−18.5
900.000	0.762	−47.2	2.777	103.3	0.011	134.3	0.928	−20.8
1000.000	0.733	−52.8	2.597	96.3	0.009	132.2	0.924	−22.7
1100.000	0.689	−56.7	2.549	88.6	0.010	140.9	0.920	−25.6
1200.000	0.651	−60.8	2.509	81.3	0.018	138.3	0.917	−28.9
1300.000	0.620	−64.9	2.411	71.4	0.019	150.0	0.913	−31.8
1400.000	0.590	−68.6	2.274	64.2	0.023	152.4	0.901	−35.2
1500.000	0.570	−72.8	2.241	56.3	0.033	154.4	0.890	−38.8

V_{DS} = 5 V, V_{G2S} = 1 V, I_D = 10 mA

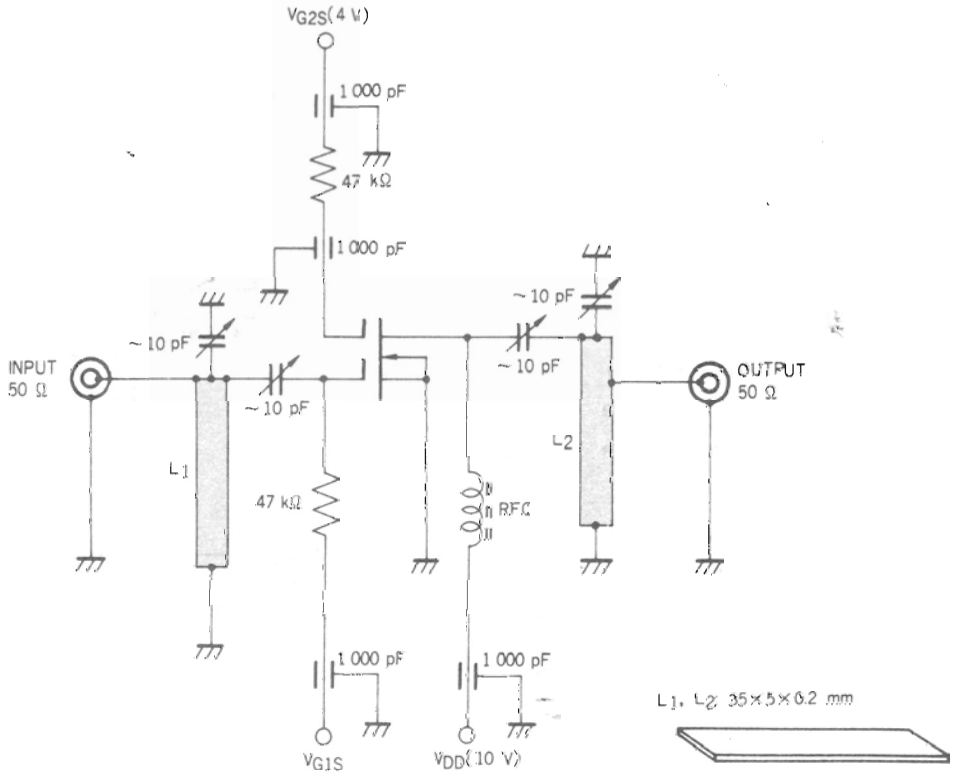


O:S_{11} ×:S_{22}



O:S_{21} ×:S_{12}

900 MHz G_{ps} AND NF TEST CIRCUIT



NEC
ELECTRON DEVICE

MOS FIELD EFFECT TRANSISTOR

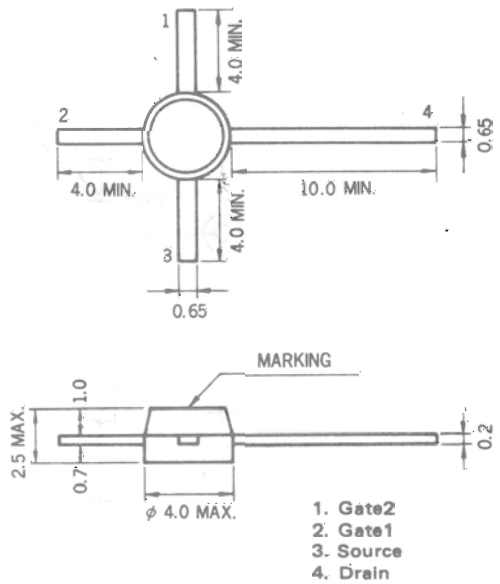
3SK161A

NEW DEVICE

FEATURES

- Suitable for use as RF amplifier in UHF TV tuner. (RF Amp. for half wave length resonator : λ/2)
- Low C_{rss} : 0.02 pF TYP.
- High G_{ps} : 22.5 dB TYP.
- Low NF : 2.5 dB TYP.

PACKAGE DIMENSIONS (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

V_{DSX}	Drain to Source Voltage	18	V
V_{G1S}	Gate1 to Source Voltage	±8 (±10)*	V
V_{G2S}	Gate2 to Source Voltage	±8 (±10)*	V
I_D	Drain Current	25	mA
P_T	Total Power Dissipation	200	mW
T_{ch}	Channel Temperature	125	°C
T_{stg}	Storage Temperature	−55 to +125	°C

*$R_L \geqq 10\ k\Omega$

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
BV_{DSX}	Drain to Source Breakdown Voltage	18	22		V	$V_{G1S} = V_{G2S} = -2$ V, $I_D = 10\ \mu A$
I_{DSX}	Drain Current	0.5		8	mA	$V_{DS} = 5$ V, $V_{G2S} = 4$ V, $V_{G1S} = 0.5$ V
$V_{G1S(off)}$	Gate1 to Source Cutoff Voltage			−2.0	V	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10\ \mu A$
$V_{G2S(off)}$	Gate2 to Source Cutoff Voltage			−0.7	V	$V_{DS} = 10$ V, $V_{G1S} = 4$ V, $I_D = 10\ \mu A$
I_{G1SS}	Gate1 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G1S} = \pm 8$ V, $V_{G2S} = 0$
I_{G2SS}	Gate2 Reverse Current			±20	nA	$V_{DS} = 0$, $V_{G2S} = \pm 8$ V, $V_{G1S} = 0$
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	24.0	27.5		mS	$V_{DS} = 5$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1.0 kHz
C_{iss}	Input Capacitance	1.5	2.5	3.5	pF	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 1 MHz
C_{oss}	Output Capacitance	0.5	1.3	2.5	pF	
C_{rss}	Reverse Transfer Capacitance		0.02	0.03	pF	
G_{ps}**	Power Gain	20.0	22.5		dB	$V_{DS} = 10$ V, $V_{G2S} = 4$ V, $I_D = 10$ mA, f = 900 MHz
NF**	Noise Figure		2.5	4.5	dB	

I_{DSX} Classification

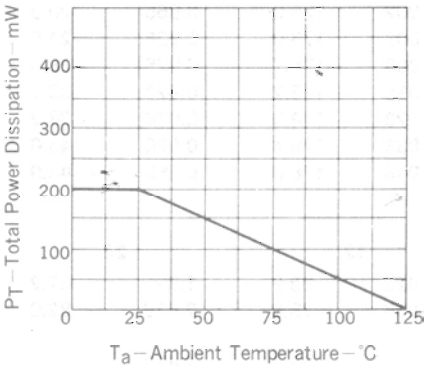
Marking	L	K
I_{DSX}	0.5 to 5	3 to 8

UNIT: mA

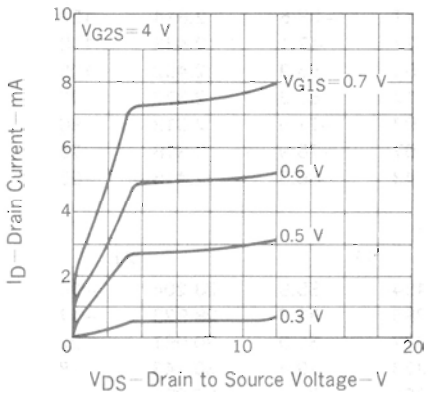
**See Test Circuit.

TYPICAL CHARACTERISTICS (T_a = 25 °C)

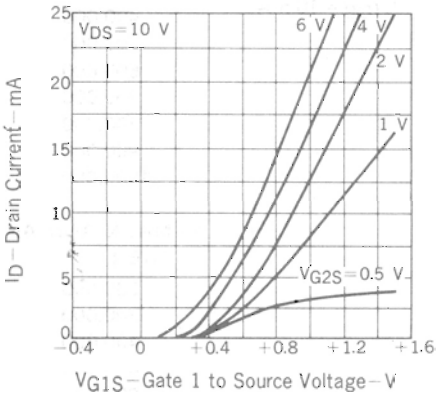
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



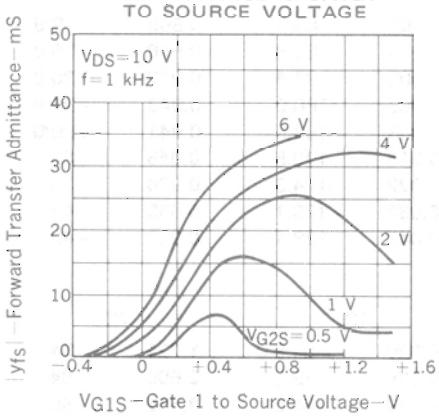
DRAIN CURRENT vs DRAIN TO SOURCE VOLTAGE



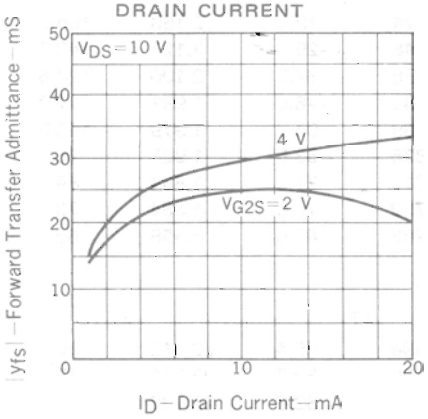
DRAIN CURRENT vs GATE1 TO SOURCE VOLTAGE



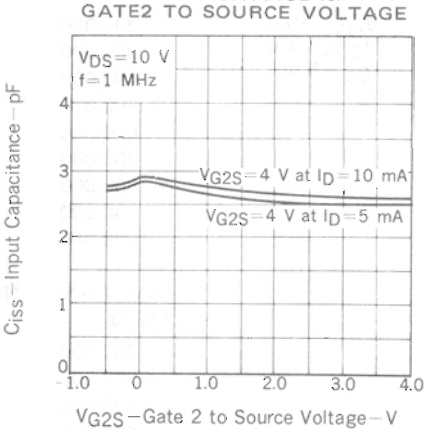
FORWARD TRANSFER ADMITTANCE vs. GATE1 TO SOURCE VOLTAGE



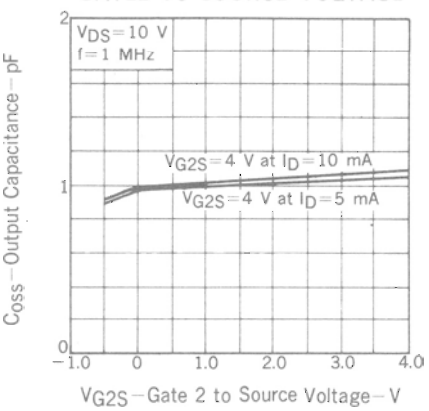
FORWARD TRANSFER ADMITTANCE vs DRAIN CURRENT



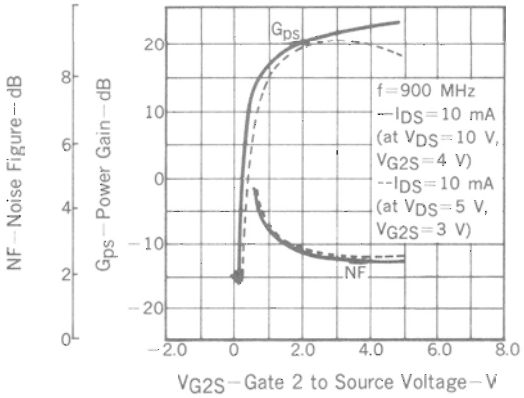
INPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



OUTPUT CAPACITANCE vs. GATE2 TO SOURCE VOLTAGE



POWER GAIN AND NOISE FIGURE vs. GATE2 TO SOURCE VOLTAGE



S-PARAMETER, Y-PARAMETER

S1, Y1
CONDITION
(V_{DS} = 10 V, V_{G2S} = 4 V, I_{DS} = 10 mA)

S–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	0.975	–19.7	2.702	154.8	0.002	71.5	0.976	–9.9
300.000	0.939	–29.7	2.650	140.8	0.003	79.7	0.968	–14.9
400.000	0.917	–38.5	2.614	129.4	0.002	125.3	0.955	–20.3
500.000	0.877	–47.1	2.483	118.3	0.003	176.0	0.926	–24.8
600.000	0.858	–55.9	2.462	106.9	0.008	–174.7	0.925	–28.6
700.000	0.817	–63.9	2.377	96.9	0.015	–175.2	0.927	–33.7
800.000	0.797	–71.5	2.313	86.4	0.023	–174.5	0.918	–38.2
900.000	0.767	–78.9	2.316	75.5	0.033	178.4	0.920	–43.6
1000.000	0.743	–86.3	2.415	65.6	0.046	176.8	0.955	–48.9

Y–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	3.454	85.9	28.204	–10.6	0.026	–93.9	1.721	82.2
300.000	5.285	82.7	28.923	–17.6	0.036	–78.8	2.579	82.9
400.000	7.022	81.9	30.061	–22.3	0.018	–26.4	3.603	82.2
500.000	8.823	79.4	30.743	–28.1	0.038	29.7	4.452	78.8
600.000	10.726	78.6	32.286	–34.0	0.104	44.5	5.155	79.1
700.000	12.673	75.7	33.758	–38.9	0.211	48.9	6.075	79.7
800.000	14.582	74.2	35.422	–45.0	0.346	54.1	6.881	78.5
900.000	16.513	71.5	38.596	–51.9	0.554	51.0	7.772	78.2
1000.000	18.619	68.4	43.298	–57.8	0.826	53.5	8.531	80.2

S2, Y2
CONDITION
(V_{DS} = 10 V, V_{G2S} = 4 V, I_{DS} = 5 mA)

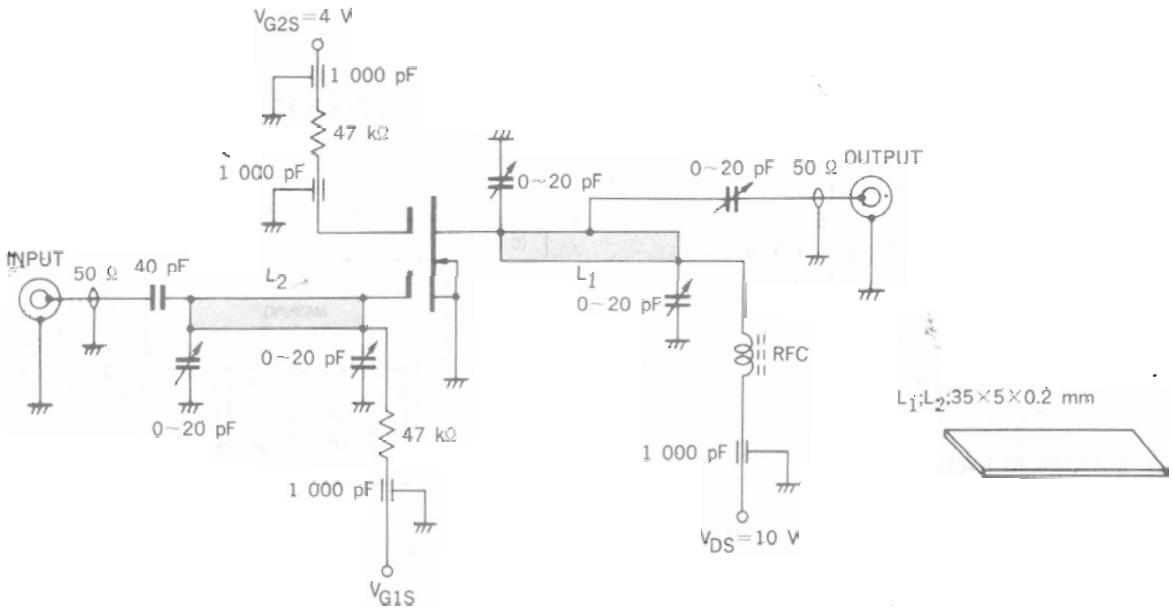
S–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	0.974	–19.3	2.150	154.7	0.002	80.8	0.983	–9.9
300.000	0.948	–29.1	2.127	140.5	0.003	86.6	0.976	–15.0
400.000	0.925	–37.9	2.100	128.6	0.002	97.4	0.972	–20.2
500.000	0.890	–46.6	1.991	117.3	0.003	180.0	0.943	–24.8
600.000	0.869	–55.3	1.979	105.8	0.008	–164.5	0.941	–29.0
700.000	0.835	–63.5	1.920	95.3	0.015	–173.5	0.945	–34.2
800.000	0.812	–71.2	1.864	84.5	0.022	–174.3	0.934	–38.7
900.000	0.782	–79.0	1.864	73.7	0.032	–179.1	0.939	–44.2
1000.000	0.763	–86.6	1.958	63.5	0.047	178.1	0.967	–49.8

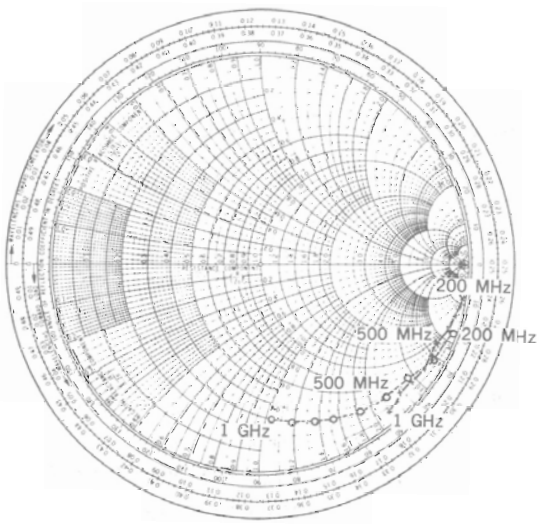
Y–MAGN AND ANGLES :

FREQ	11		21		12		22	
200.000	3.394	85.4	22.312	–10.9	0.020	–84.8	1.721	84.5
300.000	5.180	83.7	23.013	–18.1	0.035	–72.0	2.600	84.8
400.000	6.885	82.6	23.726	–23.4	0.019	–54.5	3.552	85.2
500.000	8.698	80.5	24.205	–28.9	0.037	33.7	4.431	81.5
600.000	10.581	79.6	25.547	–34.8	0.098	54.9	5.212	81.6
700.000	12.524	77.3	26.668	–39.9	0.208	51.4	6.143	82.2
800.000	14.458	75.8	27.981	–46.2	0.333	55.1	6.967	81.1
900.000	16.573	73.3	30.497	–52.3	0.530	54.9	7.939	81.1
1000.000	18.728	70.8	34.649	–58.0	0.829	56.7	8.826	82.5

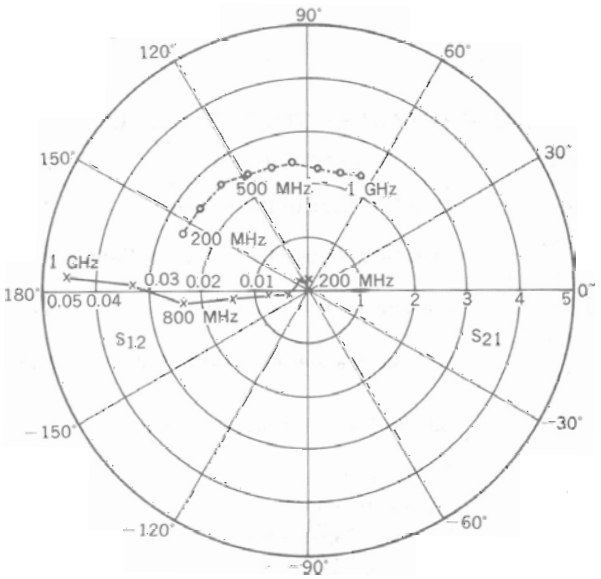
900 MHz G_{ps} & FN TEST CIRCUIT



V_{DS} = 10 V, V_{G2S} = 4 V, I_D = 10 mA



O:S_{11} ×:S_{22}



O:S_{21} ×:S_{12}

NEC
ELECTRON DEVICE

N-CHANNEL SILICON DUAL JUNCTION FIELD EFFECT TRANSISTOR

μPA68H

DESCRIPTION The μPA68H is designed for use in the top stage for differential amplifier of a stereo main amplifier.

FEATURES

- Excellent pair balance
  ΔV_{GS} = 20 mV MAX.
  @V_{DS} = 10 V, I_D = 1.0 mA
  $\Delta V_{GS} = V_{GS(L)} - V_{GS(S)}$
  $|Y_{fs}|$ Ratio; 0.95 MIN.
  @V_{DS} = 10 V, I_D = 1.0 mA
- High bleakdown voltage.
  $V_{GDO} > 50$ V

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 250 mW/Unit

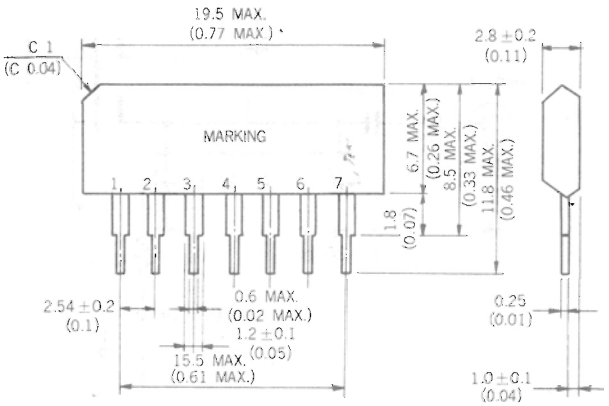
Maximum Voltages and Currents (Ta = 25 °C)

V_{GDO}	Gate to Drain Voltage	−50	V
V_{GSO}	Gate to Source Voltage	−50	V
V_{DSX}*	Drain to Source Voltage	50	V
I_D	Drain Current	30	mA
I_G	Gate Current	10	mA

* V_{GS} = −3.0 V

PACKAGE DIMENSIONS

in millimeters (inches)



1. DRAIN 1
2. GATE 1
3. SOURCE 1
4. SUB.
5. SOURCE 2
6. GATE 2
7. DRAIN 2

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{DSS}	Zero-Gate Voltage Drain Current	1.0		18	mA	V_{DS}=10 V, V_{GS}=0
$\frac{I_{DSS(S)}}{I_{DSS(L)}}$	Zero-Gate Voltage Drain Current Ratio	0.9		1.0		V_{DS}=10 V, V_{GS}=0 $I_{DSS(S)}/I_{DSS(L)}$*
$\lvert Y_{fs}\rvert$	Forward Transfer Admittance	5.0	7.0		mS	V_{DS}=10 V, I_D=1.0 mA, f=1.0 kHz
$\frac{\lvert Y_{fs}\rvert_{(S)}}{\lvert Y_{fs}\rvert_{(L)}}$	Forward Transfer Admittance Ratio	0.95		1.0		V_{DS}=10 V, I_D=1.0 mA, f=1.0 kHz $\lvert Y_{fs}\rvert_{(S)}/\lvert Y_{fs}\rvert_{(L)}$*
ΔV_{GS}	Gate to Source Voltage Difference		3.0	20	mV	V_{DS}=10 V, I_D=1.0 mA $\Delta V_{GS} = V_{GS(L)} - V_{GS(S)}$*
NV	Noise Voltage		25	35	mV	See Test Circuit
C_{iss}	Input Capacitance		15		pF	V_{DS}=10 V, V_{GS}=0, f=1.0 MHz
C_{rss}	Feedback Capacitance		3.0		pF	V_{DS}=10 V, V_{GS}=0, f=1.0 MHz
$V_{GS(off)}$	Gate to Source Cutoff Voltage	−0.15		−2.5	V	V_{DS}=10 V, I_D=10 μA
I_{GSS}	Gate Cutoff Current			−1.0	nA	V_{GS}=−20 V, V_{DS}=0

*(S) : The Smaller Value, (L) : The Larger of the pair

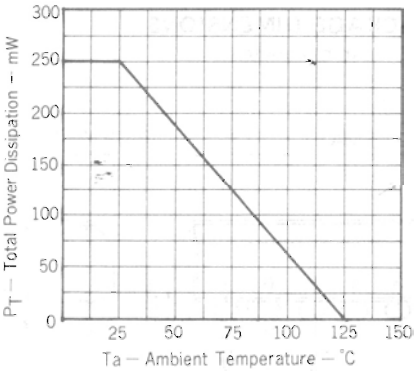
Classification of I_{DSS}

Rank	K	L	M	N
I_{DSS}(mA)	1.0 – 6.0	5.0 – 10	9.0 – 14	13 – 18

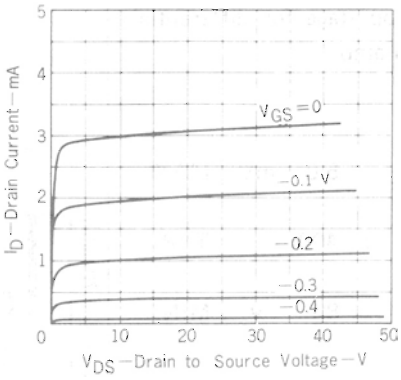
I_{DSS} Test Conditions : V_{DS} = 10 V, V_{GS} = 0

TYPICAL CHARACTERISTICS (Ta = 25 °C)

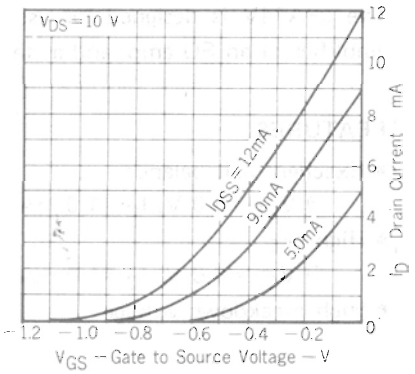
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



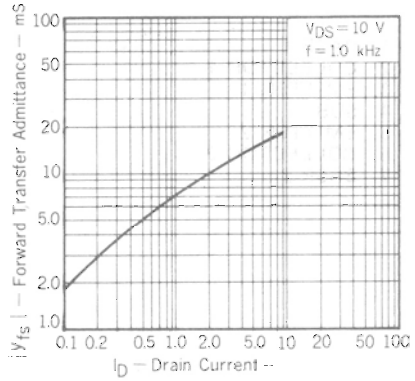
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



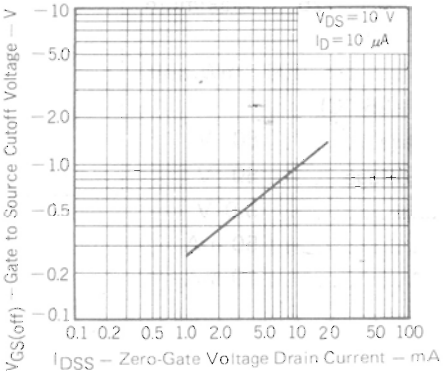
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



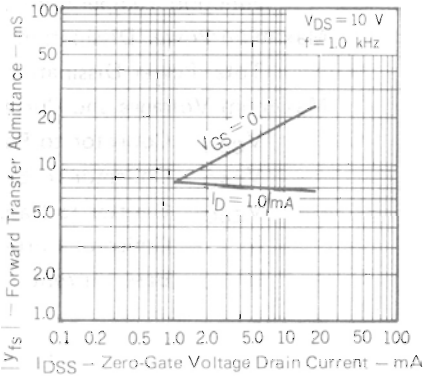
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



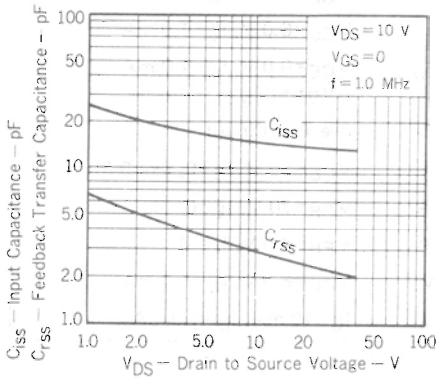
CORRELATION CURVE GATE TO SOURCE CUTOFF VOLTAGE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



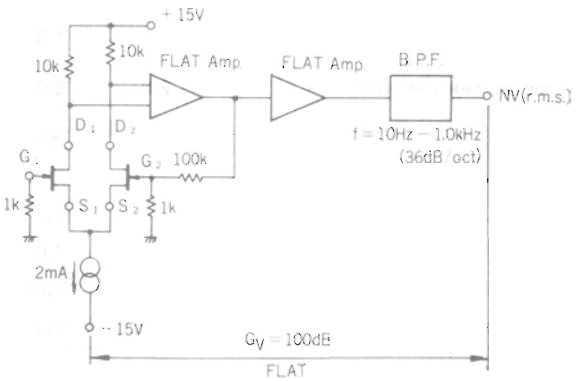
CORRELATION CURVE FORWARD TRANSFER ADMITTANCE vs. ZERO-GATE VOLTAGE DRAIN CURRENT



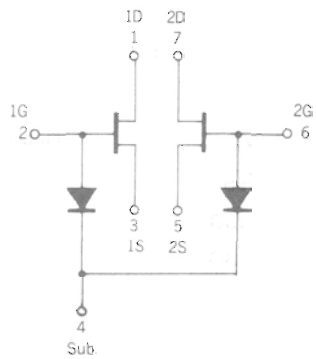
INPUT CAPACITANCE AND FEEDBACK TRANSFER CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



NOISE VOLTAGE TEST CIRCUIT



LEAD CONNECTION



NEC
ELECTRON DEVICE

NPN SILICON TWIN TRANSISTOR
μPA74HA

DESCRIPTION

The μPA74V is designed for use in the top stage for differential amplifier of an EQ amp. and a stereo main amp.

FEATURES

- Excellent pair balance — ΔV_{BE} : 5.0 mV MAX.
  @ V_{CE} = 6.0 V, I_C = 1.0 mA
- High h_{FE} — h_{FE} : 400 TYP.
  @ V_{CE} = 6.0 V, I_C = 1.0 mA
- High breakdown voltage — V_{CEO} : 80 V MIN.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

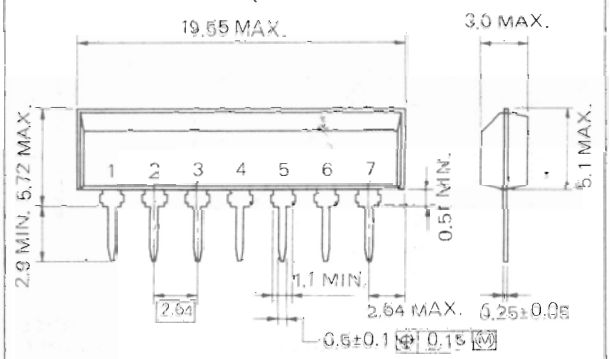
Total Power Dissipation . . . . . 300 mW/unit

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	80 V
V_{CEO}	Collector to Emitter Voltage	80 V
V_{EBO}	Emitter to Base Voltage	5.0 V
I_C	Collector Current	50 mA
I_B	Base Current	10 mA

PACKAGE DIMENSIONS

in millimeters



1. BASE 1
2. COLLECTOR 1
3. EMITTER 1
4. SUB
5. EMITTER 2
6. COLLECTOR 2
7. BASE 2

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	350			V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	DC Current Gain	200	400	800		V_{CE} = 6.0 V, I_C = 1.0 mA
$h_{FE(S)}/h_{FE(L)}$	DC Current Gain Ratio	0.9		1.0		V_{CE} = 6.0 V, I_C = 1.0 mA
ΔV_{BE}	Base to Emitter Voltage Difference		2.0	5.0	mV	V_{CE} = 6.0 V, I_C = 1.0 mA $\Delta V_{BE} = \lvert V_{BE1} - V_{BE2} \rvert$
NV	Noise Voltage			80	mV	See Test Circuit
C_{ob}	Output Capacitance		2.5		pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB} = 70 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB} = 4.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.55		0.65	V	V_{CE} = 6.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage			0.3	V	I_C = 10 mA, I_B = 1.0 mA

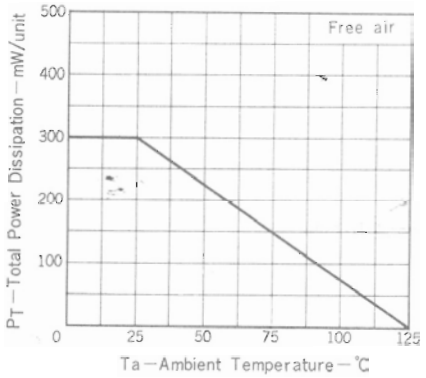
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

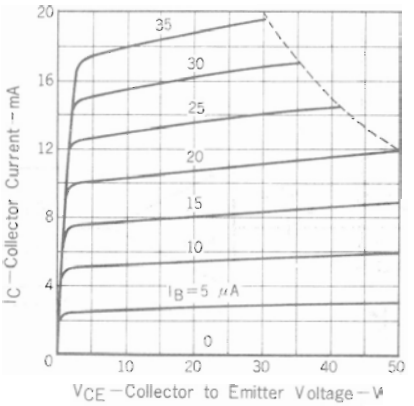
Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

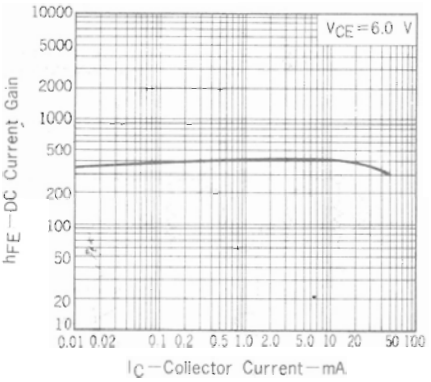
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



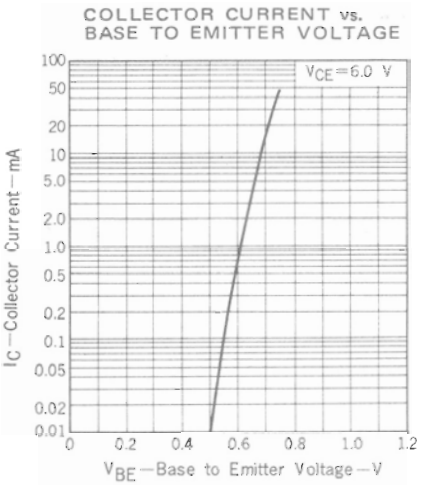
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



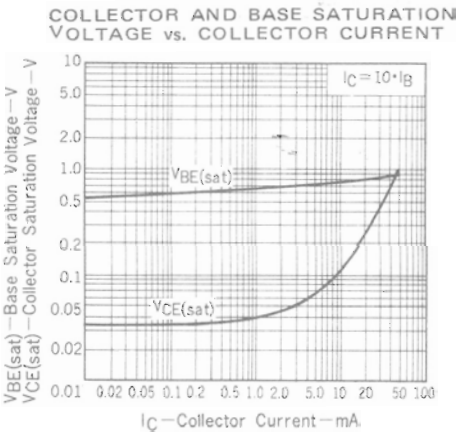
DC CURRENT GAIN vs. COLLECTOR CURRENT



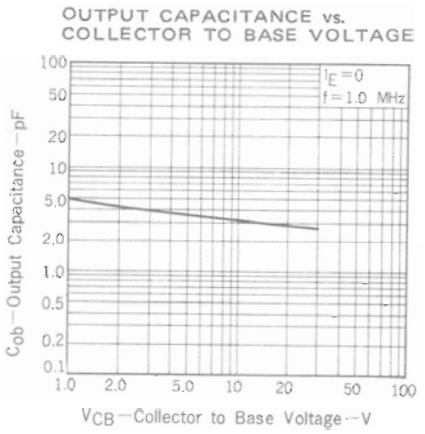
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



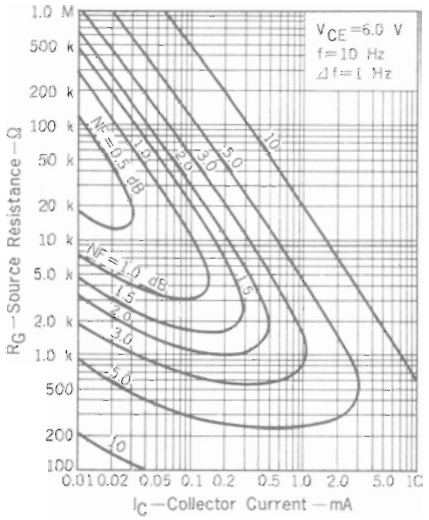
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



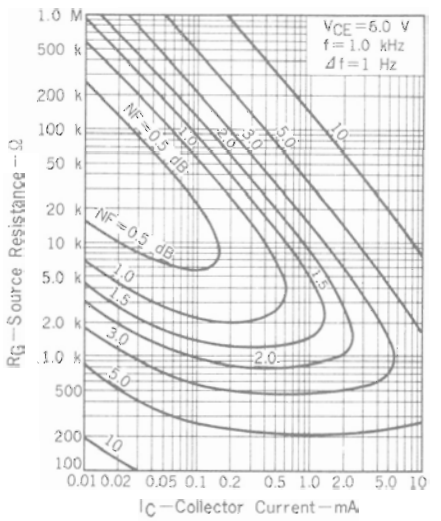
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



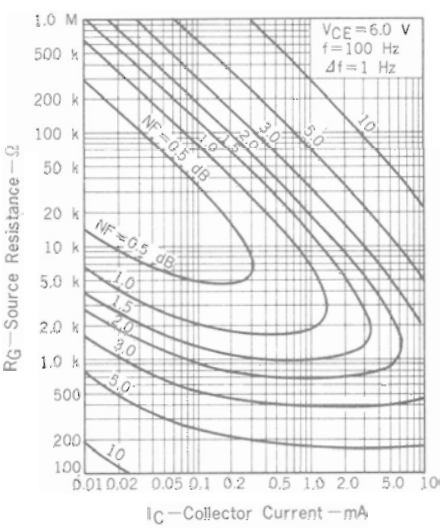
NF MAP 1



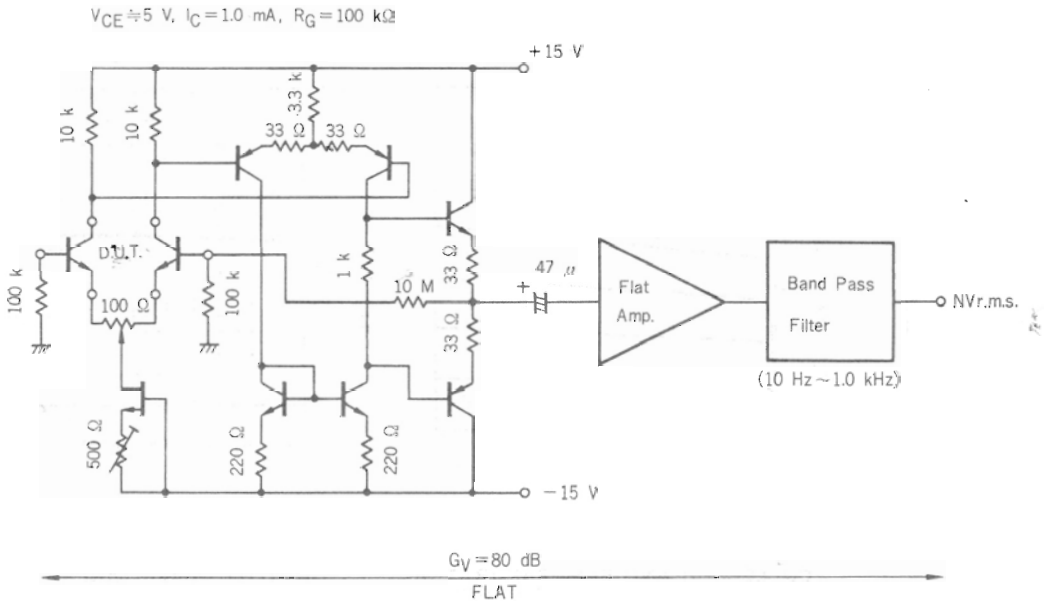
NF MAP 2



NF MAP 3



NV TEST CIRCUIT



NEC
ELECTRON DEVICE

PNP SILICON TWIN TRANSISTOR
μPA75HA

DESCRIPTION

The μPA75V is designed for use in the top stage for differential amplifier of an EQ amp. and a stereo main amp.

FEATURES

- Excellent pair balance — ΔV_{BE} : 5.0 mV MAX.
  @ V_{CE} = −6.0 V, I_C = −1.0 mA
- High h_{FE} — h_{FE} : 400 TYP.
  @ V_{CE} = −6.0 V, I_C = −1.0 mA
- High Breakdown Voltage — V_{CEO} : −80 V MIN.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +125 °C

Junction Temperature . . . . . 125 °C Maximum

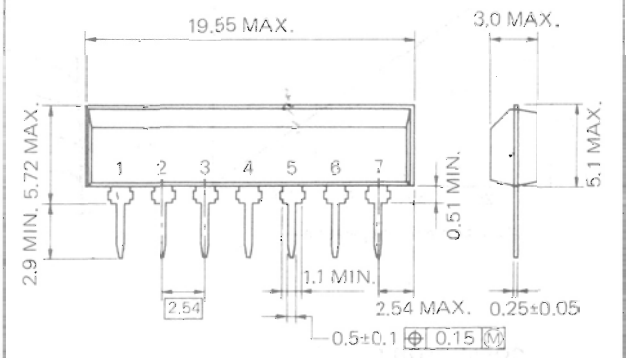
Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 300 mW/unit

Maximum Voltage and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	−80	V
V_{CEO}	Collector to Emitter Voltage . . .	−80	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
I_C	Collector Current	−50	mA
I_B	Base Current	−10	mA

PACKAGE DIMENSIONS
in millimeters



1. BASE 1
2. COLLECTOR 1
3. EMITTER 1
4. SUB
5. EMITTER 2
6. COLLECTOR 2
7. BASE 2

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	350			V_{CE}=−6.0 V, I_C=−0.1 mA
h_{FE2}	DC Current Gain	200	400	800		V_{CE}=−6.0 V, I_C=−0.1 mA
$h_{FE(S)}/h_{FE(L)}$	DC Current Gain Ratio	0.9		1.0		V_{CE}=−6.0 V, I_C=−1.0 mA
ΔV_{BE}	Base to Emitter Voltage Difference		2.0	5.0	mV	V_{CE}=−6.0 V, I_C=−1.0 mA ΔV_{BE}=|V_{BE1}−V_{BE2}|
NV	Noise Voltage			80	mV	See Test Circuit
C_{ob}	Output Capacitance		4.0		pF	V_{CB}=−30 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB}=−70 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB}=−4.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55		−0.65	V	V_{CE}=−6.0 V, I_C=−1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage			−0.3	V	I_C=−10 mA, I_B=−1.0 mA

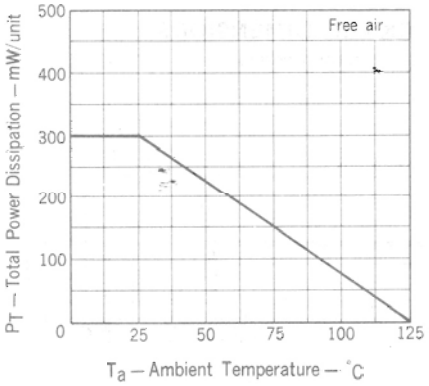
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

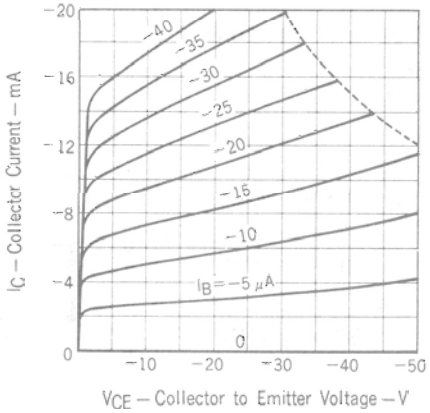
Test Conditions: V_{CE}=−6.0 V, I_C=−1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

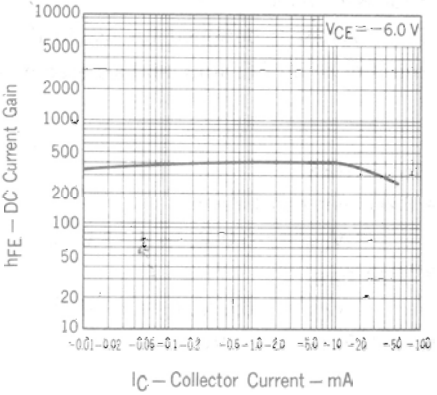
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



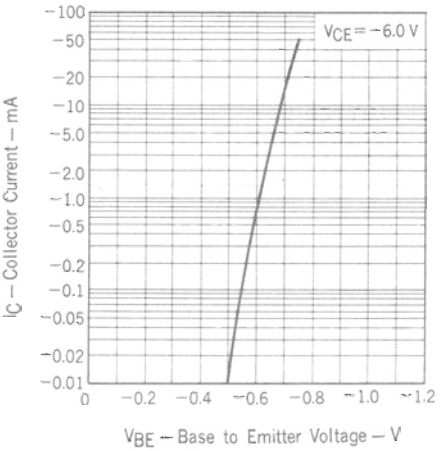
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



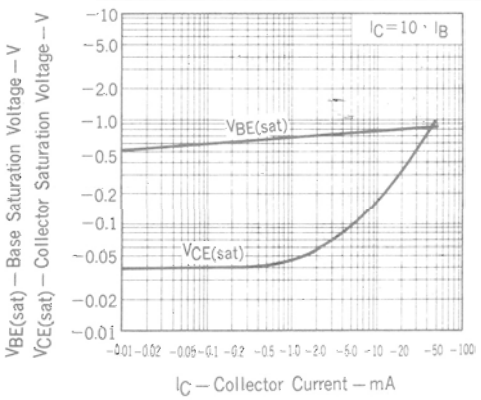
DC CURRENT GAIN vs. COLLECTOR CURRENT



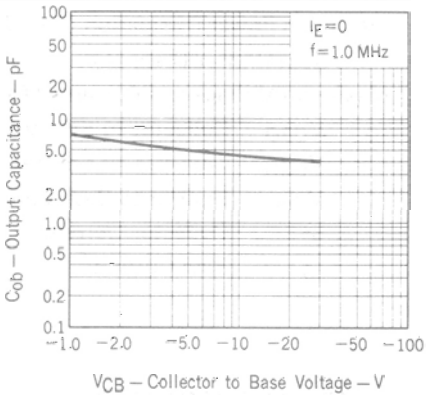
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



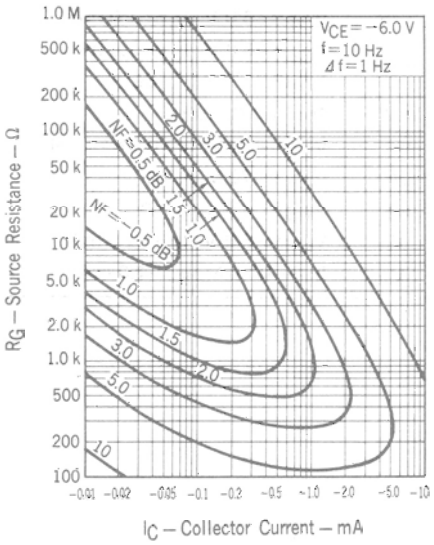
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



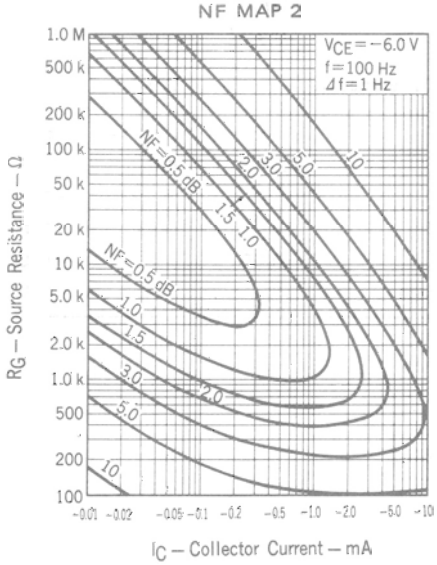
OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



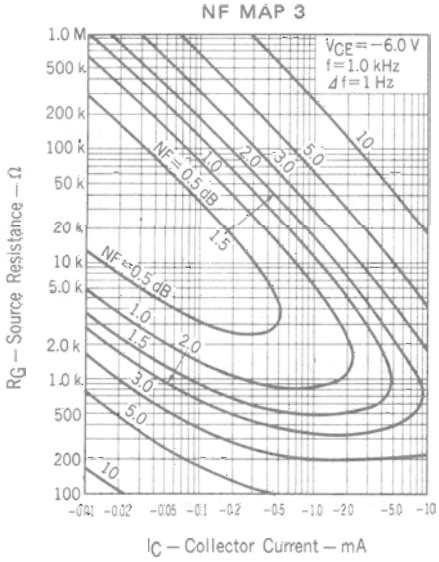
NF MAP 1



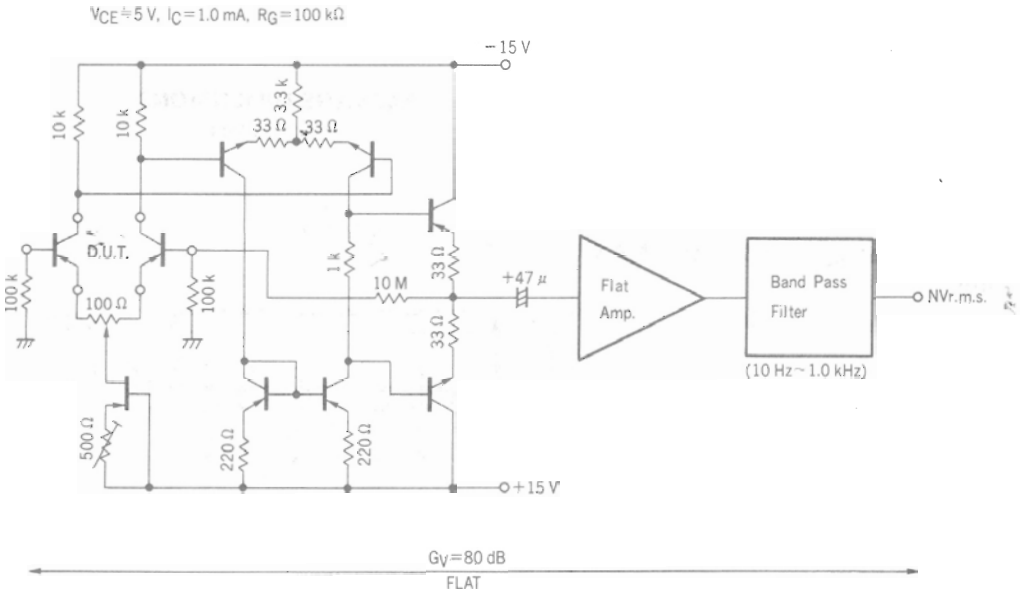
NF MAP 2



NF MAP 3



NV TEST CIRCUIT



NEC
ELECTRON DEVICE

NPN SILICON TWIN TRANSISTOR
μPA76HA

DESCRIPTION

The μPA76V is designed for use in the top stage for differential amplifier of an EQ amp. and a stereo main amp..

FEATURES

- Excellent pair balance — ΔV_{BE} : 5.0 mV MAX.
  @ V_{CE} = 6.0 V, I_C = 1.0 mA
- High h_{FE} — h_{FE} : 400 TYP.
  @ V_{CE} = 6.0 V, I_C = 1.0 mA

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

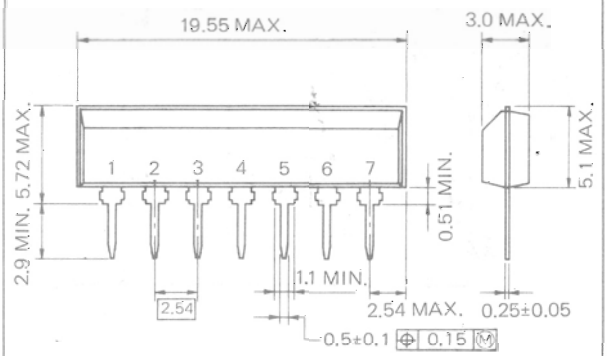
Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 300 mW/unit

Maximum Voltage and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	60	V
V_{EBO}	Emitter to Base Voltage	5.0	V
I_C	Collector Current	50	mA
I_B	Base Current	10	mA

PACKAGE DIMENSIONS
in millimeters



1. BASE 1
2. COLLECTOR 1
3. EMITTER 1
4. SUB
5. EMITTER 2
6. COLLECTOR 2
7. BASE 2

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	350			V_{CE}=6.0 V, I_C=0.1 mA
h_{FE2}	DC Current Gain	200	400	800		V_{CE}=6.0 V, I_C=1.0 mA
$h_{FE(S)}/h_{FE(L)}$	DC Current Gain Ratio	0.9		1.0		V_{CE}=6.0 V, I_C=1.0 mA
ΔV_{BE}	Base to Emitter Voltage Difference		2.0	5.0	mV	V_{CE}=6.0 V, I_C=1.0 mA $\Delta V_{BE} = \lvert V_{BE1} - V_{BE2} \rvert$
NV	Noise Voltage			160	mV	See Test Circuit
C_{ob}	Output Capacitance		2.5		pF	V_{CB}=30 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			1.0	μA	V_{CB}=50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			1.0	μA	V_{EB}=4.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	0.55		0.65	V	V_{CE}=6.0 V, I_C=1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage			0.3	V	I_C=10 mA, I_B=1.0 mA

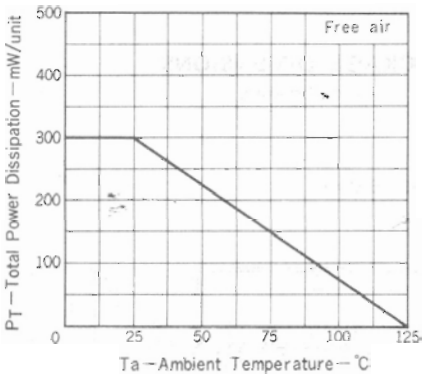
Classification of h_{FE2}

Rank	P	F	E
Range	200 — 400	300 — 600	400 — 800

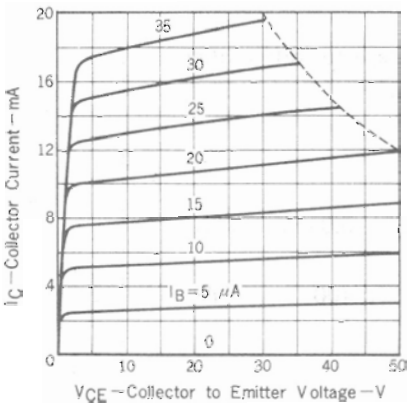
Test Conditions : V_{CE} = 6.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

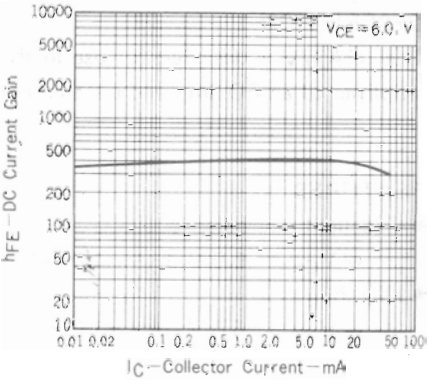
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



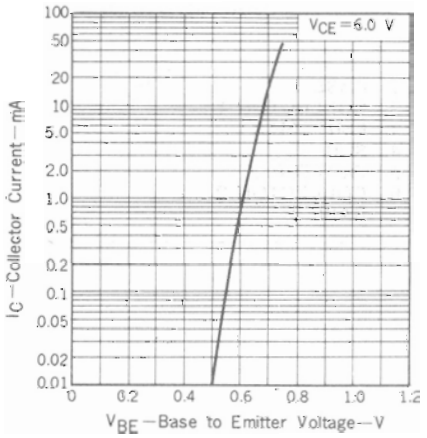
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



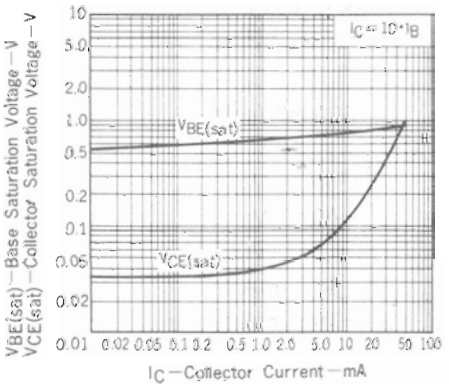
DC CURRENT GAIN vs. COLLECTOR CURRENT



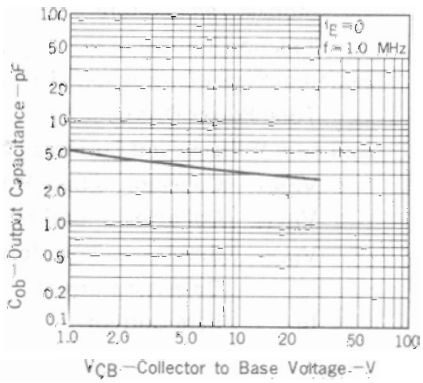
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT

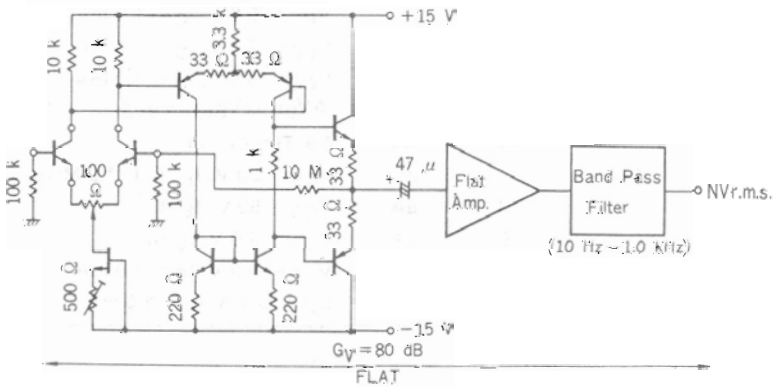


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NV TEST CIRCUIT

V_{CE} ≒ 5 V, I_C = 1.0 mA, R_G = 100 kΩ



NEC
ELECTRON DEVICE

PNP SILICON TWIN TRANSISTOR
μPA77HA

DESCRIPTION

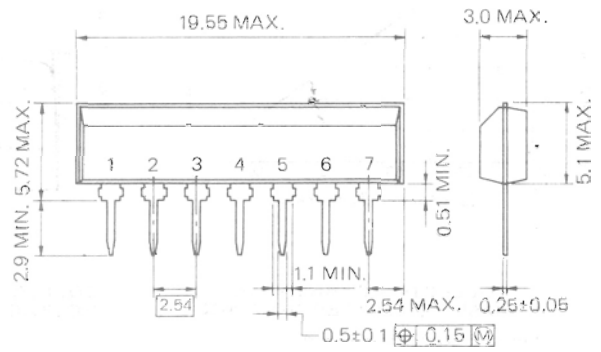
The μPA77V is designed for use in the top stage for differential amplifier of an EQ amp and a stereo main amp.

FEATURES

- Excellent pair balance — ΔV_{BE} : 5.0 mV MAX.
  @ V_{CE} = −6.0 V, I_C = −1.0 mA
- High h_{FE} — h_{FE} : 400 TYP.
  @ V_{CE} = −6.0 V, I_C = −1.0 mA

PACKAGE DIMENSIONS

in millimeters



1. BASE 1
2. COLLECTOR 1
3. EMITTER 1
4. SUB
5. EMITTER 2
6. COLLECTOR 2
7. BASE 2

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +125 °C
- Junction Temperature . . . . . 125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 300 mW/unit

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	−60	V
V_{CEO}	Collector to Emitter Voltage . . .	−60	V
V_{EBD}	Emitter to Base Voltage	−5.0	V
I_C	Collector Current	−50	mA
I_B	Base Current	−10	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	150	350			V_{CE}=−6.0 V, I_C=−0.1 mA
h_{FE2}	DC Current Gain	200	400	800		V_{CE}=−6.0 V, I_C=−1.0 mA
$h_{FE(S)}/h_{FE(L)}$	DC Current Gain Ratio	0.9		1.0		V_{CE}=−6.0 V, I_C=−1.0 mA
ΔV_{BE}	Base to Emitter Voltage Difference		2.0	5.0	mV	V_{CE}=−6.0 V, I_C=−1.0 mA $\Delta V_{BE} = \lvert V_{BE1} - V_{BE2} \rvert$
NV	Noise Voltage			160	mV	See Test Circuit
C_{ob}	Output Capacitance		4.0		pF	V_{CB}=−30 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−1.0	μA	V_{CB}=−50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−1.0	μA	V_{EB}=−4.0 V, I_C=0
V_{BE}	Base to Emitter Voltage	−0.55		−0.65	V	V_{CE}=−6.0 V, I_C=−1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage			−0.3	V	I_C=−10 mA, I_B=−1.0 mA

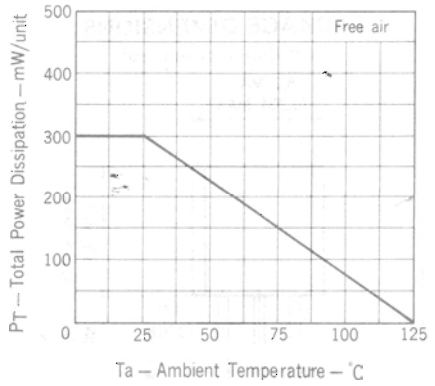
Classification of h_{FE2}

Rank	P	F	E
Range	200 – 400	300 – 600	400 – 800

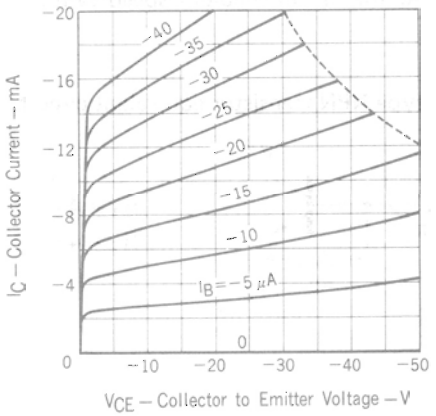
Test Conditions: V_{CE}=−6.0 V, I_C=−1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

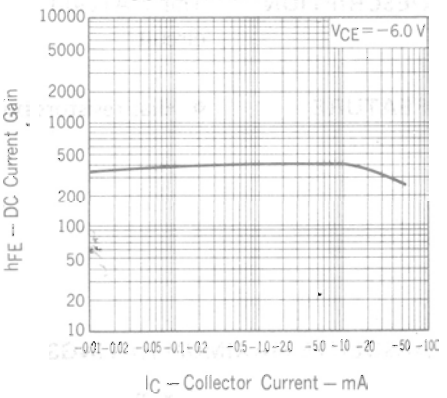
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



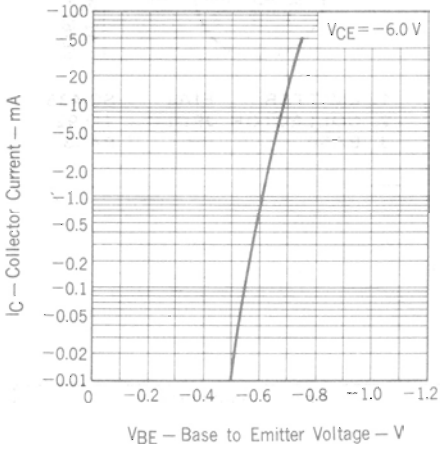
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



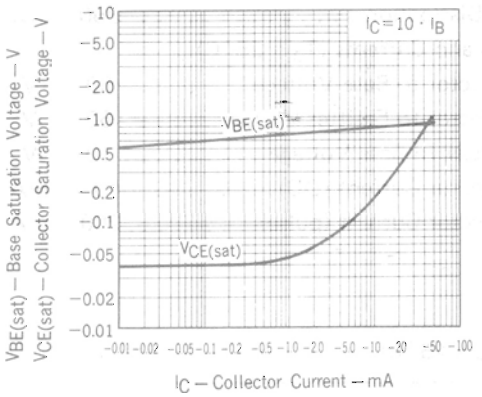
DC CURRENT GAIN vs. COLLECTOR CURRENT



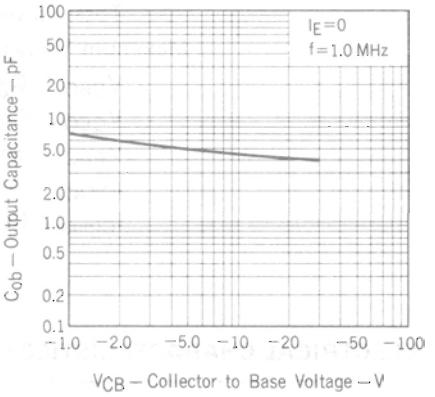
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



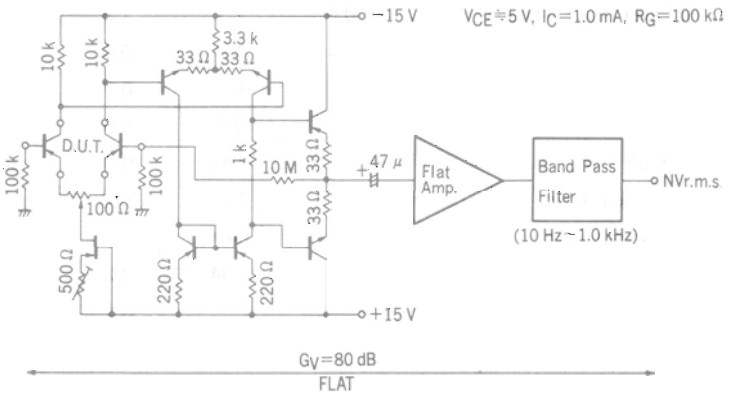
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NV TEST CIRCUIT



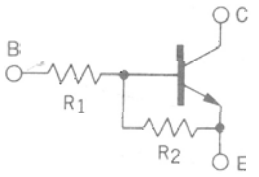
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1L4M

DESCRIPTION The AA1L4M is designed for use in medium speed switching circuit.

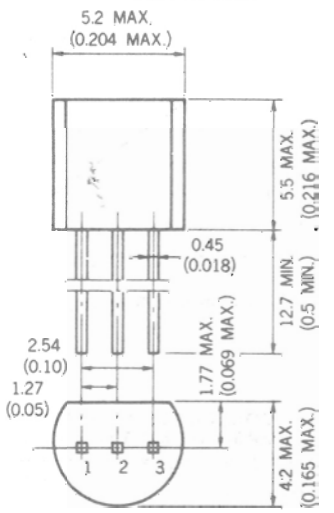
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

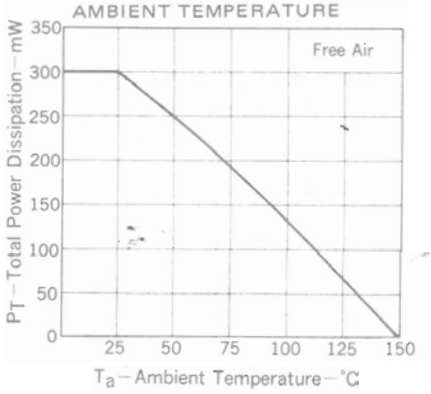
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	10	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

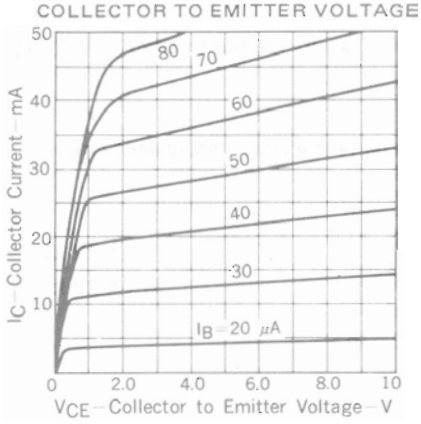
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.7	5.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time		0.27	0.7	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		2.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time		2.48	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	240	340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	95	640		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

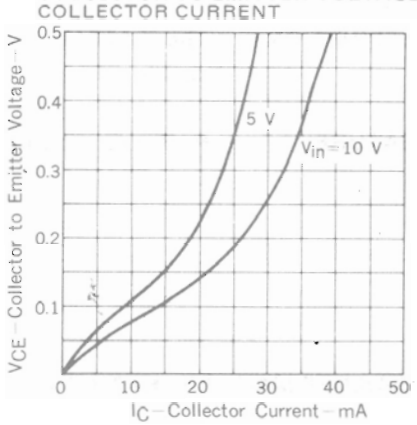
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



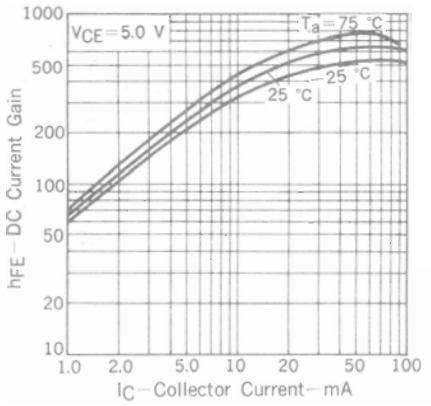
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



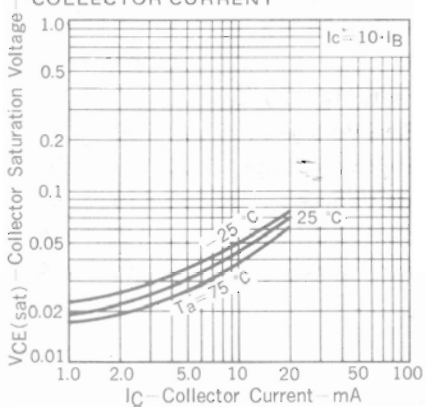
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



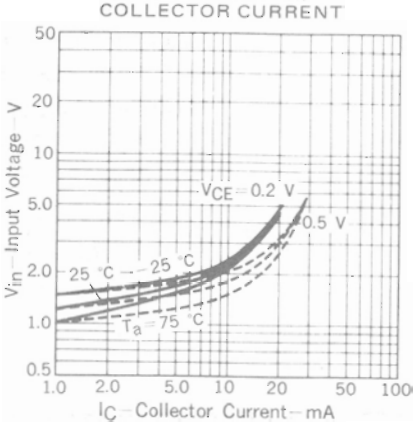
DC CURRENT GAIN vs. COLLECTOR CURRENT



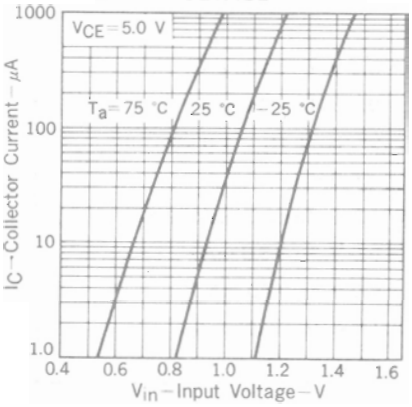
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



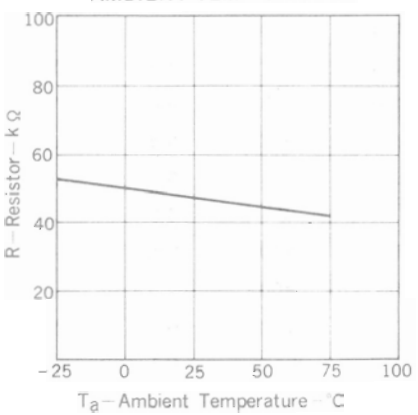
INPUT VOLTAGE vs. COLLECTOR CURRENT



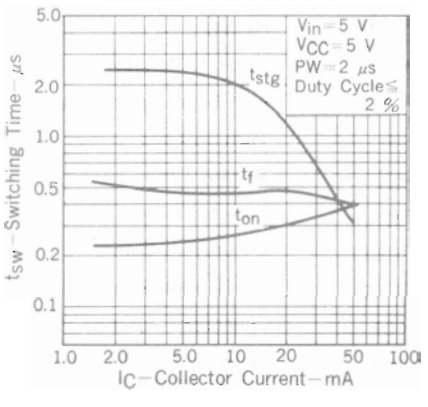
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



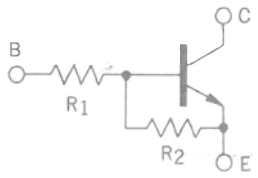
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1F4M

DESCRIPTION The AA1F4M is designed for use in medium speed switching circuit.

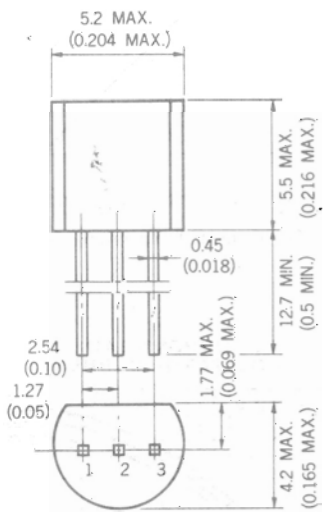
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 300 mW

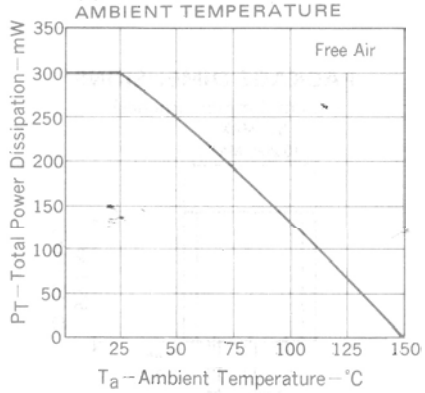
Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

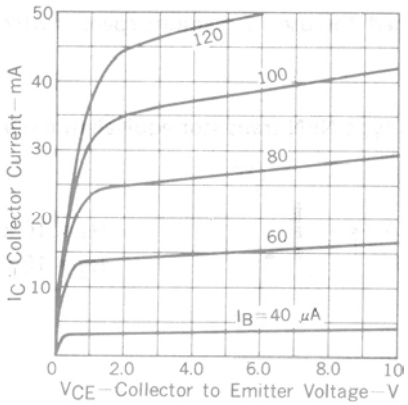
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.6	4.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time		0.11	0.4	μs	V_{CC} = 5.0 V R_L = 1.0 kΩ
t_{stg}	Storage Time		2.3	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time		2.6	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	120	195	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	90	400		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

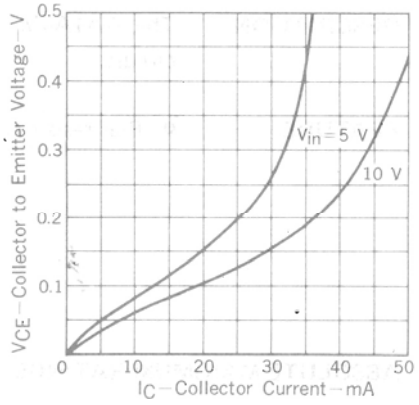
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



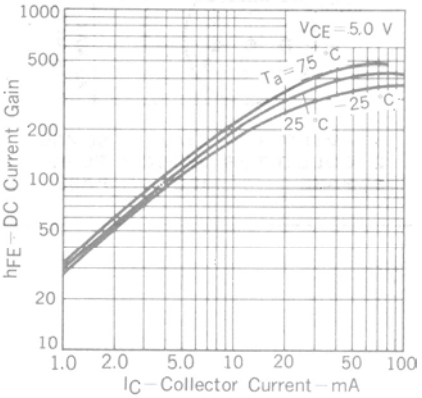
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



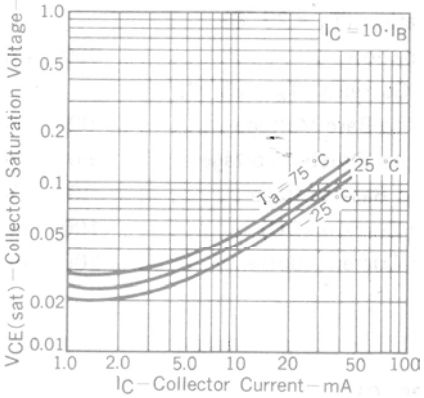
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



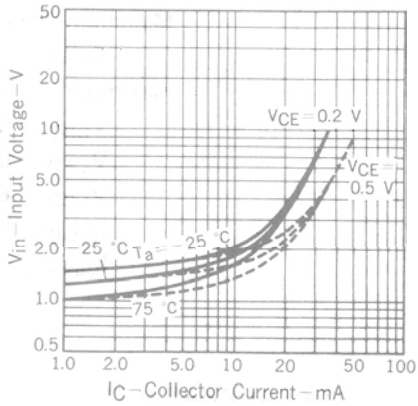
DC CURRENT GAIN vs. COLLECTOR CURRENT



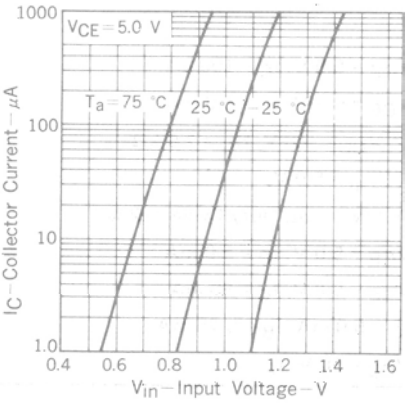
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



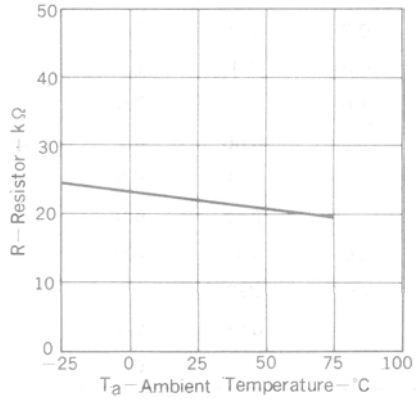
INPUT VOLTAGE vs. COLLECTOR CURRENT



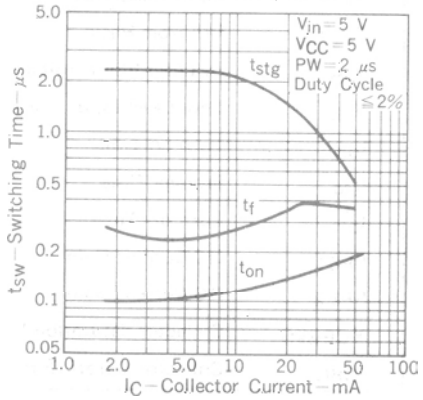
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs COLLECTOR CURRENT



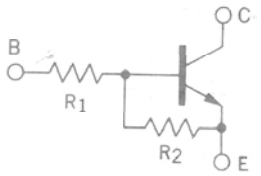
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1A4M

DESCRIPTION The AA1A4M is designed for use in medium speed switching circuit.

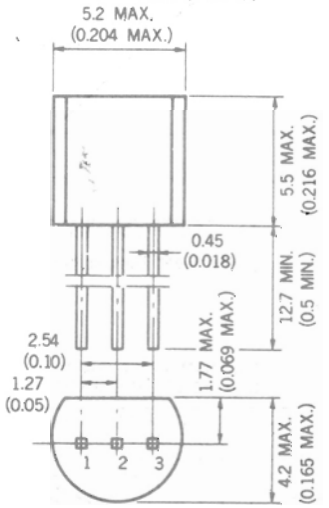
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 10 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

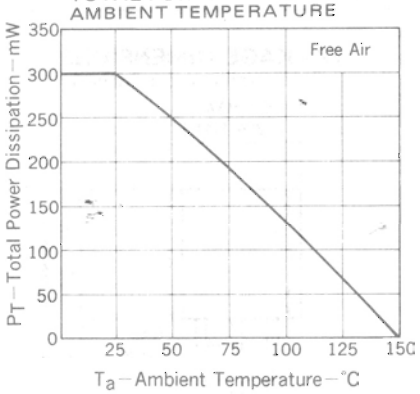
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	10	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

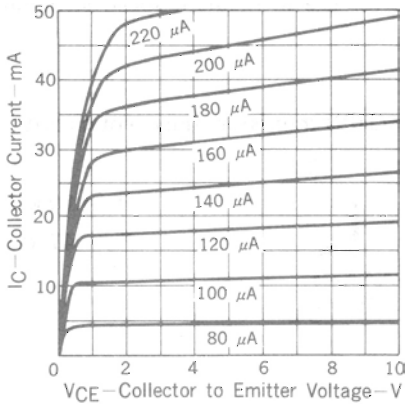
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.4	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time		0.06	0.2	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		2.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time		2.15	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	35	62	100	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	80	230		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.05	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

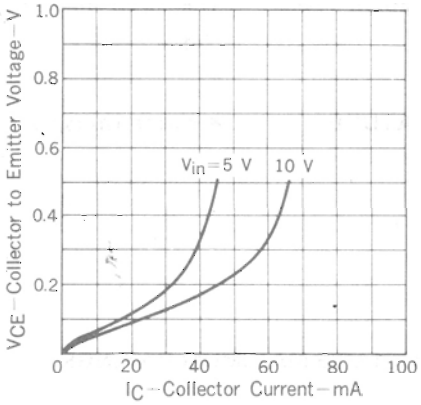
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



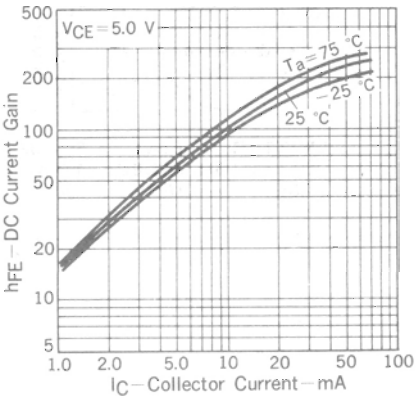
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



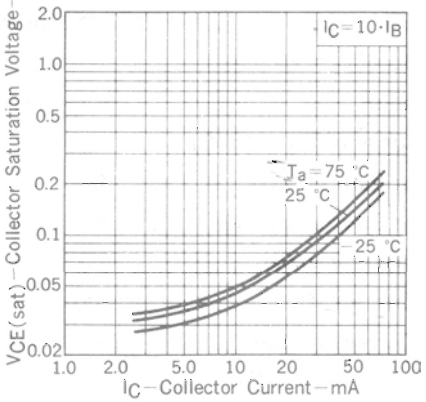
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



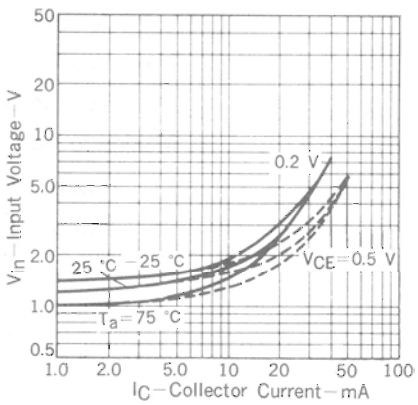
DC CURRENT GAIN vs. COLLECTOR CURRENT



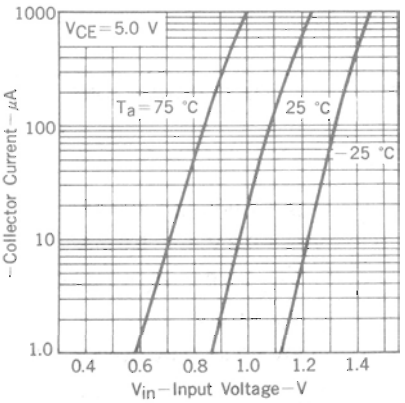
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



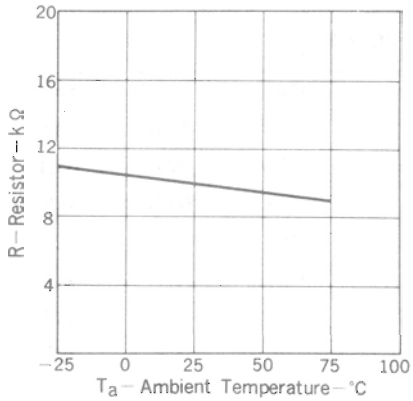
INPUT VOLTAGE vs. COLLECTOR CURRENT



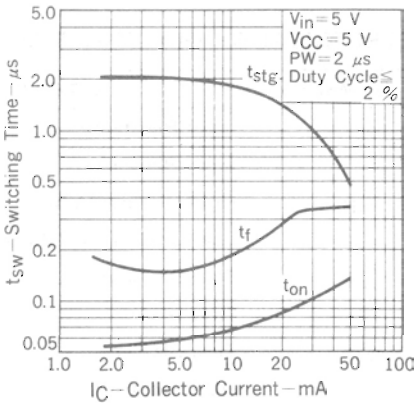
INPUT VOLTAGE vs. COLLECTOR CURRENT



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



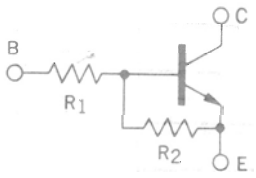
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1A4P

DESCRIPTION The AA1A4P is designed for use in medium speed switching circuit.

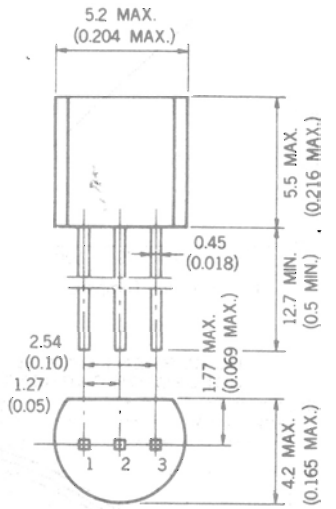
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

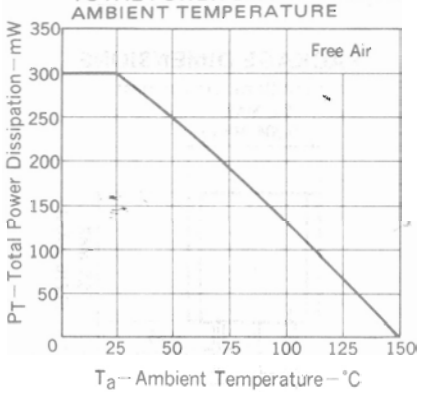
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 5.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

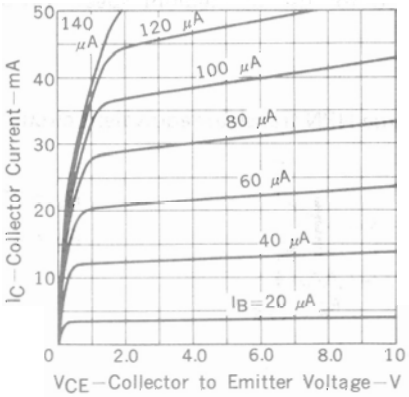
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	0.5	0.65	0.9	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	0.6	0.89	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.1	0.2	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		3.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		3.2	6.0	μs	PW = 2 μs, Duty Cycle ≤ 2 %
h_{FE1}	DC Current Gain	85	210	340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	95	370		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

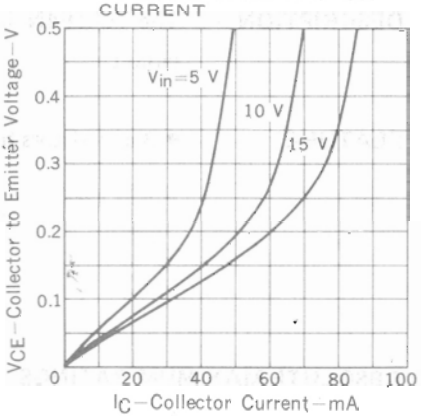
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



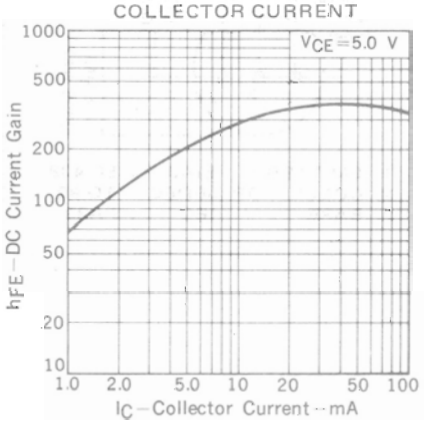
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



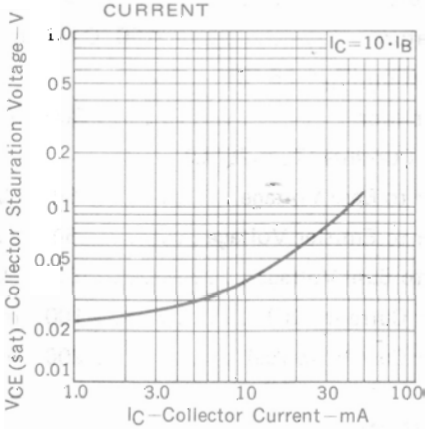
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



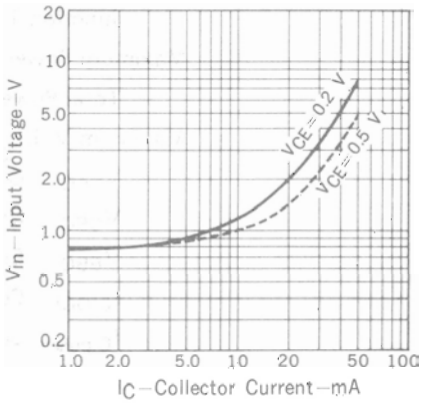
DC CURRENT GAIN vs. COLLECTOR CURRENT



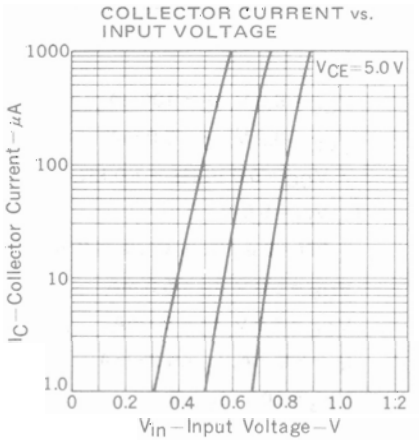
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



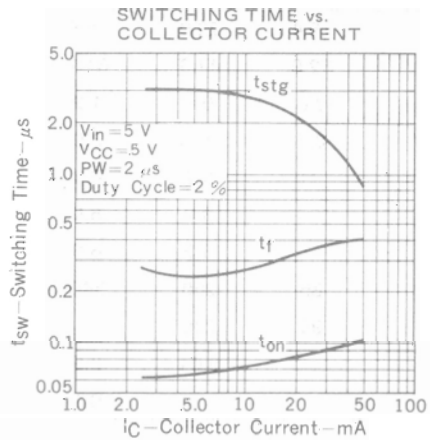
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



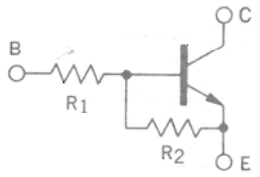
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1F4N

DESCRIPTION The AA1F4N is designed for use in medium speed switching circuit.

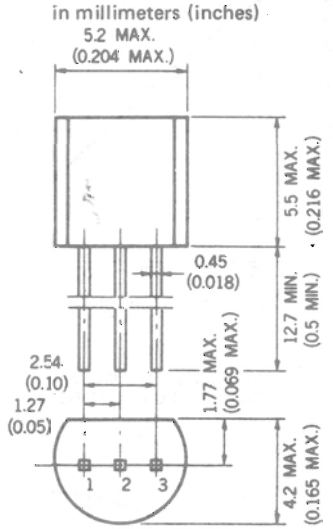
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

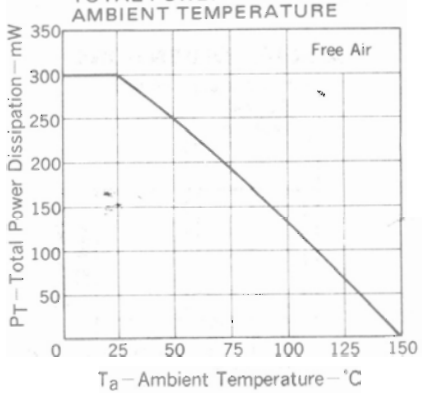
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

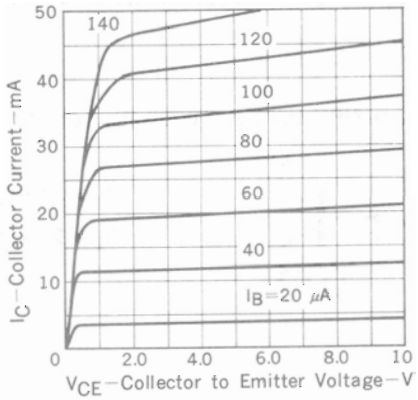
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	0.6	0.8	1.2	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	0.7	1.3	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.2	0.3	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		3.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		3.5	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	200	340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	95	230		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

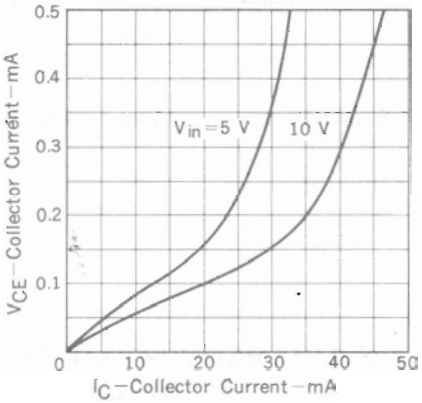
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



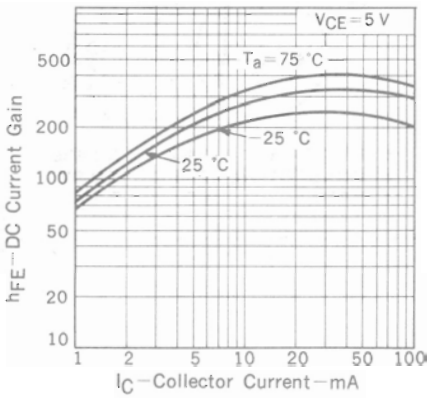
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



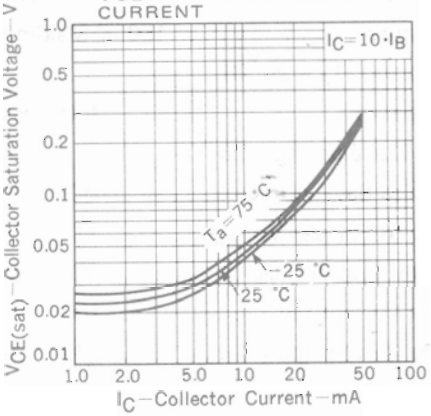
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



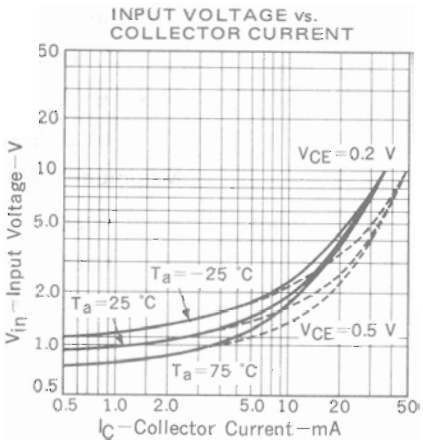
DC CURRENT GAIN vs. COLLECTOR CURRENT



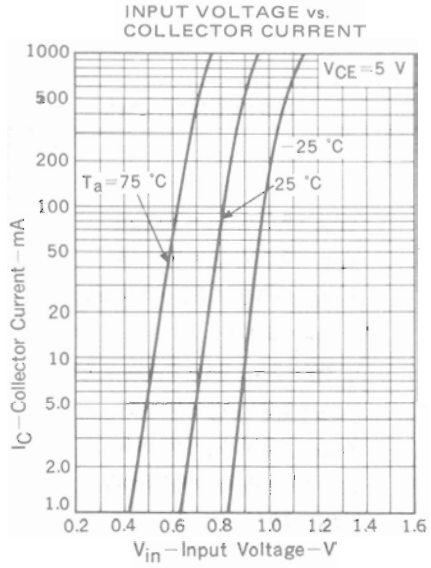
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



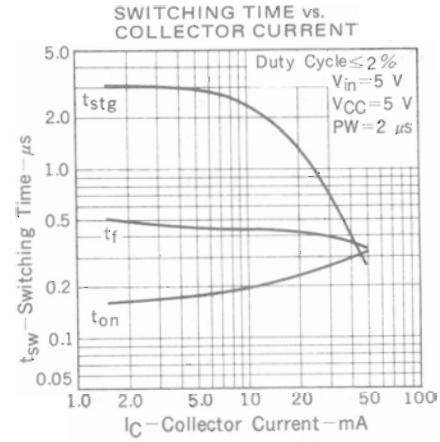
INPUT VOLTAGE vs. COLLECTOR CURRENT



INPUT VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME vs. COLLECTOR CURRENT



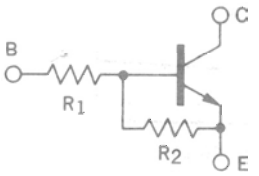
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1L4L

DESCRIPTION The AA1L4L is designed for use in medium speed switching circuit.

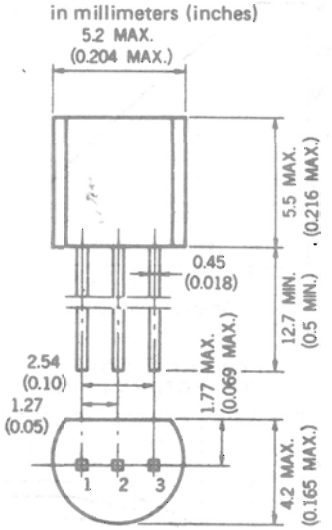
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

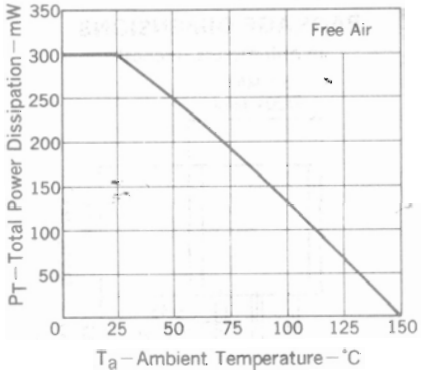
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 15 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

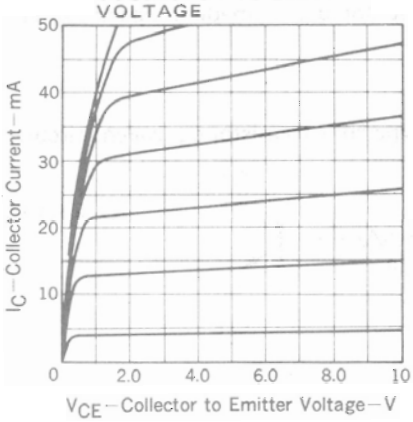
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_2	Input Resistance	15.4	22.0	28.6	kΩ	
V_{IH}	Hi Level Input Voltage	0.9	1.7	3.0	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.5	2.5	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.38	1.0	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.2	3.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		1.6	5.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	120	195	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	90	340		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

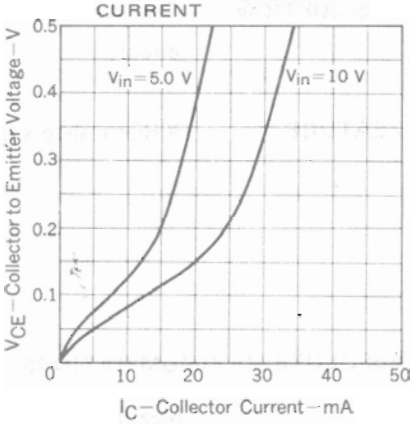
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



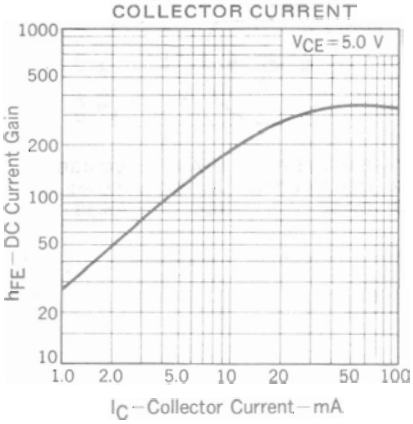
COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE



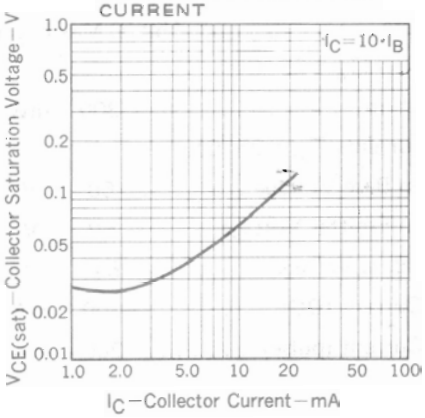
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



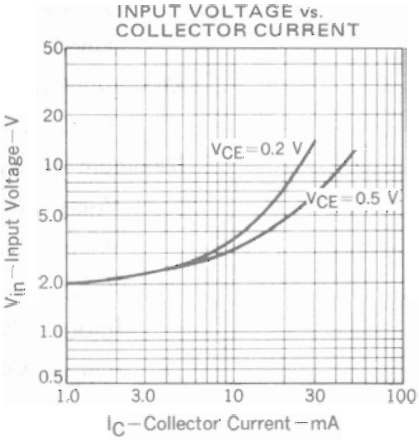
DC CURRENT GAIN vs. COLLECTOR CURRENT



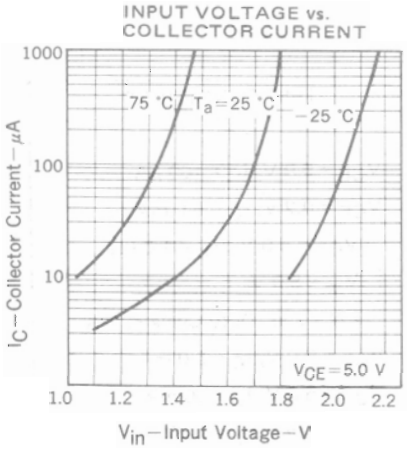
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



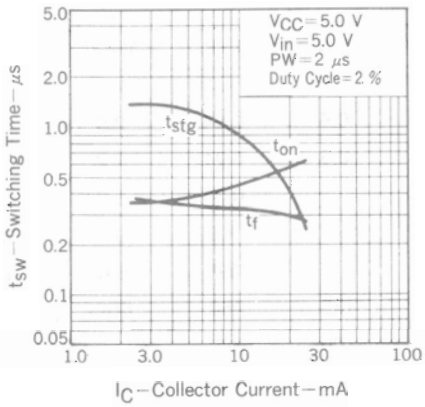
INPUT VOLTAGE vs. COLLECTOR CURRENT



INPUT VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME vs. COLLECTOR CURRENT



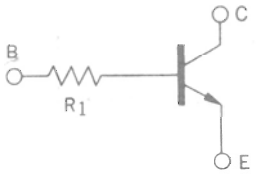
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
AA1L3Z

DESCRIPTION The AA1L3Z is designed for use in medium speed switching circuit.

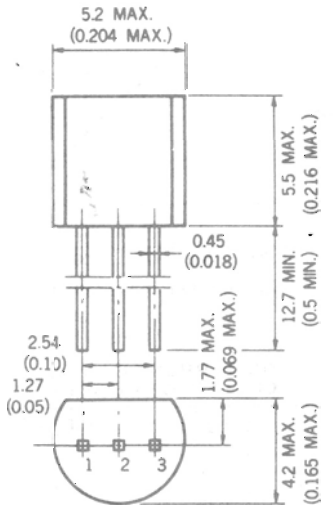
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 4.7 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

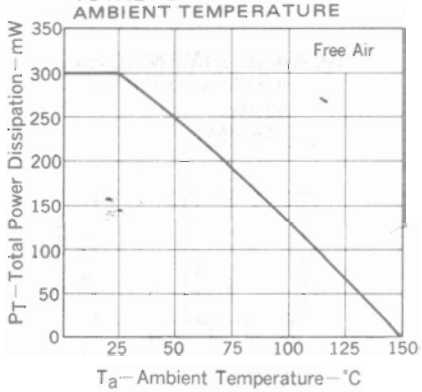
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

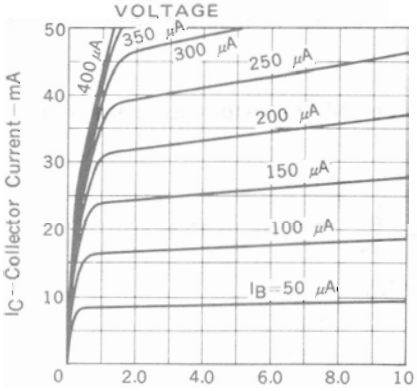
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	3.29	4.7	6.11	kΩ	
V_{IH}	Hi Level Input Voltage	0.5	0.54	0.6	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	0.5	0.71	1.2	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.03	0.2	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		3.2	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		3.4	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	135	450	600	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	100	380		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

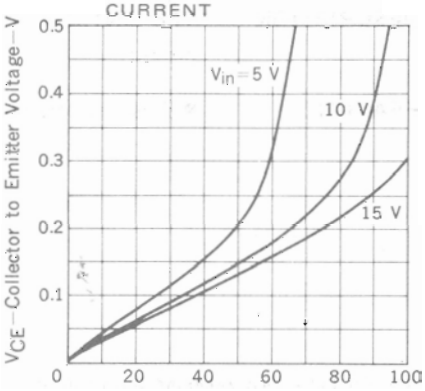
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



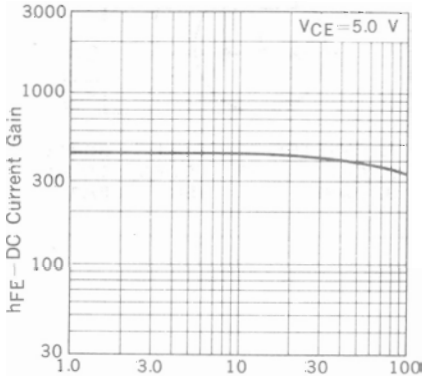
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



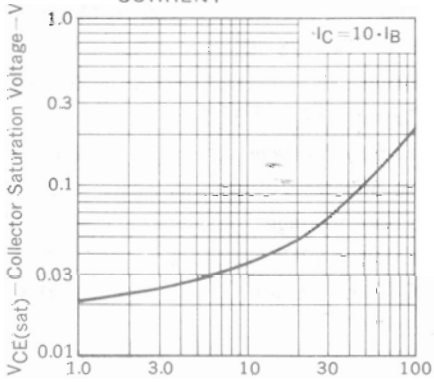
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



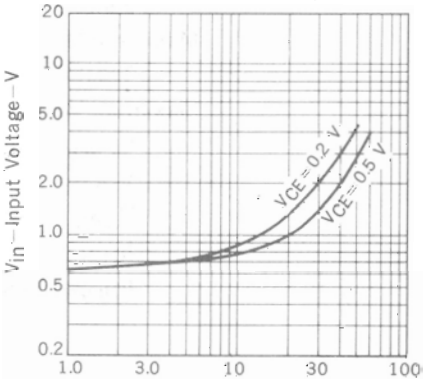
DC CURRENT GAIN vs. COLLECTOR CURRENT



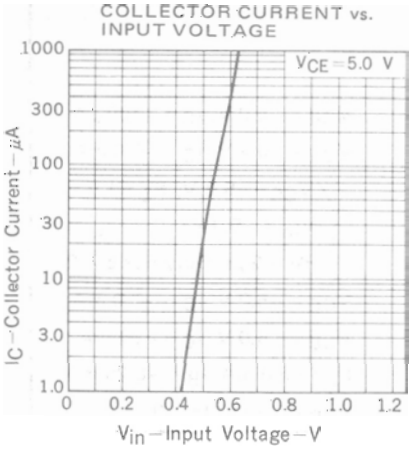
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



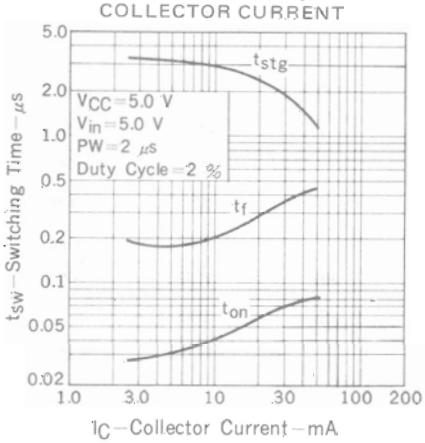
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



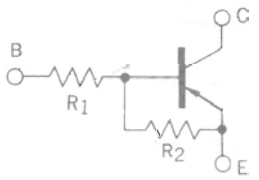
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1L4M

DESCRIPTION The AN1L4M is designed for use in medium speed switching circuit.

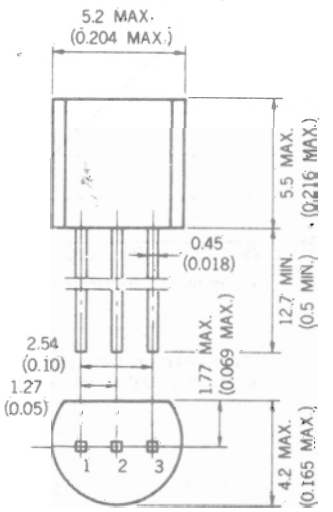
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

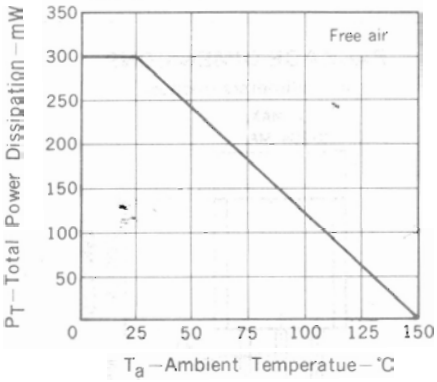
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

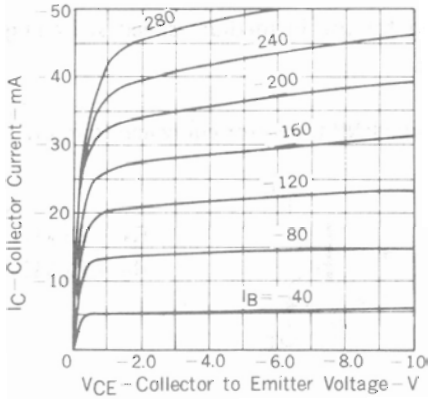
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	−0.8	−1.17	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−2.4	−5.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time		0.5	1.0	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		0.8	3.0	μs	V_{in} = −5.0 V
t_{off}	Turn off Time		1.4	4.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	135	340	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	95	180		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.05	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

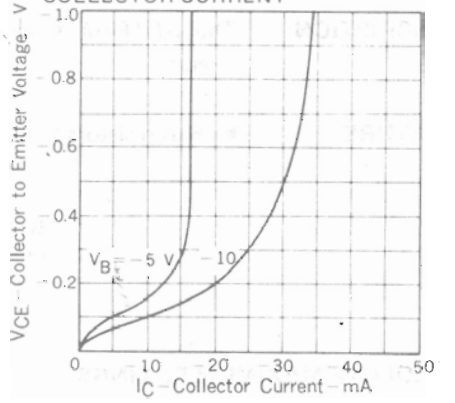
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



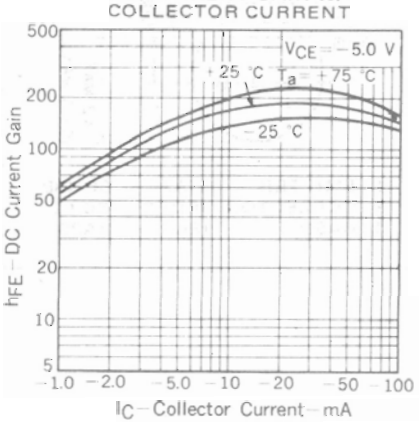
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



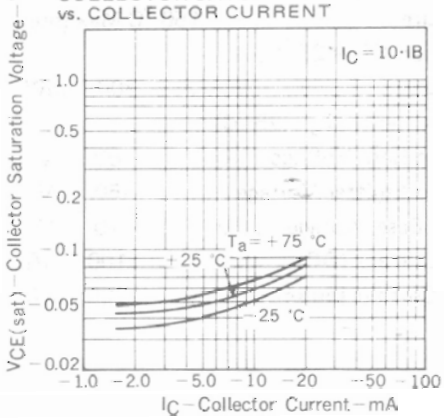
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



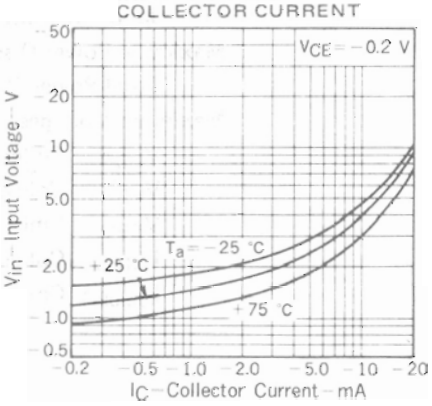
DC CURRENT GAIN vs. COLLECTOR CURRENT



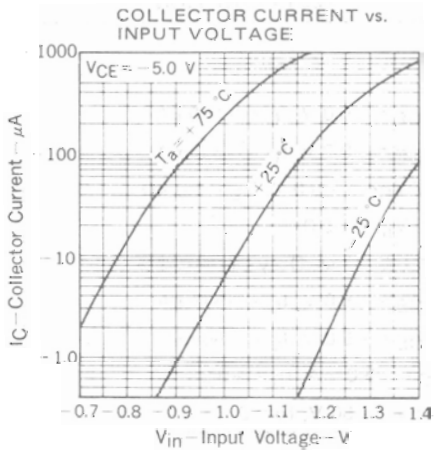
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



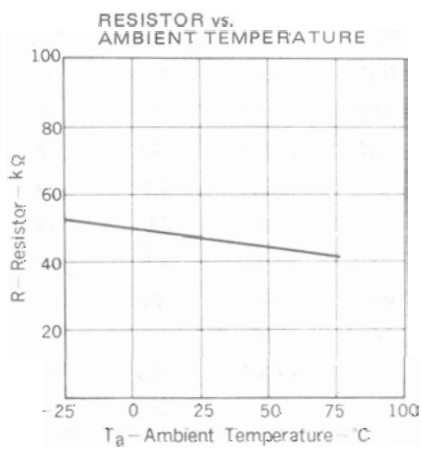
INPUT VOLTAGE vs. COLLECTOR CURRENT



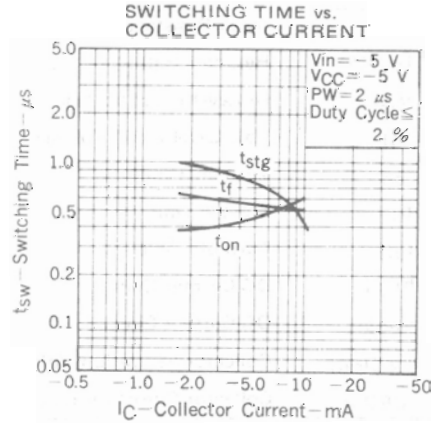
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



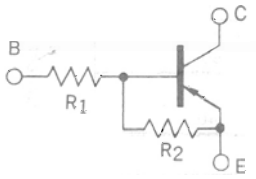
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1F4M

DESCRIPTION The AN1F4M is designed for use in medium speed switching circuit.

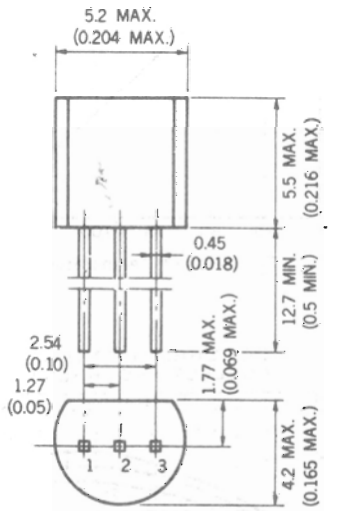
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 300 mW

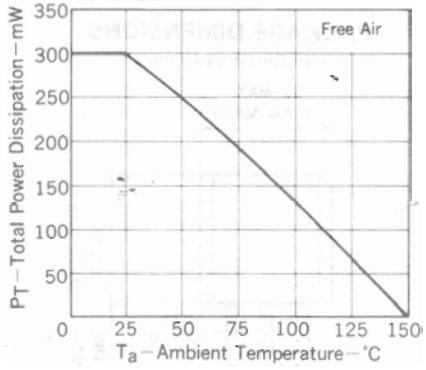
Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

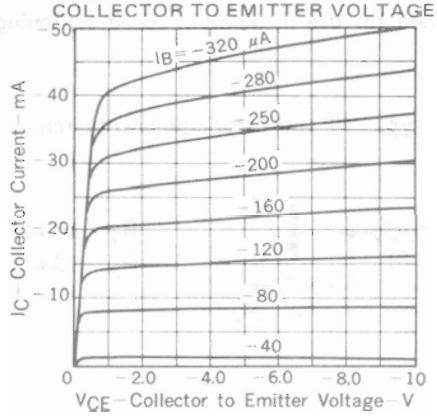
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	−0.8	−1.17	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−2.0	−4.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time		0.23	0.5	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		0.8	3.0	μs	V_{in} = −5.0 V
t_{off}	Turn off Time		1.1	3.5	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	85	195	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	90	145		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.05	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

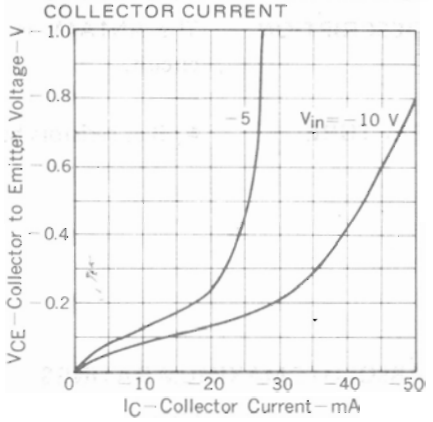
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



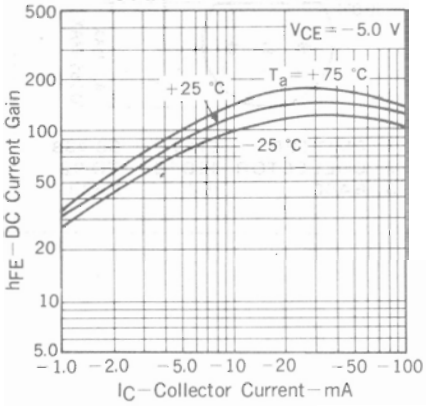
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



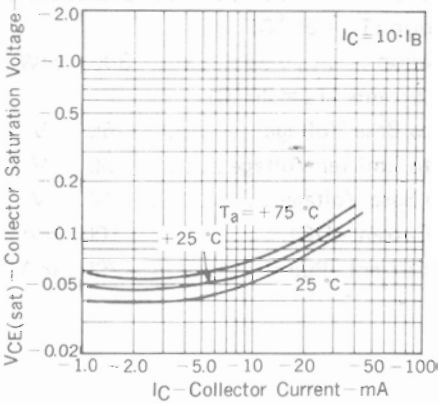
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



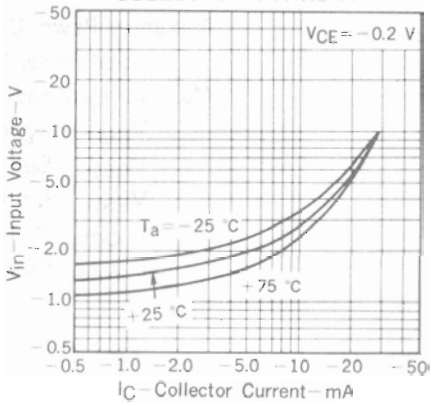
DC CURRENT GAIN vs. COLLECTOR CURRENT



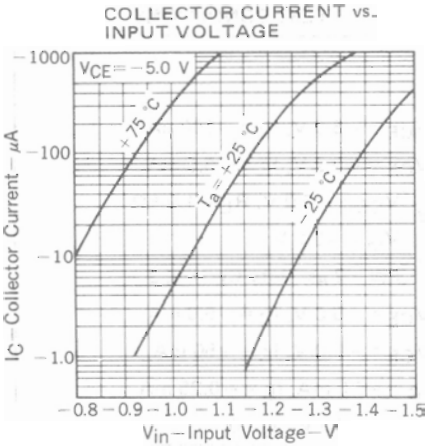
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



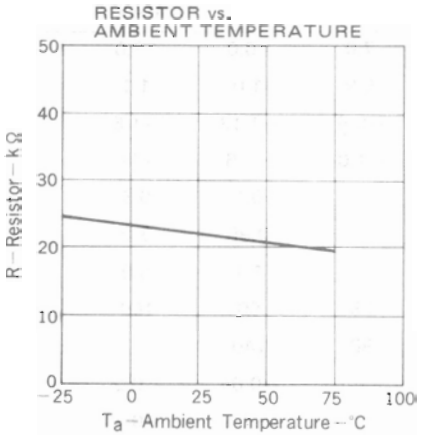
INPUT VOLTAGE vs. COLLECTOR CURRENT



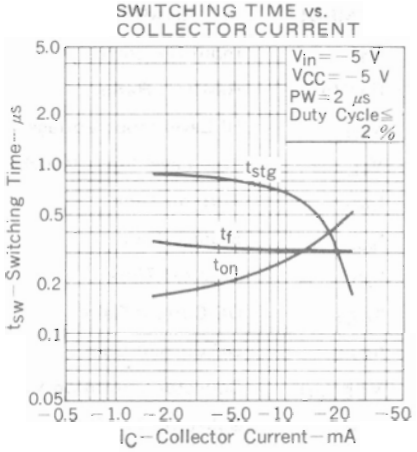
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



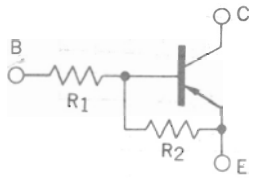
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1A4M

DESCRIPTION The AN1A4M is designed for use in medium speed switching circuit.

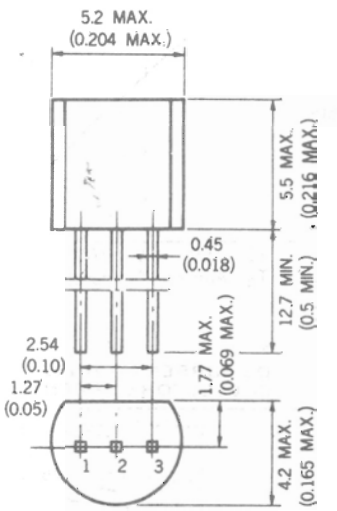
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 10 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

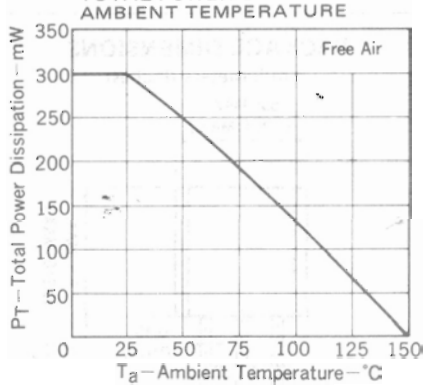
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (Pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

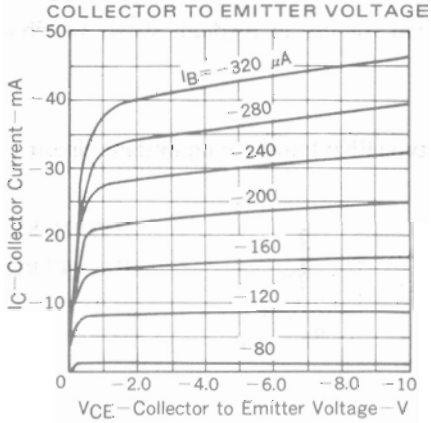
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	−0.8	−1.13	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−1.6	−3.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time		0.1	0.5	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		0.95	3.0	μs	V_{in} = −5.0 V
t_{off}	Turn off Time		1.1	5.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	35	50	100	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	80	140		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

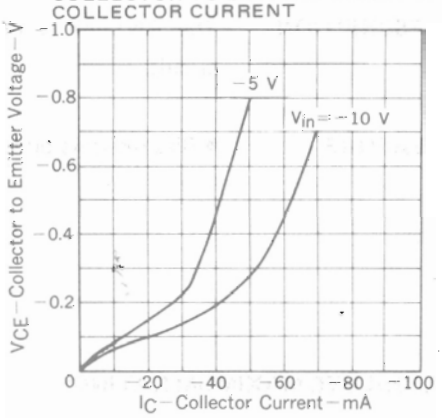
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



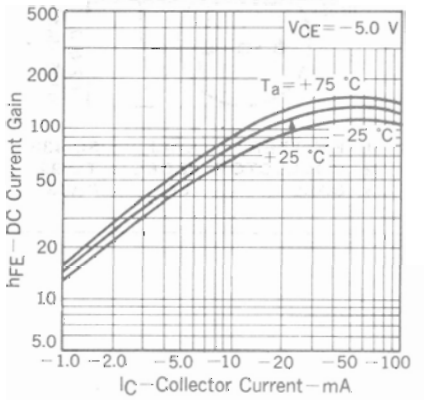
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



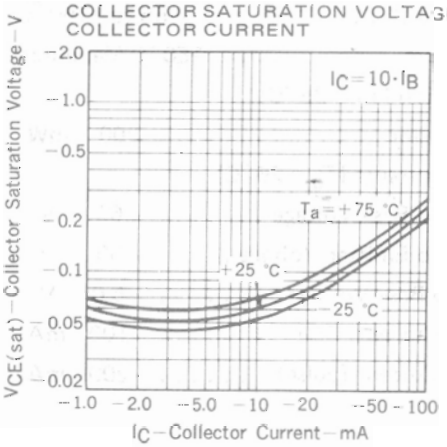
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



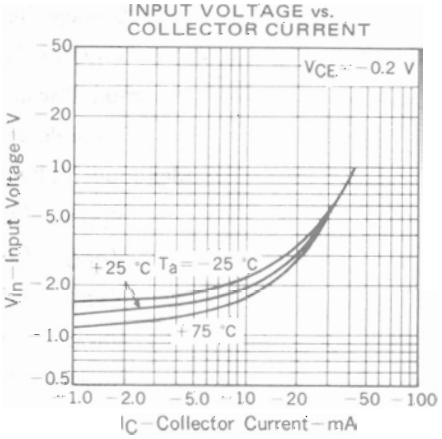
DC CURRENT GAIN vs. COLLECTOR CURRENT



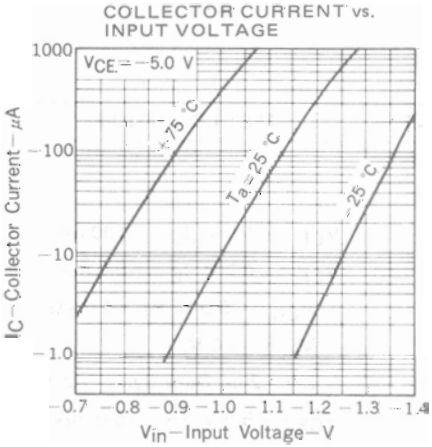
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



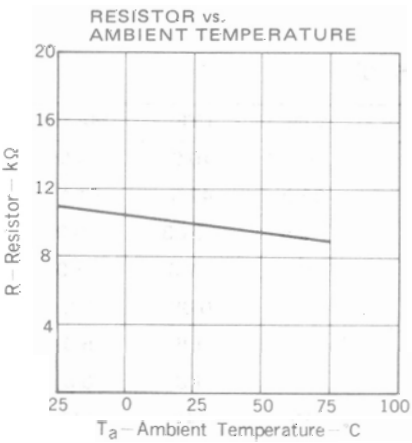
INPUT VOLTAGE vs. COLLECTOR CURRENT



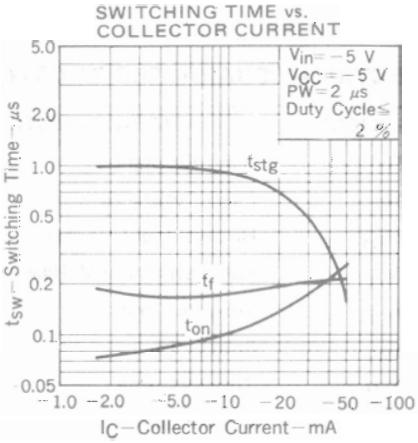
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT

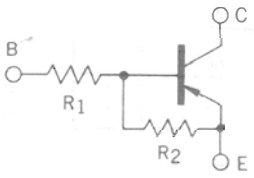


NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1A4P

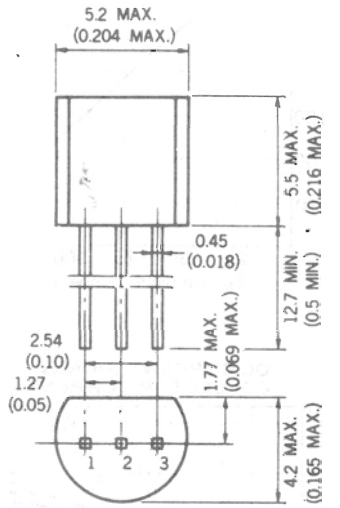
DESCRIPTION The AN1A4P is designed for use in medium speed switching circuit.

FEATURE • Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

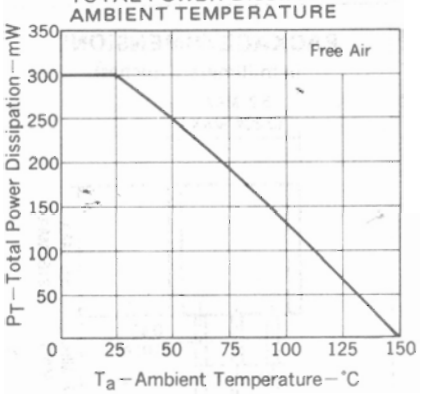
V_{CBO}	Collector to Base Voltage	−60	V
V_{CEO}	Collector to Emitter Voltage	−50	V
V_{EBO}	Emitter to Base Voltage	−5.0	V
$I_{C(DC)}$	Collector Current (DC)	−100	mA
$I_{C(pulse)}$	Collector Current (pulse)	−200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

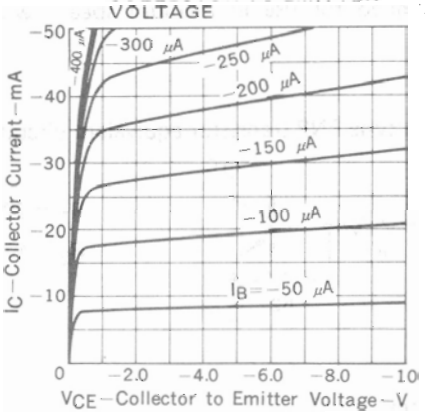
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	−0.5	−0.68	−0.9	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−0.6	−1.0	−3.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.08	0.2	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.5	5.0	μs	V_{in} = −5.0 V.
t_{off}	Turn Off Time		1.8	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	140	340	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	95	190		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

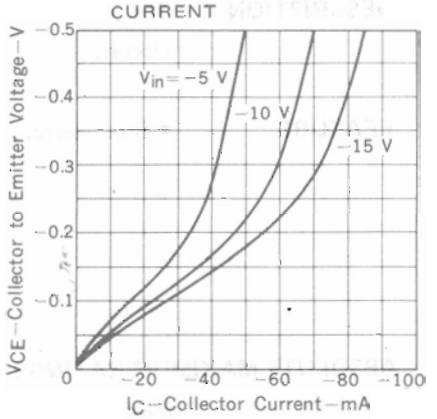
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



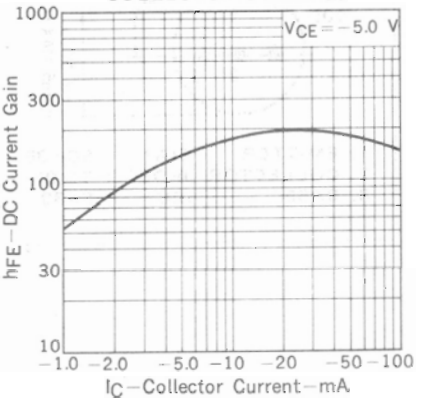
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



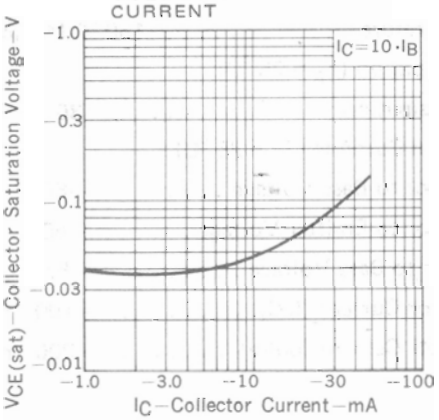
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



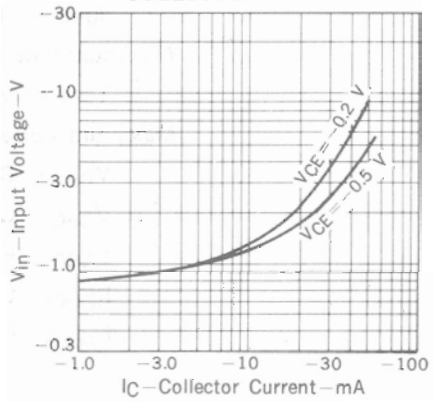
DC CURRENT GAIN vs. COLLECTOR CURRENT



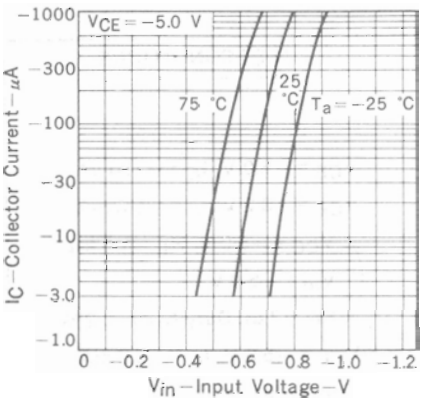
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



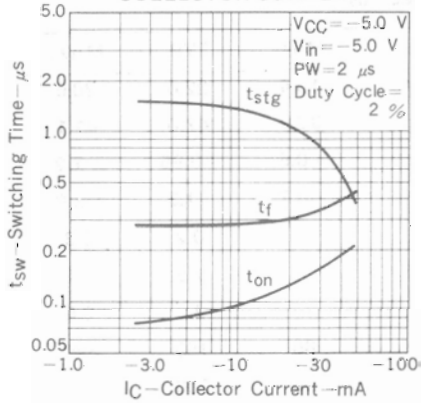
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



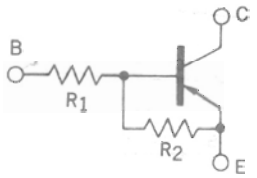
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1F4N

DESCRIPTION The AN1F4N is designed for use in medium speed switching circuit.

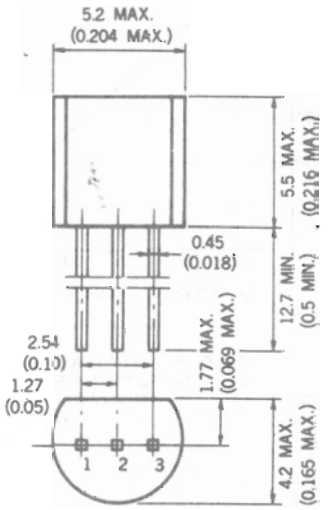
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

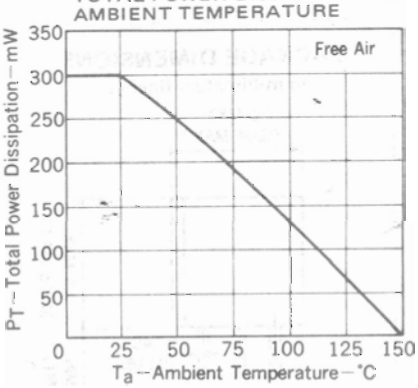
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

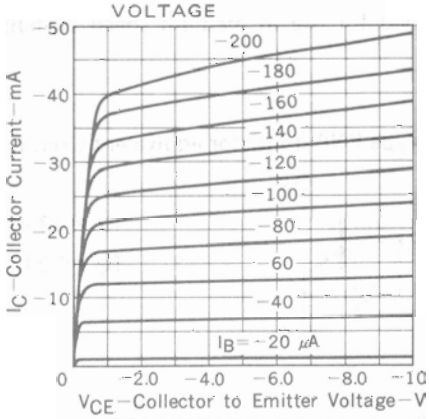
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	−0.6	−0.85	−1.2	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−0.7	−1.3	−3.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.2	0.3	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.5	5.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		2.0	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	150	340	−	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	95	200		−	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

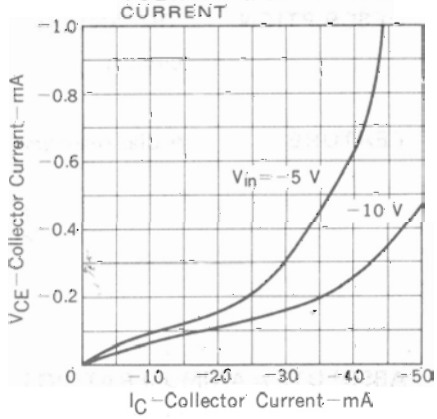
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



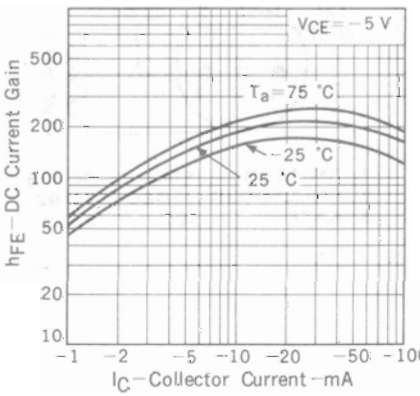
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



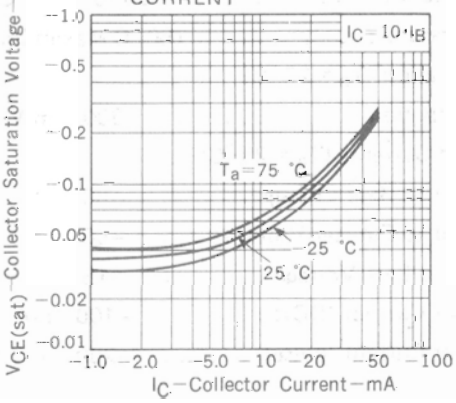
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



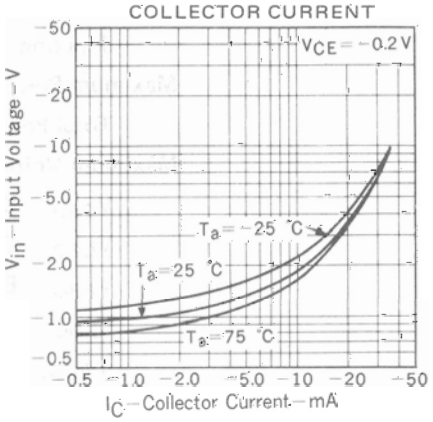
DC CURRENT GAIN vs. COLLECTOR CURRENT



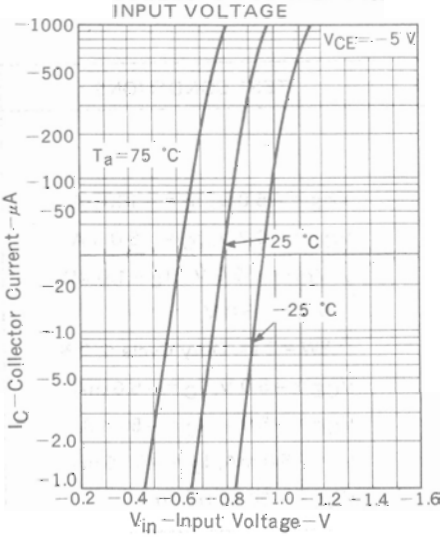
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



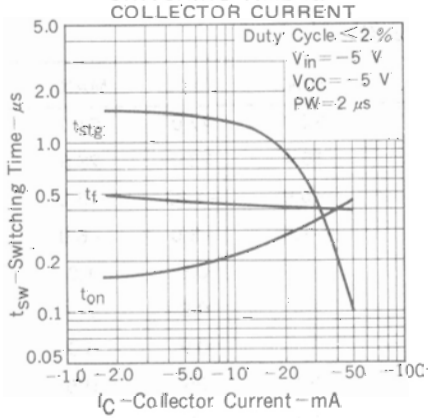
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



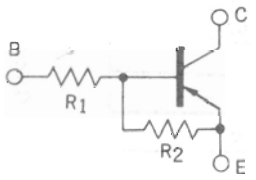
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1L4L

DESCRIPTION The AN1L4L is designed for use in medium speed switching circuit.

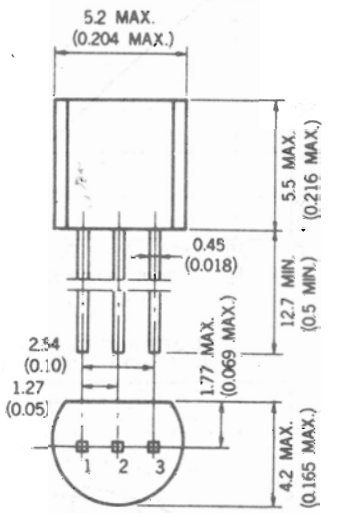
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

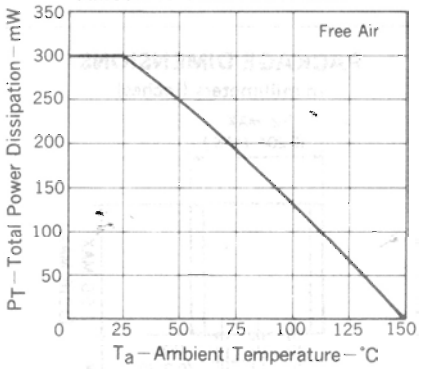
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −15 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

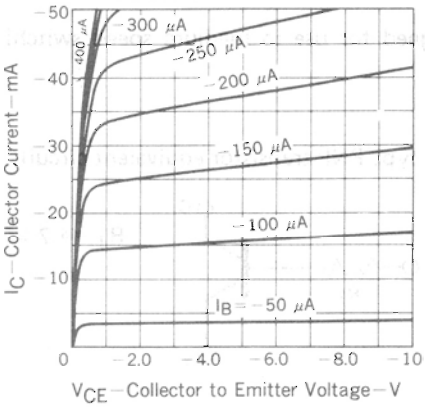
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_2	Input Resistance	15.4	22.0	28.6	kΩ	
V_{IH}	Hi Level Input Voltage	−0.9	−1.83	−3.0	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.5	−3.0	−6.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.5	1.0	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		0.6	3.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		0.9	5.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	95	195	–	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	90	185		–	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

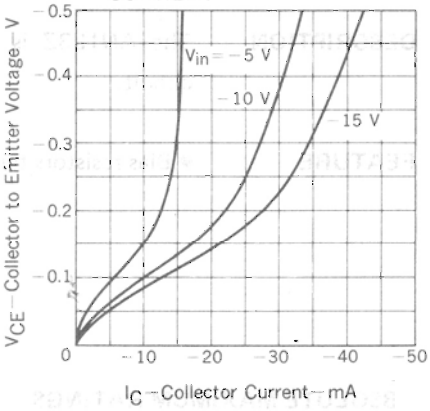
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



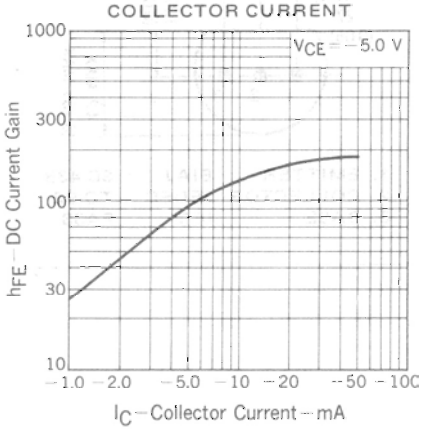
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



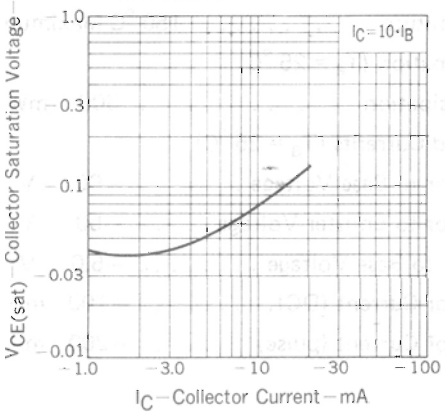
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



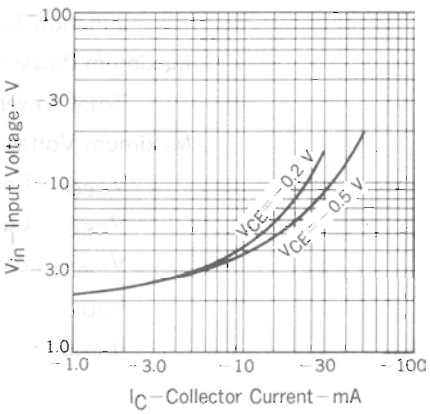
DC CURRENT GAIN vs. COLLECTOR CURRENT



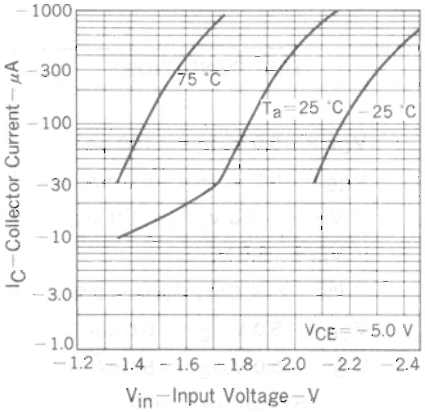
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



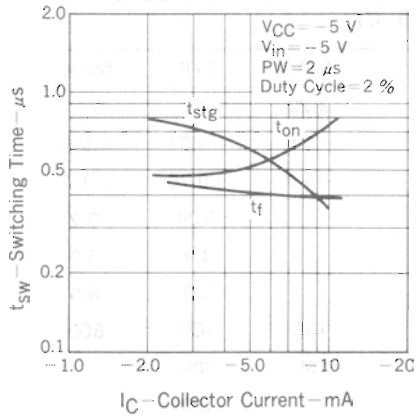
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



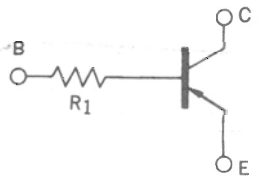
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
AN1L3Z

DESCRIPTION The AN1L3Z is designed for use in medium speed switching circuit.

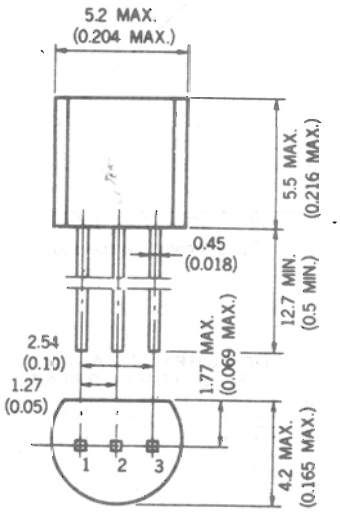
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 4.7 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

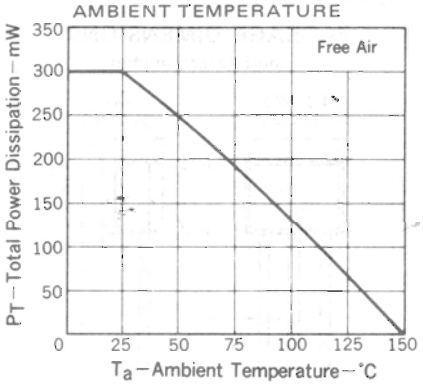
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

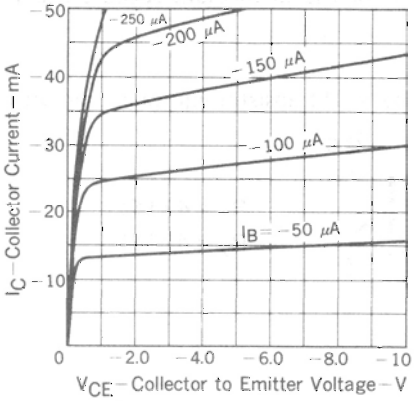
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	3.29	4.7	6.11	kΩ	
V_{IH}	Hi Level Input Voltage	−0.5	−0.57	−0.6	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−0.5	−0.75	−1.2	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.04	0.2	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.7	5.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		1.9	6.0	μs	PW = 2 μs, Duty Cycle ≤ 2 %
h_{FE1}	DC Current Gain	135	260	600	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	100	200		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

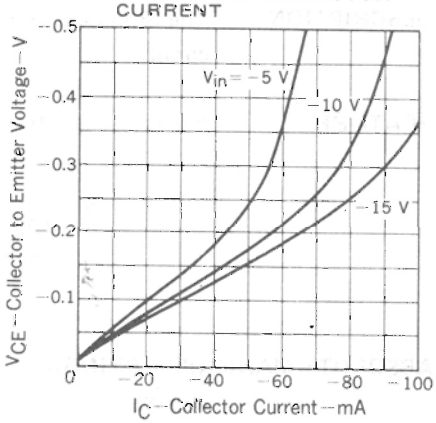
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



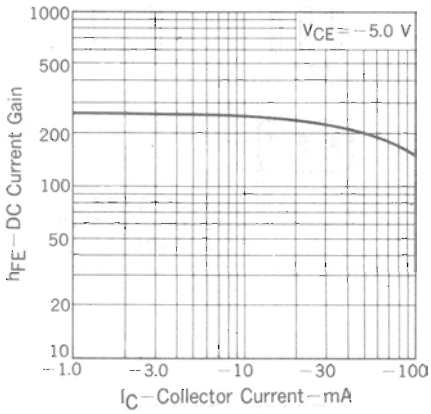
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



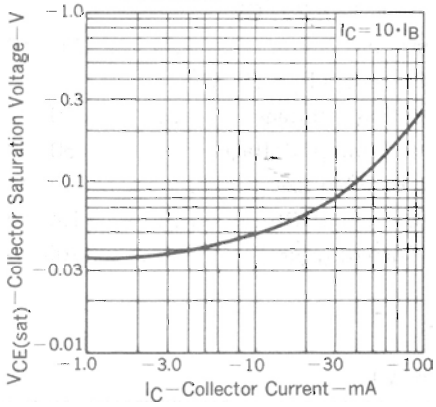
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



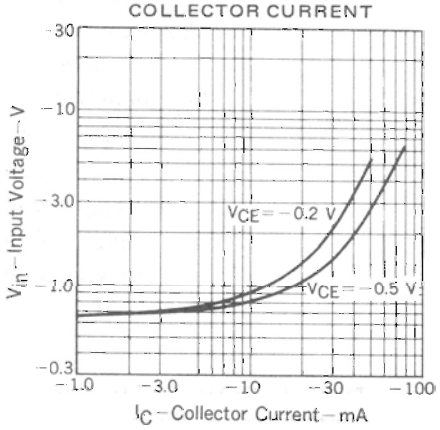
DC CURRENT GAIN vs. COLLECTOR CURRENT



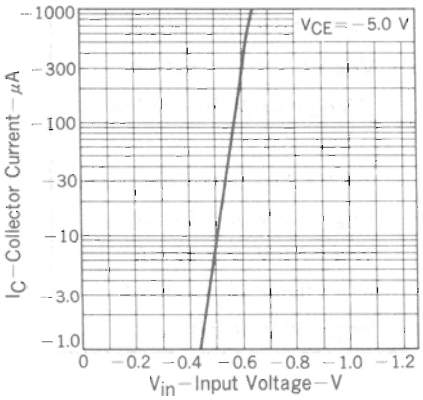
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



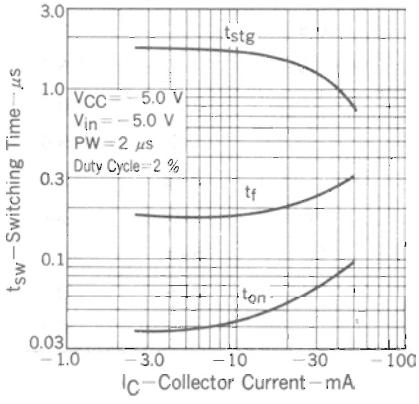
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



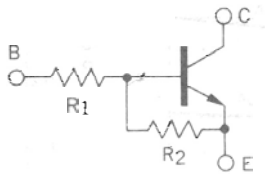
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1L4M

DESCRIPTION The BA1L4M is designed for use in medium speed switching circuit.

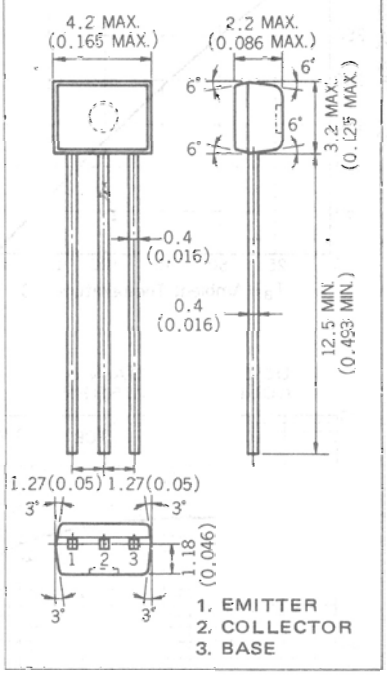
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

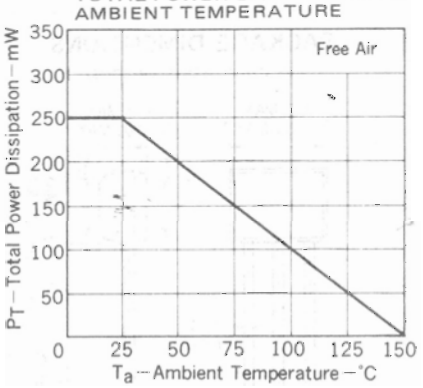
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

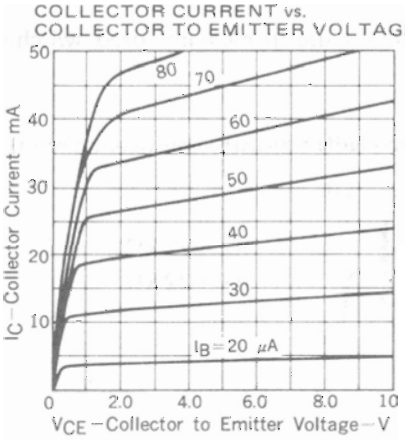
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.7	5.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time		0.27	0.7	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		2.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time		2.48	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	240	340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	95	640		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

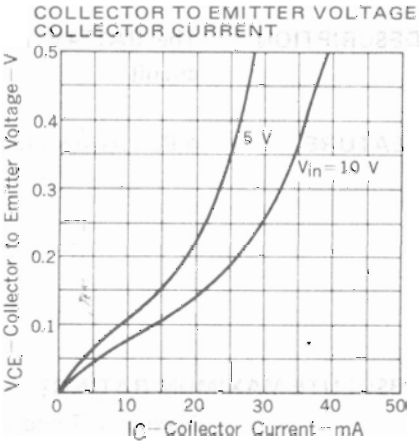
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



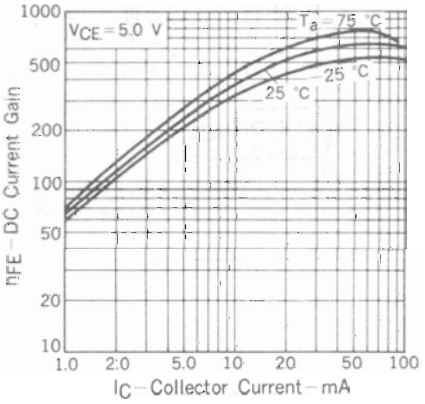
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



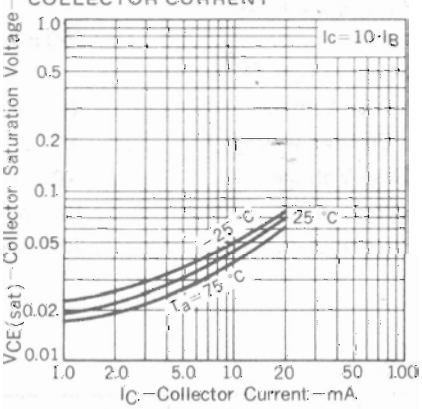
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



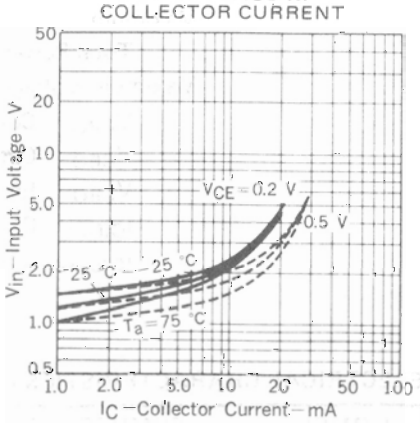
DC CURRENT GAIN vs. COLLECTOR CURRENT



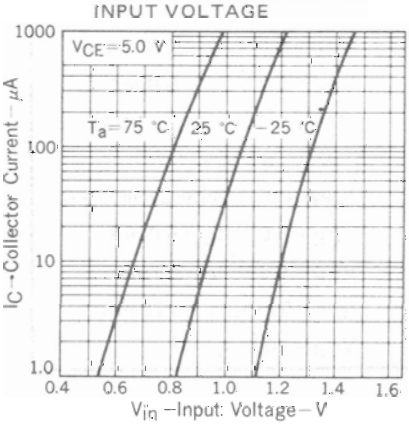
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



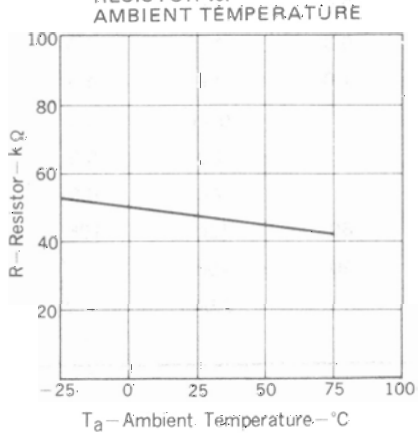
INPUT VOLTAGE vs. COLLECTOR CURRENT



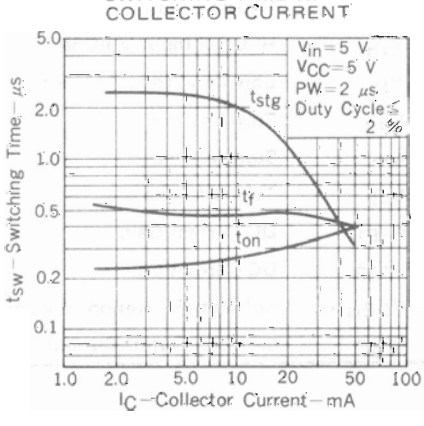
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



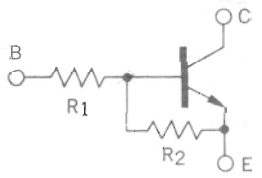
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1F4M

DESCRIPTION The BA1F4M is designed for use in medium speed switching circuit.

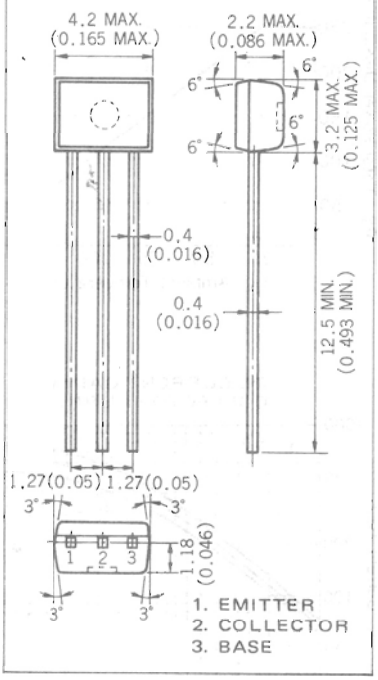
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

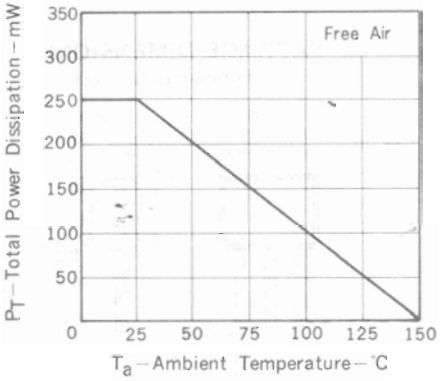
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

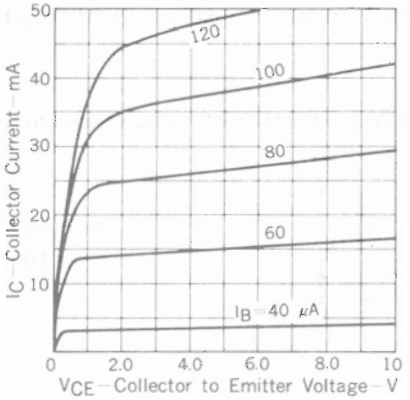
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.6	4.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time		0.11	0.4	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		2.3	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time		2.6	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	120	195	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	90	400		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

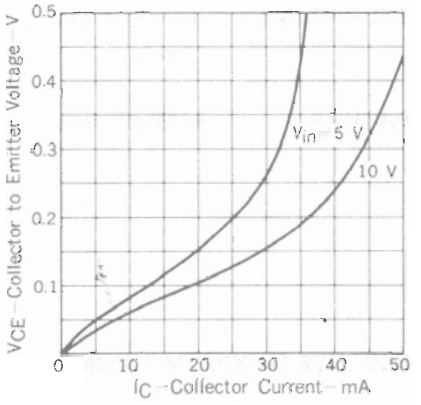
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



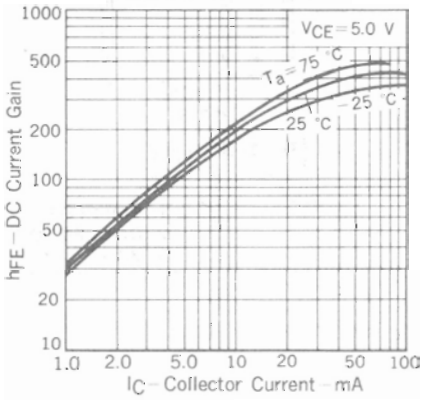
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



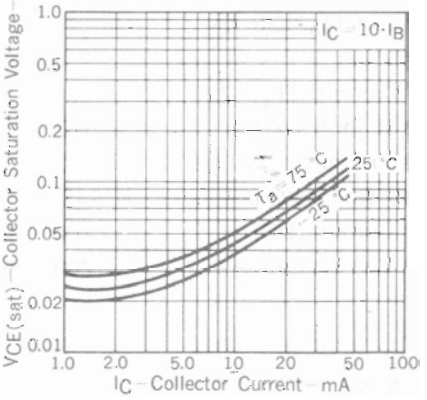
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



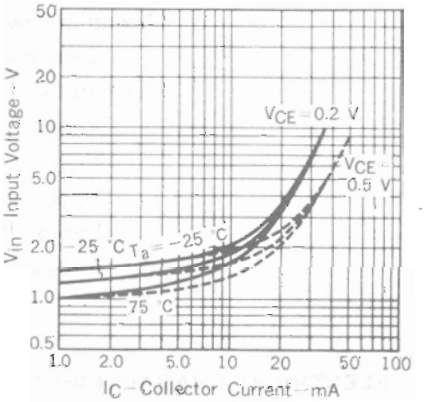
DC CURRENT GAIN vs. COLLECTOR CURRENT



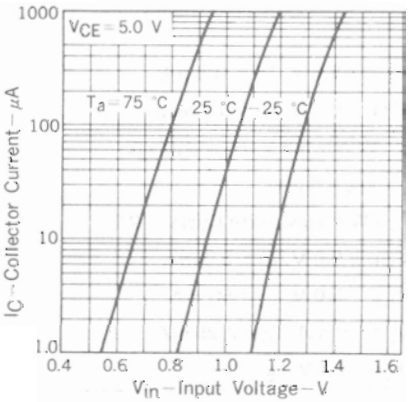
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



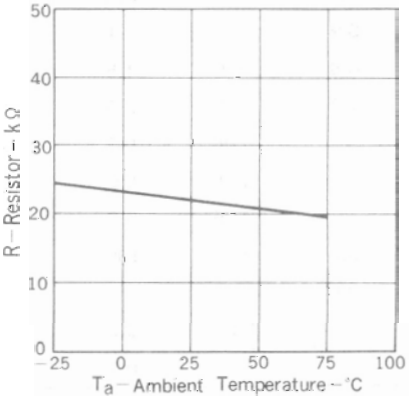
INPUT VOLTAGE vs. COLLECTOR CURRENT



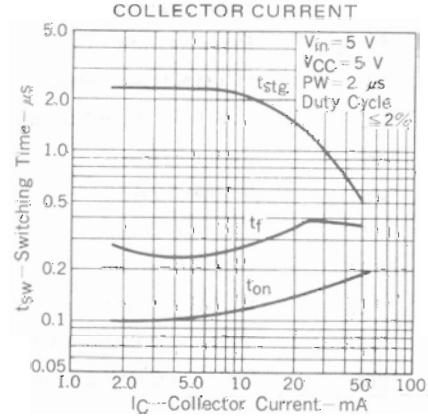
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



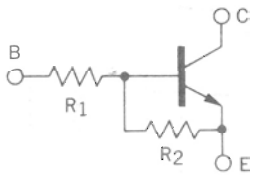
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1A4M

DESCRIPTION The BA1A4M is designed for use in medium speed switching circuit.

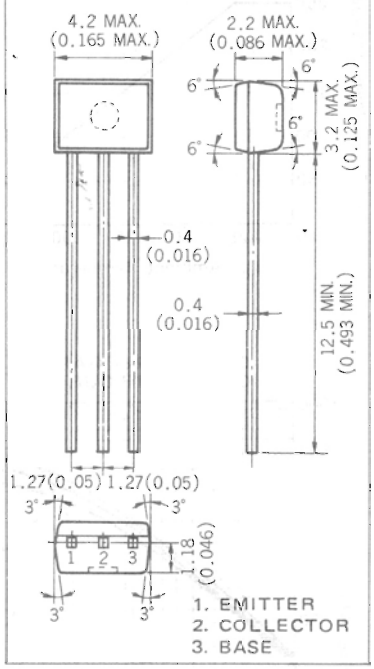
FEATURE

- Bias resistors built in type NPN transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 10 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

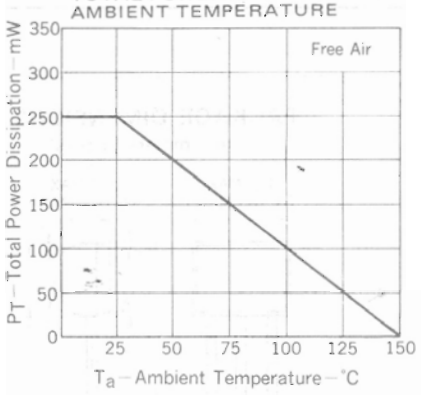
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	10	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

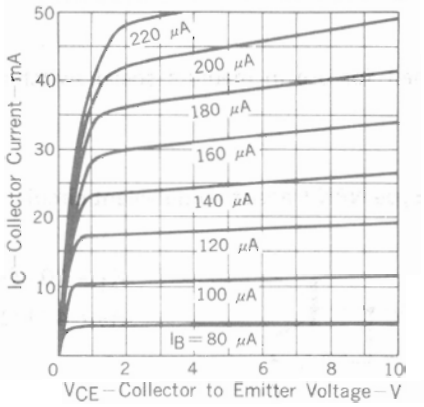
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.4	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time		0.06	0.2	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		2.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time		2.15	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	35	62	100	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	80	230		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.05	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

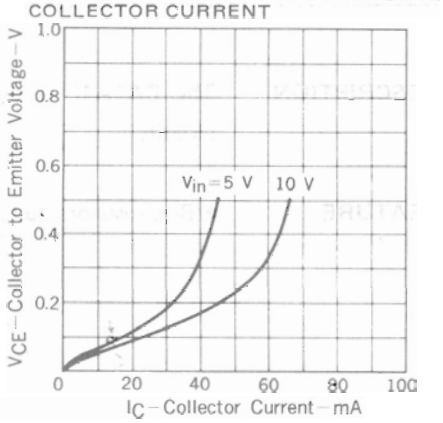
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



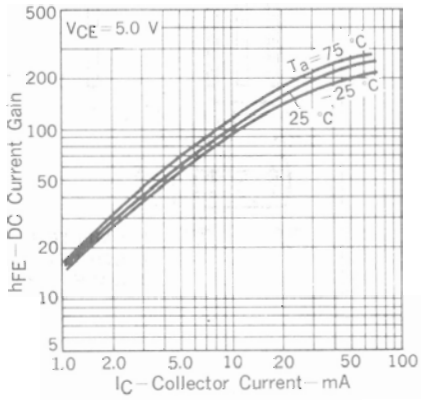
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



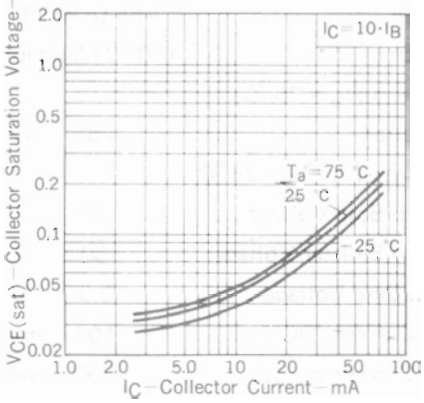
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



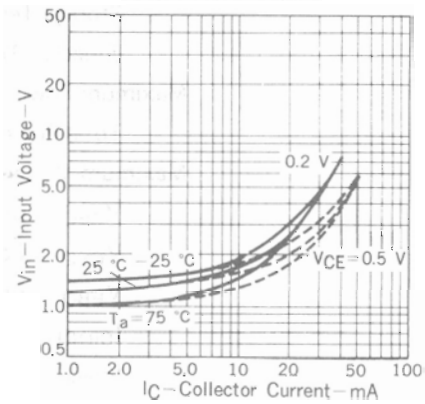
DC CURRENT GAIN vs. COLLECTOR CURRENT



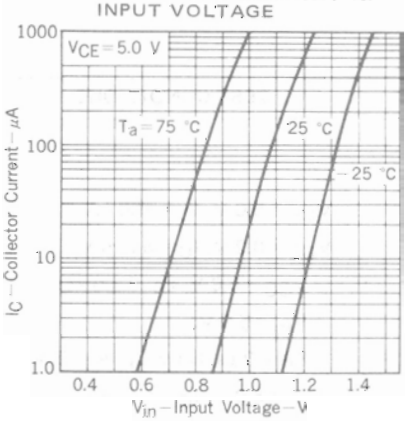
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



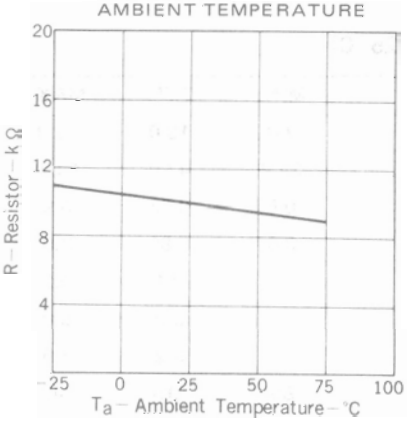
INPUT VOLTAGE vs. COLLECTOR CURRENT



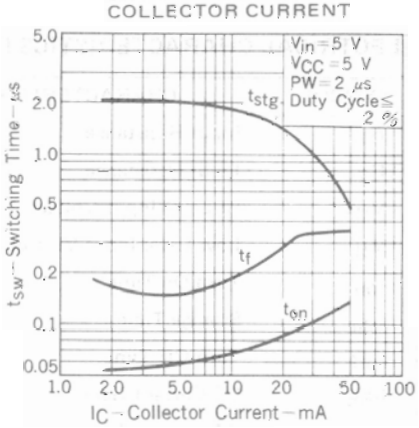
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



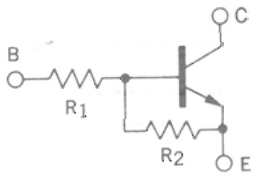
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1A4P

DESCRIPTION The BA1A4P is designed for use in medium speed switching circuit.

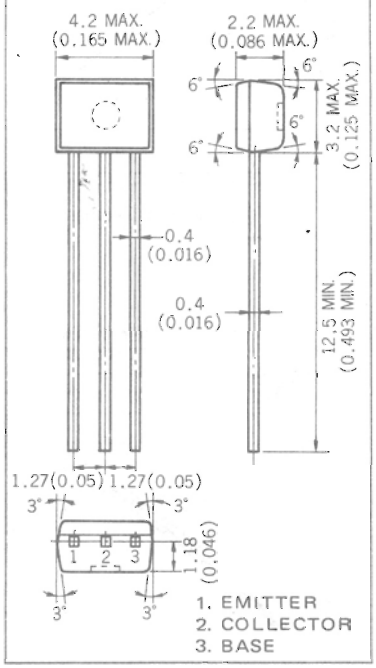
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

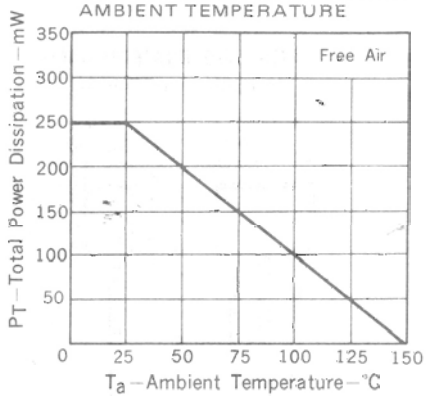
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

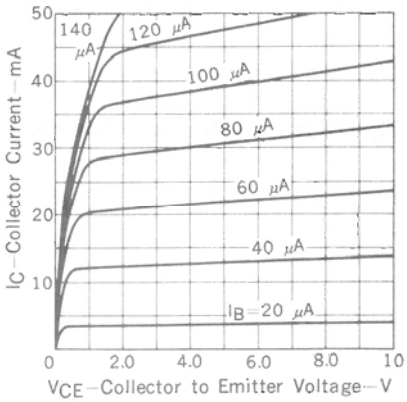
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	0.5	0.65	0.9	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	0.6	0.89	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.1	0.2	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		3.0	5.0	μs	V_{in} = 5.0 V.
t_{off}	Turn Off Time		3.2	6.0	μs	PW = 2 μs, Duty Cycle ≤ 2 %
h_{FE1}	DC Current Gain	85	210	340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	95	370		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

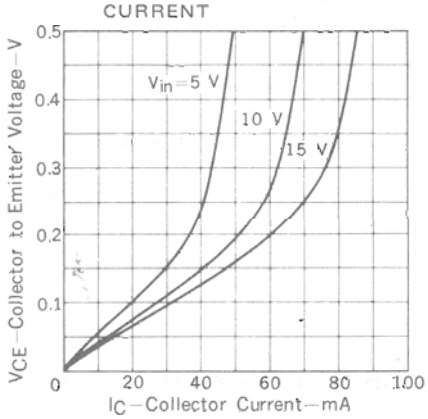
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



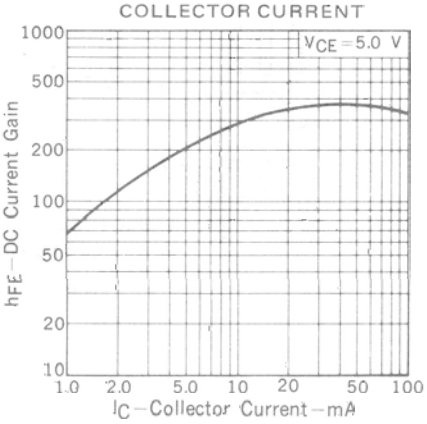
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



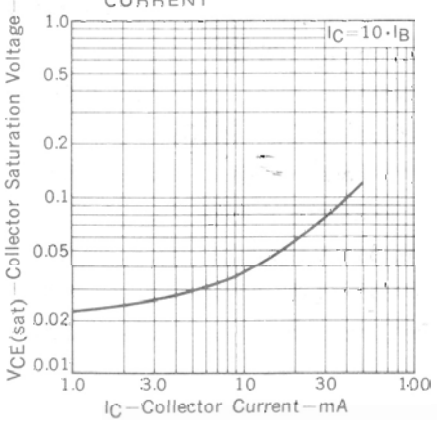
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



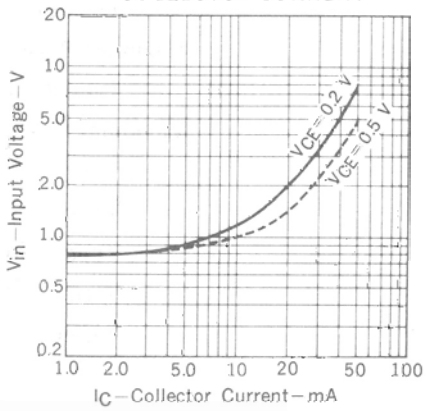
DC CURRENT GAIN vs. COLLECTOR CURRENT



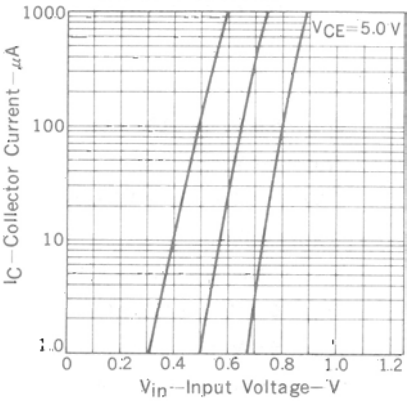
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



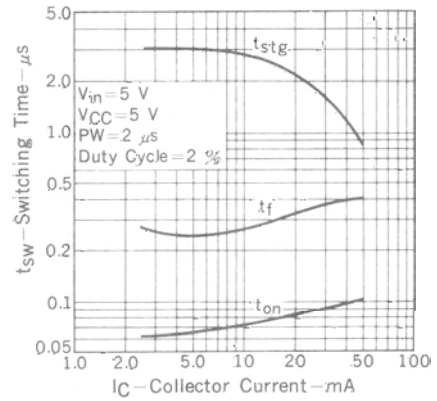
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



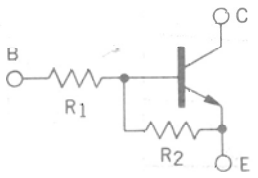
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1F4N

DESCRIPTION The BA1F4N is designed for use in medium speed switching circuit.

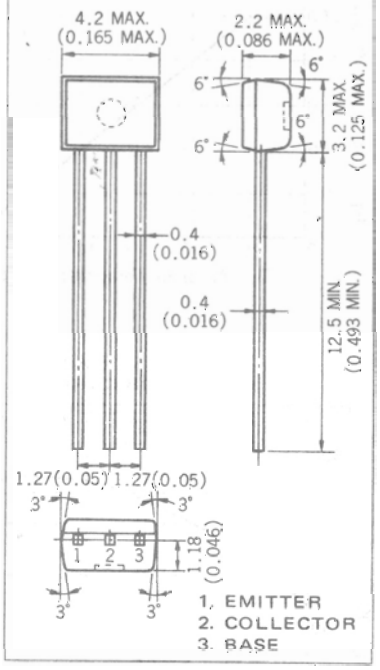
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −55 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

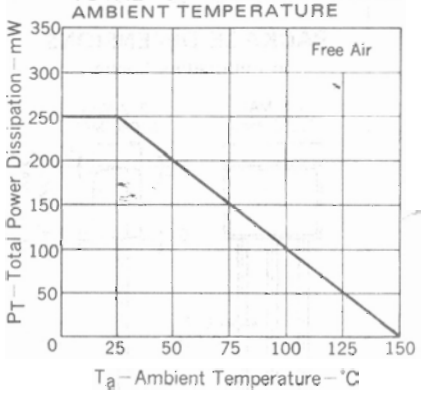
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

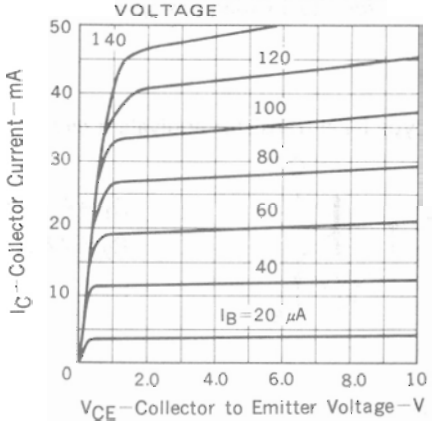
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	0.6	0.8	1.2	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	0.7	1.3	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.2	0.3	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		3.0	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		3.5	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	200	340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	95	230		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

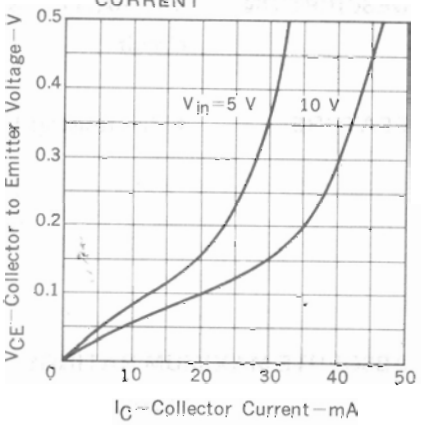
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



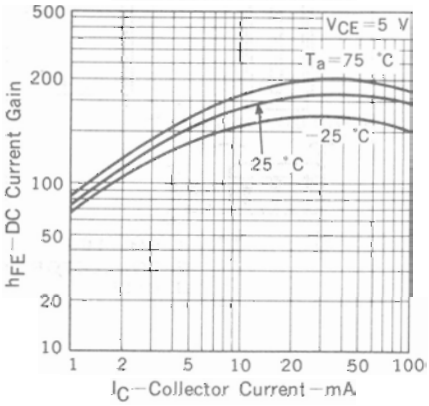
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



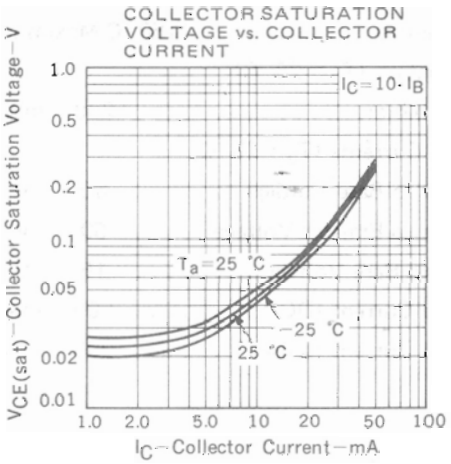
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



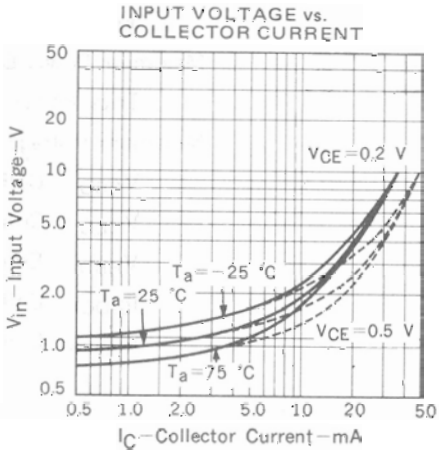
DC CURRENT GAIN vs. COLLECTOR CURRENT



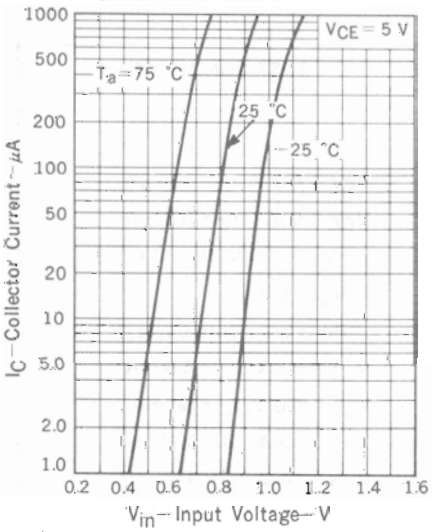
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



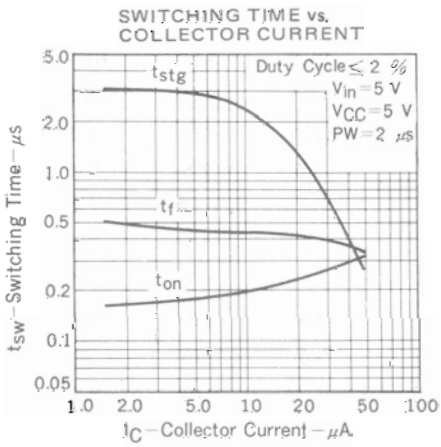
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



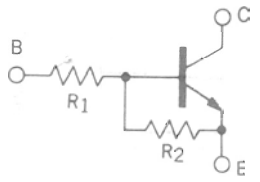
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1L4L

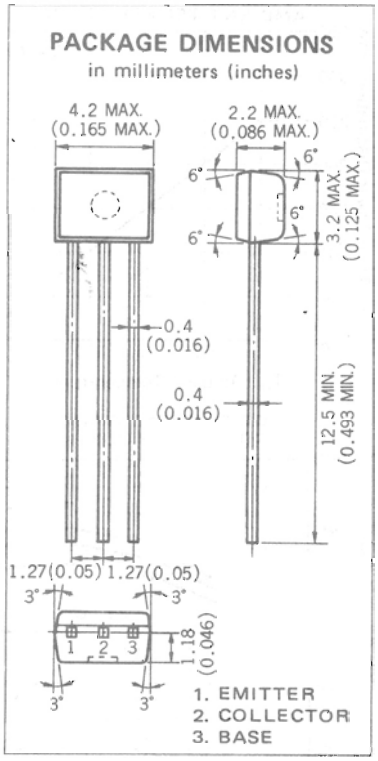
DESCRIPTION The BA1L4L is designed for use in medium speed switching circuit.

FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 22 kΩ



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

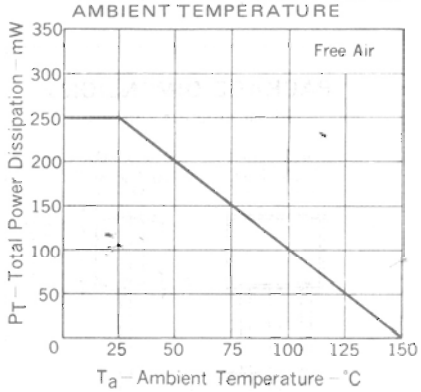
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 15 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

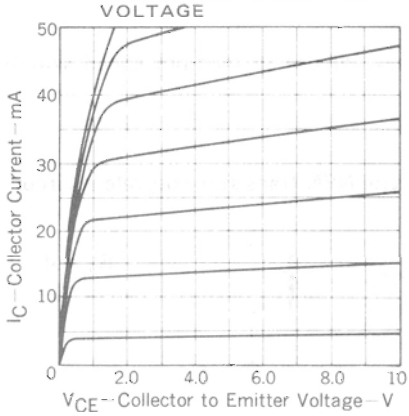
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_2	Input Resistance	15.4	22.0	28.6	kΩ	
V_{IH}	Hi Level Input Voltage	0.9	1.7	3.0	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.5	2.5	3.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.38	1.0	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.2	3.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		1.6	5.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	120	195	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	90	340		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

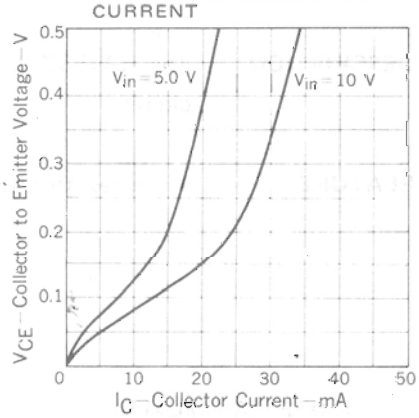
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



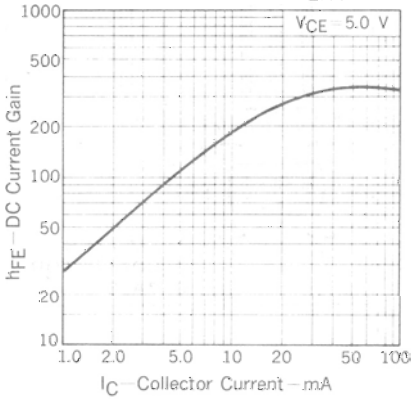
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



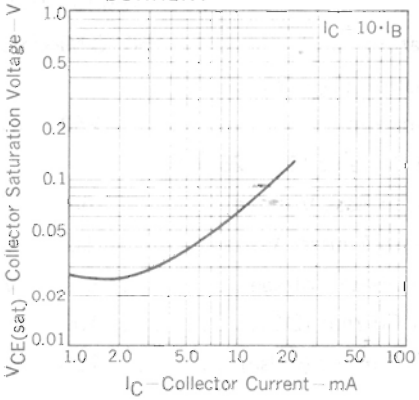
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



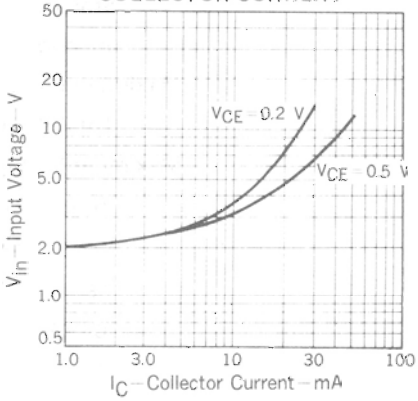
DC CURRENT GAIN vs. COLLECTOR CURRENT



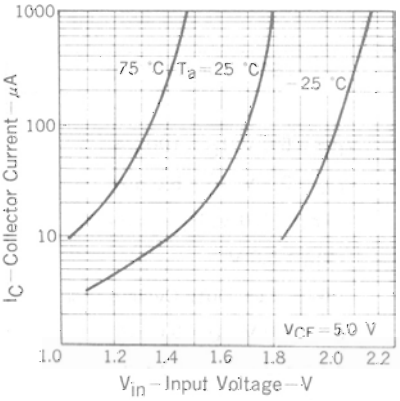
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



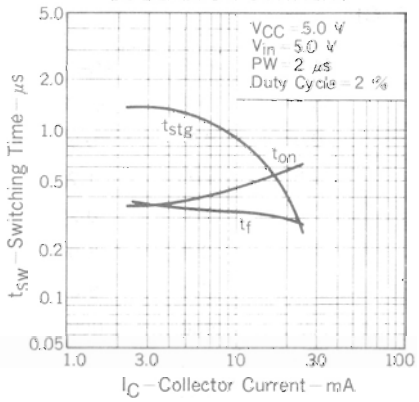
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



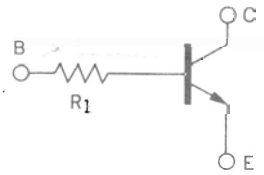
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
BA1L3Z

DESCRIPTION The BA1L3Z is designed for use in medium speed switching circuit.

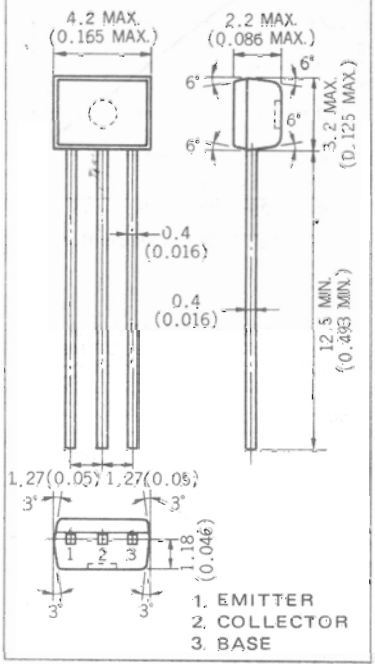
FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



R_1 = 4.7 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

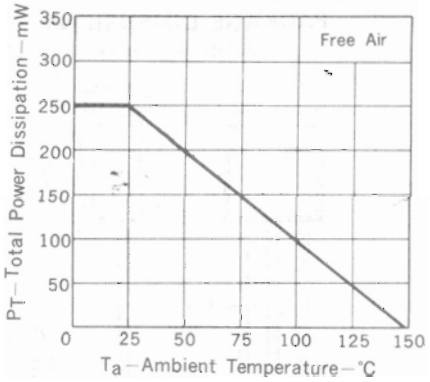
V_{CBO}	Collector to Base Voltage	60	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	5.0	V
$I_{C(DC)}$	Collector Current (DC)	100	mA
$I_{C(pulse)}$	Collector Current (pulse)	200	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

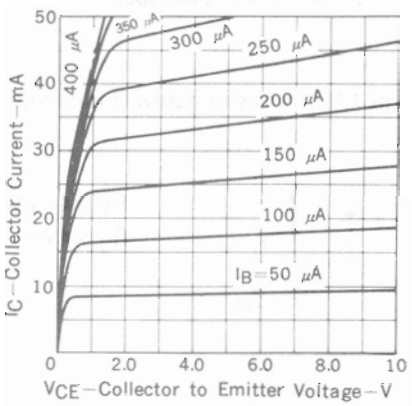
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	3.29	4.7	6.11	kΩ	
V_{IH}	Hi Level Input Voltage	0.5	0.54	0.6	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	0.5	0.71	1.2	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn On Time		0.03	0.2	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		3.2	5.0	μs	V_{in} = 5.0 V,
t_{off}	Turn Off Time		3.4	6.0	μs	PW = 2 μs, Duty Cycle ≤ 2 %
h_{FE1}	DC Current Gain	135	450	600	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	100	380		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.04	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

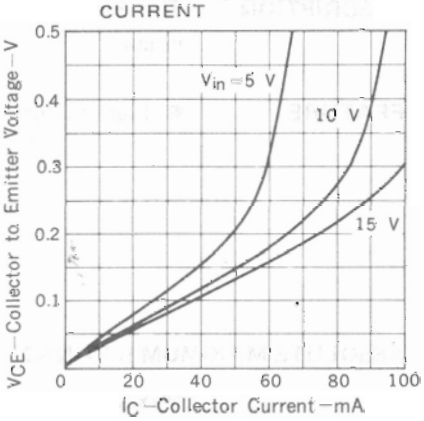
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



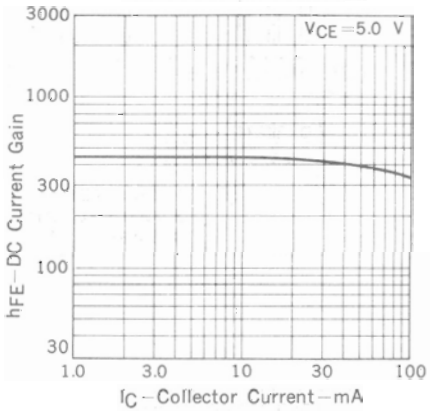
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



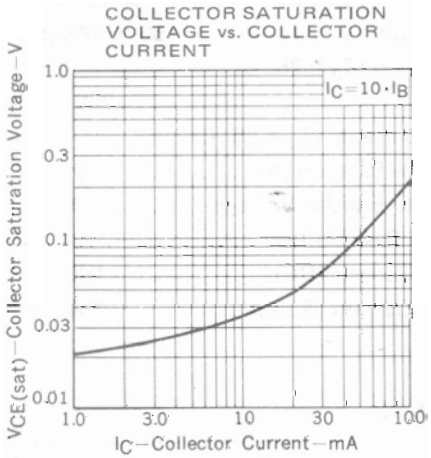
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



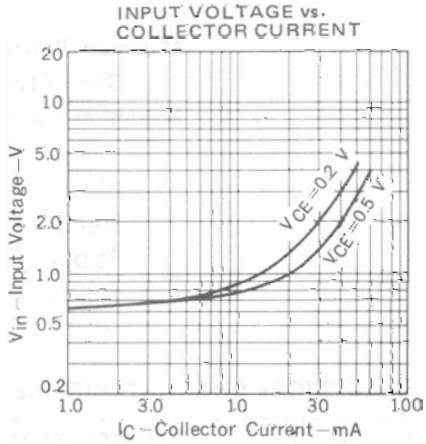
DC CURRENT GAIN vs. COLLECTOR CURRENT



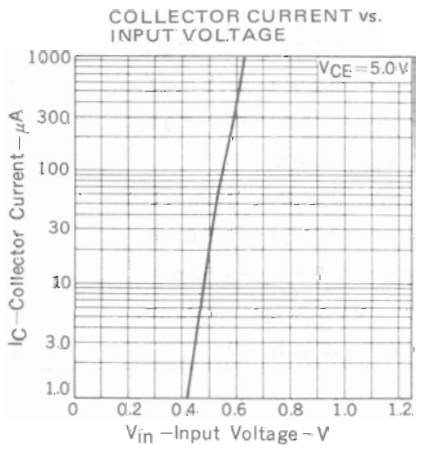
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



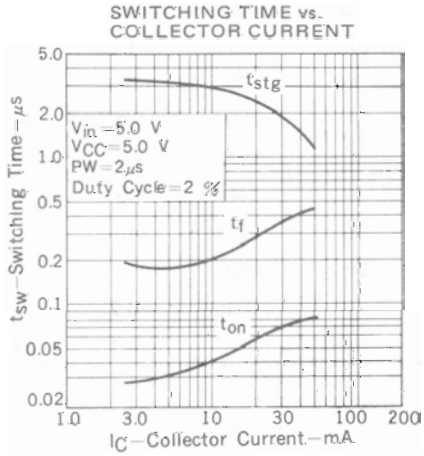
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



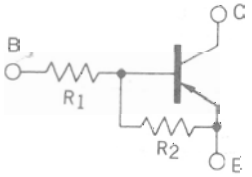
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1L4M

DESCRIPTION The BN1L4M is designed for use in medium speed switching circuit.

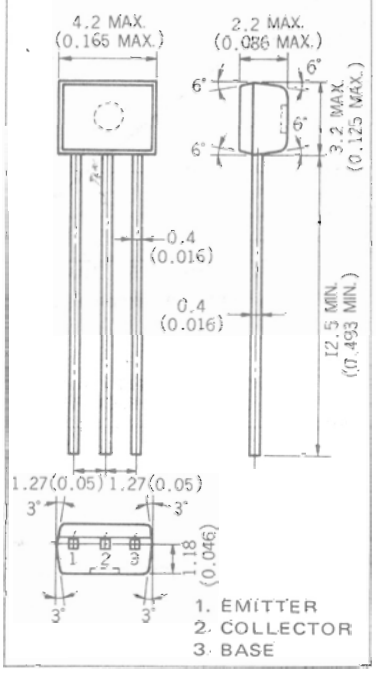
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

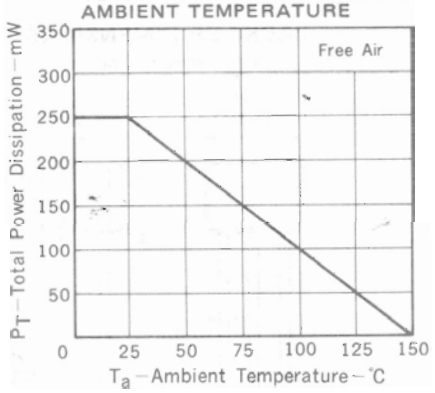
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (Pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

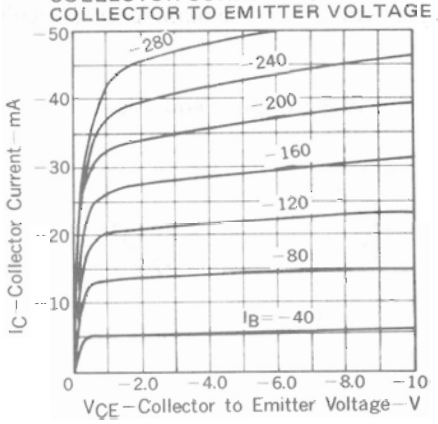
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	−0.8	−1.17	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−2.4	−5.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time		0.5	1.0	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		0.8	3.0	μs	V_{in} = −5.0 V,
t_{off}	Turn off Time		1.4	4.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	135	340	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	95	180		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.05	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

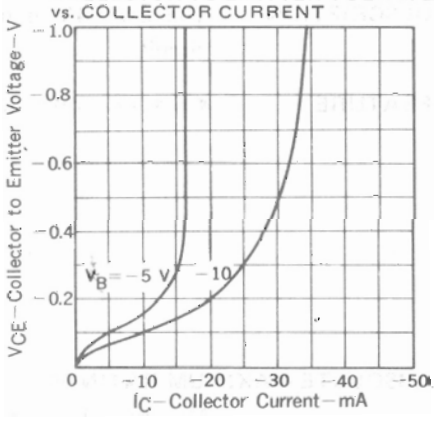
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



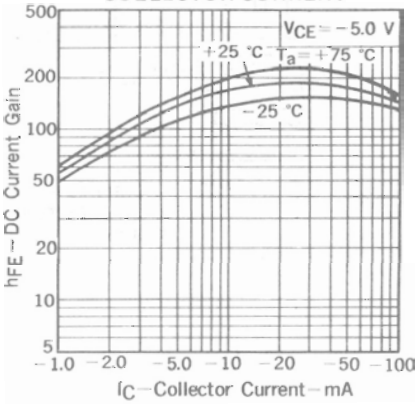
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



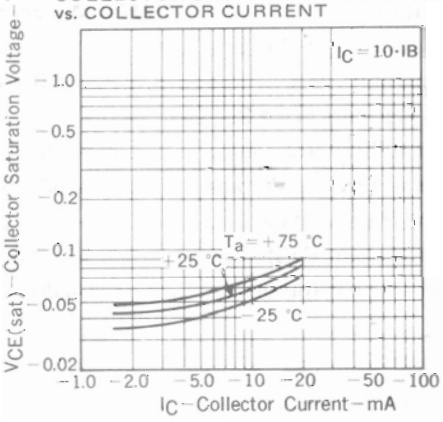
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



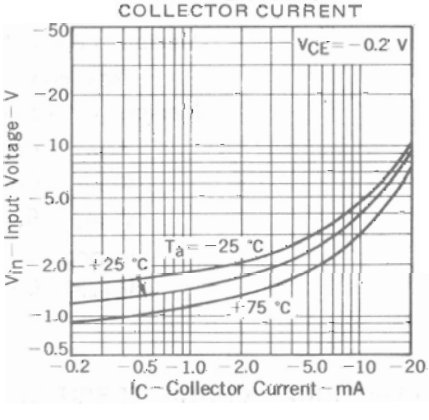
DC CURRENT GAIN vs. COLLECTOR CURRENT



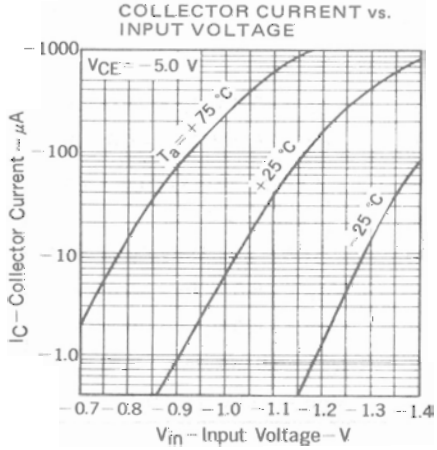
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



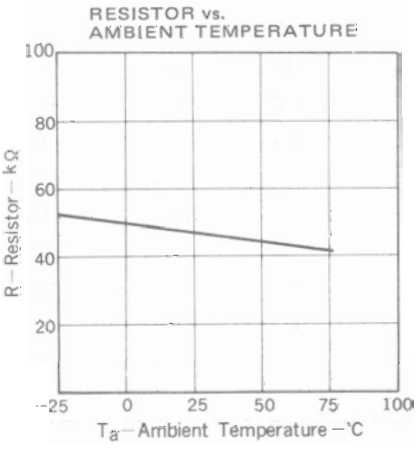
INPUT VOLTAGE vs. COLLECTOR CURRENT



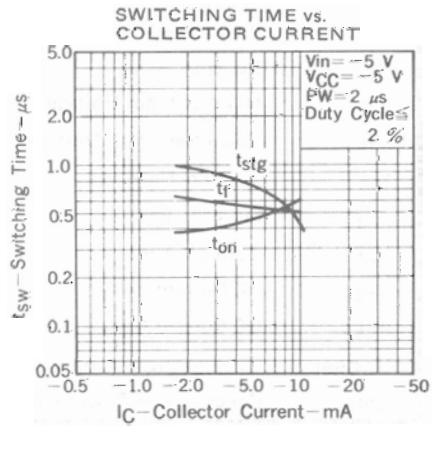
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



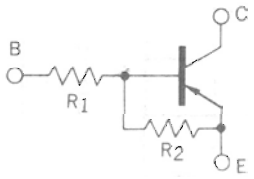
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1F4M

DESCRIPTION The BN1F4M is designed for use in medium speed switching circuit.

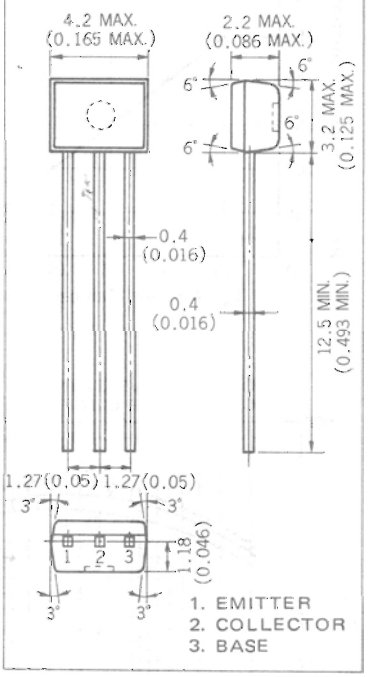
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

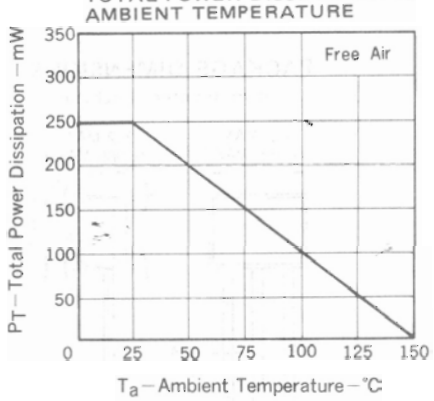
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

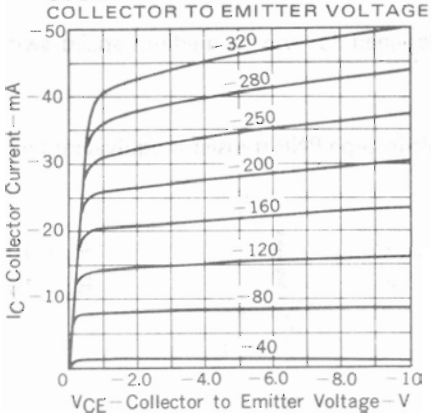
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	−0.8	−1.17	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−2.0	−4.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time		0.23	0.5	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time		0.8	3.0	μs	V_{in} = −5.0 V
t_{off}	Turn off Time		1.1	3.5	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	85	195	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	90	145		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.05	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

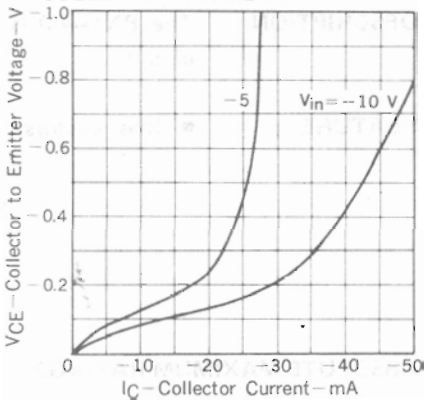
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



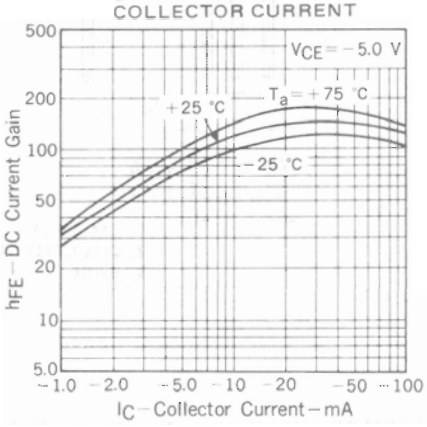
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



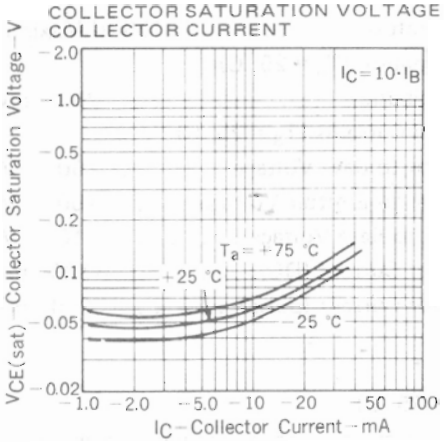
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



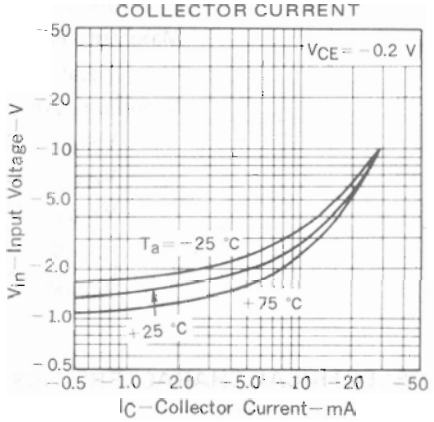
DC CURRENT GAIN vs. COLLECTOR CURRENT



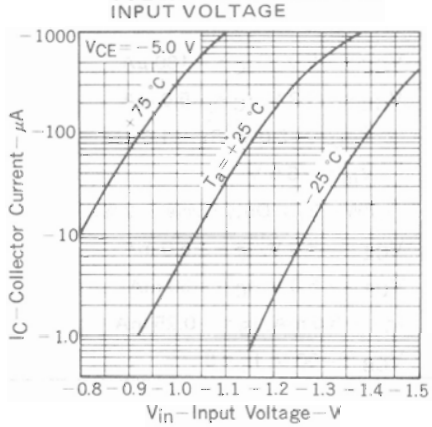
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



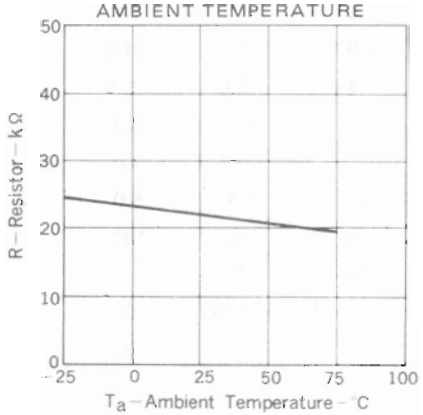
INPUT VOLTAGE vs. COLLECTOR CURRENT



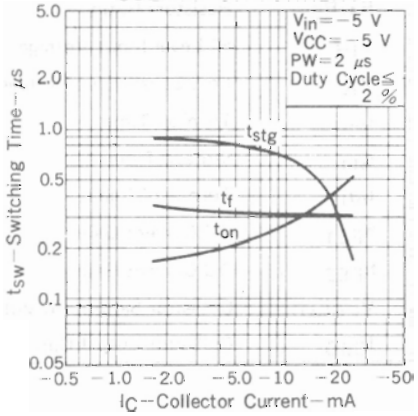
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



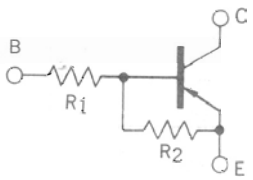
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1A4M

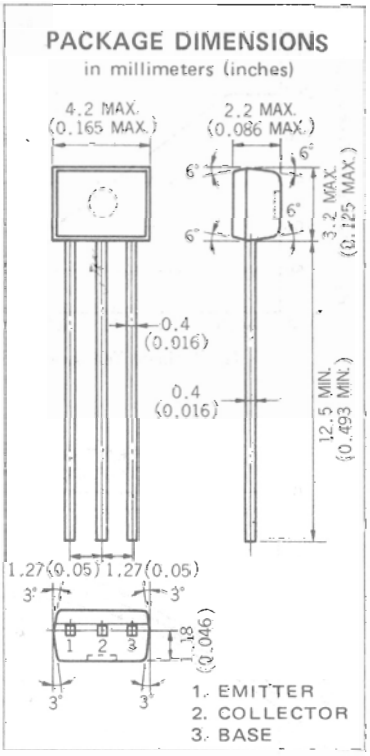
DESCRIPTION The BN1A4M is designed for use in medium speed switching circuit.

FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 10 kΩ



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

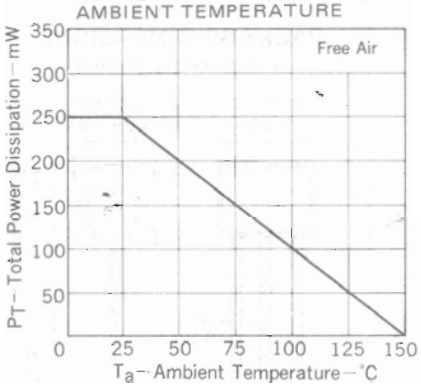
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

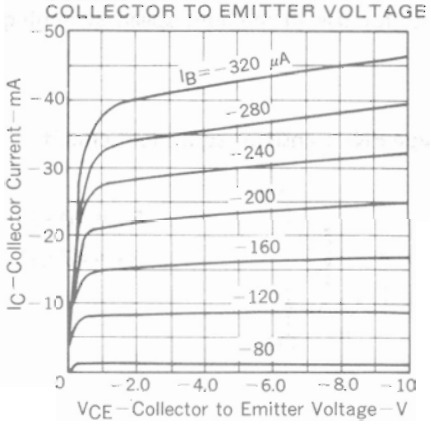
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	–	
V_{IH}	Hi Level Input Voltage	−0.8	−1.13	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−1.6	−3.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time		0.1	0.5	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ, V_{in} = −5.0 V, PW = 2 μs, Duty Cycle ≦ 2 %
t_{stg}	Storage Time		0.95	3.0	μs	
t_{off}	Turn off Time		1.1	5.0	μs	
h_{FE1}	DC Current Gain	35	50	100	–	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	80	140		–	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

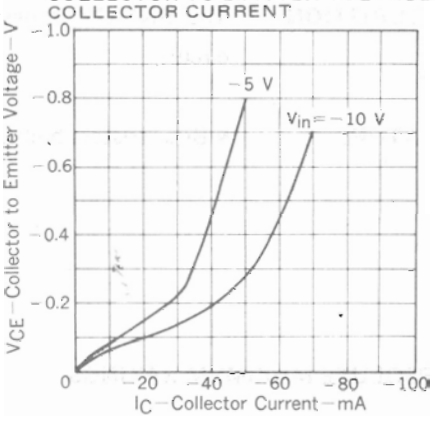
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



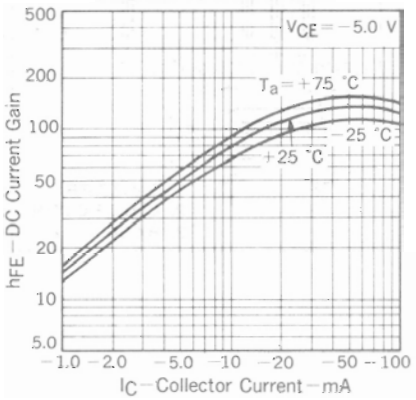
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



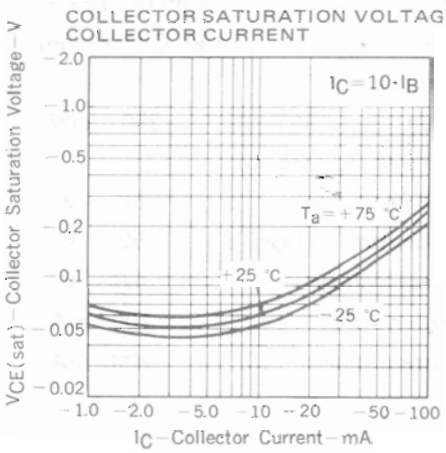
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



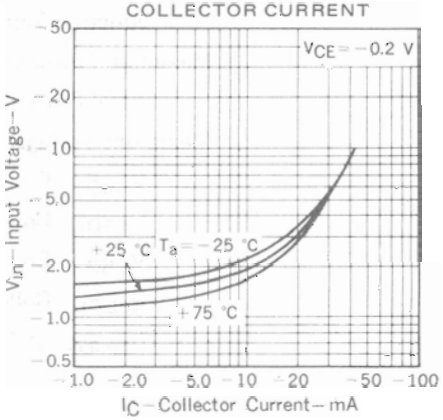
DC CURRENT GAIN vs. COLLECTOR CURRENT



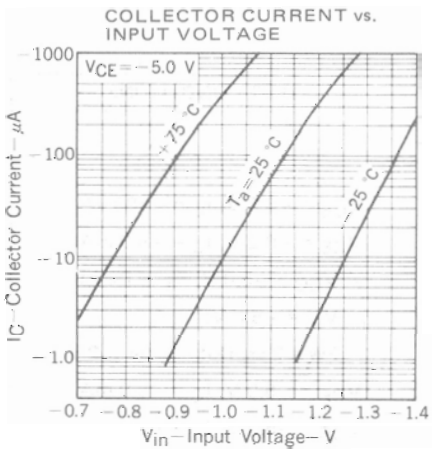
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



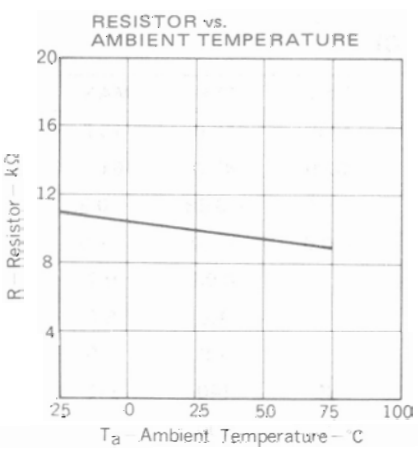
INPUT VOLTAGE vs. COLLECTOR CURRENT



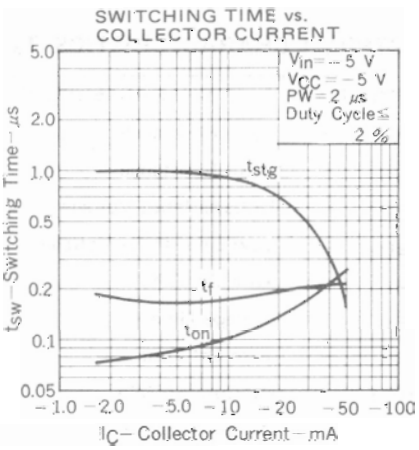
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



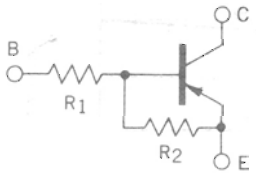
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1A4P

DESCRIPTION The BN1A4P is designed for use in medium speed switching circuit.

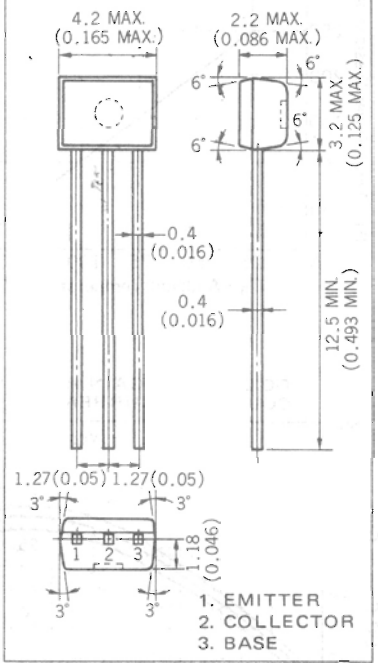
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 10 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

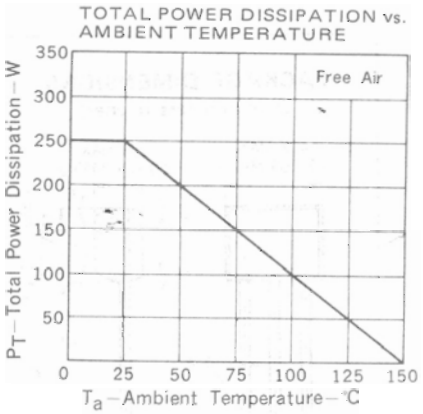
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

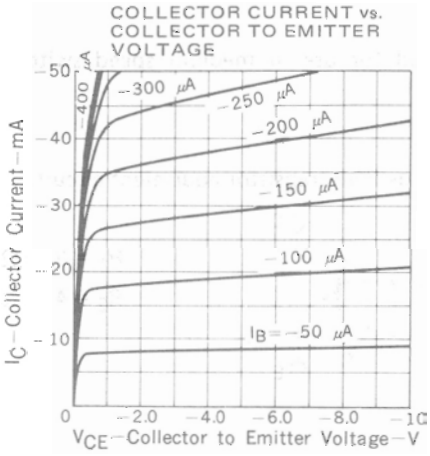
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0	10.0	13.0	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	−0.5	−0.68	−0.9	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−0.6	−1.0	−3.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.08	0.2	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.5	5.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		1.8	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	140	340	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	95	190		—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

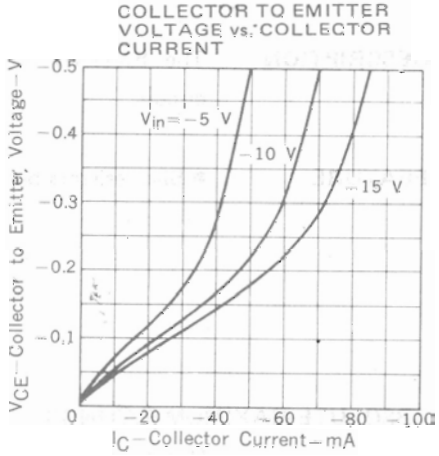
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



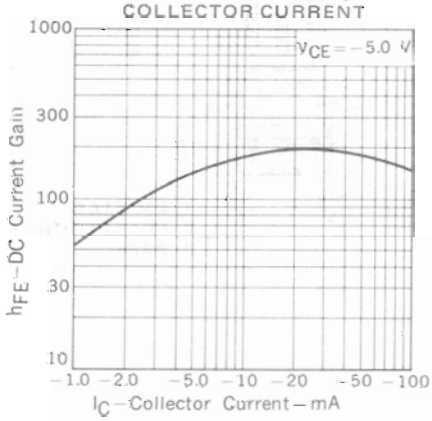
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



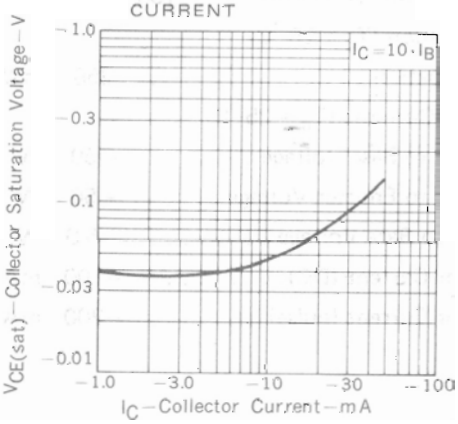
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



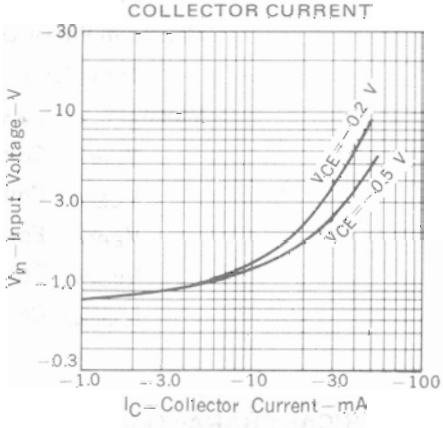
DC CURRENT GAIN vs. COLLECTOR CURRENT



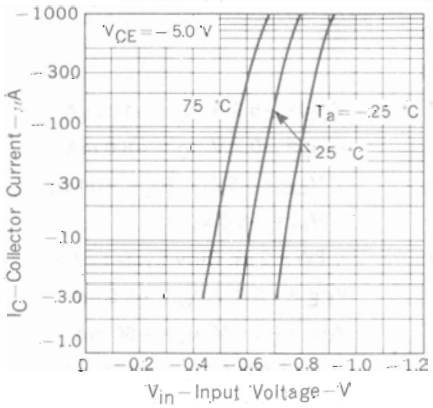
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



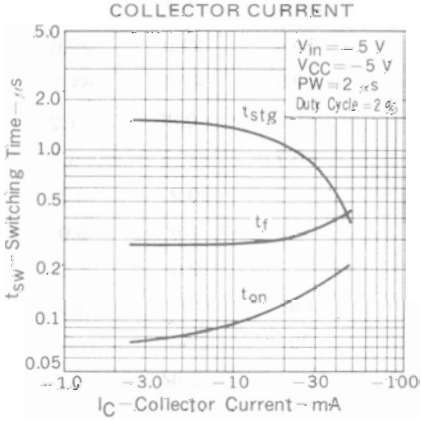
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



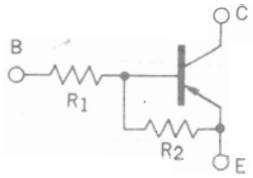
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1F4N

DESCRIPTION The BN1F4N is designed for use in medium speed switching circuit.

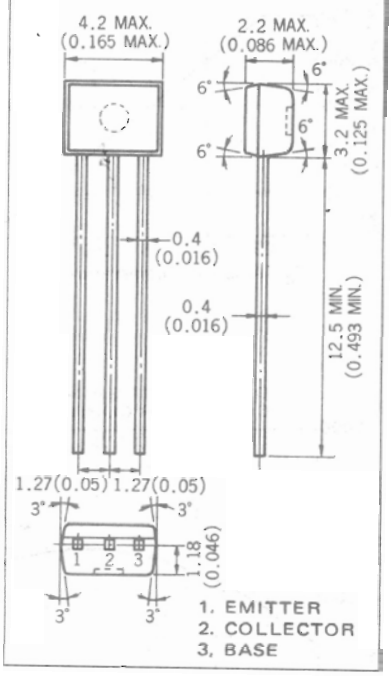
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 22 kΩ
R_2 = 47 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

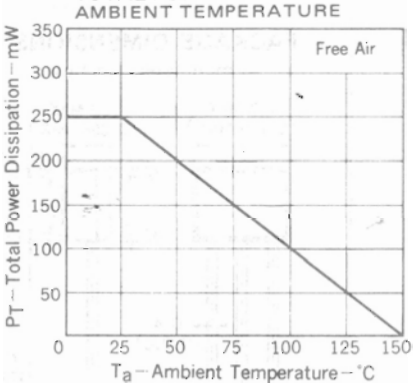
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

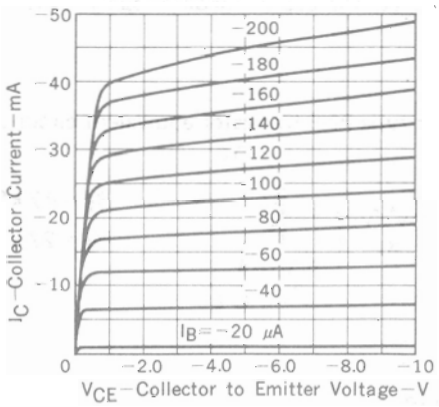
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	15.4	22.0	28.6	kΩ	
R_2	Input Resistance	32.9	47.0	61.1	kΩ	
V_{IH}	Hi Level Input Voltage	−0.6	−0.85	−1.2	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−0.7	−1.3	−3.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.2	0.3	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.5	5.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		2.0	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	85	150	340	–	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	95	200		–	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

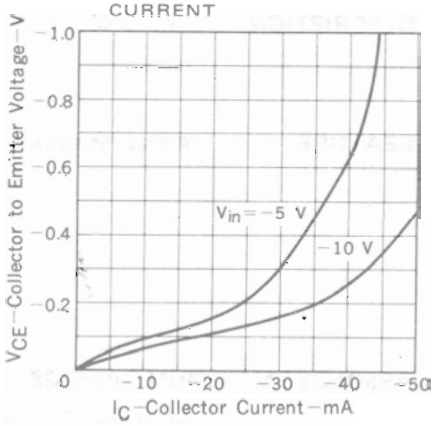
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



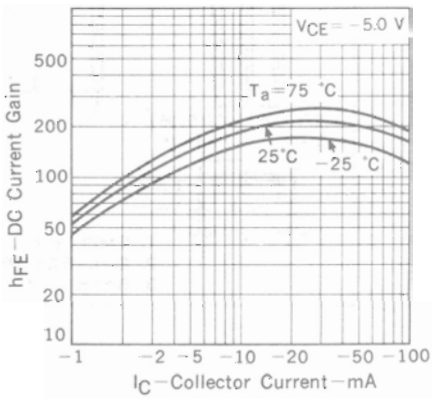
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



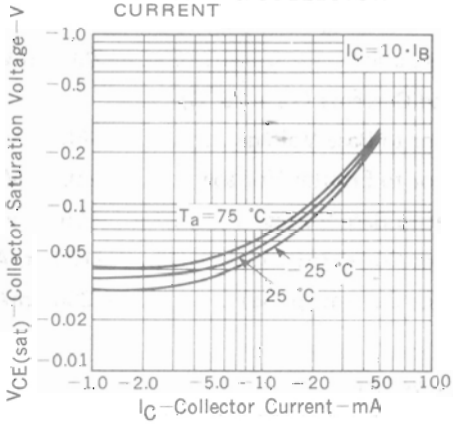
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



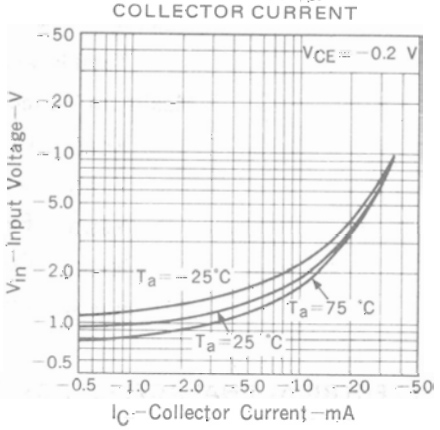
DC CURRENT GAIN vs. COLLECTOR CURRENT



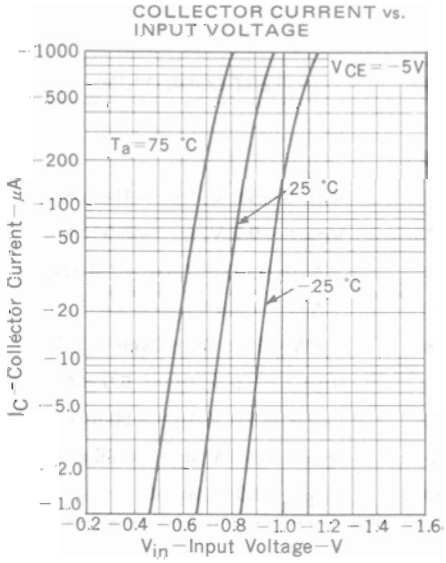
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



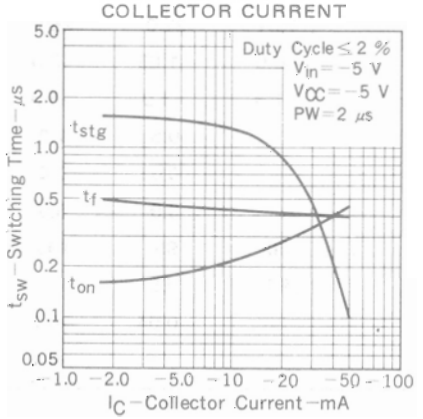
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



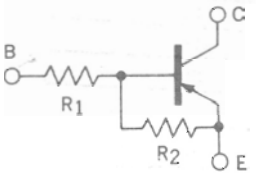
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1L4L

DESCRIPTION The BN1L4L is designed for use in medium speed switching circuit.

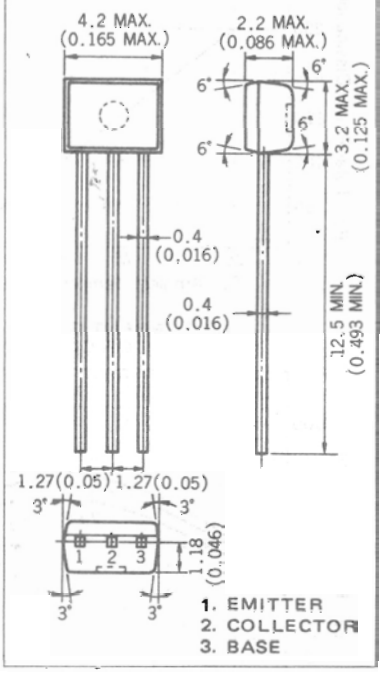
FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 47 kΩ
R_2 = 22 kΩ

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

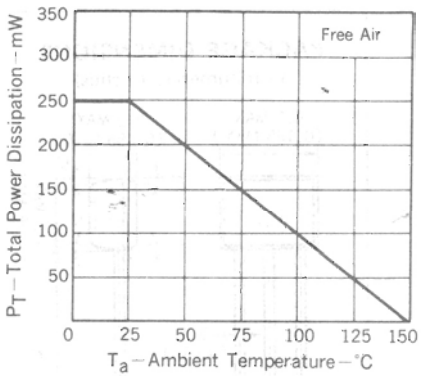
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −15 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

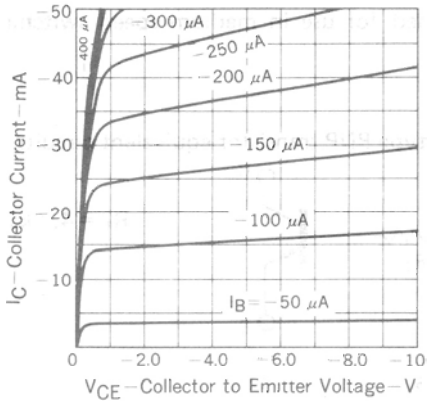
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	32.9	47.0	61.1	kΩ	
R_2	Input Resistance	15.4	22.0	28.6	kΩ	
V_{IH}	Hi Level Input Voltage	−0.9	−1.83	−3.0	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.5	−3.0	−6.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.5	1.0	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		0.6	3.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		0.9	5.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	60	95	195	–	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	90	185		–	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

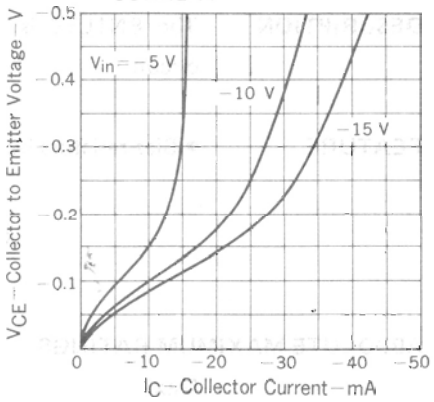
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



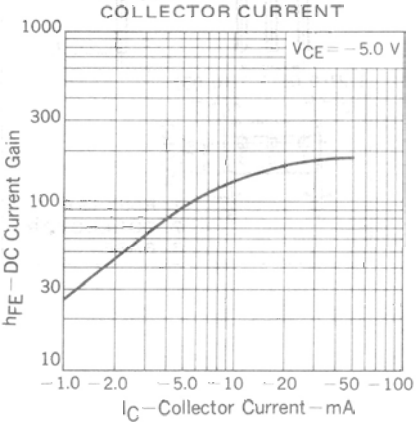
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



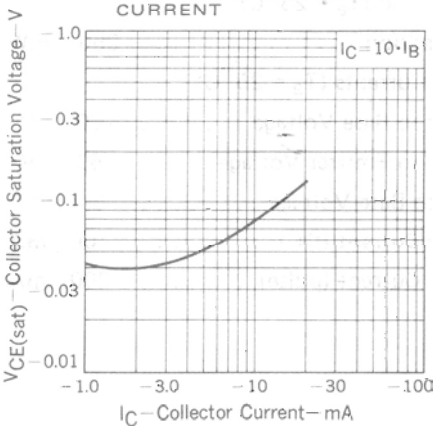
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



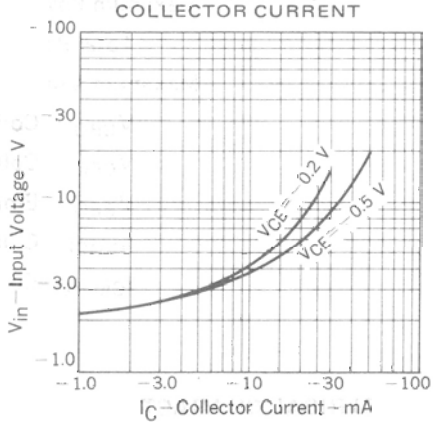
DC CURRENT GAIN vs. COLLECTOR CURRENT



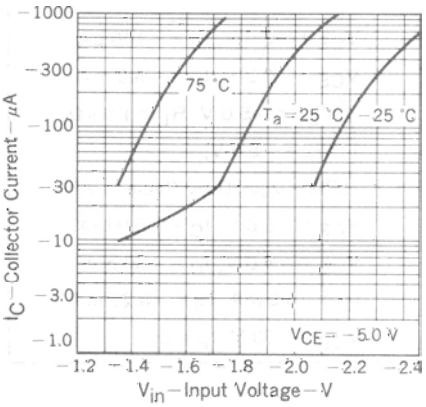
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



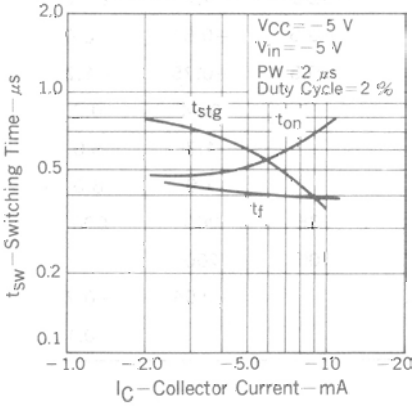
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



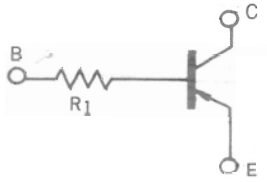
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
BN1L3Z

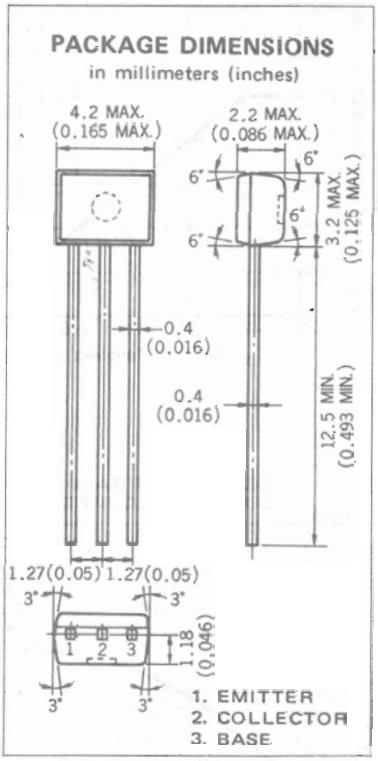
DESCRIPTION The BN1L3Z is designed for use in medium speed switching circuit.

FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



R_1 = 4.7 kΩ



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 250 mW

Maximum Voltages and Currents (T_a = 25 °C)

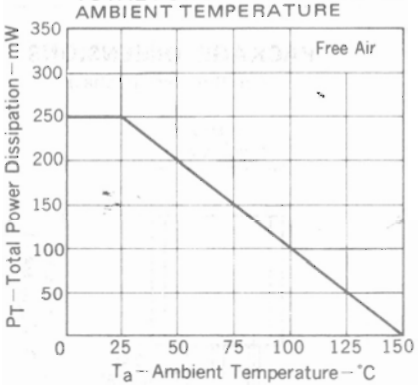
- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

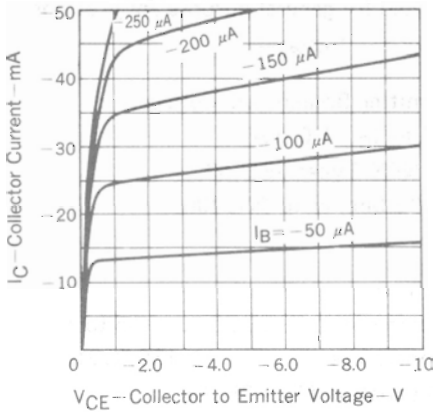
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	3.29	4.7	6.11	kΩ	
V_{IH}	Hi Level Input Voltage	−0.5	−0.57	−0.6	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−0.5	−0.75	−1.2	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn On Time		0.04	0.2	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ,
t_{stg}	Storage Time		1.7	5.0	μs	V_{in} = −5.0 V,
t_{off}	Turn Off Time		1.9	6.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	135	260	600	−	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	100	200		−	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.04	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

TYPICAL CHARACTERISTICS (T_a = 25 °C)

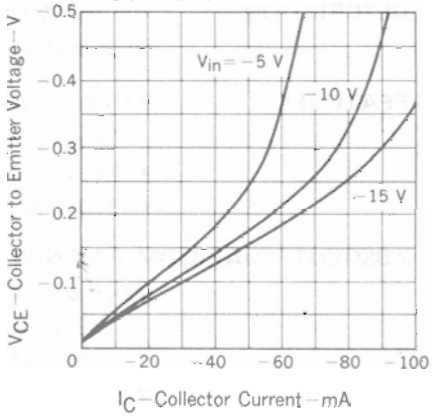
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



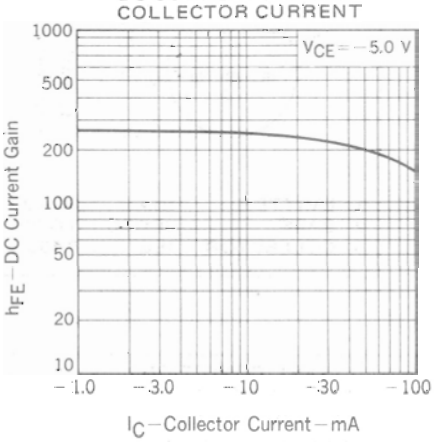
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



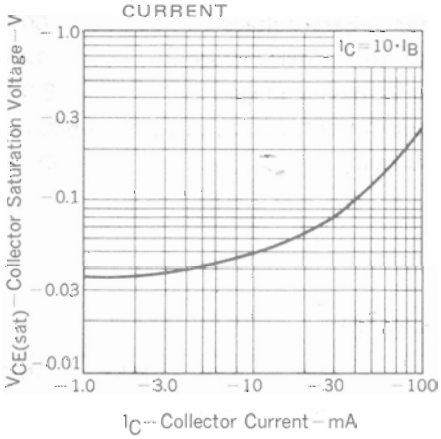
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



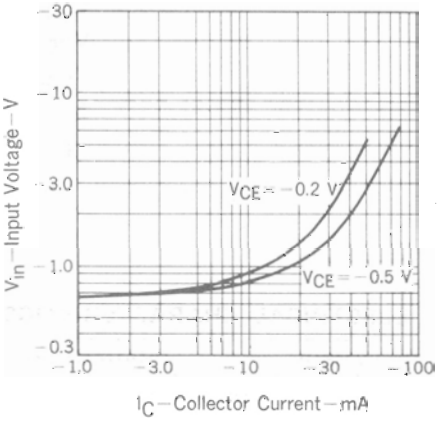
DC CURRENT GAIN vs. COLLECTOR CURRENT



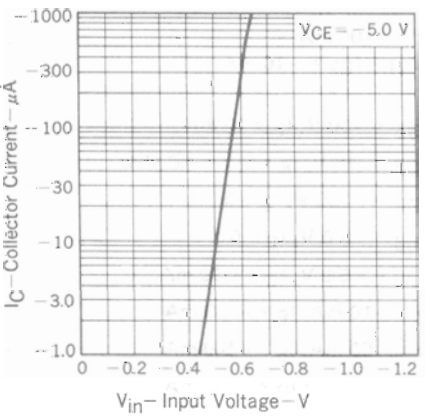
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



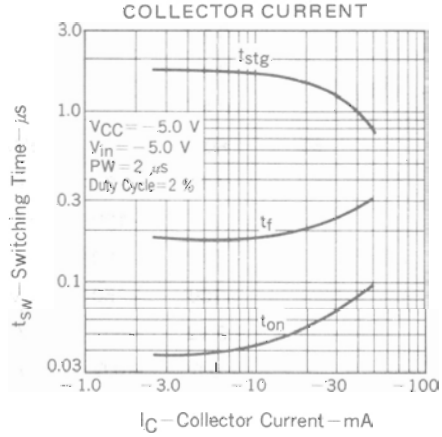
INPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. INPUT VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
JE5400

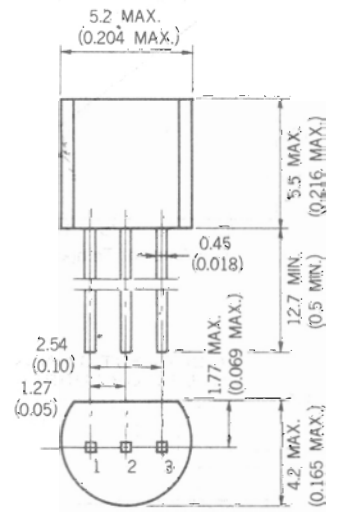
DESCRIPTION

The JE5400 is designed for general purpose applications requiring high Breakdown Voltages.

FEATURES

- High Collector-Emitter Breakdown Voltage.
  $V_{CEO} > -140$ V (@ $I_C = 1.0$ mA)
- Complements to NPN Types JE5550.
- JE5400 Electrically Similar to 2N5400.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_a = 25$ °C)
- Total Power Dissipation . . . . . 350 mW

Maximum Voltages and Currents ($T_a = 25$ °C)
- V_{CBO} Collector to Base Voltage . . . . . −160 V
- V_{CEO} Collector to Emitter Voltage . . . . . −140 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current. . . . . −600 mA
- I_B Base Current . . . . . −300 mA

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	40	180		–	$V_{CE} = -5.0$ V, $I_C = -1.0$ mA
h_{FE2}	DC Current Gain	50	200	400	–	$V_{CE} = -5.0$ V, $I_C = -10$ mA
h_{FE3}	DC Current Gain	20	70		–	$V_{CE} = -5.0$ V, $I_C = -50$ mA
t_{on}	Turn-on Time		0.1		μs	$I_C = -100$ mA, $-I_{B1} = I_{B2} = -10$ mA
t_{off}	Turn-off Time		0.2		μs	
t_{stg}	Storage Time		0.1		μs	
f_T	Gain Bandwidth Product	50	80		MHz	$V_{CE} = -10$ V, $I_E = 10$ mA
C_{ob}	Output Capacitance		2.5	5.0	pF	$V_{CB} = -10$ V, $I_E = 0$, $f = 1.0$ MHz
I_{CBO}	Collector Cutoff Current			−100	nA	$V_{CB} = -160$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			−100	nA	$V_{EB} = -6.0$ V, $I_C = 0$
V_{BE}	Base to Emitter Voltage		−700	−750	mV	$V_{CE} = -5.0$ V, $I_C = -10$ mA
$V_{CE(sat)1}$	Collector Saturation Voltage		−0.12	−0.4	V	$I_C = -10$ mA, $I_B = -1.0$ mA
$V_{CE(sat)2}$	Collector Saturation Voltage		−0.5	−0.8	V	$I_C = -50$ mA, $I_B = -5.0$ mA
$V_{BE(sat)1}$	Base Saturation Voltage		−0.75	−1.0	V	$I_C = -10$ mA, $I_B = -1.0$ mA
$V_{BE(sat)2}$	Base Saturation Voltage		−0.8	−1.0	V	$I_C = -50$ mA, $I_B = -5.0$ mA

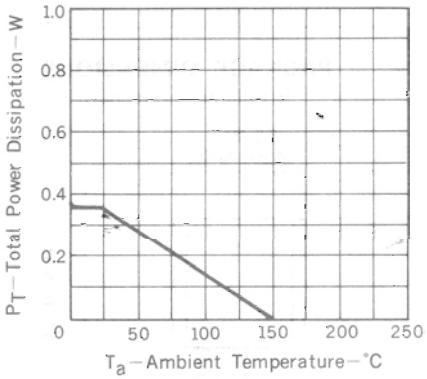
Classification of h_{FE2}

Rank	A	B	C
Range	50 – 150	100 – 300	200 – 400

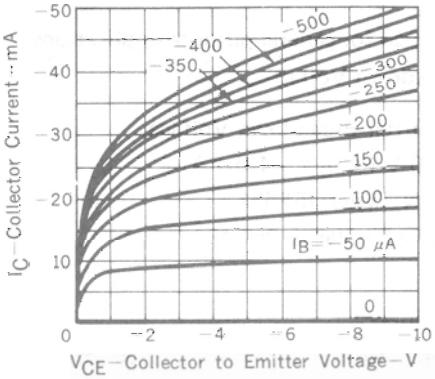
Test Conditions : $V_{CE} = -5.0$ V, $I_C = -10$ mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

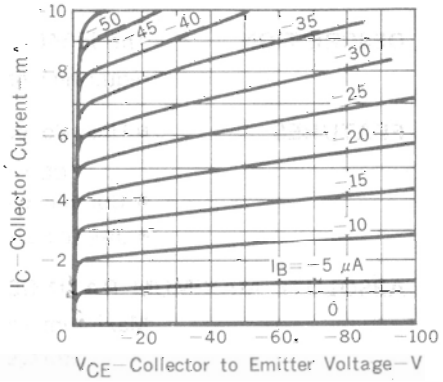
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



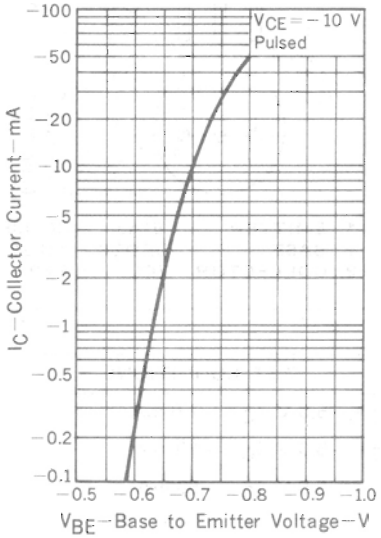
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



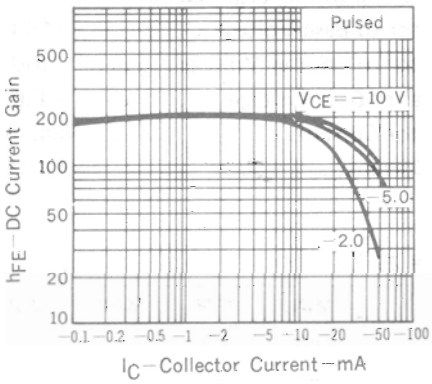
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



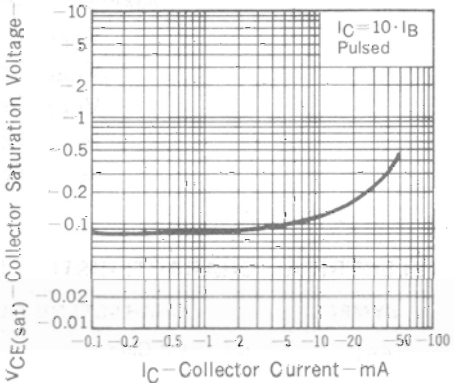
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



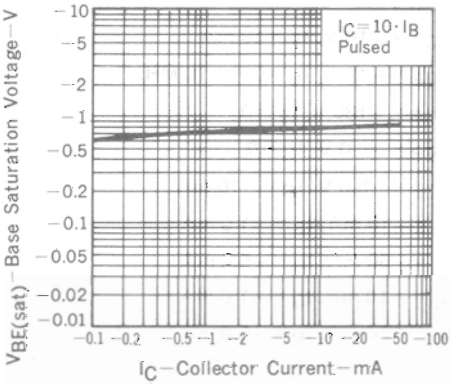
DC CURRENT GAIN vs. COLLECTOR CURRENT



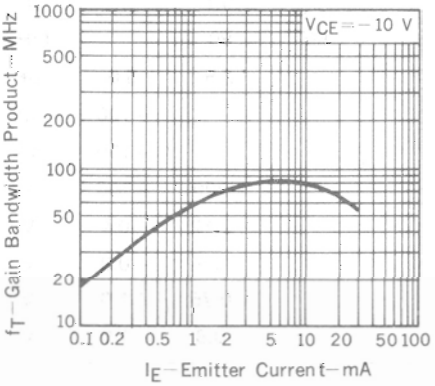
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



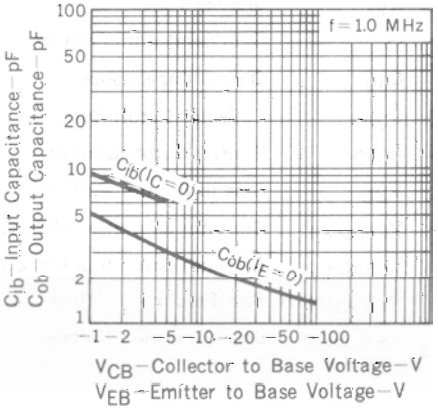
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

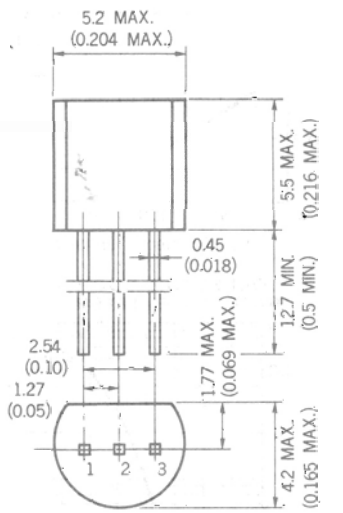
PNP SILICON TRANSISTOR
JE5401

DESCRIPTION The JE5401 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Collector-Emitter Breakdown Voltage.
  $V_{CEO} > -160$ V (@ $I_C = -1.0$ mA)
- Complements NPN Types JE5551.
- JE5401 Electrically Similar to 2N5401

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 350 mW

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −180 V
- V_{CEO} Collector to Emitter Voltage . . . . . −160 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current. . . . . −600 mA
- I_B Base Current. . . . . −300 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	40	180		–	V_{CE} = −5.0 V, I_C = −1.0 mA
h_{FE2}	DC Current Gain	50	200	400	–	V_{CE} = −5.0 V, I_C = −10 mA
h_{FE3}	DC Current Gain	20	70		–	V_{CE} = −5.0 V, I_C = −50 mA
t_{on}	Turn-on Time		0.1		μs	I_C = −100 mA $-I_{B1} = I_{B2}$ = −10 mA
t_{off}	Turn-off Time		0.2		μs	
t_{stg}	Storage Time		0.1		μs	
f_T	Gain Bandwidth Product	50	80		MHz	V_{CE} = −10 V, I_E = 10 mA
C_{ob}	Output Capacitance		2.5	5.0	pF	V_{CB} = −10 V, I_E = 0, f = 10 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −180 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage		−700	−750	mV	V_{CE} = −5.0 V, I_C = −10 mA
$V_{CE(sat)1}$	Collector Saturation Voltage		−0.12	−0.4	V	I_C = −10 mA, I_B = −1.0 mA
$V_{CE(sat)2}$	Collector Saturation Voltage		−0.5	−0.8	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)1}$	Base Saturation Voltage		−0.75	−1.0	V	I_C = −10 mA, I_B = −1.0 mA
$V_{BE(sat)2}$	Base Saturation Voltage		−0.8	−1.0	V	I_C = −50 mA, I_B = −5.0 mA

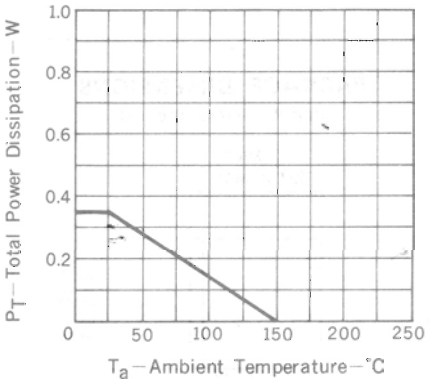
Classification of h_{FE2}

Rank	A	B	C
Range	50 – 150	100 – 300	200 – 400

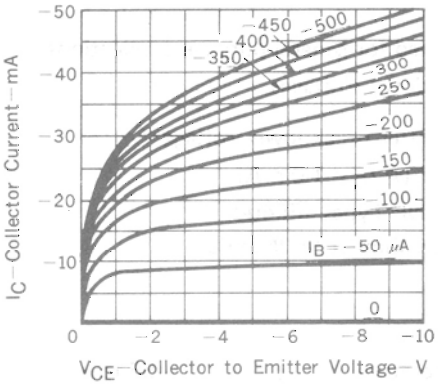
Test Conditions : V_{CE} = −5.0 V, I_C = −10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

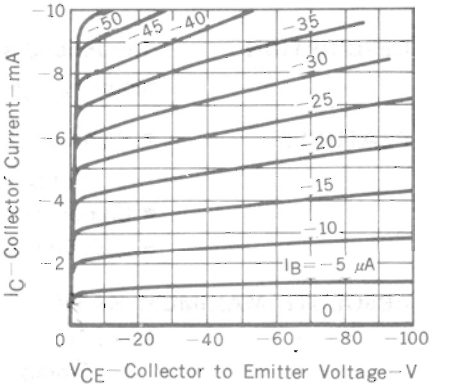
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



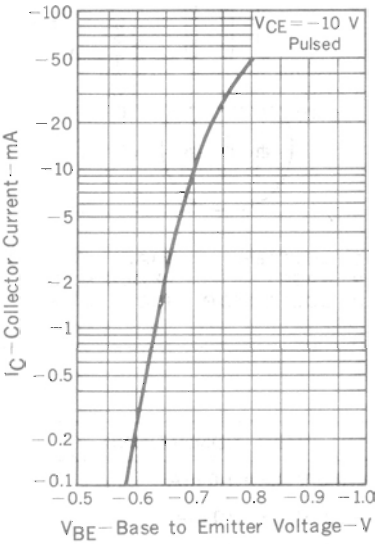
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



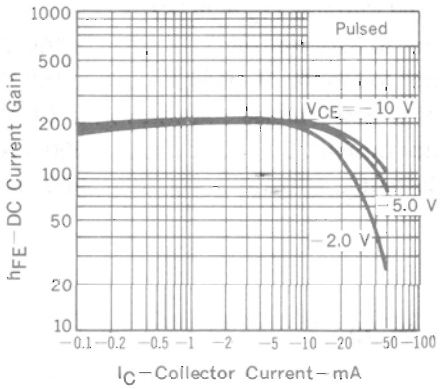
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



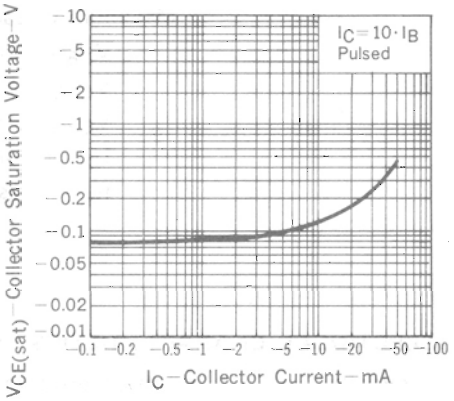
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



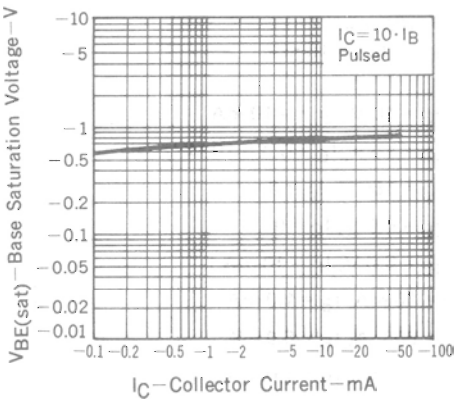
DC CURRENT GAIN vs. COLLECTOR CURRENT



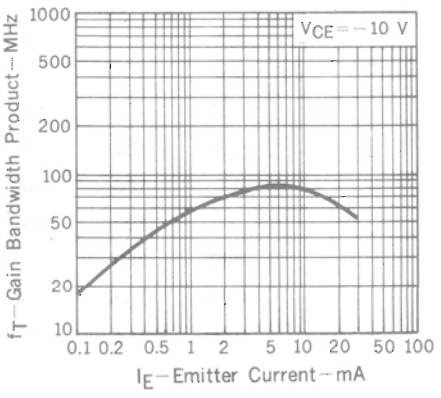
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



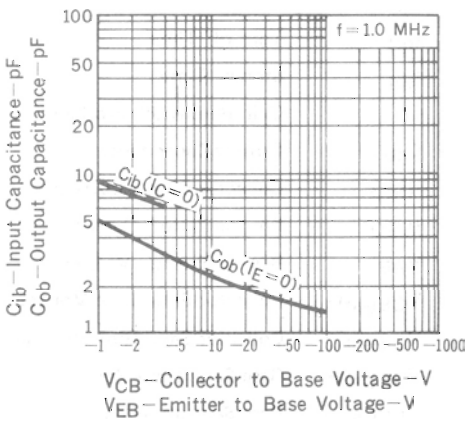
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

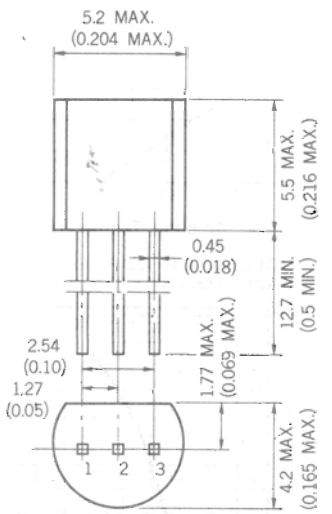
NPN SILICON TRANSISTOR
JE5550

DESCRIPTION The JE5550 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Collector-Emitter Breakdown Voltage.
  $V_{CEO} > 140$ V (@ $I_C = 1.0$ mA)
- Complements to PNP Types JE5400.
- JE5550 Electrically Similar to 2N5550.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_a = 25$ °C)
- Total Power Dissipation . . . . . 350 mW

Maximum Voltages and Currents ($T_a = 25$ °C)
- V_{CBO} Collector to Base Voltage . . . . . 160 V
- V_{CEO} Collector to Emitter Voltage . . . . . 140 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current. . . . . 600 mA
- I_B Base Current. . . . . 300 mA

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	40	190		—	$V_{CE} = 5.0$ V, $I_C = 1.0$ mA
h_{FE2}	DC Current Gain	50	200	400	—	$V_{CE} = 5.0$ V, $I_C = 10$ mA
h_{FE3}	DC Current Gain	20	160		—	$V_{CE} = 5.0$ V, $I_C = 50$ mA
t_{on}	Turn-on Time		0.3		μs	$I_C = 100$ mA $I_{B1} = -I_{B2} = 10$ mA
t_{off}	Turn-off Time		0.4		μs	
t_{stg}	Storage Time		0.2		μs	
f_T	Gain Bandwidth Product	50	110		MHz	$V_{CE} = 10$ V, $I_E = -10$ mA
C_{ob}	Output Capacitance		2.2	5.0	pF	$V_{CB} = 10$ V, $I_E = 0$, f = 10 MHz
I_{CBO}	Collector Cutoff Current			100	nA	$V_{CB} = 160$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			100	nA	$V_{EB} = 6.0$ V, $I_C = 0$
V_{BE}	Base to Emitter Voltage		680	750	mV	$V_{CE} = 5.0$ V, $I_C = 10$ mA
$V_{CE(sat)1}$	Collector Saturation Voltage		0.06	0.15	V	$I_C = 10$ mA, $I_B = 1.0$ mA
$V_{CE(sat)2}$	Collector Saturation Voltage		0.09	0.3	V	$I_C = 50$ mA, $I_B = 5.0$ mA
$V_{BE(sat)1}$	Base Saturation Voltage		0.7	1.0	V	$I_C = 10$ mA, $I_B = 1.0$ mA
$V_{BE(sat)2}$	Base Saturation Voltage		0.8	1.0	V	$I_C = 50$ mA, $I_B = 5.0$ mA

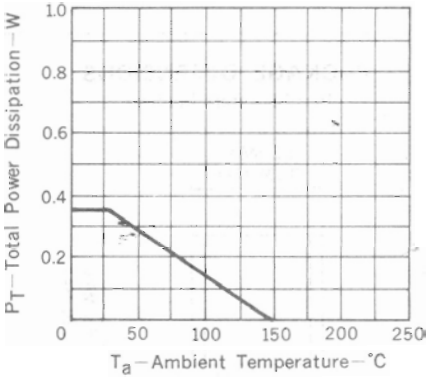
Classification of h_{FE2}

Rank	A	B	C
Range	50 – 150	100 – 300	200 – 400

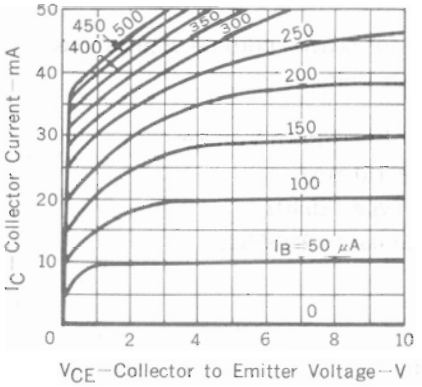
Test Conditions : $V_{CE} = 5.0$ V, $I_C = 10$ mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

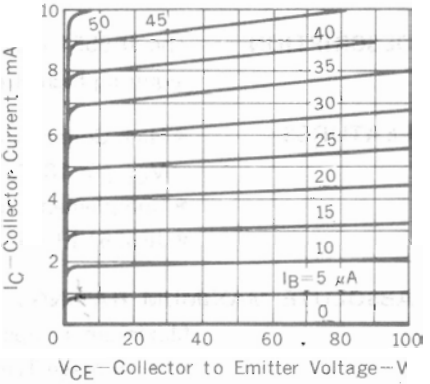
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



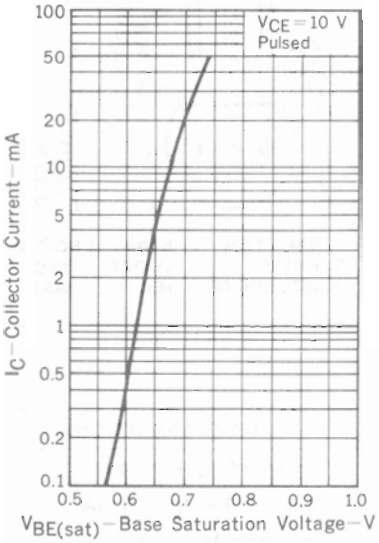
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



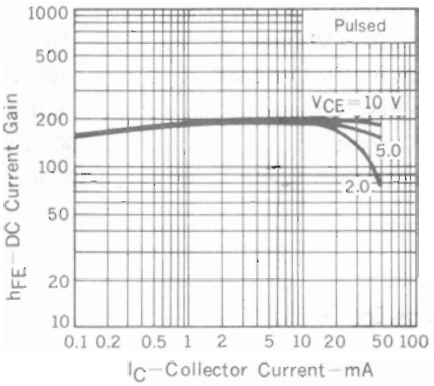
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



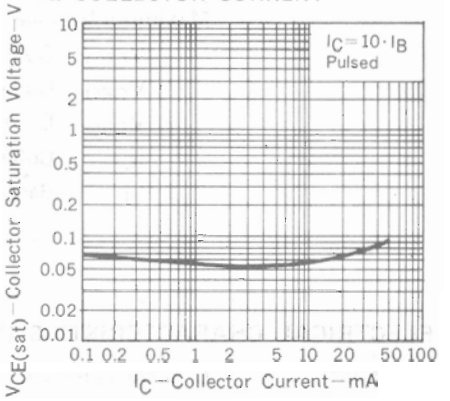
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



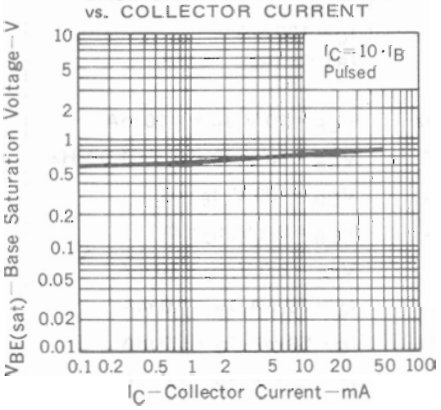
DC CURRENT GAIN vs. COLLECTOR CURRENT



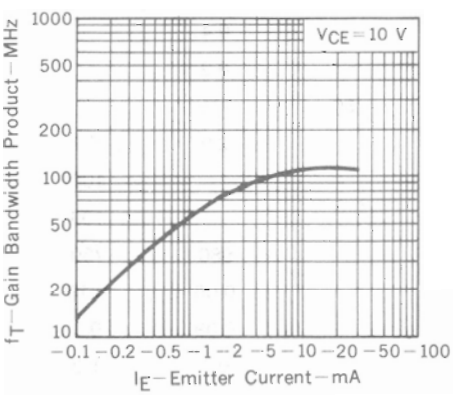
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



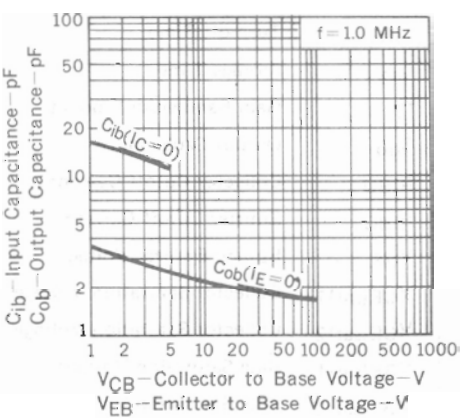
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

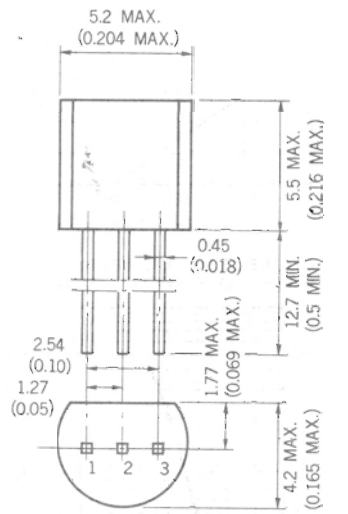
NPN SILICON TRANSISTOR
JE5551

DESCRIPTION The JE5551 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Collector-Emitter Breakdown Voltage. $V_{CEO} > 160$ V (@ I_C = 1.0 mA)
- Complements to PNP Type JE5401.
- JE5551 Electrically Similar to 2N5551.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 350 mW

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 180 V
- V_{CEO} Collector to Emitter Voltage . . . . . 160 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current . . . . . 600 mA
- I_B Base Current . . . . . 300 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	40	190		—	V_{CE} = 5.0 V, I_C = 1.0 mA
h_{FE2}	DC Current Gain	50	200	400	—	V_{CE} = 5.0 V, I_C = 10 mA
h_{FE3}	DC Current Gain	20	160		—	V_{CE} = 5.0 V, I_C = 50 mA
t_{on}	Turn-on Time		0.3		μs	I_C = 100 mA, $I_{B1} = -I_{B2}$ = 10 mA
t_{off}	Turn-off Time		0.4		μs	
t_{stg}	Storage Time		0.2		μs	
f_T	Gain Bandwidth Product	50	110		MHz	V_{CE} = 10 V, I_E = −10 mA
C_{ob}	Output Capacitance		2.2	5.0	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 180 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage		680	750	mV	V_{CE} = 5.0 V, I_C = 10 mA
$V_{CE(sat)1}$	Collector Saturation Voltage		0.06	0.15	V	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)2}$	Collector Saturation Voltage		0.09	0.3	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)1}$	Base Saturation Voltage		0.7	1.0	V	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)2}$	Base Saturation Voltage		0.8	1.0	V	I_C = 50 mA, I_B = 5.0 mA

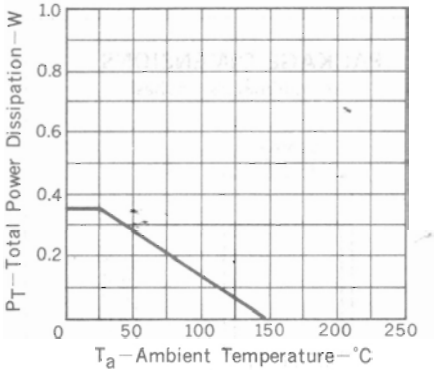
Classification of h_{FE2}

Rank	A	B	C
Range	50 – 150	100 – 300	200 – 400

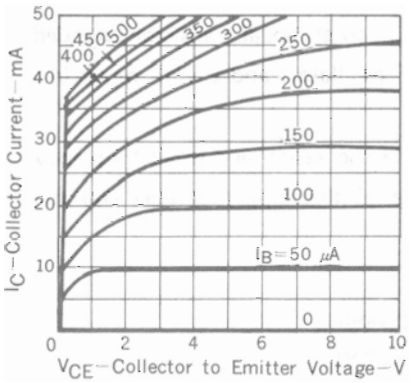
Test Conditions : V_{CE}=5.0 V, I_C=10 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

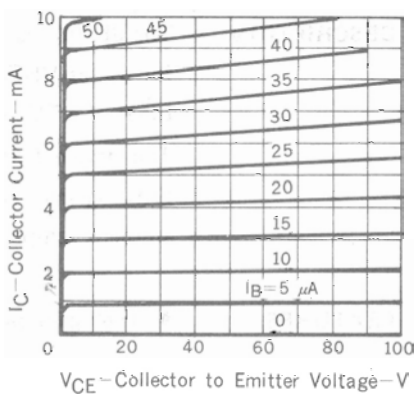
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



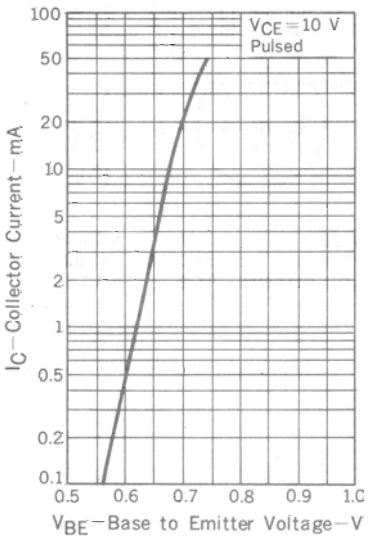
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



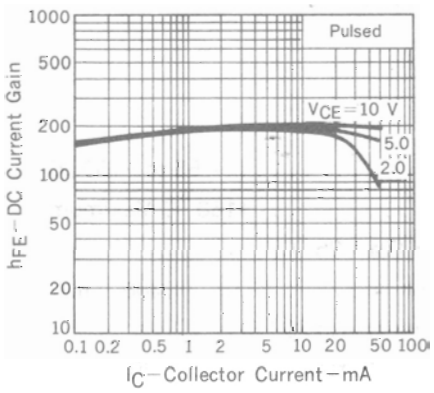
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



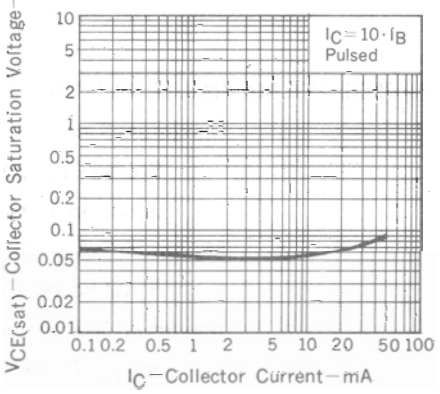
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



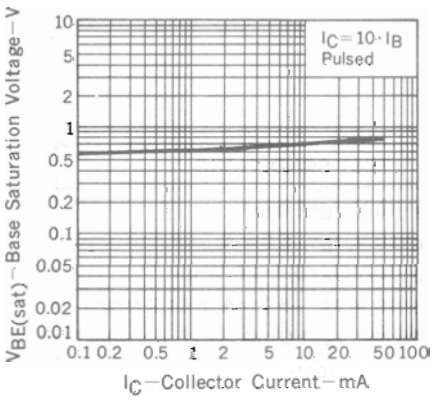
DC CURRENT GAIN vs. COLLECTOR CURRENT



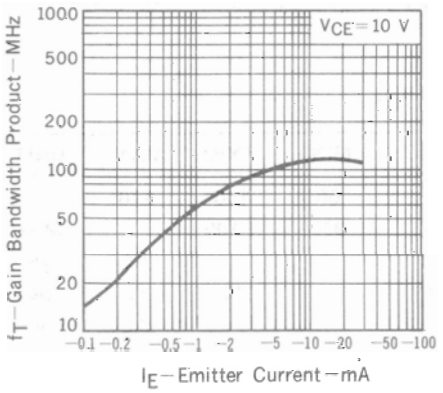
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



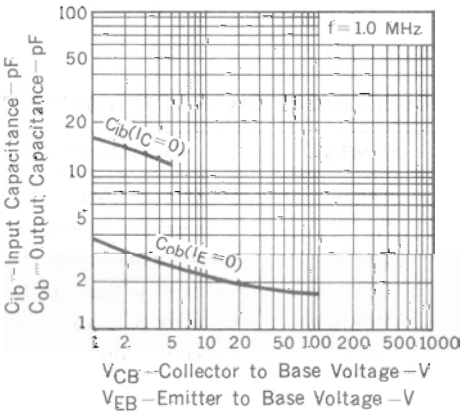
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE7001

DESCRIPTION

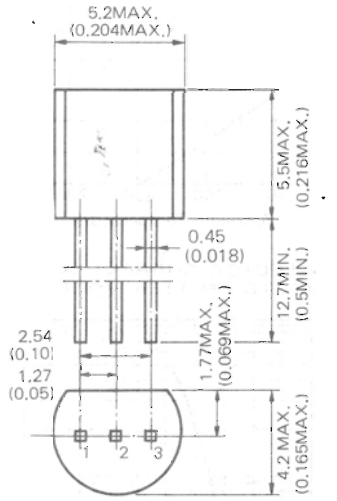
The JE7001 is an NPN silicon epitaxial transistor intended for use as VHF and UHF oscillators and a VHF mixer in a tuner of a TV receiver.

The device features stable oscillation and small frequency drift against any change of the supply voltage and the ambient temperature.

FEATURES

- High gain bandwidth product;
  f_T=1 100 MHz TYP.
- Low collector to base time constant;
  $C_c \cdot r_{b'b}$=10 ps TYP.
- Low output capacitance;
  C_{ob}=1.5 pF MAX.

PACKAGE DIMENSIONS
in millimeters (inches)



1. BASE
2. EMITTER
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 400 mW

Maximum Voltages and Currents (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . . 15 V
- V_{EBO} Emitter to Base Voltage . . . . . 4.0 V
- I_C Collector Current . . . . . 50 mA
- I_B Base Current. . . . . 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	100	270		V_{CE}=10 V, I_C=5.0 mA
f_T	Gain Bandwidth Product	800	1 100		MHz	V_{CE}=10 V, I_E=−5.0 mA
C_{ob}	Output Capacitance			1.5	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
$C_c \cdot r_{b'b}$	Collector to Base Time Constant		10	15	ps	V_{CE}=10 V, I_E=−5.0 mA, f=31.9 MHz
$V_{CE(sat)}$	Collector Saturation Voltage			0.5	V	I_C=10 mA, I_B=1.0 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB}=12 V, I_E=0

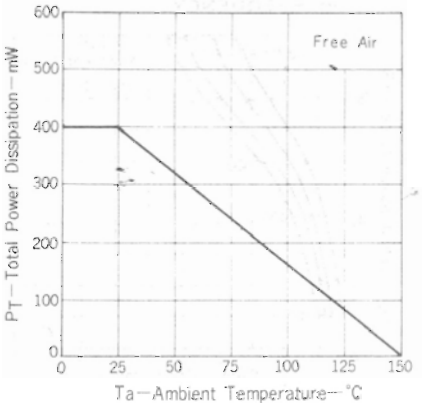
Classification of h_{FE}

Rank	L	K	J
Range	60 – 120	90 – 180	135 – 270

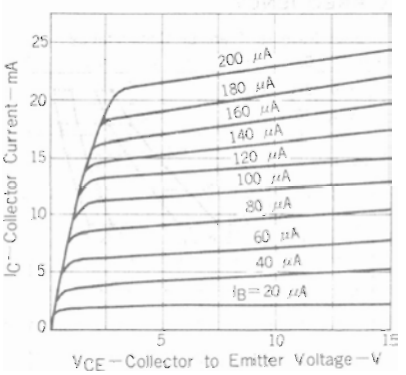
h_{FE} Test Conditions: V_{CE}=10 V, I_C=5.0 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

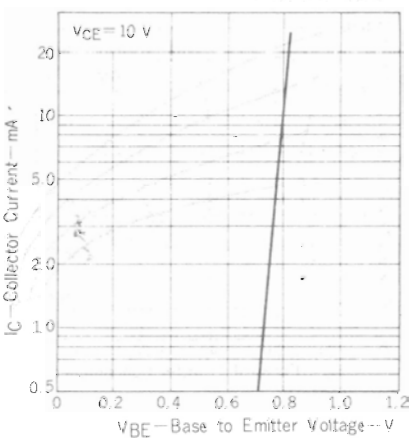
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



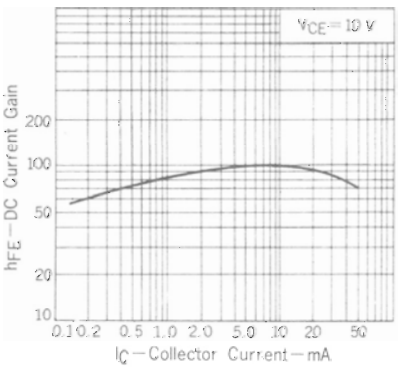
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



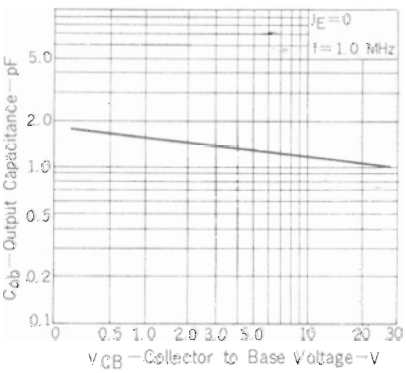
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT

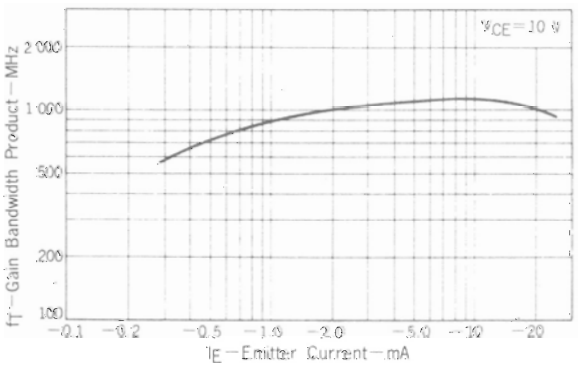


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

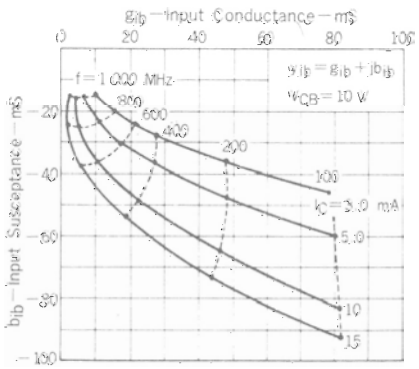


TYPICAL CHARACTERISTICS of "Y" PARAMETERS

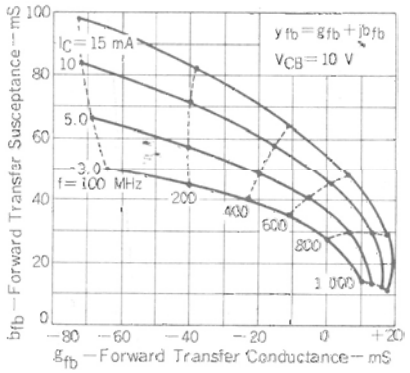
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



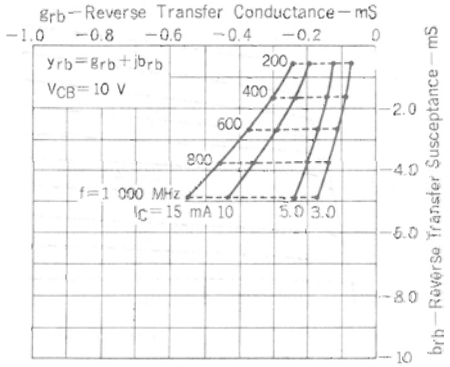
INPUT ADMITTANCE (y_{ib}) vs. FREQUENCY



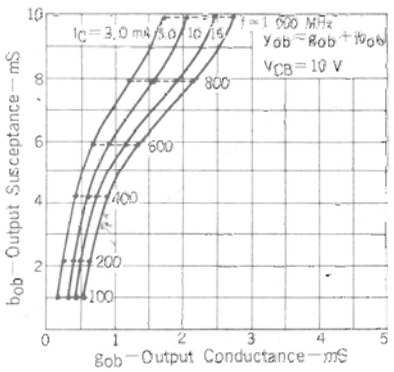
FORWARD TRANSFER ADMITTANCE (y_{fb}) vs. FREQUENCY



REVERSE TRANSFER ADMITTANCE (y_{rb}) vs. FREQUENCY



OUTPUT ADMITTANCE (y_{ob}) vs. FREQUENCY



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE8050

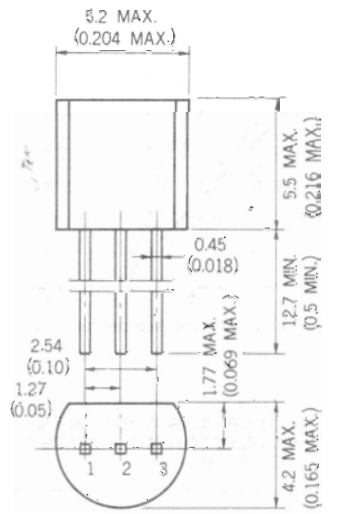
DESCRIPTION

The JE8050 is designed for use in 2 W output amplifier of portable radios in class B push-pull operation.

FEATURES

- High total power dissipation. (P_T : 2.0 W, T_C = 25 °C)
- High collector current. (I_C : 1.5 A)
- Complementary to JE8550.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation (Ta = 25 °C) . . . . . 1.0 W

Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

Total Power Dissipation (T_C = 25 °C) . . . . 2.0 W

Thermal Resistance (Ta = 25 °C)
(Junction to Ambient) . . . 156.25 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . 40 V

V_{CEO} Collector to Emitter Voltage . . . . . 25 V

V_{EBO} Emitter to Base Voltage . . . . . 6.0 V

I_C Collector Current . . . . . 1.5 A

I_B Base Current . . . . . 0.5 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	45	135		—	V_{CE}=1.0 V, I_C=5.0 mA
h_{FE2}	DC Current Gain	85	160	300	—	V_{CE}=1.0 V, I_C=100 mA
h_{FE3}	DC Current Gain	40	110		—	V_{CE}=1.0 V, I_C=800 mA
f_T	Gain Bandwidth Product	100	190		MHz	V_{CE}=10 V, I_C=50 mA
C_{ob}	Output Capacitance		9.0		pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=35 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=6.0 V, I_C=0
V_{BE}	Base to Emitter Voltage		0.66	1.0	V	V_{CE}=1.0 V, I_C=10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.28	0.5	V	I_C=800 mA, I_B=80 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.98	1.2	V	I_C=800 mA, I_B=80 mA
BV_{CBO}	Collector to Base Breakdown Voltage	40			V	I_C=0.1 mA, I_E=0
BV_{CEO}	Collector to Emitter Breakdown Voltage	25			V	I_C=2.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=0.1 mA, I_C=0

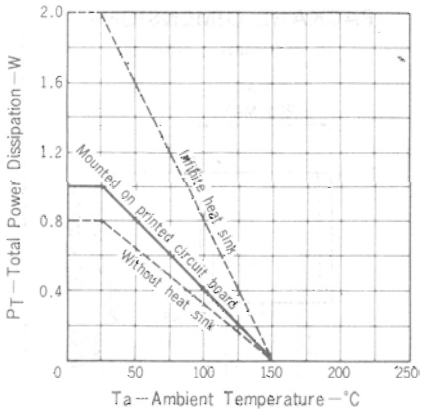
Classification of h_{FE2}

Rank	B	C	D
Range	85 – 160	120 – 200	160 – 300

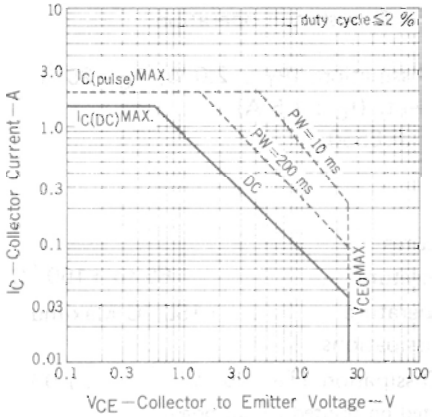
h_{FE} Test Conditions : V_{CE} = 1.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

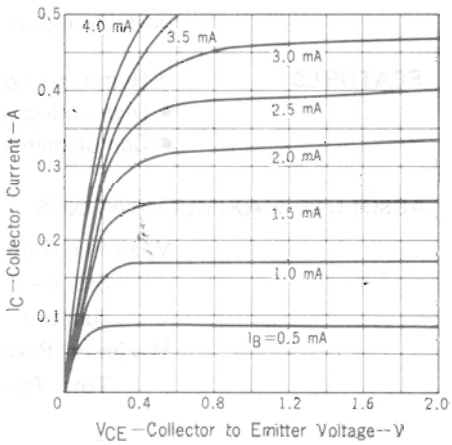
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



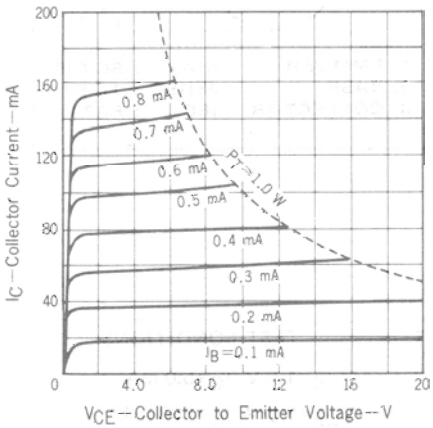
SAFE OPERATING AREA



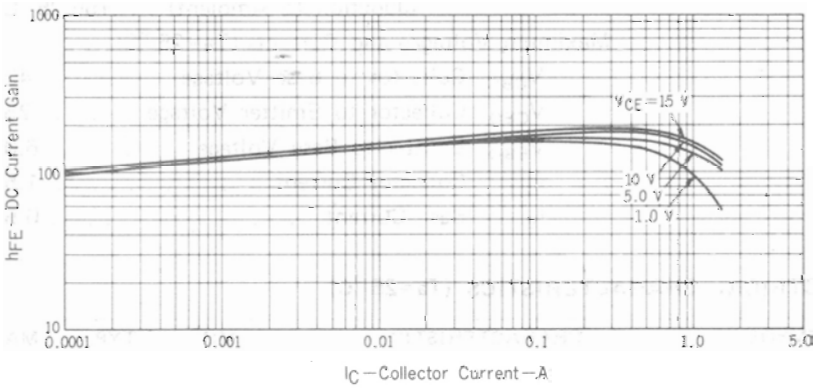
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



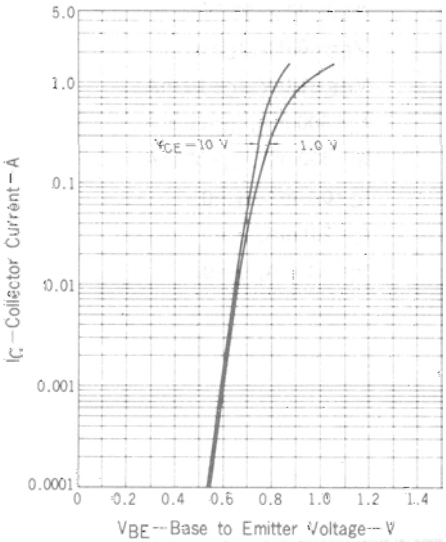
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



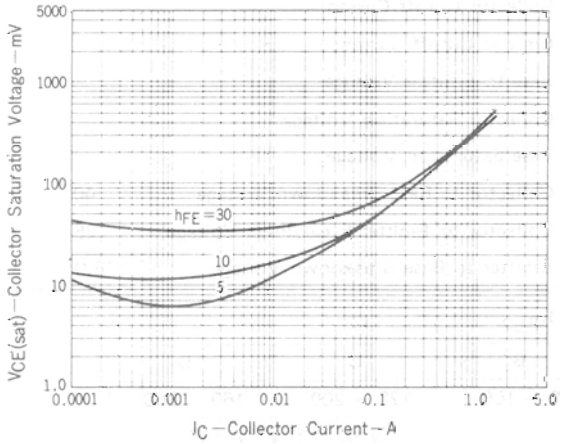
DC CURRENT GAIN vs. COLLECTOR CURRENT



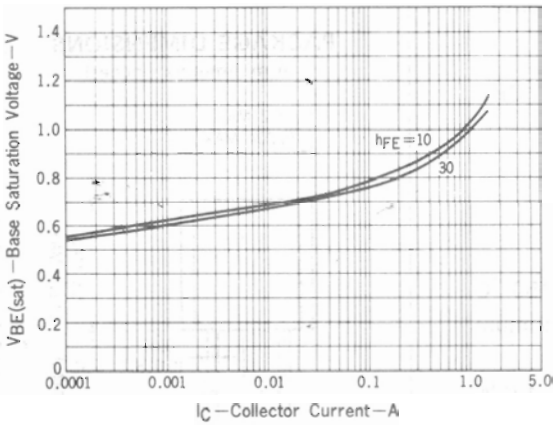
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



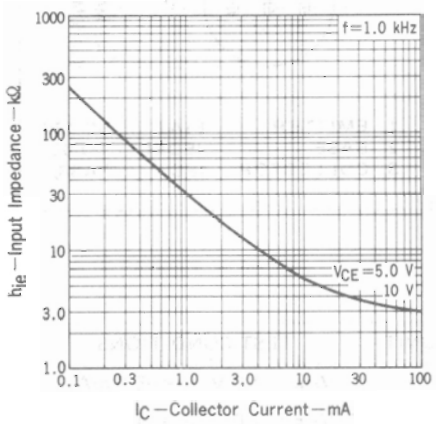
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



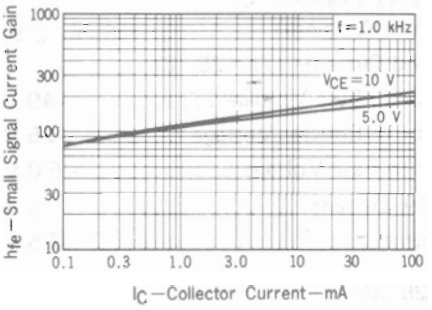
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



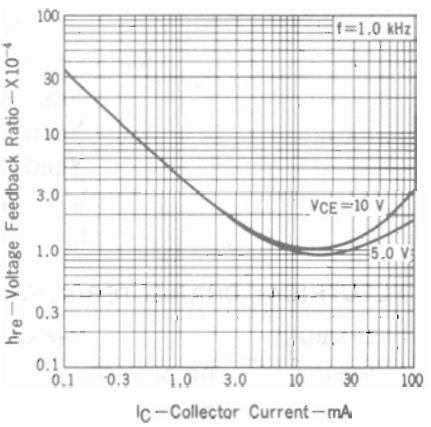
INPUT IMPEDANCE vs. COLLECTOR CURRENT



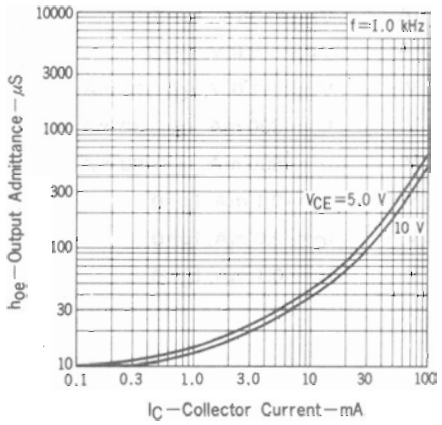
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



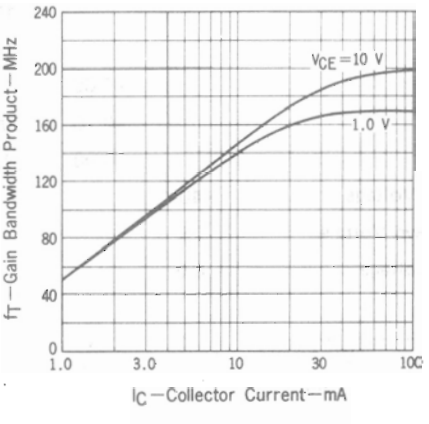
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



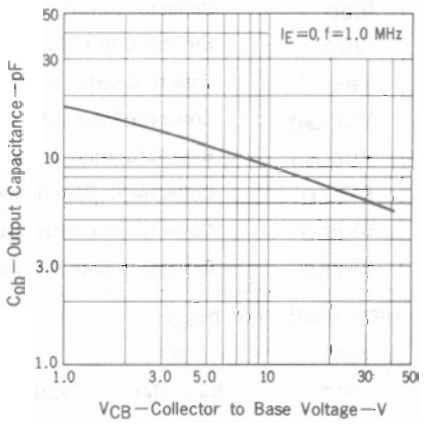
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

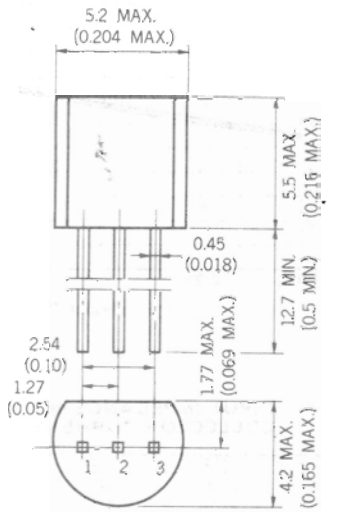
PNP SILICON TRANSISTOR
JE8550

DESCRIPTION The JE8550 is designed for use in 2 W output amplifier of portable radios in class B push-pull operation.

FEATURES

- High total power dissipation. (P_T : 2.0 W, T_C = 25 °C)
- High collector current. (I_C : −1.5 A)
- Complementary to JE8050.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −65 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation (Ta = 25 °C) ..... 1.0 W

Transistor mounted on printed circuit board, max. lead length 4 mm, mounting for collector lead min. 10 mm x 10 mm.

Total Power Dissipation (T_C = 25 °C) ..... 2.0 W

Thermal Resistance (Ta = 25 °C)

(Junction to Ambient) ..... 156.25 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage ..... −40 V

V_{CEO} Collector to Emitter Voltage ..... −25 V

V_{EBO} Emitter to Base Voltage ..... −6.0 V

I_C Collector Current ..... −1.5 A

I_B Base Current ..... −0.5 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	45	170		–	V_{CE}=−1.0 V, I_C=−5.0 mA
h_{FE2}	DC Current Gain	85	160	300	–	V_{CE}=−1.0 V, I_C=−100 mA
h_{FE3}	DC Current Gain	40	80		–	V_{CE}=−1.0 V, I_C=−800 mA
f_T	Gain Bandwidth Product	100	200		MHz	V_{CE}=−10 V, I_C=−50 mA
C_{ob}	Output Capacitance		15		pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB}=−35 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB}=−6.0 V, I_C=0
V_{BE}	Base to Emitter Voltage		−0.66	−1.0	V	V_{CE}=−1.0 V, I_C=−10 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.28	−0.5	V	I_C=−800 mA, I_B=−80 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.98	−1.2	V	I_C=−800 mA, I_B=−80 mA
BV_{CBO}	Collector to Base Breakdown Voltage	−40			V	I_C=−0.1 mA, I_E=0
BV_{CEO}	Collector to Emitter Breakdown Voltage	−25			V	I_C=−2.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−6.0			V	I_E=−0.1 mA, I_C=0

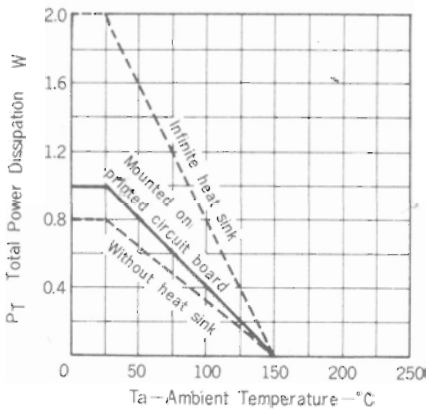
Classification of h_{FE2}

Rank	B	C	D
Range	85 – 160	120 – 200	160 – 300

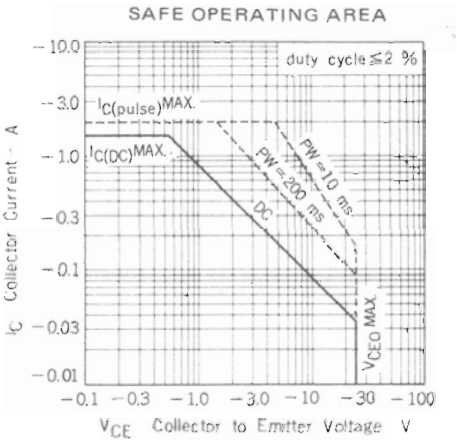
h_{FE} Test Conditions : V_{CE} = −1.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

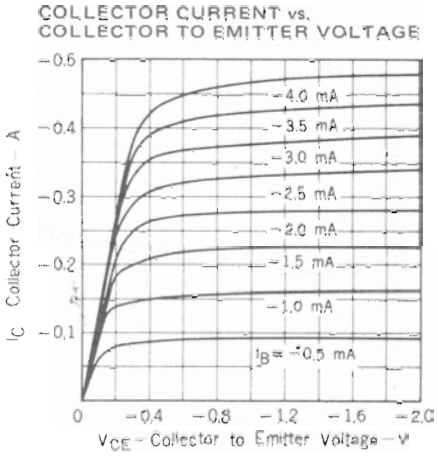
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



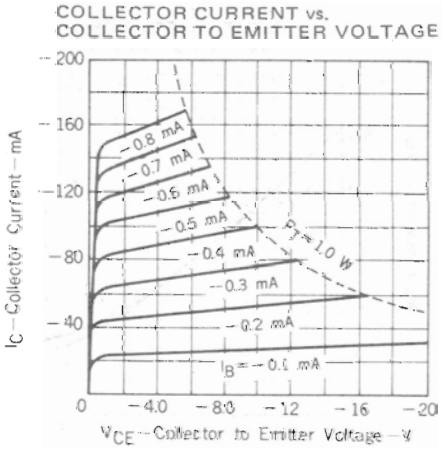
SAFE OPERATING AREA



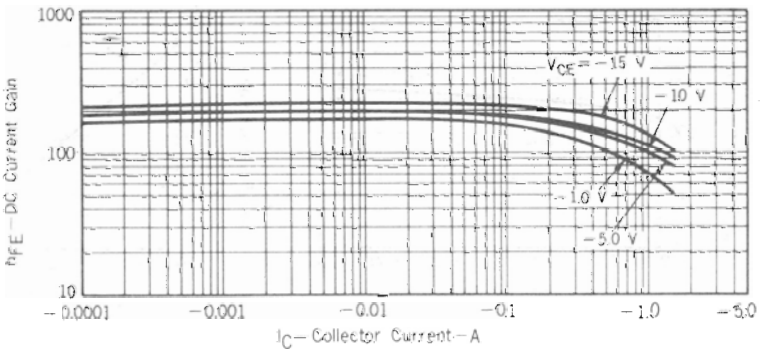
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



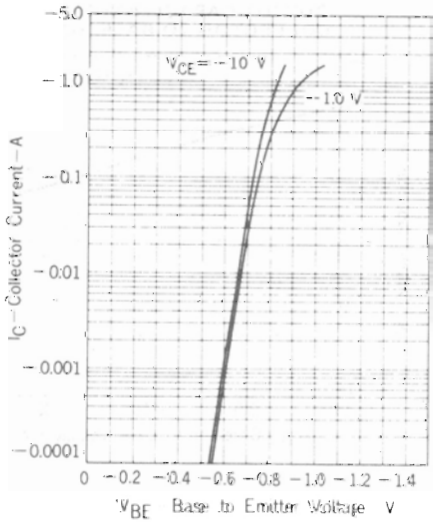
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



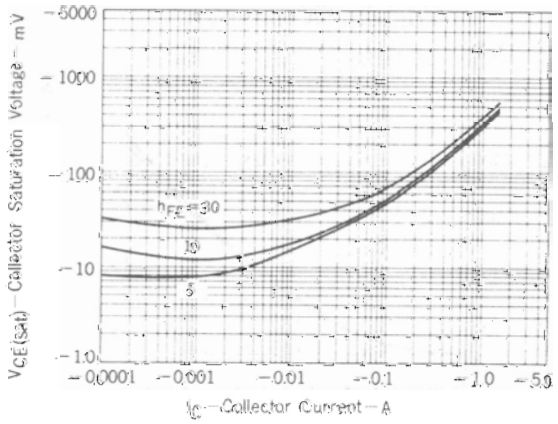
DC CURRENT GAIN vs. COLLECTOR CURRENT



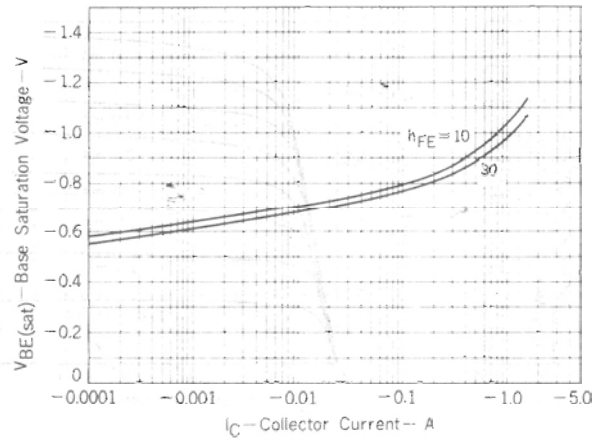
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



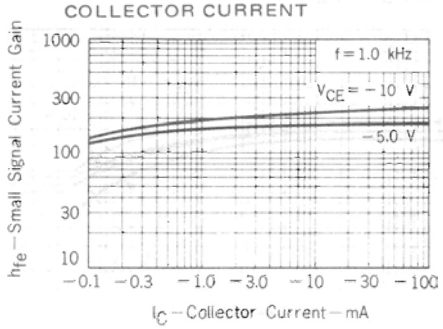
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



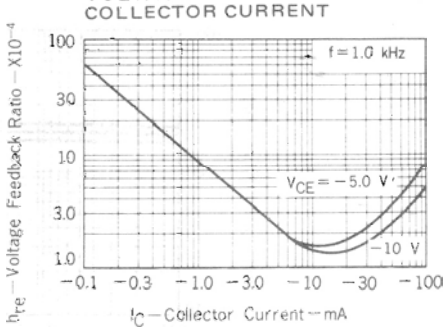
BASE SATURATION VOLTAGE vs.
COLLECTOR CURRENT



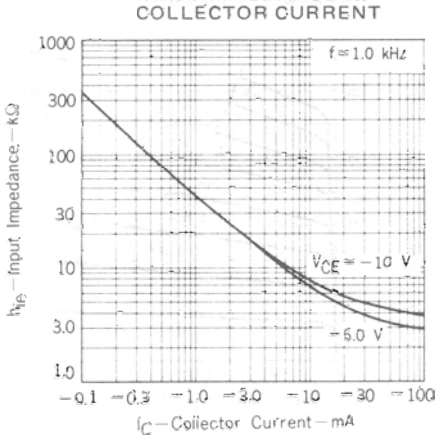
SMALL SIGNAL CURRENT GAIN vs.
COLLECTOR CURRENT



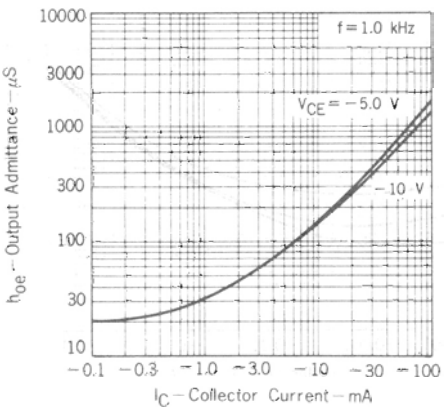
VOLTAGE FEEDBACK RATIO vs.
COLLECTOR CURRENT



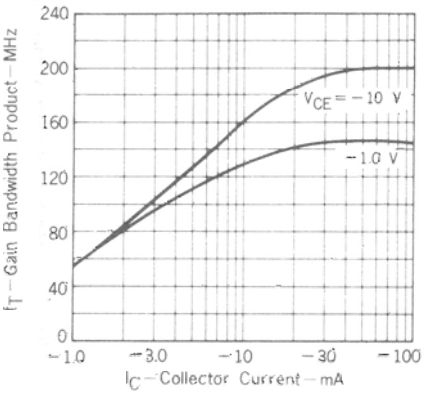
INPUT IMPEDANCE vs.
COLLECTOR CURRENT



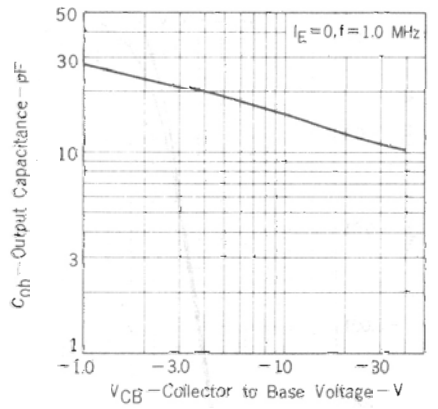
OUTPUT ADMITTANCE vs.
COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs.
COLLECTOR CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

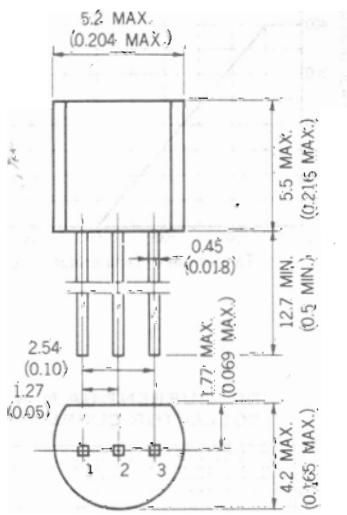
NPN SILICON TRANSISTOR
JE9011

DESCRIPTION The JE9011 is designed for use in AM converter, AM/FM IF amplifier and general purpose amplifier.

FEATURES

- High total power dissipation. (P_T : 400 mW)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation .....400 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... 50 V
- V_{CEO} Collector to Emitter Voltage ..... 30 V
- V_{EBO} Emitter to Base Voltage .....5.0 V
- I_C Collector Current.....30 mA
- I_B Base Current .....10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	28	90	198	—	V_{CE} = 5.0 V, I_C = 1.0 mA
C_{ob}	Output Capacitance		1.5		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
NF	Noise Figure		2.0	4.0	dB	V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 500 Ω, f = 1.0 MHz
f_T	Gain Bandwidth Product	150	370		MHz	V_{CE} = 5.0 V, I_C = 1.0 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	0.65	0.70	0.75	V	V_{CE} = 5.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.08	0.3	V	I_C = 10 mA, I_B = 1.0 mA
BV_{CBO}	Collector to Base Breakdown Voltage	50			V	I_C = 0.1 mA, I_E = 0
BV_{CEO}	Collector to Emitter Breakdown Voltage	30			V	I_C = 1.0 mA, I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E = 0.1 mA, I_C = 0

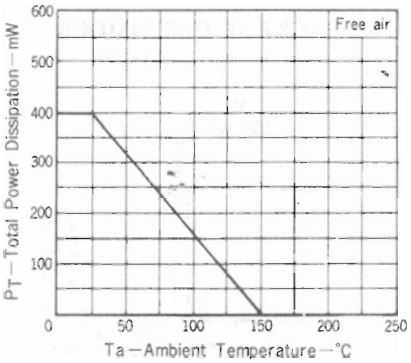
Classification of h_{FE}

Rank	D	E	F	G	H	I
Range	28 – 45	39 – 60	54 – 80	72 – 108	97 – 146	132 – 198

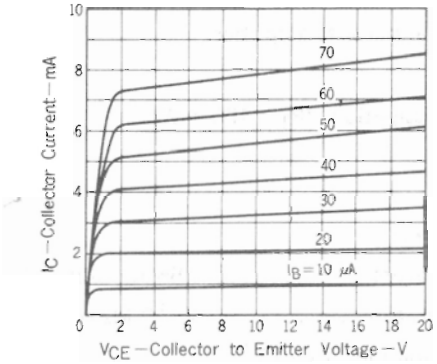
h_{FE} Test Conditions : V_{CE} = 5.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

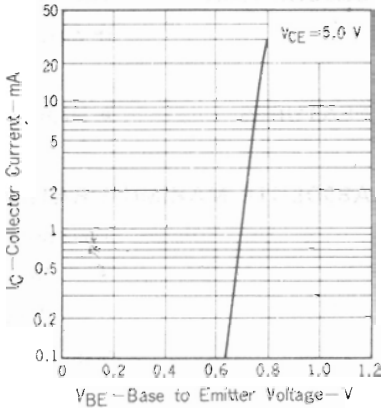
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



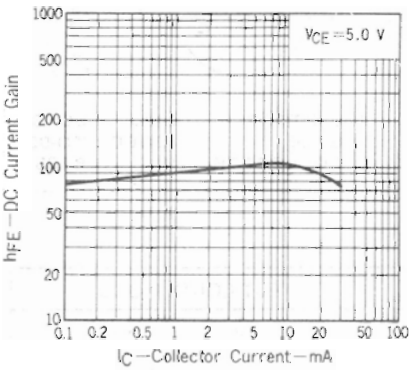
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



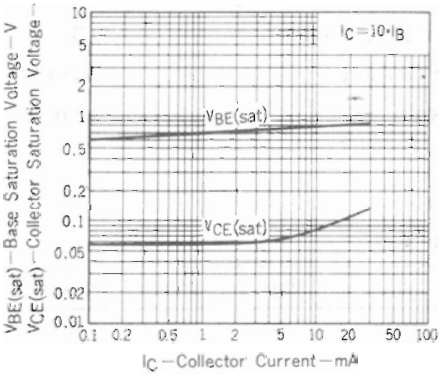
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



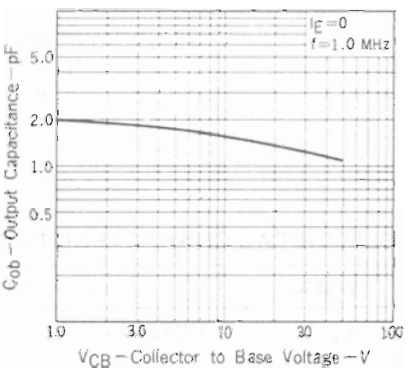
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

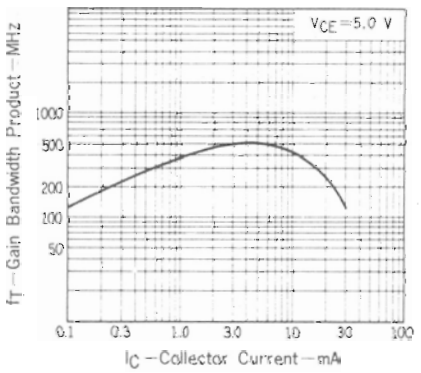


OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

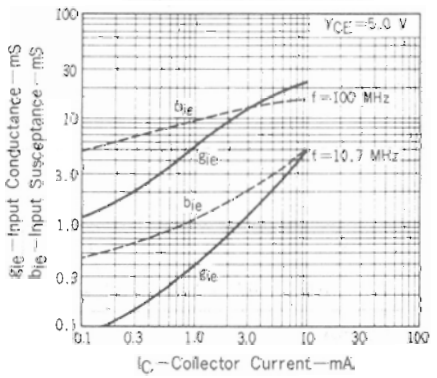


TYPICAL SMALL SIGNAL "y" PARAMETERS COMMON EMITTER

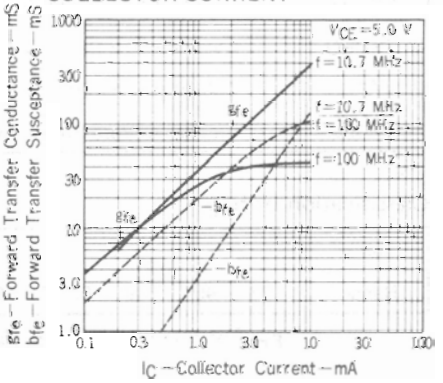
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



INPUT ADMITTANCE vs. COLLECTOR CURRENT

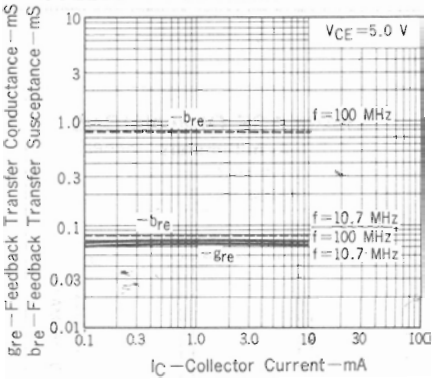


FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT

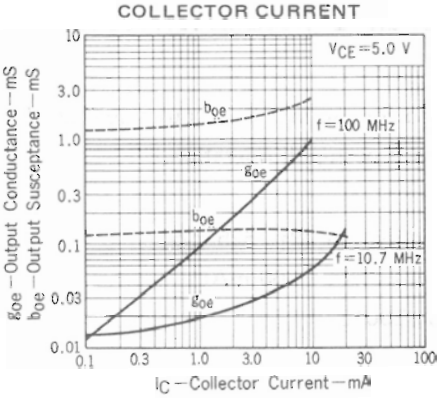


COMMON BASE

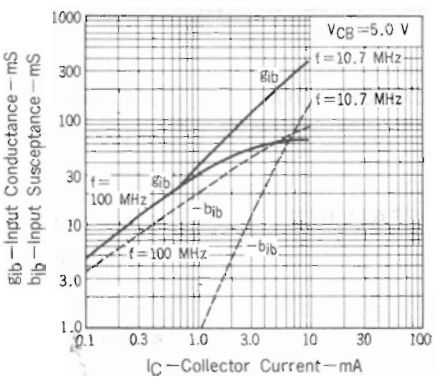
FEEDBACK TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



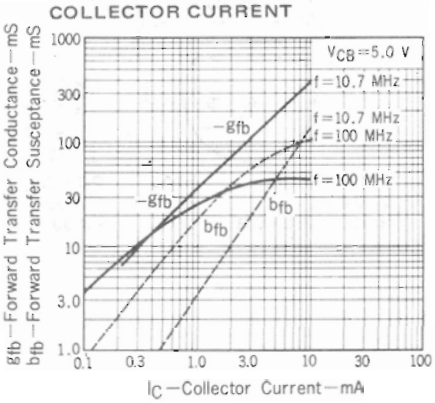
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



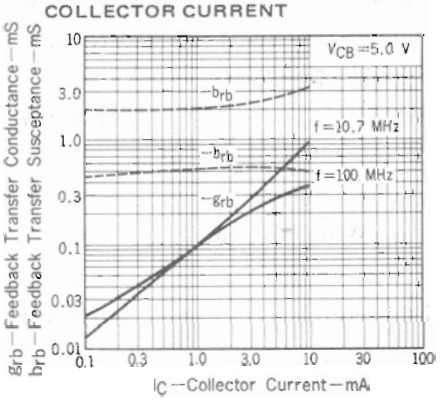
INPUT ADMITTANCE vs. COLLECTOR CURRENT



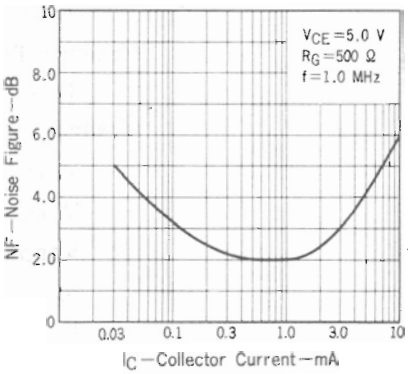
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



FEEDBACK TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



NOISE FIGURE vs. COLLECTOR CURRENT



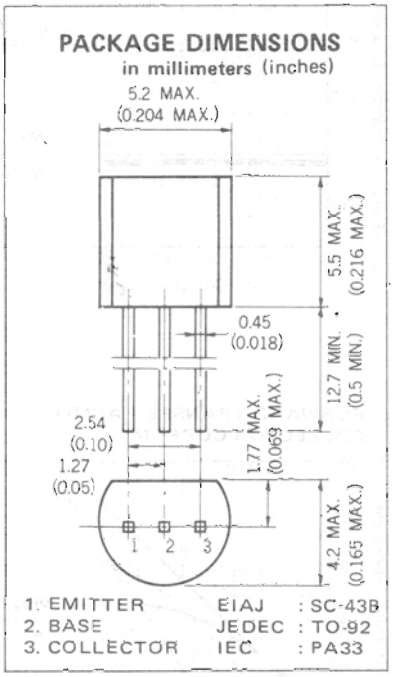
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
JE9012

DESCRIPTION The JE9012 is designed for use in 1 W output amplifier of portable radios in class B push-pull operation.

FEATURES

- High total power dissipation. (P_T: 625 mW)
- High collector current. (I_C : −500 mA)
- Complementary to JE9013.
- Excellent linearity.



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 625 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage ..... −40 V

V_{CEO} Collector to Emitter Voltage ..... −20 V

V_{EBO} Emitter to Base Voltage ..... −5.0 V

I_C Collector Current ..... −500 mA

I_B Base Current ..... −100 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	64	120	202	--	V_{CE} = −1.0 V, I_C = −50 mA
h_{FE2}	DC Current Gain	40	90		—	V_{CE} = −1.0 V, I_C = −500 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.60	V	I_C = −500 mA, I_B = −50 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.95	−1.20	V	I_C = −500 mA, I_B = −50 mA
V_{BE}	Base to Emitter Voltage	−0.60	−0.67	−0.70	V	V_{CE} = −1.0 V, I_C = −10 mA
BV_{CBO}	Collector to Base Breakdown Voltage	−40			V	I_C = −0.1 mA, I_E = 0
BV_{CEO}	Collector to Emitter Breakdown Voltage	−20			V	I_C = −1.0 mA, I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E = −0.1 mA, I_C = 0
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −25 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −3.0 V, I_C = 0

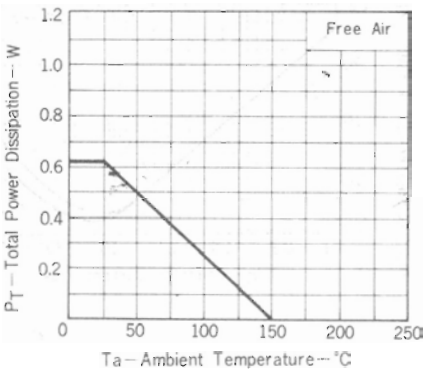
Classification of h_{FE1}

Rank	D	E	F	G	H
Range	64–91	78–112	96–135	112–166	144–202

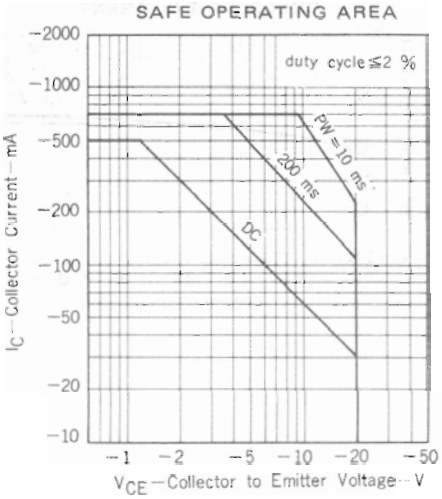
h_{FE} Test Conditions : V_{CE} = −1.0 V, I_C = −50 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

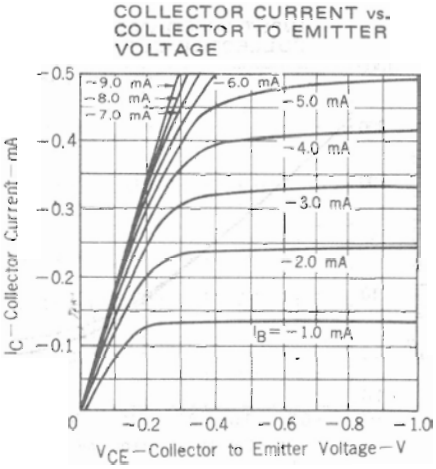
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



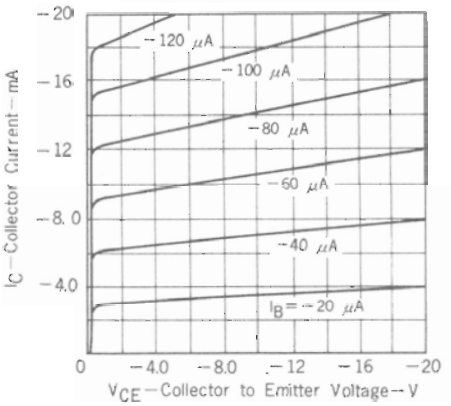
SAFE OPERATING AREA



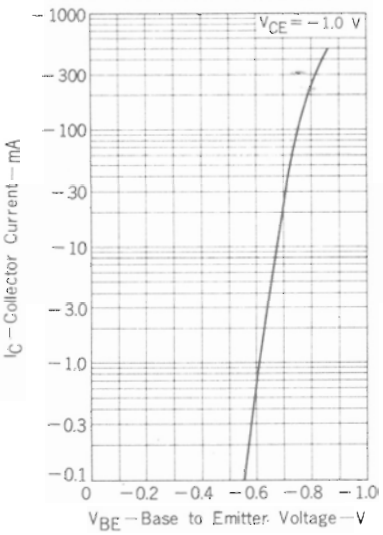
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



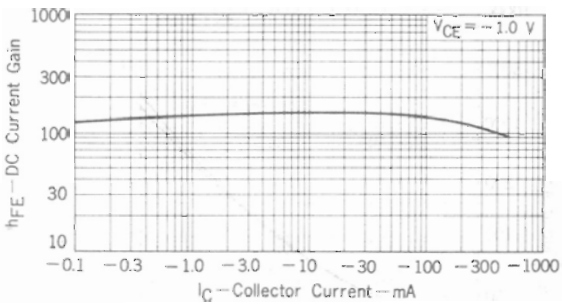
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



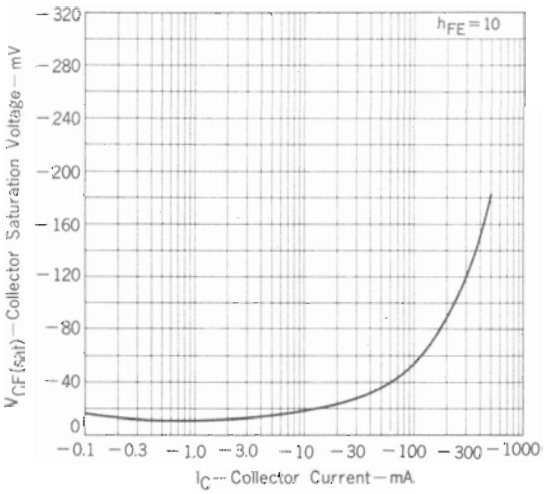
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



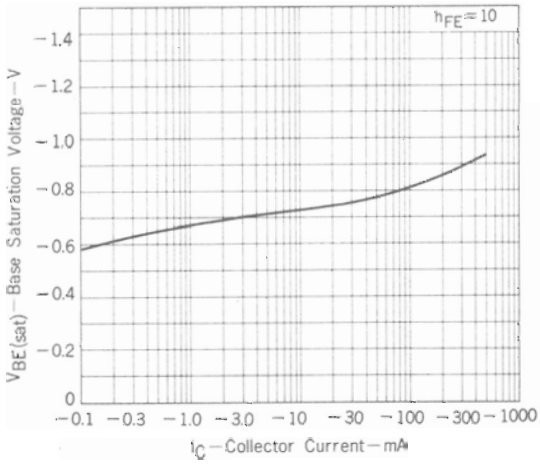
DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

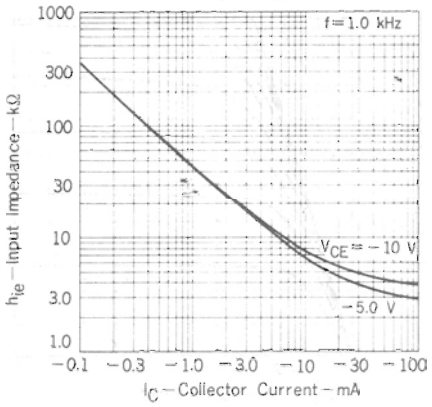


BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT

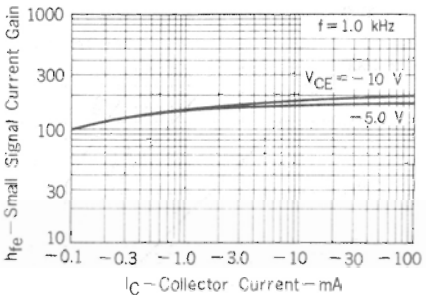


TYPICAL SMALL SIGNAL "h" PARAMETERS COMMON EMITTER

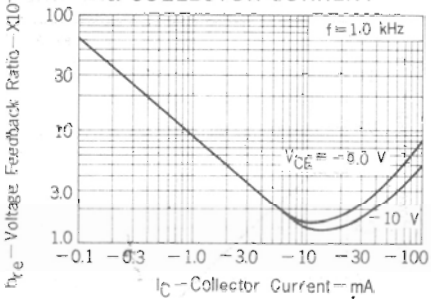
INPUT IMPEDANCE vs. COLLECTOR CURRENT



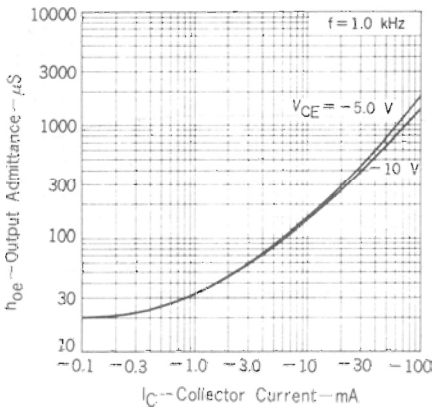
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE9013

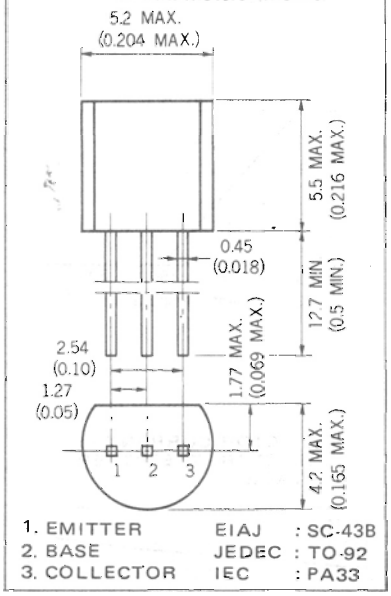
DESCRIPTION

The JE9013 is designed for use in 1 W output amplifier of portable radios in class B push-pull operation.

FEATURES

- High total power dissipation. (P_T: 625 mW)
- High collector current. (I_C: 500 mA)
- Complementary to JE9012.
- Excellent h_{FE} linearity.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 625 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage ..... 40 V

V_{CEO} Collector to Emitter Voltage ..... 20 V

V_{EBO} Emitter to Base Voltage ..... 5.0 V

I_C Collector Current ..... 500 mA

I_B Base Current ..... 100 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	64	120	202	–	V_{CE} = 1.0 V, I_C = 50 mA
h_{FE2}	DC Current Gain	40	120		–	V_{CE} = 1.0 V, I_C = 500 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.16	0.60	V	I_C = 500 mA, I_B = 50 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.91	1.20	V	I_C = 500 mA, I_B = 50 mA
V_{BE}	Base to Emitter Voltage	0.60	0.67	0.70	V	V_{CE} = 1.0 V, I_C = 10 mA
BV_{CBO}	Collector to Base Breakdown Voltage	40			V	I_C = 0.1 mA, I_E = 0
BV_{CEO}	Collector to Emitter Breakdown Voltage	20			V	I_C = 1.0 mA, I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E = −0.1 mA, I_C = 0
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 25 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 3.0 V, I_C = 0

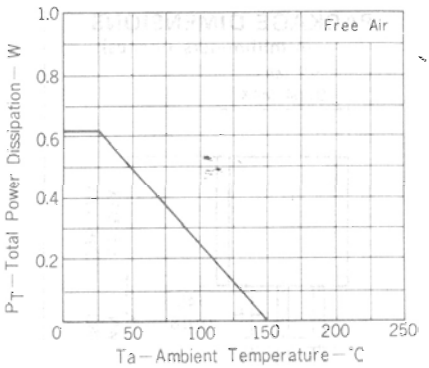
Classification of h_{FE1}

Rank	D	E	F	G	H
Range	64–91	78–112	96–135	112–166	144–202

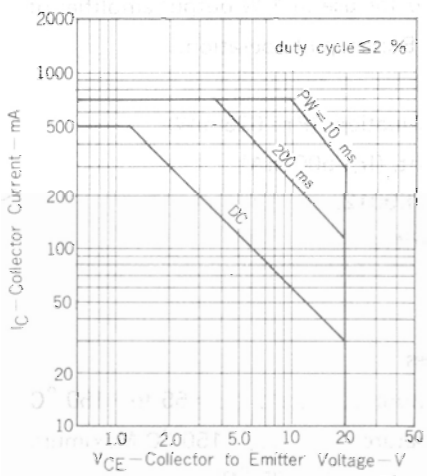
h_{FE} Test Conditions : V_{CE} = 1.0 V, I_C = 50 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

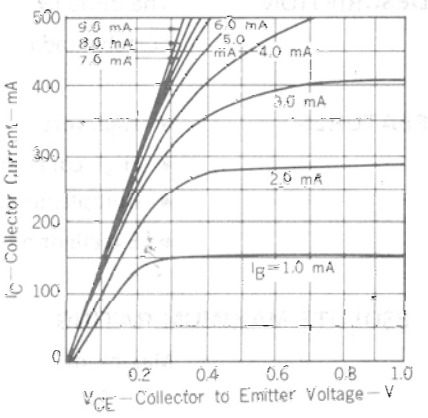
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



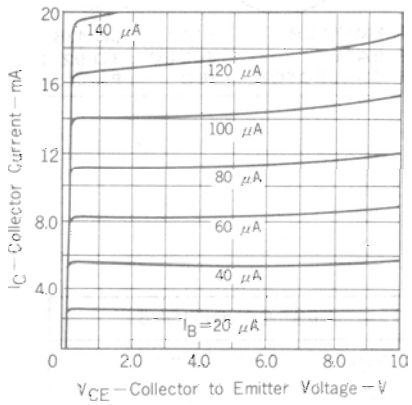
SAFE OPERATING AREA



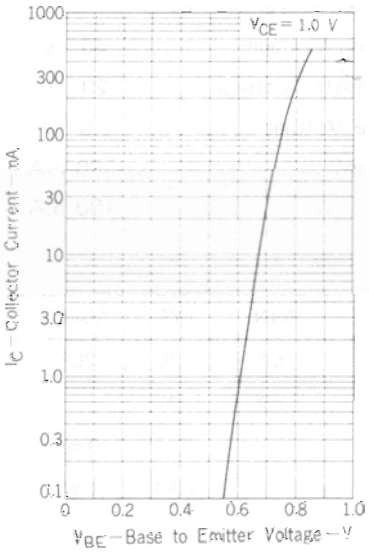
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



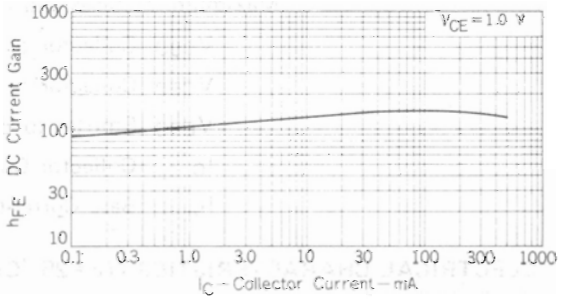
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



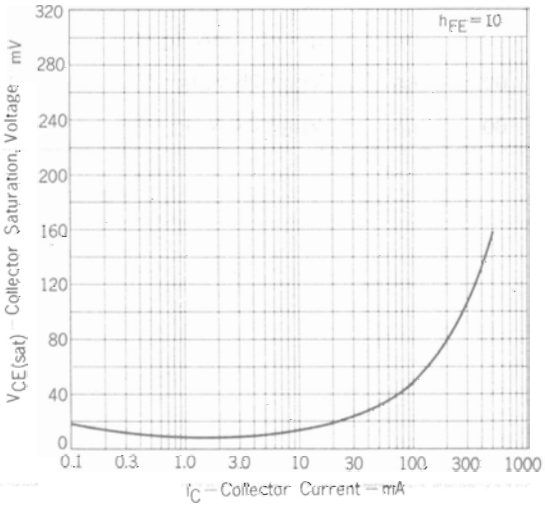
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



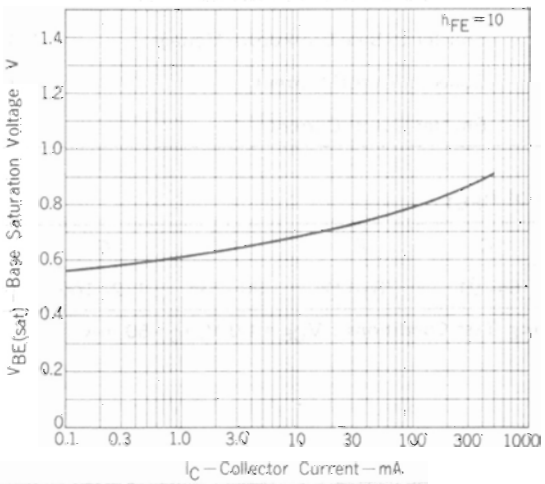
DC CURRENT GAIN vs. COLLECTOR CURRENT



COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

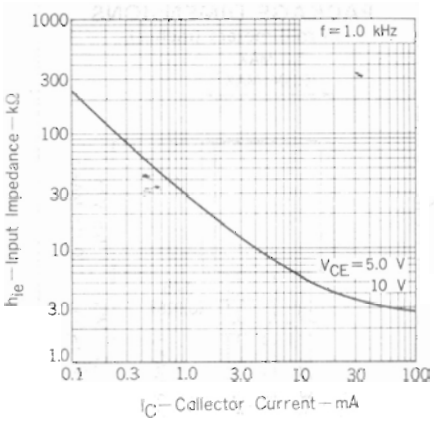


BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT

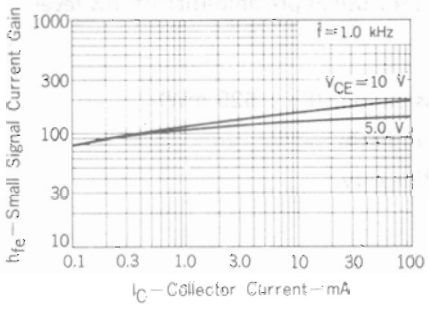


TYPICAL SMALL SIGNAL "h" PARAMETERS COMMON EMITTER

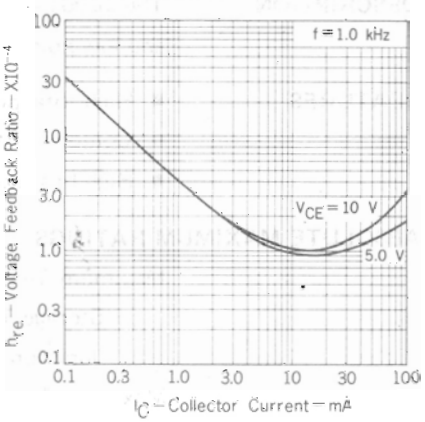
INPUT IMPEDANCE vs. COLLECTOR CURRENT



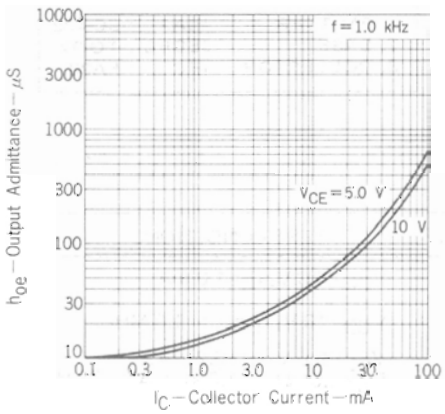
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

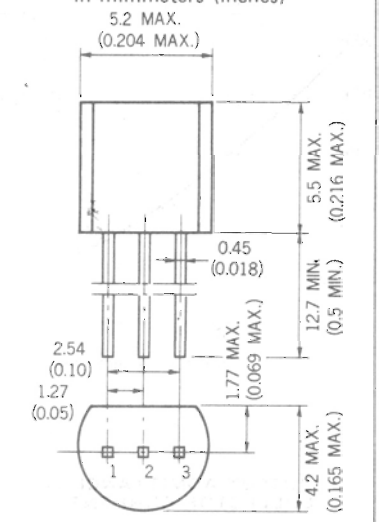
NPN SILICON TRANSISTOR
JE9014

DESCRIPTION The JE9014 is designed for use in pre-amplifier of low level and low noise.

FEATURES

- High total power dissipation. (P_T : 625 mW)
- Complementary to JE9015.
- High h_{FE} and good linearity.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 450 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage ..... 50 V

V_{CEO} Collector to Emitter Voltage ..... 45 V

V_{EBO} Emitter to Base Voltage ..... 5.0 V

I_C Collector Current ..... 100 mA

I_B Base Current ..... 100 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	280	1000	–	V_{CE}=5.0 V, I_C=1.0 mA
C_{ob}	Collector to Base Capacitance		2.2	3.5	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
NF	Noise Figure		0.9	10	dB	V_{CE}=5.0 V, I_C=0.2 mA, R_G=2.0 kΩ, f=1.0 kHz, Δf=200 Hz
f_T	Gain Bandwidth Product	150	270		MHz	V_{CE}=5.0 V, I_C=10 mA
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB}=50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB}=5.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	50			V	I_C=0.1 mA, I_E=0
BV_{CEO}	Collector to Emitter Breakdown Voltage	45			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E=0.1 mA, I_C=0
V_{BE}	Base to Emitter Voltage	0.58	0.63	0.70	V	V_{CE}=5.0 V, I_C=2.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.14	0.30	V	I_C=100 mA, I_B=5.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.84	1.00	V	I_C=100 mA, I_B=5.0 mA

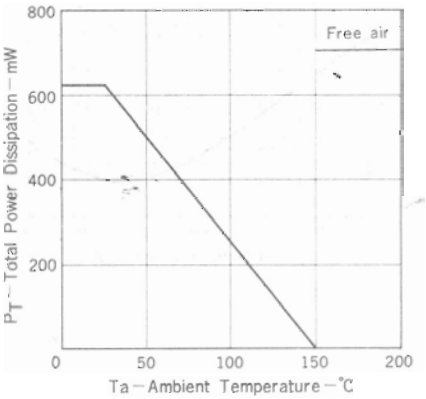
Classification of h_{FE}

Rank	A	B	C	D
Range	60 – 150	100 – 300	200 – 600	400 – 1000

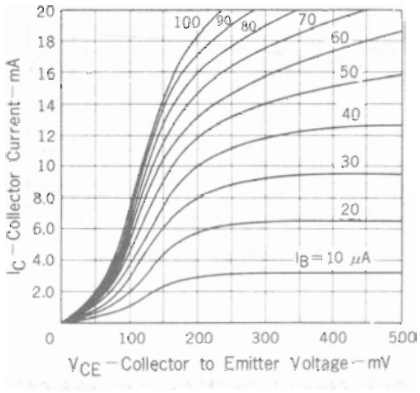
h_{FE} Test Conditions : V_{CE} = 5.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

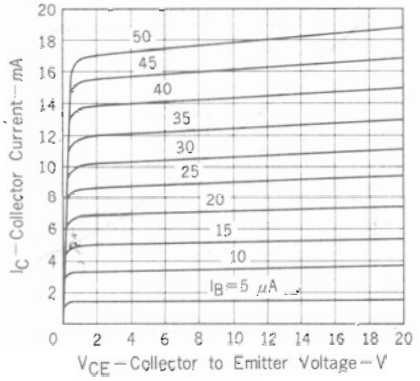
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



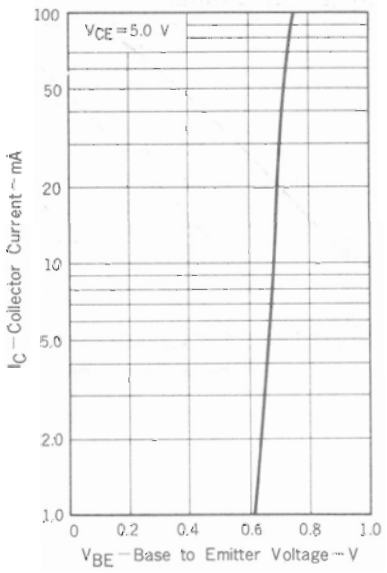
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



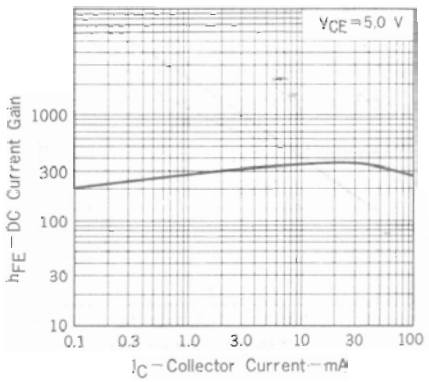
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



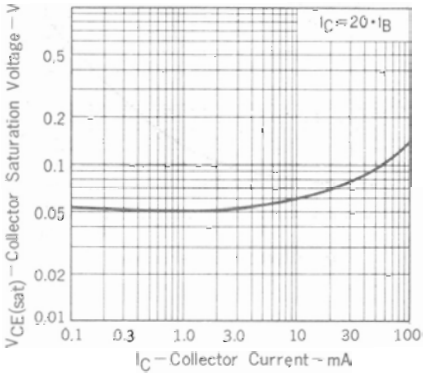
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



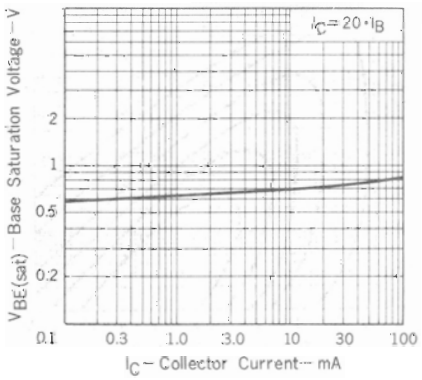
DC CURRENT GAIN vs. COLLECTOR CURRENT



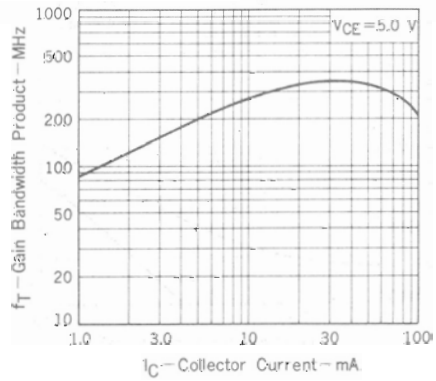
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



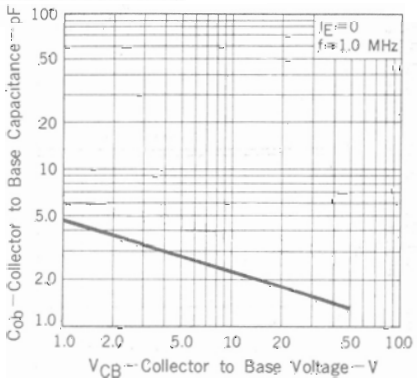
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

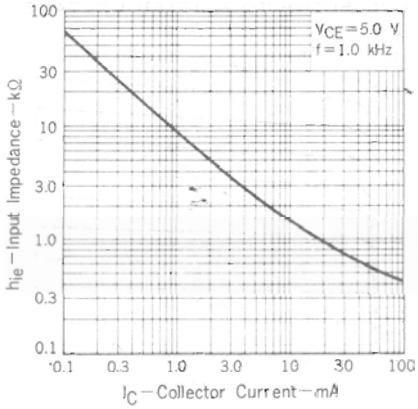


COLLECTOR TO BASE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

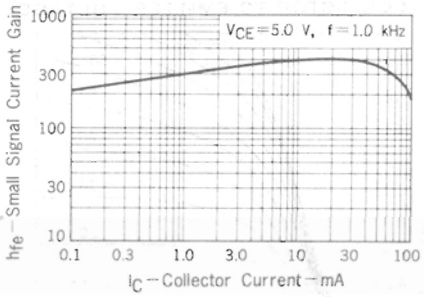


TYPICAL SMALL SIGNAL "h" PARAMETERS
COMMON EMITTER

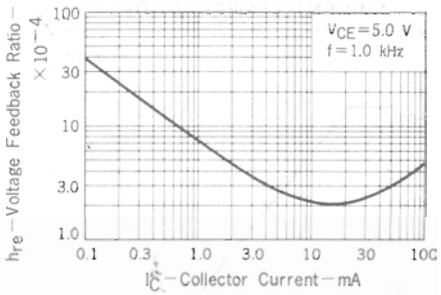
INPUT IMPEDANCE vs.
COLLECTOR CURRENT



SMALL SIGNAL CURRENT GAIN vs.
COLLECTOR CURRENT

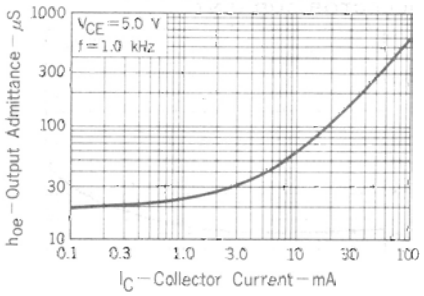


VOLTAGE FEEDBACK RATIO vs.
COLLECTOR CURRENT

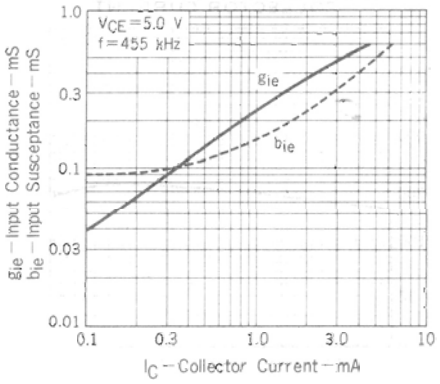


TYPICAL SMALL SIGNAL "y" PARAMETERS
COMMON EMITTER

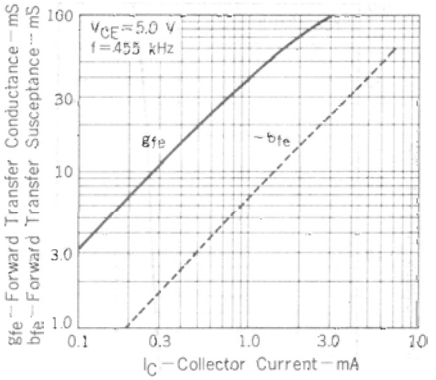
OUTPUT ADMITTANCE vs.
COLLECTOR CURRENT



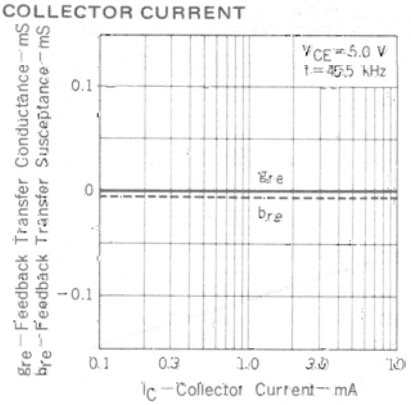
INPUT ADMITTANCE vs.
COLLECTOR CURRENT



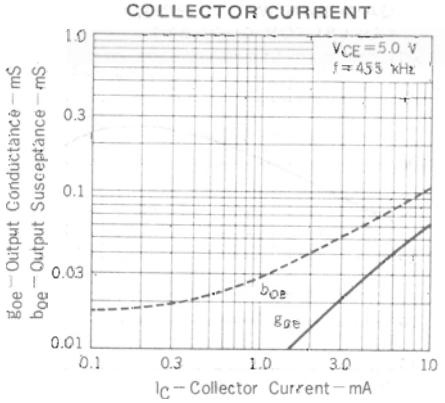
FORWARD TRANSFER ADMITTANCE vs.
COLLECTOR CURRENT



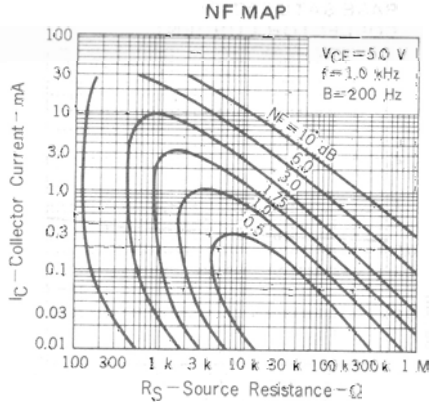
FEEDBACK TRANSFER ADMITTANCE vs.
COLLECTOR CURRENT



OUTPUT ADMITTANCE vs.
COLLECTOR CURRENT



NF MAP



NEC
ELECTRON DEVICE

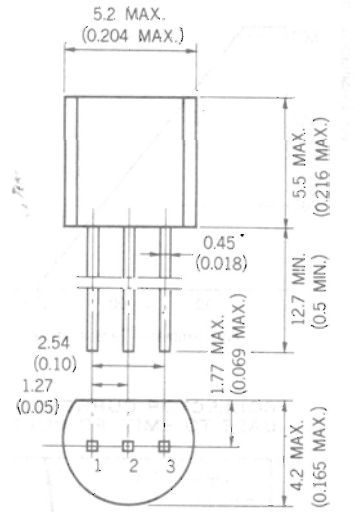
PNP SILICON TRANSISTOR
JE9015

DESCRIPTION The JE9015 is designed for use in pre-amplifier of low level and low noise.

FEATURES

- High total power dissipation. (P_T: 625 mW)
- Complementary to JE9014.
- High h_{FE} and good linearity.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 450 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage ..... −50 V

V_{CEO} Collector to Emitter Voltage ..... −45 V

V_{EBO} Emitter to Base Voltage ..... −5.0 V

I_C Collector Current ..... −100 mA

I_B Base Current ..... −100 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	60	200	600		V_{CE}=−5.0 V, I_C=−1.0 mA
C_{ob}	Collector to Base Capacitance		4.5	7.0	pF	V_{CB}=−10 V, I_E=0, f=1.0 MHz
NF	Noise Figure		0.7	10	dB	V_{CE}=−5.0 V, I_C=−0.2 mA, R_G=2.0 kΩ, f=1.0 kHz, Δf=200 Hz
f_T	Gain Bandwidth Product	100	190		MHz	V_{CE}=−5.0 V, I_C=−10 mA
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB}=−50 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB}=−5.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	−50			V	I_C=−0.1 mA, I_E=0
BV_{CEO}	Collector to Emitter Breakdown Voltage	−45			V	I_C=−1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−0.1 mA, I_C=0
V_{BE}	Base to Emitter Voltage	−0.60	−0.65	−0.75	V	V_{CE}=−5.0 V, I_C=−2.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.20	−0.70	V	I_C=−100 mA, I_B=−5.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.82	−1.0	V	I_C=−100 mA, I_B=−5.0 mA

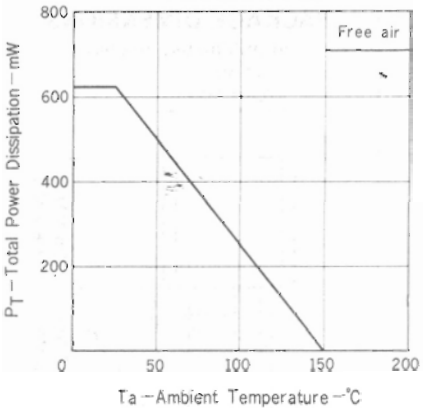
Classification of h_{FE}

Rank	A	B	C
Range	60 – 150	100 – 300	200 – 600

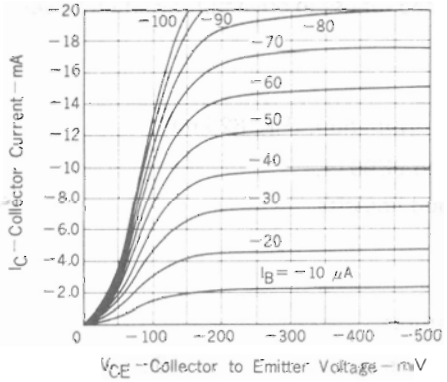
h_{FE} Test Conditions : V_{CE} = −5.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta=25 °C unless otherwise noted)

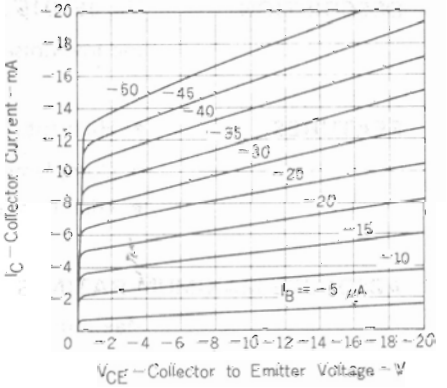
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



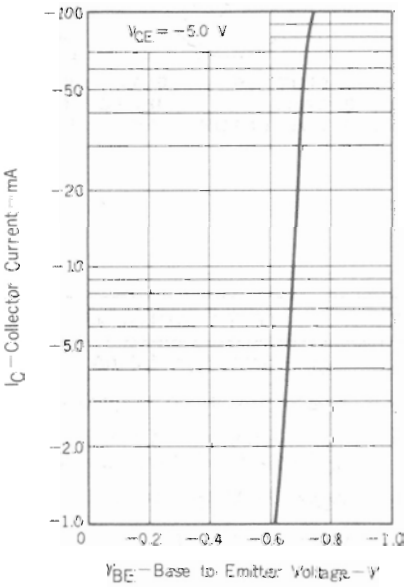
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



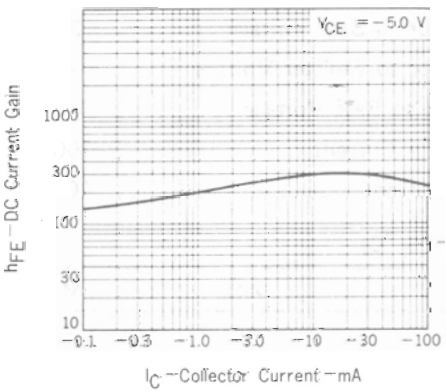
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



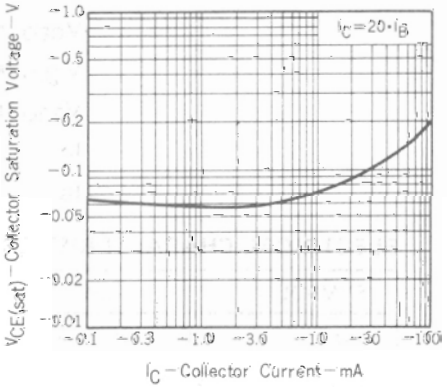
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



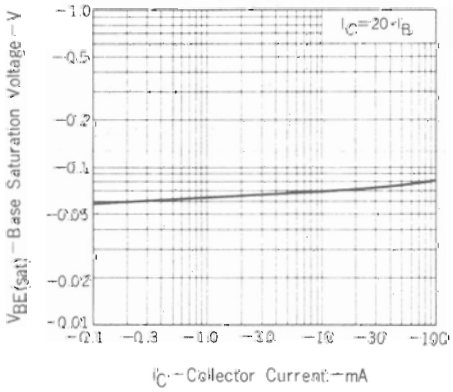
DC CURRENT GAIN vs. COLLECTOR CURRENT



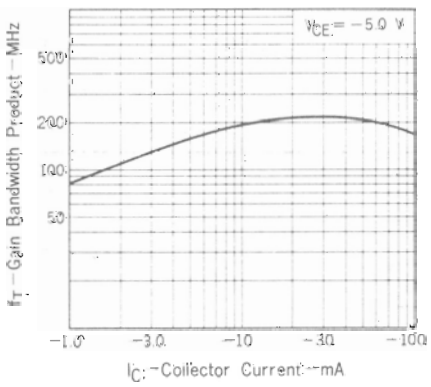
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



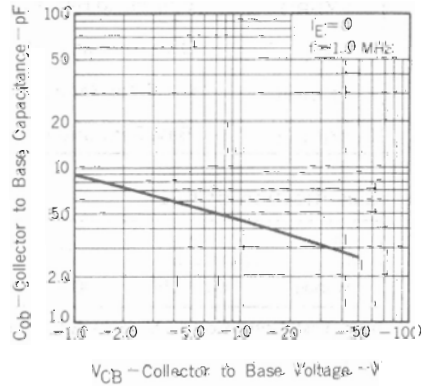
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

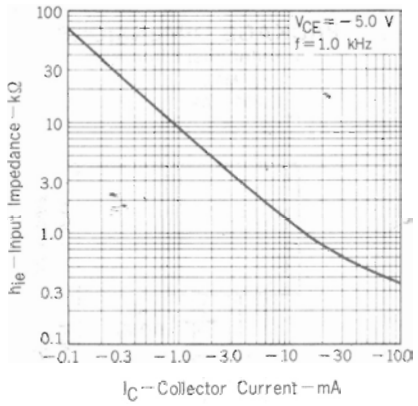


COLLECTOR TO BASE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

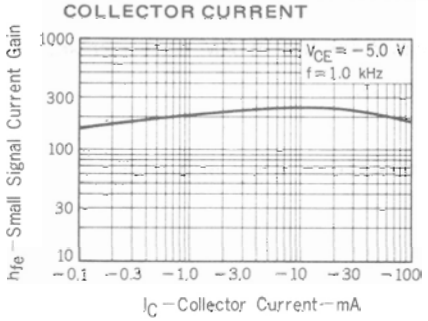


TYPICAL SMALL SIGNAL "h" PARAMETERS COMMON EMITTER

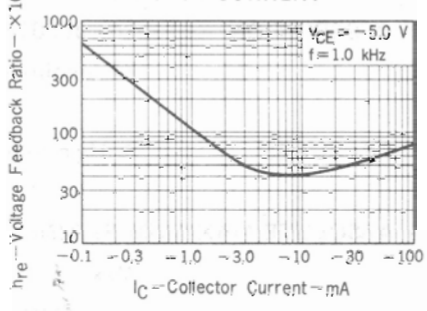
INPUT IMPEDANCE vs. COLLECTOR CURRENT



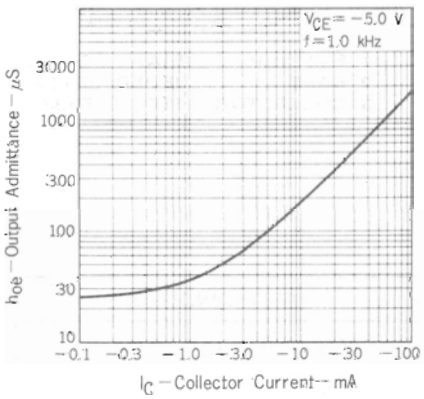
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



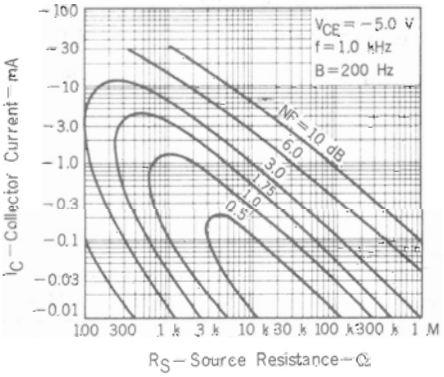
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



NF MAP



NEC
ELECTRON DEVICE

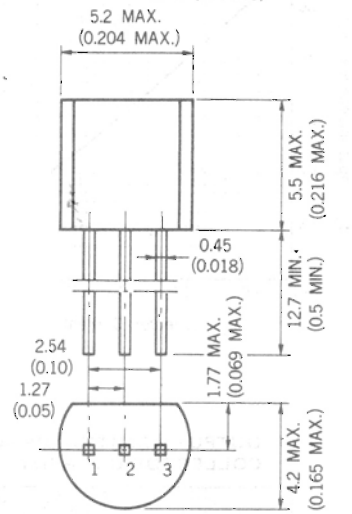
NPN SILICON TRANSISTOR
JE9016

DESCRIPTION The JE9016 is designed for use in AM converter and FM RF amplifier of low noise.

FEATURES

- High total power dissipation. (P_T : 400 mW)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature ..... −55 to +150 °C
- Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation ..... 400 mW

Maximum Voltages and Currents (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage ..... 30 V
- V_{CEO} Collector to Emitter Voltage ..... 20 V
- V_{EBO} Emitter to Base Voltage ..... 4.0 V
- I_C Collector Current ..... 25 mA
- I_B Base Current ..... 5.0 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	28	90	198	—	V_{CE} = 5.0 V, I_C = 1.0 mA
C_{ob}	Collector to Base Capacitance		1.2	1.6	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
NF	Noise Figure		3.0	5.0	dB	V_{CE} = 5.0 V, I_C = 1.0 mA, R_G = 50 Ω, f = 100 MHz
f_T	Gain Bandwidth Product	400	620		MHz	V_{CE} = 5.0 V, I_C = 1.0 mA
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 3.0 V, I_C = 0
BV_{CBO}	Collector to Base Breakdown Voltage	30			V	I_C = 0.1 mA, I_E = 0
BV_{CEO}	Collector to Emitter Breakdown Voltage	20			V	I_C = 1.0 mA, I_B = 0
V_{BE}	Base to Emitter Voltage		0.72		V	V_{CE} = 5.0 V, I_C = 1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.1	0.3	V	I_C = 10 mA, I_B = 1.0 mA

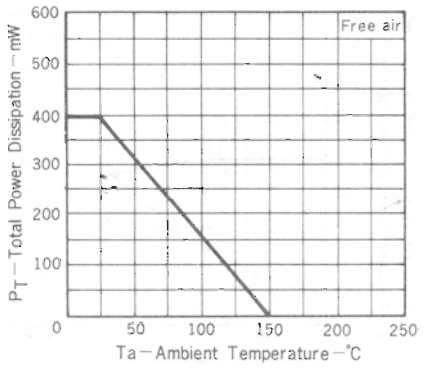
Classification of h_{FE}

Rank	D	E	F	G	H	I
Range	28 – 45	39 – 60	54 – 80	72 – 108	97 – 146	132 – 198

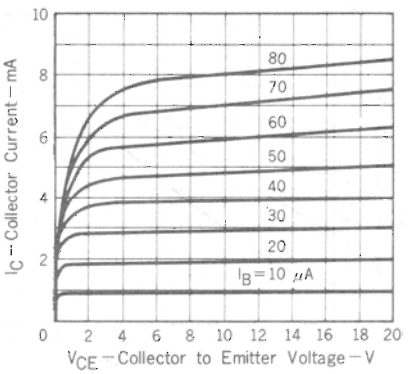
h_{FE} Test Conditions : V_{CE} = 5.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

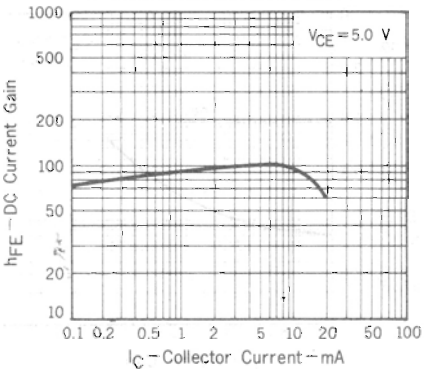
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



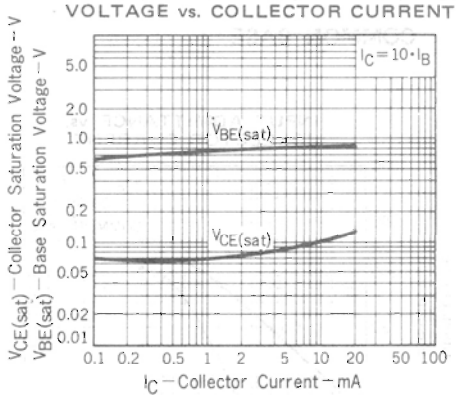
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



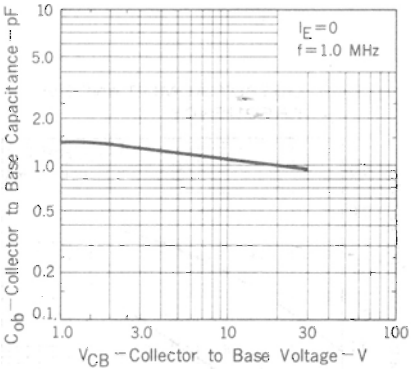
DC CURRENT GAIN vs. COLLECTOR CURRENT



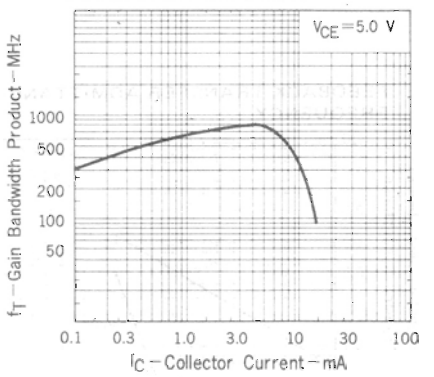
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR TO BASE CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE

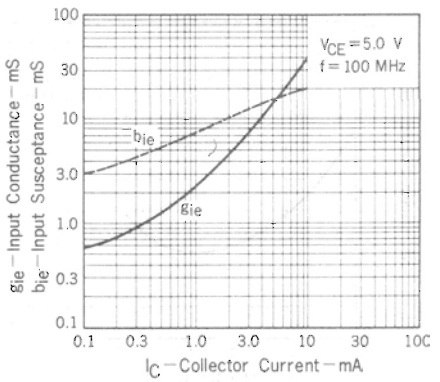


GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

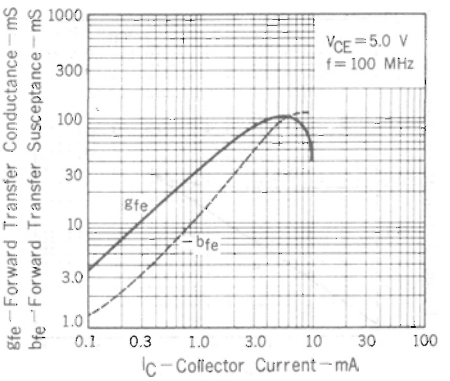


TYPICAL SMALL SIGNAL "y" PARAMETERS COMMON EMITTER

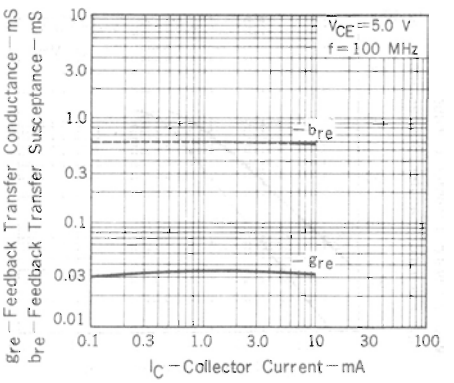
INPUT ADMITTANCE vs. COLLECTOR CURRENT



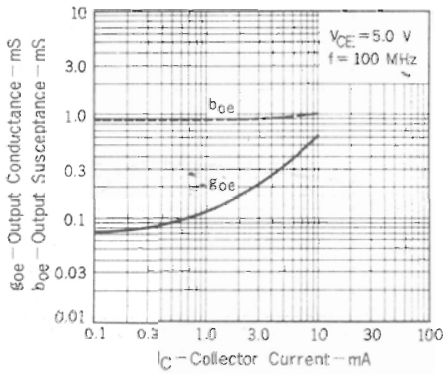
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



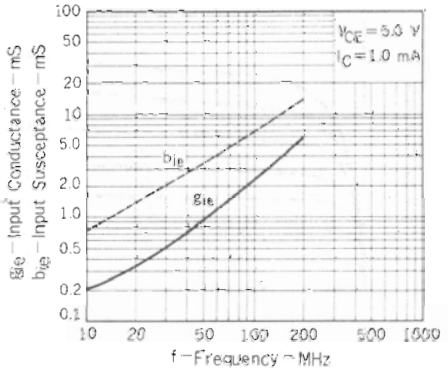
FEEDBACK TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



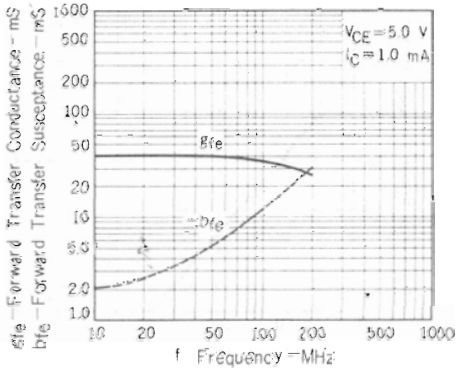
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



INPUT ADMITTANCE vs. FREQUENCY

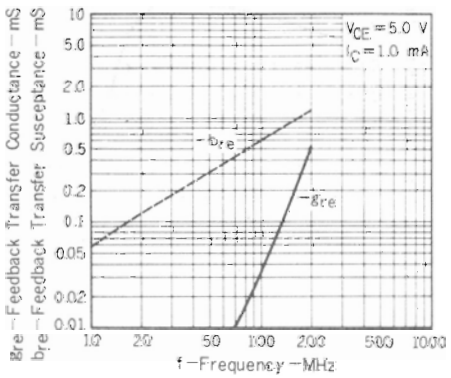


FORWARD TRANSFER ADMITTANCE vs. FREQUENCY

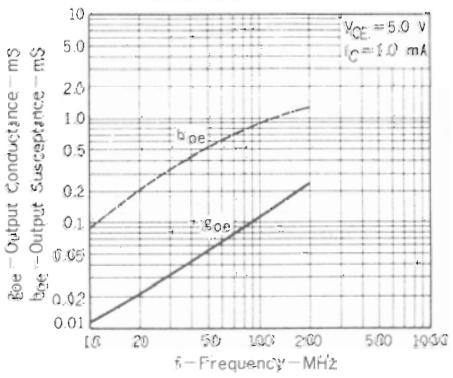


COMMON BASE

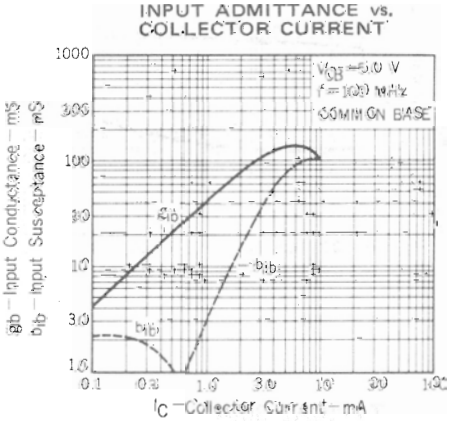
FEEDBACK TRANSFER ADMITTANCE vs. FREQUENCY



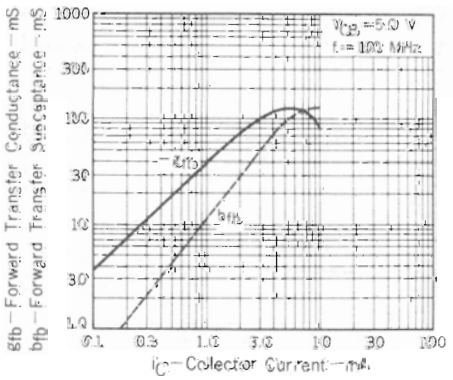
OUTPUT ADMITTANCE vs. FREQUENCY



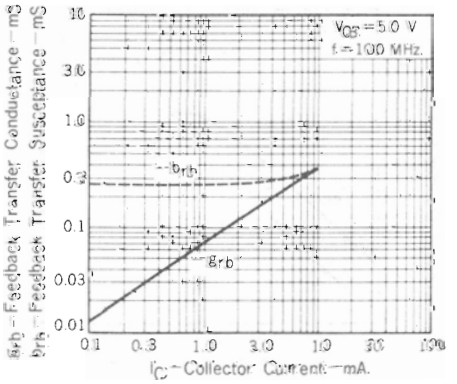
INPUT ADMITTANCE vs. COLLECTOR CURRENT



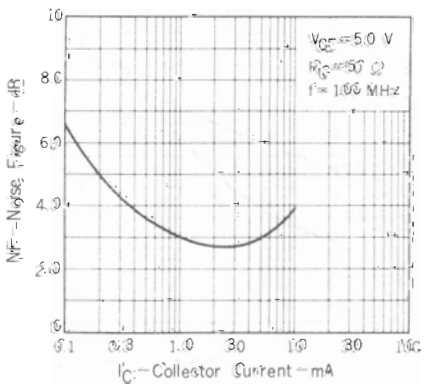
FORWARD TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



FEEDBACK TRANSFER ADMITTANCE vs. COLLECTOR CURRENT



NOISE FIGURE vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE9018

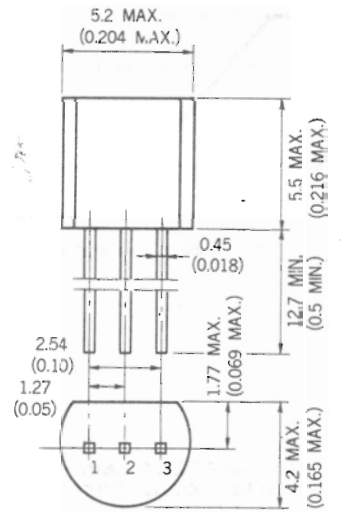
DESCRIPTION

The JE9018 is designed for use in AM/FM IF amplifier and local oscillator of FM/VHF tuner.

FEATURES

- High total power dissipation. (P_T : 400 mW)
- High gain bandwidth product. (f_T=1 100 MHz TYP.)
- Stable oscillation and small frequency drift for supply voltage and ambient temperature change.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature ..... −55 to +150 °C

Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation ..... 400 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage ..... 30 V

V_{CEO} Collector to Emitter Voltage ..... 15 V

V_{EBO} Emitter to Base Voltage ..... 5.0 V

I_C Collector Current ..... 50 mA

I_B Base Current ..... 10 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	28	100	198	—	V_{CE} = 5.0 V, I_C = 1.0 mA
C_{ob}	Output Capacitance		1.3	1.7	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
f_T	Gain Bandwidth Product	700	1100		MHz	V_{CE} = 5.0 V, I_C = 5.0 mA
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB} = 12 V, I_E = 0
BV_{CBO}	Collector to Base Breakdown Voltage	30			V	I_C = 0.1 mA, I_E = 0
BV_{CEO}	Collector to Emitter Breakdown Voltage	15			V	I_C = 1.0 mA, I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E = 0.1 mA, I_C = 0
$V_{CE(sat)}$	Collector Saturation Voltage			0.5	V	I_C = 10 mA, I_B = 1.0 mA

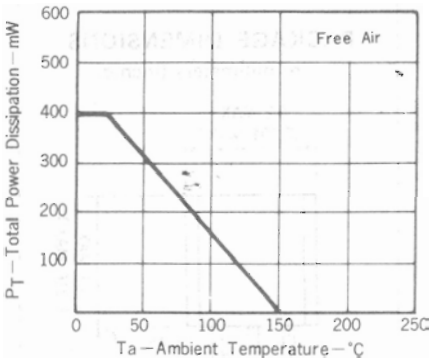
Classification of h_{FE}

Rank	D	E	F	G	H	I
Range	28–45	39–60	54–80	72–108	97–146	132–198

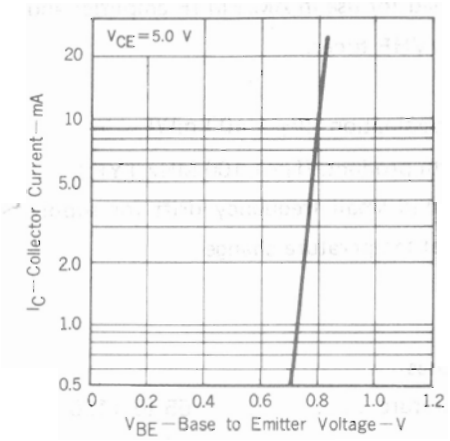
h_{FE} Test Conditions : V_{CE} = 5.0 V, I_C = 1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C)

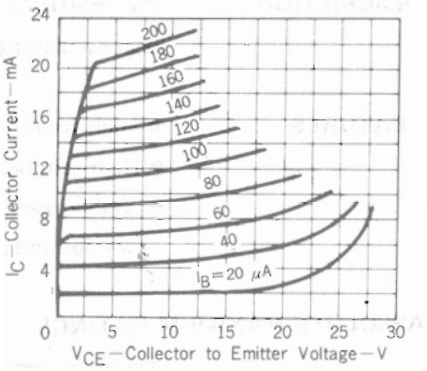
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



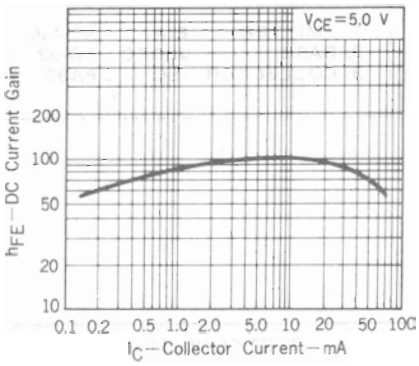
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



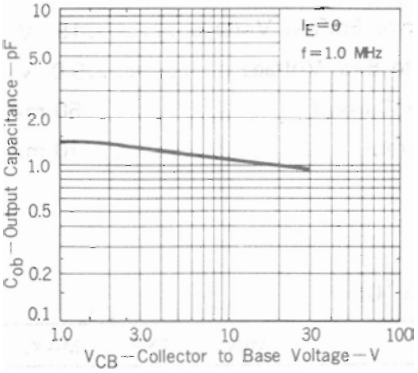
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



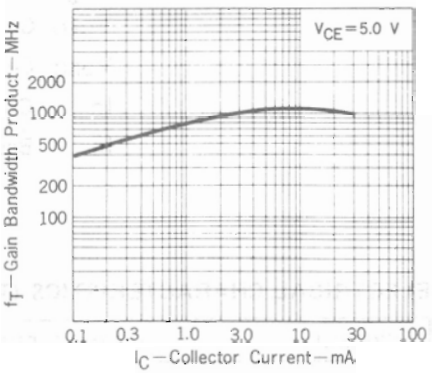
DC CURRENT GAIN vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



NEC
ELECTRON DEVICE

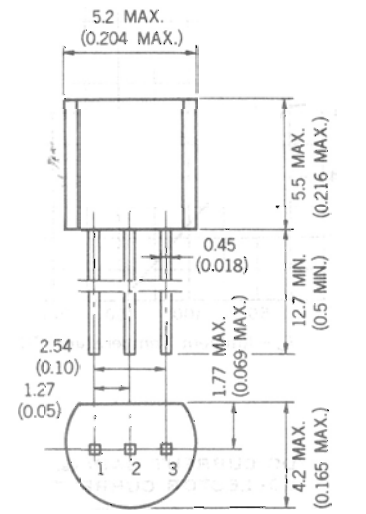
NPN SILICON TRANSISTOR
JE9042

DESCRIPTION The JE9042 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- Complements to PNP Type JE9092.
- JE9042 Electrically Similar to MPS-A42.
- High voltage $V_{CEO} \geqq 300$ V
- High Electrostatic-Discharge-Resistant (E-B reverse bias, C = 2 300 pF) ESDR : TYP. 1 000 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 300 V
- V_{CEO} Collector to Emitter Voltage . . . . . 300 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current . . . . . 500 mA
- I_B Base Current . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	25	110		—	V_{CE} = 10 V, I_C = 1.0 mA
h_{FE2}	DC Current Gain	40	120	300	—	V_{CE} = 10 V, I_C = 30 mA
ESDR	Electrostatic-Discharge-Resistant		1000		V	See Test Circuit
t_{on}	Turn-on Time			2.0	μs	V_{CC} = 30 V, I_C = 100 mA, $I_{B1} = -I_{B2}$ = 10 mA
t_{off}	Turn-off Time			3.0	μs	
t_{stg}	Storage Time			2.0	μs	
f_T	Gain Bandwidth Product	30	60		MHz	V_{CE} = 30 V, I_E = −10 mA
C_{ob}	Output Capacitance		2.8	4.0	pF	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 300 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600	670	700	mV	V_{CE} = 10 V, I_C = 10 mA
$V_{CE(sat)1}$	Collector Saturation Voltage		0.08	0.5	V	I_C = 20 mA, I_B = 2.0 mA
$V_{CE(sat)2}$	Collector Saturation Voltage		0.15	1.5	V	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)1}$	Base Saturation Voltage		0.7	0.9	V	I_C = 20 mA, I_B = 2.0 mA
$V_{BE(sat)2}$	Base Saturation Voltage		0.8	1.5	V	I_C = 50 mA, I_B = 5.0 mA

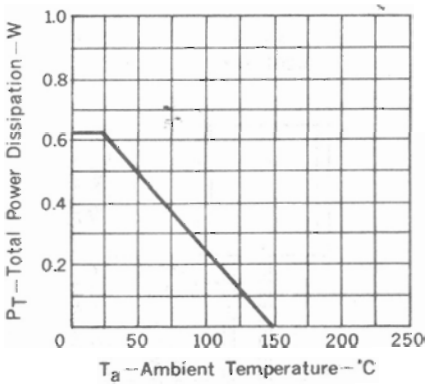
Classification of h_{FE2}

Rank	A	B	C
Range	40 — 90	70 — 180	140 — 300

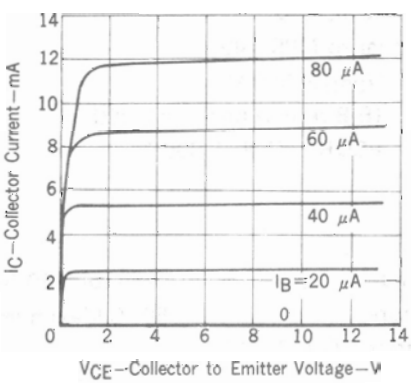
Test Conditions : V_{CE} = 10 V, I_C = 30 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

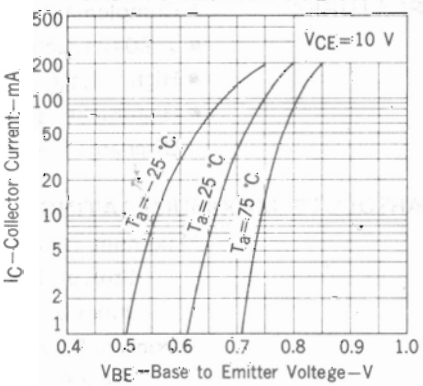
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



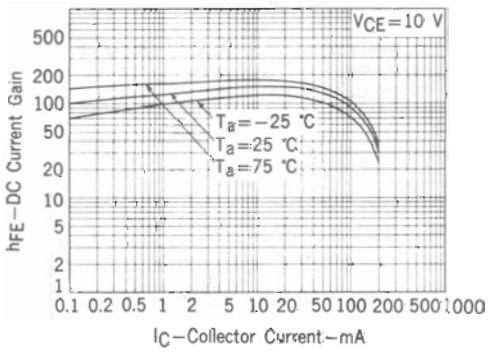
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



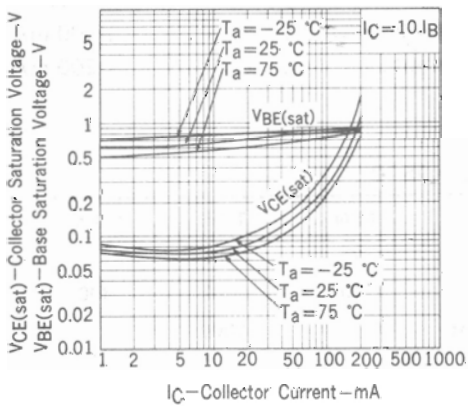
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



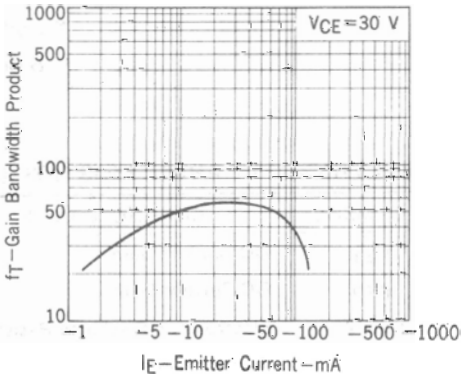
DC CURRENT GAIN vs. COLLECTOR CURRENT



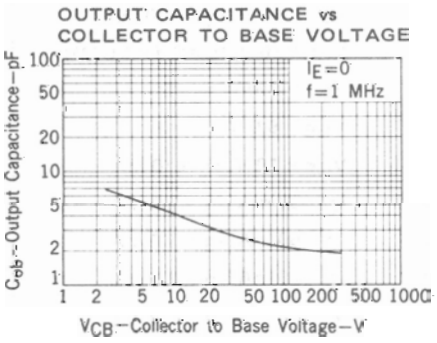
COLLECTOR SATURATION VOLTAGE, BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



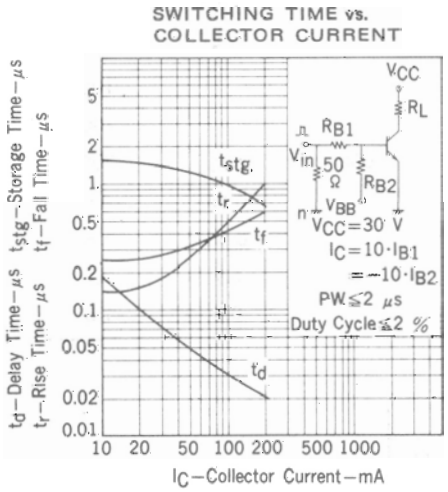
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



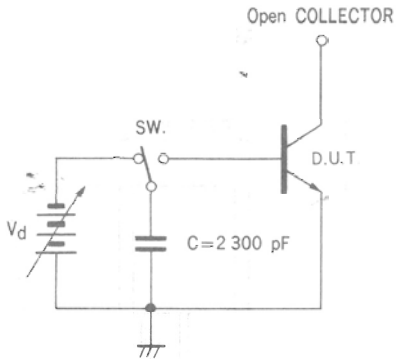
OUTPUT CAPACITANCE vs COLLECTOR TO BASE VOLTAGE



SWITCHING TIME vs. COLLECTOR CURRENT



ELECTROSTATIC-DISCHARGE-RESISTANT TEST CIRCUIT



TEST CONDITION

1) E-B reverse bias
2) C = 2 300 pF
3) Apply one shot pluse to D.U.T. (Device Under the Test) by SW.

JUDGEMENT

REJECT; BV_{EBO} waveform defect
As a result if D.U.T. is not rejected, apply higher voltage to capacitor and test again.

NEC
ELECTRON DEVICE

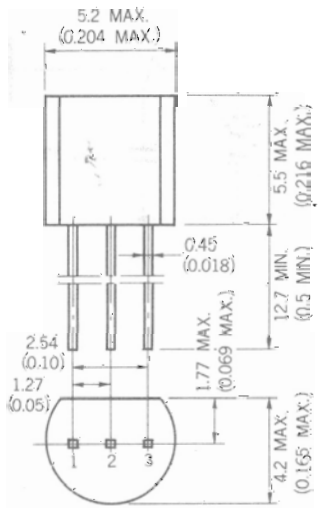
NPN SILICON TRANSISTOR
JE9043

DESCRIPTION The JE9043 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Collector-Emitter Breakdown Voltage.
  $V_{CEO} > 200$ V (@ $I_C = 1.0$ mA)
- Complements to PNP Type JE9093.
- JE9043 Electrically Similar to MPS-A43.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation ($T_a = 25$ °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Currents ($T_a = 25$ °C)

- V_{CBO} Collector to Base Voltage . . . . . 200 V
- V_{CEO} Collector to Emitter Voltage . . . . . 200 V
- V_{EBO} Emitter to Base Voltage . . . . . 6.0 V
- I_C Collector Current . . . . . 500 mA
- I_B Base Current . . . . . 200 mA

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	25	230		−	$V_{CE} = 10$ V, $I_C = 1.0$ mA
h_{FE2}	DC Current Gain	40	250	500	−	$V_{CE} = 10$ V, $I_C = 10$ mA
h_{FE3}	DC Current Gain	30	250		−	$V_{CE} = 10$ V, $I_C = 30$ mA
t_{on}	Turn-on Time		0.2		μs	$I_C = 100$ mA, $I_{B1} = -I_{B2} = 10$ mA
t_{off}	Turn-off Time		0.5		μs	
t_{stg}	Storage Time		0.2		μs	
f_T	Gain Bandwidth Product	50	150		MHz	$V_{CE} = 20$ V, $I_E = -10$ mA
C_{ob}	Output Capacitance		3.0	5.0	pF	$V_{CB} = 20$ V, $I_E = 0$, $f = 1.0$ MHz
I_{CBO}	Collector Cutoff Current			100	nA	$V_{CB} = 200$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			100	nA	$V_{EB} = 6.0$ V, $I_C = 0$
V_{BE}	Base to Emitter Voltage		650	700	mV	$V_{CE} = 10$ V, $I_C = 10$ mA
$V_{CE(sat)1}$	Collector Saturation Voltage		0.05	0.3	V	$I_C = 20$ mA, $I_B = 2.0$ mA
$V_{CE(sat)2}$	Collector Saturation Voltage		0.08	0.3	V	$I_C = 50$ mA, $I_B = 5.0$ mA
$V_{BE(sat)1}$	Base Saturation Voltage		0.7	1.0	V	$I_C = 20$ mA, $I_B = 2.0$ mA
$V_{BE(sat)2}$	Base Saturation Voltage		0.75	1.2	V	$I_C = 50$ mA, $I_B = 5.0$ mA

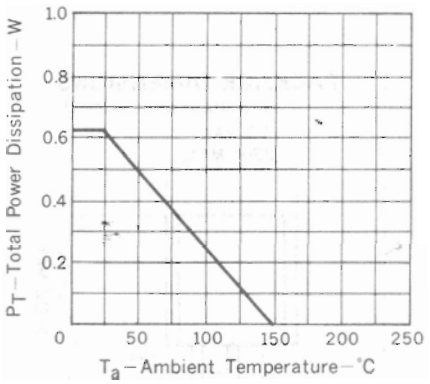
Classification of h_{FE2}

Rank	A	B	C
Range	40 – 150	100 – 300	200 – 500

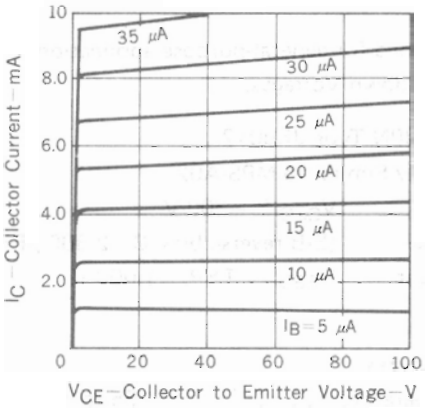
Test Conditions : $V_{CE} = 10$ V, $I_C = 10$ mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

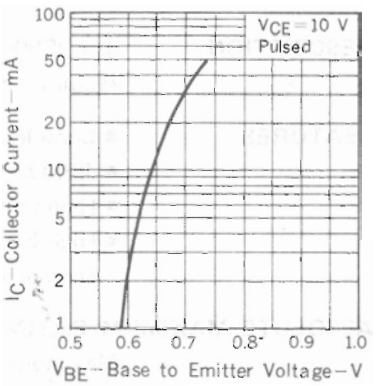
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



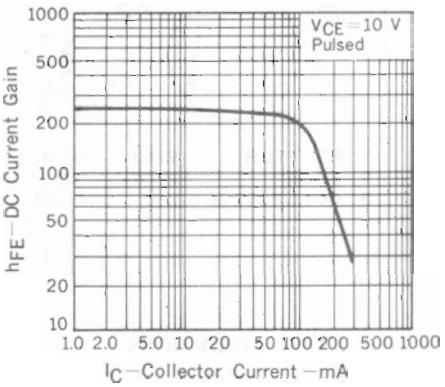
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



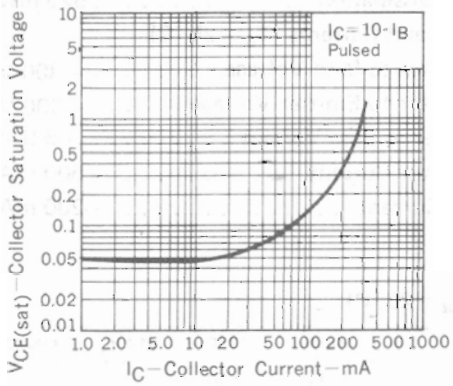
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



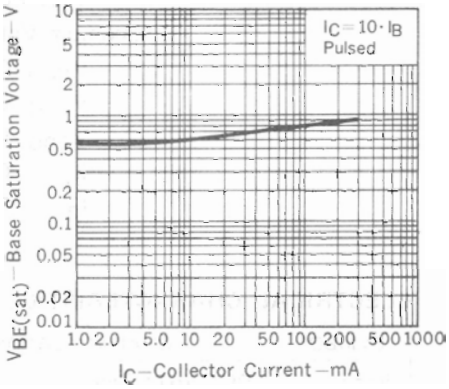
DC CURRENT GAIN vs. COLLECTOR CURRENT



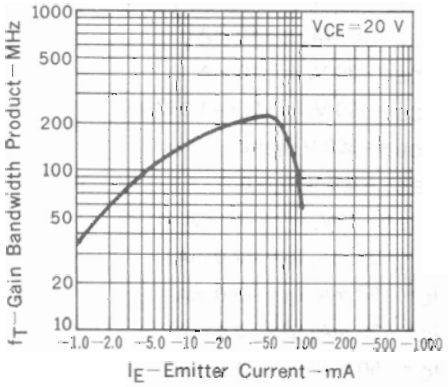
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



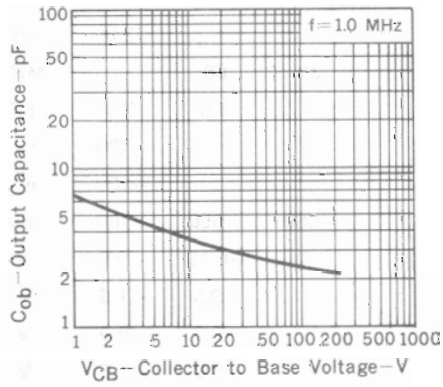
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

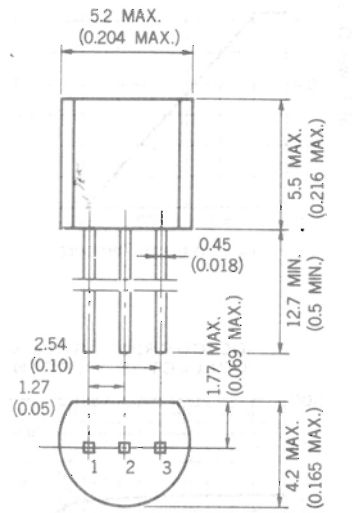
PNP SILICON TRANSISTOR
JE9092

DESCRIPTION The JE9092 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- Complements to NPN Type JE9042.
- JE9093 Electrically Similar to MPS-A92
- High voltage $V_{CEO} \geqq -300$ V
- High Electrostatic-Discharge-Resistant (E-B reverse bias, C = 2 300 pF) V_{ESDR} : TYP. −1 000 V

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −300 V
- V_{CEO} Collector to Emitter Voltage . . . . . −300 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current. . . . . −500 mA
- I_B Base Current. . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	25	120		–	V_{CE} = −10 V, I_C = −1.0 mA
h_{FE2}	DC Current Gain	40	120	300	–	V_{CE} = −10 V, I_C = −30 mA
V_{ESDR}	Electrostatic-Discharge-Resistant		−1000		V	See Test Circuit
t_{on}	Turn-on Time			2.0	μs	V_{CC} = −30 V, I_C = −100 mA, $-I_{B1} = I_{B2}$ = −10 mA
t_{off}	Turn-off Time			3.0	μs	
t_{stg}	Storage Time			2.0	μs	
f_T	Gain Bandwidth Product	30	80		MHz	V_{CE} = −30 V, I_E = 10 mA
C_{ob}	Output Capacitance		5.0	7.0	pF	V_{CB} = −30 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −300 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−600	−650	−700	mV	V_{CE} = −10V, I_C = −10 mA
$V_{CE(sat)1}$	Collector Saturation Voltage		−0.15	−0.5	V	I_C = −20 mA, I_B = −2.0 mA
$V_{CE(sat)2}$	Collector Saturation Voltage		−0.5	−1.5	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)1}$	Base Saturation Voltage		−0.7	−0.9	V	I_C = −20 mA, I_B = −2.0 mA
$V_{BE(sat)2}$	Base Saturation Voltage		−0.8	−1.5	V	I_C = −50 mA, I_B = −5.0 mA

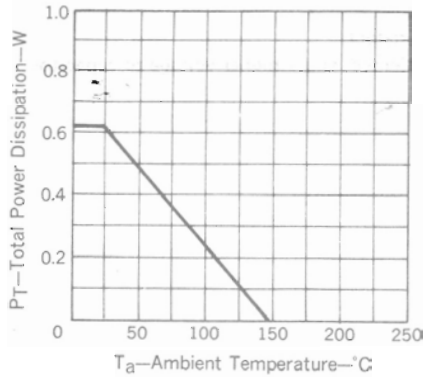
Classification of h_{FE2}

Rank	A	B	C
Range	40 – 90	70 – 180	140 – 300

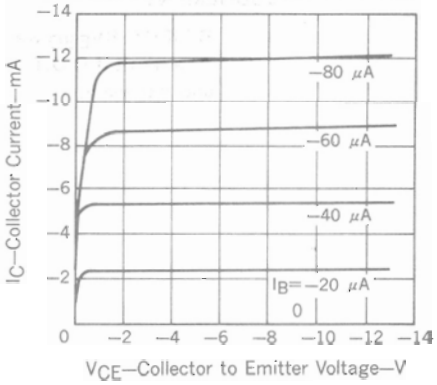
Test Conditions : V_{CE} = −10 V, I_C = −30 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

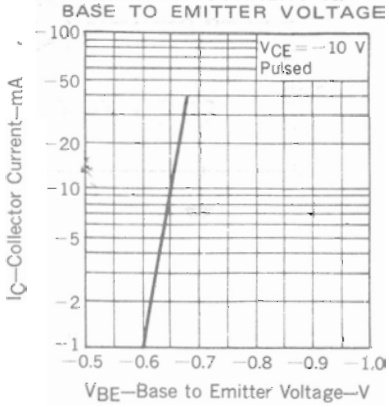
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



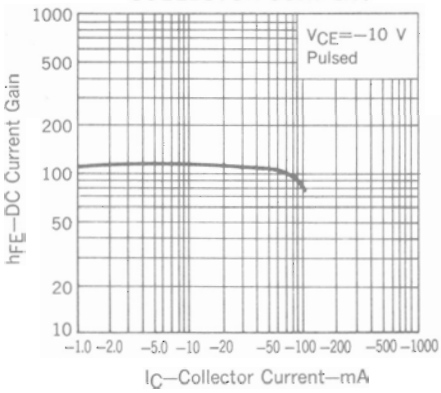
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



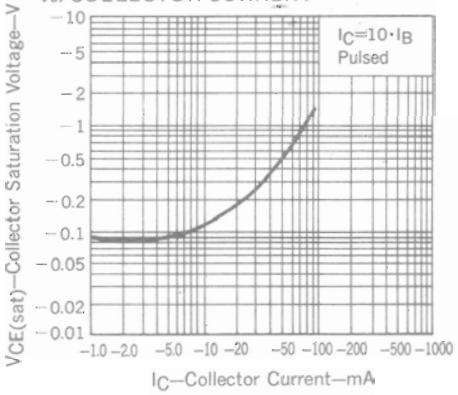
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



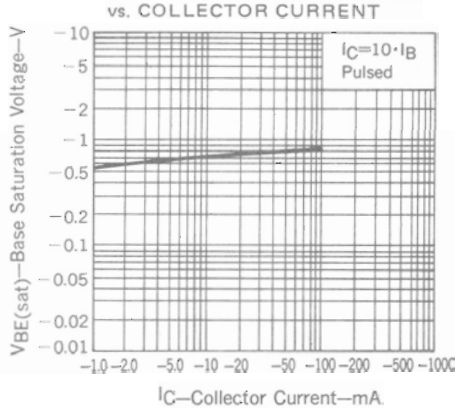
DC CURRENT GAIN vs. COLLECTOR CURRENT



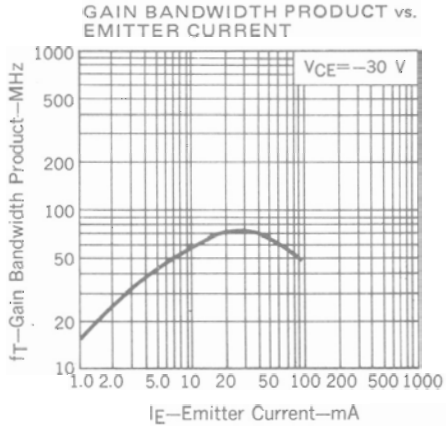
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



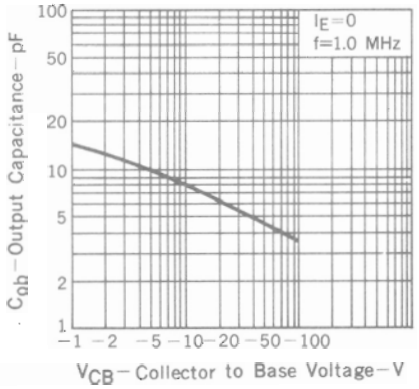
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



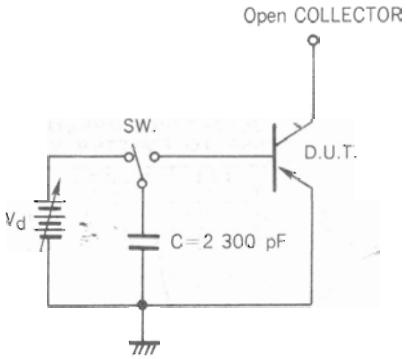
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



ELECTROSTATIC-DISCHARGE-RESISTANT TEST CIRCUIT



TEST CONDITION

1) E-B reverse bias
2) C = 2 300 pF
3) Apply one shot pluse to D.U.T. (Device Under the Test) by SW.

JUDGEMENT

REJECT; BV_{EBO} waveform defect
As a result if D.U.T. is not rejected, apply higher voltage to capacitor and test again.

NEC
ELECTRON DEVICE

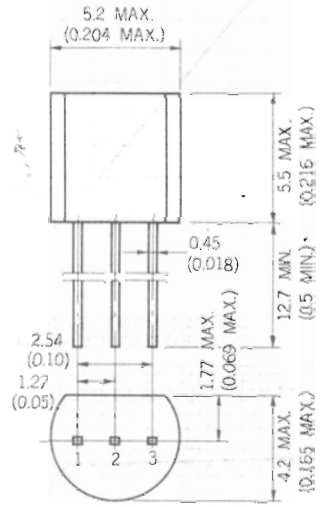
PNP SILICON TRANSISTOR
JE9093

DESCRIPTION The JE9093 is designed for general-purpose applications requiring high Breakdown Voltages.

FEATURES

- High Collector-Emitter Breakdown Voltage.
  $V_{CEO} > -200$ V (@ $I_C = -1.0$ mA)
- Complements to NPN Type JE9043.
- JE9093 Electrically Similar to MPS-A93

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . −200 V
- V_{CEO} Collector to Emitter Voltage . . . . . −200 V
- V_{EBO} Emitter to Base Voltage . . . . . −6.0 V
- I_C Collector Current. . . . . −500 mA
- I_B Base Current. . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	25	250		–	$V_{CE} = -10$ V, $I_C = -1.0$ mA
h_{FE2}	DC Current Gain	40	250	500	–	$V_{CE} = -10$ V, $I_C = -10$ mA
h_{FE3}	DC Current Gain	30	250		–	$V_{CE} = -10$ V, $I_C = -30$ mA
t_{on}	Turn-on Time		0.08		μs	$I_C = -100$ mA, $-I_{B1} = I_{B2} = -10$ mA
t_{off}	Turn-off Time		0.4		μs	
t_{stg}	Storage Time		0.1		μs	
f_T	Gain Bandwidth Product	50	130		MHz	$V_{CE} = -20$ V, $I_E = 10$ mA
C_{ob}	Output Capacitance		4.0	5.0	pF	$V_{CB} = -20$ V, $I_E = 0$, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	$V_{CB} = -200$ V, $I_E = 0$
I_{EBO}	Emitter Cutoff Current			−100	nA	$V_{EB} = -6.0$ V, $I_C = 0$
V_{BE}	Base to Emitter Voltage		−650	−700	mV	$V_{CE} = -10$ V, $I_C = -10$ mA
$V_{CE(sat)1}$	Collector Saturation Voltage		−0.09	−0.3	V	$I_C = -20$ mA, $I_B = -2.0$ mA
$V_{CE(sat)2}$	Collector Saturation Voltage		−0.15	−0.5	V	$I_C = -50$ mA, $I_B = -5.0$ mA
$V_{BE(sat)1}$	Base Saturation Voltage		−0.7	−1.0	V	$I_C = -20$ mA, $I_B = -2.0$ mA
$V_{BE(sat)2}$	Base Saturation Voltage		−0.75	−1.2	V	$I_C = -50$ mA, $I_B = -5.0$ mA

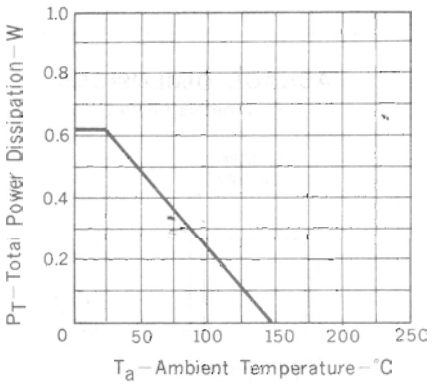
Classification of h_{FE2}

Rank	A	B	C
Range	40 – 150	100 – 300	200 – 500

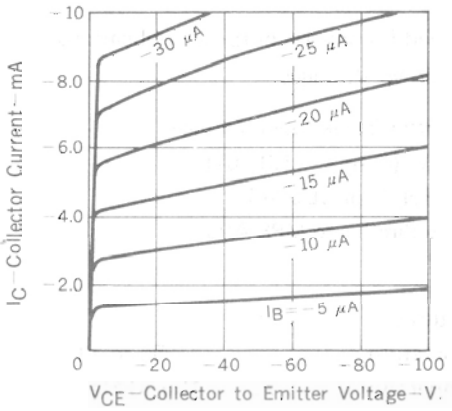
Test Conditions : $V_{CE} = -10$ V, $I_C = -10$ mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

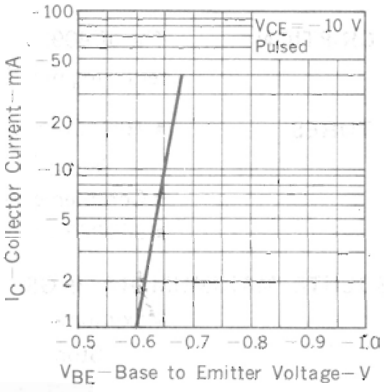
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



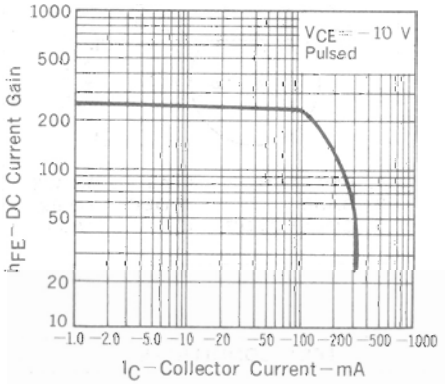
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



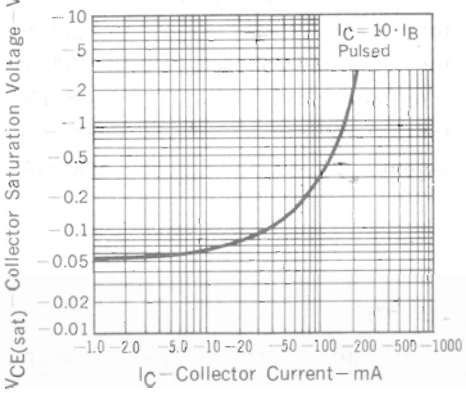
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



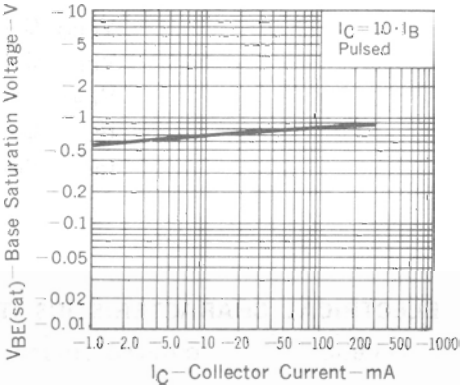
DC CURRENT GAIN vs. COLLECTOR CURRENT



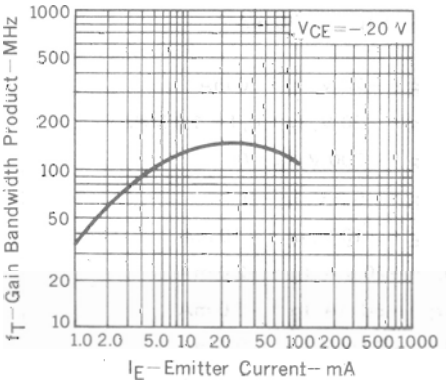
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



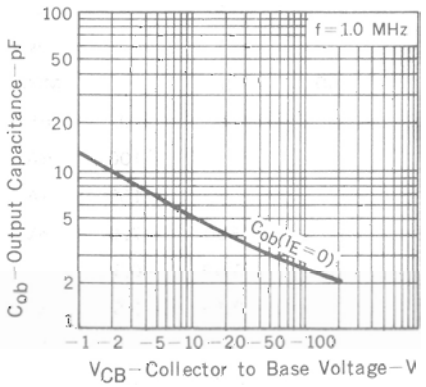
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

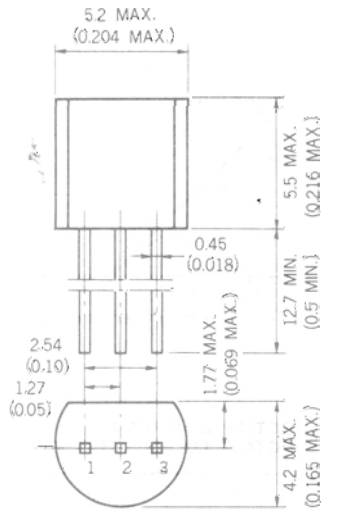
PNP SILICON TRANSISTOR
JE9112

DESCRIPTION The JE9112 is designed for use in output amplifier of portable radios in class B push-pull operation.

FEATURES

- High total power dissipation. (P_T : 2.0 W, T_C = 25 °C)
- High collector current. (I_C : −1.5 A)
- Complementary to JE9113.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation (Ta = 25 °C) . . . . . 1.0 W

Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

Total Power Dissipation (T_C = 25 °C) . . . . . 2.0 W

Thermal Resistance (Ta = 25 °C)
(Junction to Ambient) . . . 156.25 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . −35 V

V_{CEO} Collector to Emitter Voltage . . . . . −25 V

V_{EBO} Emitter to Base Voltage . . . . . −6.0 V

I_C Collector Current . . . . . −1.5 A

I_B Base Current . . . . . −0.5 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	40	180		—	V_{CE} = −1.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	60	180	300	—	V_{CE} = −1.0 V, I_C = −100 mA
h_{FE3}	DC Current Gain	30	110		—	V_{CE} = −1.0 V, I_C = −1000 mA
f_T	Gain Bandwidth Product	10	50		MHz	V_{CE} = −5.0 V, I_C = −10 mA
C_{ob}	Output Capacitance		26		pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−100	nA	V_{CB} = −35 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−100	nA	V_{EB} = −6.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage		−0.96	−1.0	V	V_{CE} = −1.0 V, I_C = −800 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.2	−0.5	V	I_C = −800 mA, I_B = −80 mA
$V_{BE(sat)}$	Base Saturation Voltage		−0.95	−1.2	V	I_C = −800 mA, I_B = −80 mA
BV_{CBO}	Collector to Base Breakdown Voltage	−35			V	I_C = −0.1 mA, I_E = 0
BV_{CEO}	Collector to Emitter Breakdown Voltage	−25			V	I_C = −2.0 mA, I_B = 0
BV_{EBO}	Emitter to Base Breakdown Voltage	−6.0			V	I_E = −0.1 mA, I_C = 0

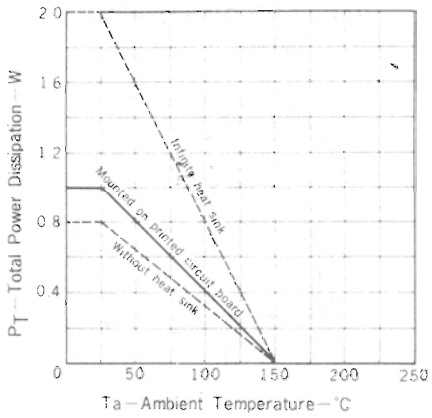
Classification of h_{FE2}

Rank	A	B	C	D
Range	60 – 120	85 – 160	120 – 200	160 – 300

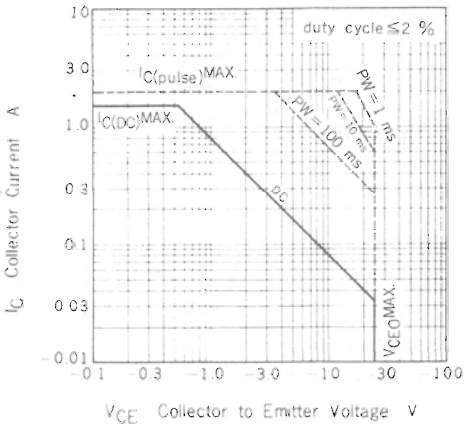
h_{FE} Test Conditions : V_{CE} = −1.0 V, I_C = −100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

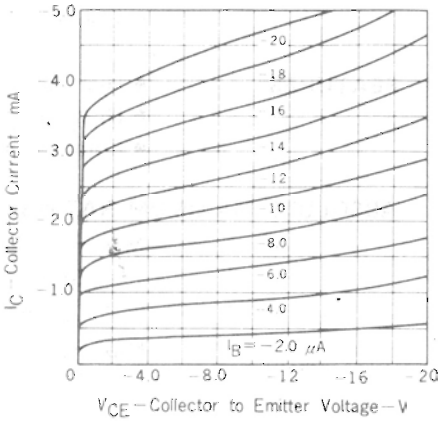
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



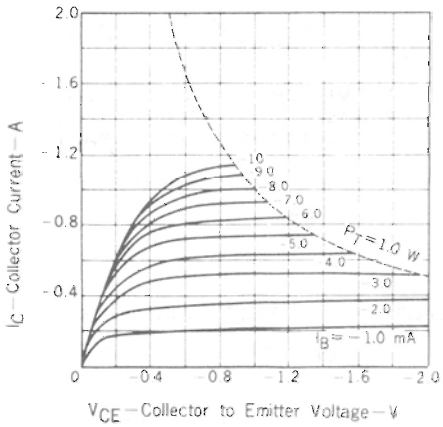
SAFE OPERATING AREA



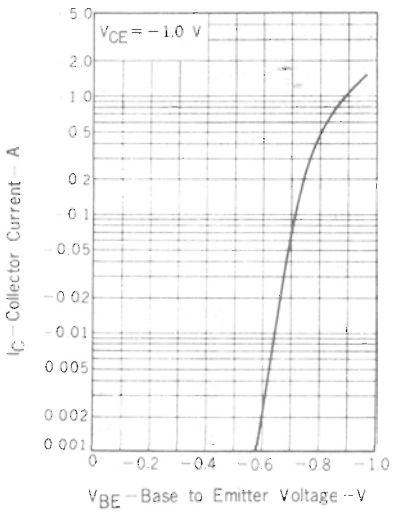
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



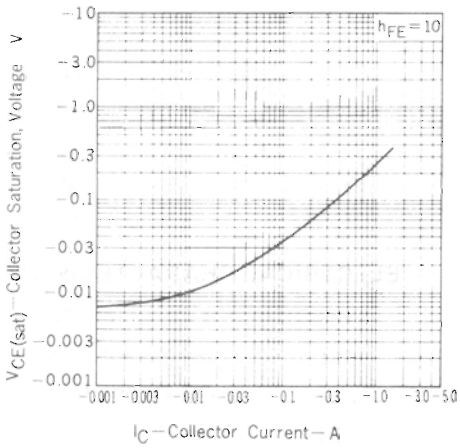
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



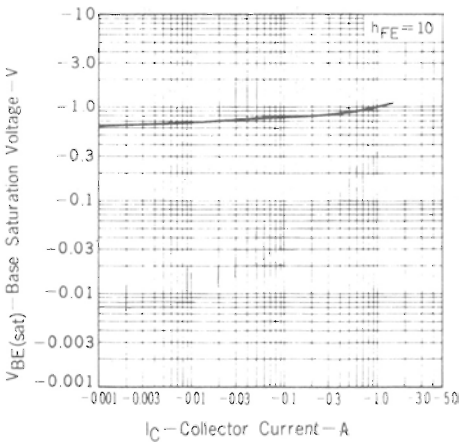
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



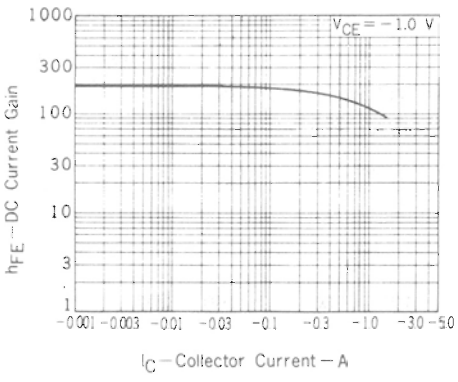
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



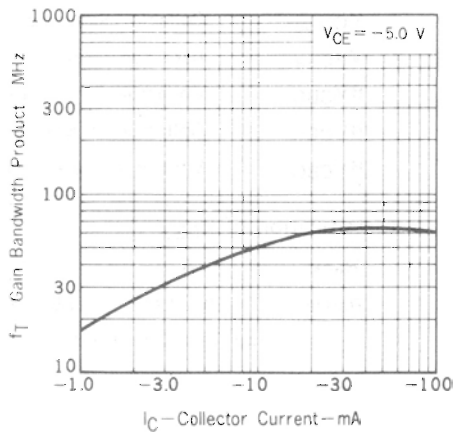
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



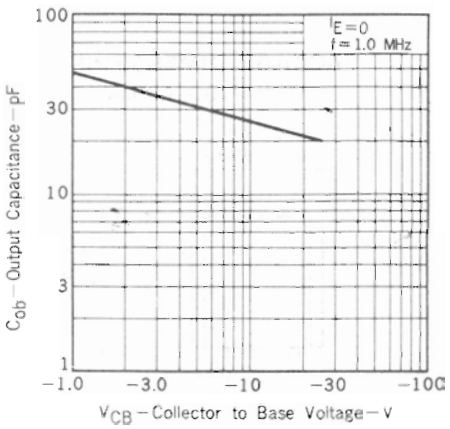
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

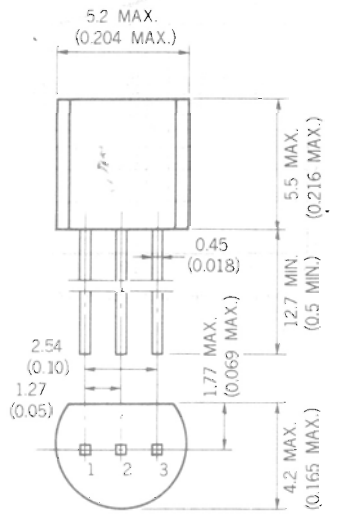
NPN SILICON TRANSISTOR
JE9113

DESCRIPTION The JE9113 is designed for use in output amplifier of portable radios in class B push-pull operation.

FEATURES

- High total power dissipation. (P_T : 2.0 W, T_C=25 °C)
- High collector current. (I_C : 1.5 A)
- Complementary to JE9112.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipations

Total Power Dissipation(Ta = 25 °C) . . . . . 1.0 W

Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

Total Power Dissipation (T_C = 25 °C) . . . . . 2.0 W

Thermal Resistance (Ta=25 °C)
(Junction to Ambient) . . 156.25 °C/W

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . 35 V

V_{CEO} Collector to Emitter Voltage . . . . . 25 V

V_{EBO} Emitter to Base Voltage . . . . . 6.0 V

I_C Collector Current . . . . . 1.5 A

I_B Base Current . . . . . 0.5 A

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	40	170		—	V_{CE}=1.0 V, I_C=5.0 mA
h_{FE2}	DC Current Gain	60	180	300	—	V_{CE}=1.0 V, I_C=100 mA
h_{FE3}	DC Current Gain	30	130		—	V_{CE}=1.0 V, I_C=1000 mA
f_T	Gain Bandwidth Product	30	140		MHz	V_{CE}=5.0 V, I_C=10 mA
C_{ob}	Output Capacitance		17		pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB}=35 V, I_E=0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB}=6.0 V, I_C=0
V_{BE}	Base to Emitter Voltage		0.96	1.0	V	V_{CE}=1.0 V, I_C=800 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.15	0.5	V	I_C=800 mA, I_B=80 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.95	1.2	V	I_C=800 mA, I_B=80 mA
BV_{CBO}	Collector to Base Breakdown Voltage	35			V	I_C=0.1 mA, I_E=0
BV_{CEO}	Collector to Emitter Breakdown Voltage	25			V	I_C=2.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=0.1 mA, I_C=0

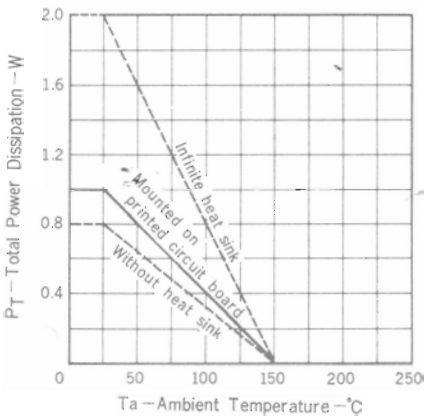
Classification of h_{FE2}

Rank	A	B	C	D
Range	60 – 120	85 – 160	120 – 200	160 – 300

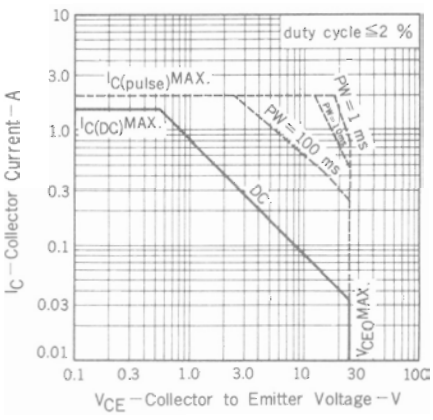
h_{FE2} Test Conditions : V_{CE} = 1.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

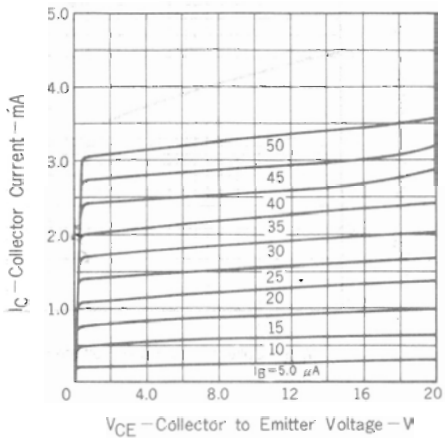
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



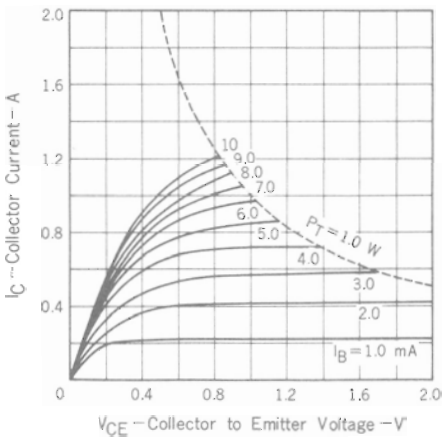
SAFE OPERATING AREA



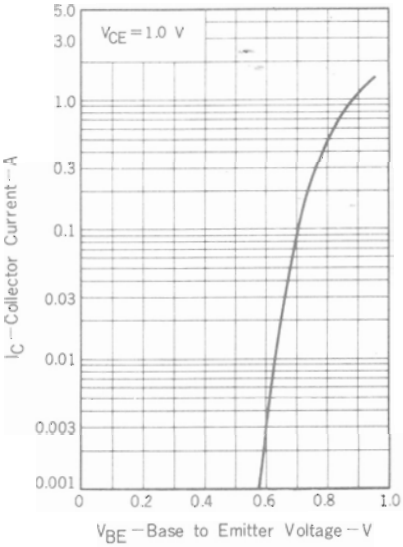
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



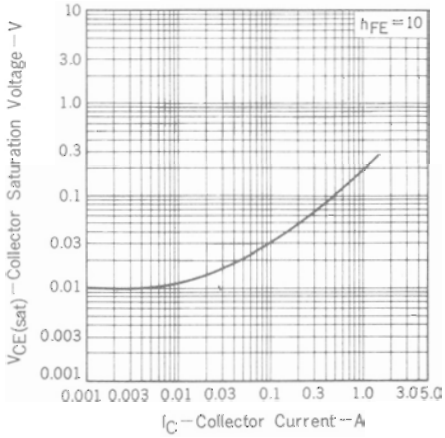
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



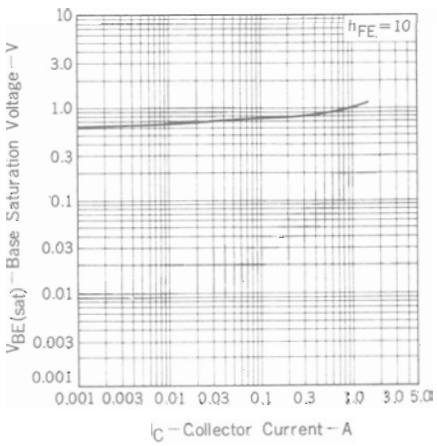
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



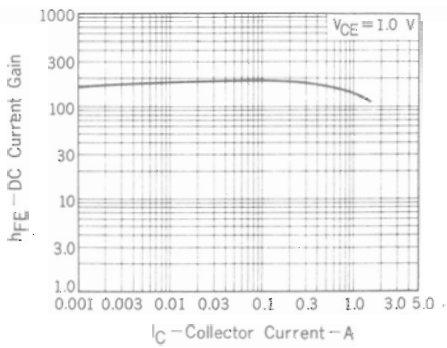
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



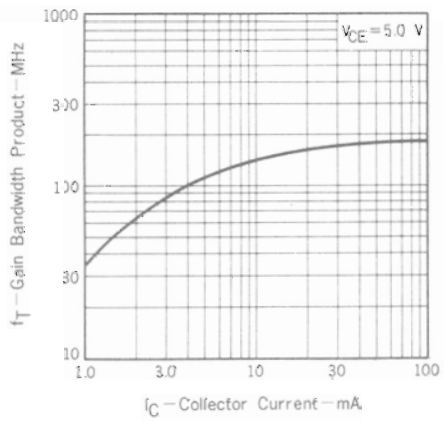
BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



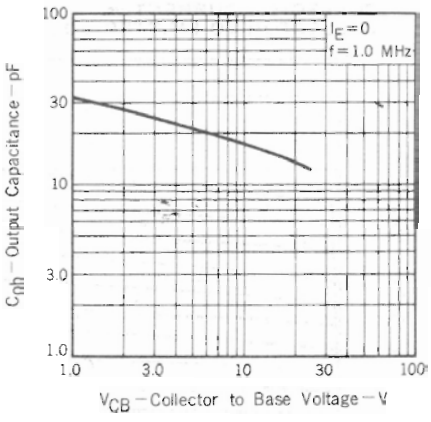
DC CURRENT GAIN vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE9123

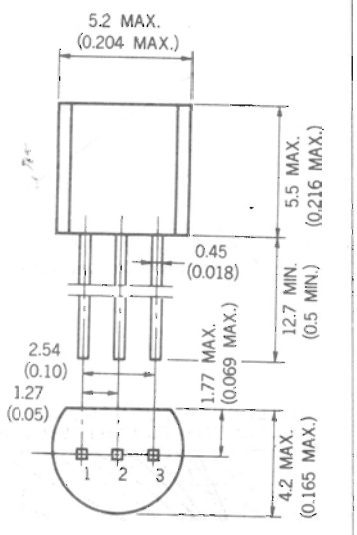
DESCRIPTION

The JE9123 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving, instead of Darlington Transistor, or muting.

FEATURES

- High DC Current Gain.
  h_{FE} = 800 to 3200 (@ V_{CE} = 2.0 V, I_C = 300 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.14 V TYP. (@ I_C/I_B = 300 mA/3.0 mA)
- High V_{EBO} : V_{EBO} = 15V
- Large Current : $I_{C(DC)}$ = 700 mA, $I_{C(pulse)}$ = 1.0 A
- High Total Power Dissipation. : P_T = 0.75 W (T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	25	V
V_{CEO}	Collector to Emitter Voltage	25	V
V_{EBO}	Emitter to Base Voltage	15	V
I_C	Collector Current (DC)	700	mA
I_C	Collector Current (pulse)*	1.0	A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}**	DC Current Gain	800		3200	—	V_{CE} = 2.0 V, I_C = 300 mA
h_{FE2}**	DC Current Gain	640			—	V_{CE} = 2.0 V, I_C = 500 mA
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 5.0 V, I_E = −300 mA
C_{ob}	Output Capacitance		10		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 25 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}**	Base to Emitter Voltage	600		700	mV	V_{CE} = 2.0 V, I_C = 50 mA
$V_{CE(sat)}$**	Collector Saturation Voltage		0.14	0.3	V	I_C = 300 mA, I_B = 3.0 mA
$V_{BE(sat)}$**	Base Saturation Voltage		0.77	1.2	V	I_C = 300 mA, I_B = 3.0 mA
t_{on}	Turn-On Time		0.13		μs	V_{CC} = 10 V, $V_{BE(off)}$ ≒ −2.7 V I_C = 200 mA I_{B1} = −I_{B2} = 4.0 mA
t_{stg}	Storage Time		0.90		μs	
t_{off}	Turn-Off Time		1.1		μs	

**Pulsed PW ≦ 350 μs, Duty Cycle ≦ 2 %

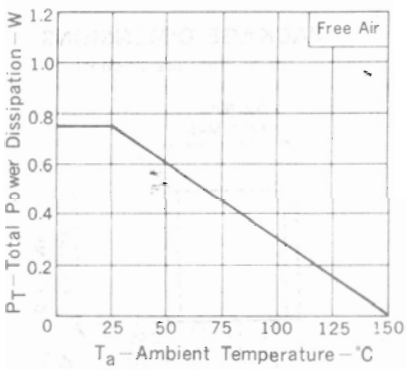
Classification of h_{FE1}

Rank	A	B	C
Range	800 to 1600	1200 to 2400	2000 to 3200

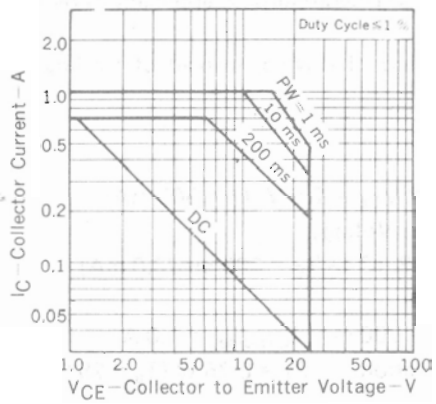
Test Conditions: V_{CE} = 2.0 V, I_C = 300 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

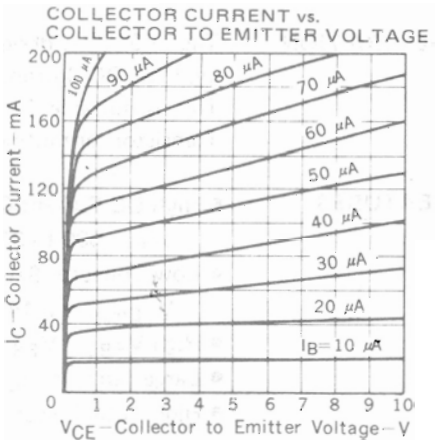
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



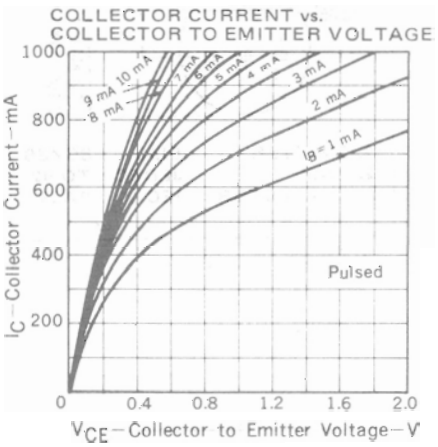
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



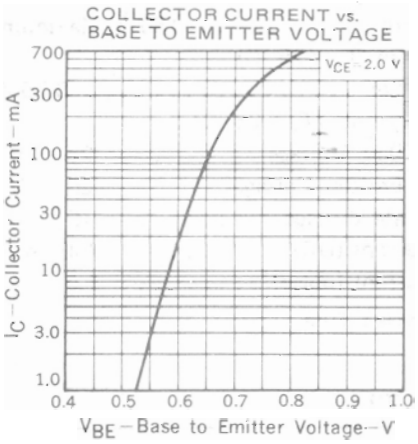
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



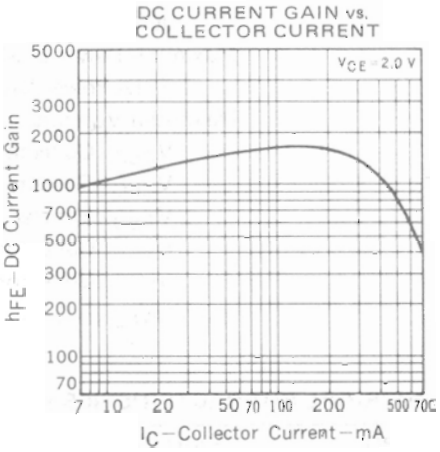
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



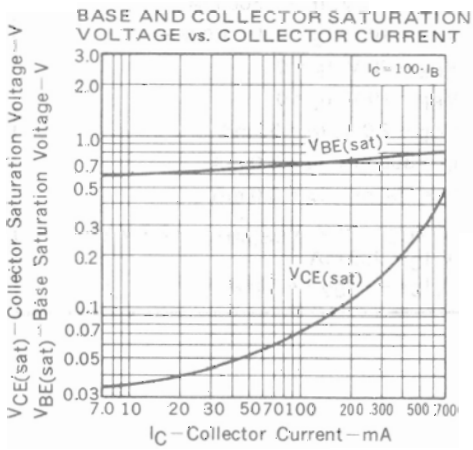
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



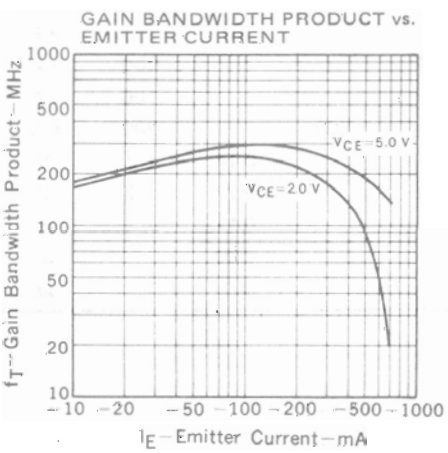
DC CURRENT GAIN vs. COLLECTOR CURRENT



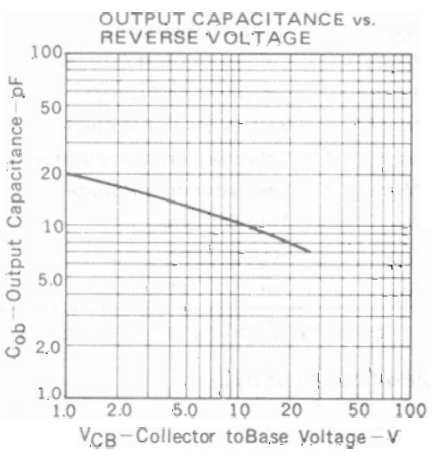
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



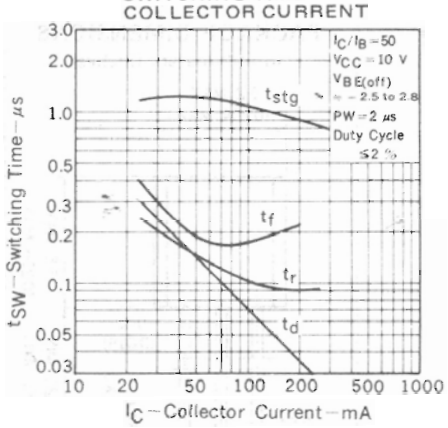
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE9133

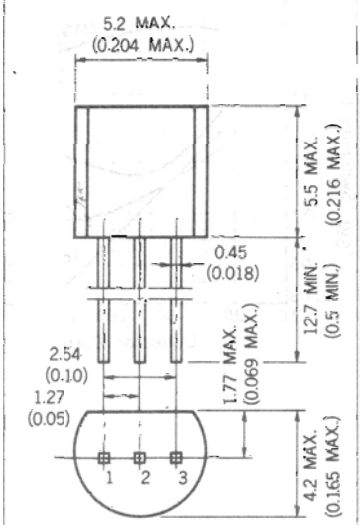
DESCRIPTION

The JE9133 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving, instead of Darlington Transistor, or muting.

FEATURES

- High DC Current Gain.
  h_{FE} = 800 to 3200 (@ V_{CE} = 5.0 V, I_C = 100 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.11 V TYP. (@ I_C/I_B = 100 mA/1.0 mA)
- High V_{EBO} : V_{EBO} = 15 V
- High Total Power Dissipation. : P_T = 0.75 W (@ T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)

V_{CBO}	Collector to Base Voltage	50	V
V_{CEO}	Collector to Emitter Voltage	50	V
V_{EBO}	Emitter to Base Voltage	15	V
I_C	Collector Current (DC)	300	mA
I_C	Collector Current (pulse)*	500	mA

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	800		3200	–	V_{CE} = 5.0 V, I_C = 100 mA
h_{FE2}	DC Current Gain	640			–	V_{CE} = 5.0 V, I_C = 300 mA
f_T	Gain Bandwidth Product	150	220		MHz	V_{CE} = 5.0 V, I_E = −100 mA
C_{ob}	Output Capacitance		8.0		pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 50 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600		700	mV	V_{CE} = 5.0 V, I_C = 100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.11	0.3	V	I_C = 100 mA, I_B = 1.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.7	1.2	V	I_C = 100 mA, I_B = 1.0 mA
t_{on}	Turn-On Time		0.15		μs	(V_{CC} = 10 V, $V_{BE(off)}$ ≒ − 2.7 V, I_C = 200 mA, $I_{B1} = -I_{B2}$ = 4.0 mA)
t_{stg}	Storage Time		0.75		μs	
t_{off}	Turn-Off Time		1.1		μs	

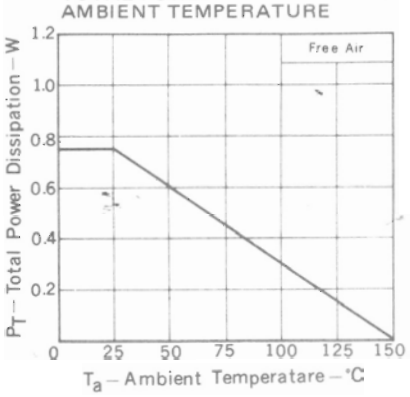
Classification of h_{FE1}

Rank	A	B	C
Range	800 to 1600	1200 to 2400	2000 to 3200

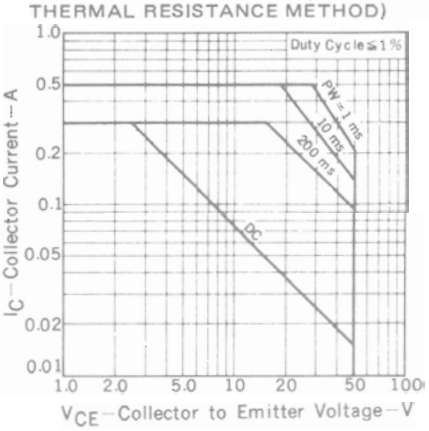
Test Conditions: V_{CE} = 5.0 V, I_C = 100 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

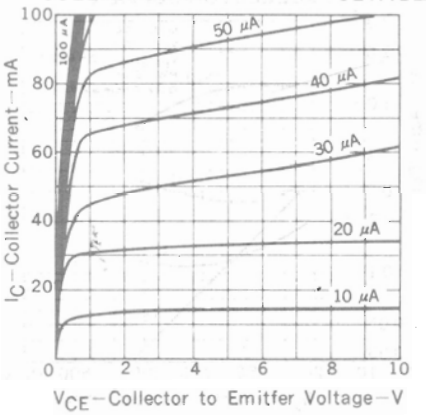
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



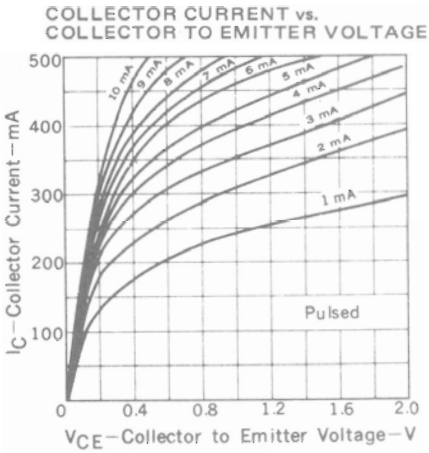
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



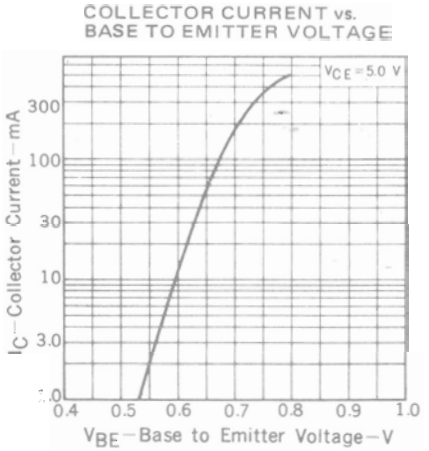
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



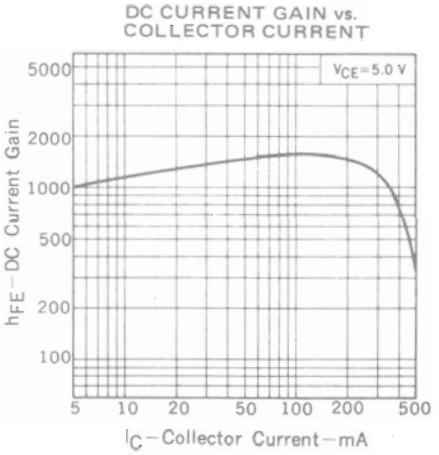
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



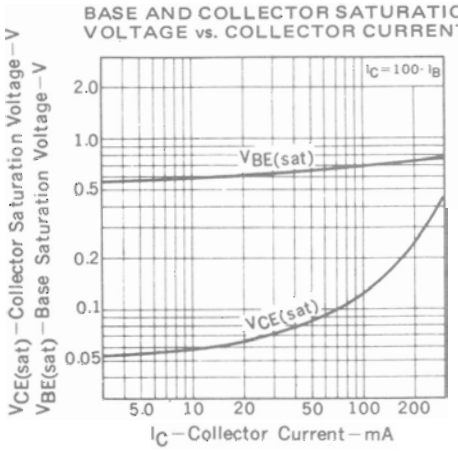
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



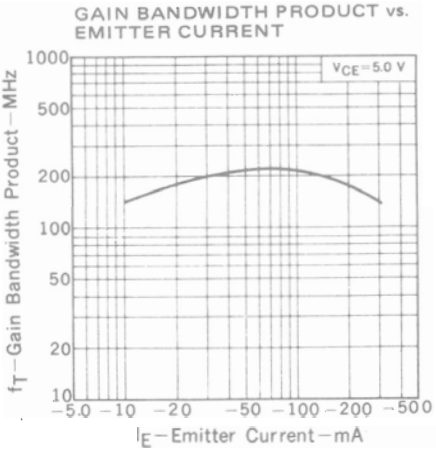
DC CURRENT GAIN vs. COLLECTOR CURRENT



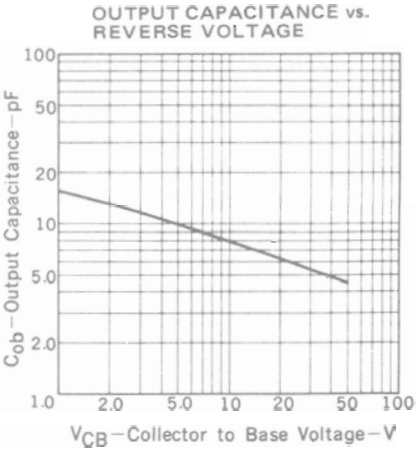
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



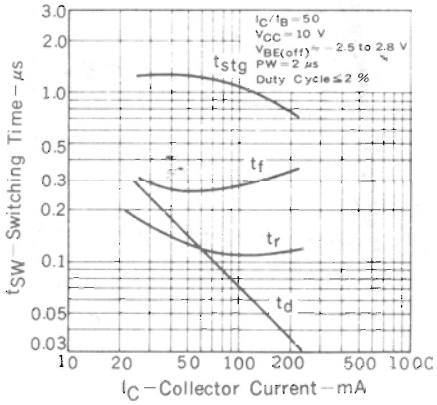
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

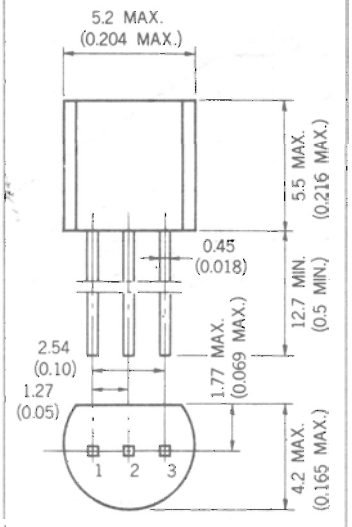
NPN SILICON TRANSISTOR
JE9143

DESCRIPTION The JE9143 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving or muting.

FEATURES

- High DC Current Gain and good h_{FE} linearity.
  h_{FE} = 800 to 3 200 (@ V_{CE} = 5.0 V, I_C = 500 mA)
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.22 V TYP. (@ I_C = 1.0 A, I_B = 10 mA)
- High V_{EBO} : V_{EBO} = 15 V
- High Total Power Dissipation : P_T = 1.0 W, (@ T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 30 V
- V_{CEO} Collector to Emitter Voltage . . . . . 25 V
- V_{EBO} Emitter to Base Voltage . . . . . 15 V
- I_C Collector Current (DC) . . . . . 2.0 A
- I_C Collector Current (pulse)* . . . . . 3.0 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	800	1500	3200	–	V_{CE} = 5.0 V, I_C = 500 mA
h_{FE2}	DC Current Gain	400			–	V_{CE} = 5.0 V, I_C = 2.0 A
f_T	Gain Bandwidth Product	150	350		MHz	V_{CE} = 10 V, I_E = −500 mA
C_{ob}	Output Capacitance		26	35	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 30 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600	630	700	mV	V_{CE} = 5.0 V, I_C = 100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.22	0.30	V	I_C = 1.0 A, I_B = 10 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.90	1.2	V	I_C = 1.0 A, I_B = 10 mA

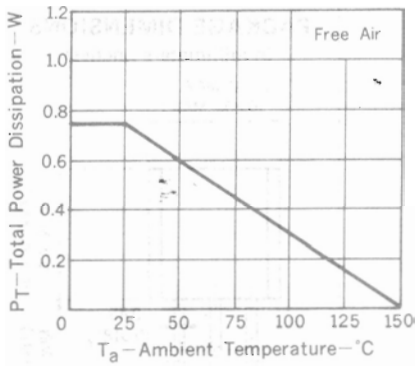
Classification of h_{FE1}

Rank	A	B	C
Range	800 – 1600	1200 – 2400	2000 – 3200

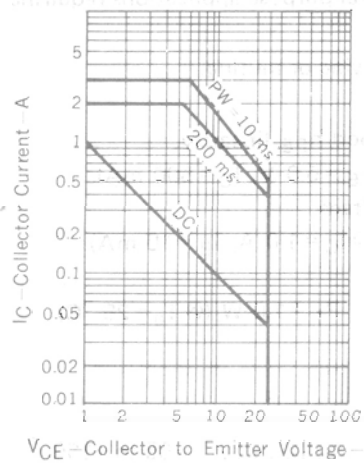
Test Conditions: V_{CE} = 5.0 V, I_C = 500 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

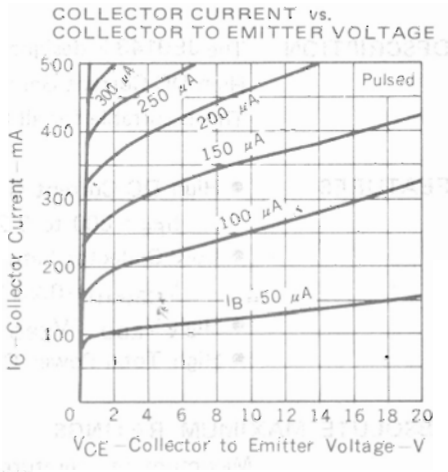
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



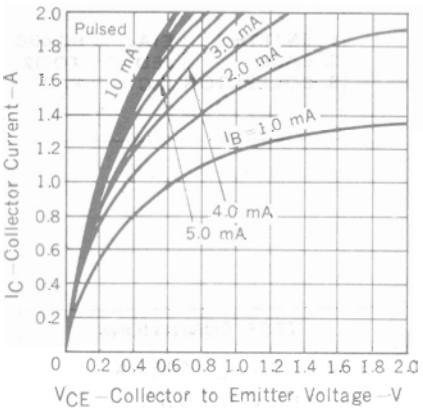
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



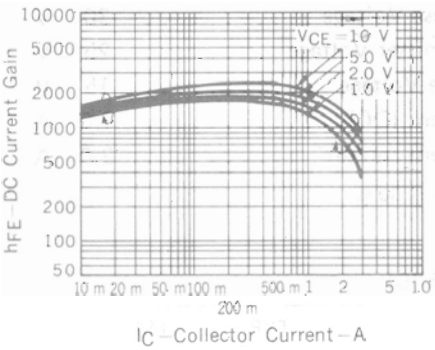
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



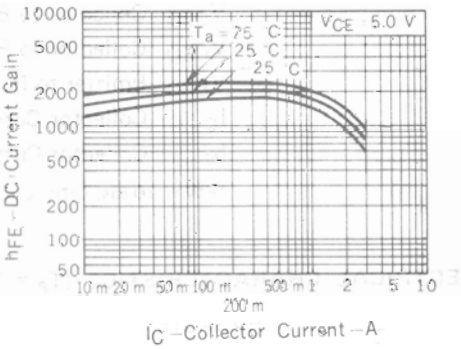
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



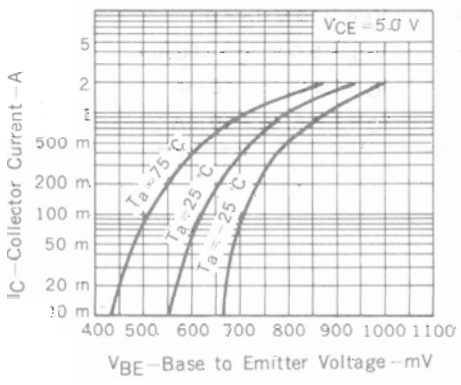
DC CURRENT vs. COLLECTOR CURRENT



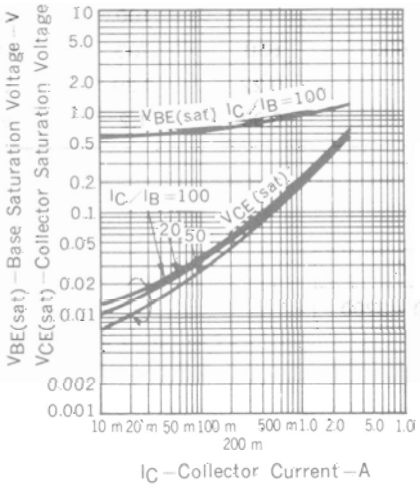
DC CURRENT GAIN vs. COLLECTOR CURRENT



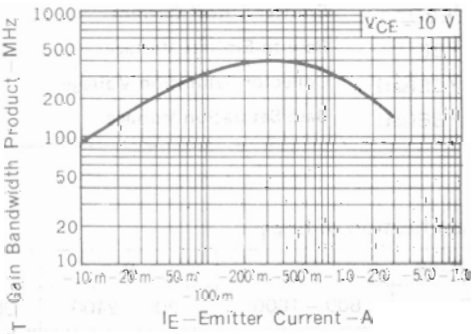
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



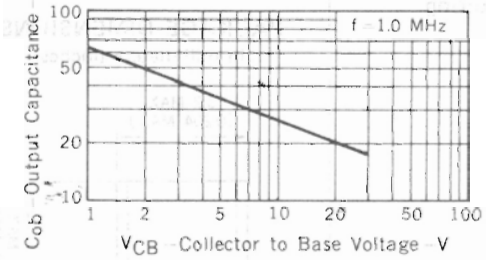
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



NEC
ELECTRON DEVICE

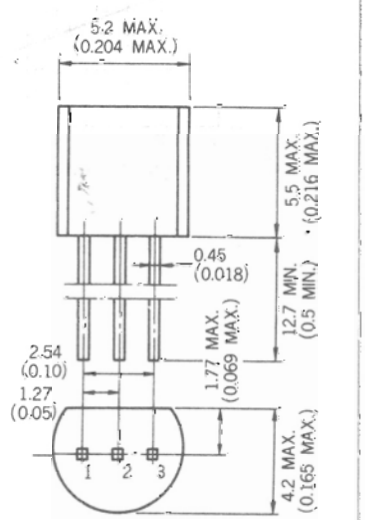
NPN SILICON TRANSISTOR
JE9153

DESCRIPTION The JE9153 is designed for general-purpose applications requiring High DC Current Gain.
This is suitable for all kind of driving or muting.

FEATURES

- High DC Current Gain and good h_{FE} linearity.
  h_{FE} = 800 to 3200 (@ V_{CE} = 5.0 V, I_C = 300 mA)
- High Voltage and Wide "SOA".
  V_{CEO} = 50 V, V_{EBO} = 15 V
- Low Collector Saturation Voltage.
  $V_{CE(sat)}$ = 0.17 V TYP. (@ I_C = 500 mA, I_B = 5.0 mA)
- High Total Power Dissipation : P_T = 1.0 W (@ T_a = 25 °C)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . +150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 0.75 W

Maximum Voltages and Currents (T_a = 25 °C)
- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 15 V
- I_C Collector Current (DC) . . . . . 1.0 A
- I_C Collector Current (pulse)* . . . . . 1.5 A

*PW ≦ 10 ms, Duty Cycle ≦ 50 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE1}	DC Current Gain	800	1500	3200	–	V_{CE} = 5.0 V, I_C = 300 mA
h_{FE2}	DC Current Gain	400			–	V_{CE} = 5.0 V, I_C = 1.0 A
f_T	Gain Bandwidth Product	150	250		MHz	V_{CE} = 10 V, I_E = −500 mA
C_{ob}	Output Capacitance		18	30	pF	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			100	nA	V_{CB} = 60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			100	nA	V_{EB} = 10 V, I_C = 0
V_{BE}	Base to Emitter Voltage	600	630	700	mV	V_{CE} = 5.0 V, I_C = 100 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.17	0.30	V	I_C = 500 mA, I_B = 5.0 mA
$V_{BE(sat)}$	Base Saturation Voltage		0.80	1.2	V	I_C = 500 mA, I_B = 5.0 mA

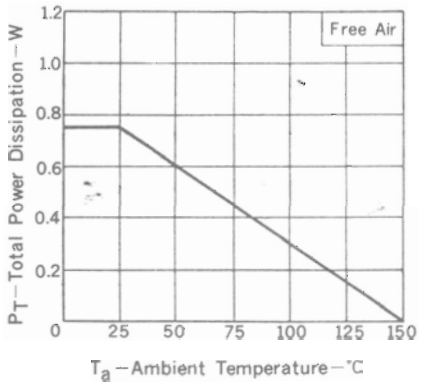
Classification of h_{FE1}

Rank	A	B	C
Range	800 – 1600	1200 – 2400	2000 – 3200

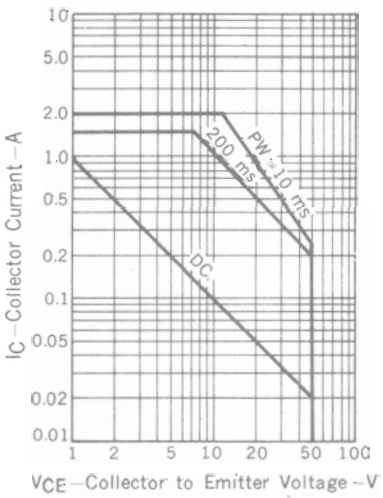
Test Conditions: V_{CE} = 5.0 V, I_C = 300 mA

TYPICAL CHARACTERISTICS (T_a = 25 °C)

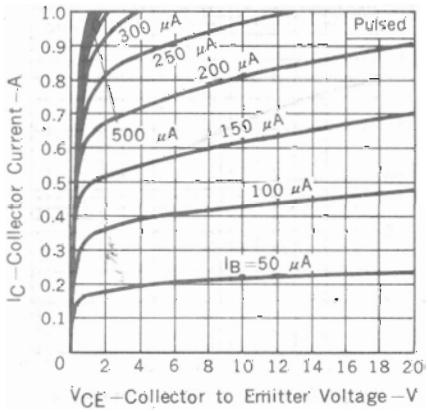
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



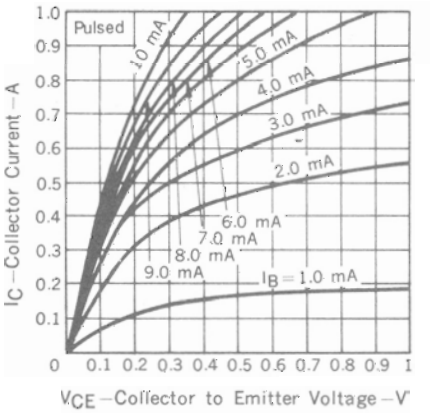
SAFE OPERATING AREAS (TRANSIENT THERMAL RESISTANCE METHOD)



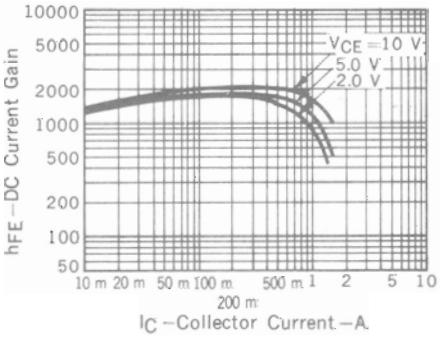
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



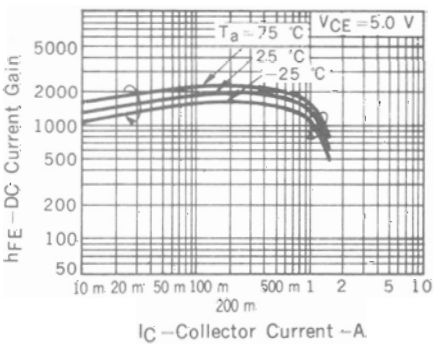
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



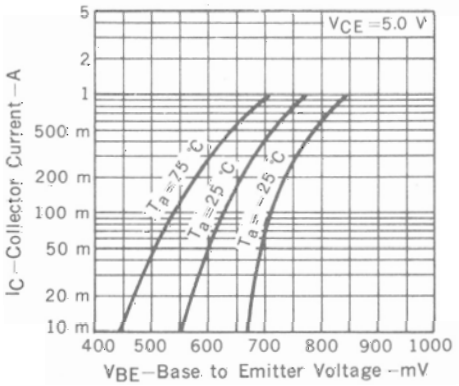
DC CURRENT GAIN vs. COLLECTOR CURRENT



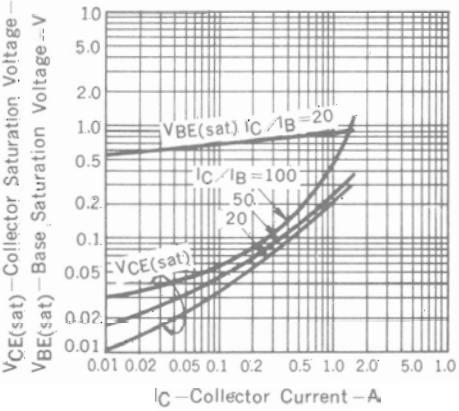
DC CURRENT GAIN vs. COLLECTOR CURRENT



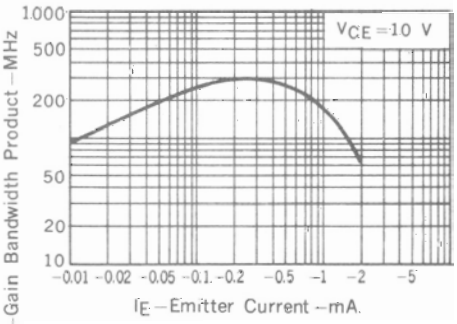
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



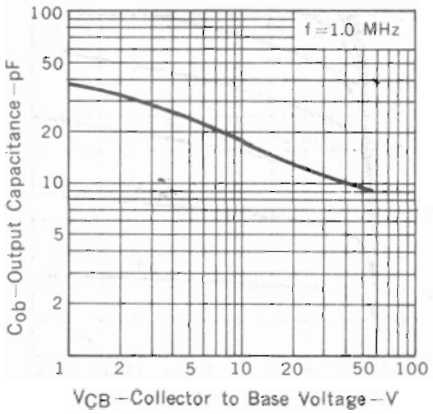
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



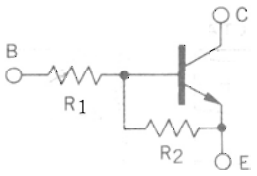
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
JE9214

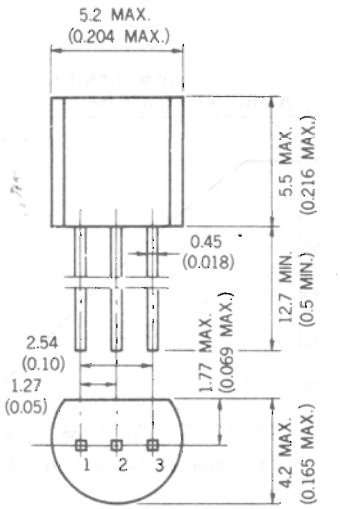
DESCRIPTION The JE9214 is designed for use in medium speed switching circuit.

FEATURE

- Bias resistors built-in type NPN transistor equivalent circuit.



PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . –55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . 60 V
- V_{CEO} Collector to Emitter Voltage . . . . . 50 V
- V_{EBO} Emitter to Base Voltage . . . . . 10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . 100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . 200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0		61.1	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	0.8	1.1	1.5	V	V_{CE} = 5.0 V, I_C = 100 μA
V_{IL}	Low Level Input Voltage	1.0	1.5	5.0	V	V_{CE} = 0.2 V, I_C = 5.0 mA
t_{on}	Turn on Time			1.0	μs	V_{CC} = 5.0 V, R_L = 1.0 kΩ
t_{stg}	Storage Time			2.5	μs	V_{in} = 5.0 V,
t_{off}	Turn off Time			4.0	μs	PW = 2 μs, Duty Cycle ≦ 2 %
h_{FE1}	DC Current Gain	35		340	—	V_{CE} = 5.0 V, I_C = 5.0 mA
h_{FE2}	DC Current Gain	80	200		—	V_{CE} = 5.0 V, I_C = 50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		0.02	0.2	V	I_C = 5.0 mA, I_B = 0.25 mA
I_{CBO}	Collector Cutoff Current			0.1	μA	V_{CB} = 50 V, I_E = 0

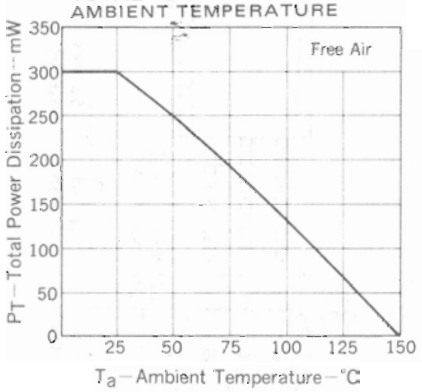
Classification of h_{FE1}, R_1

Rank	A	B	C
h_{FE1} Range	35 to 100	60 to 195	85 to 340
R_1 Range (kΩ)	7.0 to 10 to 13	15.4 to 22.0 to 28.6	32.9 to 47.0 to 61.1

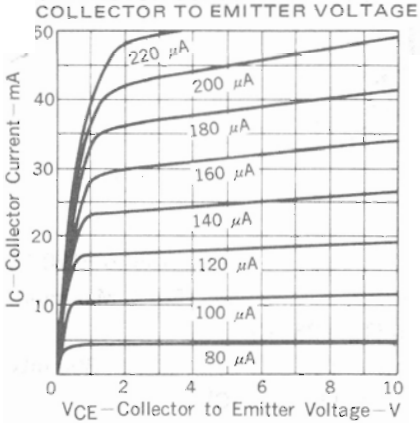
TYPICAL CHARACTERISTICS (T_a = 25 °C)

Rank A

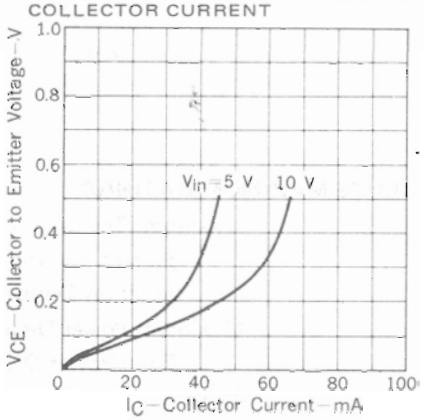
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



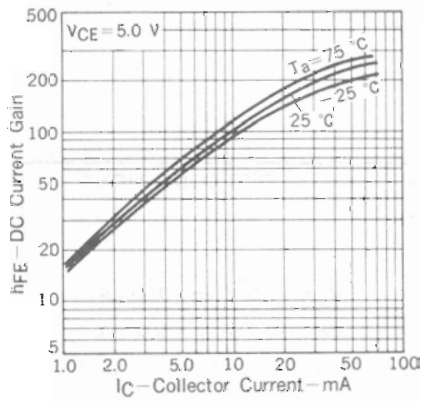
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



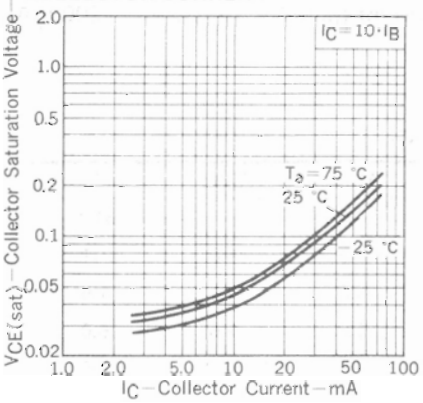
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



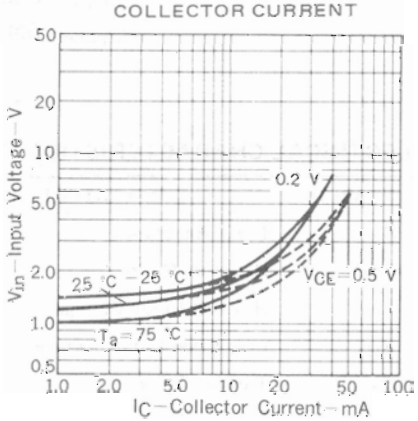
DC CURRENT GAIN vs. COLLECTOR CURRENT



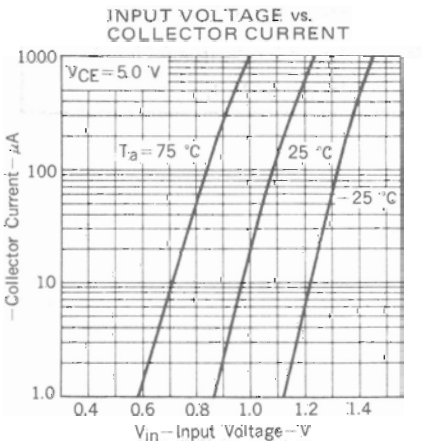
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



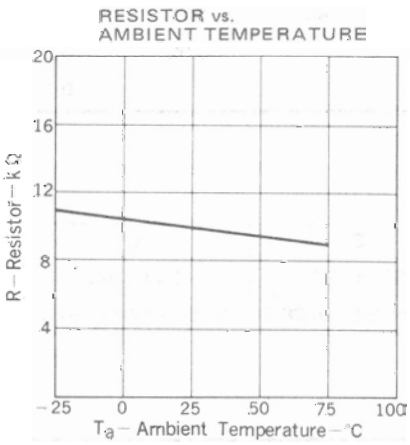
INPUT VOLTAGE vs. COLLECTOR CURRENT



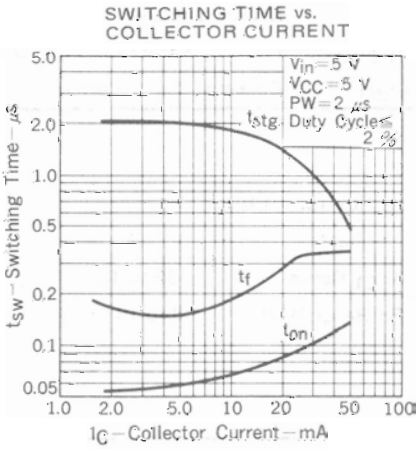
INPUT VOLTAGE vs. COLLECTOR CURRENT



RESISTOR vs. AMBIENT TEMPERATURE

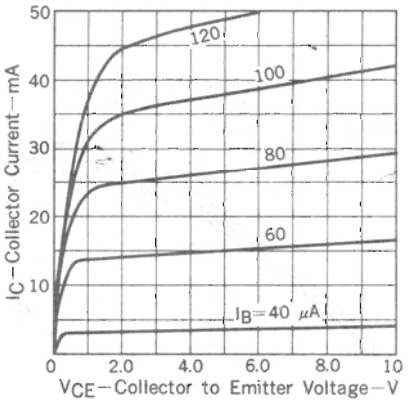


SWITCHING TIME vs. COLLECTOR CURRENT

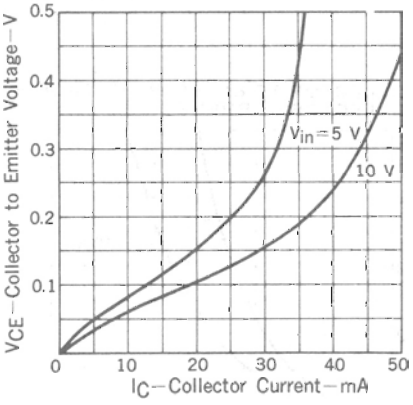


Rank B

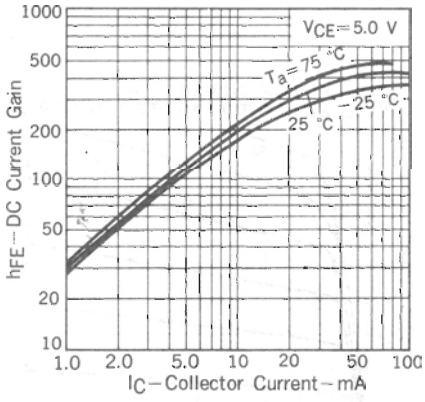
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



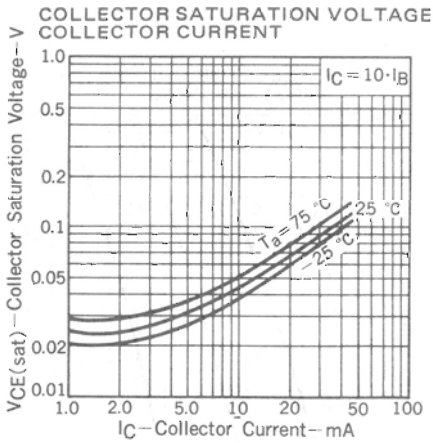
COLLECTOR TO EMITTER VOLTAGE vs.
COLLECTOR CURRENT



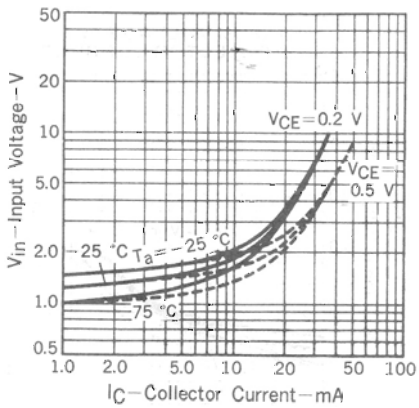
DC CURRENT GAIN vs.
COLLECTOR CURRENT



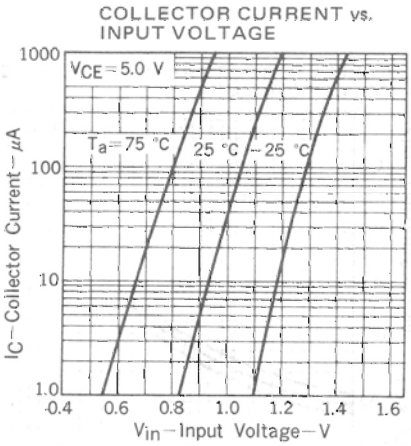
COLLECTOR SATURATION VOLTAGE vs.
COLLECTOR CURRENT



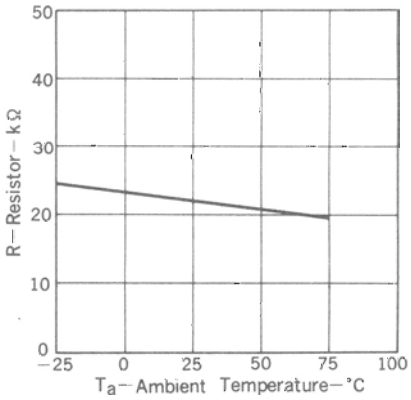
INPUT VOLTAGE vs.
COLLECTOR CURRENT



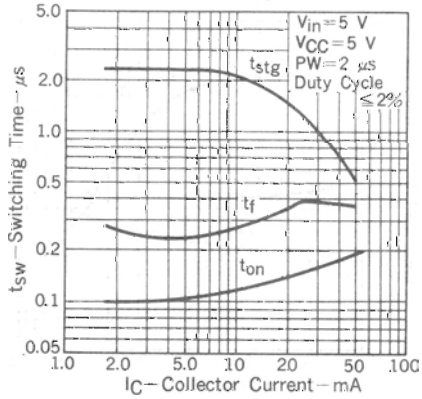
COLLECTOR CURRENT vs.
INPUT VOLTAGE



RESISTOR vs.
AMBIENT TEMPERATURE

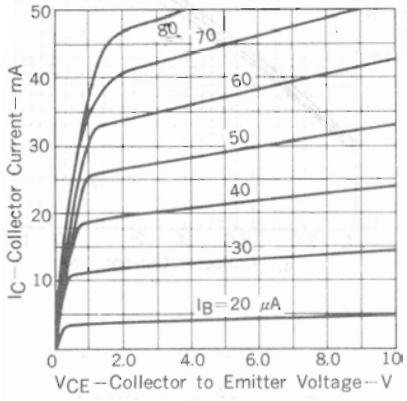


SWITCHING TIME vs.
COLLECTOR CURRENT

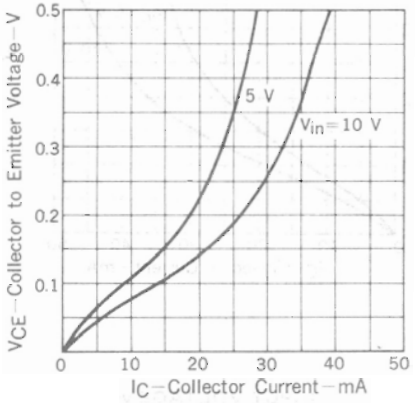


Rank C

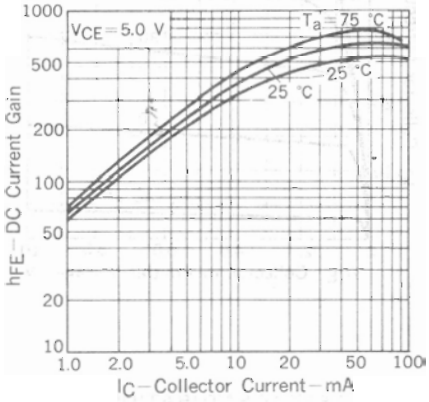
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



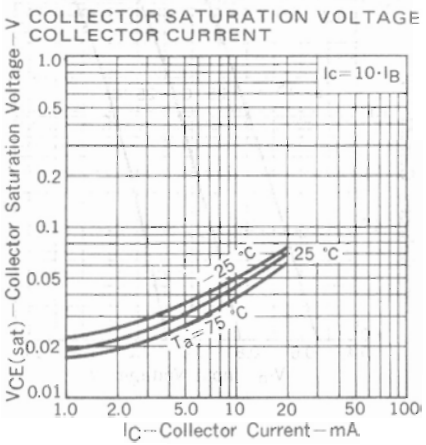
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



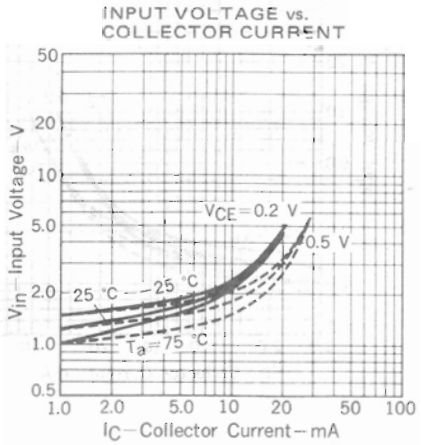
DC CURRENT GAIN vs. COLLECTOR CURRENT



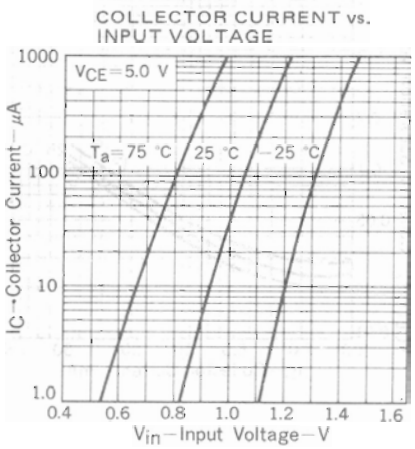
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



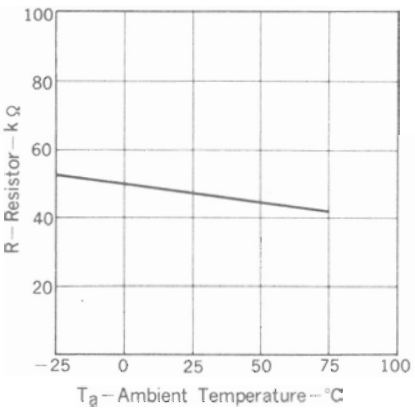
INPUT VOLTAGE vs. COLLECTOR CURRENT



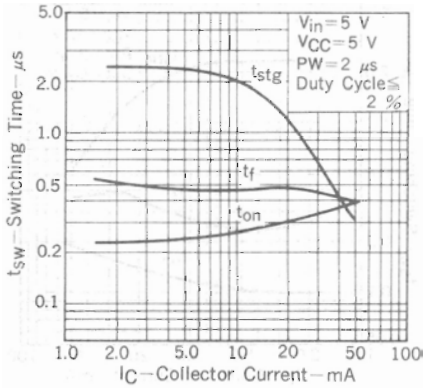
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE



SWITCHING TIME vs. COLLECTOR CURRENT



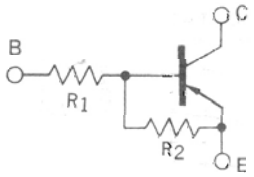
NEC
ELECTRON DEVICE

PNP SILICON TRANSISTOR
JE9215

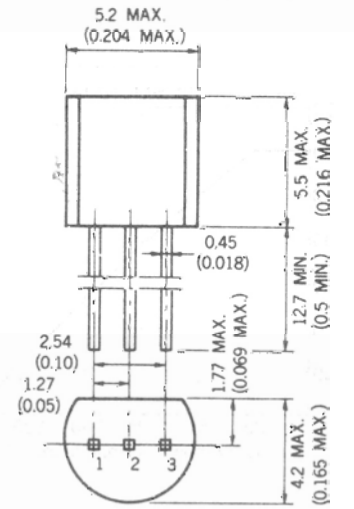
DESCRIPTION The JE9215 is designed for use in medium speed switching circuit.

FEATURE

- Bias resistors built-in type PNP transistor equivalent circuit.



PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −55 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

- Total Power Dissipation . . . . . 300 mW

Maximum Voltages and Currents (T_a = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −50 V
- V_{EBO} Emitter to Base Voltage . . . . . −10 V
- $I_{C(DC)}$ Collector Current (DC) . . . . . −100 mA
- $I_{C(pulse)}$ Collector Current (pulse) . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
R_1	Input Resistance	7.0		61.1	kΩ	
R_1/R_2	Resistors Ratio	0.9	1.0	1.1	—	
V_{IH}	Hi Level Input Voltage	−0.8	−1.1	−1.5	V	V_{CE} = −5.0 V, I_C = −100 μA
V_{IL}	Low Level Input Voltage	−1.0	−1.5	−5.0	V	V_{CE} = −0.2 V, I_C = −5.0 mA
t_{on}	Turn on Time			1.0	μs	V_{CC} = −5.0 V, R_L = 1.0 kΩ, V_{in} = −5.0 V, PW = 2 μs, Duty Cycle ≦ 2 %
t_{stg}	Storage Time			2.5	μs	
t_{off}	Turn off Time			3.0	μs	
h_{FE1}	DC Current Gain	35		340	—	V_{CE} = −5.0 V, I_C = −5.0 mA
h_{FE2}	DC Current Gain	80			—	V_{CE} = −5.0 V, I_C = −50 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.02	−0.2	V	I_C = −5.0 mA, I_B = −0.25 mA
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −50 V, I_E = 0

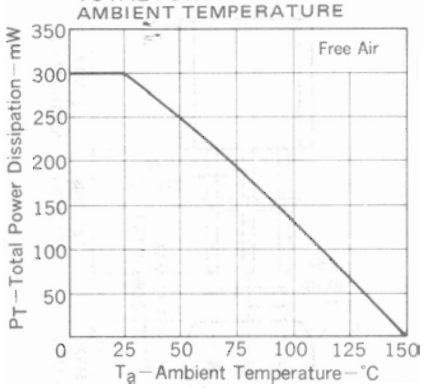
Classification of h_{FE1}, R_1

Rank	A	B	C
h_{FE1} Range	35 to 100	60 to 195	85 to 340
R_1 Range (kΩ)	7.0 to 10 to 13	15.4 to 22.0 to 28.6	32.9 to 47.0 to 61.1

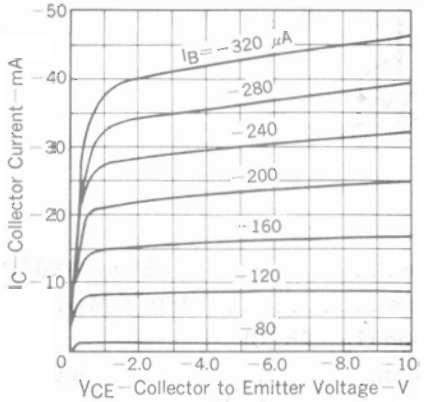
TYPICAL CHARACTERISTICS (T_a = 25 °C)

Rank A

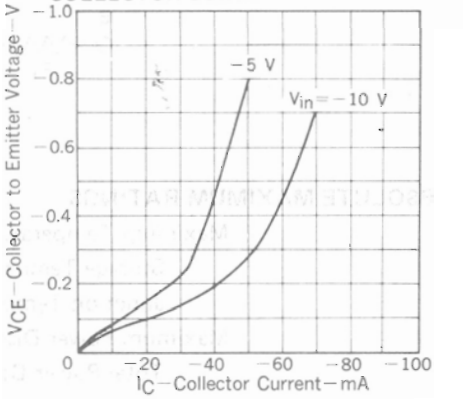
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



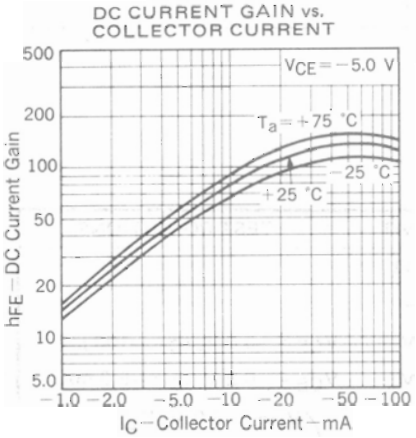
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



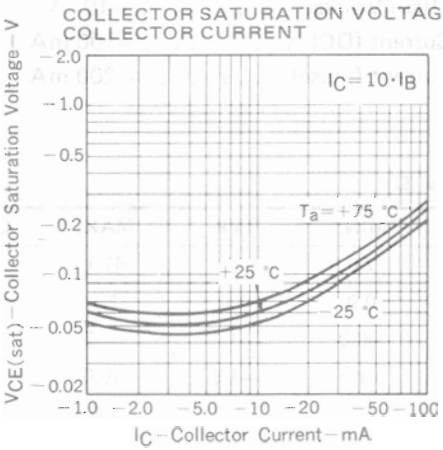
COLLECTOR TO EMITTER VOLTAGE vs. COLLECTOR CURRENT



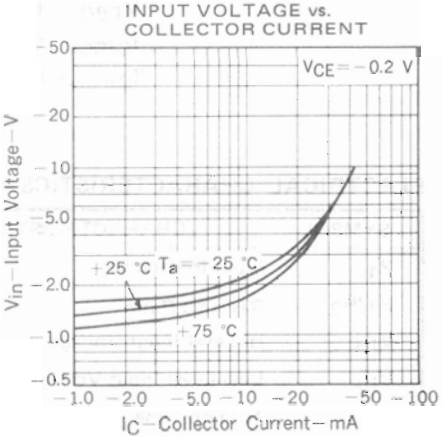
DC CURRENT GAIN vs. COLLECTOR CURRENT



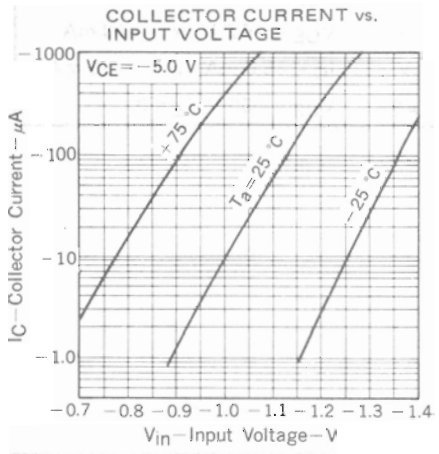
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



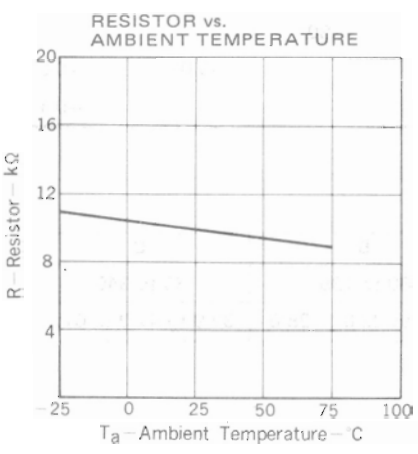
INPUT VOLTAGE vs. COLLECTOR CURRENT



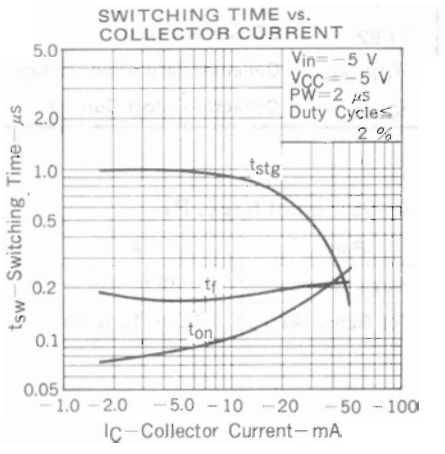
COLLECTOR CURRENT vs. INPUT VOLTAGE



RESISTOR vs. AMBIENT TEMPERATURE

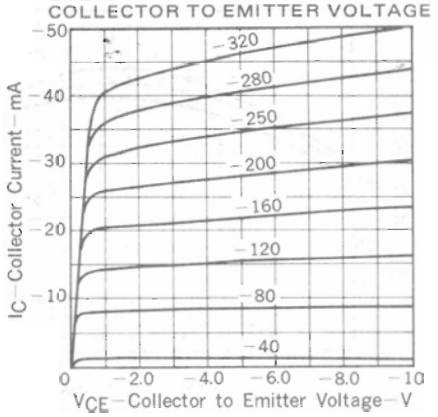


SWITCHING TIME vs. COLLECTOR CURRENT

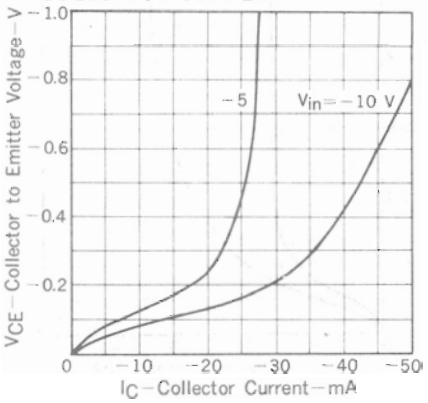


Rank B

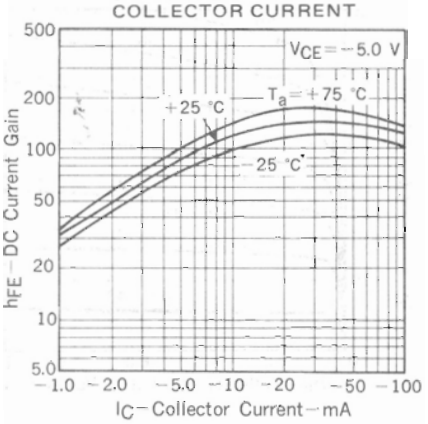
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



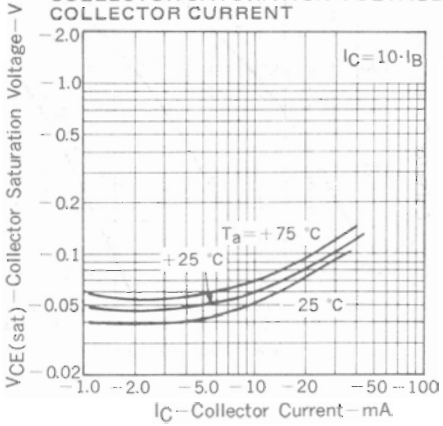
COLLECTOR TO EMITTER VOLTAGE vs.
COLLECTOR CURRENT



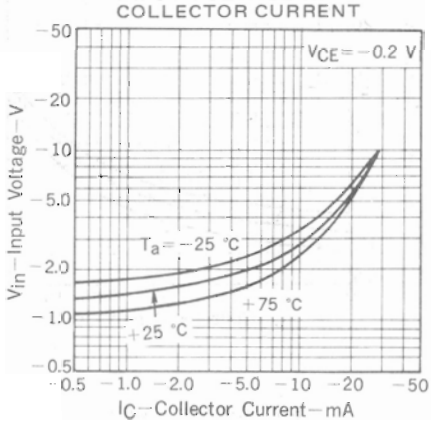
DC CURRENT GAIN vs.
COLLECTOR CURRENT



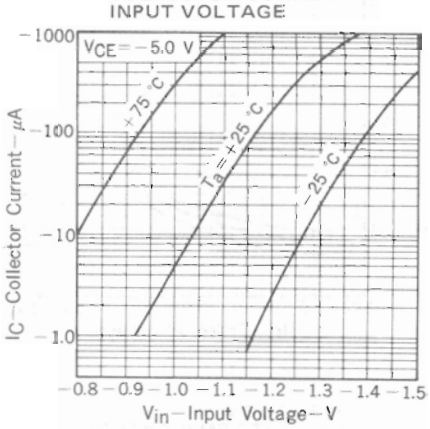
COLLECTOR SATURATION VOLTAGE vs.
COLLECTOR CURRENT



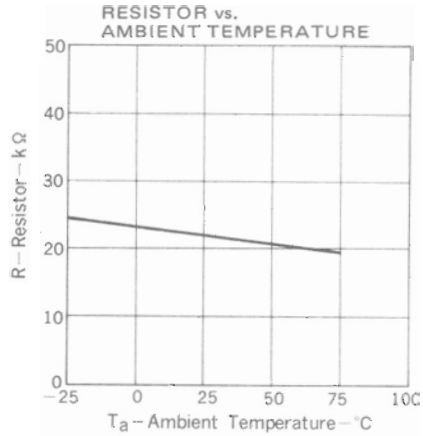
INPUT VOLTAGE vs.
COLLECTOR CURRENT



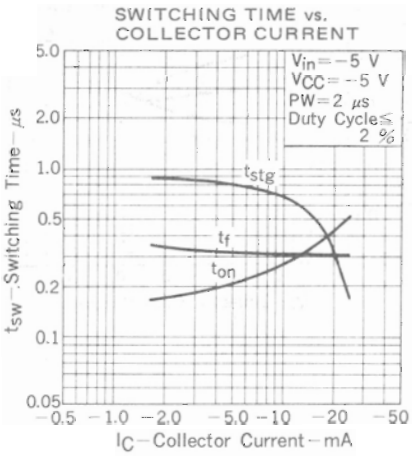
COLLECTOR CURRENT vs.
INPUT VOLTAGE



RESISTOR vs.
AMBIENT TEMPERATURE

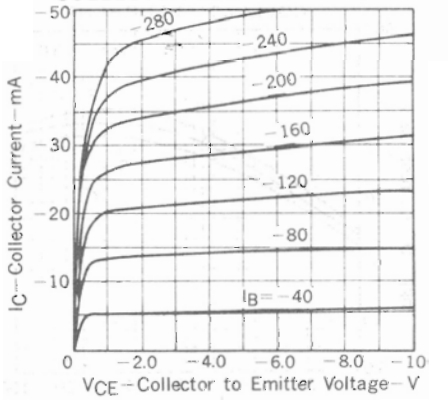


SWITCHING TIME vs.
COLLECTOR CURRENT

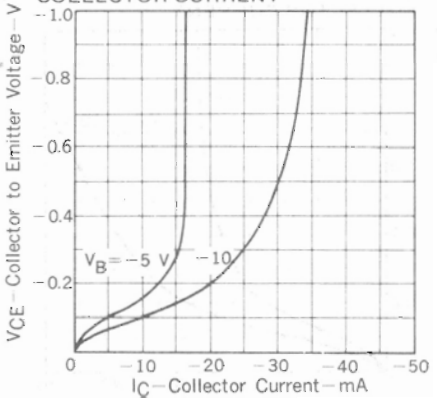


Rank C

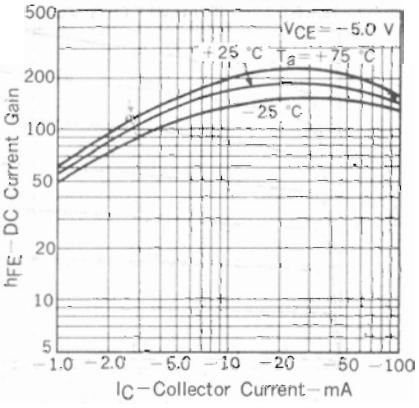
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



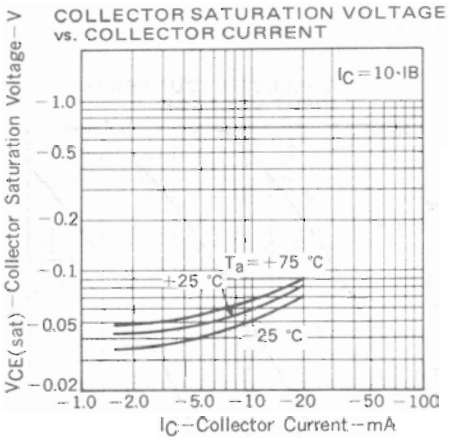
COLLECTOR TO EMITTER VOLTAGE vs.
COLLECTOR CURRENT



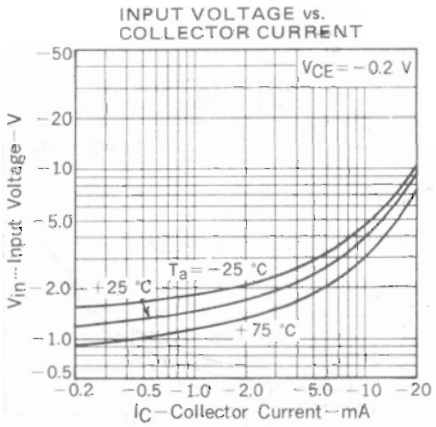
DC CURRENT GAIN vs.
COLLECTOR CURRENT



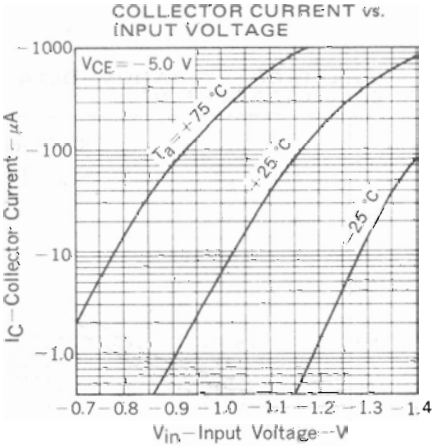
COLLECTOR SATURATION VOLTAGE
vs. COLLECTOR CURRENT



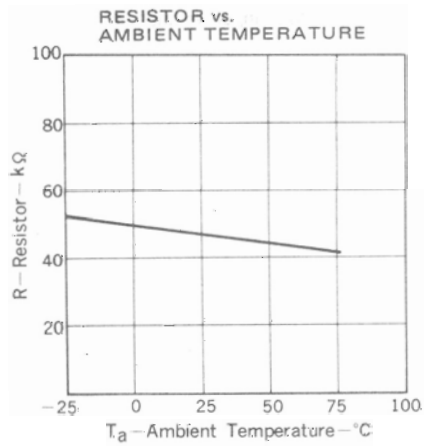
INPUT VOLTAGE vs.
COLLECTOR CURRENT



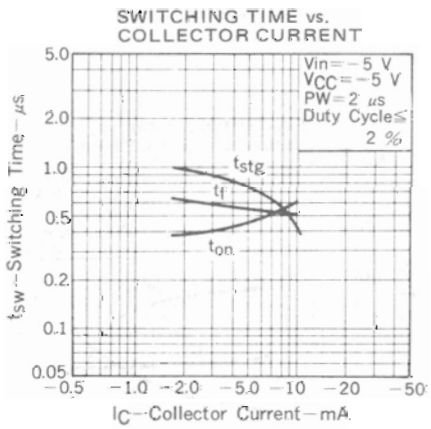
COLLECTOR CURRENT vs.
INPUT VOLTAGE



RESISTOR vs.
AMBIENT TEMPERATURE



SWITCHING TIME vs.
COLLECTOR CURRENT



NEC
ELECTRON DEVICE

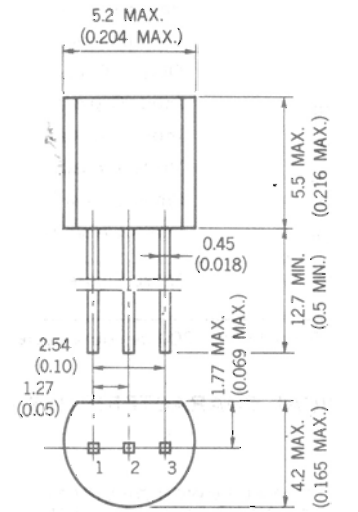
NPN SILICON TRANSISTOR
2N3903

DESCRIPTION The 2N3903 is designed for general purpose switching and amplifier application.

FEATURES

- High Power : P_T 625 mW at 25 °C
- High Voltage : V_{CEO} 40 V
- For Complementary Use with PNP Type 2N3905

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	60 V
V_{CEO}	Collector to Emitter Voltage	40 V
V_{EBO}	Emitter to Base Voltage	6.0 V
I_C	Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			35	ns	V_{CC}=3 V, V_{BB}=−0.5 V
t_r	Rise Time			35	ns	I_C=10 mA, I_{B1}=1.0 mA
t_{stg}	Storage Time			175	ns	V_{CC}=3 V, I_C=10 mA
t_f	Fall Time			50	ns	I_{B1}=−I_{B2}=1 mA
h_{FE1}*	DC Current Gain	20	80		—	V_{CE}=1.0 V, I_C=100 μA
h_{FE2}*	DC Current Gain	35	100		—	V_{CE}=1.0 V, I_C=1 mA
h_{FE3}*	DC Current Gain	50	110	150	—	V_{CE}=1.0 V, I_C=10 mA
h_{FE4}*	DC Current Gain	30	110		—	V_{CE}=1.0 V, I_C=50 mA
h_{FE5}*	DC Current Gain	15	80		—	V_{CE}=1.0 V, I_C=100 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.10	0.2	V	I_C=10 mA, I_B=1.0 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.15	0.3	V	I_C=50 mA, I_B=5.0 mA

* Pulsed PW ≦300 μs, duty cycle ≦2 %

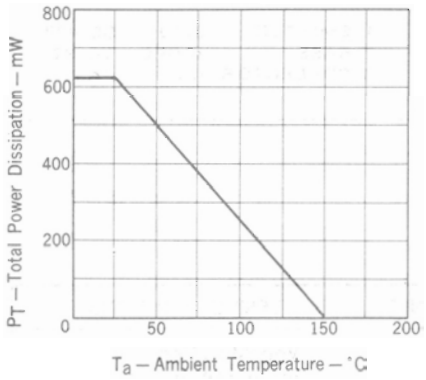
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			50	nA	V_{CE}=30 V, V_{BE}=−3 V
I_{BEX}	Base Cutoff Current			−50	nA	V_{CE}=30 V, V_{BE}=−3 V
BV_{CBO}	Collector to Base Breakdown Voltage	60			V	I_C=10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	40			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	0.65	0.72	0.85	V	I_C=10 mA, I_B=1.0 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		0.80	0.95	V	I_C=50 mA, I_B=5.0 mA
f_T	Gain Bandwidth Product	250	500		MHz	V_{CE}=20 V, I_C=10 mA
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		6.5	8.0	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	1.0	3.5	8	kΩ	V_{CE}=10 V, I_C=1 mA, f=1 kHz
h_{re}	Voltage Feedback Ratio	0.1	3.5	5.0	$\times 10^{-4}$	V_{CE}=10 V, I_C=1 mA, f=1 kHz
h_{fe}	Small Signal Current Gain	50	120	200	—	V_{CE}=10 V, I_C=1 mA, f=1 kHz
h_{oe}	Output Admittance	1.0	12	40	μS	V_{CE}=10 V, I_C=1 mA, f=1 kHz
NF	Noise Figure			6.0	dB	V_{CE}=5.0 V, I_C=0.1 mA, R_G=1 kΩ, f=10 Hz to 15.7 kHz

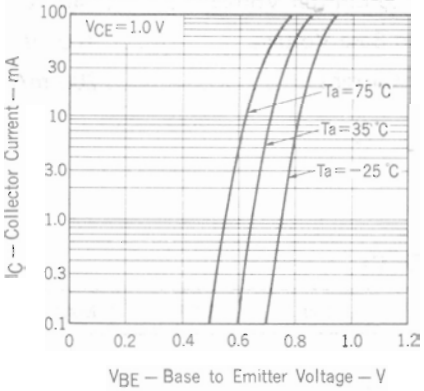
* Pulsed PW ≤300 μs, duty cycle ≤2%

TYPICAL CHARACTERISTICS (Ta=25 °C)

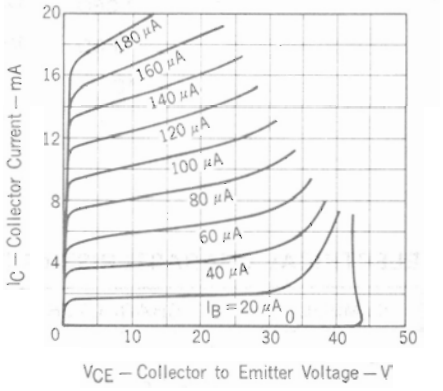
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



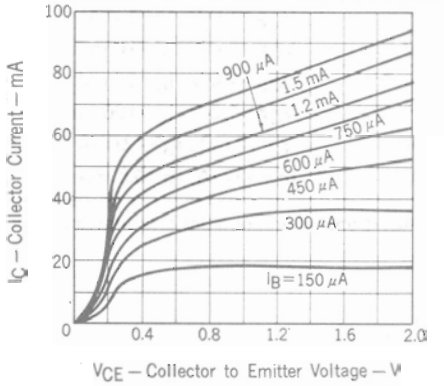
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



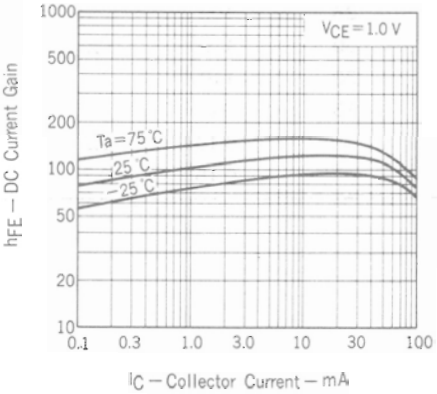
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



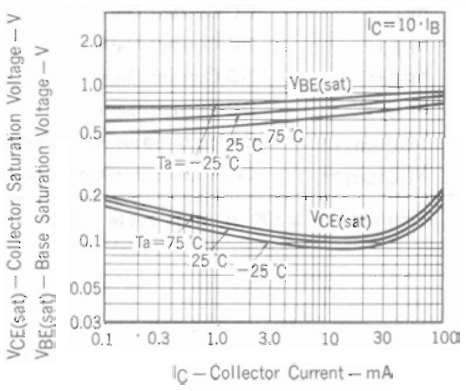
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



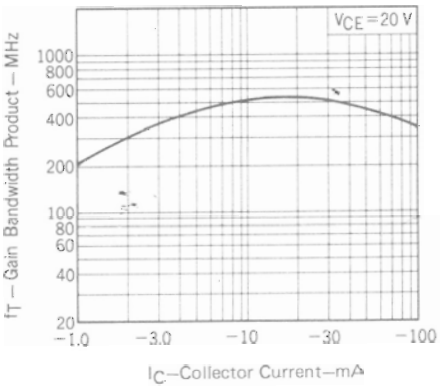
DC CURRENT GAIN vs. COLLECTOR CURRENT



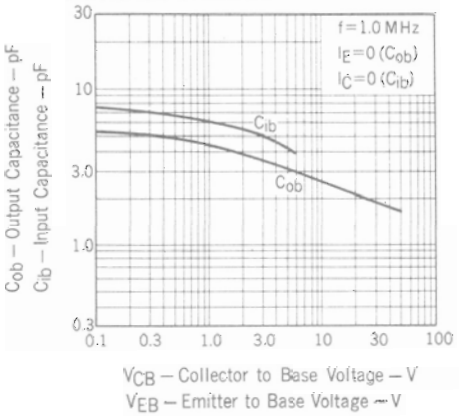
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



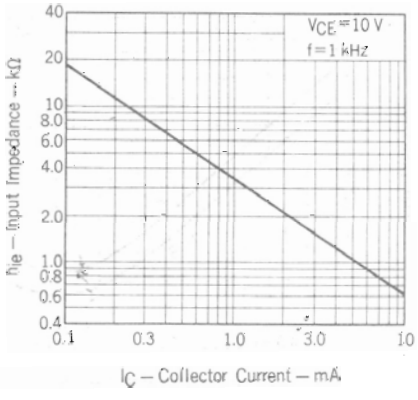
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



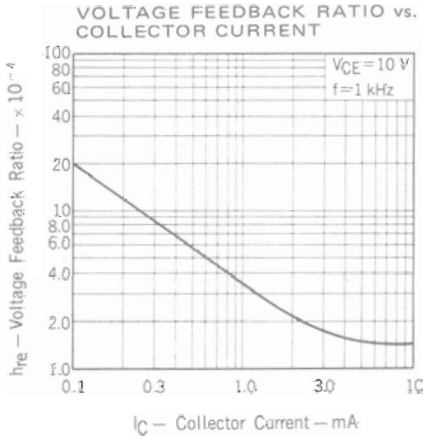
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



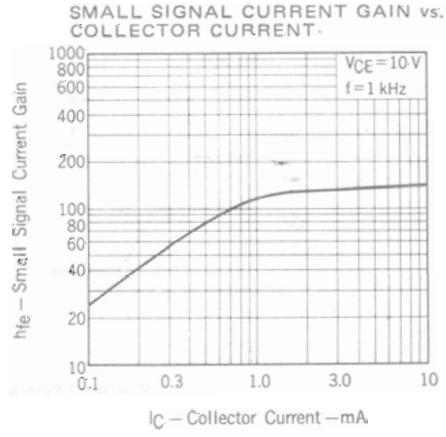
INPUT IMPEDANCE vs. COLLECTOR CURRENT



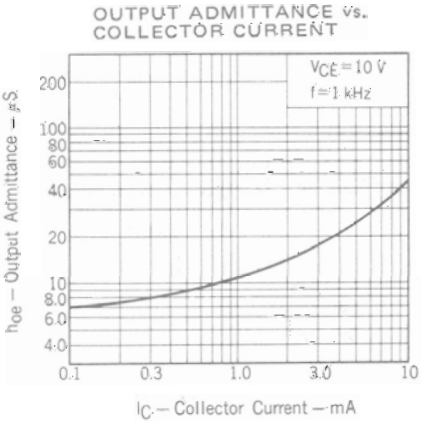
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



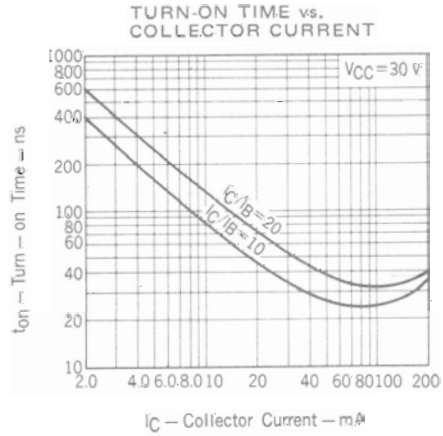
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



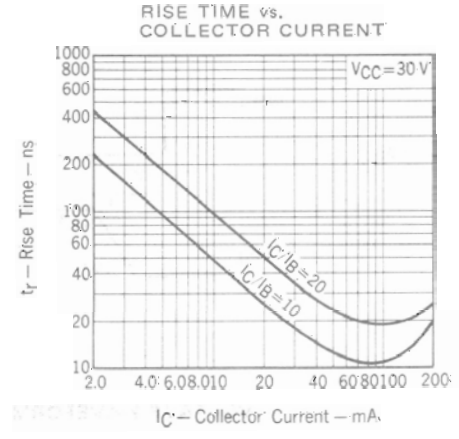
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



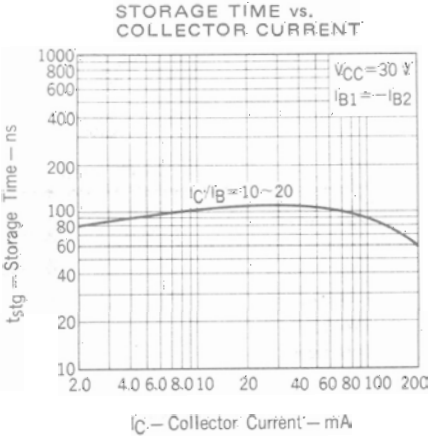
TURN-ON TIME vs. COLLECTOR CURRENT

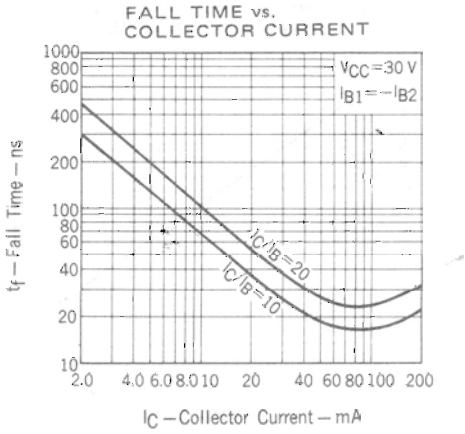


RISE TIME vs. COLLECTOR CURRENT

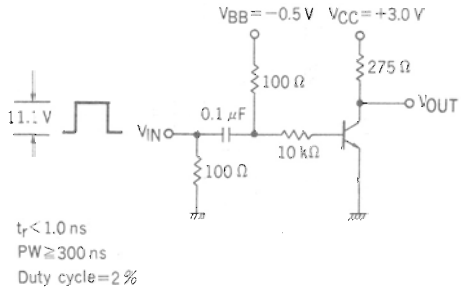


STORAGE TIME vs. COLLECTOR CURRENT

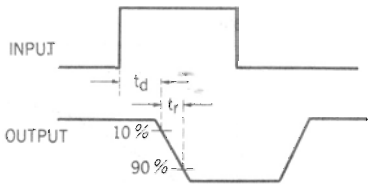




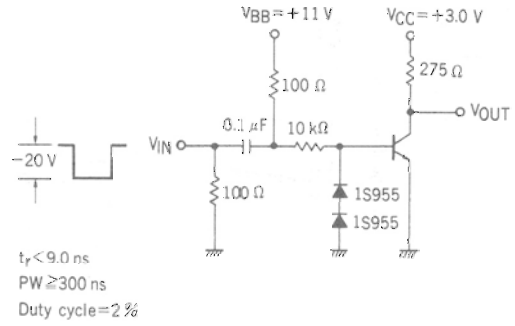
SWITCHING TIME TEST CIRCUIT



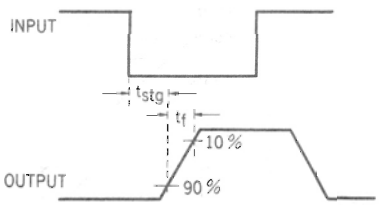
t_{on} SWITCHING



'E WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

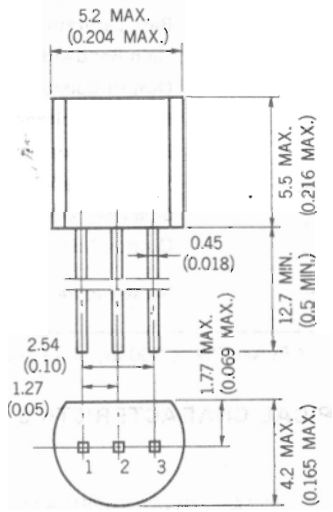
NPN SILICON TRANSISTOR
2N3904

DESCRIPTION The 2N3904 is designed for general purpose switching and amplifier application.

FEATURES

- High Power : P_T 625 mW at 25 °C
- High Voltage : V_{CEO} 40 V
- For Complementary Use with PNP Type 2N3906

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	60 V
V_{CEO}	Collector to Emitter Voltage	40 V
V_{EBO}	Emitter to Base Voltage	6.0 V
I_C	Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			35	ns	V_{CC}=3 V, V_{BB}=−0.5 V
t_r	Rise Time			35	ns	I_C=10 mA, I_{B1}=1.0 mA
t_{stg}	Storage Time			200	ns	V_{CC}=3 V, I_C=10 mA
t_f	Fall Time			50	ns	I_{B1}=−I_{B2}=1 mA
h_{FE1}*	DC Current Gain	40	150		—	V_{CE}=1.0 V, I_C=100 μA
h_{FE2}*	DC Current Gain	70	180		—	V_{CE}=1.0 V, I_C=1 mA
h_{FE3}*	DC Current Gain	100	200	300	—	V_{CE}=1.0 V, I_C=10 mA
h_{FE4}*	DC Current Gain	60	150		—	V_{CE}=1.0 V, I_C=50 mA
h_{FE5}*	DC Current Gain	30	80		—	V_{CE}=1.0 V, I_C=100 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.1	0.2	V	I_C=10 mA, I_B=1.0 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.12	0.3	V	I_C=50 mA, I_B=5.0 mA

* Pulsed PW ≤ 300 μs, duty cycle ≤ 2 %

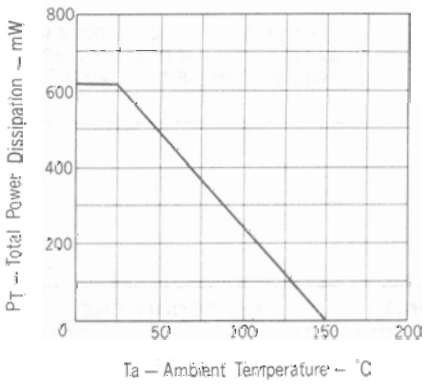
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			50	nA	V_{CE}=30 V, V_{BE}=−3 V
I_{BEX}	Base Cutoff Current			−50	nA	V_{CE}=30 V, V_{BE}=−3 V
BV_{CBO}	Collector to Base Breakdown Voltage	60			V	I_C=10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	40			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	0.65	0.72	0.85	V	I_C=10 mA, I_B=1.0 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		0.80	0.95	V	I_C=50 mA, I_B=5.0 mA
f_T	Gain Bandwidth Product	300	500		MHz	V_{CE}=20 V, I_C=10 mA
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		6.0	8.0	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	1.0	5.0	10	kΩ	V_{CE}=10 V, I_C=1 mA, f=1 kHz
h_{re}	Voltage Feedback Ratio	0.5	5.0	8.0	$\times 10^{-4}$	V_{CE}=10 V, I_C=1 mA, f=1 kHz
h_{fe}	Small Signal Current Gain	100	200	400	—	V_{CE}=10 V, I_C=1 mA, f=1 kHz
h_{oe}	Output Admittance	1.0	18	40	μS	V_{CE}=10 V, I_C=1 mA, f=1 kHz
NF	Noise Figure			5.0	dB	V_{CE}=5.0 V, I_C=0.1 mA, R_G=1 kΩ, f=10 Hz to 15.7 kHz

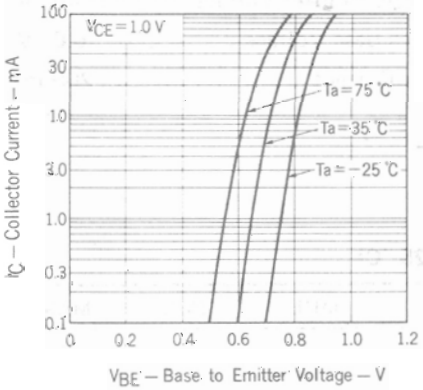
* Pulsed PW ≤300 μs, duty cycle ≤2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

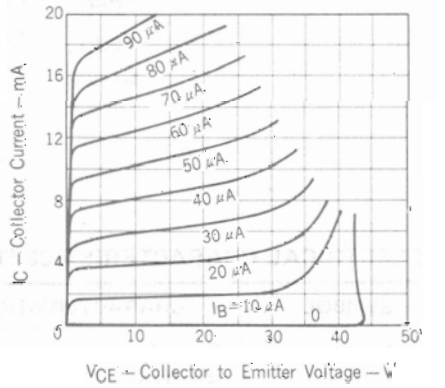
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



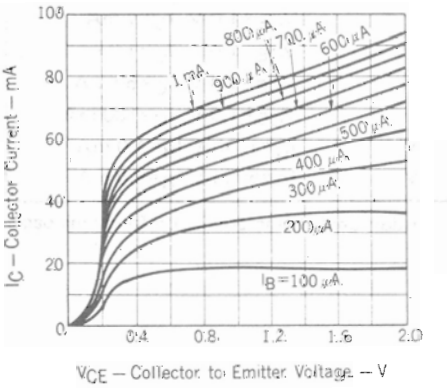
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



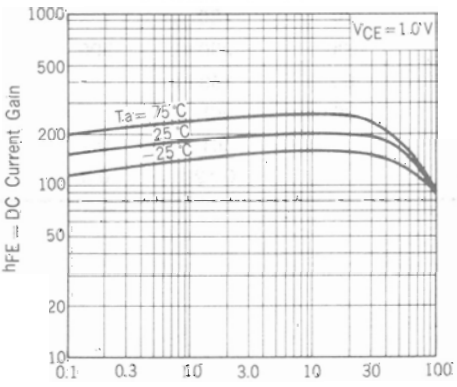
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



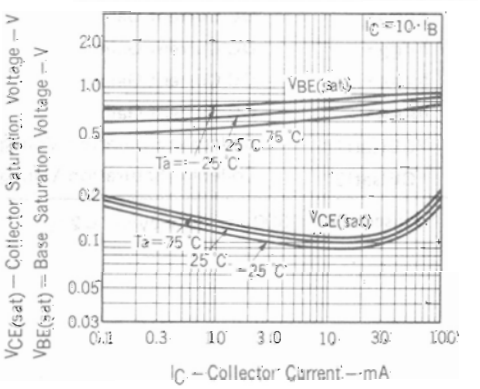
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



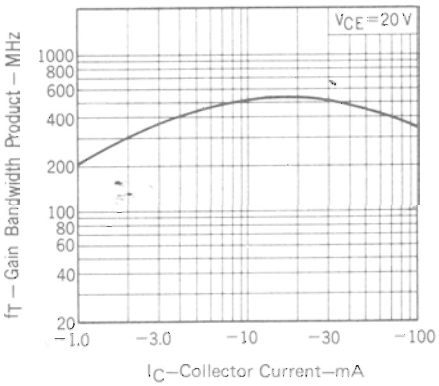
DC CURRENT GAIN vs. COLLECTOR CURRENT



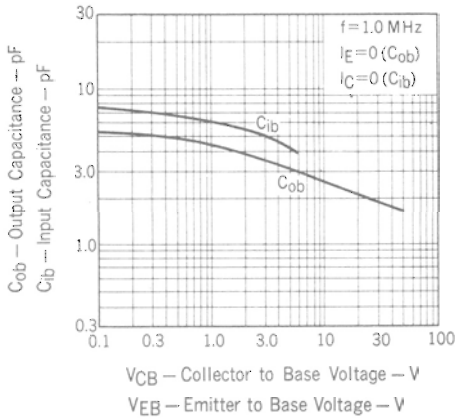
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



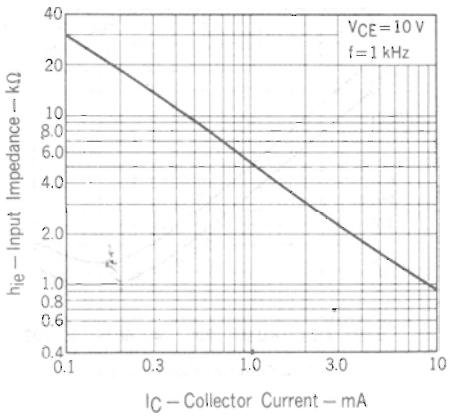
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



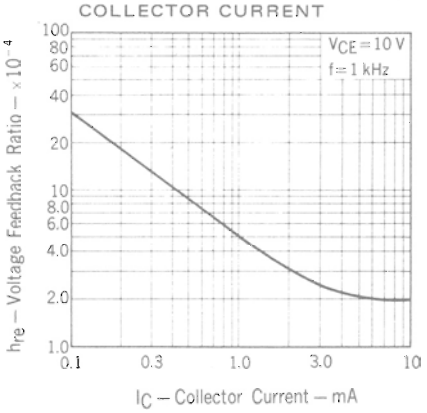
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



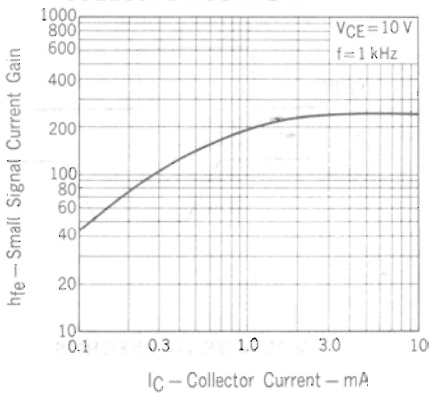
INPUT IMPEDANCE vs. COLLECTOR CURRENT



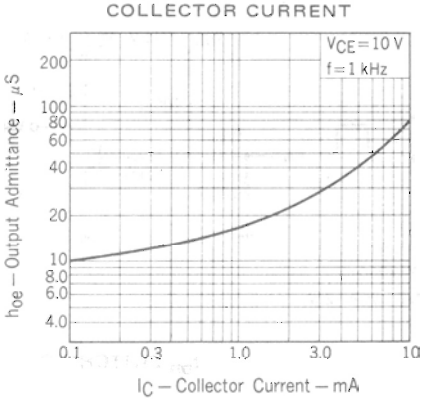
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



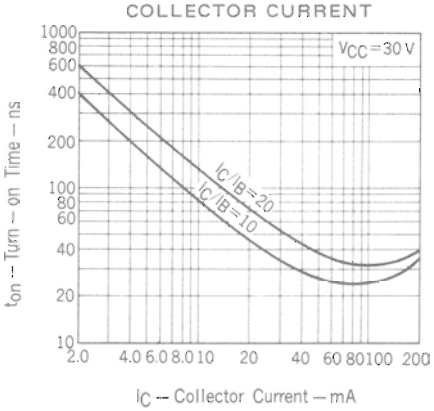
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



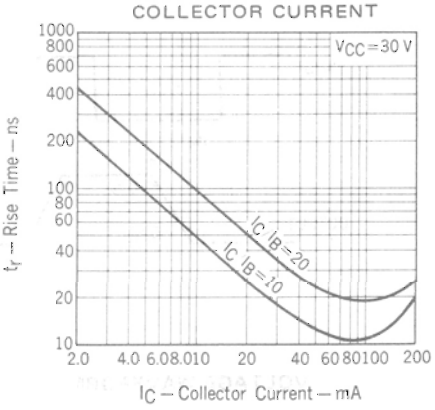
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



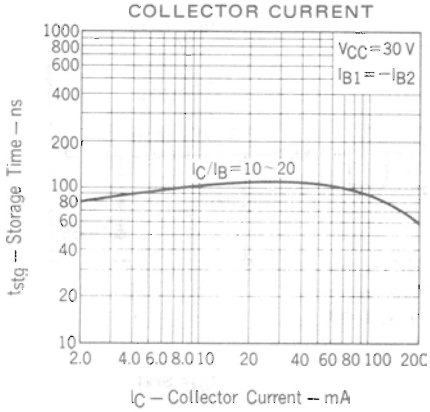
TURN-ON TIME vs. COLLECTOR CURRENT

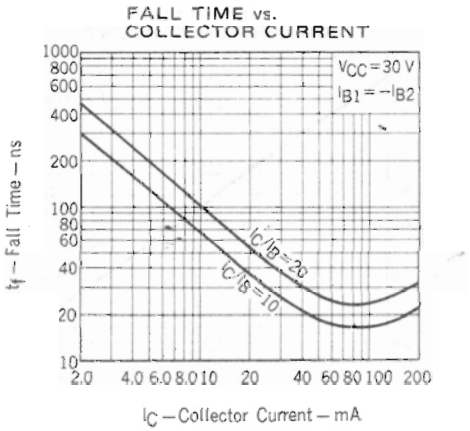


RISE TIME vs. COLLECTOR CURRENT

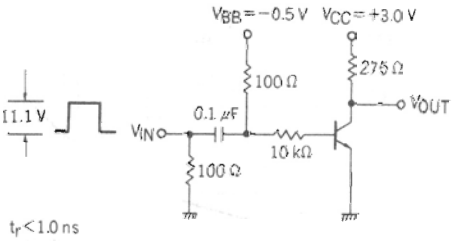


STORAGE TIME vs. COLLECTOR CURRENT



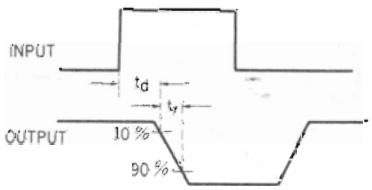


SWITCHING TIME TEST CIRCUIT

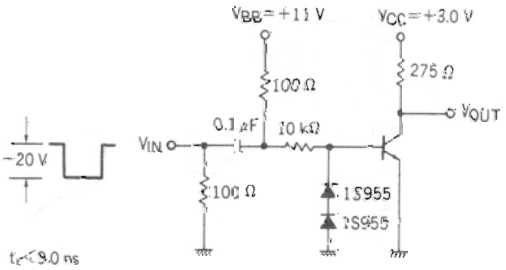


t_r < 1.0 ns
PW ≥ 300 ns
Duty cycle = 2 %

t_{on} SWITCHING

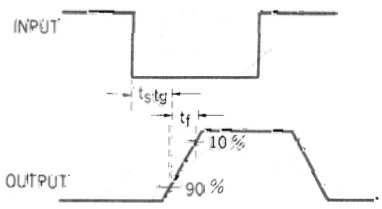


VOLTAGE WAVEFORMS



t_f < 9.0 ns
PW ≥ 300 ns
Duty cycle = 2 %

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

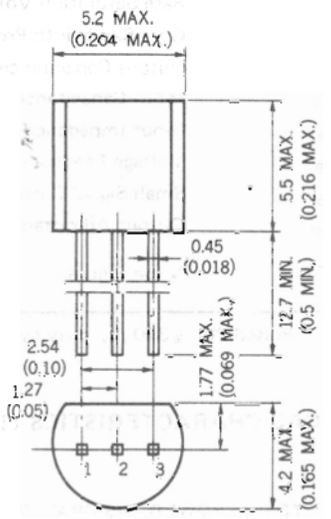
PNP SILICON TRANSISTOR
2N3905

DESCRIPTION The 2N3905 is designed for general purpose switching and amplifier application.

FEATURES

- High Power P_T : 625 mW at 25 °C
- High Voltage V_{CEO} : −40 V
- DC Current Gain h_{FE} : 50 to 150 at −10 mA
- For Complementary Use with NPN Type 2N3903

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43E
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −40 V
- V_{CEO} Collector to Emitter Voltage . . . . . −40 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			35	ns	V_{CC} = −3 V, V_{BB} = 0.5 V
t_r	Rise Time			35	ns	I_C = −10 mA, I_{B1} = −1.0 mA
t_{stg}	Storage Time			200	ns	V_{CC} = −3 V, I_C = −10 mA
t_f	Fall Time			60	ns	I_{B1} = −I_{B2} = −1.0 mA
h_{FE1}*	DC Current Gain	30	55		−	V_{CE} = −1.0 V, I_C = −0.1 mA
h_{FE2}*	DC Current Gain	40	80		−	V_{CE} = −1.0 V, I_C = −1.0 mA
h_{FE3}*	DC Current Gain	50	120	150	−	V_{CE} = −1.0 V, I_C = −10 mA
h_{FE4}*	DC Current Gain	30	100		−	V_{CE} = −1.0 V, I_C = −50 mA
h_{FE5}*	DC Current Gain	15	80		−	V_{CE} = −1.0 V, I_C = −100 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		−0.05	−0.25	V	I_C = −10 mA, I_B = −1.0 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		−0.2	−0.4	V	I_C = −50 mA, I_B = −5.0 mA

* Pulsed PW ≤ 300 μs, duty cycle ≤ 2%

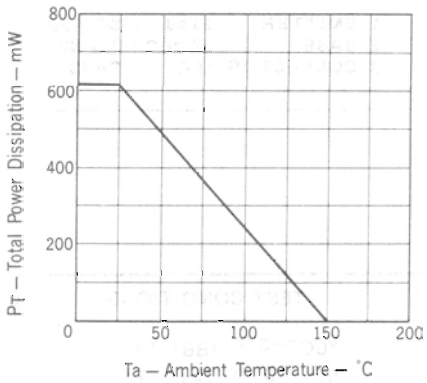
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			−50	nA	V_{CE}=−30 V, V_{BE}=3.0 V
I_{BEX}	Base Cutoff Current			50	nA	V_{CE}=−30 V, V_{BE}=3.0 V
BV_{CBO}	Collector to Base Breakdown Voltage	−40			V	I_C=−10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−40			V	I_C=−1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	−0.65	−0.75	−0.85	V	I_C=−10 mA, I_B=−1.0 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		−0.84	−0.95	V	I_C=−50 mA, I_B=−5.0 mA
f_T	Gain Bandwidth Product	200	500		MHz	V_{CE}=−20 V, I_C=−10 mA
C_{ob}	Output Capacitance		2.5	4.5	pF	V_{CB}=−5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		8.0	10	pF	V_{EB}=−0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	0.5	2.5	8.0	kΩ	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{re}	Voltage Feedback Ratio	0.1	4.0	5.0	X10^{-4}	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{fe}	Small Signal Current Gain	50	120	200	—	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{oe}	Output Admittance	1.0	15	40	μS	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
NF	Noise Figure			5.0	dB	V_{CE}=−5 V, I_C=−0.1 mA, R_G=1 kΩ, f=10 Hz to 15.7 kHz

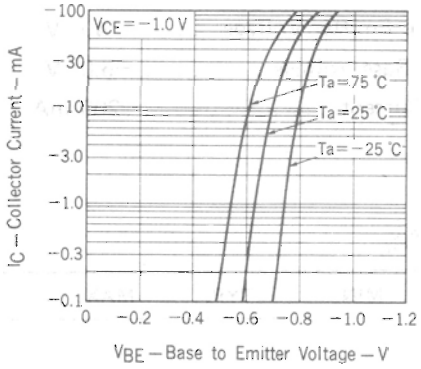
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

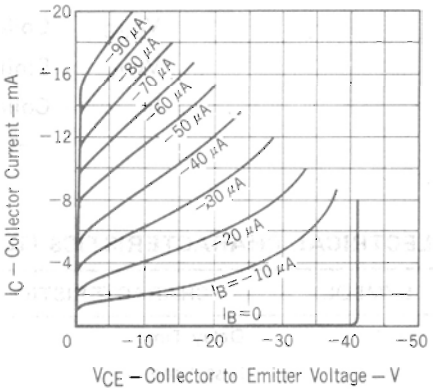
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



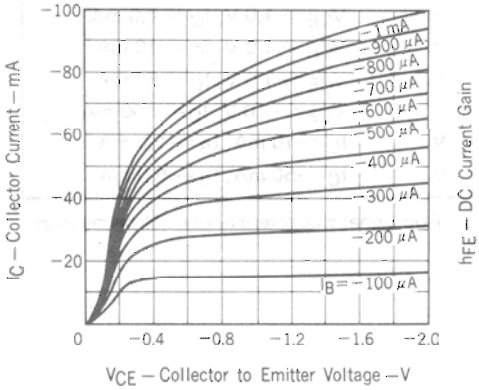
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



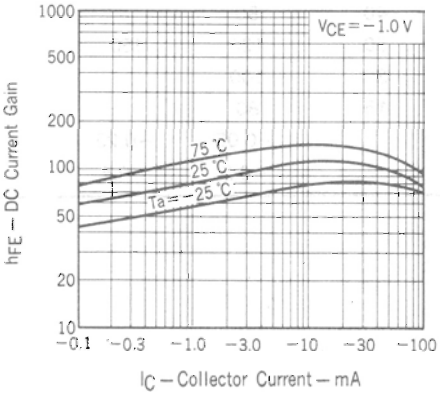
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



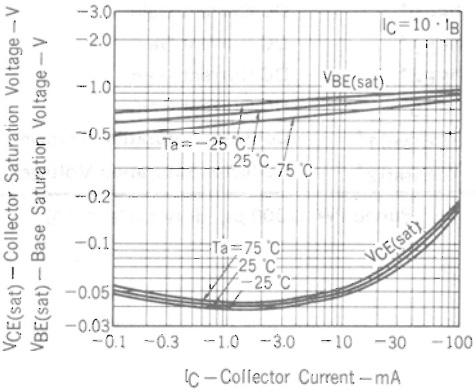
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



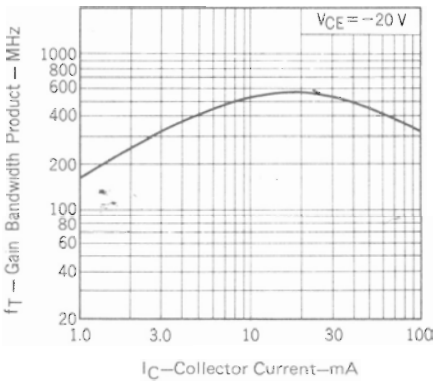
DC CURRENT GAIN vs. COLLECTOR CURRENT



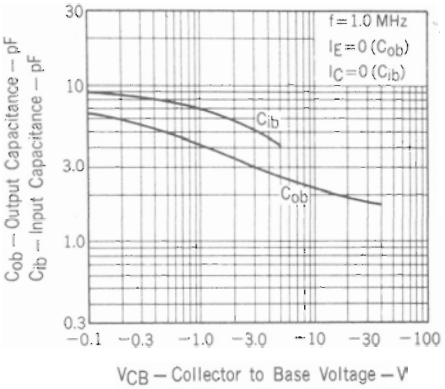
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



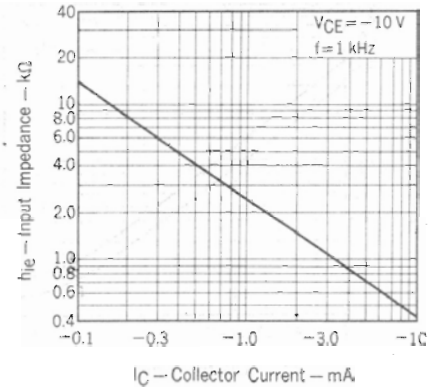
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



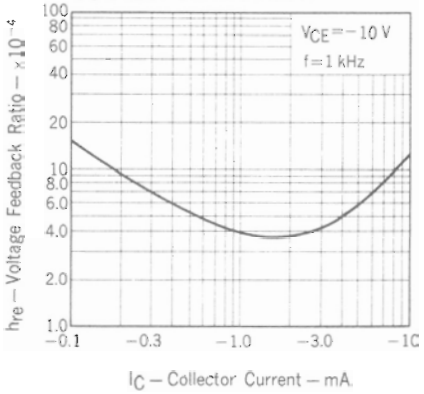
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



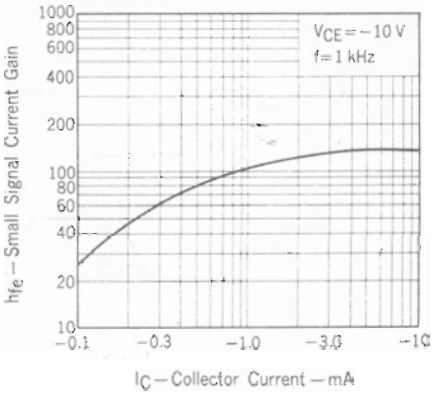
INPUT IMPEDANCE vs. COLLECTOR CURRENT



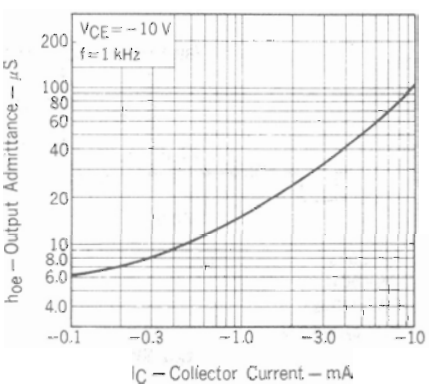
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



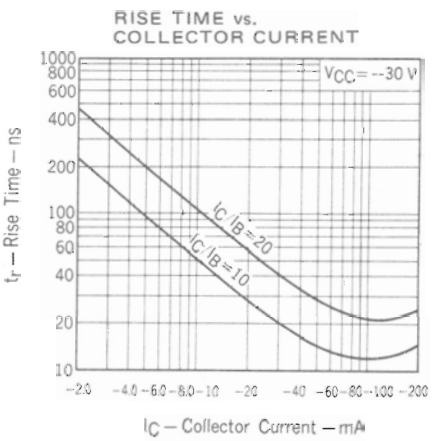
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



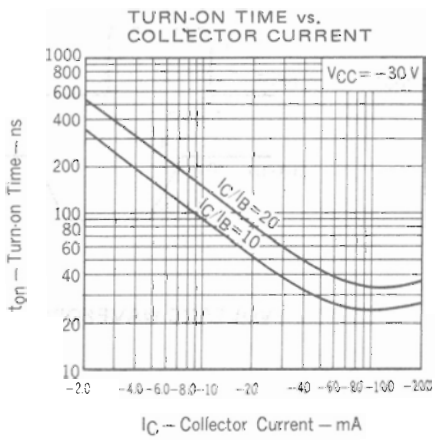
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



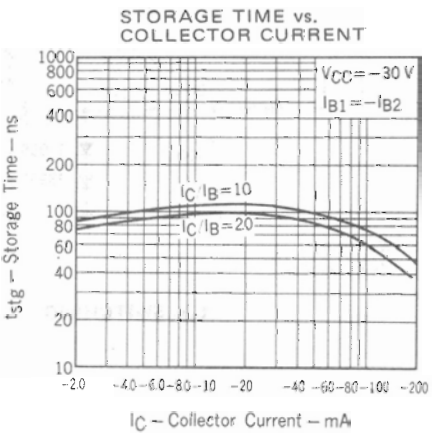
RISE TIME vs. COLLECTOR CURRENT

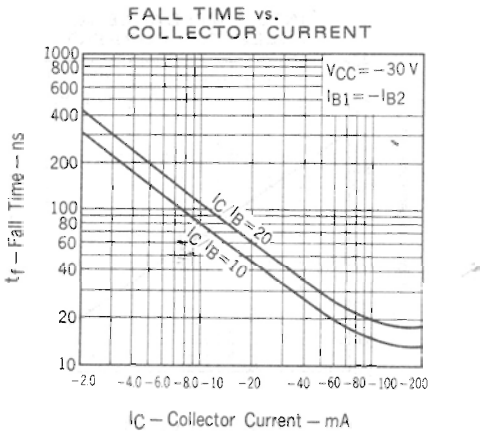


TURN-ON TIME vs. COLLECTOR CURRENT

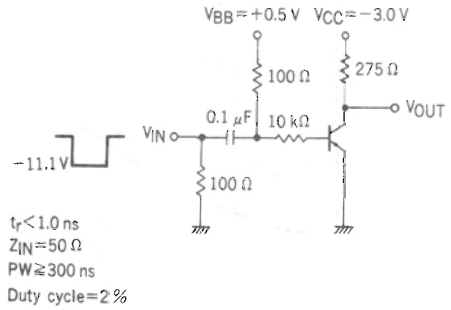


STORAGE TIME vs. COLLECTOR CURRENT

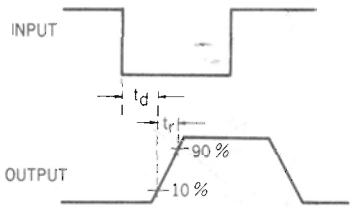




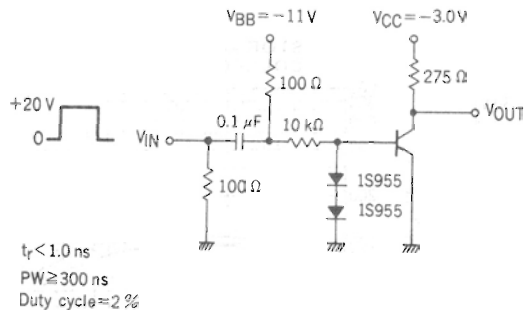
SWITCHING TIME TEST CIRCUIT



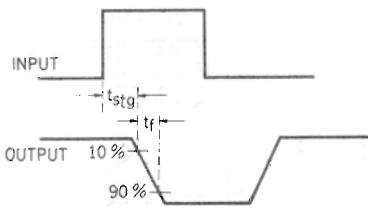
t_{on} SWITCHING



VOLTAGE WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

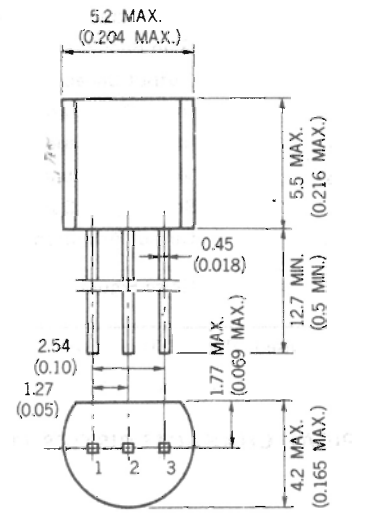
PNP SILICON TRANSISTOR
2N3906

DESCRIPTION The 2N3906 is designed for general purpose switching and amplifier application.

FEATURES

- High Power P_T : 625 mW at 25 °C
- High Voltage V_{CEO} : −40 V
- High DC Current Gain h_{FE} : 100 to 300 at −10 mA
- For Complementary Use with NPN Type 2N3904

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . −40 V

V_{CEO} Collector to Emitter Voltage . . . . . −40 V

V_{EBO} Emitter to Base Voltage . . . . . −5.0 V

I_C Collector Current . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			35	ns	V_{CC}=−3 V, V_{BB}=0.5 V
t_r	Rise Time			35	ns	I_C=−10 mA, I_{B1}=−1.0 mA
t_{stg}	Storage Time			225	ns	V_{CC}=−3 V, I_C=−10 mA
t_f	Fall Time			75	ns	I_{B1}=−I_{B2}=−1.0 mA
h_{FE1}*	DC Current Gain	60	100		—	V_{CE}=−1.0 V, I_C=−0.1 mA
h_{FE2}*	DC Current Gain	80	140		—	V_{CE}=−1.0 V, I_C=−1.0 mA
h_{FE3}*	DC Current Gain	100	180	300	—	V_{CE}=−1.0 V, I_C=−10 mA
h_{FE4}*	DC Current Gain	60	150		—	V_{CE}=−1.0 V, I_C=−50 mA
h_{FE5}*	DC Current Gain	30	100		—	V_{CE}=−1.0 V, I_C=−100 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		−0.05	−0.25	V	I_C=−10 mA, I_B=−1.0 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		−0.2	−0.4	V	I_C=−50 mA, I_B=−5.0 mA

* Pulsed PW ≤300 μs, duty cycle ≤2 %

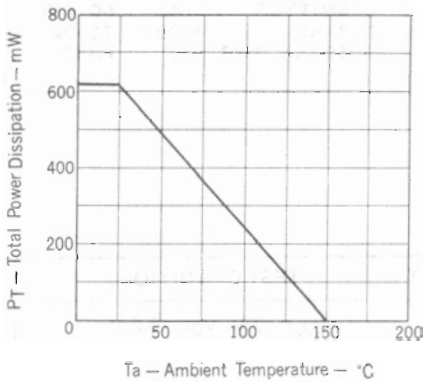
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			−50	nA	V_{CE}=−30 V, V_{BE}=3.0 V
I_{BEX}	Base Cutoff Current			50	nA	V_{CE}=−30 V, V_{BE}=3.0 V
BV_{CBO}	Collector to Base Breakdown Voltage	−40			V	I_C=−10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−40			V	I_C=−1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	−0.65	−0.75	−0.85	V	I_C=−10 mA, I_B=−1.0 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		−0.84	−0.95	V	I_C=−50 mA, I_B=−5.0 mA
f_T	Gain Bandwidth Product	250	500		MHz	V_{CE}=−20 V, I_C=−10 mA
C_{ob}	Output Capacitance		2.5	4.5	pF	V_{CB}=−5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		8.0	10	pF	V_{EB}=−0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	2.0	4.0	12	kΩ	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{re}	Voltage Feedback Ratio	1.0	6.0	10	×10⁻⁴	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{fe}	Small Signal Current Gain	100	150	400	—	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{oe}	Output Admittance	3.0	25	60	μS	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
NF	Noise Figure			4.0	dB	V_{CE}=−5.0 V, I_C=−0.1 mA, R_G=1 kΩ, f=10 Hz to 15.7 kHz

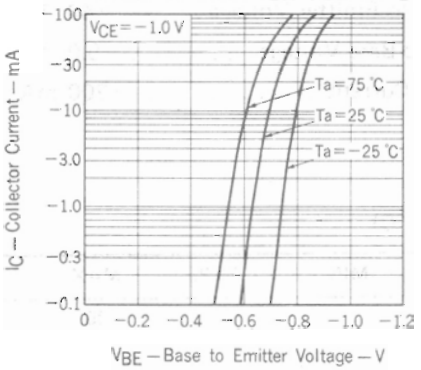
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

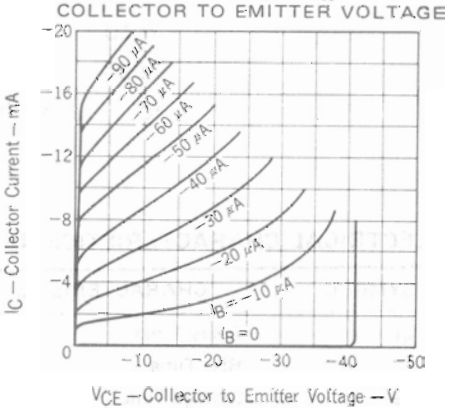
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



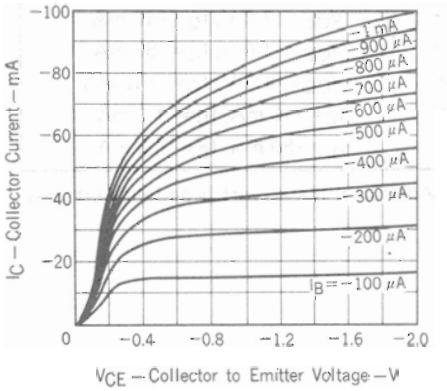
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



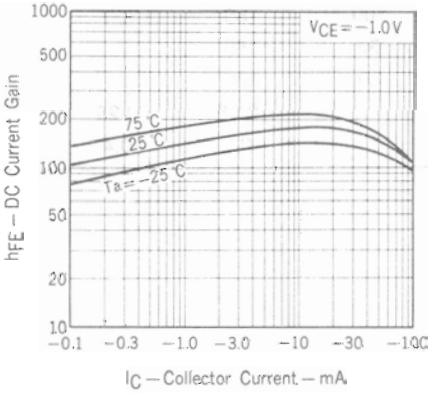
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



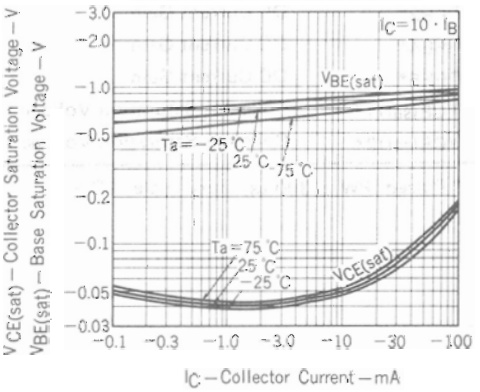
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



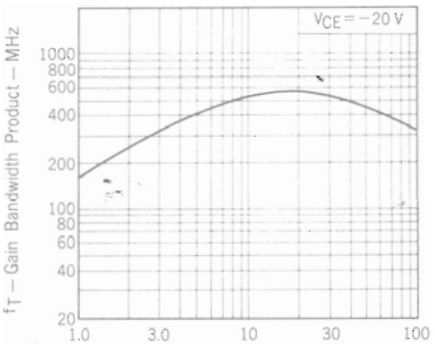
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

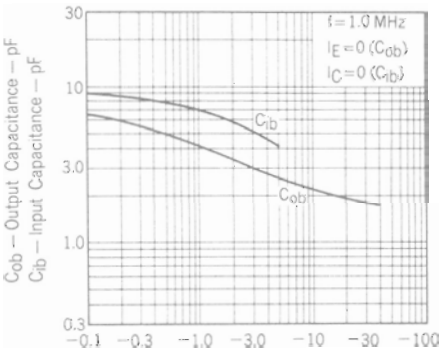


GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



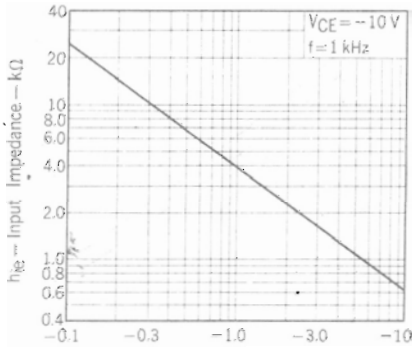
I_C – Collector Current – mA

INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



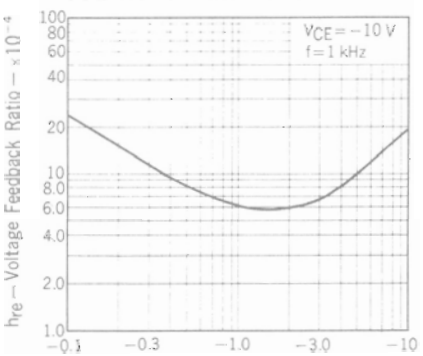
V_{CB} – Collector to Base Voltage – V
V_{EB} – Emitter to Base Voltage – V

INPUT IMPEDANCE vs. COLLECTOR CURRENT



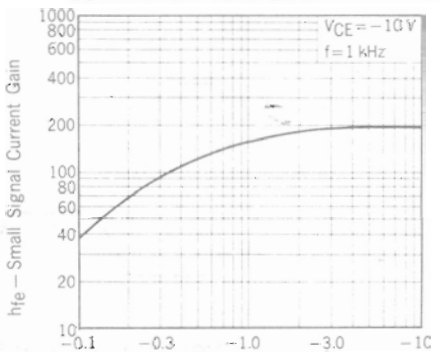
I_C – Collector Current – mA

VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



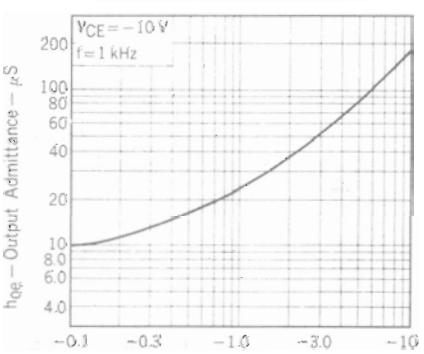
I_C – Collector Current – mA

SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



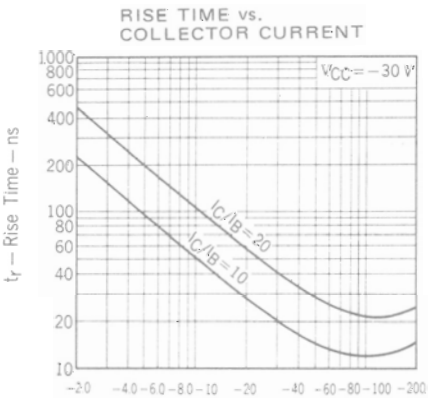
I_C – Collector Current – mA

OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



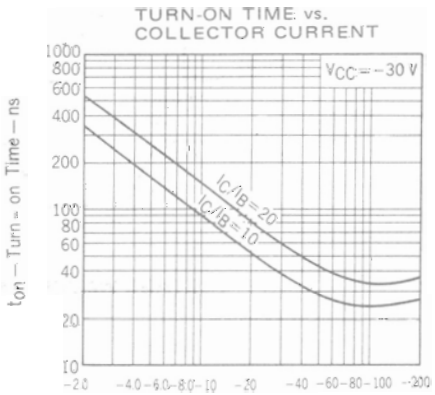
I_C – Collector Current – mA

RISE TIME vs. COLLECTOR CURRENT



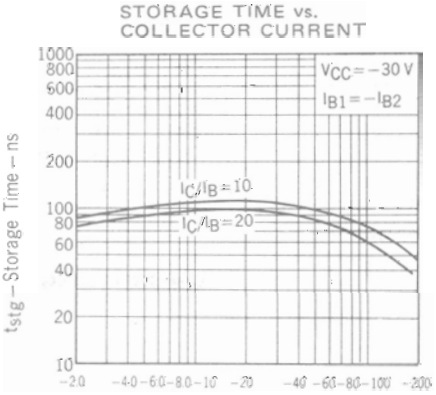
I_C – Collector Current – mA

TURN-ON TIME vs. COLLECTOR CURRENT



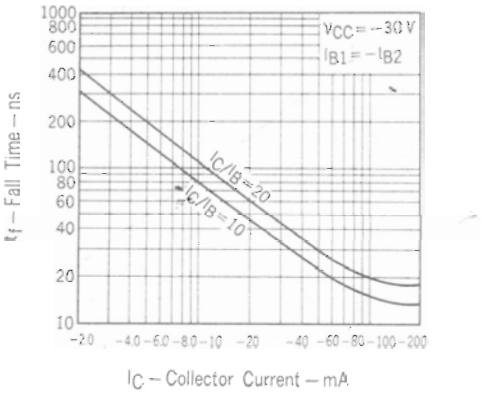
I_C – Collector Current – mA

STORAGE TIME vs. COLLECTOR CURRENT

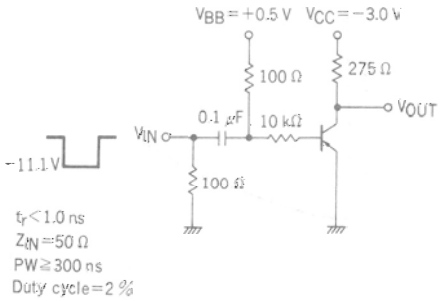


I_C – Collector Current – mA

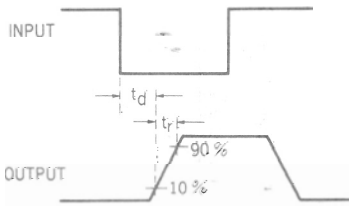
FALL TIME vs.
COLLECTOR CURRENT



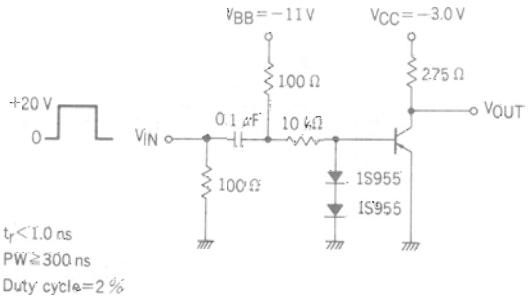
SWITCHING TIME TEST CIRCUIT



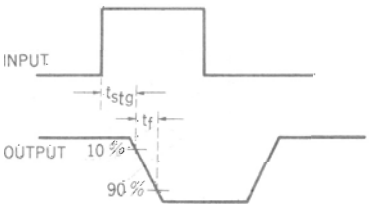
t_{on} SWITCHING



VOLTAGE WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

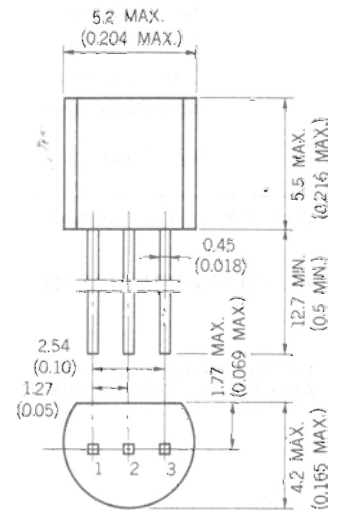
NPN SILICON TRANSISTOR
2N4123

DESCRIPTION The 2N4123 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power : P_T 625 mW at 25 °C
- h_{FE} : 50 to 150 at 2 mA
- For Complementary Use with PNP Type 2N4125

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	40 V
V_{CEO}	Collector to Emitter Voltage	30 V
V_{EBO}	Emitter to Base Voltage	5 V
I_C	Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time		20		ns	I_C=10 mA, V_{CC}=3 V
t_r	Rise Time		13		ns	V_{EB}=−0.5 V, I_{B1}=1 mA
t_{stg}	Storage Time		100		ns	I_C=10 mA, V_{CC}=3 V
t_f	Fall Time		21		ns	I_{B1}=−I_{B2}=1 mA
h_{FE1}*	DC Current Gain	50	110	150	—	V_{CE}=1.0 V, I_C=2.0 mA
h_{FE2}*	DC Current Gain	25	110		—	V_{CE}=1.0 V, I_C=50 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.15	0.3	V	I_C=50 mA, I_B=5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.8	0.95	V	I_C=50 mA, I_B=5.0 mA

* Pulsed PW ≦300 μs, duty cycle ≦2 %

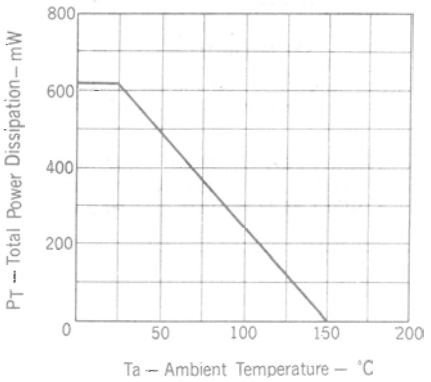
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB}=20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB}=3.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	40			V	I_C=10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	30			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E=10 μA, I_C=0
h_{fe}	Small Signal Current Gain	50	160	200	–	V_{CE}=10 V, I_C=2.0 mA, f=1.0 kHz
$\|h_{fe}\|$	High Frequency Current Gain	2.5	5.0		–	V_{CE}=20 V, I_C=10 mA, f=100 MHz
f_T	Gain Bandwidth Product	250	500		MHz	V_{CE}=20 V, I_C=10 mA, f=100 MHz
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		6.5	8.0	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
NF	Noise Figure			6.0	dB	V_{CE}=5.0 V, I_C=100 μA, R_S=1 kΩ f=10 Hz to 15.7 kHz

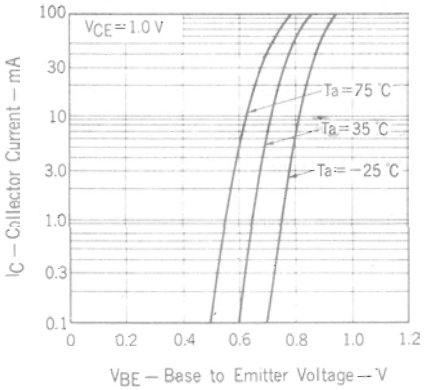
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

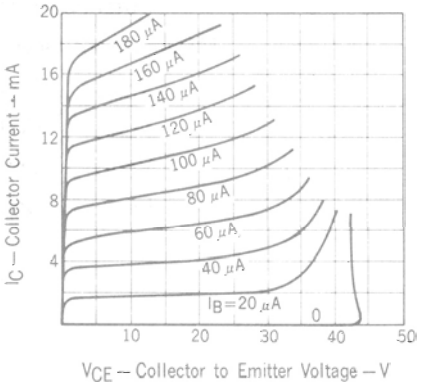
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



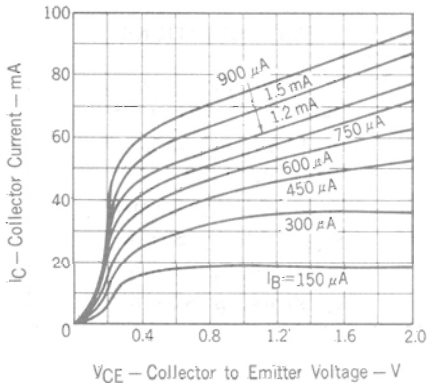
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



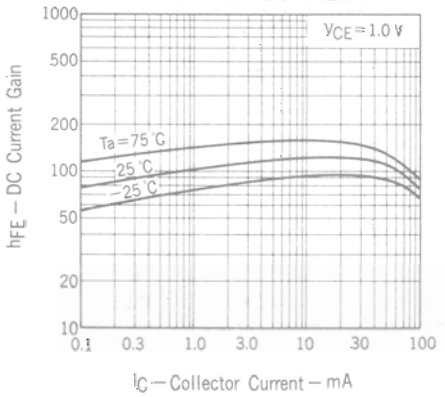
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



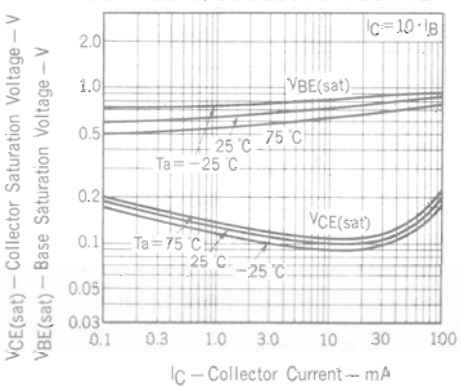
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



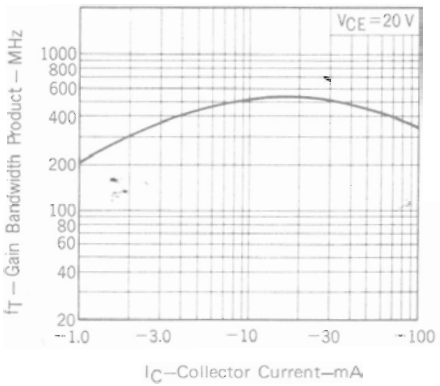
DC CURRENT GAIN vs. COLLECTOR CURRENT



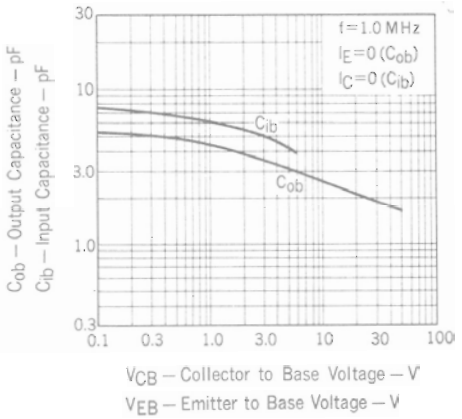
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



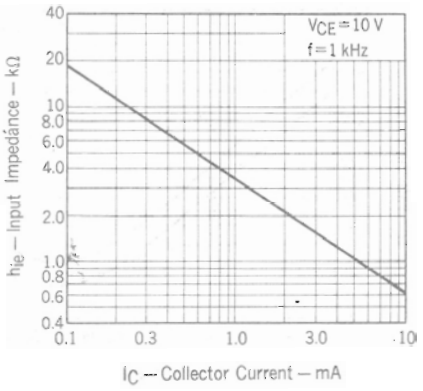
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



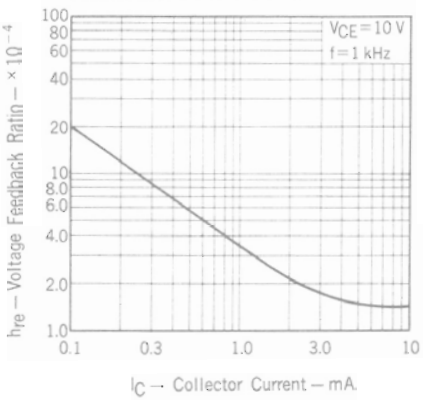
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



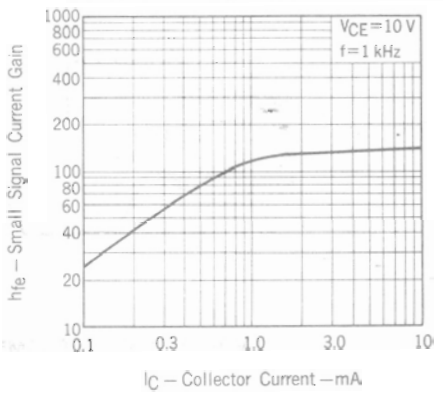
INPUT IMPEDANCE vs. COLLECTOR CURRENT



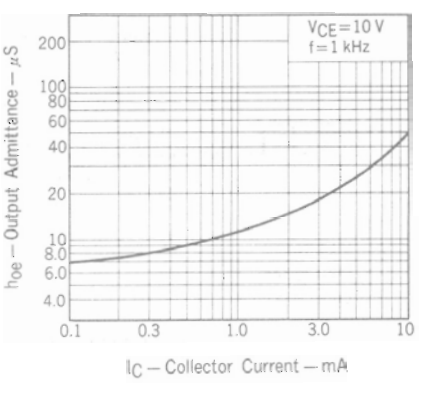
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



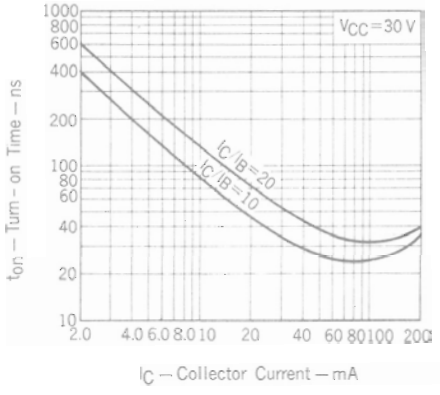
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



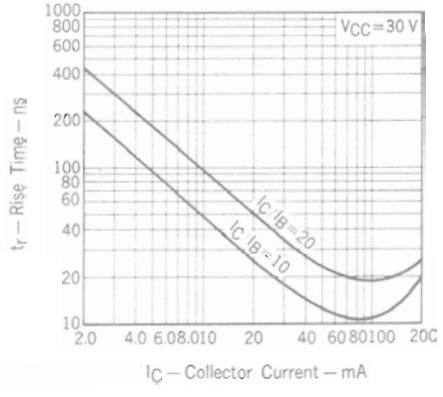
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



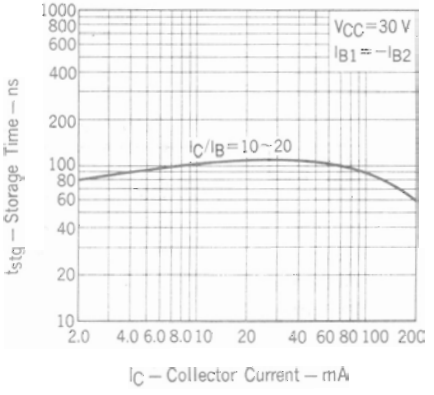
TURN-ON TIME vs. COLLECTOR CURRENT



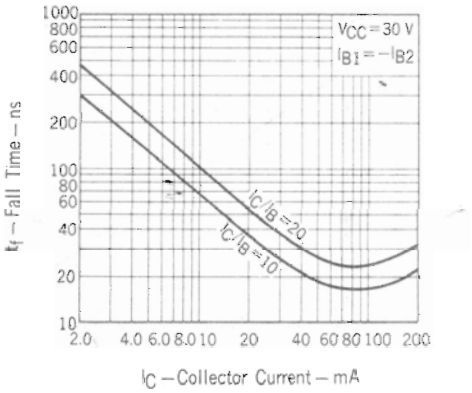
RISE TIME vs. COLLECTOR CURRENT



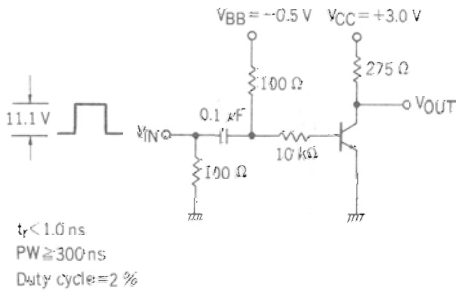
STORAGE TIME vs. COLLECTOR CURRENT



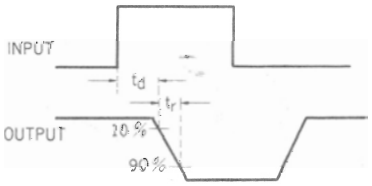
FALL TIME vs.
COLLECTOR CURRENT



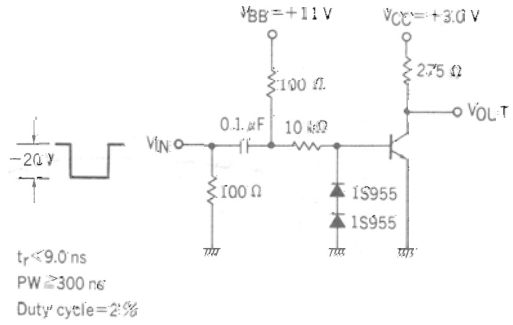
SWITCHING TIME TEST CIRCUIT



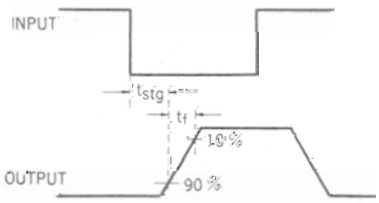
t_{on} SWITCHING



VOLTAGE WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

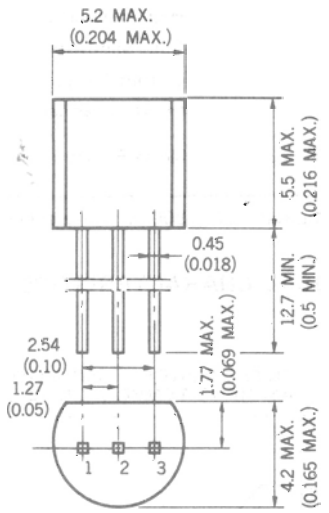
NPN SILICON TRANSISTOR
2N4124

DESCRIPTION The 2N4124 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power : P_T 625 mW at 25 °C
- High h_{FE} : 120 to 360 at 2 mA
- For Complementary Use with PNP Type 2N4126

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	30 V
V_{CEO}	Collector to Emitter Voltage	25 V
V_{EBO}	Emitter to Base Voltage	5 V
I_C	Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time		20		ns	I_C=10 mA, V_{CC}=3 V
t_r	Rise Time		13		ns	V_{EB}=−0.5 V, I_{B1}=1 mA
t_{stg}	Storage Time		100		ns	I_C=10 mA, V_{CC}=3 V
t_f	Fall Time		21		ns	I_{B1}=−I_{B2}=1 mA
h_{FE1}*	DC Current Gain	120	200	360	—	V_{CE}=1.0 V, I_C=2.0 mA
h_{FE2}*	DC Current Gain	60	150		—	V_{CE}=1.0 V, I_C=50 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		0.13	0.3	V	I_C=50 mA, I_B=5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		0.80	0.95	V	I_C=50 mA, I_B=5.0 mA

* Pulsed PW ≦300 μs, duty cycle ≦2 %

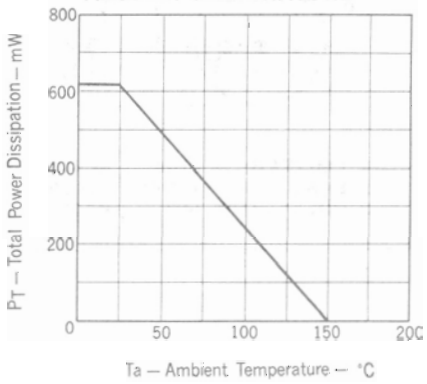
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			50	nA	V_{CB}=20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			50	nA	V_{EB}=3.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	30			V	I_C=10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	25			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E=10 μA, I_C=0
h_{fe}	Small Signal Current Gain	120	250	480	—	V_{CE}=10 V, I_C=2.0 mA, f=1.0 kHz
$\|h_{fe}\|$	High Frequency Current Gain	3.0	5.0		—	V_{CE}=20 V, I_C=10 mA, f=100 MHz
f_T	Gain Bandwidth Product	300	500		MHz	V_{CE}=20 V, I_C=10 mA, f=100 MHz
C_{ob}	Output Capacitance		3.0	4.0	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		6.5	8.0	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
NF	Noise Figure			5.0	dB	V_{CE}=5.0 V, I_C=100 μA, R_S=1 kΩ f=10 Hz to 15.7 kHz

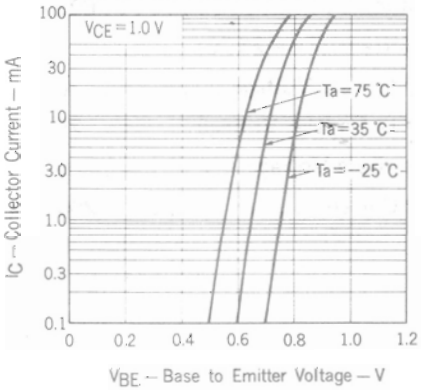
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

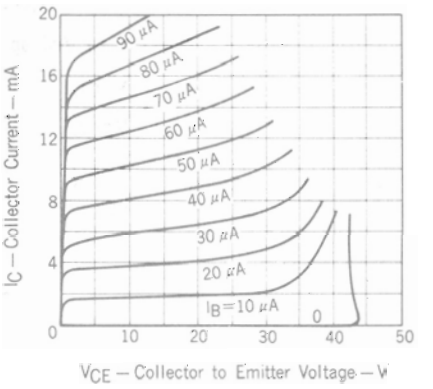
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



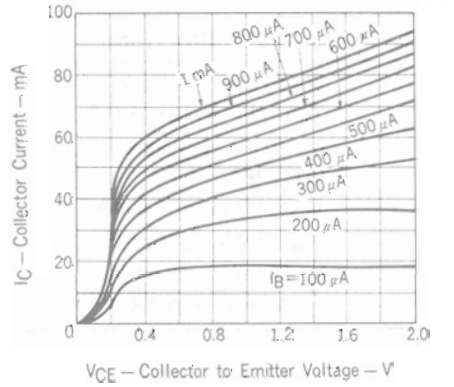
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



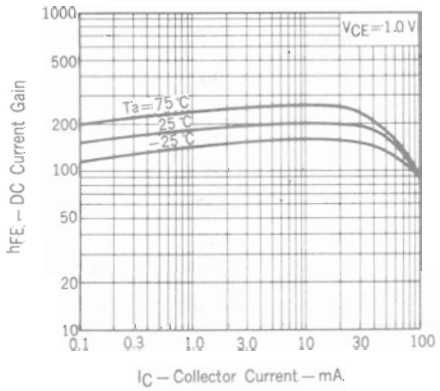
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



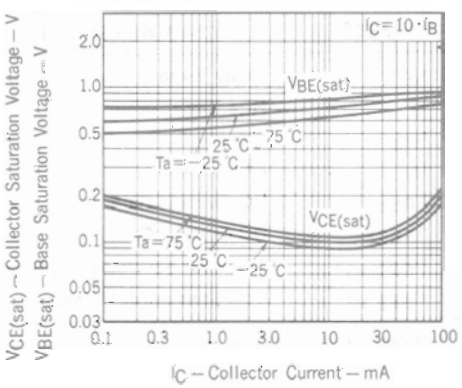
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



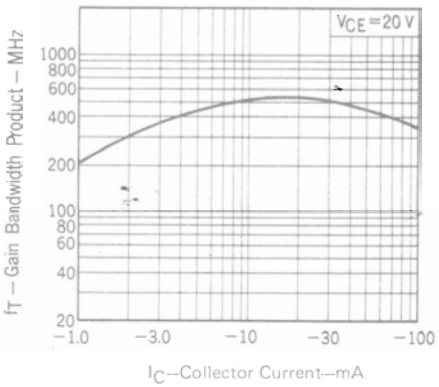
DC CURRENT GAIN vs. COLLECTOR CURRENT



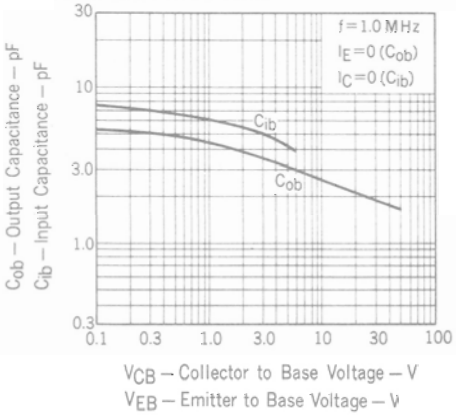
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



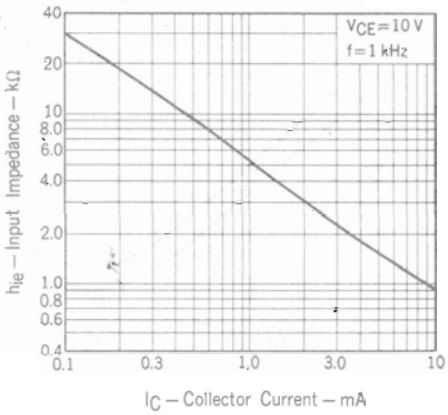
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



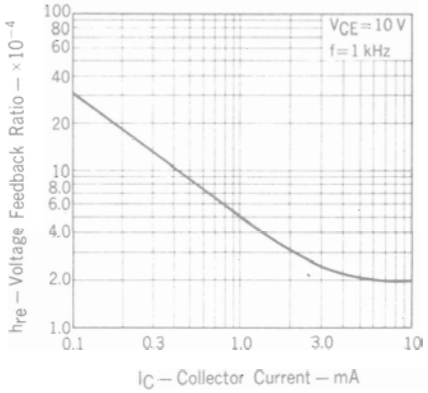
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



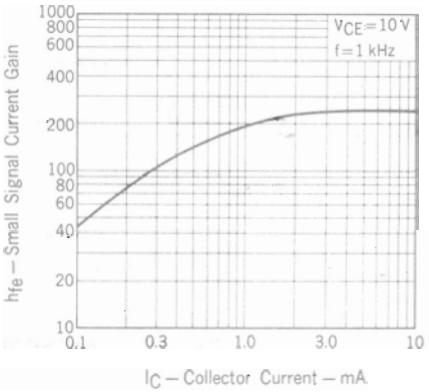
INPUT IMPEDANCE vs. COLLECTOR CURRENT



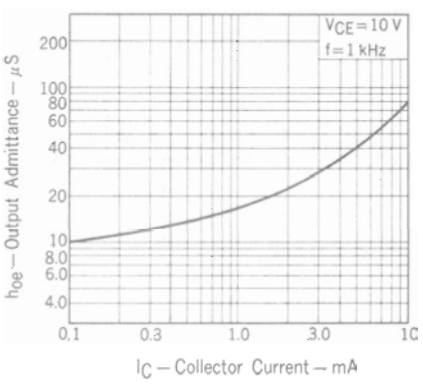
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



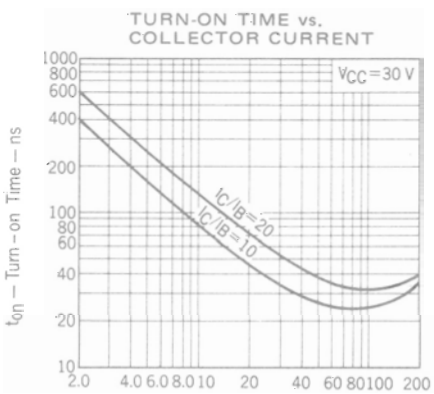
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



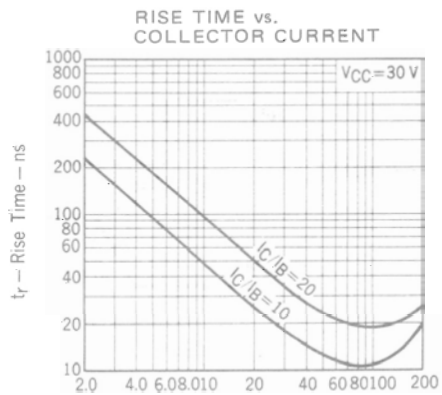
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



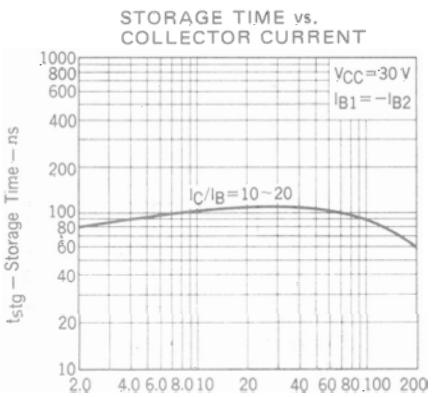
TURN-ON TIME vs. COLLECTOR CURRENT



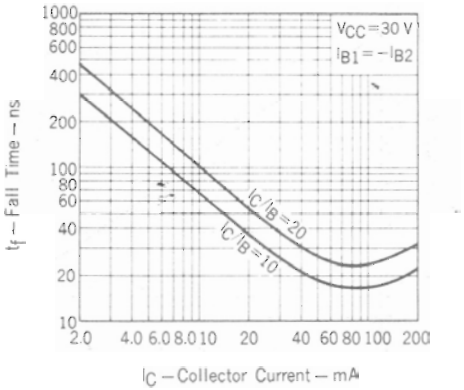
RISE TIME vs. COLLECTOR CURRENT



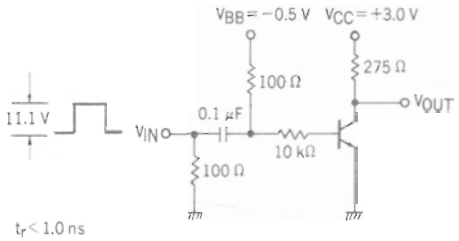
STORAGE TIME vs. COLLECTOR CURRENT



FALL TIME vs.
COLLECTOR CURRENT

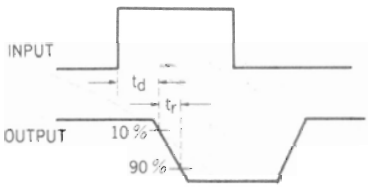


SWITCHING TIME TEST CIRCUIT

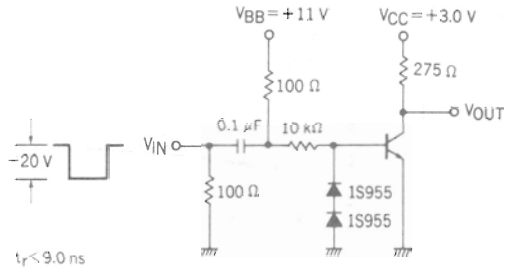


t_r < 1.0 ns
PW ≧ 300 ns
Duty cycle = 2 %

t_{on} SWITCHING

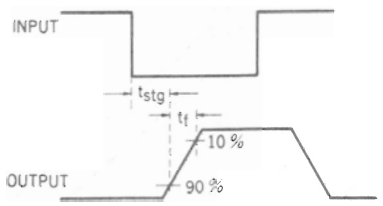


VOLTAGE WAVEFORMS



t_r < 9.0 ns
PW ≧ 300 ns
Duty cycle = 2 %

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

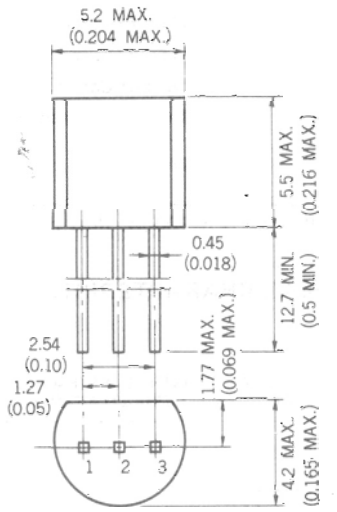
PNP SILICON TRANSISTOR
2N4125

DESCRIPTION The 2N4125 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power P_T : 625 mW at 25 °C
- h_{FE} : 50 to 150 at −2 mA
- For Complementary Use with NPN Type 2N4123

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	−30 V
V_{CEO}	Collector to Emitter Voltage	−30 V
V_{EBO}	Emitter to Base Voltage	−4.0 V
I_C	Collector Current	−200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time		8.0		ns	I_C=−10 mA, V_{CC}=−3 V
t_r	Rise Time		28		ns	V_{EB}=0.5 V, I_{B1}=−1 mA
t_{stg}	Storage Time		130		ns	I_C=−10 mA, V_{CC}=−3 V
t_f	Fall Time		40		ns	I_{B1}=−I_{B2}=−1 mA
h_{FE1}*	DC Current Gain	50	110	150	—	V_{CE}=−1.0 V, I_C=−2.0 mA
h_{FE2}*	DC Current Gain	25	95		—	V_{CE}=−1.0 V, I_C=−50 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.1	−0.4	V	I_C=−50 mA, I_B=−5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.85	−0.95	V	I_C=−50 mA, I_B=−5.0 mA

* Pulsed PW ≦300 μs, duty cycle ≦2 %

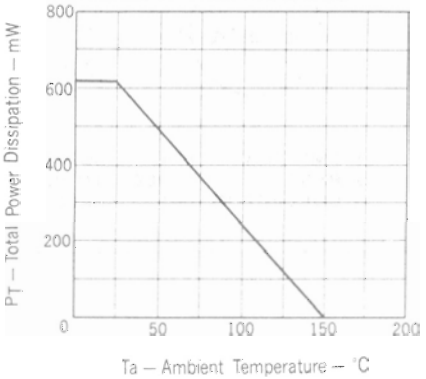
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB}=−20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB}=−3.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	−30			V	I_C=−10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−30			V	I_C=−1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−4.0			V	I_E=−10 μA, I_C=0
h_{fe}	Small Signal Current Gain	50	110	200	—	V_{CE}=−10 V, I_C=−2.0 mA, f=1.0 kHz
$\|h_{fe}\|$	High Frequency Current Gain	2.0	5.0		—	V_{CE}=−20 V, I_C=−10 mA, f=100 MHz
f_T	Gain Bandwidth Product	200	500		MHz	V_{CE}=−20 V, I_C=−10 mA, f=100 MHz
C_{ob}	Output Capacitance		2.5	4.5	pF	V_{CB}=−5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		7.8	10	pF	V_{EB}=−0.5 V, I_C=0, f=1 MHz
NF	Noise Figure			5.0	dB	V_{CE}=−5.0 V, I_C=−100 μA, R_S=1 kΩ f=10 Hz to 15.7 kHz

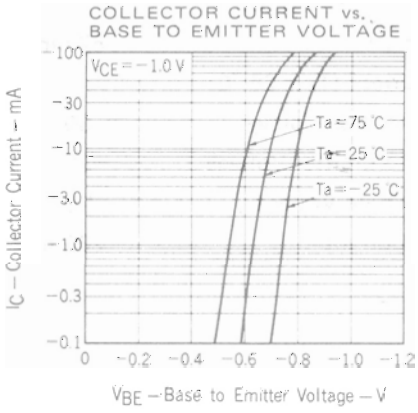
* Pulsed PW ≤300 μs, duty cycle ≤2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

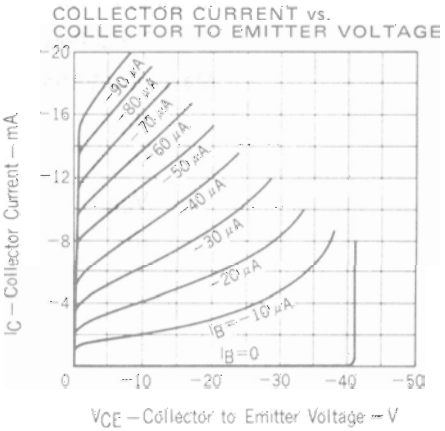
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



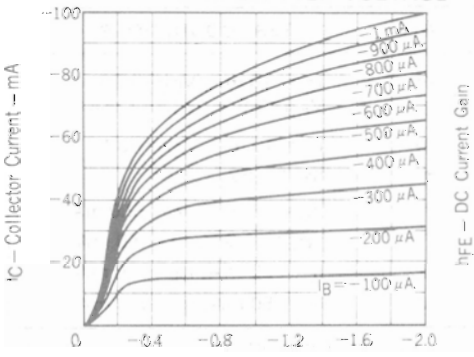
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



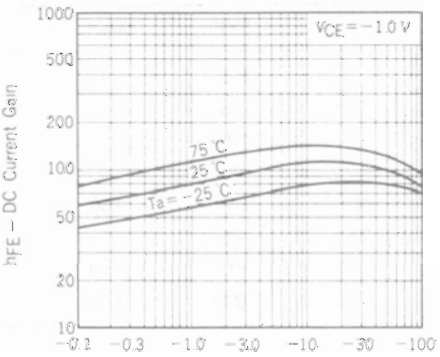
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



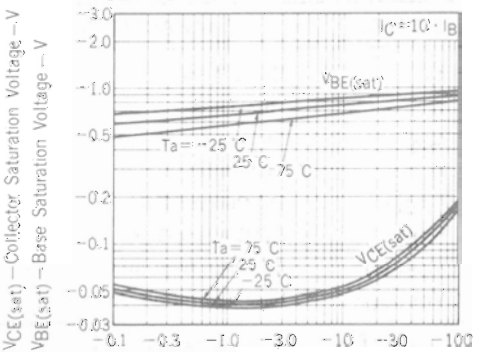
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



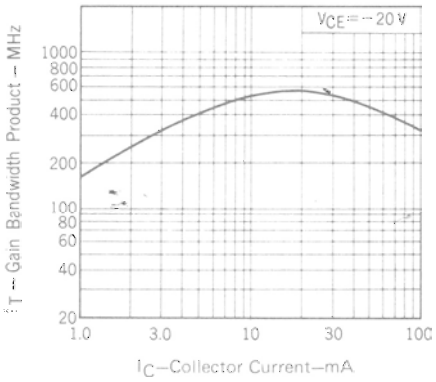
DC CURRENT GAIN vs. COLLECTOR CURRENT



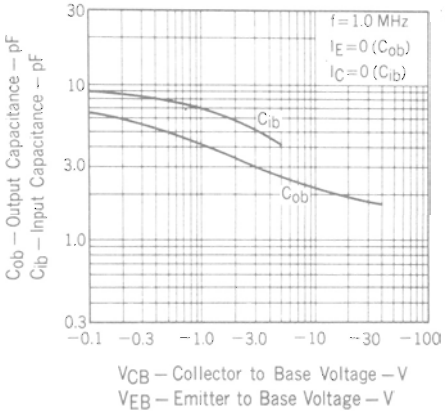
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



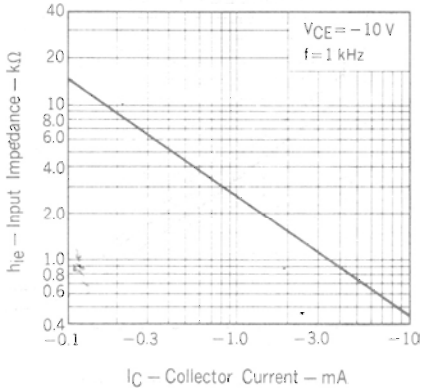
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



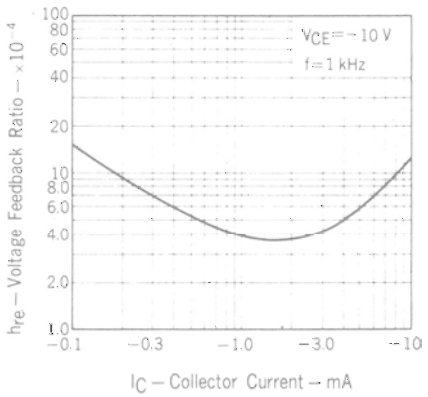
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



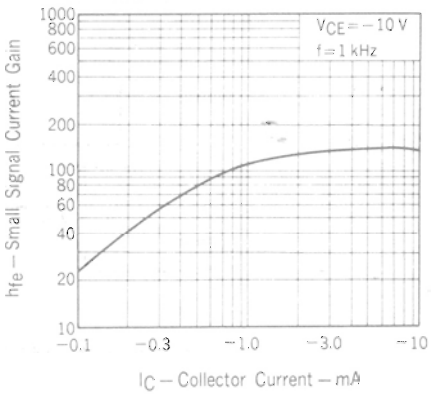
INPUT IMPEDANCE vs. COLLECTOR CURRENT



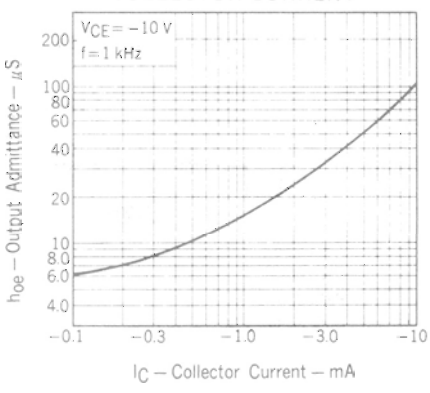
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



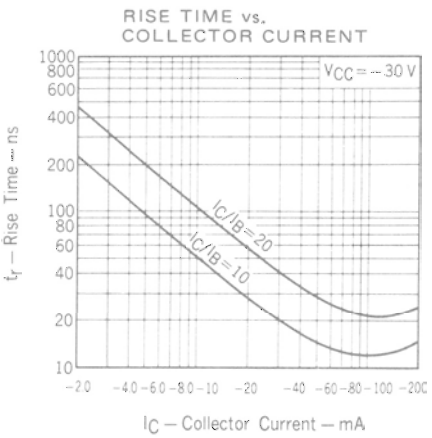
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



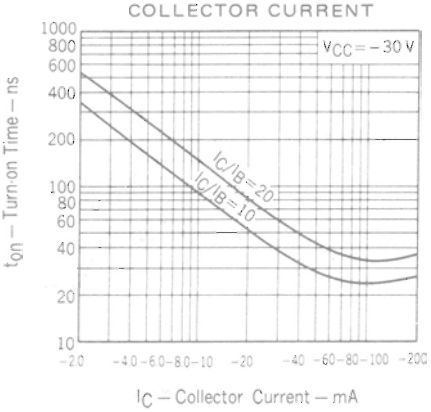
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



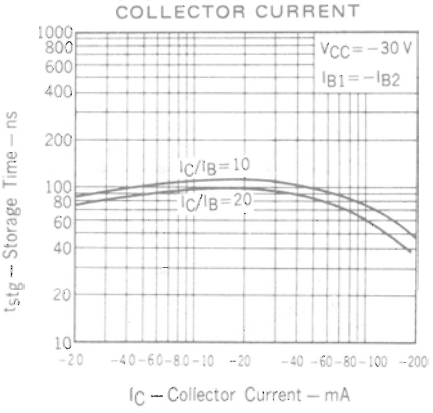
RISE TIME vs. COLLECTOR CURRENT

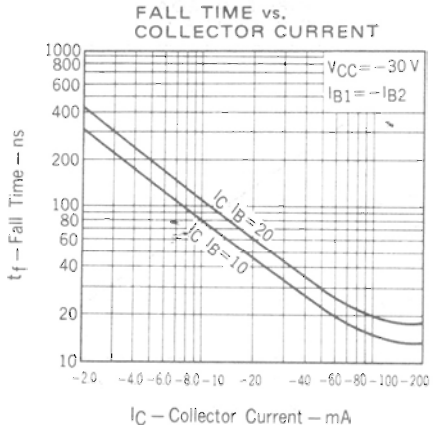


TURN-ON TIME vs. COLLECTOR CURRENT

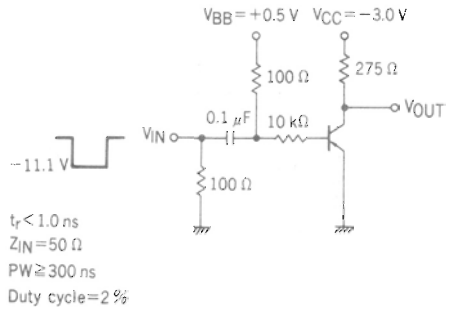


STORAGE TIME vs. COLLECTOR CURRENT

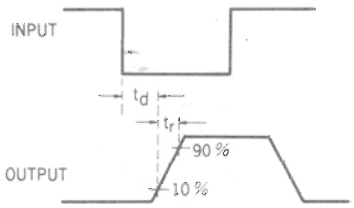




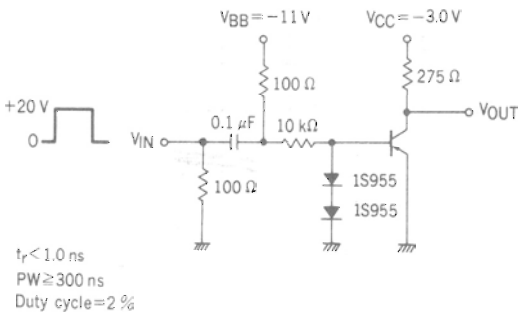
SWITCHING TIME TEST CIRCUIT



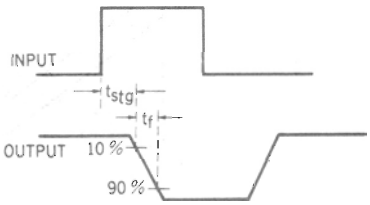
t_{on} SWITCHING



VOLTAGE WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

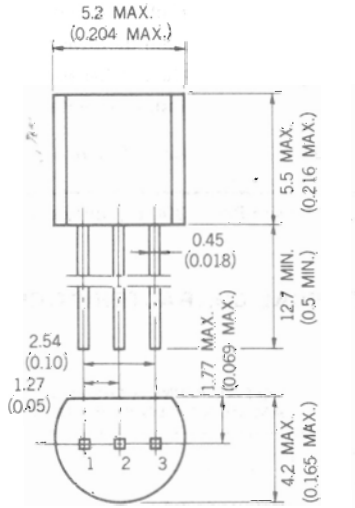
PNP SILICON TRANSISTOR
2N4126

DESCRIPTION The 2N4126 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power P_T : 625 mW at 25 °C
- High h_{FE} : 120 to 360 at −2 mA
- For Complementary Use with NPN Type 2N4124

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . −25 V

V_{CEO} Collector to Emitter Voltage . . . . . −25 V

V_{EBO} Emitter to Base Voltage . . . . . −4.0 V

I_C Collector Current . . . . . −200 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time		8.0		ns	I_C = −10 mA, V_{CC} = −3 V
t_r	Rise Time		28		ns	V_{EB} = 0.5 V, I_{B1} = −1 mA
t_{stg}	Storage Time		130		ns	I_C = −10 mA, V_{CC} = −3 V
t_f	Fall Time		40		ns	I_{B1} = −I_{B2} = −1 mA
h_{FE1}*	DC Current Gain	120	160	360	—	V_{CE} = −1.0 V, I_C = −2.0 mA
h_{FE2}*	DC Current Gain	60	150		—	V_{CE} = −1.0 V, I_C = −50 mA
$V_{CE(sat)}$*	Collector Saturation Voltage		−0.1	−0.4	V	I_C = −50 mA, I_B = −5.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage		−0.82	−0.95	V	I_C = −50 mA, I_B = −5.0 mA

* Pulsed PW ≤ 300 μs, duty cycle ≤ 2 %

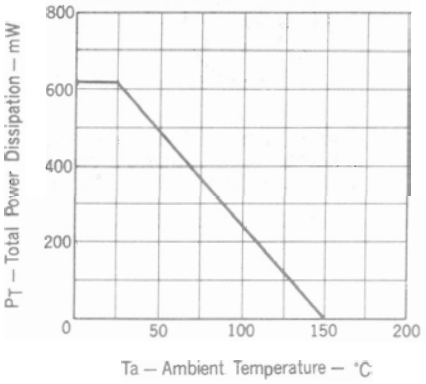
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current			−50	nA	V_{CB}=−20 V, I_E=0
I_{EBO}	Emitter Cutoff Current			−50	nA	V_{EB}=−3.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	−25			V	I_C=−10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−25			V	I_C=−1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−4.0			V	I_E=−10 μA, I_C=0
h_{fe}	Small Signal Current Gain	120	180	480	—	V_{CE}=−10 V, I_C=−2.0 mA, f=1.0 kHz
$\|h_{fe}\|$	High Frequency Current Gain	2.5	5.0		—	V_{CE}=−20 V, I_C=−10 mA, f=100 MHz
f_T	Gain Bandwidth Product	250	500		MHz	V_{CE}=−20 V, I_C=−10 mA, f=100 MHz
C_{ob}	Output Capacitance		2.5	4.5	pF	V_{CB}=−5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		7.8	10	pF	V_{EB}=−0.5 V, I_C=0, f=1 MHz
NF	Noise Figure			4.0	dB	V_{CE}=−5.0 V, I_C=−100 μA, R_S=1 kΩ f=10 Hz to 15.7 kHz

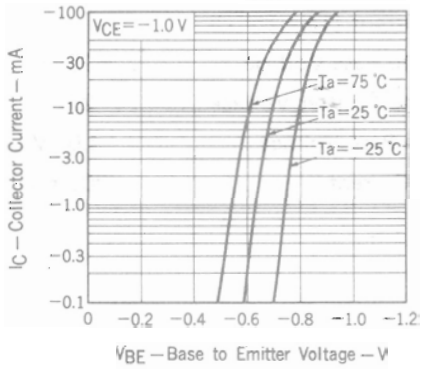
* Pulsed PW ≦300 μs, duty cycle ≦2%

TYPICAL CHARACTERISTICS (Ta=25 °C)

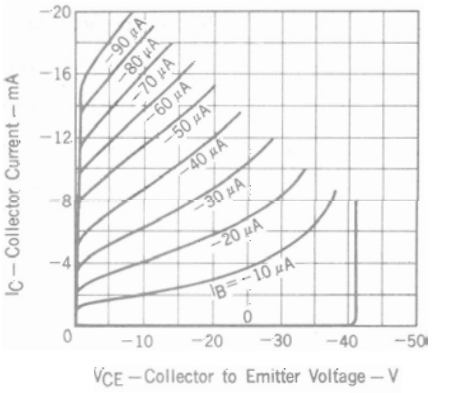
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



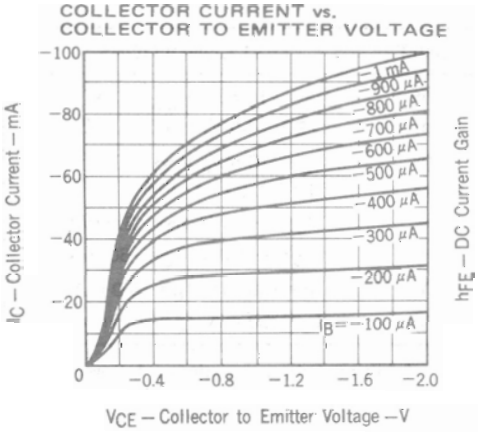
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



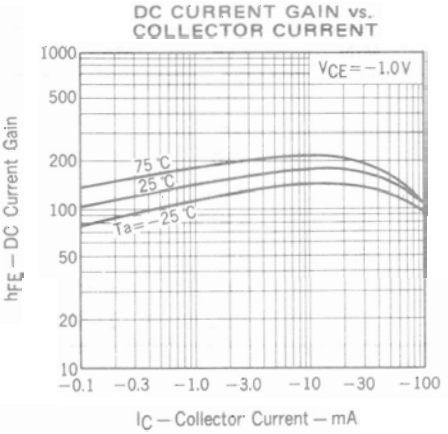
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



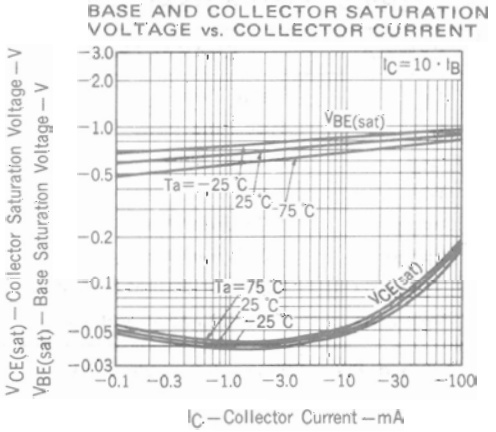
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



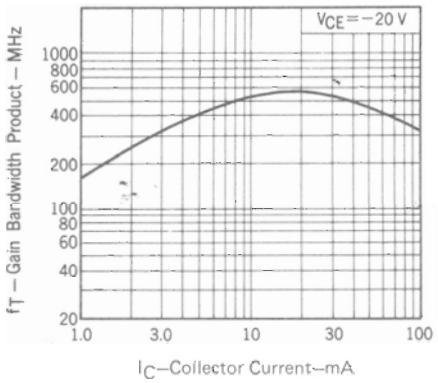
DC CURRENT GAIN vs. COLLECTOR CURRENT



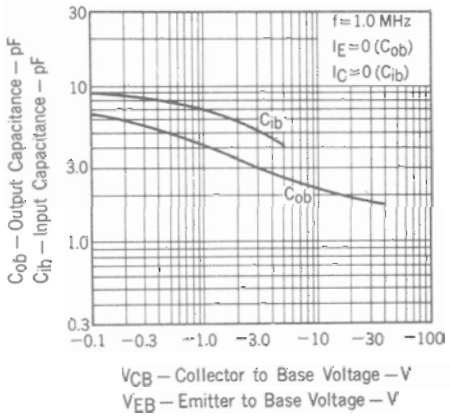
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



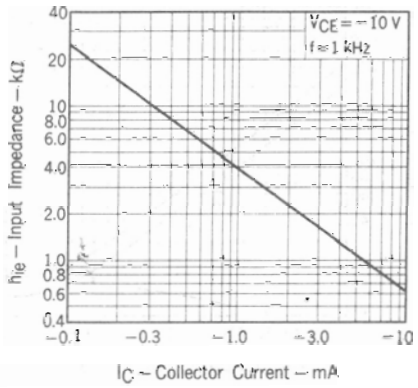
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



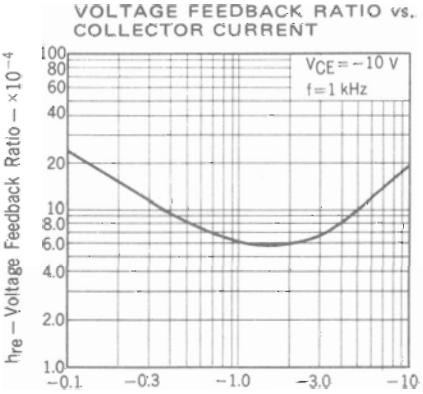
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



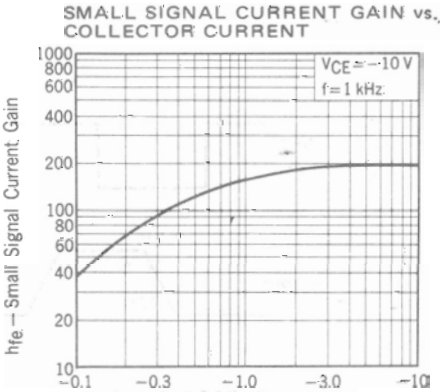
INPUT IMPEDANCE vs. COLLECTOR CURRENT



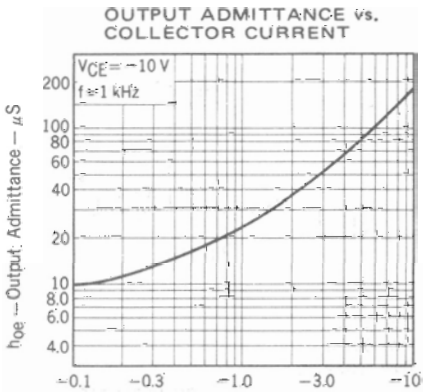
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



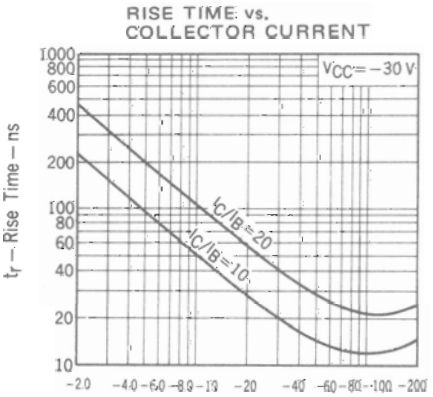
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



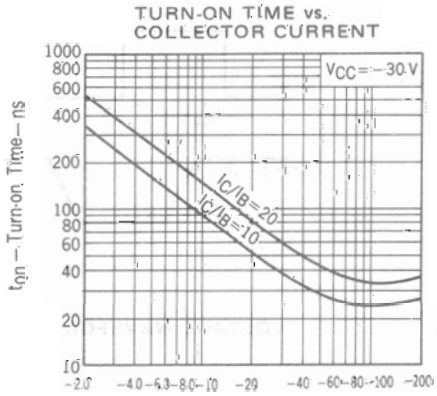
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



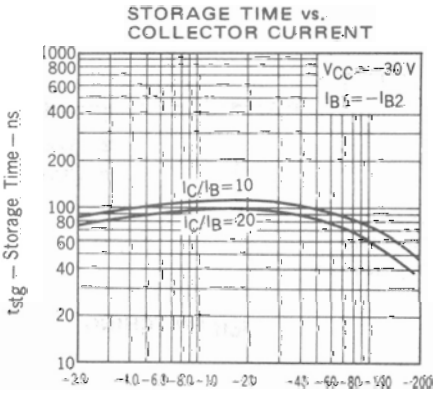
RISE TIME vs. COLLECTOR CURRENT

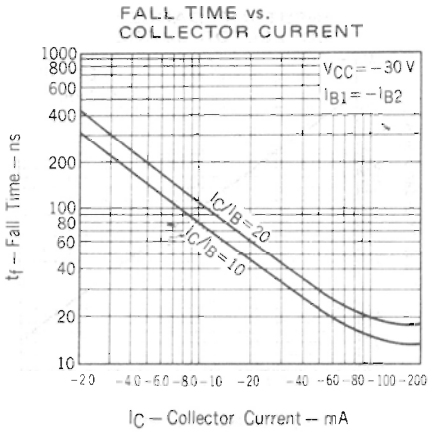


TURN-ON TIME vs. COLLECTOR CURRENT

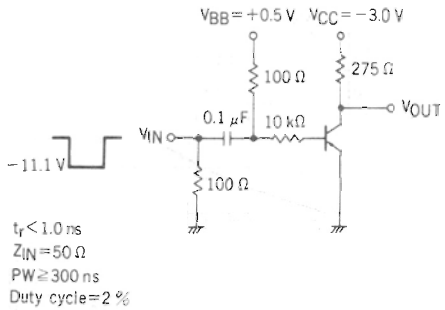


STORAGE TIME vs. COLLECTOR CURRENT

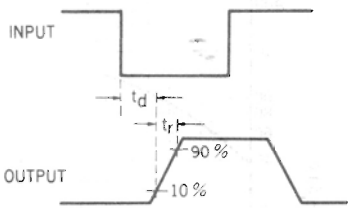




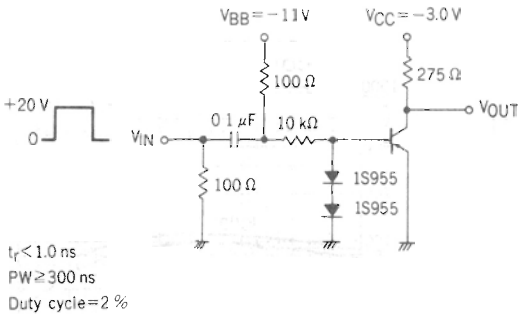
SWITCHING TIME TEST CIRCUIT



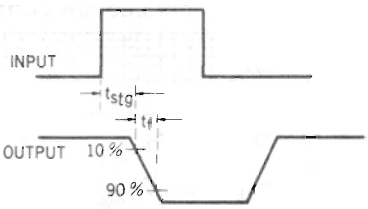
t_{on} SWITCHING



VOLTAGE WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

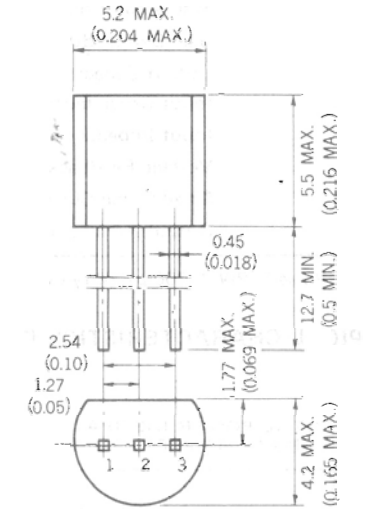
NPN SILICON TRANSISTOR
2N4400

DESCRIPTION The 2N4400 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power . . . P_T 625 mW at 25 °C
- High Voltage . . . V_{CEO} 40 V
- DC Current Gain h_{FE} 50 to 150 at 150 mA
- For Complementary Use with PNP Type 2N4402

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	60 V
V_{CEO}	Collector to Emitter Voltage	40 V
V_{EBO}	Emitter to Base Voltage	6.0 V
I_C	Collector Current	600 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			15	ns	V_{CC}=30 V, I_C=150 mA
t_r	Rise Time			20	ns	I_{B1}=15 mA, V_{EB}=−2 V
t_{stg}	Storage Time			225	ns	V_{CC}=30 V, I_C=150 mA
t_f	Fall Time			30	ns	I_{B1}=−I_{B2}=15 mA
h_{FE1}	DC Current Gain	20	80		—	V_{CE}=1.0 V, I_C=1.0 mA
h_{FE2}	DC Current Gain	40	90		—	V_{CE}=1.0 V, I_C=10 mA
h_{FE3}*	DC Current Gain	50	100	150	—	V_{CE}=1.0 V, I_C=150 mA
h_{FE4}*	DC Current Gain	20	60		—	V_{CE}=2.0 V, I_C=500 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.15	0.4	V	I_C=150 mA, I_B=15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.4	0.75	V	I_C=500 mA, I_B=50 mA

*Pulsed PW ≤300 μs, duty cycle ≤2 %

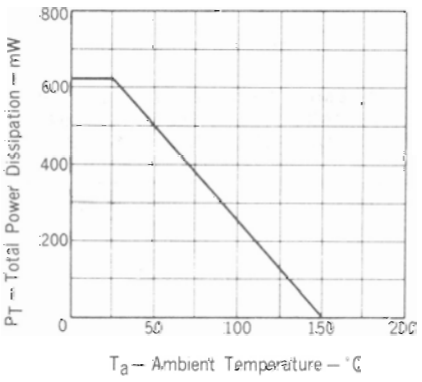
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			100	nA	V_{CE}=35 V, V_{BE}=−0.4 V
I_{BEX}	Base Cutoff Current			−100	nA	V_{CE}=35 V, V_{BE}=−0.4 V
BV_{CBO}	Collector to Base Breakdown Voltage	60			V	I_C=100 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	40			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=100 μA, I_C=0
$V_{BE(sat)}1$*	Base Saturation Voltage	0.75	0.85	0.95	V	I_C=150 mA, I_B=15 mA
$V_{BE(sat)}2$*	Base Saturation Voltage		1.0	1.2	V	I_C=500 mA, I_B=50 mA
f_T	Gain Bandwidth Product	200	400		MHz	V_{CE}=10 V, I_C=20 mA
C_{ob}	Output Capacitance		4.5	6.5	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		21	30	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	0.5	3.0	7.5	kΩ	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz
h_{re}	Voltage Feedback Ratio	0.1	3.5	8.0	$\times10^{-4}$	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz
h_{fe}	Small Signal Current Gain	20	150	250	—	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz
h_{oe}	Output Admittance	1.0	14	30	μS	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz

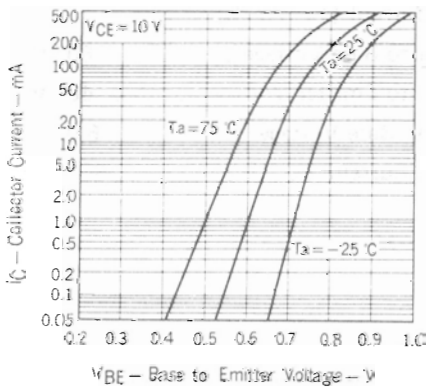
* Pulsed PW ≦ 300 μs, duty cycle ≦ 2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

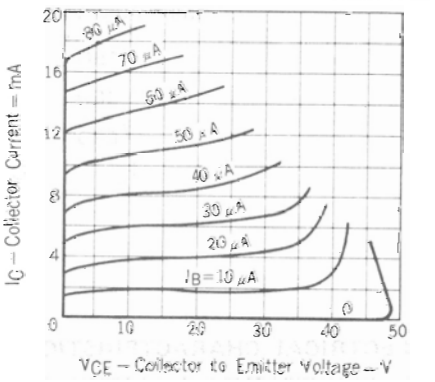
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



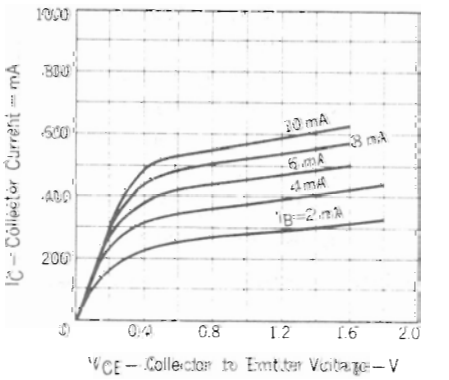
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



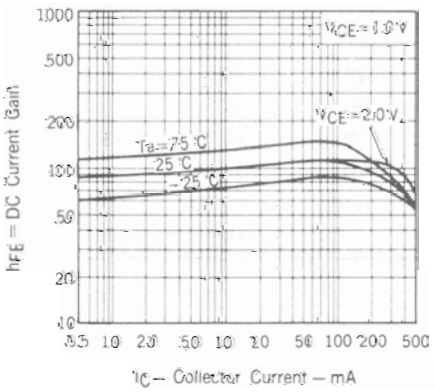
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



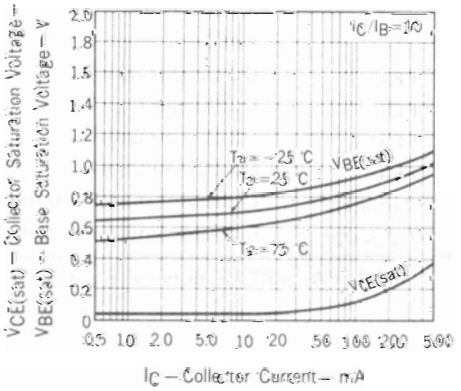
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



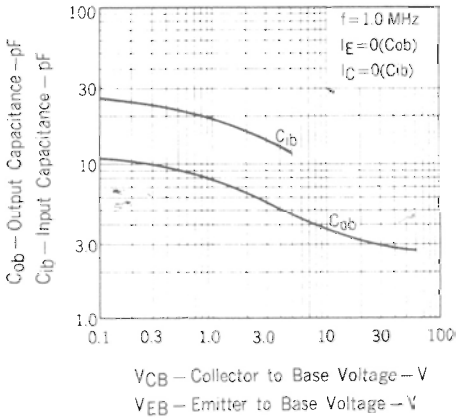
DC CURRENT GAIN vs. COLLECTOR CURRENT



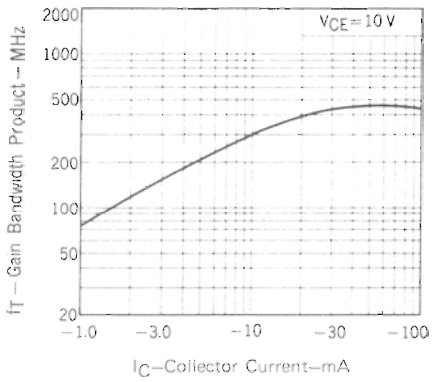
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



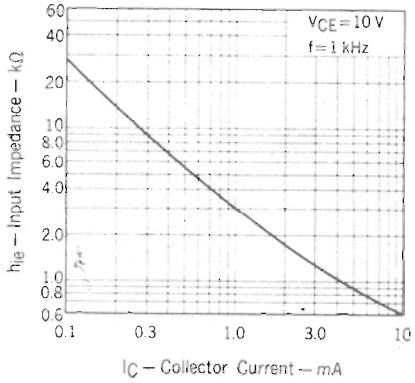
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



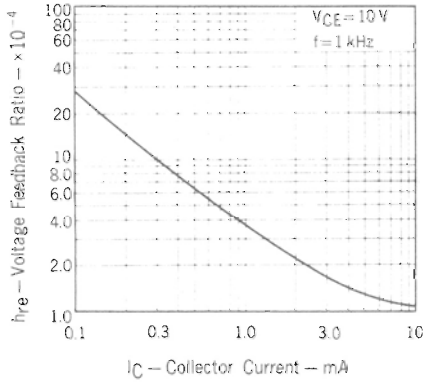
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



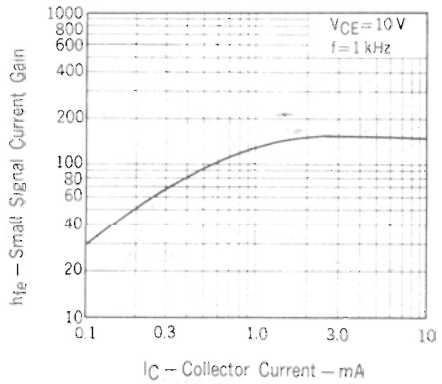
INPUT IMPEDANCE vs. COLLECTOR CURRENT



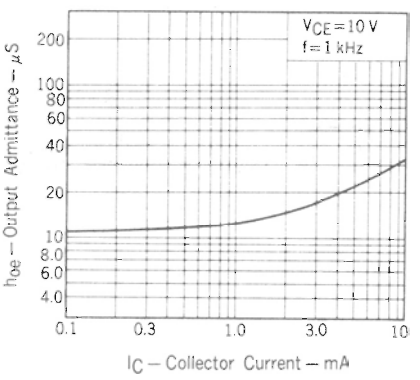
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



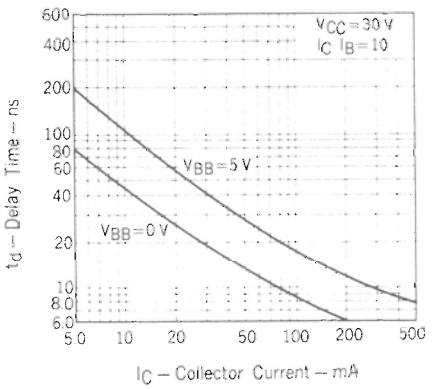
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



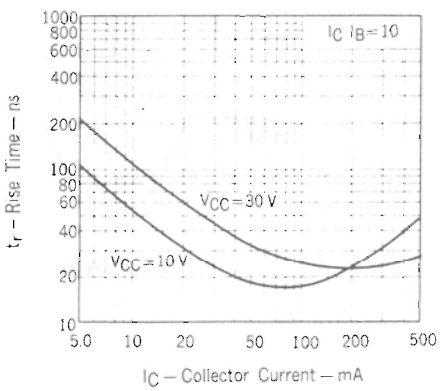
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



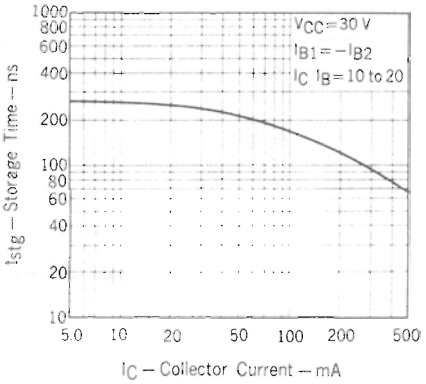
DELAY TIME vs. COLLECTOR CURRENT



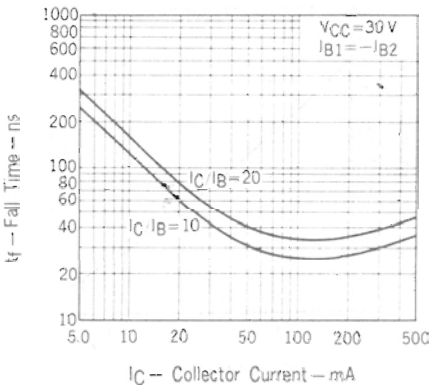
RISE TIME vs. COLLECTOR CURRENT



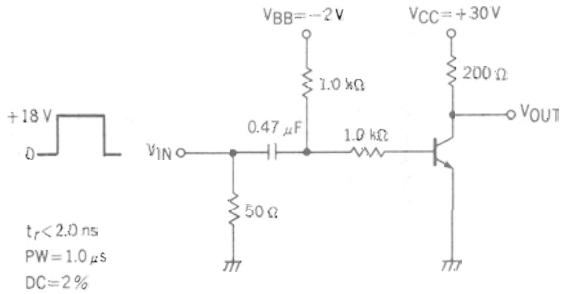
STORAGE TIME vs. COLLECTOR CURRENT



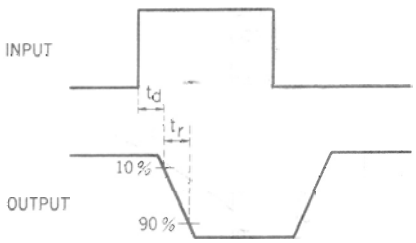
FALL TIME vs.
COLLECTOR CURRENT



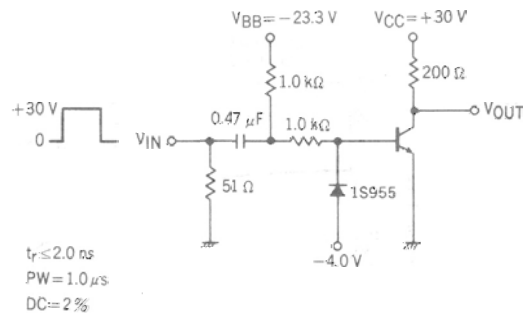
SWITCHING TIME TEST CIRCUIT



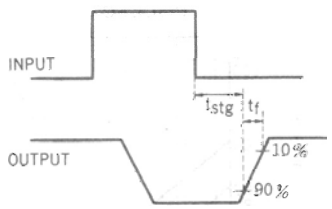
t_{on} SWITCHING



VOLTAGE WAVEFORMS



t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

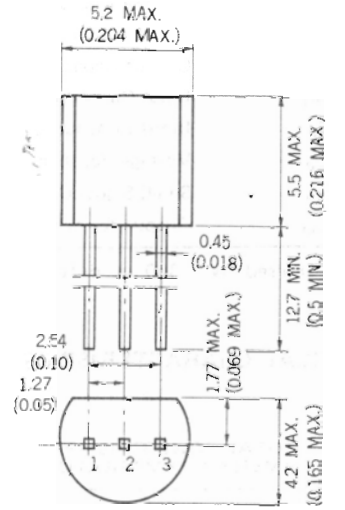
NPN SILICON TRANSISTOR
2N4401

DESCRIPTION The 2N4401 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power . . . P_T 625 mW at 25 °C
- High Voltage . . V_{CEO} 40 V
- High DC Current Gain h_{FE} 100 to 300 at 150 mA
- For Complementary Use with PNP Type 2N4403

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta=25 °C)

V_{CBO}	Collector to Base Voltage	60 V
V_{CEO}	Collector to Emitter Voltage	40 V
V_{EBO}	Emitter to Base Voltage	6.0 V
I_C	Collector Current	600 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			15	ns	V_{CC}=30 V, I_C=150 mA
t_r	Rise Time			20	ns	I_{B1}=15 mA, V_{EB}=−2 V
t_{stg}	Storage Time			225	ns	V_{CC}=30 V, I_C=150 mA
t_f	Fall Time			30	ns	I_{B1}=−I_{B2}=15 mA
h_{FE1}	DC Current Gain	20	190		—	V_{CE}=1.0 V, I_C=100 μA
h_{FE2}	DC Current Gain	40	200		—	V_{CE}=1.0 V, I_C=1.0 mA
h_{FE3}	DC Current Gain	80	220		—	V_{CE}=1.0 V, I_C=10 mA
h_{FE4}*	DC Current Gain	100	200	300	—	V_{CE}=1.0 V, I_C=150 mA
h_{FE5}*	DC Current Gain	40	100		—	V_{CE}=2.0 V, I_C=500 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.15	0.4	V	I_C=150 mA, I_B=15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.4	0.75	V	I_C=500 mA, I_B=50 mA

* Pulsed PW ≦ 300 μs, duty cycle ≦ 2 %

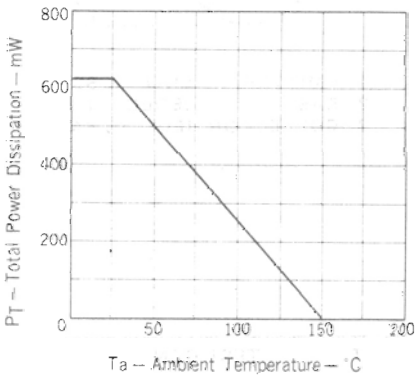
Additional Characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			100	nA	V_{CE}=35 V, V_{BE}=−0.4 V
I_{BEX}	Base Cutoff Current			−100	nA	V_{CE}=35 V, V_{BE}=−0.4 V
BV_{CBO}	Collector to Base Breakdown Voltage	60			V	I_C=100 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	40			V	I_C=1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=100 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	0.75	0.85	0.95	V	I_C=150 mA, I_B=15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		1.0	1.2	V	I_C=500 mA, I_B=50 mA
f_T	Gain Bandwidth Product	250	400		MHz	V_{CE}=10 V, I_C=20 mA
C_{ob}	Output Capacitance		4.5	6.5	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		21	30	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	1.0	5.0	15	kΩ	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz
h_{re}	Voltage Feedback Ratio	0.1	5.0	8.0	X10^{-4}	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz
h_{fe}	Small Signal Current Gain	40	180	500	—	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz
h_{oe}	Output Admittance	1.0	19	30	μS	V_{CE}=10 V, I_C=1.0 mA, f=1.0 kHz

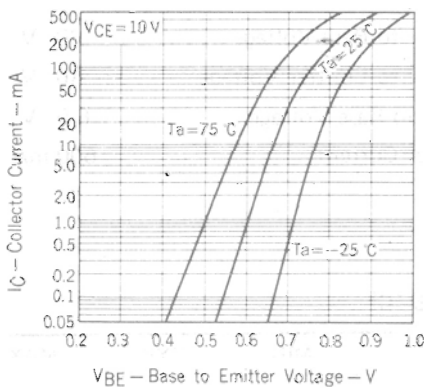
* Pulsed PW ≤300 μs, duty cycle ≤2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

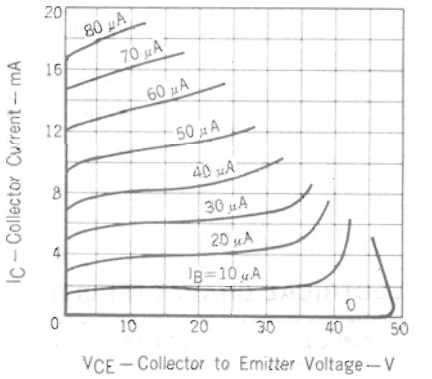
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



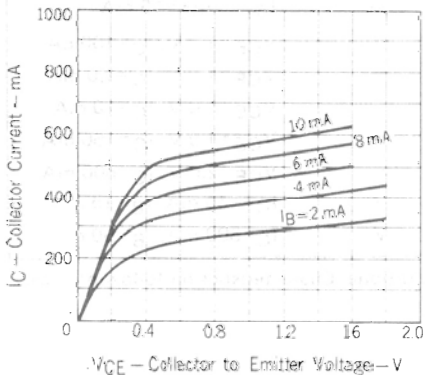
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



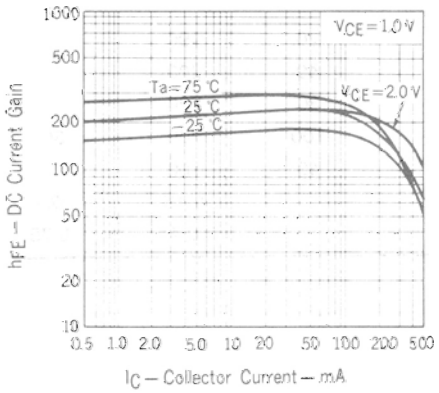
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



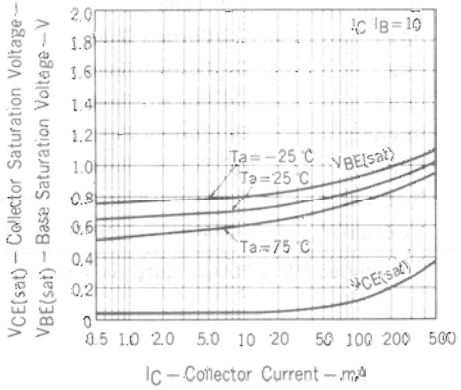
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



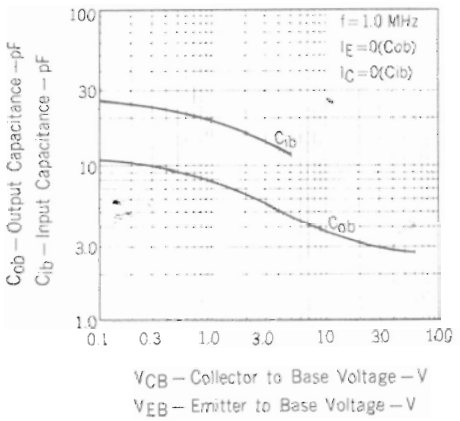
DC CURRENT GAIN vs. COLLECTOR CURRENT



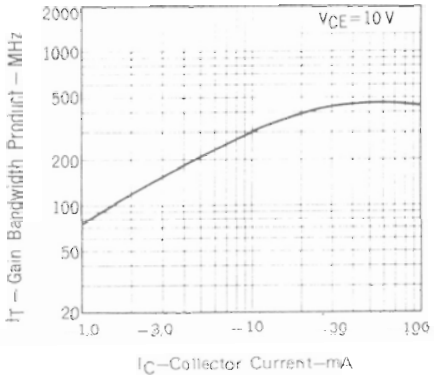
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



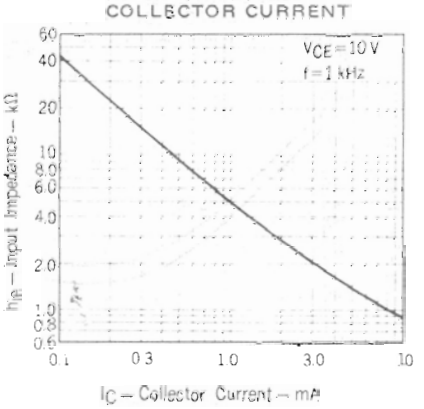
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



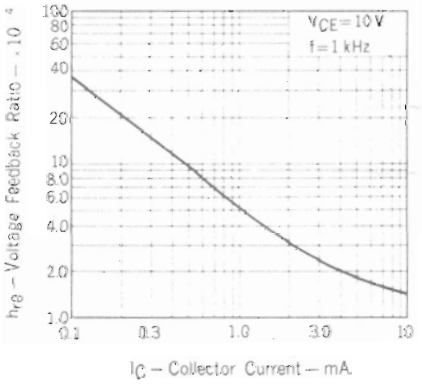
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



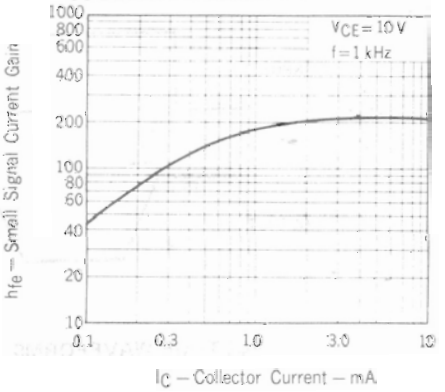
INPUT IMPEDANCE vs. COLLECTOR CURRENT



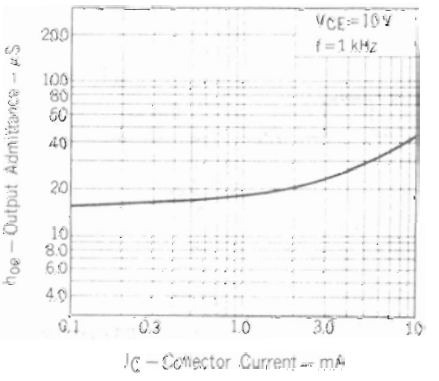
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



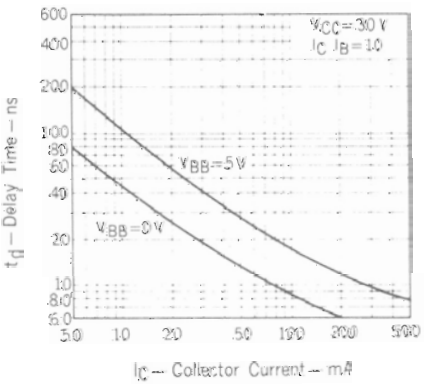
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



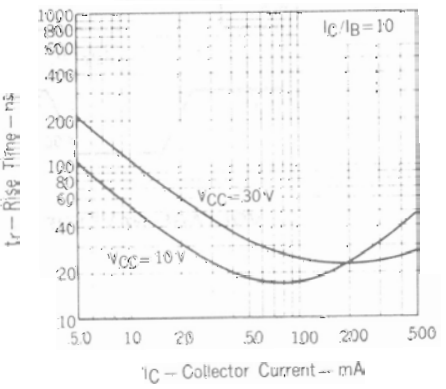
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



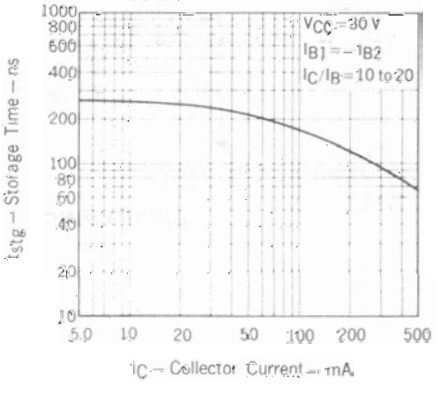
DELAY TIME vs. COLLECTOR CURRENT

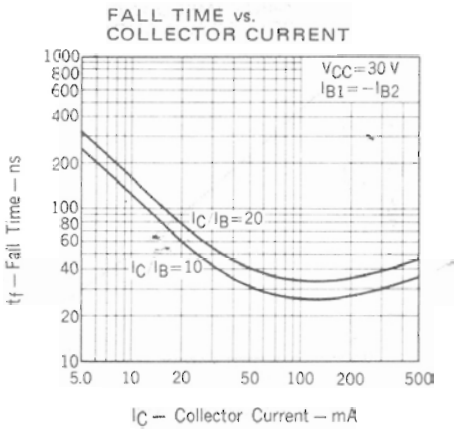


RISE TIME vs. COLLECTOR CURRENT

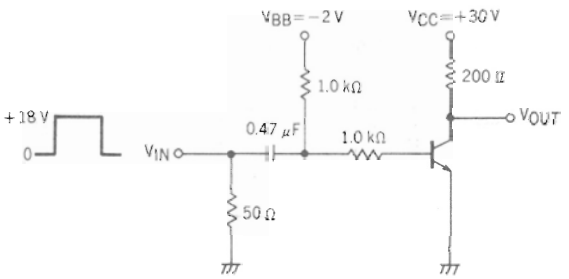


STORAGE TIME vs. COLLECTOR CURRENT



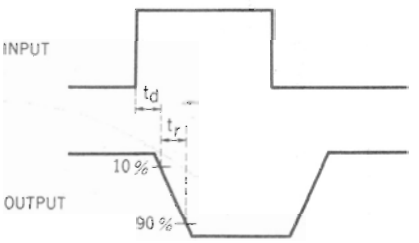


SWITCHING TIME TEST CIRCUIT

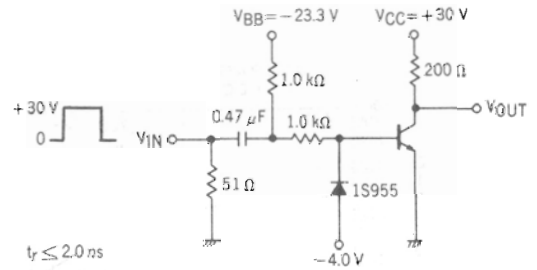


t_r<2.0 ns
PW=1.0 μs
DC=2 %

t_{on} SWITCHING

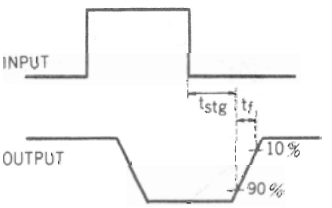


VOLTAGE WAVEFORMS



$t_r \leq 2.0$ ns
PW=1.0 μs
DC=2 %

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

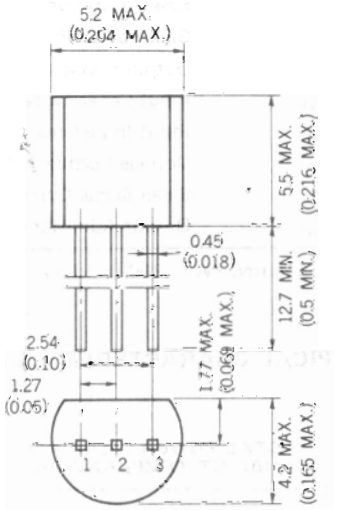
PNP SILICON TRANSISTOR
2N4402

DESCRIPTION The 2N4402 is designed for general purpose switching and amplifier applications.

FEATURES

- High Power . . . . P_T 625 mW at 25 °C
- High Voltage . . . V_{CEO} −40 V
- DC Current Gain h_{FE} 50 to 150 at −150 mA
- For Complementary Use with NPN Type 2N4400

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −40 V
- V_{CEO} Collector to Emitter Voltage . . . . . −40 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −600 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			15	ns	V_{CC}=−30 V, I_C=−150 mA
t_r	Rise Time			20	ns	I_{B1}=−15 mA, V_{EB}=2 V
t_{stg}	Storage Time			225	ns	V_{CC}=−30 V, I_C=−150 mA
t_f	Fall Time			30	ns	I_{B1}=−I_{B2}=−15 mA
h_{FE1}	DC Current Gain	30	95		—	V_{CE}=−1.0 V, I_C=−1.0 mA
h_{FE2}	DC Current Gain	50	110		—	V_{CE}=−1.0 V, I_C=−10 mA
h_{FE3}*	DC Current Gain	50	100	150	—	V_{CE}=−2.0 V, I_C=−150 mA
h_{FE4}*	DC Current Gain	20	40		—	V_{CE}=−2.0 V, I_C=−500 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		−0.2	−0.4	V	I_C=−150 mA, I_B=−15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		−0.5	−0.75	V	I_C=−500 mA, I_B=−50 mA

* Pulsed PW ≤300 μs, duty cycle ≤2 %

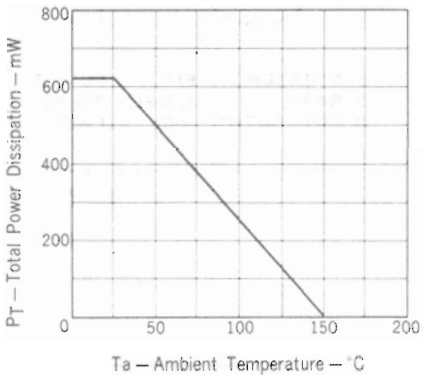
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			−100	nA	V_{CE}=−35 V, V_{BE}=0.4 V
I_{BEX}	Base Cutoff Current			100	nA	V_{CE}=−35 V, V_{BE}=0.4 V
BV_{CEO}	Collector to Base Breakdown Voltage	−40			V	I_C=−100 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−40			V	I_C=−1.0 mA, I_B=0
BV_{EEO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−100 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	−0.75	−0.9	−0.95	V	I_C=−150 mA, I_B=−15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		−1.1	−1.3	V	I_C=−500 mA, I_B=−50 mA
f_T	Gain Bandwidth Product	150	400		MHz	V_{CE}=−10 V, I_C=−20 mA
C_{ob}	Output Capacitance		5.0	8.5	pF	V_{CB}=−10 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		25	30	pF	V_{EB}=−0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	0.75	3.0	7.5	kΩ	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{re}	Voltage Feedback Ratio	0.1	3.0	8.0	X10^{-4}	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{fe}	Small Signal Current Gain	30	80	250	—	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{oe}	Output Admittance	1.0	15	100	μS	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz

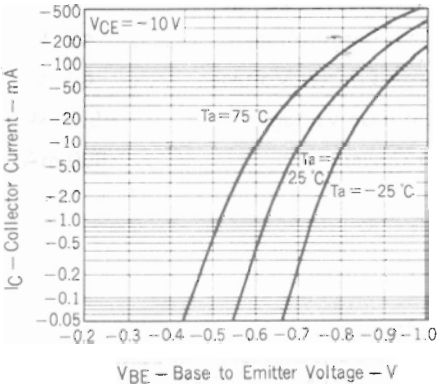
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

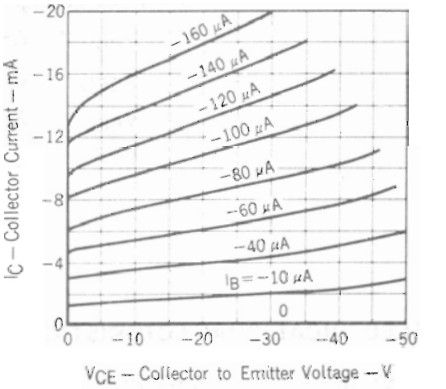
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



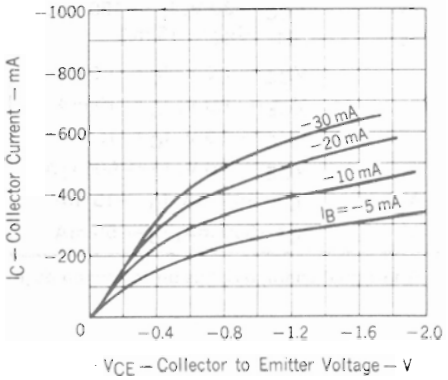
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



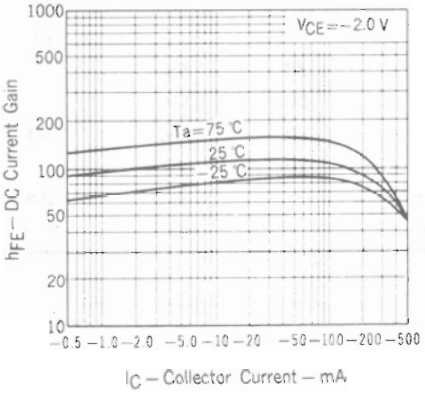
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



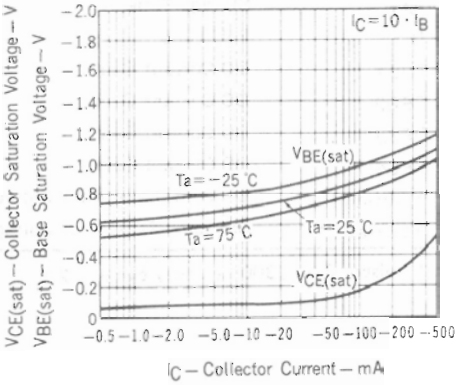
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



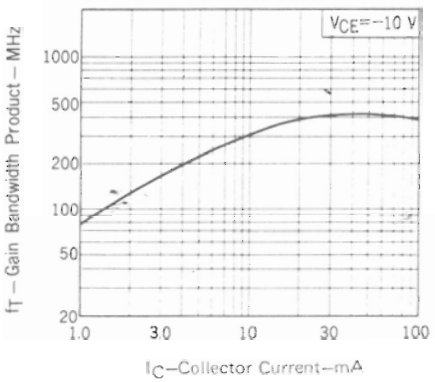
DC CURRENT GAIN vs. COLLECTOR CURRENT



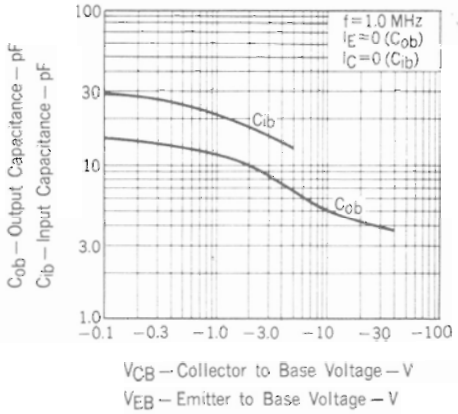
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



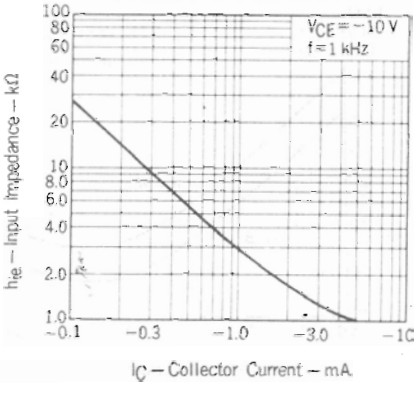
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



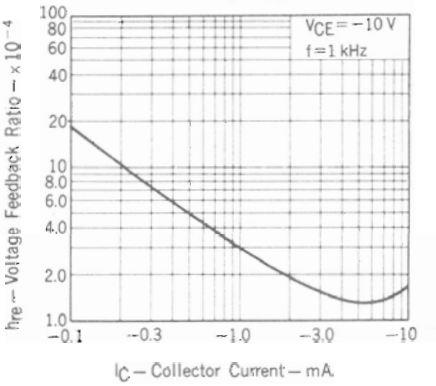
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



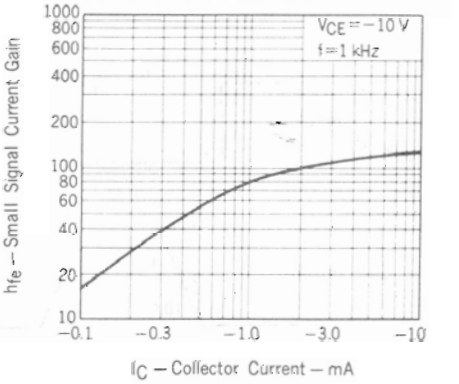
INPUT IMPEDANCE vs. COLLECTOR CURRENT



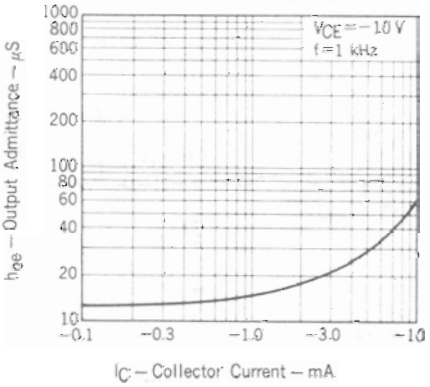
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



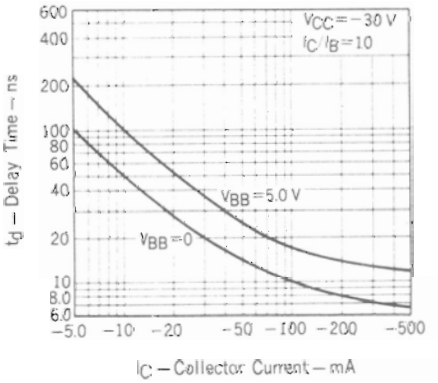
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



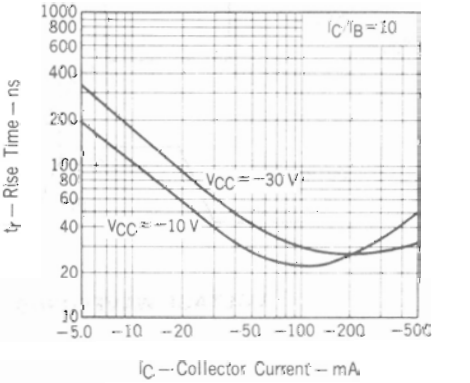
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



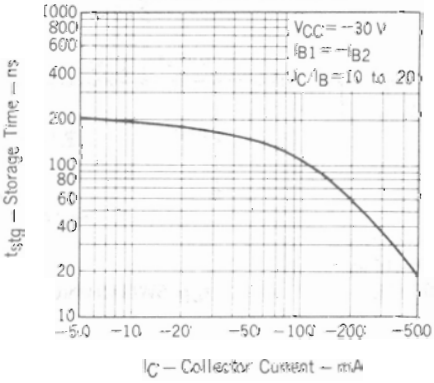
DELAY TIME vs. COLLECTOR CURRENT



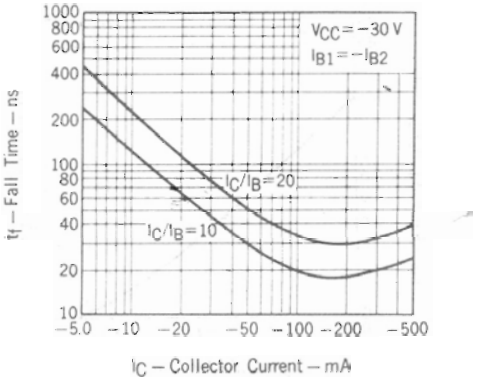
RISE TIME vs. COLLECTOR CURRENT



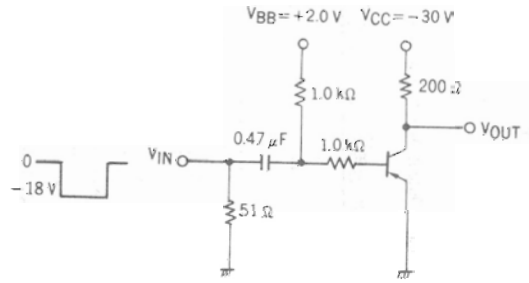
STORAGE TIME vs. COLLECTOR CURRENT



FALL TIME vs.
COLLECTOR CURRENT

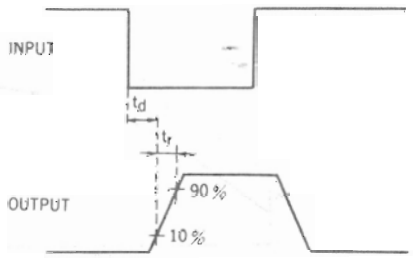


SWITCHING TIME TEST CIRCUIT

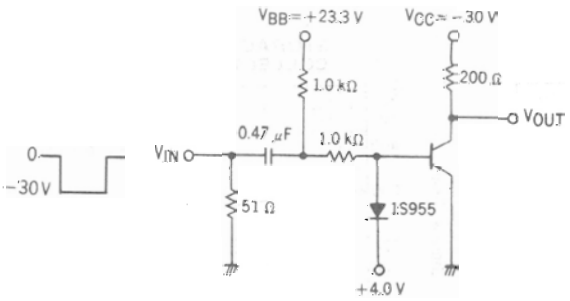


t_r < 2.0 ns
PW = 1.0 μs
DC = 2%

t_{on} SWITCHING

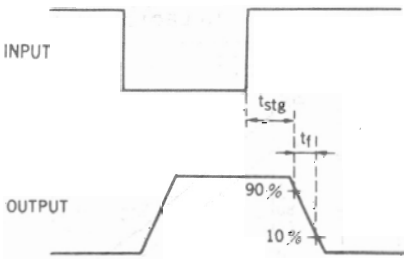


VOLTAGE WAVEFORMS



t_r ≤ 2.0 ns
PW ≥ 1.0 μs
DC = 2%

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

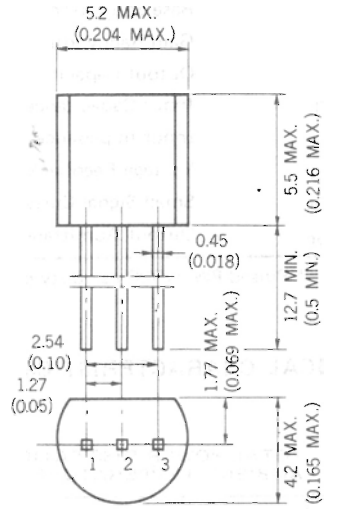
PNP SILICON TRANSISTOR
2N4403

DESCRIPTION The 2N4403 is designed for general purpose switching and amplifier applications

FEATURES

- High Power . . . P_T 625 mW at 25 °C
- High Voltage . . V_{CEO} −40 V
- High DC Current Gain h_{FE} 100 to 300 at −150 mA
- For Complementary Use with NPN Type 2N4401

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −40 V
- V_{CEO} Collector to Emitter Voltage . . . . . −40 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −600 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			15	ns	V_{CC}=−30 V, I_C=−150 mA
t_r	Rise Time			20	ns	I_{B1}=−15 mA, V_{EB}=2 V
t_{stg}	Storage Time			225	ns	V_{CC}=−30 V, I_C=−150 mA
t_f	Fall Time			30	ns	I_{B1}=−I_{B2}=−15 mA
h_{FE1}	DC Current Gain	30	130		—	V_{CE}=−1.0 V, I_C=−100 μA
h_{FE2}	DC Current Gain	60	150		—	V_{CE}=−1.0 V, I_C=−1.0 mA
h_{FE3}	DC Current Gain	100	170		—	V_{CE}=−1.0 V, I_C=−10 mA
h_{FE4}*	DC Current Gain	100	140	300	—	V_{CE}=−2.0 V, I_C=−150 mA
h_{FE5}*	DC Current Gain	20	40		—	V_{CE}=−2.0 V, I_C=−500 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		−0.2	−0.4	V	I_C=−150 mA, I_B=−15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		−0.5	−0.75	V	I_C=−500 mA, I_B=−50 mA

* Pulsed PW ≦300 μs, duty cycle ≦2 %

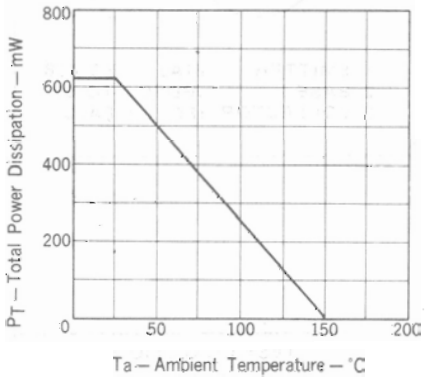
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			−100	nA	V_{CE}=−35 V, V_{BE}=0.4 V
I_{BEX}	Base Cutoff Current			100	nA	V_{CE}=−35 V, V_{BE}=0.4 V
BV_{CBO}	Collector to Base Breakdown Voltage	−40			V	I_C=−100 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−40			V	I_C=−1.0 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−100 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	−0.75	−0.9	−0.95	V	I_C=−150 mA, I_B=−15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		−1.1	−1.3	V	I_C=−500 mA, I_B=−50 mA
f_T	Gain Bandwidth Product	200	400		MHz	V_{CE}=−10 V, I_C=−20 mA
C_{ob}	Output Capacitance		5.0	8.5	pF	V_{CB}=−10 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		25	30	pF	V_{EB}=−0.5 V, I_C=0, f=1 MHz
h_{ie}	Input Impedance	1.5	7.0	15	kΩ	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{re}	Voltage Feedback Ratio	0.1	4.5	8.0	$X10^{-4}$	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{fe}	Small Signal Current Gain	60	250	500	−	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz
h_{oe}	Output Admittance	1.0	35	100	μS	V_{CE}=−10 V, I_C=−1.0 mA, f=1.0 kHz

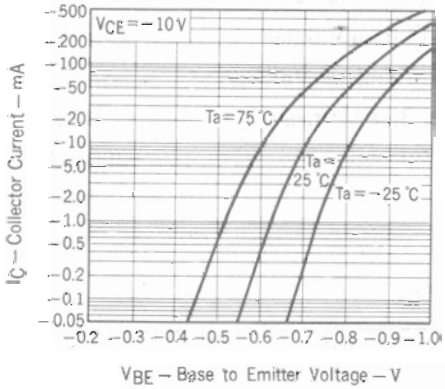
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

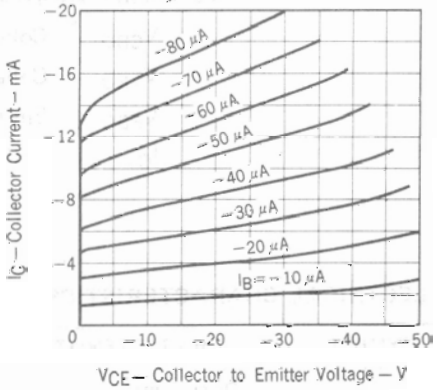
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



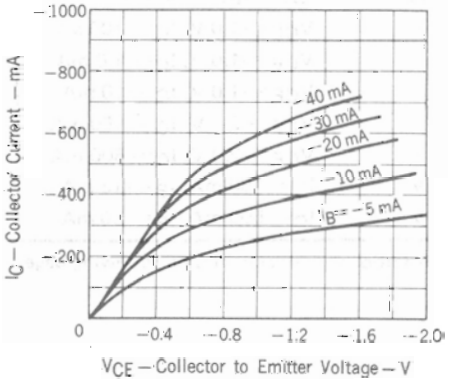
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



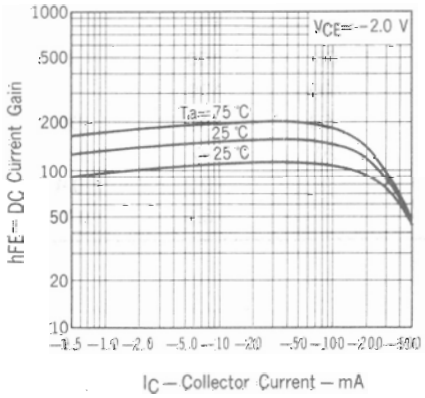
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



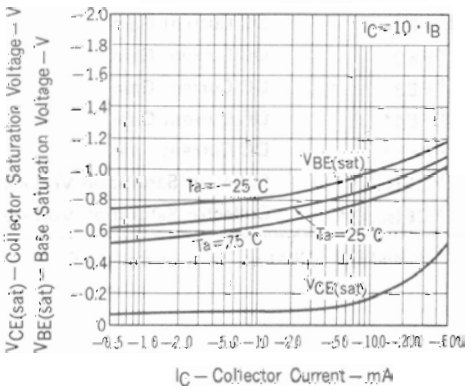
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



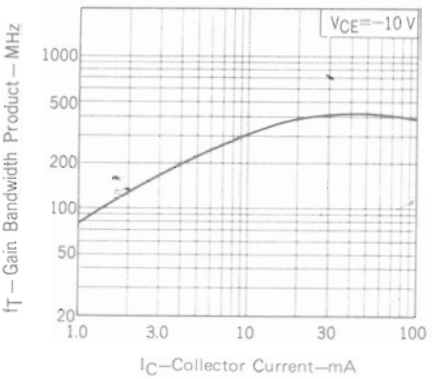
DC CURRENT GAIN vs. COLLECTOR CURRENT



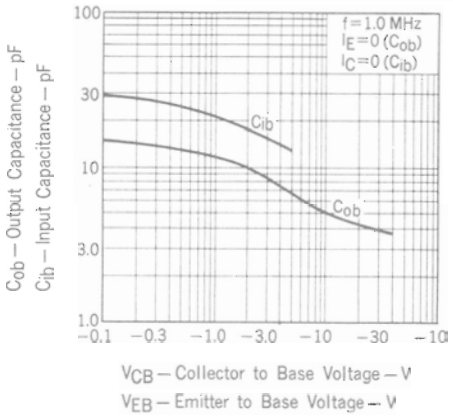
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



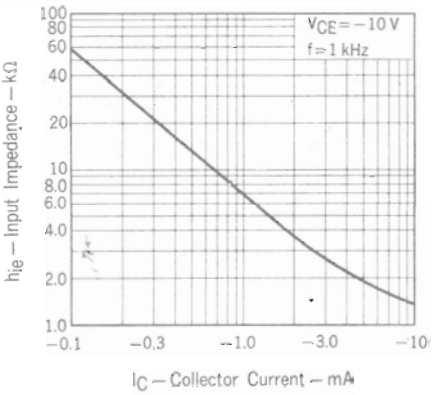
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



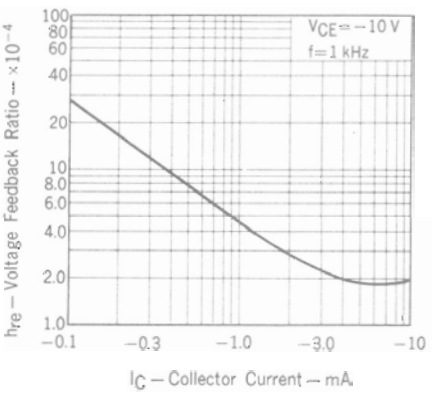
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



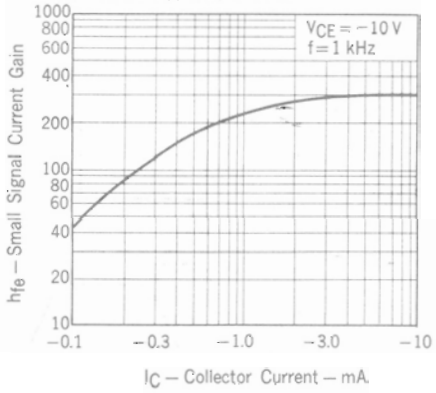
INPUT IMPEDANCE vs. COLLECTOR CURRENT



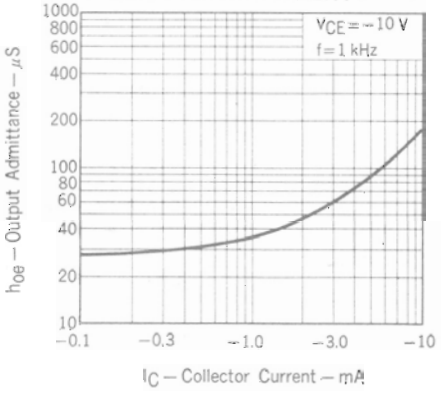
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



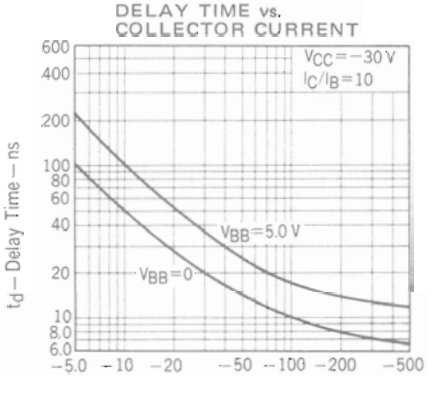
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



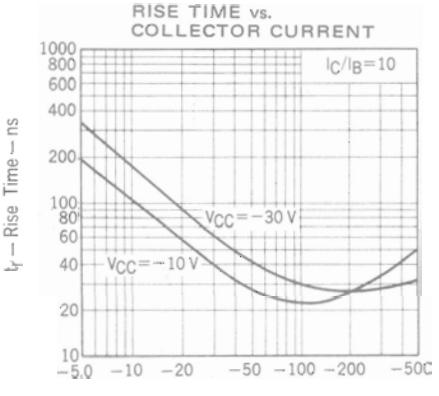
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



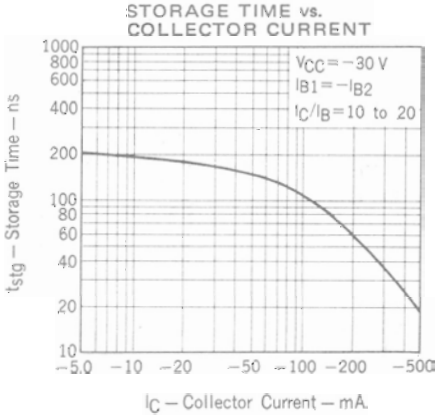
DELAY TIME vs. COLLECTOR CURRENT



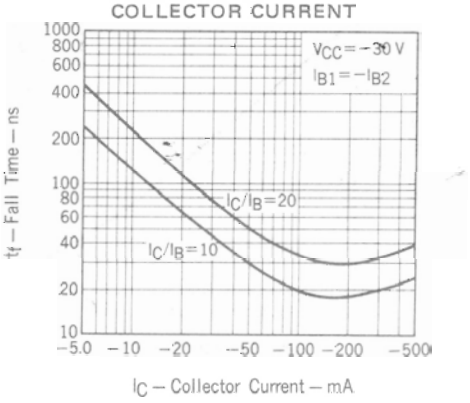
RISE TIME vs. COLLECTOR CURRENT



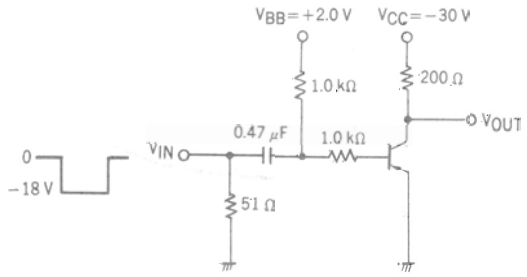
STORAGE TIME vs. COLLECTOR CURRENT



FALL TIME vs.
COLLECTOR CURRENT

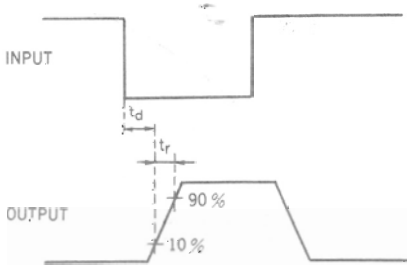


SWITCHING TIME TEST CIRCUIT

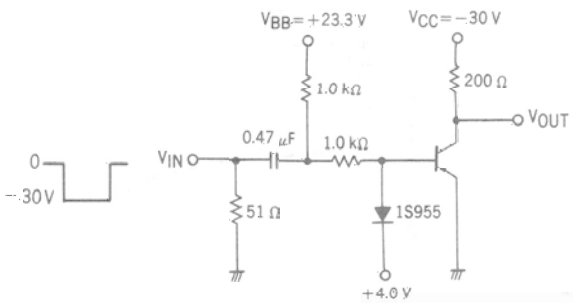


t_r < 2.0 ns
PW = 1.0 μs
DC = 2 %

t_{on} SWITCHING

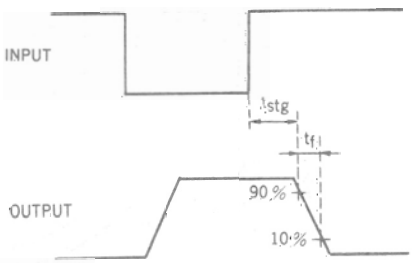


VOLTAGE WAVEFORMS



t_r ≤ 2.0 ns
PW ≥ 1.0 μs
DC = 2 %

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

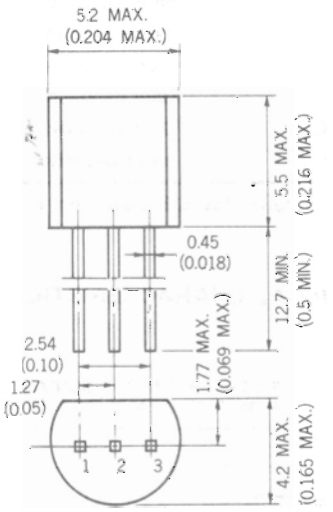
NPN SILICON TRANSISTOR
NT2222

DESCRIPTION The NT2222 is designed for general purpose amplifier and high-speed, medium power switching applications.

FEATURES

- High Frequency Current Gain.
- Low Collector Saturation Voltage.
- High Speed Switching.
- For Complementary Use with PNP Type NT2907.
- NT2222 Electrically Similar to 2N2222.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC: TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO} Collector to Base Voltage . . . . . 60 V

V_{CEO} Collector to Emitter Voltage . . . . . 30 V

V_{EBO} Emitter to Base Voltage . . . . . 5.0 V

I_C Collector Current . . . . . 800 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			10	ns	V_{CC}=30 V, V_{BE}=−0.5 V
t_r	Rise Time			25	ns	I_C=150 mA, I_{B1}=15 mA
t_{stg}	Storage Time			225	ns	V_{CC}=30 V, I_C=15 mA
t_f	Fall Time			60	ns	I_{B1}=−I_{B2}=15 mA
h_{FE1}	DC Current Gain	35	180		—	V_{CE}=10 V, I_C=100 μA
h_{FE2}	DC Current Gain	50	190		—	V_{CE}=10 V, I_C=1 mA
h_{FE3}*	DC Current Gain	75	210		—	V_{CE}=10 V, I_C=10 mA
h_{FE4}*	DC Current Gain	100	230	300	—	V_{CE}=10 V, I_C=150 mA
h_{FE5}*	DC Current Gain	30	180		—	V_{CE}=10 V, I_C=500 mA
h_{FE6}*	DC Current Gain	50	200		—	V_{CE}=1.0 V, I_C=150 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.13	0.4	V	I_C=150 mA, I_B=15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.3	1.6	V	I_C=500 mA, I_B=50 mA

* Pulsed PW ≤300 μs, duty cycle ≤2%

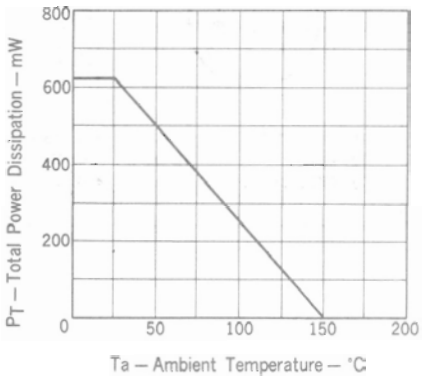
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CBO1}	Collector Cutoff Current			10	nA	V_{CB}=50 V, I_E=0
I_{CBO2}	Collector Cutoff Current			10	μA	V_{CB}=50 V, I_E=0, Ta=150 °C
I_{EBO}	Emitter Cutoff Current			10	nA	V_{EB}=3.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	60			V	I_C=10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	30			V	I_C=10 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	5.0			V	I_E=10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage		0.85	1.3	V	I_C=150 mA, I_B=15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		1.0	2.6	V	I_C=500 mA, I_B=50 mA
$\|h_{fe}\|$	High Frequency Current Gain	2.5	4.0		—	V_{CE}=20 V, I_C=20 mA, f=100 MHz
f_T	Gain Bandwidth Product	250	400		MHz	V_{CE}=20 V, I_C=20 mA, f=100 MHz
C_{ob}	Output Capacitance		3.8	8	pF	V_{CB}=10 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		20	30	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz

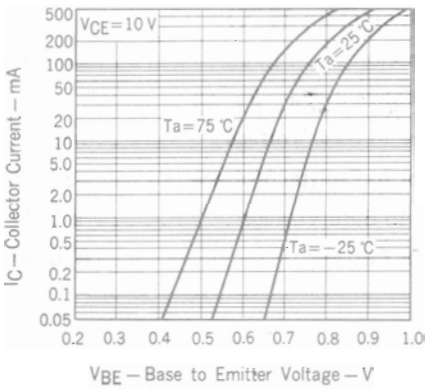
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

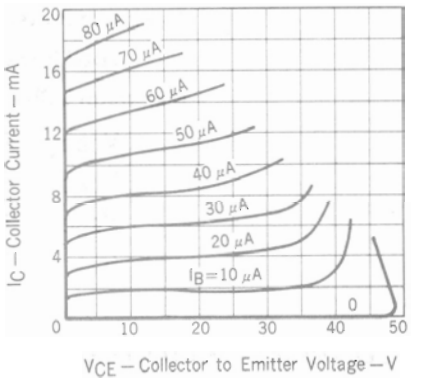
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



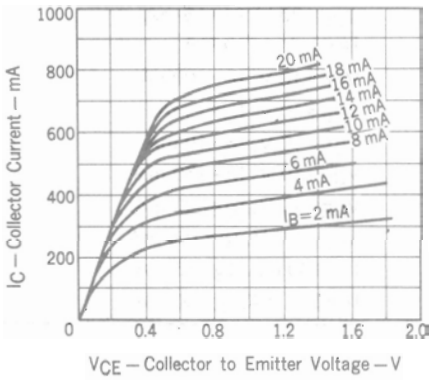
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



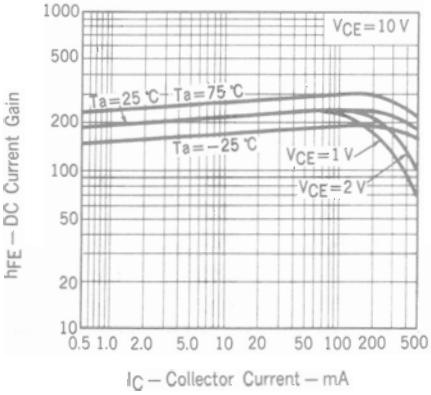
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



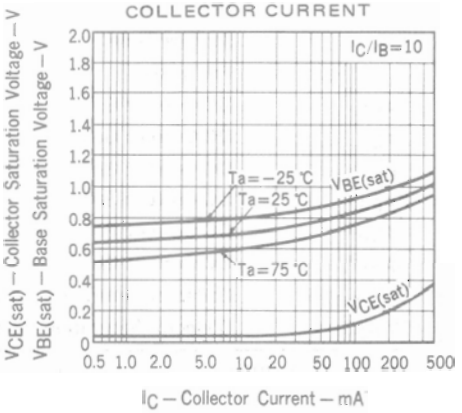
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



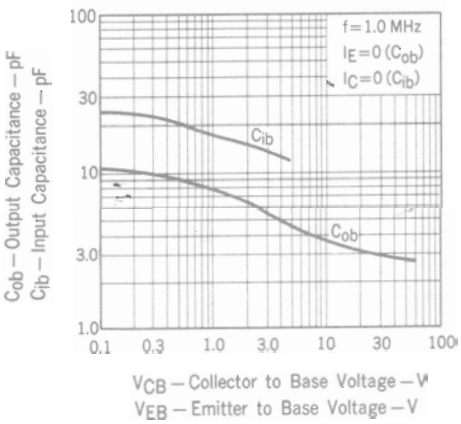
DC CURRENT GAIN vs. COLLECTOR CURRENT



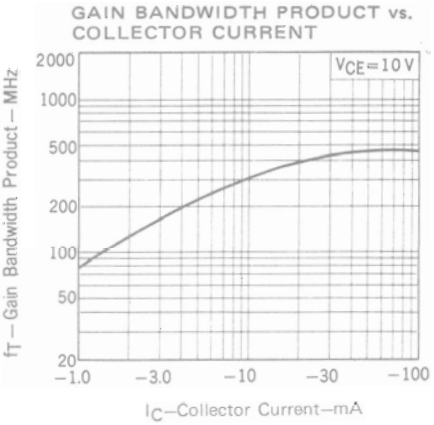
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



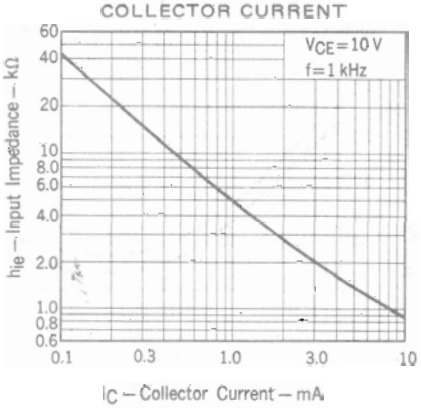
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



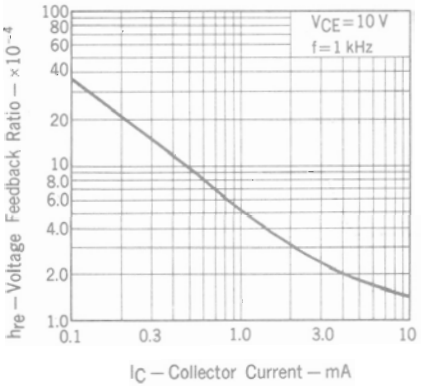
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



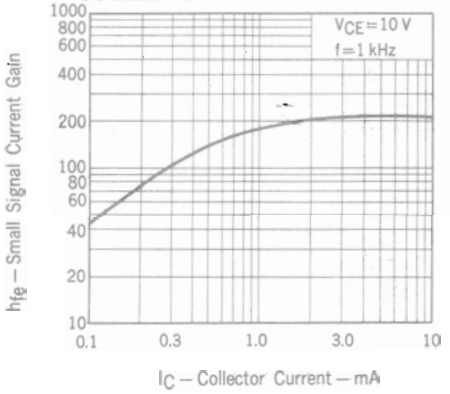
INPUT IMPEDANCE vs. COLLECTOR CURRENT



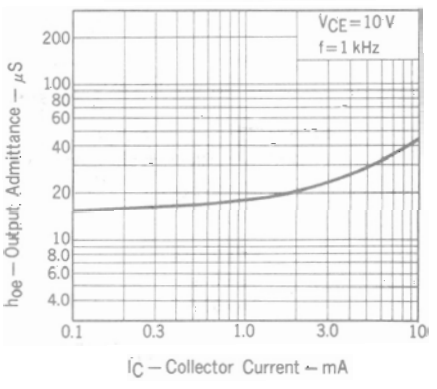
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



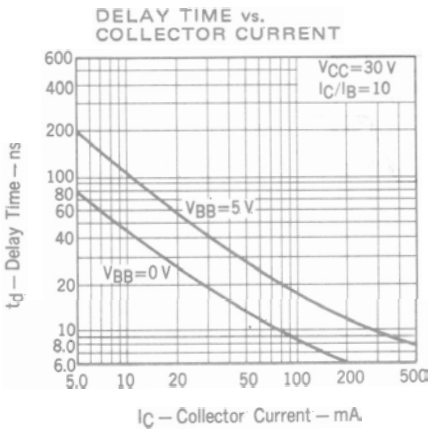
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



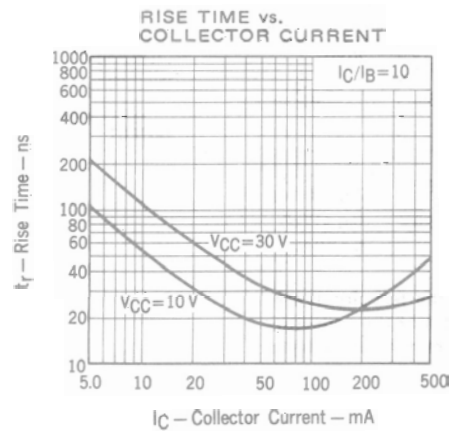
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



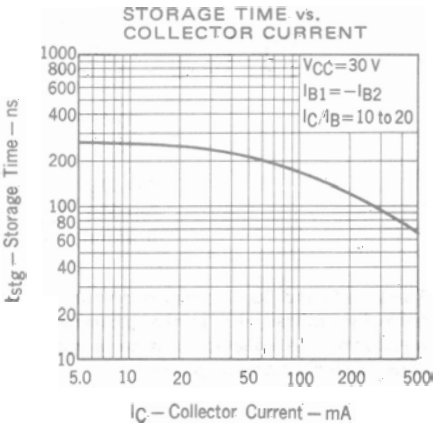
DELAY TIME vs. COLLECTOR CURRENT



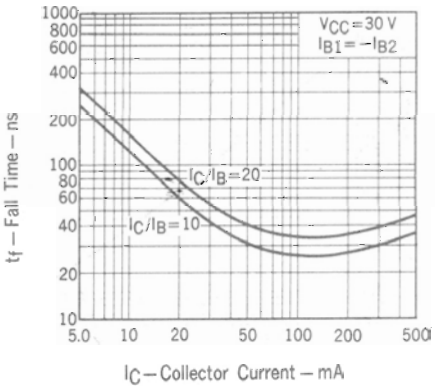
RISE TIME vs. COLLECTOR CURRENT



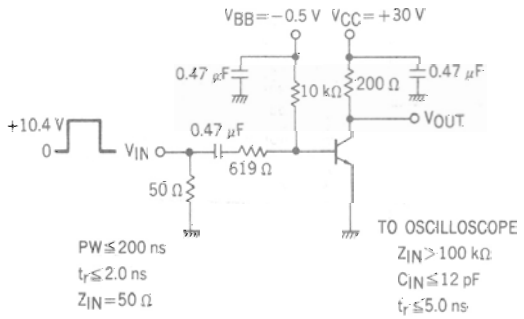
STORAGE TIME vs. COLLECTOR CURRENT



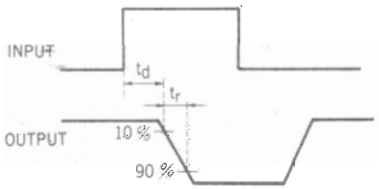
FALL TIME vs.
COLLECTOR CURRENT



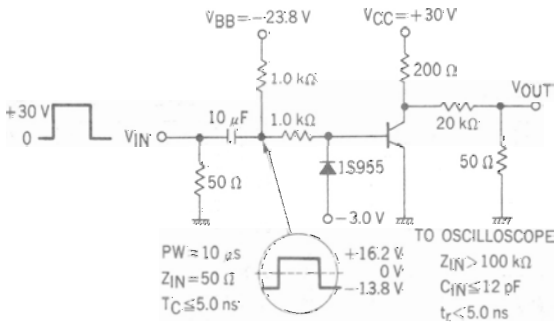
SWITCHING TIME TEST CIRCUIT



t_{on} SWITCHING

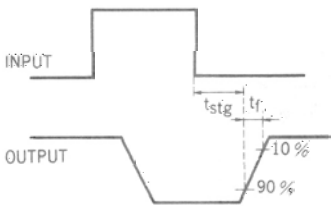


VOLTAGE WAVEFORMS



The 20 kΩ and 50 Ω resistors on the output of the test circuit are normally omitted, due to the excessive attenuation of the collector waveform. The collector voltage is monitored directly with a high impedance oscilloscope probe.

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

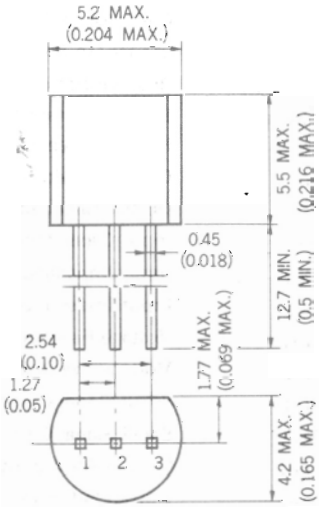
NPN SILICON TRANSISTOR
NT2222A

DESCRIPTION The NT2222A is designed for general purpose amplifier and high-speed, medium-power switching applications.

FEATURES

- High Frequency Current Gain.
- Low Collector Saturation Voltage.
- High speed Switching.
- For Complementary Use with PNP Type NT2907A.
- NT2222A Electrically Similar to 2N2222A.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	75 V
V_{CEO}	Collector to Emitter Voltage	40 V
V_{EBO}	Emitter to Base Voltage	6.0 V
I_C	Collector Current	800 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			10	ns	V_{CC} = 30 V, V_{BE} = −0.5 V
t_r	Rise Time			25	ns	I_C = 150 mA, I_{B1} = 15 mA
t_{stg}	Storage Time			225	ns	V_{CC} = 30 V, I_C = 150 mA
t_f	Fall Time			60	ns	I_{B1} = −I_{B2} = 15 mA
h_{FE1}	DC Current Gain	35	180		−	V_{CE} = 10 V, I_C = 100 μA
h_{FE2}	DC Current Gain	50	190		−	V_{CE} = 10 V, I_C = 1 mA
h_{FE3}*	DC Current Gain	75	210		−	V_{CE} = 10 V, I_C = 10 mA
h_{FE4}*	DC Current Gain	100	230	300	−	V_{CE} = 10 V, I_C = 150 mA
h_{FE5}*	DC Current Gain	40	180		−	V_{CE} = 10 V, I_C = 500 mA
h_{FE6}*	DC Current Gain	50	200		−	V_{CE} = 1.0 V, I_C = 150 mA
h_{FE7}*	DC Current Gain	35			−	V_{CE} = 10 V, I_C = 10 mA, Ta = −55 °C
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.13	0.3	V	I_C = 150 mA, I_B = 15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.3	1.0	V	I_C = 500 mA, I_B = 50 mA

* Pulsed PW ≤ 300 μs, duty cycle ≤ 2 %

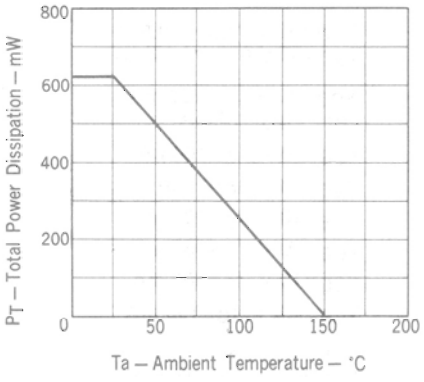
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			10	nA	V_{CE}=60 V, V_{BE}=−3 V
I_{BEX}	Base Cutoff Current			−20	nA	V_{CE}=60 V, V_{BE}=−3 V
I_{CBO1}	Collector Cutoff Current			10	nA	V_{CB}=60 V, I_E=0
I_{CBO2}	Collector Cutoff Current			10	μA	V_{CB}=60 V, I_E=0, Ta=150 °C
I_{EBO}	Emitter Cutoff Current			10	nA	V_{EB}=3.0 V, I_C=0
BV_{CBO}	Collector to Base Breakdown Voltage	75			V	I_C=10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	40			V	I_C=10 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	6.0			V	I_E=10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	0.6	0.85	1.2	V	I_C=150 mA, I_B=15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		1.0	2.0	V	I_C=500 mA, I_B=50 mA
$\|h_{fe}\|$	High Frequency Current Gain	3.0	4.0		—	V_{CE}=20 V, I_C=20 mA, f=100 MHz
f_T	Gain Bandwidth Product	300	400		MHz	V_{CE}=20 V, I_C=20 mA, f=100 MHz
Cob	Output Capacitance		3.8	8	pF	V_{CB}=10 V, I_E=0, f=1 MHz
Cib	Input Capacitance		20	25	pF	V_{EB}=0.5 V, I_C=0, f=1 MHz
h_{ie1}	Input Impedance	2.0	5.0	8.0	kΩ	V_{CE}=10 V, I_C=1.0 mA, f=1 kHz
h_{ie2}	Input Impedance	0.25	0.8	1.25	kΩ	V_{CE}=10 V, I_C=10 mA, f=1 kHz
h_{re1}	Voltage Feedback Ratio		5.0	8.0	$\times 10^{-4}$	V_{CE}=10 V, I_C=1.0 mA, f=1 kHz
h_{re2}	Voltage Feedback Ratio		1.5	4.0	$\times 10^{-4}$	V_{CE}=10 V, I_C=10 mA, f=1 kHz
h_{fe1}	Small-Signal Current Gain	50	180	300	—	V_{CE}=10 V, I_C=1.0 mA, f=1 kHz
h_{fe2}	Small-Signal Current Gain	75	210	375	—	V_{CE}=10 V, I_C=10 mA, f=1 kHz
h_{oe1}	Output Admittance	5.0	18	35	μS	V_{CE}=10 V, I_C=1.0 mA, f=1 kHz
h_{oe2}	Output Admittance	25	45	200	μS	V_{CE}=10 V, I_C=10 mA, f=1 kHz
$C_{c\cdot rb'b}$	Collector to Base Time Constant			150	ps	V_{CB}=20 V, I_E=20 mA, f=31.8 MHz
NF	Noise Figure			4.0	dB	V_{CE}=10 V, I_C=100 μA, R_S=1 kΩ f=1.0 kHz

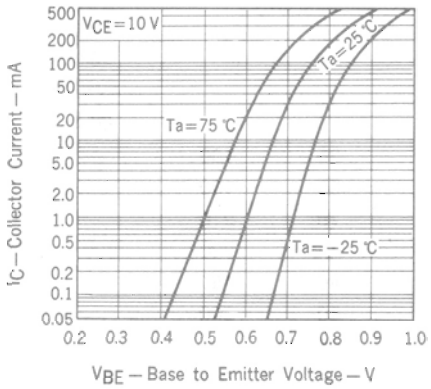
* Pulsed PW ≦300 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

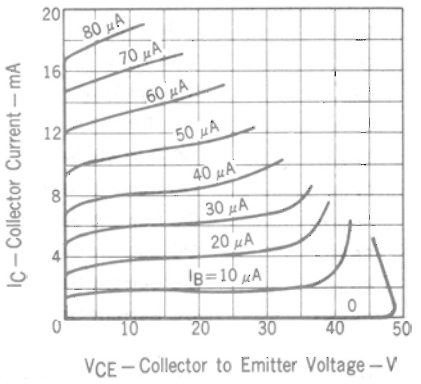
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



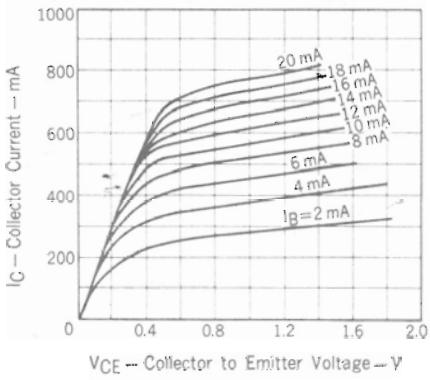
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



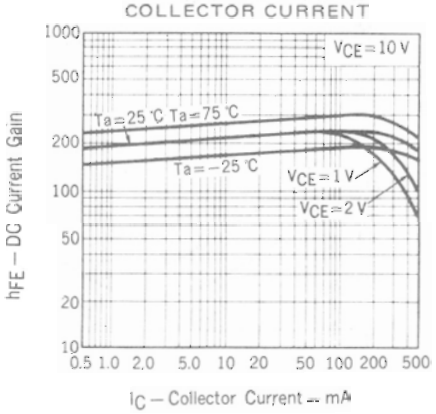
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



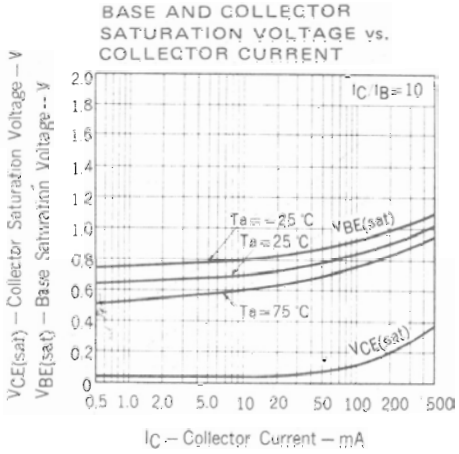
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



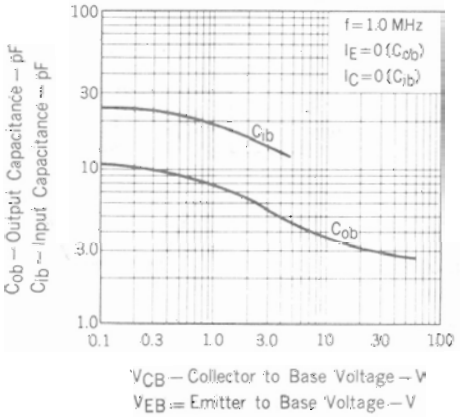
DC CURRENT GAIN vs. COLLECTOR CURRENT



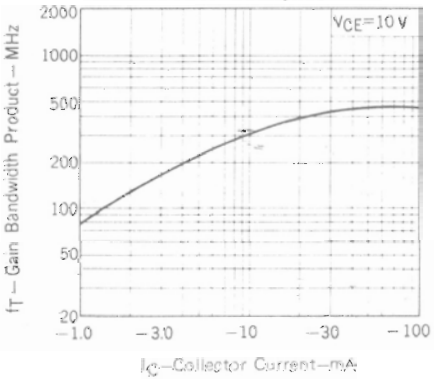
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



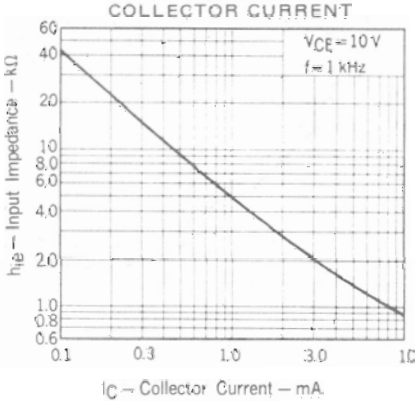
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



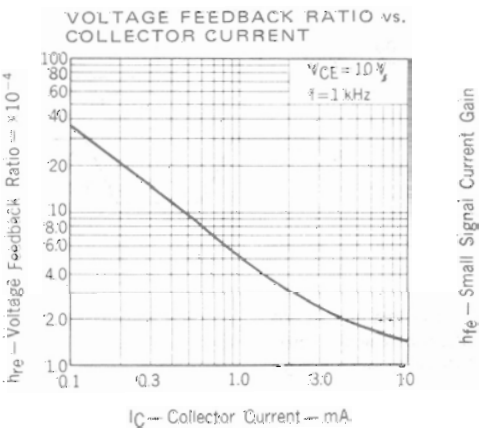
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



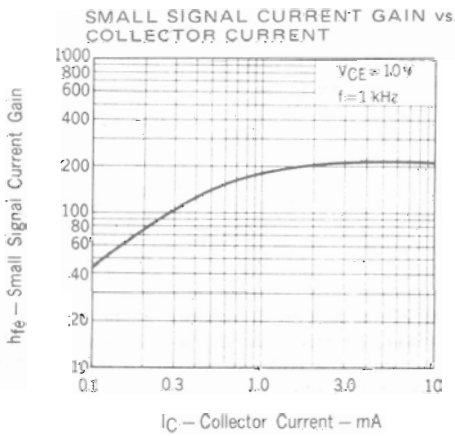
INPUT IMPEDANCE vs. COLLECTOR CURRENT



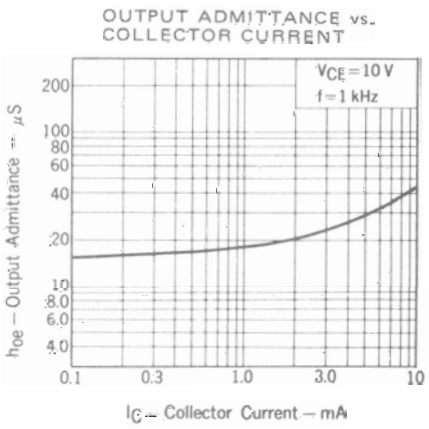
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



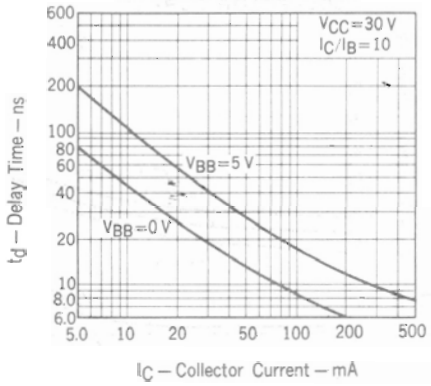
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



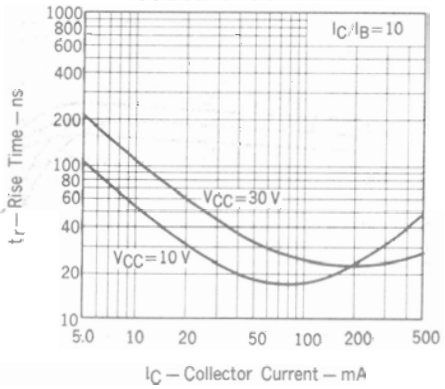
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



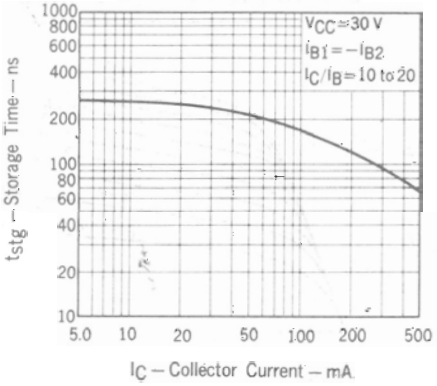
DELAY TIME vs. COLLECTOR CURRENT



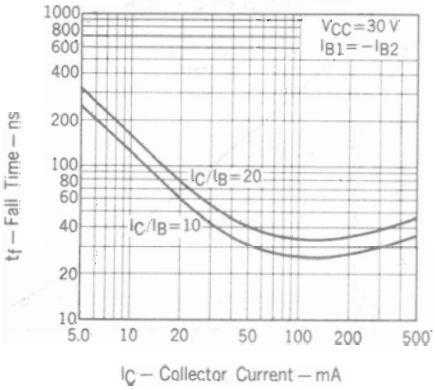
RISE TIME vs. COLLECTOR CURRENT



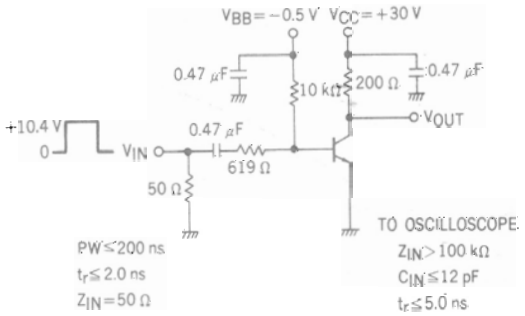
STORAGE TIME vs. COLLECTOR CURRENT



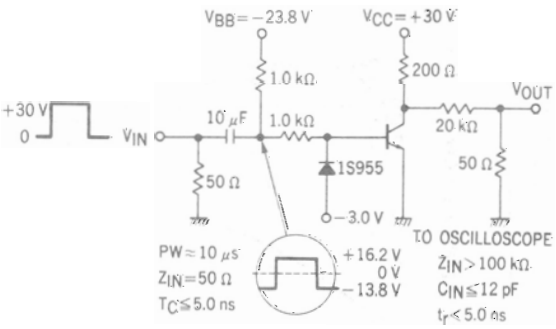
FALL TIME vs. COLLECTOR CURRENT



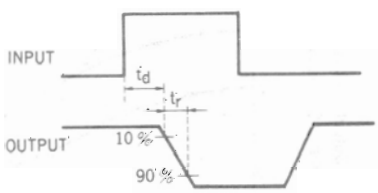
SWITCHING TIME TEST CIRCUIT



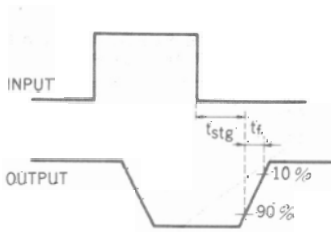
t_{on} SWITCHING



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



The 20 kΩ and 50 Ω resistors on the output of the test circuit are normally omitted, due to the excessive attenuation of the collector waveform. The collector voltage is monitored directly with a high impedance oscilloscope probe.

t_{off} SWITCHING

VOLTAGE WAVEFORMS

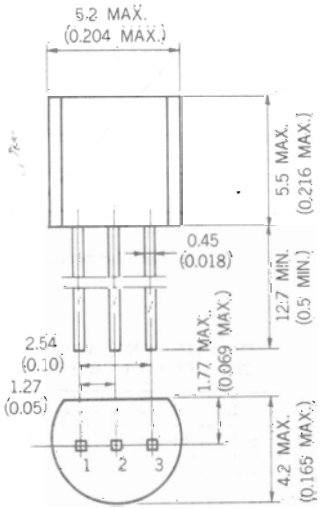
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
NT2369

DESCRIPTION The NT2369 is designed for general purpose amplifier and high speed switching applications.

FEATURES
- High Frequency Current Gain.
- High Speed Switching.
- NT2369 Electrically Similar to 2N2369.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	40 V
V_{CES}	Collector to Emitter Voltage	40 V
V_{CEO}	Collector to Emitter Voltage	15 V
V_{EBO}	Emitter to Base Voltage	4.5 V
I_C	Collector Current	200 mA
I_C	Collector Current (10 μs pulse)	500 mA

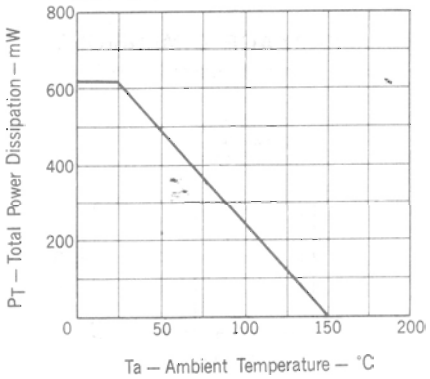
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			12	ns	V_{CC}=3.0 V, I_C=10 mA, I_{B1}=3.0 mA, V_{BE}=−1.5 V
t_{off}	Turn-off Time			18	ns	V_{CC}=3.0 V, I_C=10 mA, I_{B1}=3.0 mA, I_{B2}=−1.5 mA
t_{stg}	Storage Time			13	ns	I_C=10 mA, I_{B1}=−I_{B2}=10 mA
h_{fe}	High Frequency Current Gain	5.0	7.5			V_{CE}=10 V, I_C=10 mA, f=100 MHz
f_T	Gain Bandwidth Product	500	750		MHz	V_{CE}=10 V, I_C=10 mA, f=100 MHz
C_{ob}	Output Capacitance		1.8	4.0	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
h_{FE1}*	DC Current Gain	40	90	120	—	V_{CE}=1.0 V, I_C=10 mA
h_{FE2}*	DC Current Gain	20	35		—	V_{CE}=2.0 V, I_C=100 mA
h_{FE3}*	DC Current Gain	20			—	V_{CE}=1.0 V, I_C=10 mA, Ta=−55 °C
$V_{CE(sat)}$*	Collector Saturation Voltage		0.15	0.25	V	I_C=10 mA, I_B=1.0 mA
$V_{BE(sat)}$*	Base Saturation Voltage	0.7	0.78	0.85	V	I_C=10 mA, I_B=1.0 mA
BV_{CBO}	Collector to Base Breakdown Voltage	40			V	I_C=10 μA, I_E=0
BV_{CES}	Collector to Emitter Breakdown Voltage	40			V	I_C=10 μA, V_{BE}=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	15			V	I_C=10 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	4.5			V	I_E=10 μA, I_C=0
I_{CBO1}	Collector Cutoff Current			0.4	μA	V_{CB}=20 V, I_E=0
I_{CBO2}	Collector Cutoff Current			30	μA	V_{CB}=20 V, I_E=0, Ta=125 °C

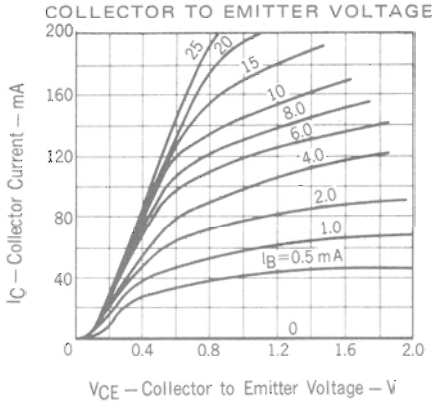
* Pulsed PW ≤350 μs, duty cycle ≤2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

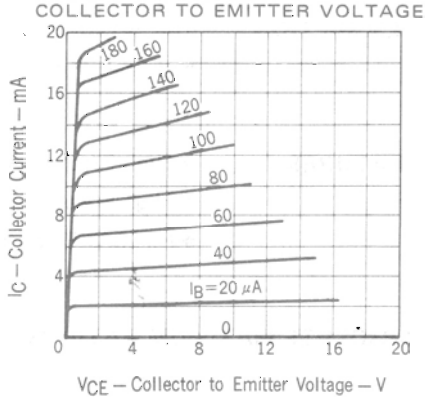
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



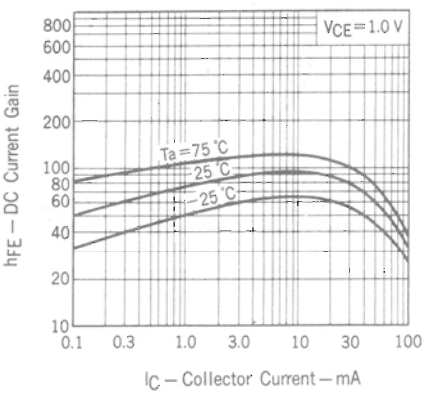
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



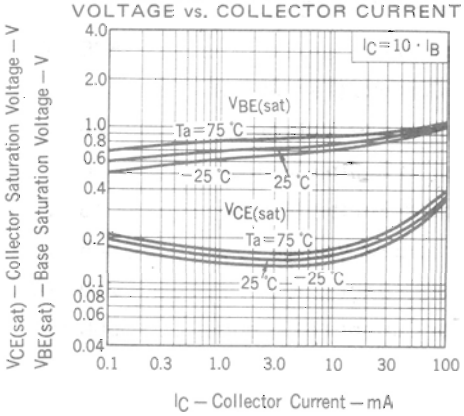
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



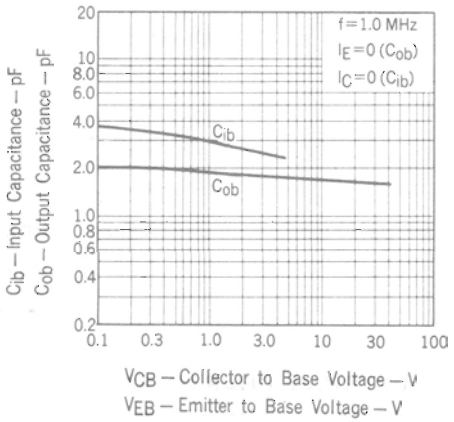
DC CURRENT GAIN vs. COLLECTOR CURRENT



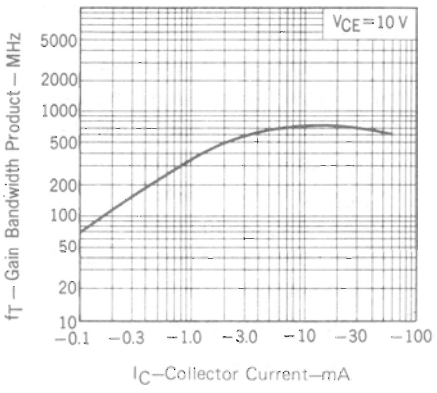
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



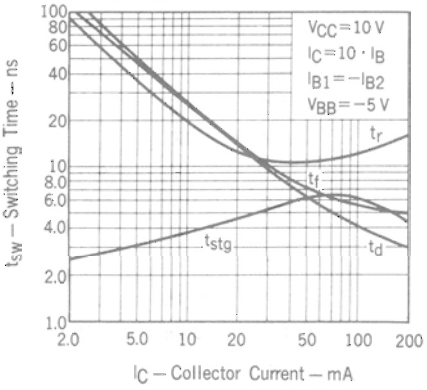
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



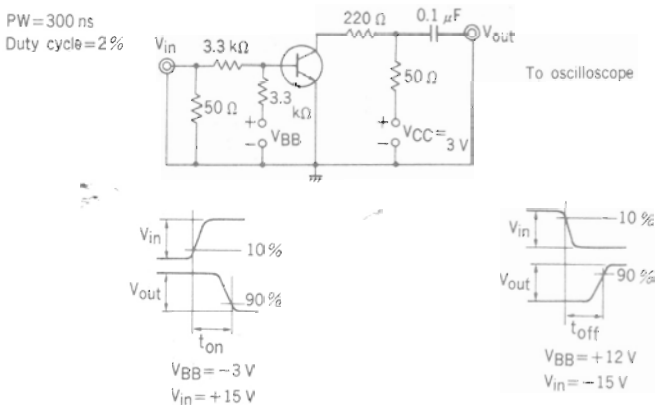
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



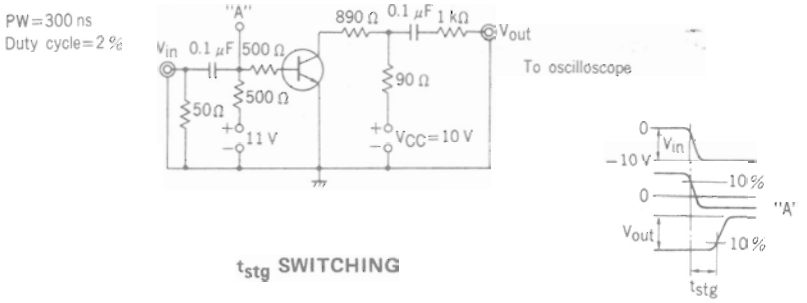
SWITCHING TIME vs. COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT



t_{on}, t_{off} SWITCHING



t_{stg} SWITCHING

Voltage waveforms

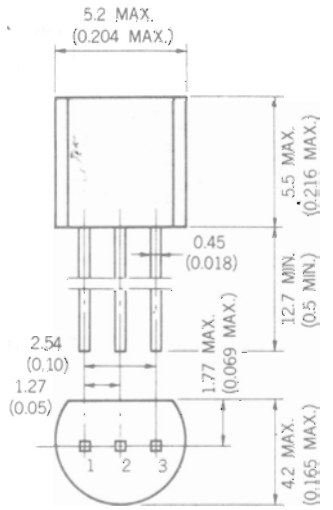
NEC
ELECTRON DEVICE

NPN SILICON TRANSISTOR
NT2369A

DESCRIPTION The NT2369A is designed for general purpose amplifier and high speed switching applications.

FEATURES
- High Frequency Current Gain.
- High Speed Switching.
- NT2369A Electrically Similar to 2N2369A.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature . . . . . −65 to +150 °C

Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Currents (Ta = 25 °C)

V_{CBO}	Collector to Base Voltage	40 V
V_{CES}	Collector to Emitter Voltage	40 V
V_{CEO}	Collector to Emitter Voltage	15 V
V_{EBO}	Emitter to Base Voltage	4.5 V
I_C	Collector Current	200 mA
I_C	Collector Current (10 μs pulse)	500 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{on}	Turn-on Time			12	ns	V_{CC}=3.0 V, I_C=10 mA, I_{B1}=3.0 mA, V_{BE}=−1.5 V
t_{off}	Turn-off Time			18	ns	V_{CC}=3.0 V, I_C=10 mA, I_{B1}=3.0 mA, I_{B2}=−1.5 mA
t_{stg}	Storage Time			13	ns	I_C=10 mA, I_{B1}=−I_{B2}=10 mA
f_T	Gain Bandwidth Product	500	750		MHz	V_{CE}=10 V, I_C=10 mA, f=100 MHz
C_{ob}	Output Capacitance		1.8	4.0	pF	V_{CB}=5.0 V, I_E=0, f=1 MHz
h_{FE1}*	DC Current Gain	40	85	120	—	V_{CE}=0.35 V, I_C=10 mA
h_{FE2}*	DC Current Gain	30	60		—	V_{CE}=0.4 V, I_C=30 mA
h_{FE3}*	DC Current Gain	20	35		—	V_{CE}=1.0 V, I_C=100 mA
h_{FE4}*	DC Current Gain	20			—	V_{CE}=0.35 V, I_C=10 mA, Ta=−55 °C
$V_{CE(sat)1}$*	Collector Saturation Voltage		0.15	0.2	V	I_C=10 mA, I_B=1.0 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		0.20	0.25	V	I_C=30 mA, I_B=3.0 mA
$V_{CE(sat)3}$*	Collector Saturation Voltage		0.35	0.5	V	I_C=100 mA, I_B=10 mA
$V_{CE(sat)4}$*	Collector Saturation Voltage			0.3	V	I_C=10 mA, I_B=1.0 mA, Ta=125 °C

* Pulsed PW ≤ 350 μs, duty cycle ≤ 2 %

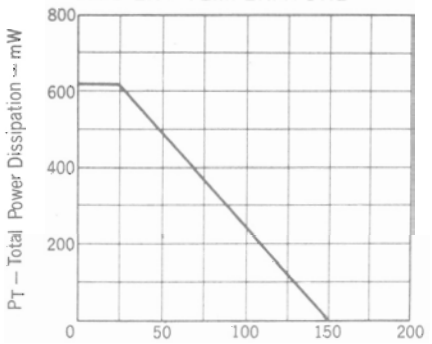
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CES}	Collector Cutoff Current			0.4	μA	V_{CB}=20 V, V_{BE}=0
I_{CBO}	Collector Cutoff Current			30	μA	V_{CB}=20 V, I_E=0, Ta=150 °C
BV_{CBO}	Collector to Base Breakdown Voltage	40			V	I_C=10 μA, I_E=0
BV_{CES}	Collector to Emitter Breakdown Voltage	40			V	I_C=10 μA, V_{BE}=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	15			V	I_C=10 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	4.5			V	I_E=10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage	0.7	0.78	0.85	V	I_C=10 mA, I_B=1.0 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		0.85	1.15	V	I_C=30 mA, I_B=3.0 mA
$V_{BE(sat)3}$*	Base Saturation Voltage		1.05	1.6	V	I_C=100 mA, I_B=10 mA
$V_{BE(sat)4}$*	Base Saturation Voltage	0.59		1.02	V	I_C=10 mA, I_B=1.0 mA, Ta=−55 to +125 °C

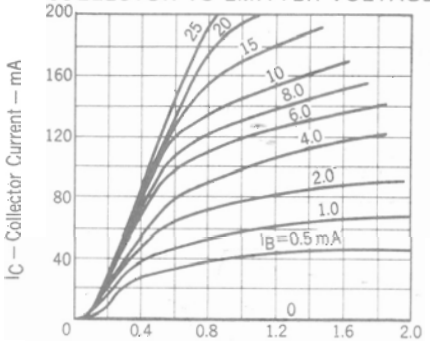
* Pulsed PW ≦350 μs, duty cycle ≦2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

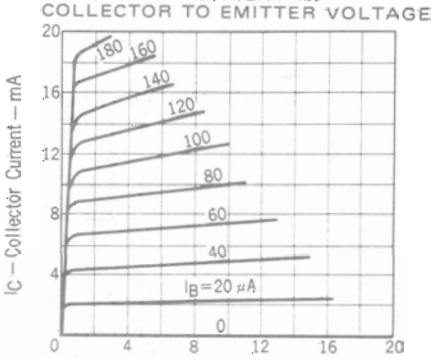
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



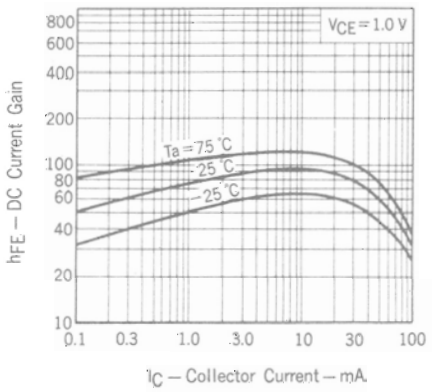
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



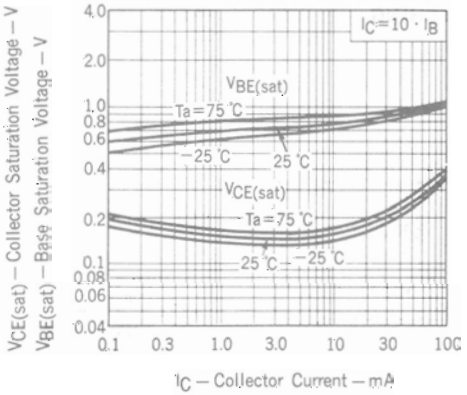
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



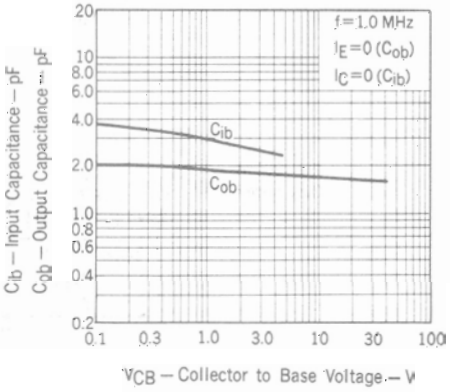
DC CURRENT GAIN vs. COLLECTOR CURRENT



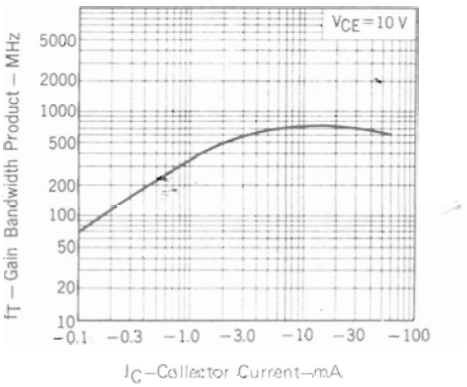
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



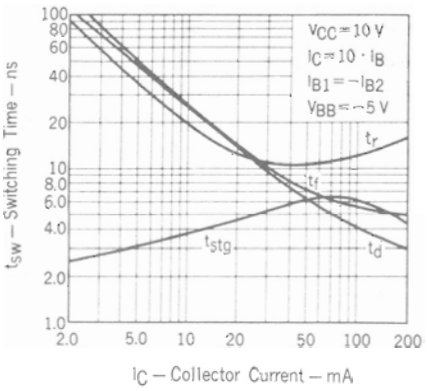
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



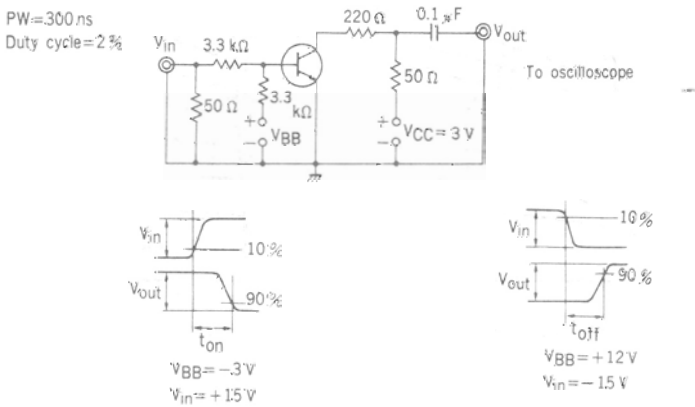
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



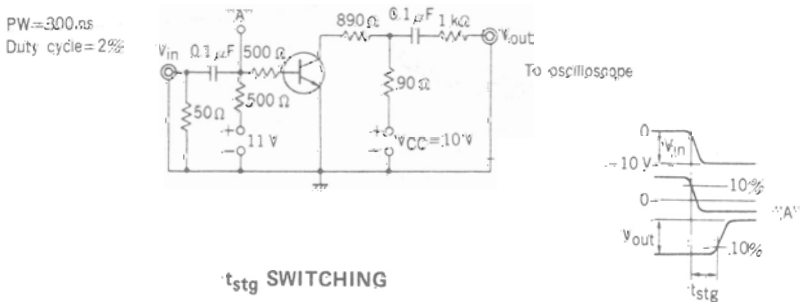
SWITCHING TIME vs. COLLECTOR CURRENT



SWITCHING TIME TEST CIRCUIT



t_{on}, t_{off} SWITCHING



t_{stg} SWITCHING

NEC
ELECTRON DEVICE

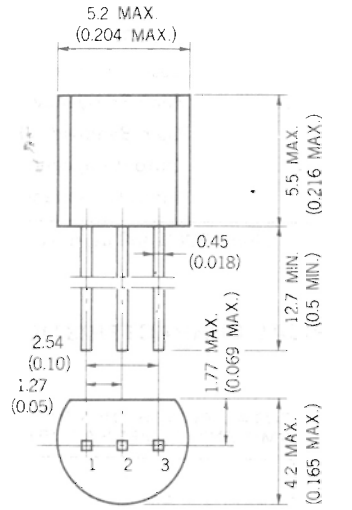
PNP SILICON TRANSISTOR
NT2907

DESCRIPTION The NT2907 is designed for general purpose amplifier and high speed, medium-power switching applications.

FEATURES

- High Frequency Current Gain.
- Low Collector Saturation Voltage.
- High Speed Switching.
- For Complementary Use with NPN Type NT2222.
- NT2907 Electrically Similar to 2N2907.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta = 25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −40 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −600 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			10	ns	V_{CC} = −30 V, I_C = −150 mA
t_r	Rise Time			40	ns	V_{BE} = 0, I_{B1} = −15 mA
t_{on}	Turn-On Time			45	ns	
t_{stg}	Storage Time			80	ns	V_{CC} = −6 V, I_C = −150 mA
t_f	Fall Time			30	ns	I_{B1} = −I_{B2} = −15 mA
t_{off}	Turn-Off Time			100	ns	
h_{FE1}	DC Current Gain	35	130		—	V_{CE} = −10 V, I_C = −100 μA
h_{FE2}	DC Current Gain	50	150		—	V_{CE} = −10 V, I_C = −1 mA
h_{FE3}	DC Current Gain	75	170		—	V_{CE} = −10 V, I_C = −10 mA
h_{FE4}*	DC Current Gain	100	150	300	—	V_{CE} = −10 V, I_C = −150 mA
h_{FE5}*	DC Current Gain	30	120		—	V_{CE} = −10 V, I_C = −500 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		−0.2	−0.4	V	I_C = −150 mA, I_B = −15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		−0.5	−1.6	V	I_C = −500 mA, I_B = −50 mA

* Pulsed PW ≤ 300 μs, duty cycle ≤ 2 %

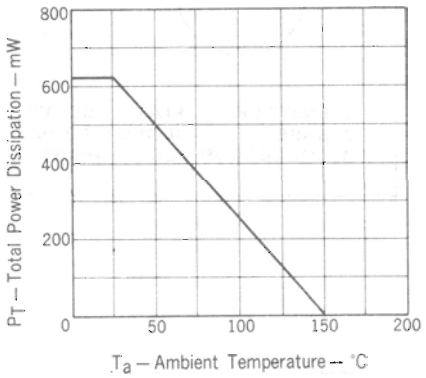
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			−50	nA	V_{CE}=−30 V, V_{BE}=0.5 V
I_{CBO1}	Collector Cutoff Current			−20	nA	V_{CB}=−50 V, I_E=0
I_{CBO2}	Collector Cutoff Current			−20	μA	V_{CB}=−50 V, I_E=0, Ta=150 °C
I_{BEX}	Base Cutoff Current			50	nA	V_{CE}=−30 V, V_{BE}=0.5 V
BV_{CBO}	Collector to Base Breakdown Voltage	−60			V	I_C=−10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−40			V	I_C=−10 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage		−0.9	−1.3	V	I_C=−150 mA, I_B=−15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		−1.1	−2.6	V	I_C=−500 mA, I_B=−50 mA
$\|h_{fe}\|$	High Frequency Current Gain	2	4		−	V_{CE}=−20 V, I_C=−50 mA, f=100 MHz
f_T	Gain Bandwidth Product	200	400		MHz	V_{CE}=−20 V, I_C=−50 mA, f=100 MHz
C_{ob}	Output Capacitance		5.0	8.0	pF	V_{CB}=−10 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		18	30	pF	V_{EB}=−2 V, I_C=0, f=1 MHz

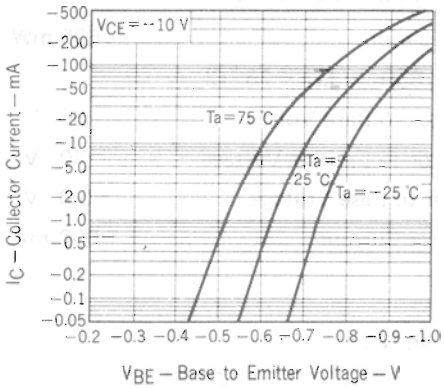
* Pulsed PW ≦ 300 μs, duty cycle ≦ 2 %

TYPICAL CHARACTERISTICS (Ta=25 °C)

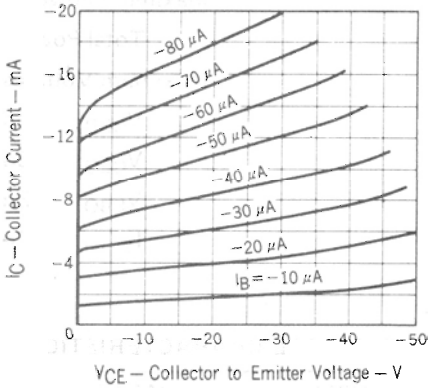
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



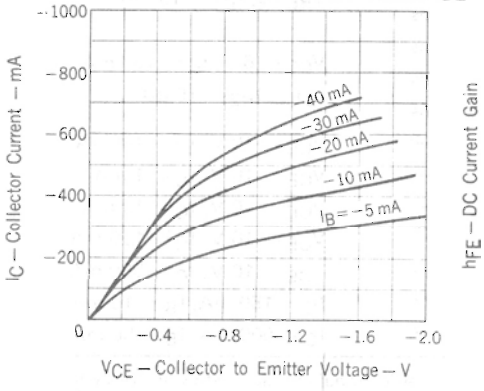
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



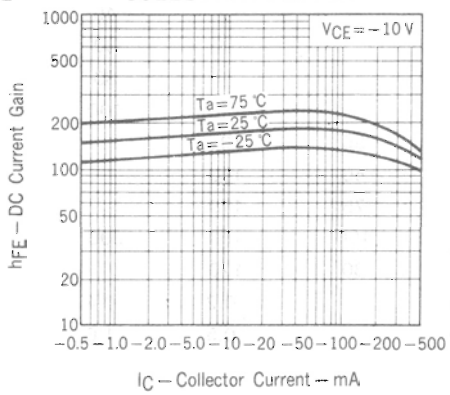
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



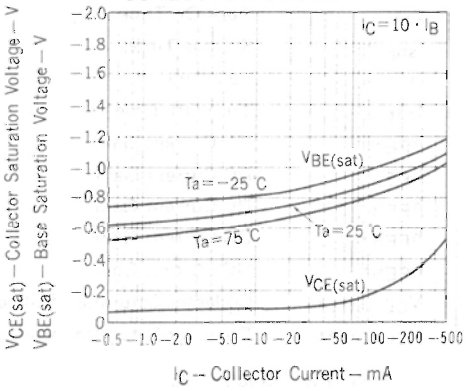
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



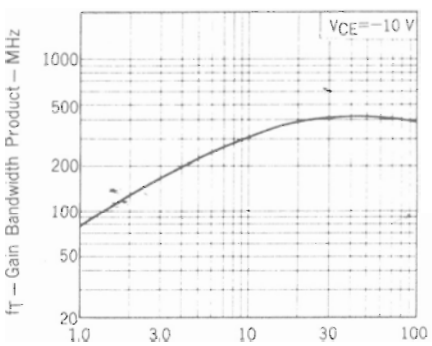
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT

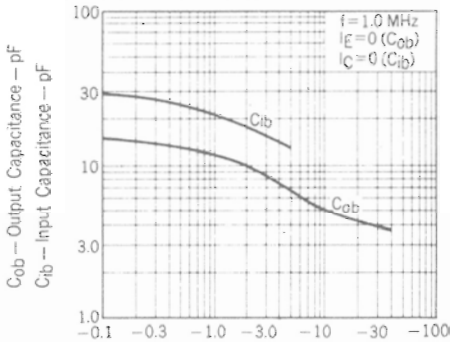


GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



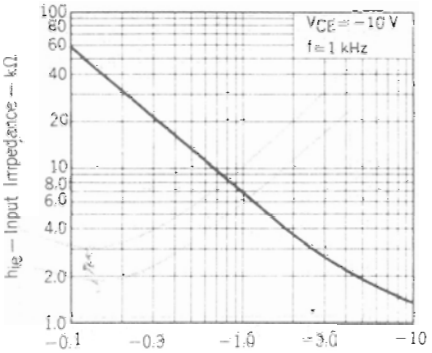
I_C – Collector Current – mA

INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



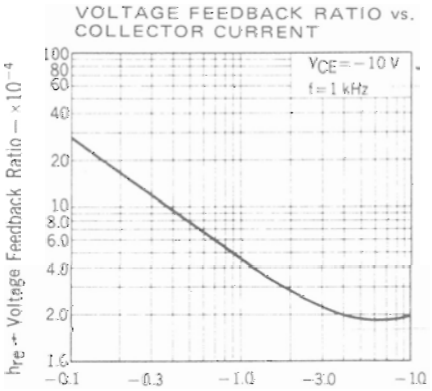
V_{CB} – Collector to Base Voltage – V
V_{EB} – Emitter to Base Voltage – V

INPUT IMPEDANCE vs. COLLECTOR CURRENT



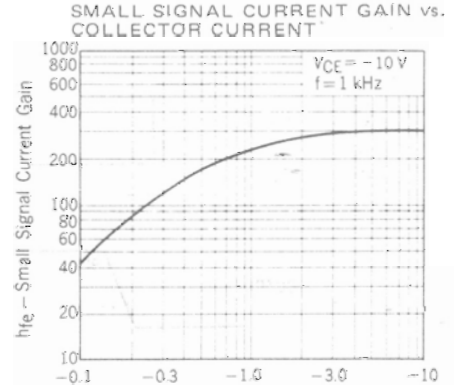
I_C – Collector Current – mA

VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



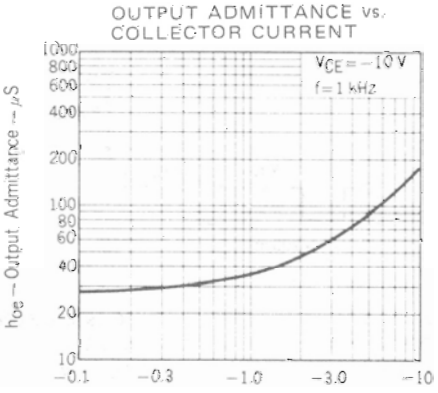
I_C – Collector Current – mA

SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



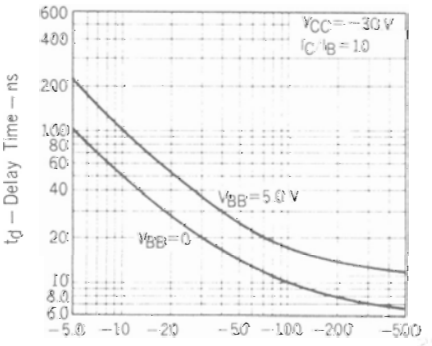
I_C – Collector Current – mA

OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



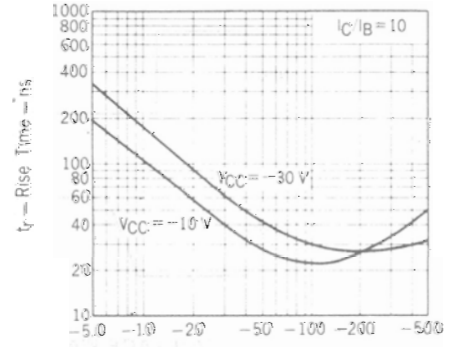
I_C – Collector Current – mA

DELAY TIME vs. COLLECTOR CURRENT



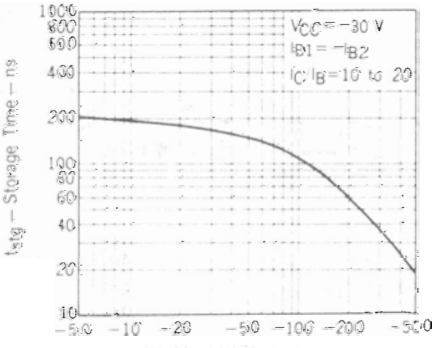
I_C – Collector Current – mA

RISE TIME vs. COLLECTOR CURRENT

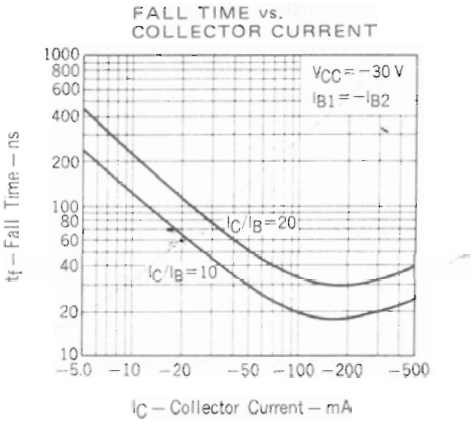


I_C – Collector Current – mA

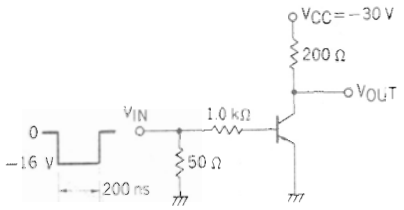
STORAGE TIME vs. COLLECTOR CURRENT



I_C – Collector Current – mA



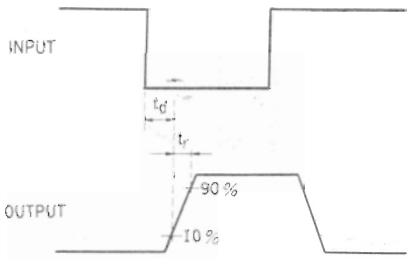
SWITCHING TIME TEST CIRCUIT



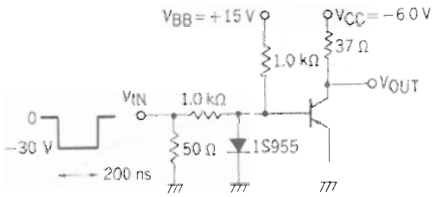
Z_O = 50 Ω
PRF = 150 pps
t_r ≤ 2.0 ns

TO OSCILLOSCOPE
t_r ≤ 5.0 ns
Z_{IN} = 10 MΩ

t_{on} SWITCHING



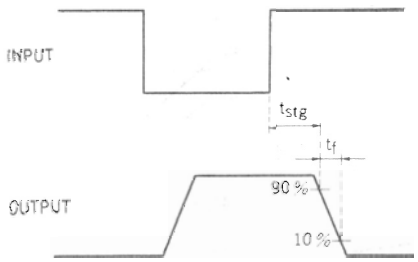
VOLTAGE WAVEFORMS



Z_O = 50 Ω
PRF = 150 pps
t_r ≤ 2.0 ns

TO OSCILLOSCOPE
t_r ≤ 5.0 ns
Z_{IN} = 10 MΩ

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

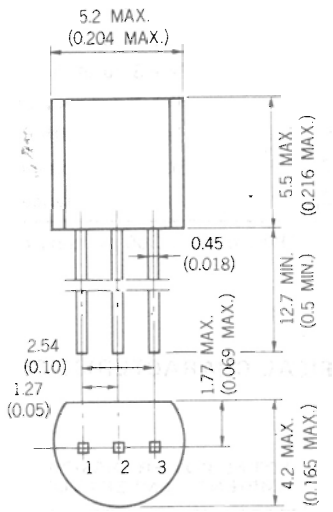
PNP SILICON TRANSISTOR
NT2907A

DESCRIPTION The NT2907A is designed for general purpose amplifier and high speed, medium power switching applications.

FEATURES

- High Frequency Current Gain.
- Low Collector Saturation Voltage.
- High Speed Switching.
- For Complementary Use with NPN Type NT2222A.
- NT2907A Electrically Similar to 2N2907A.

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. BASE
3. COLLECTOR

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta=25 °C)

- Total Power Dissipation . . . . . 625 mW

Maximum Voltages and Current (Ta=25 °C)

- V_{CBO} Collector to Base Voltage . . . . . −60 V
- V_{CEO} Collector to Emitter Voltage . . . . . −60 V
- V_{EBO} Emitter to Base Voltage . . . . . −5.0 V
- I_C Collector Current . . . . . −600 mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_d	Delay Time			10	ns	V_{CC}=−30 V, I_C=−150 mA
t_r	Rise Time			40	ns	V_{BE}=0, I_{B1}=−15 mA
t_{on}	Turn-On Time			45	ns	
t_{stg}	Storage Time			80	ns	V_{CC}=−6 V, I_C=−150 mA
t_f	Fall Time			30	ns	I_{B1}=−I_{B2}=−15 mA
t_{off}	Turn-Off Time			100	ns	
h_{FE1}	DC Current Gain	75	130		—	V_{CE}=−10 V, I_C=−100 μA
h_{FE2}	DC Current Gain	100	150		—	V_{CE}=−10 V, I_C=−1 mA
h_{FE3}	DC Current Gain	100	170		—	V_{CE}=−10 V, I_C=−10 mA
h_{FE4}*	DC Current Gain	100	150	300	—	V_{CE}=−10 V, I_C=−150 mA
h_{FE5}*	DC Current Gain	50	120		—	V_{CE}=−10 V, I_C=−500 mA
$V_{CE(sat)1}$*	Collector Saturation Voltage		−0.2	−0.4	V	I_C=−150 mA, I_B=−15 mA
$V_{CE(sat)2}$*	Collector Saturation Voltage		−0.5	−1.6	V	I_C=−500 mA, I_B=−50 mA

* Pulsed PW ≤300 μs, duty cycle ≤2.0 %

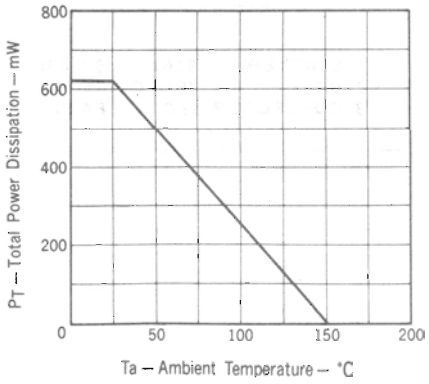
Additional characteristics on following page.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{CEX}	Collector Cutoff Current			−50	nA	V_{CE}=−30 V, V_{BE}=0.5 V
I_{CBO1}	Collector Cutoff Current			−10	nA	V_{CB}=−50 V, I_E=0
I_{CBO2}	Collector Cutoff Current			−10	μA	V_{CB}=−50 V, I_E=0, Ta=150 °C
I_{BEX}	Base Cutoff Current			50	nA	V_{CE}=−30 V, V_{BE}=0.5 V
BV_{CBO}	Collector to Base Breakdown Voltage	−60			V	I_C=−10 μA, I_E=0
BV_{CEO}*	Collector to Emitter Breakdown Voltage	−60			V	I_C=−10 mA, I_B=0
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0			V	I_E=−10 μA, I_C=0
$V_{BE(sat)1}$*	Base Saturation Voltage		−0.9	−1.3	V	I_C=−150 mA, I_B=−15 mA
$V_{BE(sat)2}$*	Base Saturation Voltage		−1.1	−2.6	V	I_C=−500 mA, I_B=−50 mA
$\|h_{fe}\|$	High Frequency Current Gain	2	4		—	V_{CE}=−20 V, I_C=−50 mA, f=100 MHz
f_T	Gain Bandwidth Product	200	400		MHz	V_{CE}=−20 V, I_C=−50 mA, f=100 MHz
C_{ob}	Output Capacitance		5.0	8.0	pF	V_{CB}=−10 V, I_E=0, f=1 MHz
C_{ib}	Input Capacitance		18	30	pF	V_{EB}=−2 V, I_C=0, f=1 MHz

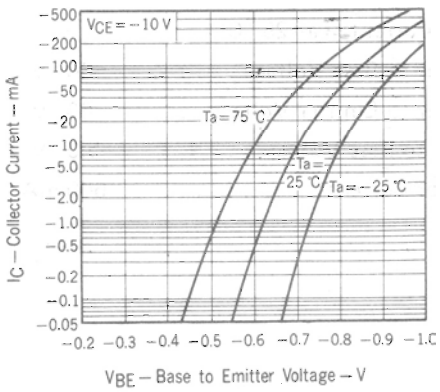
* Pulsed PW ≤300 μs, duty cycle ≤2%

TYPICAL CHARACTERISTICS (Ta=25 °C)

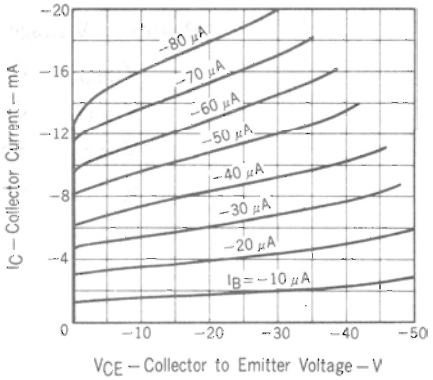
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



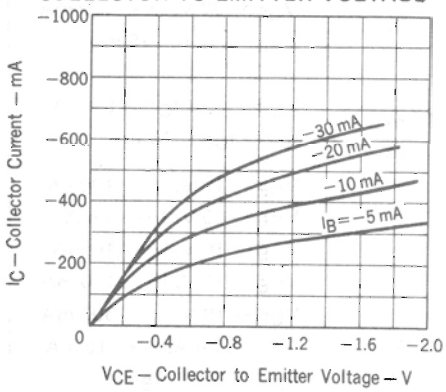
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



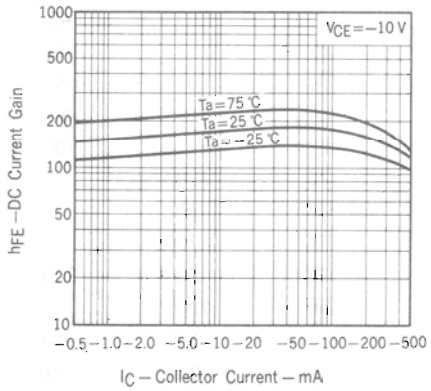
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



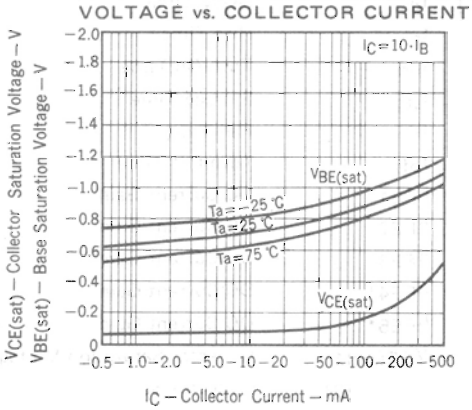
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



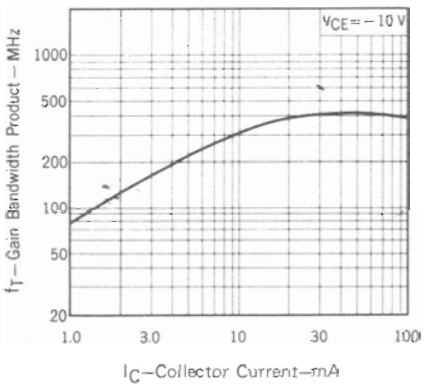
DC CURRENT GAIN vs. COLLECTOR CURRENT



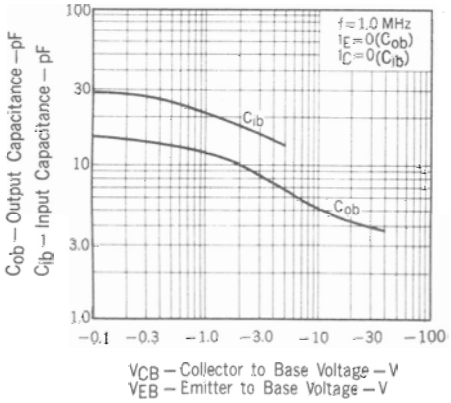
BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



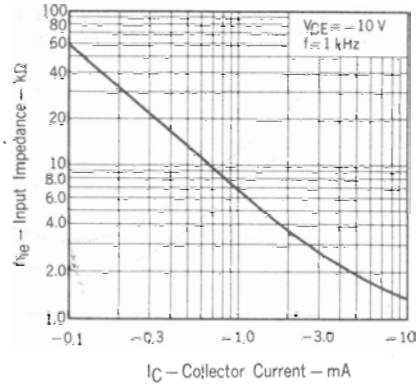
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



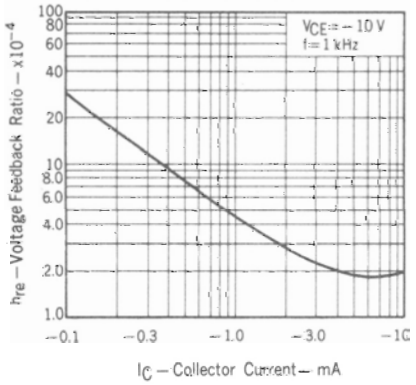
INPUT AND OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



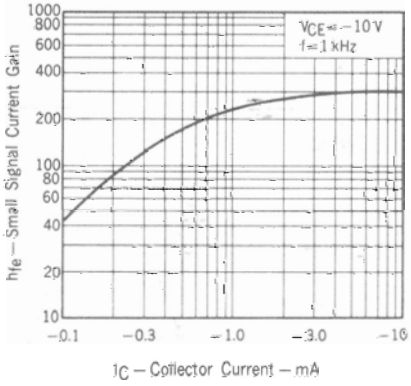
INPUT IMPEDANCE vs. COLLECTOR CURRENT



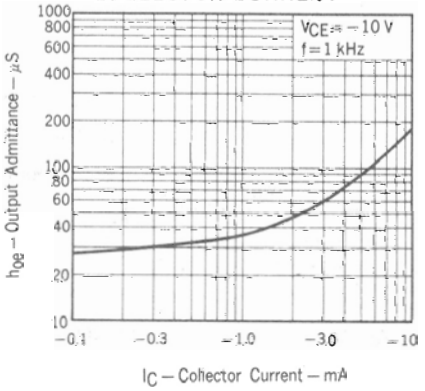
VOLTAGE FEEDBACK RATIO vs. COLLECTOR CURRENT



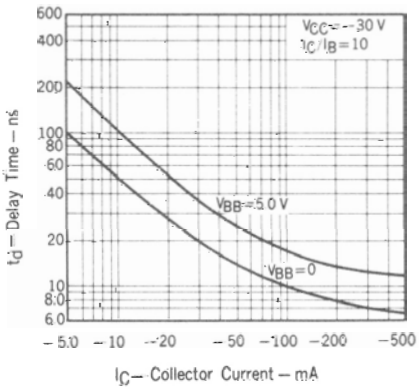
SMALL SIGNAL CURRENT GAIN vs. COLLECTOR CURRENT



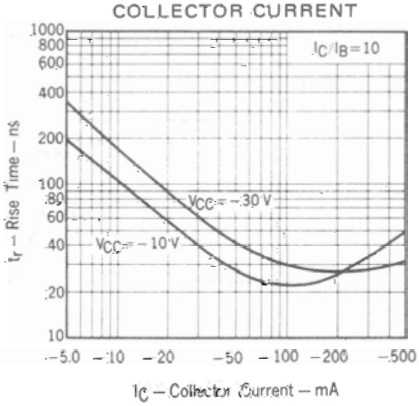
OUTPUT ADMITTANCE vs. COLLECTOR CURRENT



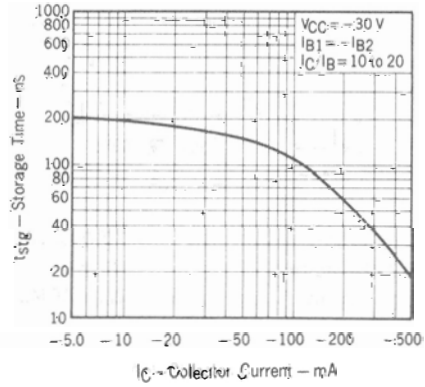
DELAY TIME vs. COLLECTOR CURRENT

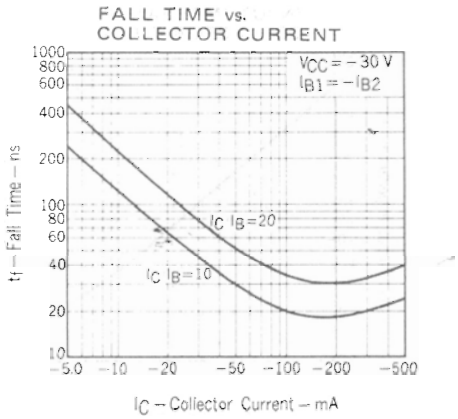


RISE TIME vs. COLLECTOR CURRENT

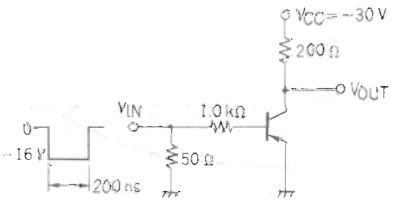


STORAGE TIME vs. COLLECTOR CURRENT





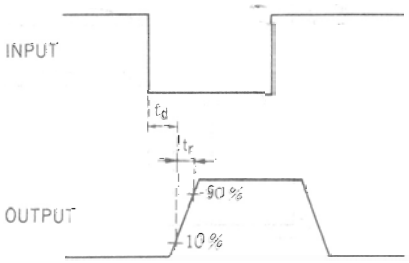
SWITCHING TIME TEST CIRCUIT



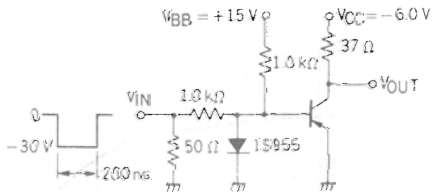
Z_O = 50 Ω
PRF = 150 pps
t_r ≤ 2.0 ns

TO OSCILLOSCOPE
t_r ≤ 5.0 ns
Z_{IN} = 10 MΩ

t_{on} SWITCHING



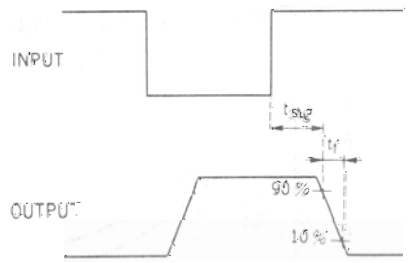
VOLTAGE WAVEFORMS



Z_O = 50 Ω
PRF = 150 pps
t_r ≤ 2.0 ns

TO OSCILLOSCOPE
t_r ≤ 5.0 ns
Z_{IN} = 10 MΩ

t_{off} SWITCHING



VOLTAGE WAVEFORMS

NEC
ELECTRON DEVICE

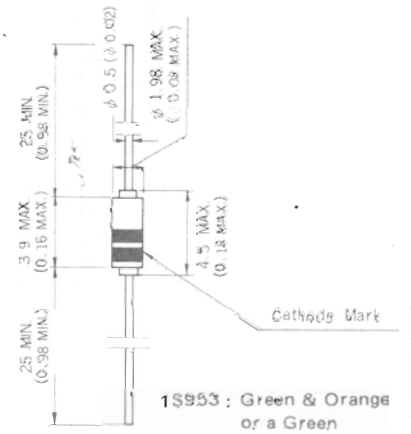
SILICON SWITCHING DIODES
1S953,1S954,1S955

DESCRIPTION The 1S953, 1S954 and 1S955 are silicon epitaxial planar diodes designed for high speed switching applications.

FEATURES

- Miniature Package.
- High Power Dissipation.
- Low Capacitance.
- Fast Recovery Time.
- Low Leakage.
- High Conductance.

PACKAGE DIMENSIONS
in millimeters (inches)



1S953 : Green & Orange or a Green
1S954 : Green & Yellow
1S955 : Green & Green

EIAJ : SC-40
JEDEC : DO-35

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	200	°C
Storage Temperature	T_{stg}	−65 to +200	°C

Maximum Power Dissipation (Ta=25 °C)

Power Dissipation	P_T	500	mW

Maximum Voltages and Currents (Ta=25 °C)

		1S953	1S954	1S955	
Peak Reverse Voltage	V_{RM}	35	75	100	V
Reverse Volstage	V_R	30	50	75	V
Peak Forward Surge Current (1 μs)	$I_{F(surge)}$	2 000	4 000	4 000	mA
Peak Forward Current	I_{FM}	300	600	600	mA
Average Rectified Current	I_O	100	200	200	mA

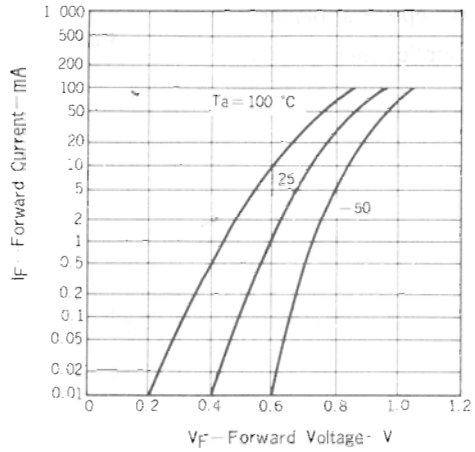
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	1S953 MIN.	1S953 TYP.	1S953 MAX.	1S954 MIN.	1S954 TYP.	1S954 MAX.	1S955 MIN.	1S955 TYP.	1S955 MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.8	1.0							V	I_F=30 mA
V_F	Forward Voltage					0.9	1.0				V	I_F=100 mA
V_F	Forward Voltage								0.9	1.0	V	I_F=150 mA
I_R	Reverse Current		0.01	0.1							μA	V_R=30 V
I_R	Reverse Current					0.015	0.1				μA	V_R=50 V
I_R	Reverse Current								0.03	0.1	μA	V_R=75 V
C_t	Terminal Capacitance		2.0	4.0		2.0	3.5		2.0	3.0	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time		2.0	3.0		2.0	3.0		2.0	3.0	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

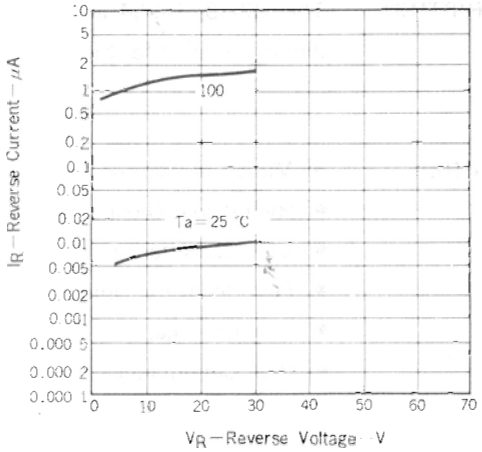
TYPICAL CHARACTERISTICS (Ta = 25 °C)

1S953

FORWARD CURRENT vs. FORWARD VOLTAGE

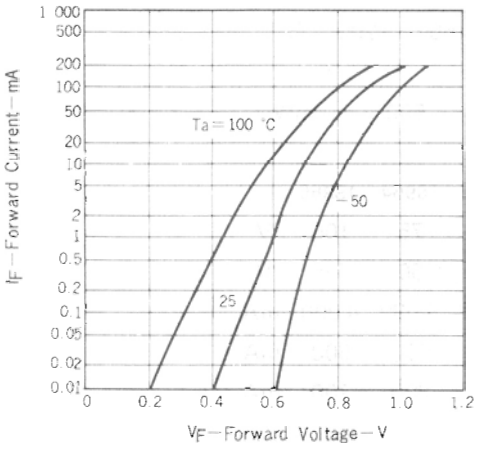


REVERSE CURRENT vs. REVERSE VOLTAGE

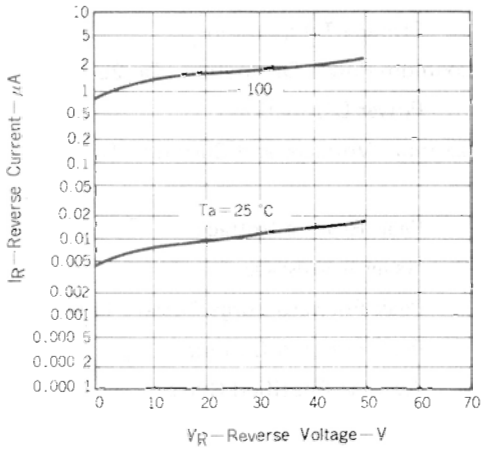


1S954

FORWARD CURRENT vs. FORWARD VOLTAGE

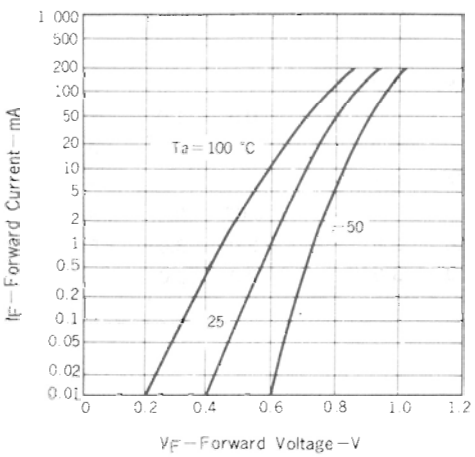


REVERSE CURRENT vs. REVERSE VOLTAGE

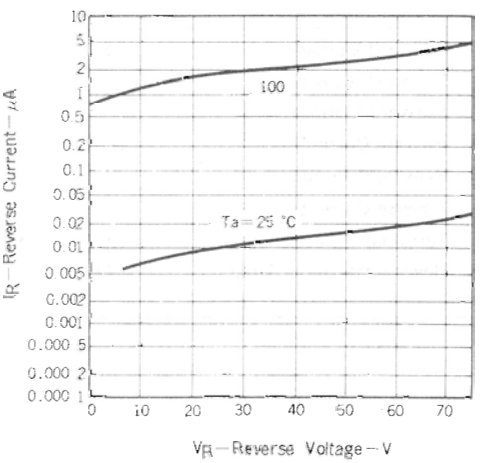


1S955

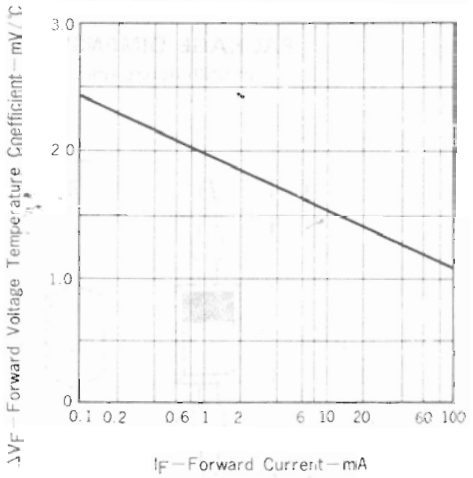
FORWARD CURRENT vs. FORWARD VOLTAGE



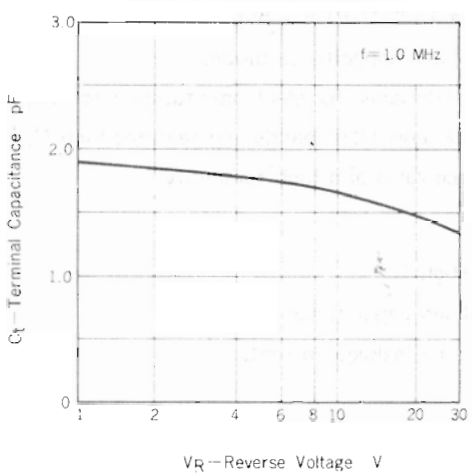
REVERSE CURRENT vs. REVERSE VOLTAGE



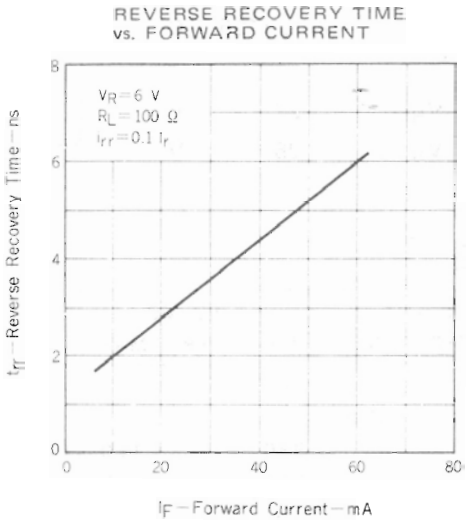
FORWARD VOLTAGE TEMPERATURE COEFFICIENT vs. FORWARD CURRENT



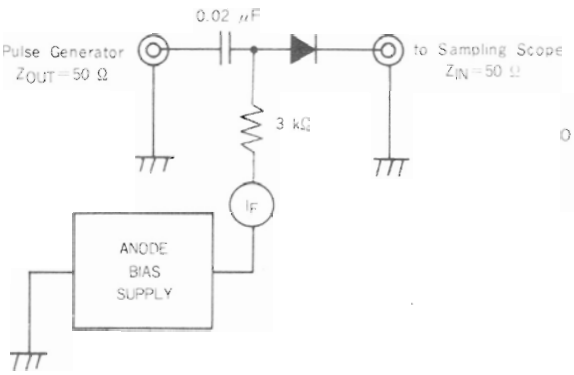
TERMINAL CAPACITANCE vs. REVERSE VOLTABE

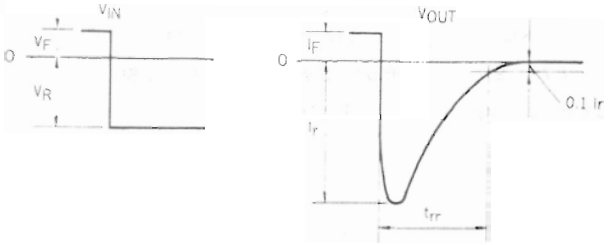


REVERSE RECOVERY TIME vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT





Test Conditions : I_F=10 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

VARACTOR DIODE
1S2207(B)

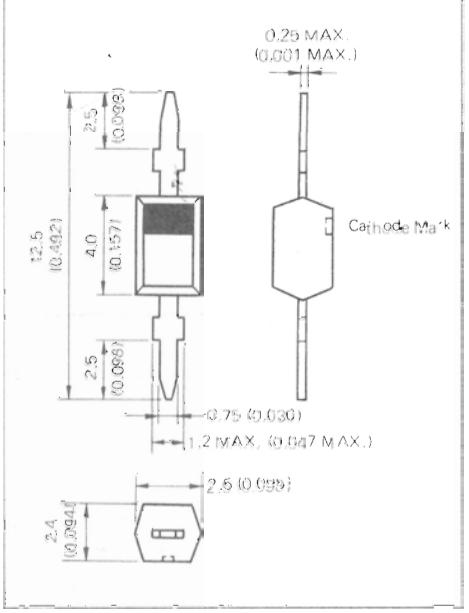
DESCRIPTION

The 1S2207(B) is a hyper-abrupt junction type voltage-variable capacitance diode.
It is designed for electronic tuning circuit applications in VHF and UHF bands and features high Q, high capacitance ratio and high reliability.

FEATURES

- High Q.
- High capacitance ratio.
- Low leakage current.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Maximum Voltages (Ta=25 °C)			
Peak Reverse Voltage	V_{RM}	27	V
DC Reverse Voltage	V_R	25	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	NC MIN.	NC TYP.	NC MAX.	KC, LC, MC MIN.	KC, LC, MC TYP.	KC, LC, MC MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	25			25			V	I_R = 1.0 μA
C_{t2}	Terminal Capacitance	11.0		17.0				pF	V_R = 2.0 V, f = 1.0 MHz
C_{t3}					9.50		14.0		V_R = 3.0 V, f = 1.0 MHz
C_{t6}					5.75		9.75		V_R = 6.0 V, f = 1.0 MHz
C_{t10}		3.8		6.4	3.80		6.40		V_R = 10 V, f = 1.0 MHz
N1	Capacitance Ratio	2.5		3.10					C_{t2}/C_{t10}
N2					2.20		2.60		C_{t3}/C_{t10}
r_s	Seriese Resistance			0.6			0.6	Ω	C_t = 9.0 pF, f = 50 MHz

C_{t6} Classification

Rank	KC	LC	MC
C_{t6}(pF)	7.75 – 9.75	6.50 – 8.75	5.75 – 7.50

C_{t6} Test Condition: V_R = 6.0 V, f = 1.0 MHz

TYPICAL CHARACTERISTICS (Ta = 25 °C)

TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

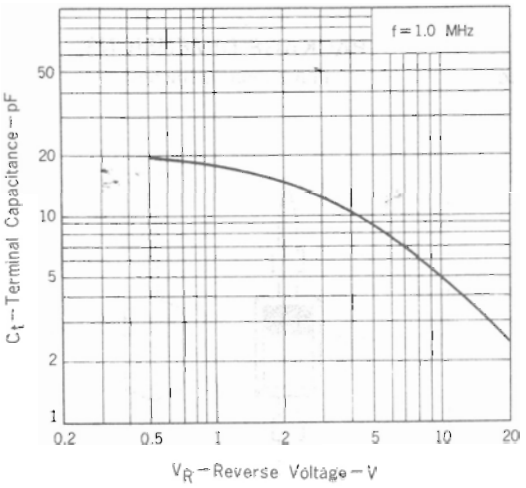
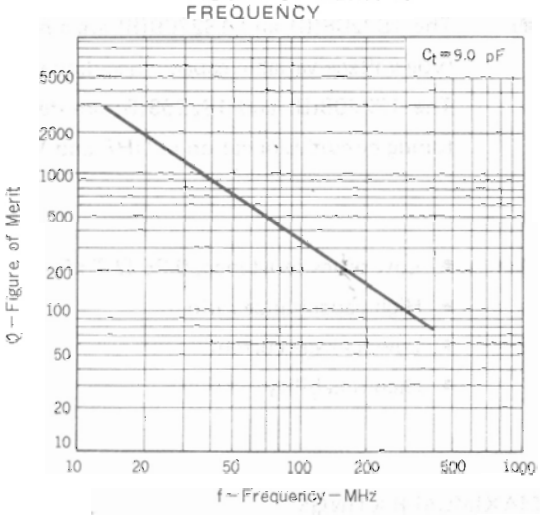
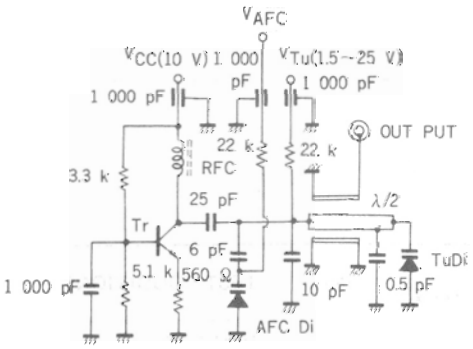


FIGURE OF MERIT vs. FREQUENCY

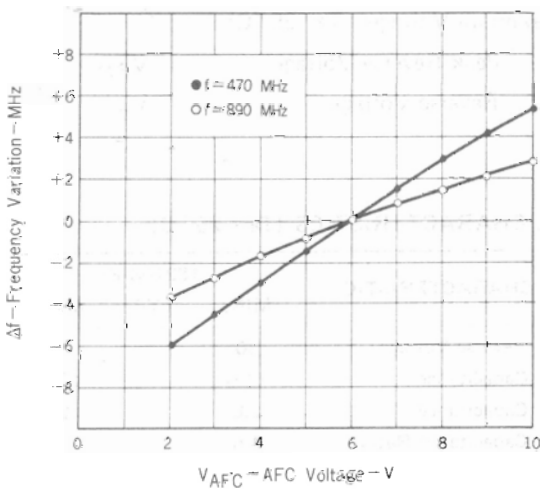


AFC Test Circuit



Tr : 2SC288A(5·B) (or 2SC1730)
Tuning Diode : 1S2208(B)

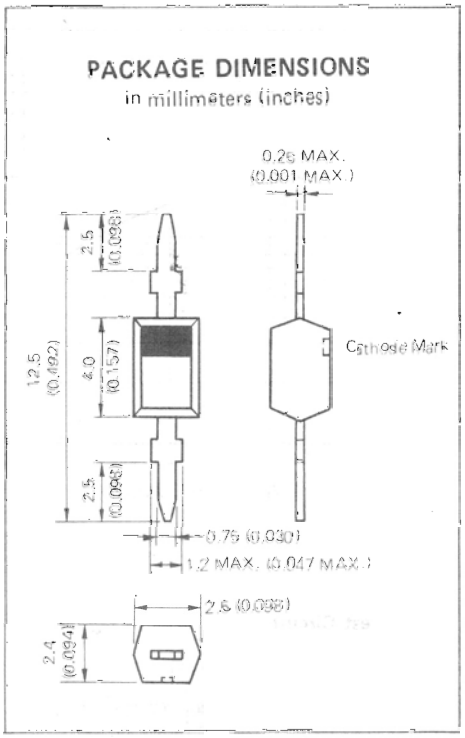
FREQUENCY VARIATION vs. AFC VOLTAGE



NEC
ELECTRON DEVICE

SILICON VARACTOR DIODES
1S2208(B),1S2209(B)

DESCRIPTION The 1S2208(B) and 1S2209(B) are a hyper-abrupt junction type voltage-variable capacitance diodes.
The 1S2208(B) and 1S2209(B) are designed for electronic tuning circuit application in UHF and VHF.



FEATURES

- Low series resistance. 0.35 Ω TYP.
- High capacitance ratio.
- Low leakage current.
- High reliability.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Maximum Voltages (Ta=25 °C)			
Peak Reverse Voltage	V_{RM}	30	V
Reverse Voltage	V_R	30	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	1S2208(B) MIN.	1S2208(B) TYP.	1S2208(B) MAX.	1S2209(B) MIN.	1S2209(B) TYP.	1S2209(B) MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	30			30			V	I_R=1.0 μA
C_{t3}	Capacitance	11.0		12.65	10.3		12.90	pF	V_R=3.0 V, f=1.0 MHz
C_{t25}	Capacitance	2.0		2.3	2.0		2.5	pF	V_R=25 V, f=1.0 MHz
N	Capacitance Ratio	4.5			4.0				C_{t3}/C_{t25}
r_s	Series Resistance		0.35	0.6		0.35	0.6	Ω	C=9.0 pF, f=50 MHz

NOTE: Diodes are available in matched sets of 20, 60, 120, 120 x n units.
For two diodes of one set the following conditions are relevant:
The variations ΔC in capacitance values at V_R=3, 10, 18 and 25 V are less than 2 % for 1S2208(B), 3 % for 1S2209(B).

$$\Delta C = \frac{C_{max.} - C_{min.}}{C_{min.}} \times 100\ (\%)$$

TYPICAL CHARACTERISTICS (Ta = 25 °C)

TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

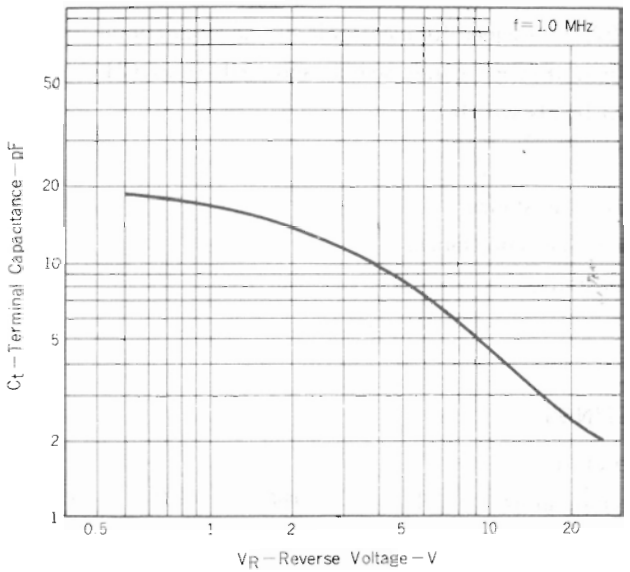
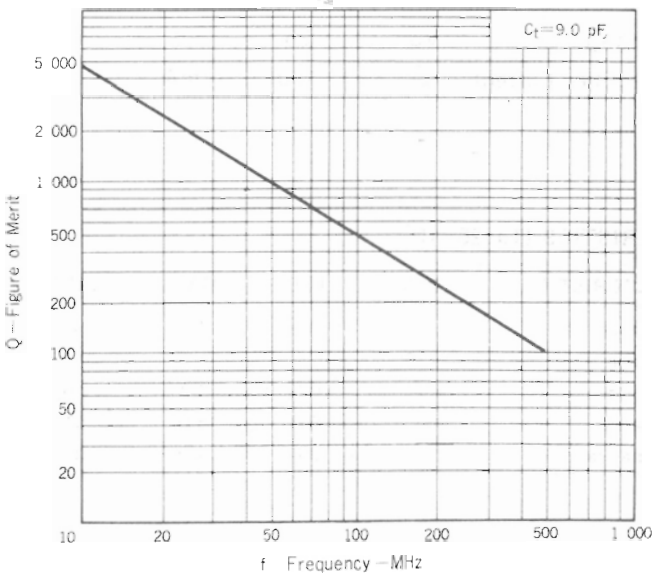


FIGURE OF MERIT vs. FREQUENCY



NEC
ELECTRON DEVICE

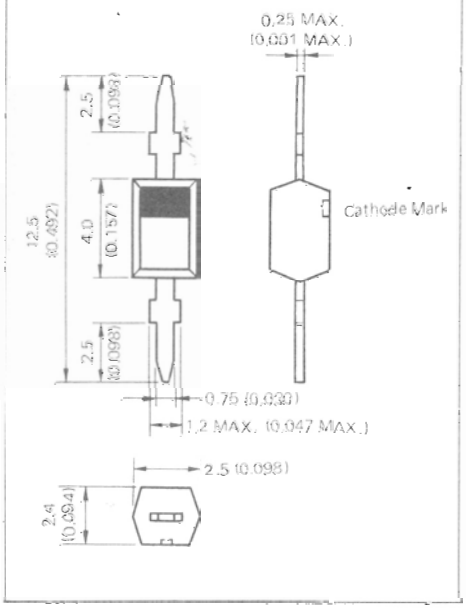
SILICON SWITCHING DIODE
1S2222

DESCRIPTION The 1S2222 is designed for electronic tuning circuit applications in UHF/VHF bands switch and VHF (Low CH., High CH.) bands switch.

FEATURES

- Low series resistance.
- Low terminal capacitance.
- High reliability.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	250	mW
Maximum Voltage and Current (Ta=25 °C)			
Reverse Voltage	V_R	35	V
Average Rectified Current	I_o	100	mA

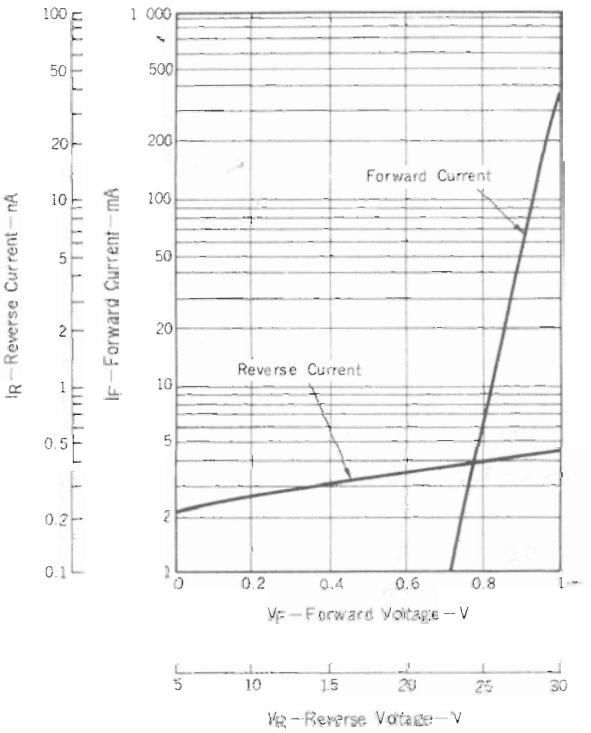
ELECTRICAL CHARACTERISTICS (Ta=25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage			1.1	V	I_F=100 mA
V_R	Reverse Voltage	35			V	I_R=1.0 μA
I_R	Reverse Current		0.5	50	nA	V_R=30 V
r_s	Series Resistance		0.6	1.0	Ω	I_F=10 mA, f=100 MHz
C_t	Terminal Capacitance		0.8	1.0	pF	V_R=15 V, f=1.0 MHz

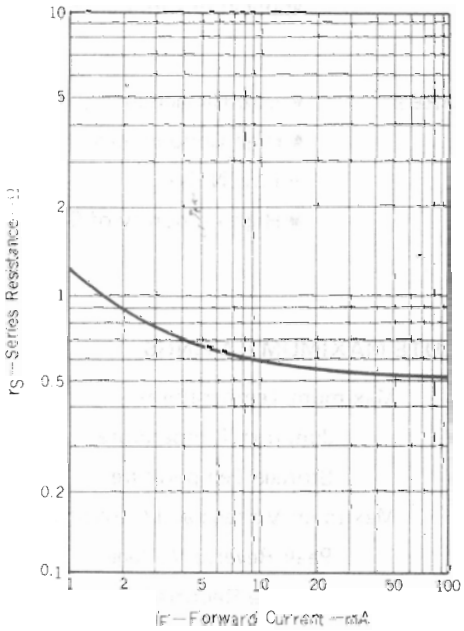
TYPICAL CHARACTERISTICS (Ta=25 °C)

FORWARD CURRENT vs.
FORWARD VOLTAGE

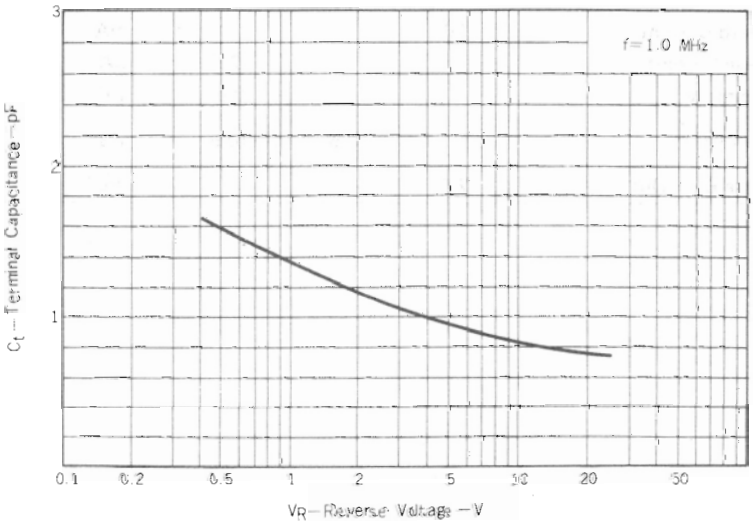
REVERSE CURRENT vs.
REVERSE VOLTAGE



SERIES RESISTANCE vs.
FORWARD CURRENT



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

SILICON UHF DETECTOR & MIXER DIODE

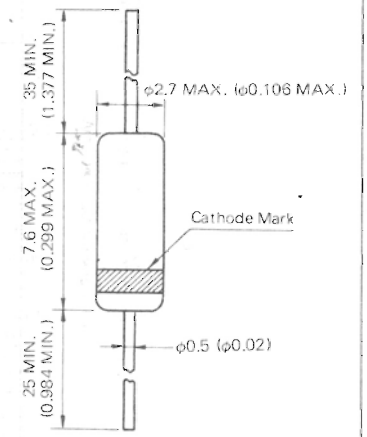
1SS16

DESCRIPTION The 1SS16 is designed for UHF detector and Mixer Diode circuit applications in TV Tuner.

FEATURES

- Low Capacitance.
- High Conductance.
- Low Noise.
- High Immunity of Surge Current.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

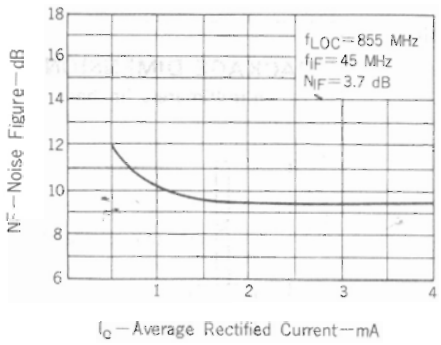
Maximum Temperatures			
Junction Temperature	T_j	100	°C
Storage Temperature	T_{stg}	−65 to +100	°C
Maximum Voltage and Current (Ta=25 °C)			
Peak Reverse Voltage	V_{RM}	5.0	V
Average Rectified Current	I_O	30	mA

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

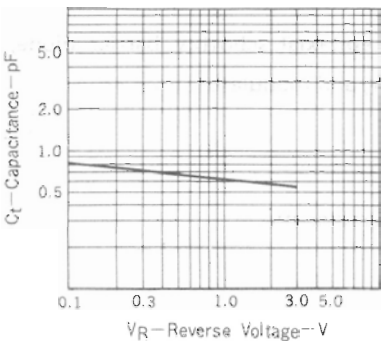
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_F	Forward Current	30			mA	V_F=0.5 V
I_R	Reverse Current			25	μA	V_R=0.5 V
C_t	Capacitance			0.9	pF	V_R=0.2 V, f=1.0 MHz
NF	Noise Figure		9.5	10.5	dB	f_{LOC}=855 MHz, f_{IF}=45 MHz, N_{IF}=3.7 dB, I_O=2.0 mA
B_O	Reverse Burn Out	2.0			erg	

TYPICAL CHARACTERISTICS (Ta=25 °C)

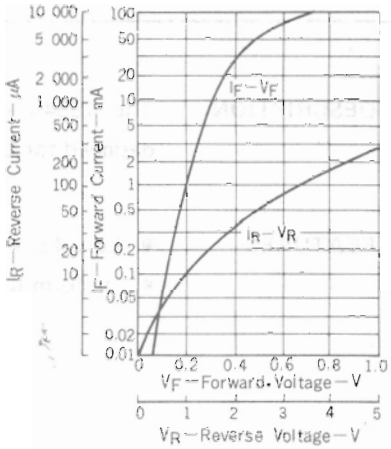
NF vs. I_O



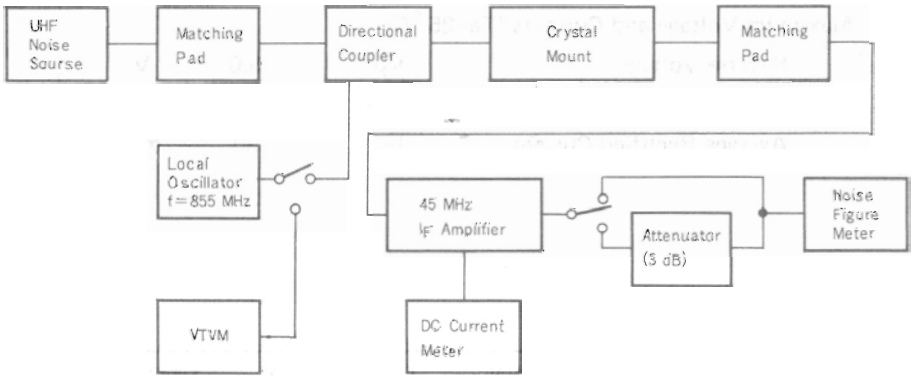
C_t vs. V_R



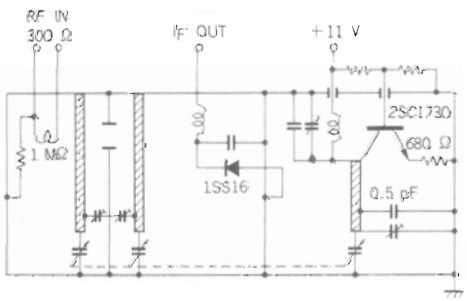
I_R vs. V_R
I_F vs. V_F

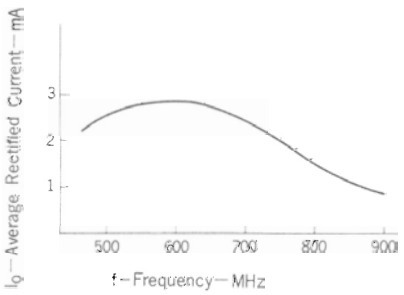


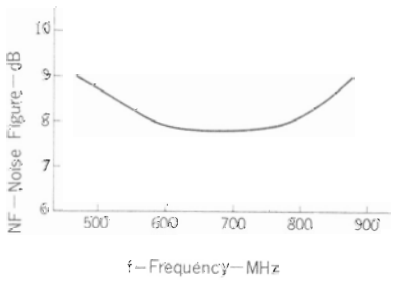
NF TEST CIRCUIT



TYPICAL APPLICATION for UHF TV TUNER







NEC
ELECTRON DEVICE

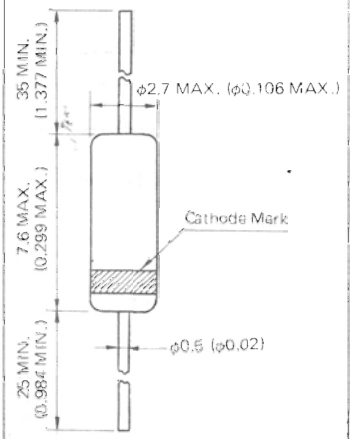
SILICON UHF MIXER DIODE
1SS43

DESCRIPTION The 1SS43 is silicon epitaxial schottky barrier diode, especially designed for UHF mixer, and modulator.

FEATURES

- Low distortion.
- Uniform forward characteristic.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code
Yellow, Orange

ABSOLUTE MAXIMUM RATINGS

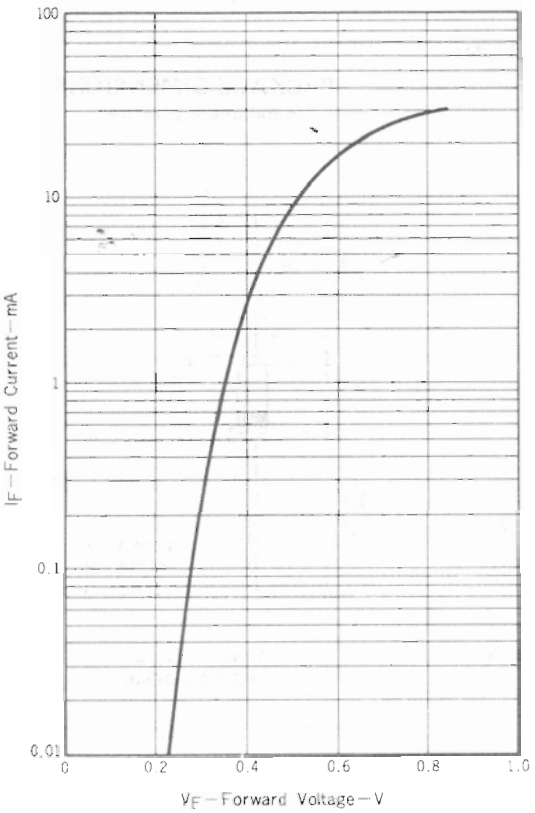
Maximum Temperatures			
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Maximum Voltage and Currents (Ta=25 °C)			
Reverse Voltage	V_R	5.0	V
Peak Forward Current (1 μs)	I_{FM}	90	mA
Average Rectified Current	I_O	30	mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

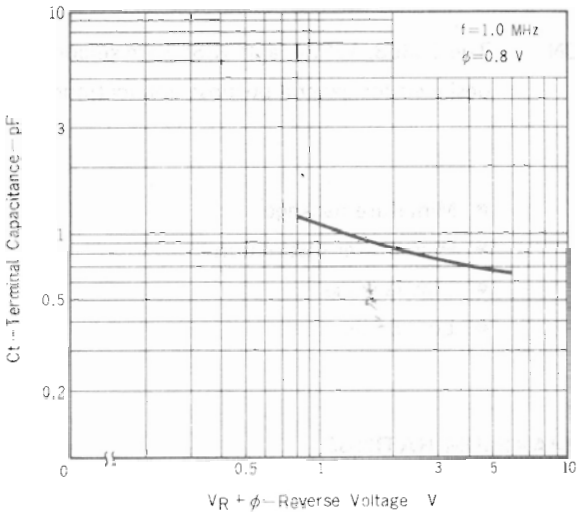
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage	460		550	mV	I_F=10 mA
I_R	Reverse Current			1.0	μA	V_R=5.0 V
C_t	Terminal Capacitance	0.55		0.75	pF	V_R=5.0 V, f=1.0 MHz
ΔV_F	Delta Forward Voltage			10	mV	I_F=10 mA (Batch Matched)

TYPICAL CHARACTERISTICS (Ta = 25 °C)

FORWARD CURRENT vs. FORWARD VOLTAGE



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

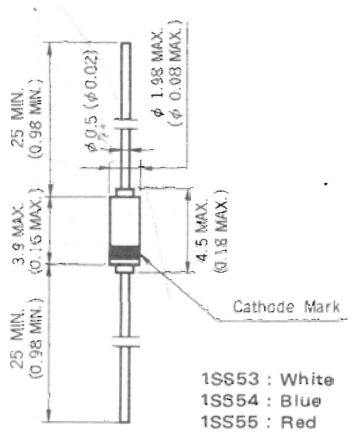
SILICON DIODES
1SS53,1SS54,1SS55

DESCRIPTION The 1SS53, 1SS54, and 1SS55 are silicon epitaxial planar diodes designed for general purpose applications.

FEATURES

- Miniature package.
- High power dissipation.
- Low leakage.
- Low price.

PACKAGE DIMENSIONS
in millimeters (inches)



EIAJ : SC-40
JEDEC : DO-35

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	200	°C
Storage Temperature	T_{stg}	−65 to +200	°C

Maximum Power Dissipation (Ta=25 °C)

Power Dissipation	P_T	500	mW

Maximum Voltages and Currents (Ta=25 °C)

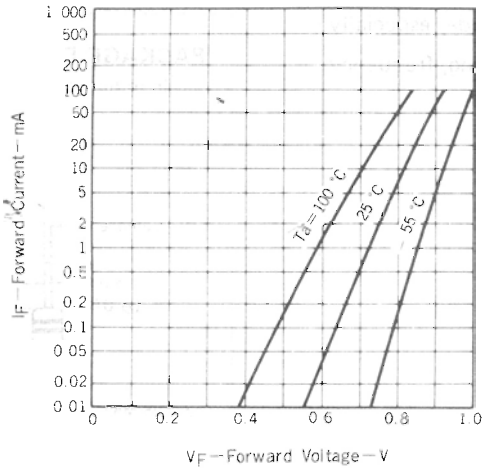
		1SS53	1SS54	1SS55	
Peak Reverse Voltage	V_{RM}	35	75	100	V
Reverse Voltage	V_R	30	50	75	V
Peak Forward Surge Current (1 μs)	$I_{F(surge)}$		2 000		mA
Peak Forward Current	I_{FM}		300		mA
Average Rectified Current	I_O		100		mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

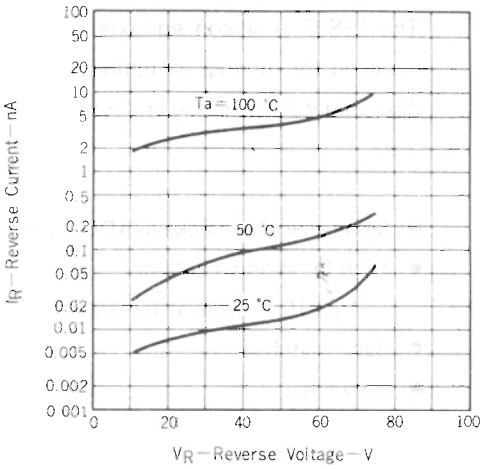
SYMBOL	CHARACTERISTIC	1SS53			1SS54			1SS55			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_F	Forward Voltage		0.7	0.8		0.7	0.8		0.7	0.8	V	I_F=1.0 mA
V_F	Forward Voltage		0.85	1.0		0.85	1.0		0.85	1.0	V	I_F=30 mA
I_R	Reverse Current			0.1							μA	V_R=30 V
I_R	Reverse Current						0.1				μA	V_R=50 V
I_R	Reverse Current									0.1	μA	V_R=75 V
C_t	Terminal Capacitance			6.0			5.0			4.0	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time		20	100		20	100		20	100	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

TYPICAL CHARACTERISTICS (Ta = 25 °C)

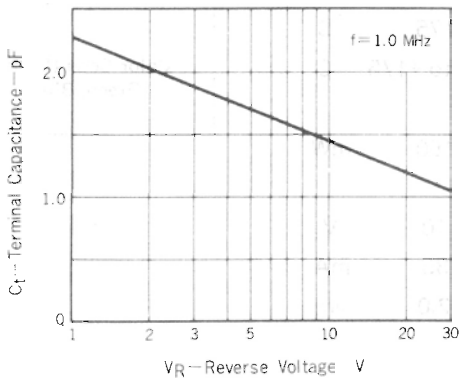
FORWARD CURRENT vs. FORWARD VOLTAGE



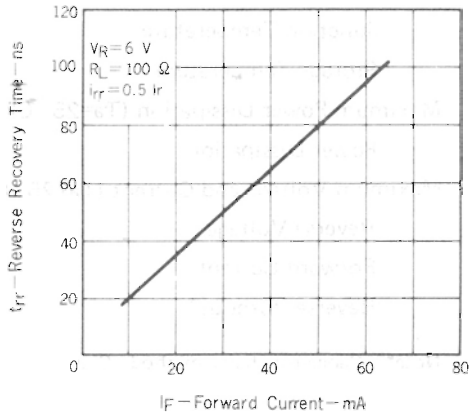
REVERSE CURRENT vs. REVERSE VOLTAGE (1SS55)



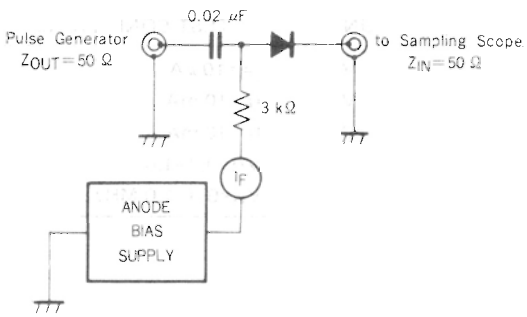
TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

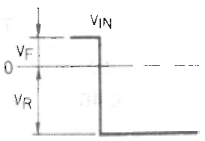


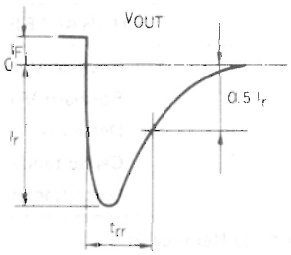
REVERSE RECOVERY TIME vs. FORWARD CURRENT



trr REVERSE RECOVERY TIME TEST CIRCUIT







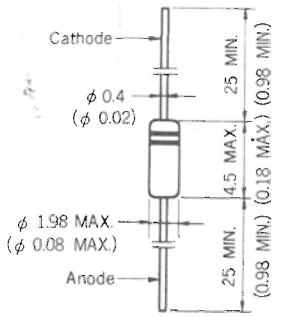
Test Conditions : I_F=10 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

SILICON MIXER DIODE
1SS97

DESCRIPTION The 1SS97 is silicon epitaxial schottky barrier diode, especially designed for mixing, switching, log or A-D converting, frequency discriminating sampling and wave shaping.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code (from cathode)
Green, Blue

FEATURES

- Small size glass package. (DO-35 TYPE)
- High breakdown voltage:
  V_R=10 V MIN. at I_R=10 μA
- Bach matched.
- Low cost.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	150	mW
Maximum Voltage and Current (Ta=25 °C)			
Reverse Voltage	V_R	10	V
Forward Current	I_F	35	mA
Reverse Burnout*	B_o	2.0	erg

Note* : Capacitor charge method C(charge)=25 pF

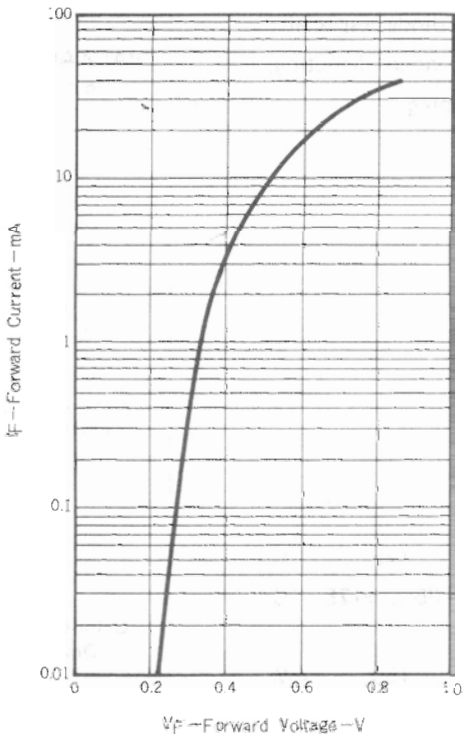
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	10			V	I_R=10 μA
V_F	Forward Voltage	0.46		0.55	V	I_F=10 mA
ΔV_F	Delta Forward Voltage*			10	mV	I_F=10 mA
C_t	Capacitance			1.0	pF	V_R=0, f=1.0 MHz
ΔC_t	Delta Capacitance*			0.2	pF	V_R=0, f=1.0 MHz

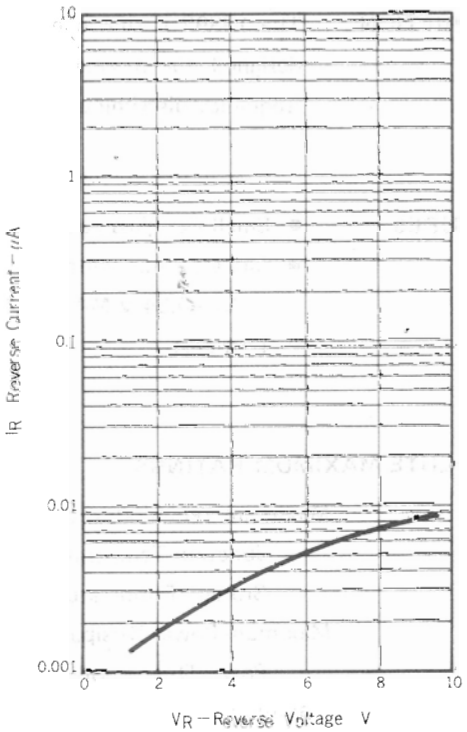
Note * : Difference of V_F, C_t.

TYPICAL CHARACTERISTICS (Ta=25 °C)

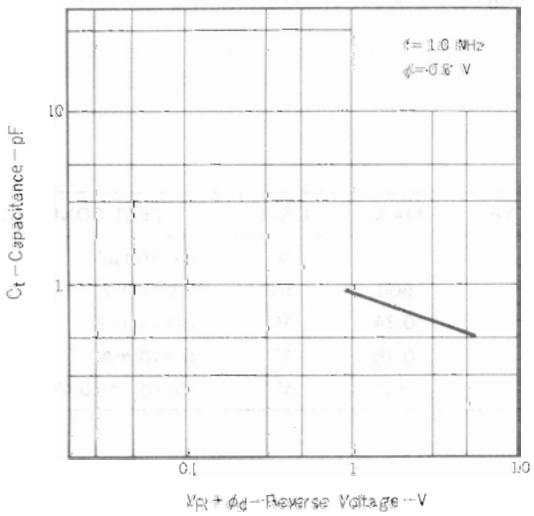
FORWARD CURRENT vs.
FORWARD VOLTAGE



REVERSE CURRENT vs.
REVERSE VOLTAGE



CAPACITANCE vs.
REVERSE VOLTAGE

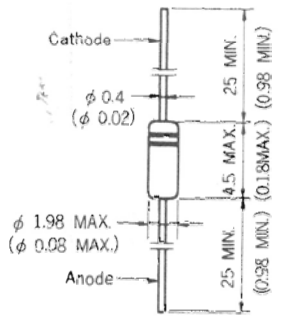


NEC
ELECTRON DEVICE

SILICON MIXER DIODE
1SS98

DESCRIPTION The 1SS98 is silicon epitaxial schottky barrier diode, especially designed for mixing, log or A-D converting, video detecting, frequency discriminating, sampling and wave shaping.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code (from cathode)
Orange, Blue

FEATURES

- Small size glass package. (DO-35 TYPE)
- Midle turn-on voltage.
  V_F=0.34 V MAX. at I_F=1 mA
- Low cost.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	150	mW
Maximum Voltage and Current (Ta=25 °C)			
Reverse Voltage	V_R	5.0	V
Forward Current	I_F	50	mA
Reverse Burnout*	B_o	2.0	erg

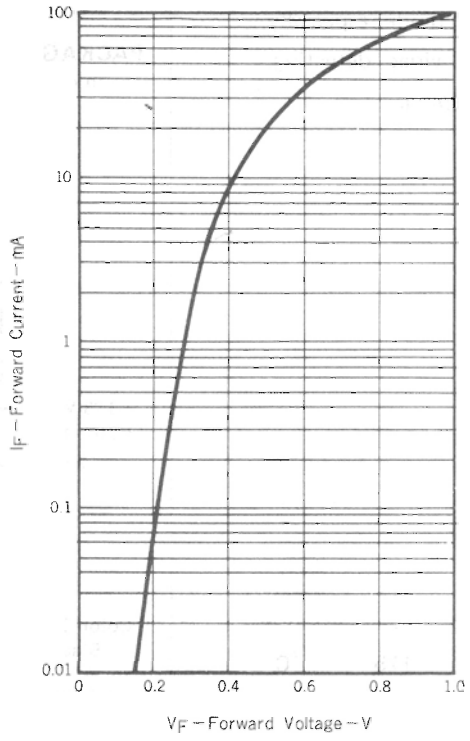
Note * : Capacitor charge method C(charge)=25 pF

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

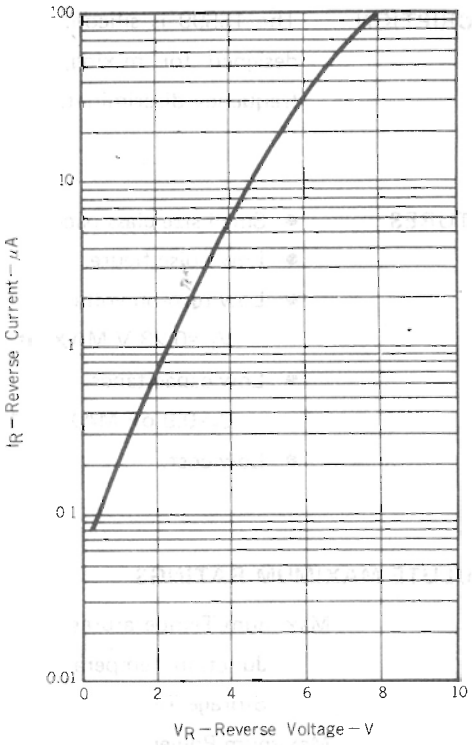
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	5.0			V	I_R=100 μA
I_R	Reverse Current			500	nA	V_R=1.0 V
V_{F1}	Forward Voltage			0.34	V	I_F=1.0 mA
V_{F2}	Forward Voltage			0.45	V	I_F=10 mA
C_t	Capacitance			1.0	pF	V_R=0, f=1.0 MHz

TYPICAL CHARACTERISTICS (Ta=25 °C)

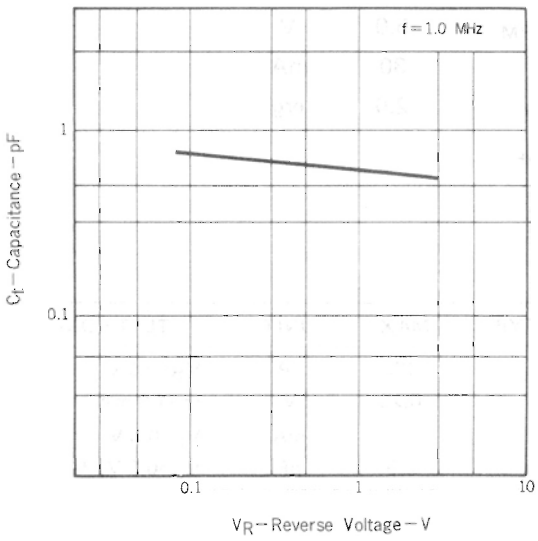
FORWARD CURRENT vs.
FORWARD VOLTAGE



REVERSE CURRENT vs.
REVERSE VOLTAGE



CAPACITANCE vs.
REVERSE VOLTAGE



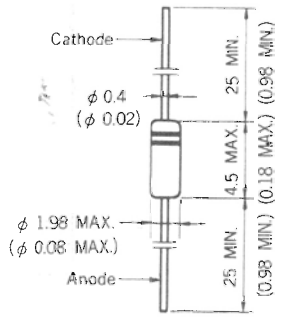
NEC
ELECTRON DEVICE

SILICON DETECTOR & MIXER DIODE

1SS99

DESCRIPTION The 1SS99 is silicon epitaxial schottky barrier diode, especially designed for mixing, log or A-D converting, video detecting, frequency discriminating, sampling and wave shaping.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code (from cathode)
Black, Blue

FEATURES

- Small size glass package. (DO-35 TYPE)
- Low noise figure.
- Low turn-on voltage.
  V_F=0.23 V MAX. at I_F=1 mA
- Low capacitance.
  C_t=0.9 pF MAX. at 1 MHz, V_R=0.2 V
- Low cost.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	150	mW
Maximum Voltage and Current (Ta=25 °C)			
Peak Reverse Voltage	V_{RM}	5.0	V
Forward Current	I_F	30	mA
Reverse Burnout*	B_o	2.0	erg

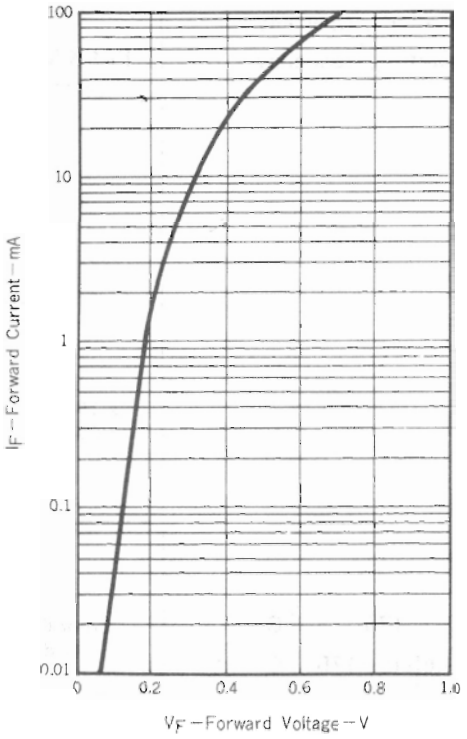
Note* : Capacitor charge method C(charge)=25 pF

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

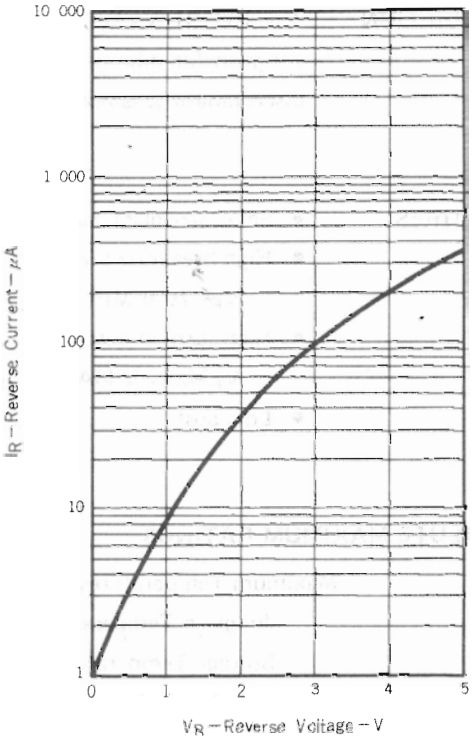
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_R	Reverse Current			25	μA	V_R=0.5 V
V_F	Forward Voltage			0.23	V	I_F=1.0 mA
I_F	Forward Current	30			mA	V_F=0.5 V
C_t	Capacitance			0.9	pF	V_R=0.2 V, f=1 MHz

TYPICAL CHARACTERISTICS (Ta=25 °C)

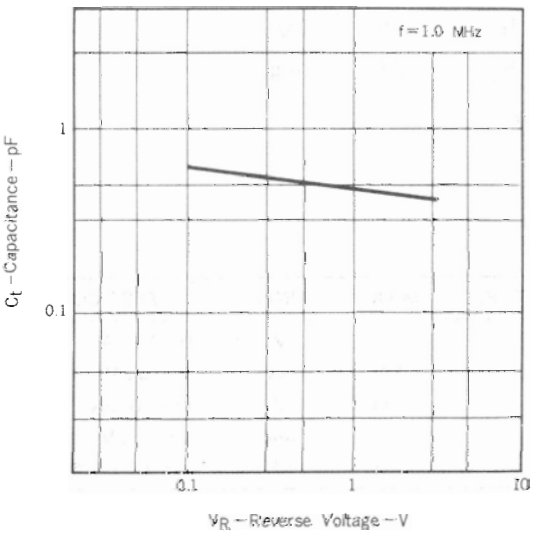
FORWARD CURRENT vs.
FORWARD VOLTAGE



REVERSE CURRENT vs.
REVERSE VOLTAGE



CAPACITANCE vs.
REVERSE VOLTAGE

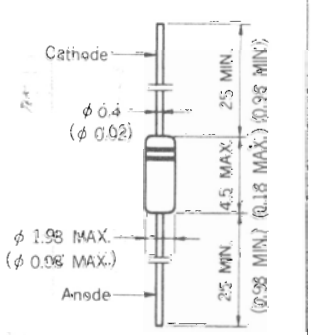


NEC
ELECTRON DEVICE

SILICON MIXER DIODE
1SS101

DESCRIPTION The 1SS101 is silicon epitaxial schottky barrier diode, especially designed for mixing, switching, log or A-D converting, frequency discriminating, sampling and wave shaping.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code (from cathode)
Red, Blue

FEATURES

- Small size glass package. (DO-35 TYPE)
- High breakdown voltage.
  V_R=70 V MIN. at I_R=10 μA
- High turn-on voltage.
  V_F=0.41 V MAX. at I_F=1 mA
- Low cost.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	150	mW
Maximum Voltage and Current (Ta=25 °C)			
Reverse Voltage	V_R	70	V
Forward Current	I_F	15	mA
Reverse Burnout*	B_o	2.0	erg

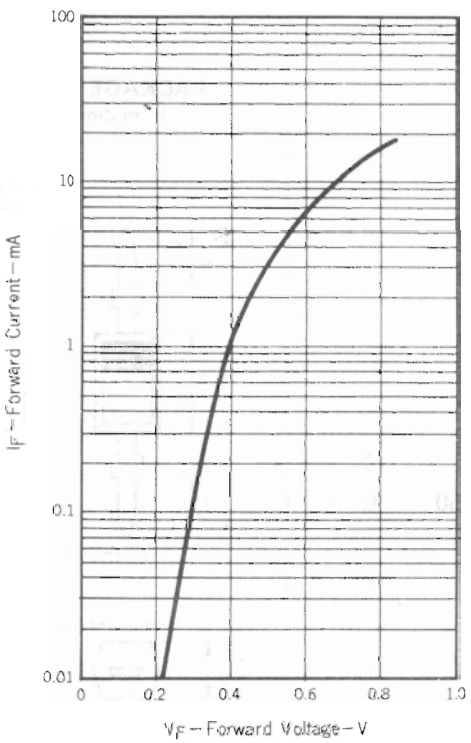
Note* : Capacitor charge method C(charge)=25 pF

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

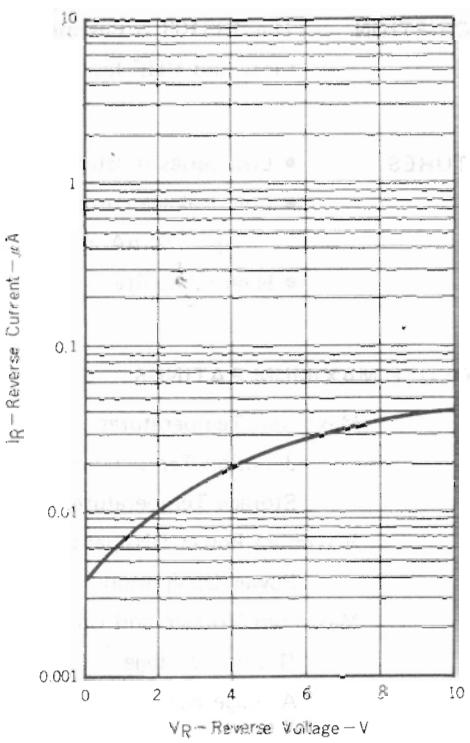
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	70			V	I_R=10 μA
I_R	Reverse Current			200	nA	V_R=50 V
V_F	Forward Voltage			0.41	V	I_F=1.0 mA
I_F	Forward Current	15			mA	V_F=1.0 V
C_T	Capacitance			2.0	pF	V_R=0, f=1.0 MHz

TYPICAL CHARACTERISTICS (Ta=25 °C)

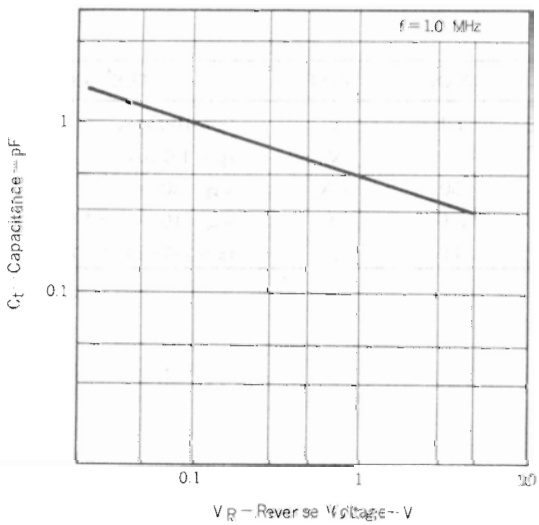
FORWARD CURRENT vs.
FORWARD VOLTAGE



REVERSE CURRENT vs.
REVERSE VOLTAGE



CAPACITANCE vs.
REVERSE VOLTAGE



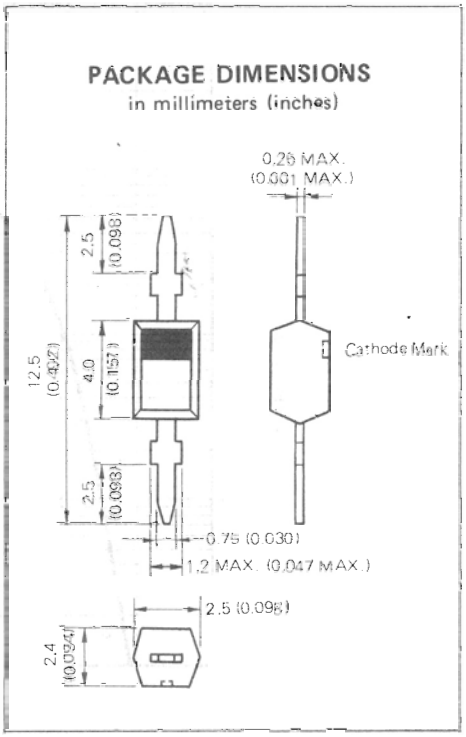
NEC
ELECTRON DEVICE

SILICON SWITCHING DIODE
1SS103

DESCRIPTION The 1SS103 is designed for use in UHF/VHF electronic tuner and VHF low, high channel switch.

FEATURES

- Low series resistance r_s.
- Low leakage current.
  $I_R \leqq 50$ nA at $V_R = 30$ V
- High reliability.



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Maximum Power Dissipation (Ta = 25 °C)			
Power Dissipation	P_T	150	mW
Maximum Voltage and Current (Ta = 25 °C)			
Reverse Voltage	V_R	35	V
Average Rectified Current	I_o	100	mA

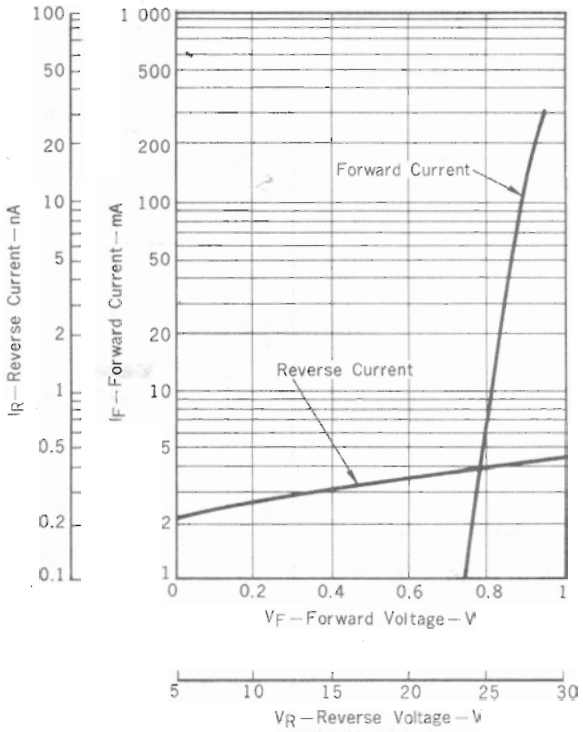
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage			1.1	V	$I_F = 100$ mA
V_R	Reverse Voltage	35			V	$I_R = 1.0$ μA
I_R	Reverse Current		0.5	50	nA	$V_R = 30$ V
C_t	Terminal Capacitance		1.5	2.0	pF	$V_R = 15$ V, f = 1.0 MHz
r_{rs}	RF Series Resistance		0.5	0.6	Ω	$I_F = 2.0$ mA, f = 100 MHz

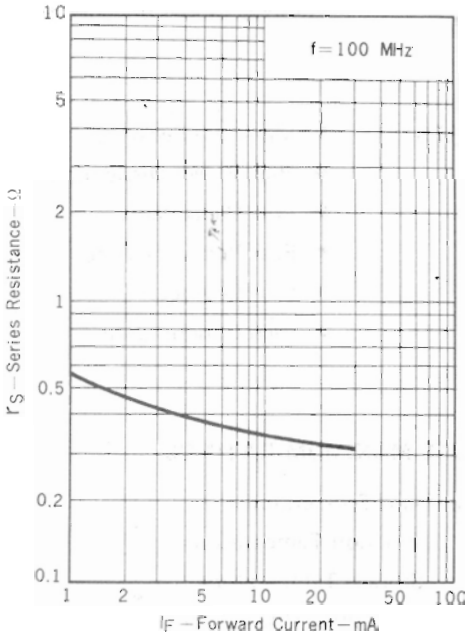
TYPICAL CHARACTERISTICS (Ta = 25 °C)

FORWARD CURRENT vs.
FORWARD VOLTAGE

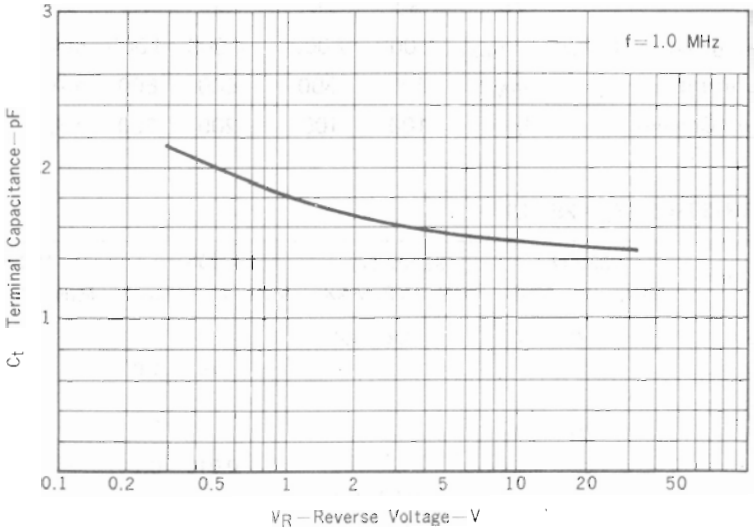
REVERSE CURRENT vs.
REVERSE VOLTAGE



SERIES RESISTANCE vs.
FORWARD CURRENT



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

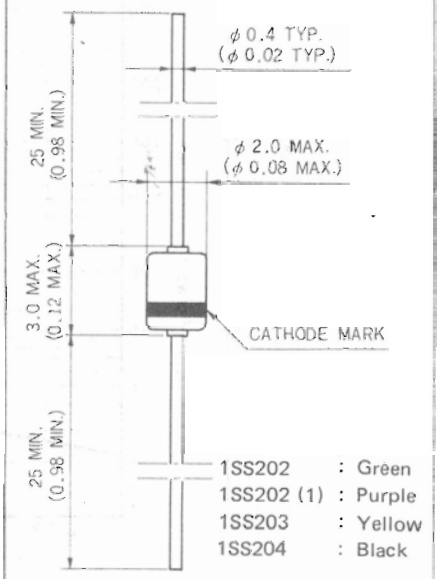
SILICON SWITCHING DIODES
1SS202,1SS202(1),1SS203,1SS204

DESCRIPTION The 1SS202, 1SS202(1), 1SS203 and 1SS204 are silicon epitaxial diodes designed for high speed switching applications.

FEATURES

- Miniature Package.
- High Power Dissipation.
- Low Capacitance.
- Fast Recovery Time.
- Low Leakage.
- High Conductance.

PACKAGE DIMENSIONS
in millimeters (inches)



1SS202 : Green
1SS202 (1) : Purple
1SS203 : Yellow
1SS204 : Black

EIAJ : —
JEDEC : DO-34

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	200	°C
Storage Temperature	T_{stg}	−65 to +200	°C

Maximum Power Dissipation (T_a=25 °C)

Power Dissipation	P_T	400	mW

Maximum Voltages and Currents (T_a=25 °C)

		1SS202	1SS202 (1)	1SS203	1SS204	
Peak Reverse Voltage	V_{RM}	35	100	75	100	V
Reverse Voltage	V_R	30	75	50	75	V
Peak Forward Surge Current (1 μs)	$I_{F(surge)}$	2 000	2 000	4 000	4 000	mA
Peak Forward Current	I_{FM}	300	300	600	600	mA
Average Rectified Current	I_O	100	100	200	200	mA

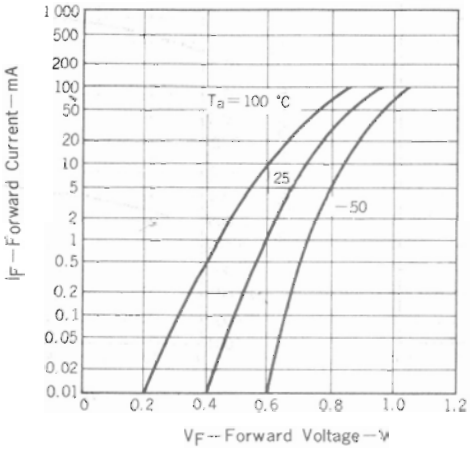
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	1SS202 MIN.	1SS202 TYP.	1SS202 MAX.	1SS202 (1) MIN.	1SS202 (1) TYP.	1SS202 (1) MAX.	1SS203 MIN.	1SS203 TYP.	1SS203 MAX.	1SS204 MIN.	1SS204 TYP.	1SS204 MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.8	1.0		0.8	1.0							V	I_F=30 mA
V_F	Forward Voltage								0.9	1.0				V	I_F=100 mA
V_F	Forward Voltage											0.9	1.0	V	I_F=150 mA
I_R	Reverse Current		0.01	0.1										μA	V_R=30 V
I_R	Reverse Current								0.015	0.1				μA	V_R=50 V
I_R	Reverse Current					0.03	0.1					0.03	0.1	μA	V_R=75 V
C_t	Terminal Capacitance		2.0	4.0		2.0	4.0		2.0	3.5		2.0	3.0	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

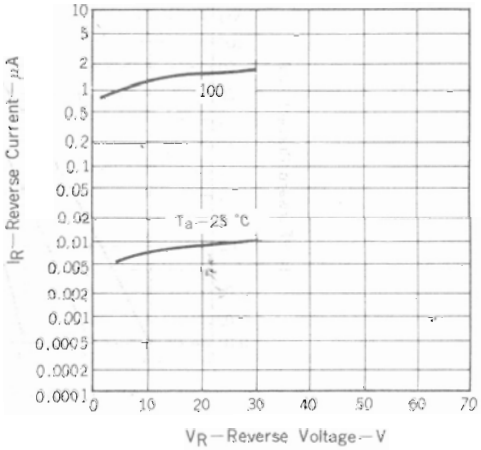
TYPICAL CHARACTERISTICS (T_a = 25 °C)

1SS202

FORWARD CURRENT vs. FORWARD VOLTAGE

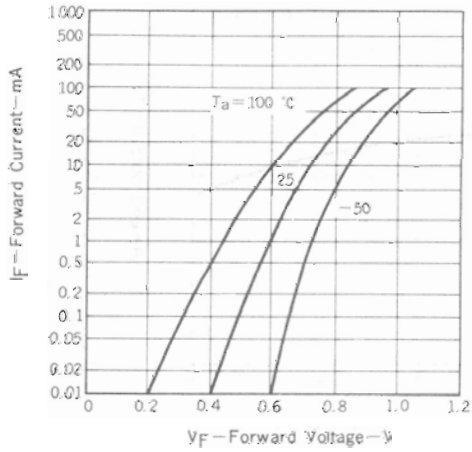


REVERSE CURRENT vs. REVERSE VOLTAGE

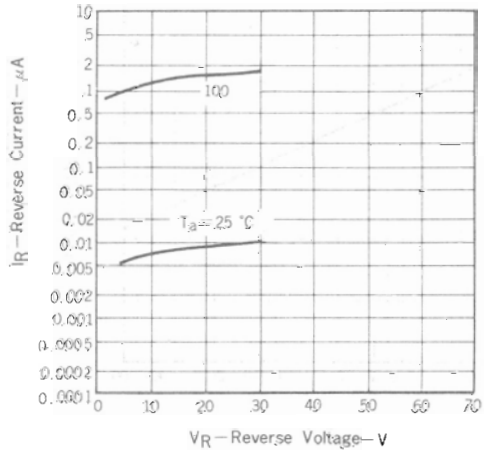


1SS202 (1)

FORWARD CURRENT vs. FORWARD VOLTAGE

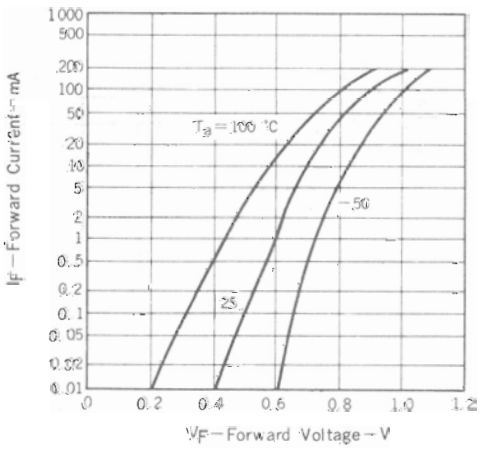


REVERSE CURRENT vs. REVERSE VOLTAGE

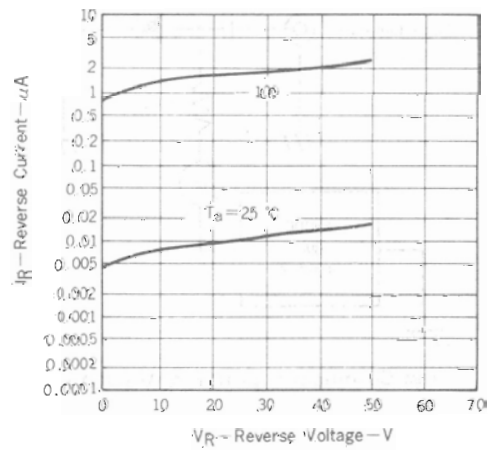


1SS203

FORWARD CURRENT vs. FORWARD VOLTAGE

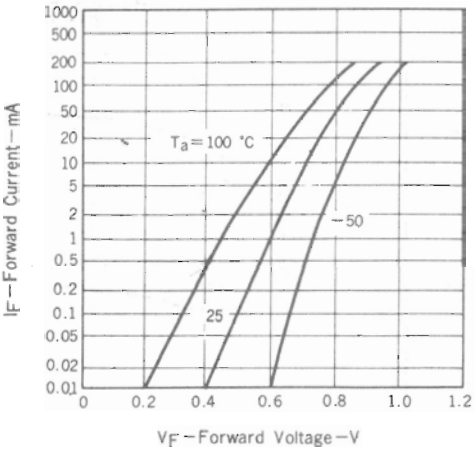


REVERSE CURRENT vs. REVERSE VOLTAGE

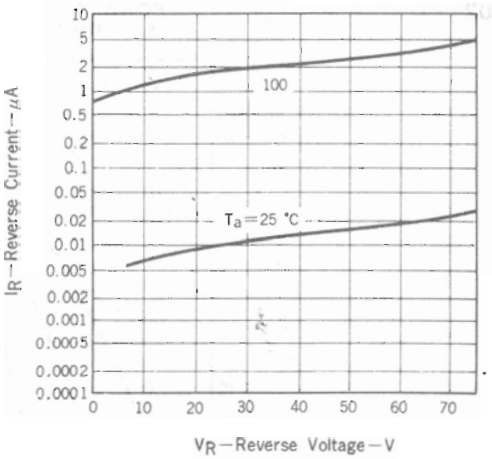


1SS204

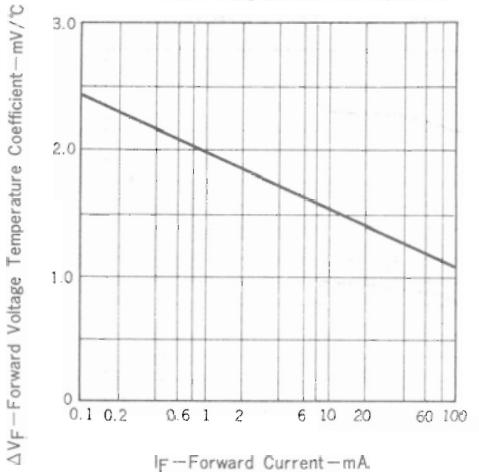
FORWARD CURRENT vs. FORWARD VOLTAGE



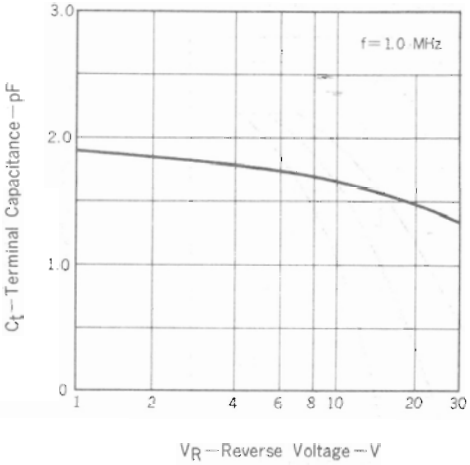
REVERSE CURRENT vs. REVERSE VOLTAGE



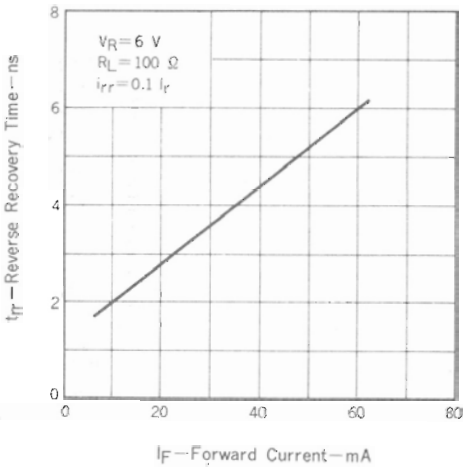
FORWARD VOLTAGE TEMPERATURE COEFFICIENT vs. FORWARD CURRENT



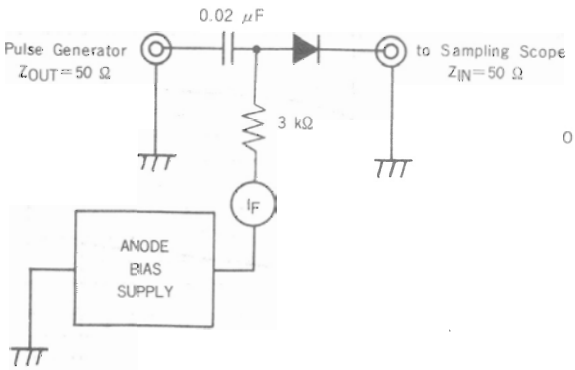
TERMINAL CAPACITANCE vs. REVERSE VOLTABE

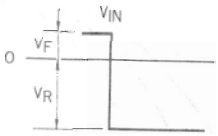


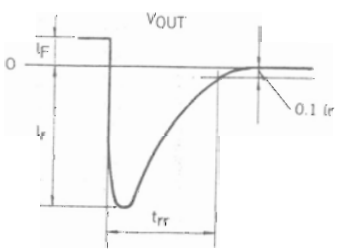
REVERSE RECOVERY TIME vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT







Test Conditions : I_F=10 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

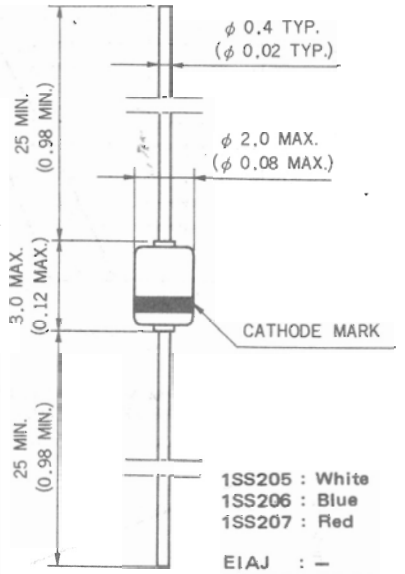
SILICON DIODES
1SS205,1SS206,1SS207

DESCRIPTION The 1SS205, 1SS206, and 1SS207 are silicon epitaxial planar diodes designed for general purpose applications.

FEATURES

- Miniature package.
- High power dissipation.
- Low leakage.
- Low price.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	200	°C
Storage Temperature	T_{stg}	−65 to +200	°C

Maximum Power Dissipation (T_a = 25 °C)

Power Dissipation	P_T	400	mW

Maximum Voltages and Currents (T_a = 25 °C)

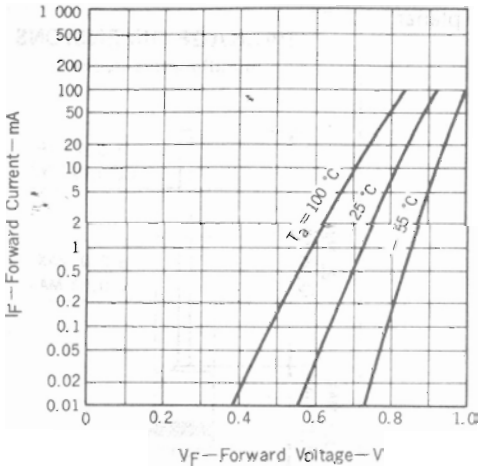
		1SS205	1SS206	1SS207	
Peak Reverse Voltage	V_{RM}	35	75	100	V
Reverse Voltage	V_R	30	50	75	V
Peak Forward Surge Current (1 μs)	$I_{F(surge)}$		2 000		mA
Peak Forward Current	I_{FM}		300		mA
Average Rectified Current	I_O		100		mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

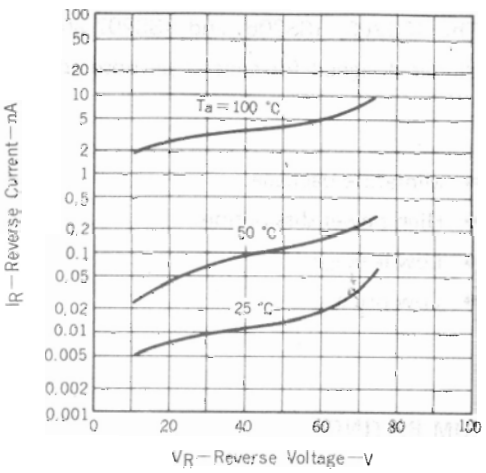
SYMBOL	CHARACTERISTIC	1SS205			1SS206			1SS207			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_F	Forward Voltage		0.7	0.8		0.7	0.8		0.7	0.8	V	I_F=1.0 mA
V_F	Forward Voltage		0.85	1.0		0.85	1.0		0.85	1.0	V	I_F=30 mA
I_R	Reverse Current			0.1							μA	V_R=30 V
I_R	Reverse Current						0.1				μA	V_R=50 V
I_R	Reverse Current									0.1	μA	V_R=75 V
C_t	Terminal Capacitance			6.0			5.0			4.0	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time		20	100		20	100		20	100	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

TYPICAL CHARACTERISTICS (T_a = 25 °C)

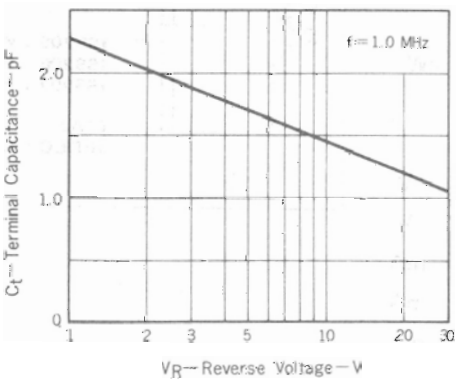
FORWARD CURRENT vs. FORWARD VOLTAGE



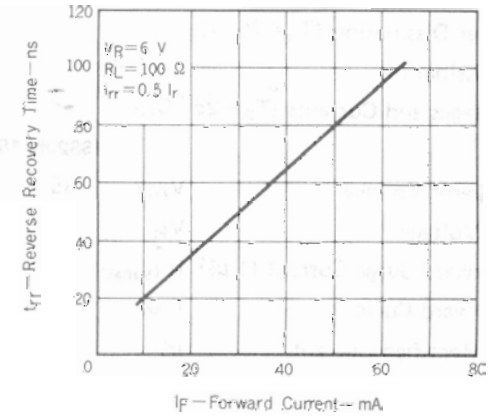
REVERSE CURRENT vs. REVERSE VOLTAGE
(1SS207)



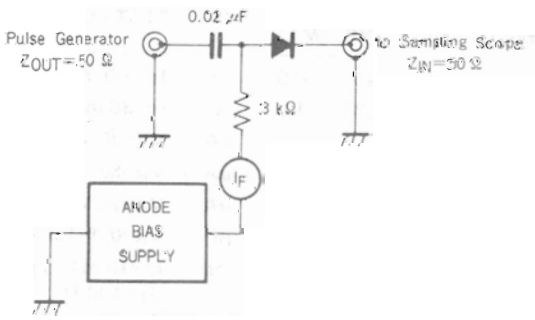
TERMINAL CAPACITANCE
vs. REVERSE VOLTAGE

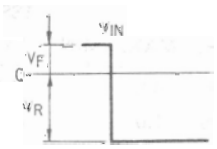


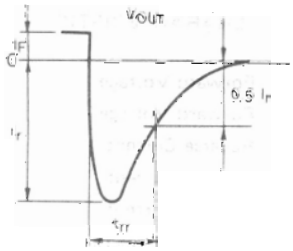
REVERSE RECOVERY TIME
vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT







Test Conditions : I_F=1.0 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

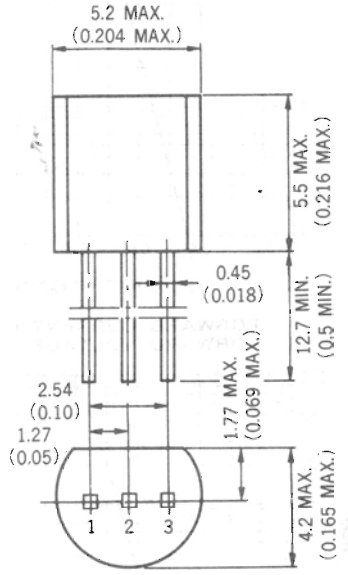
SILICON SWITCHING DIODES
1SS229, 1SS230

DESCRIPTION The 1SS229 and 1SS230 are silicon epitaxial planar double diodes designed for high speed switching applications.

FEATURES

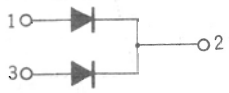
- Low Capacitance.
- Fast Recovery Time.
- Low Leakage.
- High Conductance.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Anode
2. Cathode
3. Anode

EIAJ : SC-43A
JEDEC : TO-92
IEC : PA33



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures				
Junction Temperature	T_j	150		°C
Storage Temperature	T_{stg}	−55 to +150		°C
Maximum Power Dissipation (T_a=25 °C)				
Power Dissipation	P_T*	300		mW
Maximum Voltages and Currents (T_a=25 °C)				
		1SS229	1SS230	
Peak Reverse Voltage	V_{RM}	35	75	V
Reverse Voltage	V_R	35	75	V
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$*	6 000	6 000	mA
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$	4 000	4 000	mA
Peak Forward Current	I_{FM}*	450	450	mA
Peak Forward Current	I_{FM}	300	300	mA
Average Rectified Current	I_O*	200	200	mA
Average Rectified Current	I_O	100	100	mA

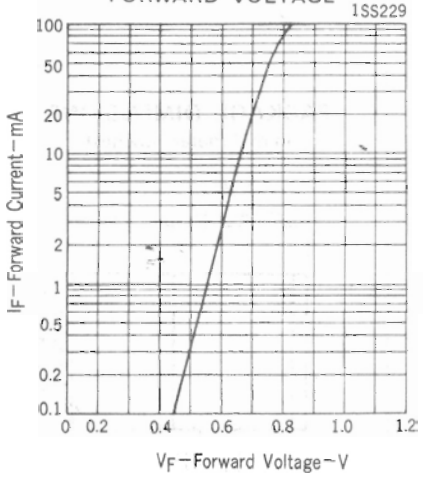
(Note) * Total Value

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

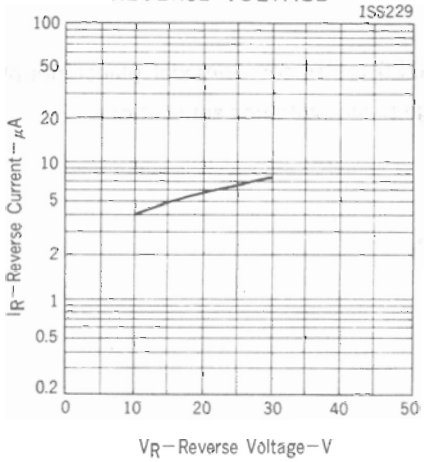
SYMBOL	CHARACTERISTIC	1SS229			1SS230			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_F	Forward Voltage		0.67	1.0		0.67	1.0	V	I_F=10 mA
V_F	Forward Voltage		0.75	1.1		0.75	1.1	V	I_F=50 mA
V_F	Forward Voltage		0.85	1.2		0.85	1.2	V	I_F=100 mA
I_R	Reverse Current			0.1				μA	V_R=30 V
I_R	Reverse Current						0.1	μA	V_R=50 V
C_t	Terminal Capacitance		1.1	4.0		1.1	4.0	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time			3.0			3.0	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

TYPICAL CHARACTERISTICS (T_a=25 °C)

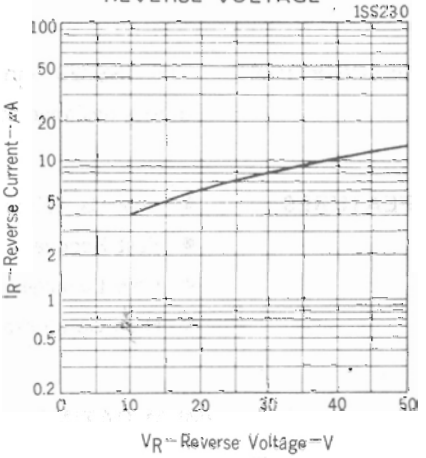
FORWARD CURRENT vs. FORWARD VOLTAGE



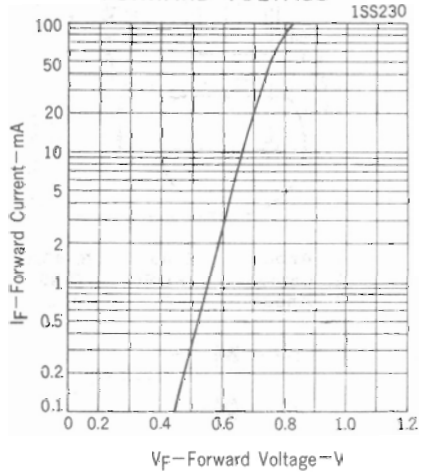
REVERSE CURRENT vs. REVERSE VOLTAGE



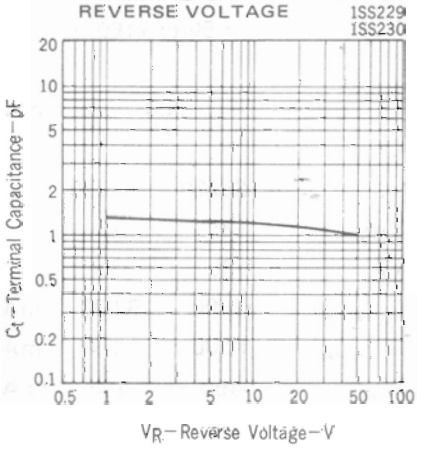
REVERSE CURRENT vs. REVERSE VOLTAGE



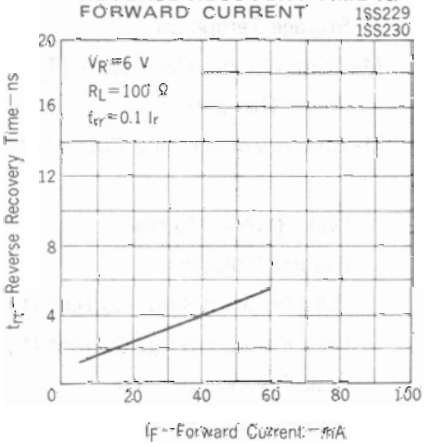
FORWARD CURRENT vs. FORWARD VOLTAGE



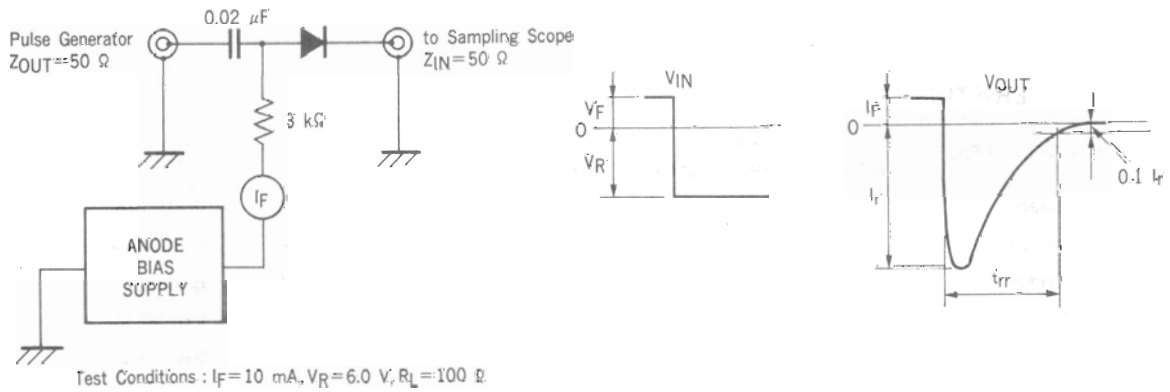
TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



REVERSE RECOVERY TIME vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT



Test Conditions : I_F = 10 mA, V_R = 6.0 V, R_L = 100 Ω

NEC
ELECTRON DEVICE

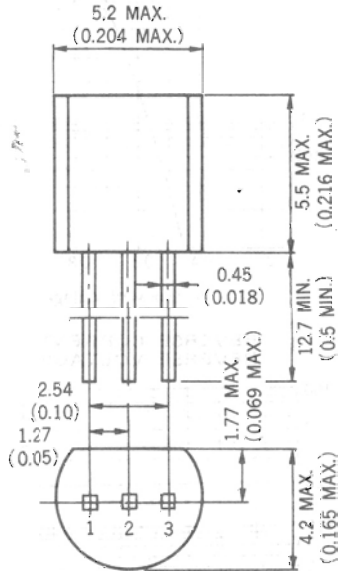
SILICON SWITCHING DIODES
1SS231, 1SS232

DESCRIPTION The 1SS231 and 1SS232 are silicon epitaxial planar double diodes designed for high speed switching applications.

FEATURES

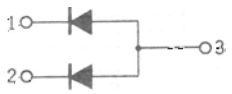
- Low Capacitance.
- Fast Recovery Time.
- Low Leakage.
- High Conductance.

PACKAGE DIMENSIONS
in millimeters (inches)



1. Cathode
2. Anode
3. Cathode

EIAJ : SC-43A
JEDEC : TO-92
IEC : PA33



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures				
Junction Temperature	T_j	150		°C
Storage Temperature	T_{stg}	−55 to +150		°C
Maximum Power Dissipation (T_a=25 °C)				
Power Dissipation	P_T*	250		mW
Maximum Voltages and Currents (T_a=25 °C)				
		1SS231	1SS232	
Peak Reverse Voltage	V_{RM}	35	75	V
Reverse Voltage	V_R	35	75	V
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$*	6 000	6 000	mA
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$	4 000	4 000	mA
Peak Forward Current	I_{FM}*	450	450	mA
Peak Forward Current	I_{FM}	300	300	mA
Average Rectified Current	I_O*	200	200	mA
Average Rectified Current	I_O	100	100	mA

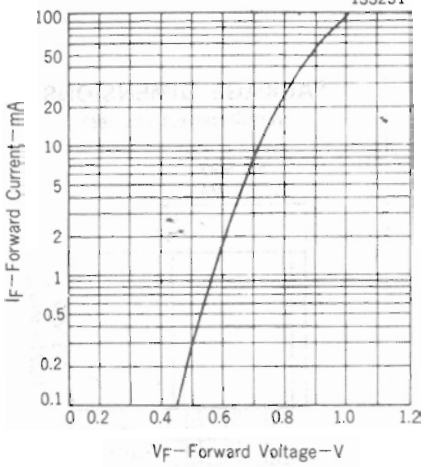
(Note) * Total Value

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

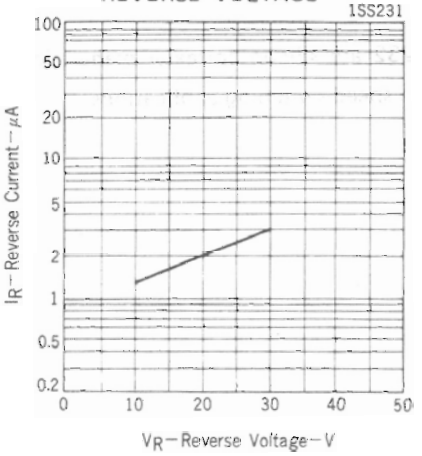
SYMBOL	CHARACTERISTIC	1SS231 MIN.	1SS231 TYP.	1SS231 MAX.	1SS232 MIN.	1SS232 TYP.	1SS232 MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.72	1.0		0.72	1.0	V	I_F=10 mA
V_F	Forward Voltage		0.88	1.1		0.88	1.1	V	I_F=50 mA
V_F	Forward Voltage		1.0	1.2		1.0	1.2	V	I_F=100 mA
I_R	Reverse Current			0.1				μA	V_R=30 V
I_R	Reverse Current						0.1	μA	V_R=50 V
C_t	Terminal Capacitance		2.5	4.0		2.5	3.5	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time			4.0			4.0	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

TYPICAL CHARACTERISTICS (T_a=25 °C)

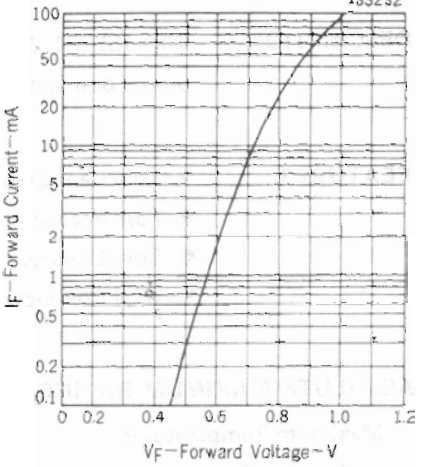
FORWARD CURRENT vs. FORWARD VOLTAGE



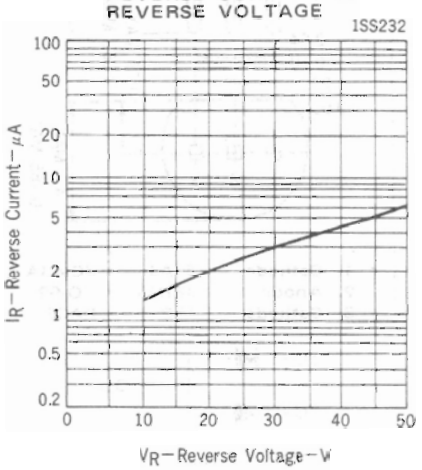
REVERSE CURRENT vs. REVERSE VOLTAGE



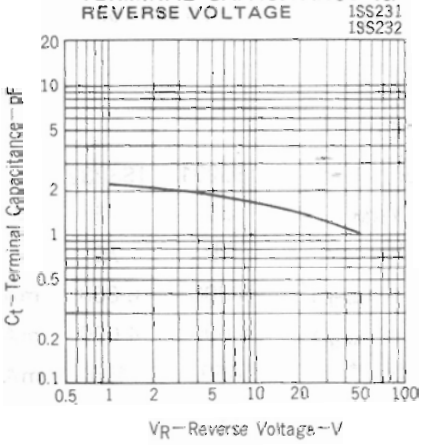
FORWARD CURRENT vs. FORWARD VOLTAGE



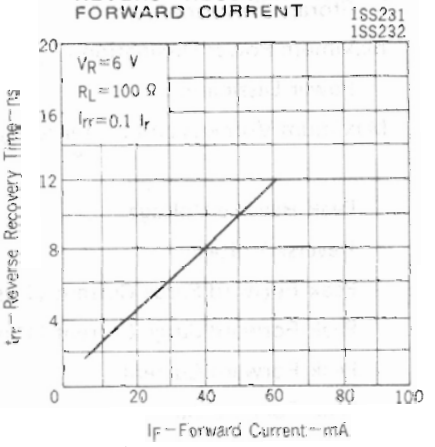
REVERSE CURRENT vs. REVERSE VOLTAGE



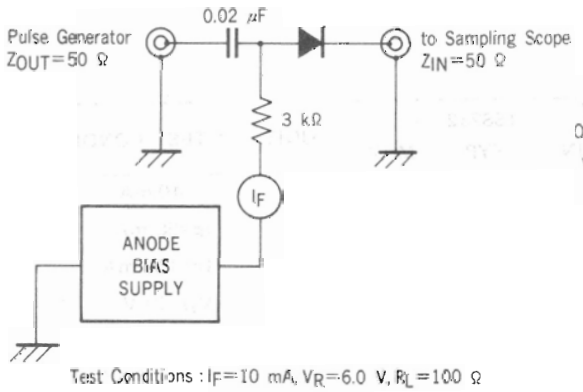
TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

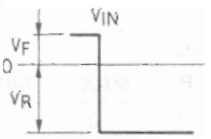


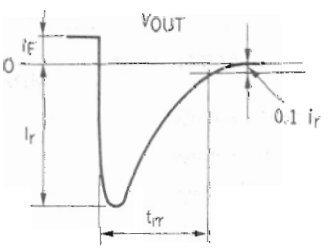
REVERSE RECOVERY TIME vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT







Test Conditions : I_F=10 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

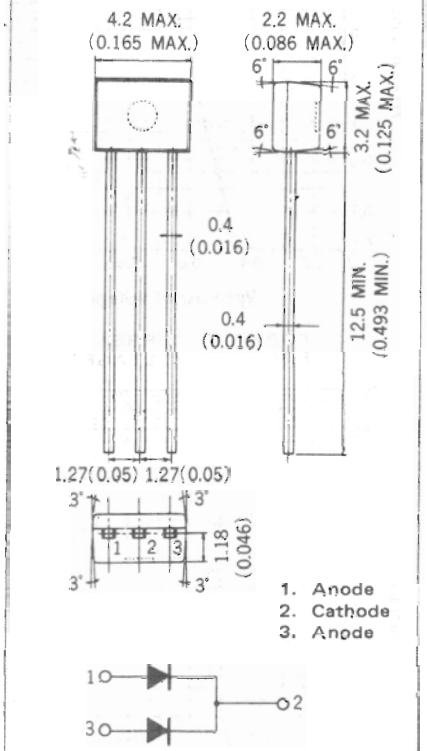
SILICON SWITCHING DIODES
1SS233, 1SS234

DESCRIPTION The 1SS233 and 1SS234 are silicon epitaxial planar double diodes designed for high speed switching applications.

FEATURES

- Low Capacitance.
- Fast Recovery Time.
- Low Leakage.
- High Conductance.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Maximum Power Dissipation (T_a=25 °C)

Power Dissipation	P_T*	250	mW

Maximum Voltages and Currents (T_a=25 °C)

		1SS233	1SS234	
Peak Reverse Voltage	V_{RM}	35	75	V
Reverse Voltage	V_R	35	75	V
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$*	6 000	6 000	mA
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$	4 000	4 000	mA
Peak Forward Current	I_{FM}*	450	450	mA
Peak Forward Current	I_{FM}	300	300	mA
Average Rectified Current	I_O*	200	200	mA
Average Rectified Current	I_O	100	100	mA

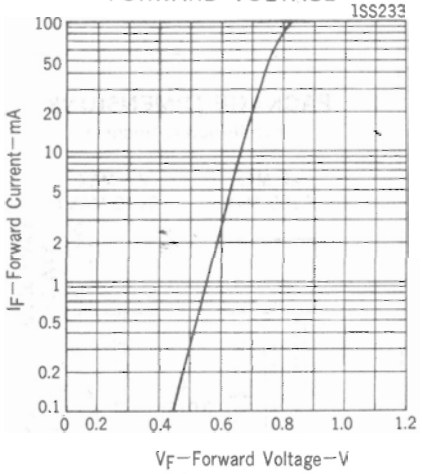
(Note) * Total Value

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

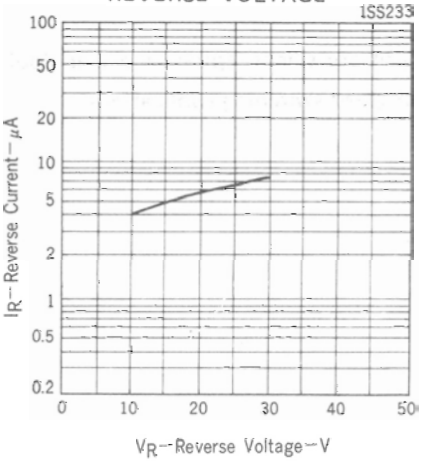
SYMBOL	CHARACTERISTIC	1SS233 MIN.	1SS233 TYP.	1SS233 MAX.	1SS234 MIN.	1SS234 TYP.	1SS234 MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.67	1.0		0.67	1.0	V	I_F=10 mA
V_F	Forward Voltage		0.75	1.1		0.75	1.1	V	I_F=50 mA
V_F	Forward Voltage		0.85	1.2		0.85	1.2	V	I_F=100 mA
I_R	Reverse Current			0.1				μA	V_R=30 V
I_R	Reverse Current						0.1	μA	V_R=50 V
C_t	Terminal Capacitance		1.1	4.0		1.1	4.0	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time			3.0			3.0	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

TYPICAL CHARACTERISTICS (T_a=25 °C)

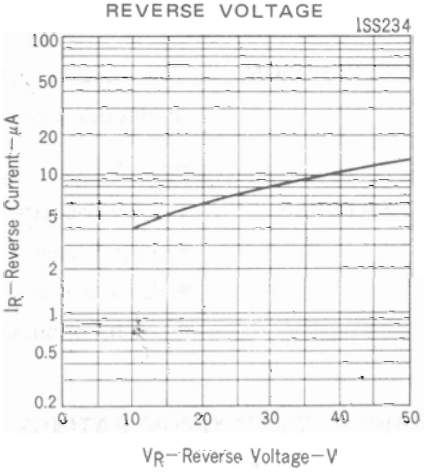
FORWARD CURRENT vs. FORWARD VOLTAGE



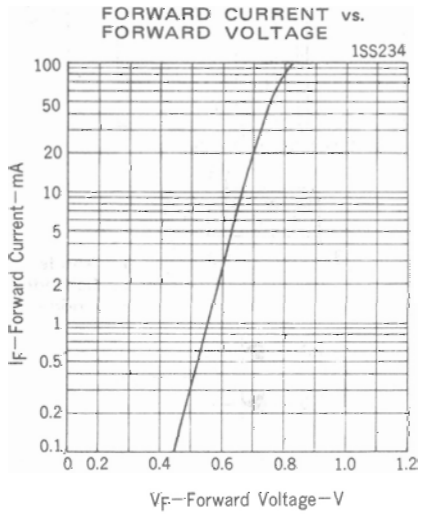
REVERSE CURRENT vs. REVERSE VOLTAGE



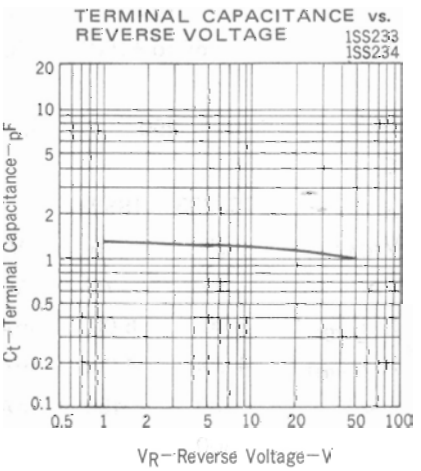
REVERSE CURRENT vs. REVERSE VOLTAGE



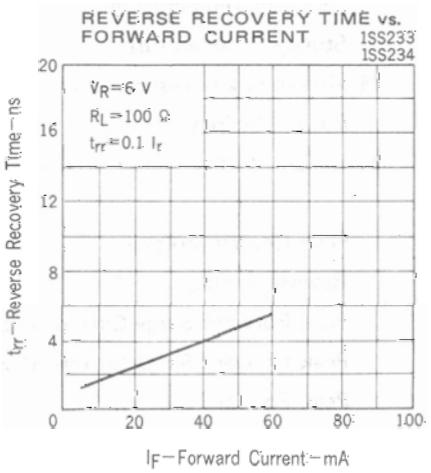
FORWARD CURRENT vs. FORWARD VOLTAGE



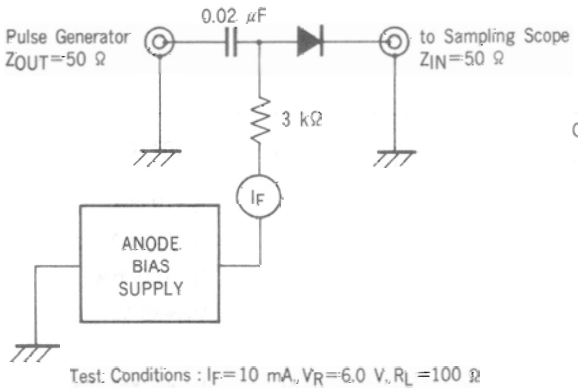
TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

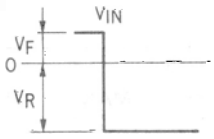


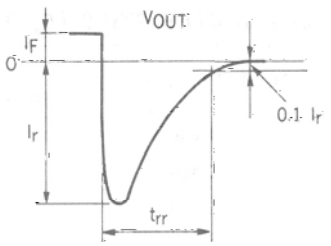
REVERSE RECOVERY TIME vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT







Test Conditions : I_F=10 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

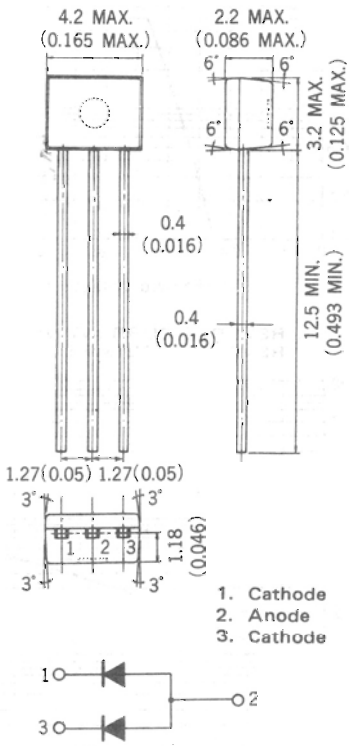
SILICON SWITCHING DIODES
1SS235, 1SS236

DESCRIPTION The 1SS235 and 1SS236 are silicon epitaxial planar double diodes designed for high speed switching applications.

FEATURES

- Low Capacitance.
- Fast Recovery Time.
- Low Leakage.
- High Conductance.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures				
Junction Temperature	T_j	150		°C
Storage Temperature	T_{stg}	−55 to +150		°C
Maximum Power Dissipation (T_a=25 °C)				
Power Dissipation	P_T*	250		mW
Maximum Voltages and Currents (T_a=25 °C)				
		1SS235	1SS236	
Peak Reverse Voltage	V_{RM}	35	75	V
Reverse Voltage	V_R	35	75	V
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$*	6 000	6 000	mA
Peak Forward Surge Current (1 μs)	$I_{F\ (surge)}$	4 000	4 000	mA
Peak Forward Current	I_{FM}*	450	450	mA
Peak Forward Current	I_{FM}	300	300	mA
Average Rectified Current	I_O*	200	200	mA
Average Rectified Current	I_O	100	100	mA

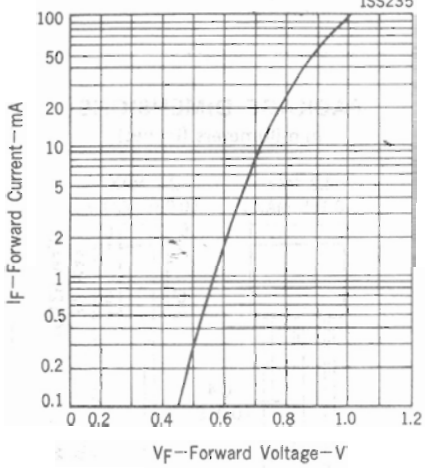
(Note) * Total Value

ELECTRICAL CHARACTERISTICS (T_a=25 °C)

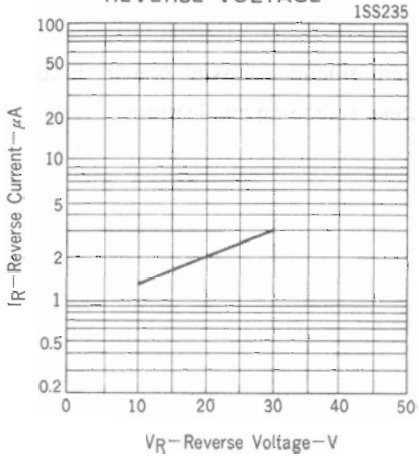
SYMBOL	CHARACTERISTIC	1SS235			1SS236			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_F	Forward Voltage		0.72	1.0		0.72	1.0	V	I_F=10 mA
V_F	Forward Voltage		0.88	1.1		0.88	1.1	V	I_F=50 mA
V_F	Forward Voltage		1.0	1.2		1.0	1.2	V	I_F=100 mA
I_R	Reverse Current			0.1				μA	V_R=30 V
I_R	Reverse Current						0.1	μA	V_R=50 V
C_t	Terminal Capacitance		2.5	4.0		2.5	3.5	pF	V_R=0, f=1.0 MHz
t_{rr}	Reverse Recovery Time			4.0			4.0	ns	I_F=10 mA, V_R=6.0 V, R_L=100 Ω

TYPICAL CHARACTERISTICS (T_a=25 °C)

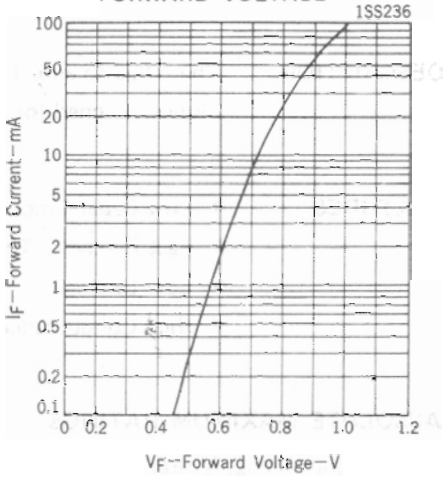
FORWARD CURRENT vs. FORWARD VOLTAGE



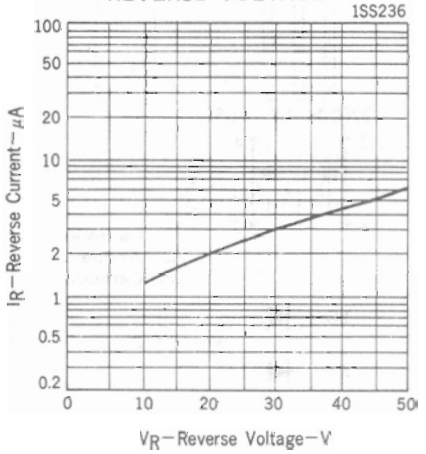
REVERSE CURRENT vs. REVERSE VOLTAGE



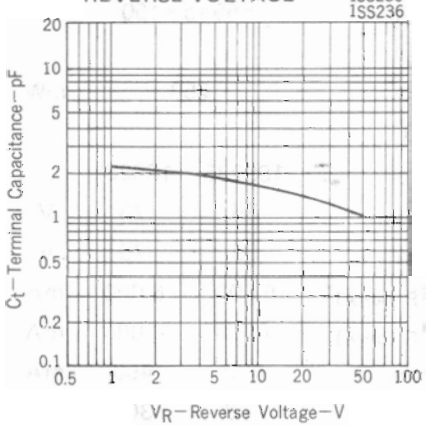
FORWARD CURRENT vs. FORWARD VOLTAGE



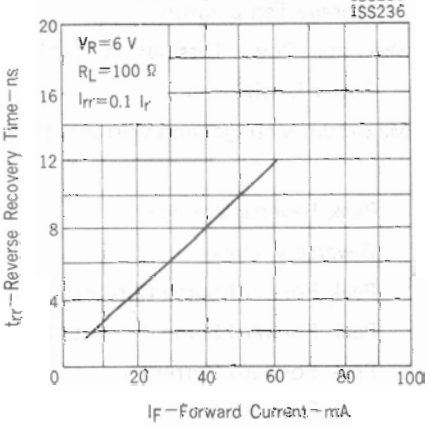
REVERSE CURRENT vs. REVERSE VOLTAGE



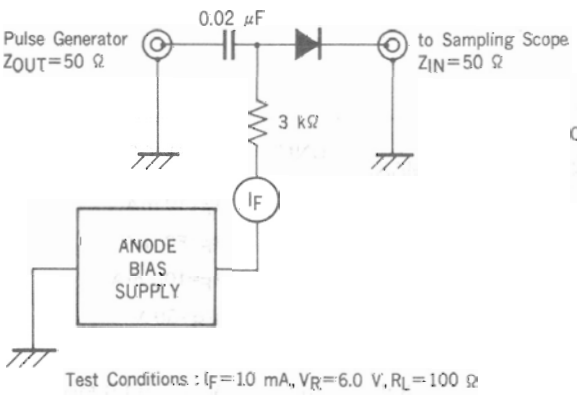
TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

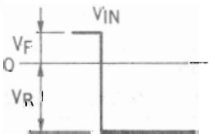


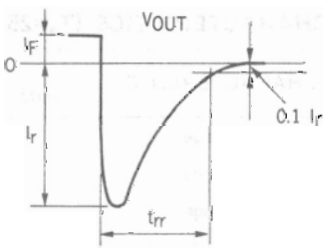
REVERSE RECOVERY TIME vs. FORWARD CURRENT



t_{rr} REVERSE RECOVERY TIME TEST CIRCUIT







Test Conditions : I_F=10 mA, V_R=6.0 V, R_L=100 Ω

NEC
ELECTRON DEVICE

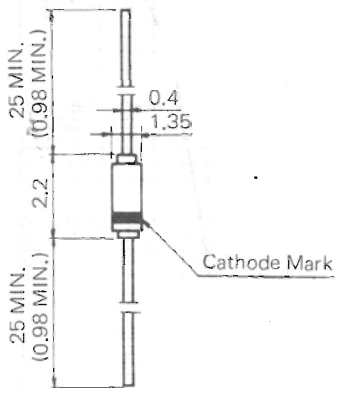
UHF DETECTOR & MIXER DIODES
1SS237,1SS237(1)

DESCRIPTION The 1SS237 is silicon epitaxial schottky barrier diode, especially designed for mixing, switching, log or A-D converting, frequency discriminating sampling and wave shaping.

FEATURES

- Small size glass package. (DO-34 TYPE; L = 2.2 mm)
- High breakdown voltage: V_R = 10 V MIN. at I_R = 10 μA
- Bach matched.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	+175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation (T_a = 25 °C)			
DC Power Dissipation	P_d	250	mW
Maximum Voltages and Currents (T_a = 25 °C)			
Reverse Voltage	V_R	10	V
Forward Current	I_F	30	mA
Reverse Burnout*	B_o	2.0	erg

Note* : Capacitor charge method C (charge) = 25 pF

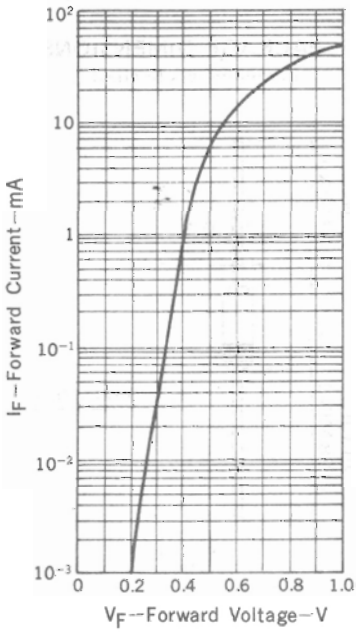
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	1SS237			1SS237 (1)			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_R	Reverse Voltage	10			10			V	I_R=10 μA
I_R	Reverse Current			100			100	mA	V_R=5.0 V
V_{F1}	Forward Voltage	0.33		0.45				V	I_F=1.0 mA
V_{F2}	Forward Voltage				0.48		0.6	V	I_F=10 mA
I_F	Forward Current	35						mA	V_F=1.0 V
C_t	Capacitance		0.8	1.0		0.8	1.0	pF	V_R=0, f=1.0 MHz
ΔV_{F2}**	Delta Forward Voltage						10	mV	I_F=10 mA
ΔC_t**	Delta Capacitance						0.2	pF	V_R=0, f=1.0 MHz
NF	Noise Figure			12.5			12.5	dB	f=855 MHz, f_{IF}=45 MHz, N_{IF}=3.7 dB, I_O=2 mA

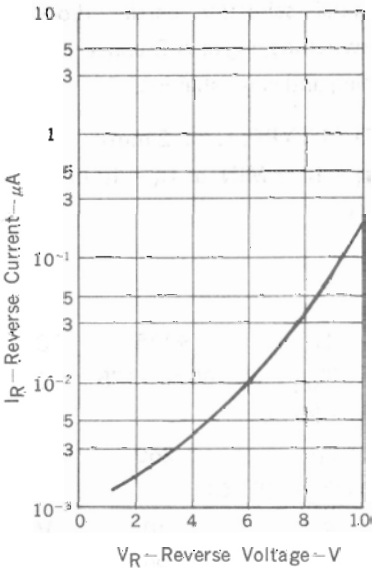
Note** : Difference of V_F, C_t

TYPICAL CHARACTERISTICS (T_a = 25 °C)

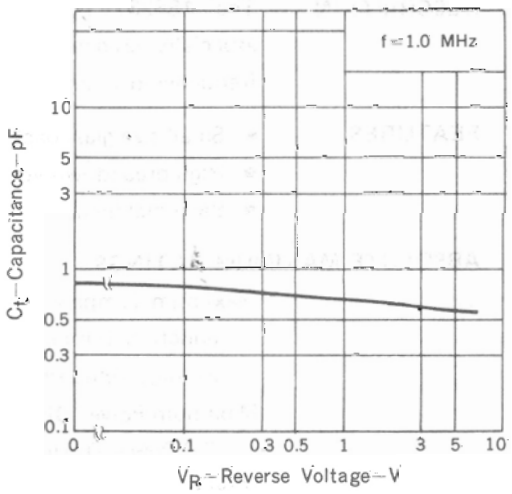
FORWARD CURRENT vs. FORWARD VOLTAGE



REVERSE CURRENT vs. REVERSE VOLTAGE



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



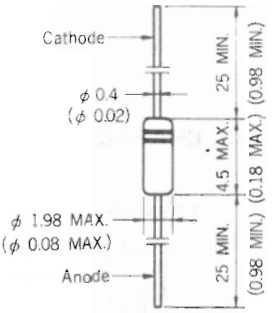
NEC
ELECTRON DEVICE

SILICON PIN DIODE
1SV34

DESCRIPTION The 1SV34 silicon PIN diode, especially designed for VHF/UHF band switching, attenuating.

The RF resistance of a PIN diode is a function of the current flowing in the diode. The current controlled resistars are specified for use in control applications such as ATT, AGC, and RF modulators.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code (from cathode)
Red, Green

FEATURES

- Low cost
- Large dynamic range.
  Typical resistance swing 5 Ω to 10 kΩ.
- Low series resistance.
  Rs=8 Ω TYP. @ I_F=10 mA, f=100 MHz
- Low capacitance.
  Ct=0.5 pF MAX. @ V_R=50 V, f=1 MHz

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Solder Temperature (Note)		260	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	250	mW
Maximum Voltages and Currents (Ta=25 °C)			
Peak Reverse Voltage	V_{RM}	110	V
Reverse Voltage	V_R	100	V
Peak Forward Current (1 μs)	I_{FM}	150	mA
Forward Current	I_F	50	mA

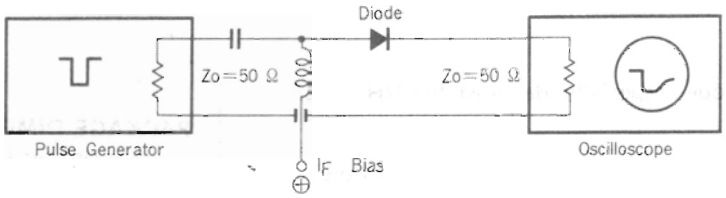
Note : Less than 5 seconds, more than 1.5 mm off the lead connection.

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

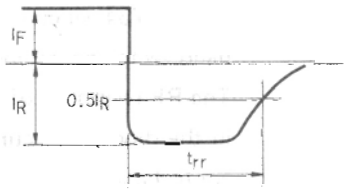
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.95	1.1	V	I_F=50 mA
I_R	Reverse Current			10	μA	V_R=100 V
Ct	Capacitance		0.3	0.5	pF	V_R=50 V, f=1.0 MHz
R_{ds}	Series Resistance	6.0	8.0	10	Ω	I_F=10 mA, f=100 MHz
R_{dp}	Parallel Resistance	2.0	2.5		kΩ	I_F=10 μA, f=100 MHz
τ	Life Time		2.0		μs	I_F=10 mA
trr	Recovery Time		1.0		μs	I_F=10 mA, I_R=16 mA*

*See measurement block diagram.

*MEASUREMENT BLOCK DIAGRAM

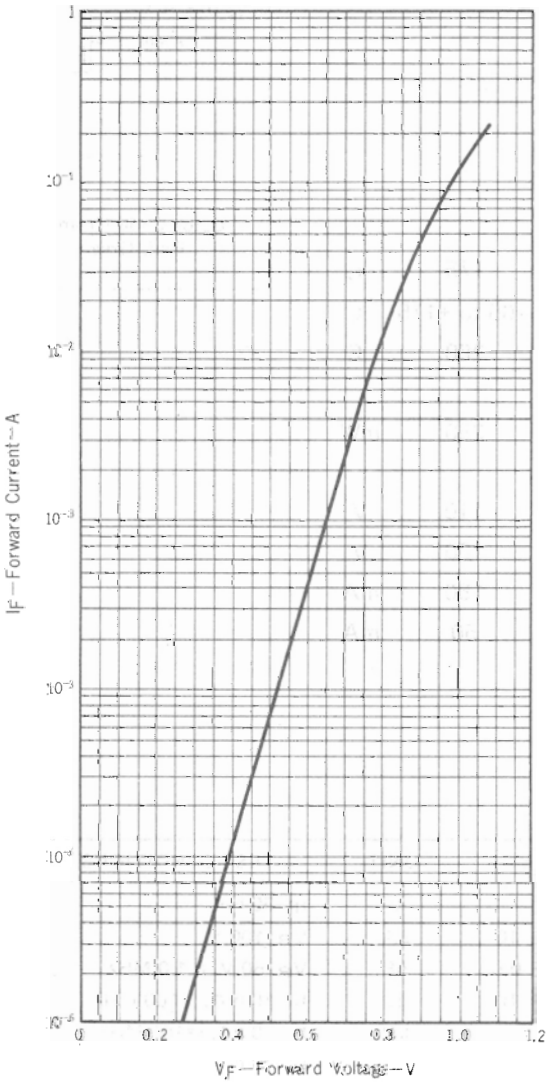


Oscilloscope Wave form

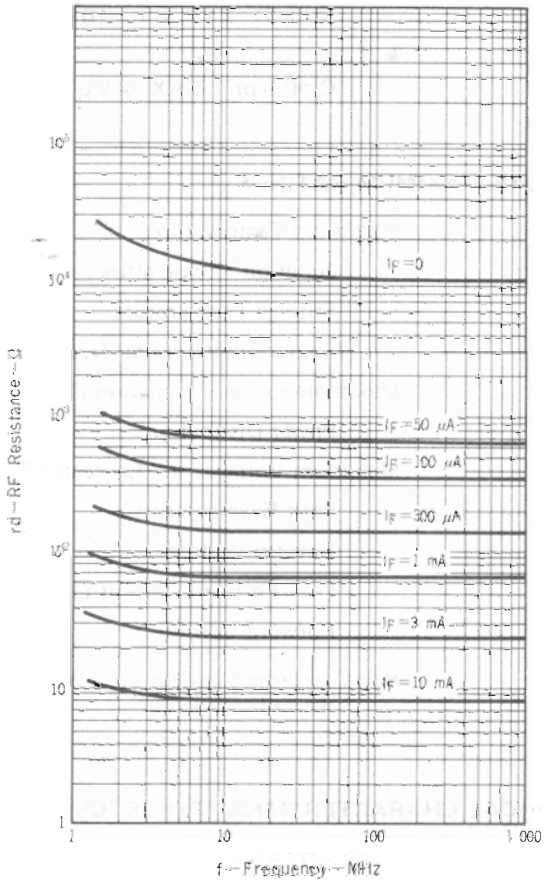


TYPICAL CHARACTERISTICS (Ta = 25 °C)

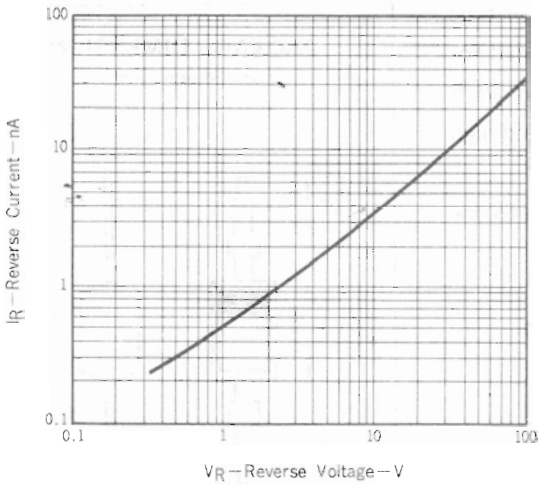
FORWARD CURRENT vs. FORWARD VOLTAGE



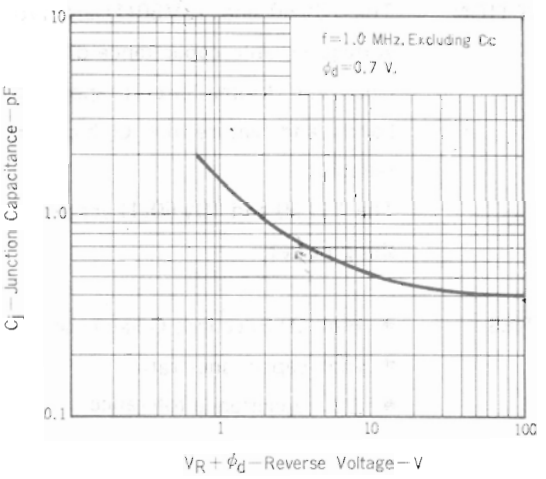
RF RESISTANCE vs. FREQUENCY



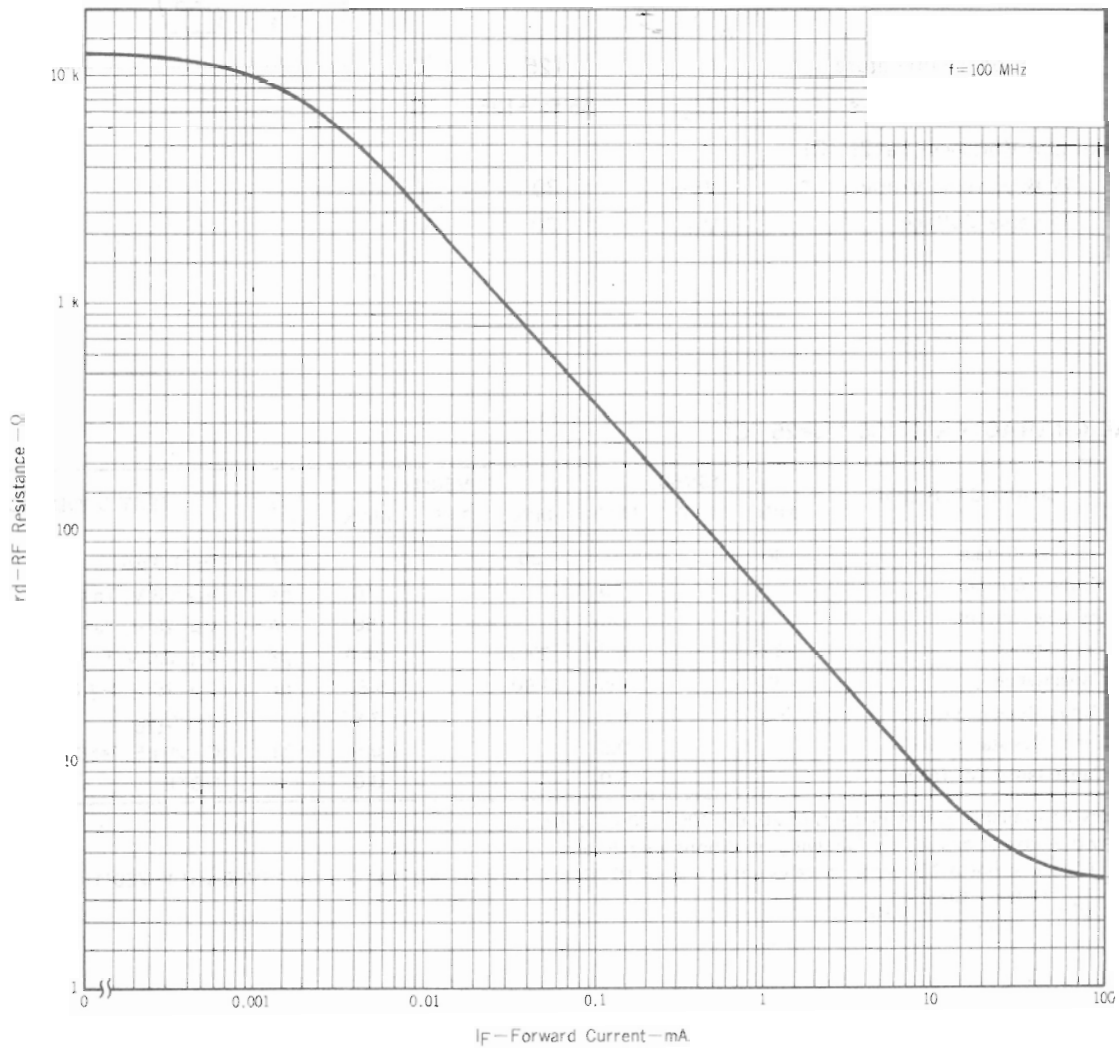
REVERSE CURRENT vs. REVERSE VOLTAGE



JUNCTION CAPACITANCE vs. REVERSE VOLTAGE



RF RESISTANCE vs. FORWARD CURRENT



NEC
ELECTRON DEVICE

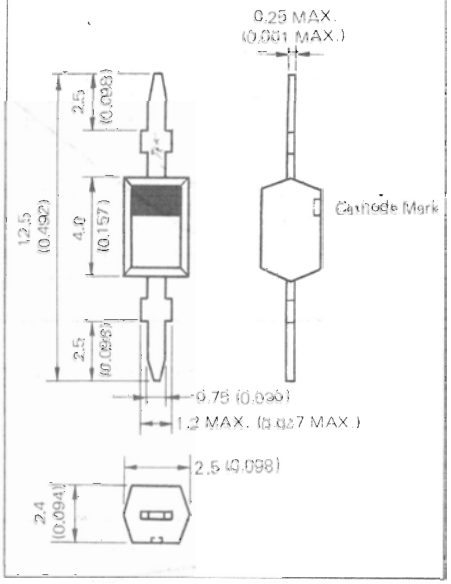
SILICON VARACTOR DIODES
1SV50, 1SV50(1)

DESCRIPTION

The 1SV50 and 1SV50(1) are hyper-abrupt junction type voltage-variable capacitance diodes. These are designed for electronic tuning circuit applications for FM and VHF bands, and feature high Q, high capacitance ratio, and high reliability.

The 1SV50 and 1SV50(1) are provided by four units as one shipping set.

PACKAGE DIMENSIONS
in millimeters (inches)



FEATURES

- High Q: Excellent Q values at FM and VHF bands.
- High capacitance ratio.
- 3 % capacitance tolerance.
- Low leakage current.
  $I_R \leq 10$ nA at V_R=28 V.

ABSOUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Maximum Voltages (Ta=25 °C)			
Peak Reverse Voltage	V_{RM}	30	V
Reverse Voltage	V_R	30	V

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

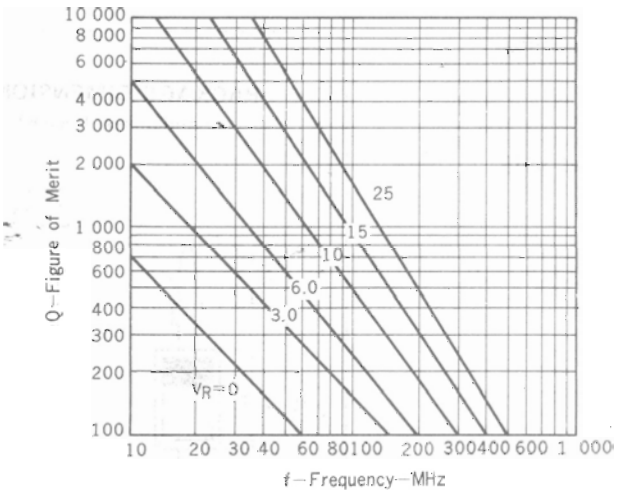
SYMBOL	CHARACTERISTIC	1SV50			1SV50(1)			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_R	Reverse Voltage	30			30			V	I_R=1.0 μA
I_{R1}	Reverse Current			10			10	nA	V_R=28 V, Ta=25 °C
I_{R2}	Reverse Current			50			50	nA	V_R=28 V, Ta=70 °C
C_{t3}	Capacitance	28.0		32.5	29.0		34.0	pF	V_R=3.0 V, f=1.0 MHz
C_{t25}	Capacitance	4.90		5.80	4.90		5.80	pF	V_R=25 V, f=1.0 MHz
N	Capacitance Ratio	5.0		6.5	5.5		7.5		C_{t3}/C_{t25}
r_s	Series Resistance			0.5			0.5	Ω	C_t=29 pF, f=50 MHz
ΔC	Capacitance Tolerance			3.0			3.0	%	NOTE

NOTE : Diodes are available in matched sets of 20, 60, 120, 120 x n units.
For two diodes of one set the following conditions are relevant :
The variations ΔC in capacitance values at V_R=3, 10, 18 and 25 V are less than 3 % for 1SV50 and 1SV50(1).

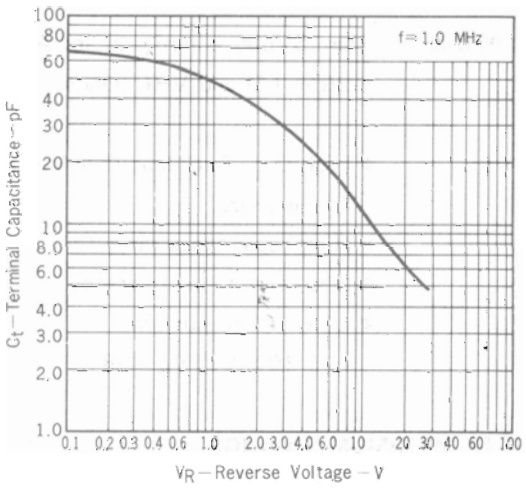
$$\Delta C = \frac{C_{max.} - C_{min.}}{C_{min.}} \times 100\ (\%)$$

TYPICAL CHARACTERISTICS (Ta =25 °C)

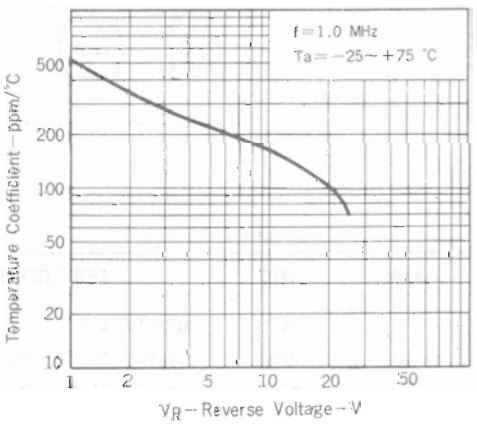
FIGURE OF MERIT vs. FREQUENCY



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



TEMPERATURE COEFFICIENT vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

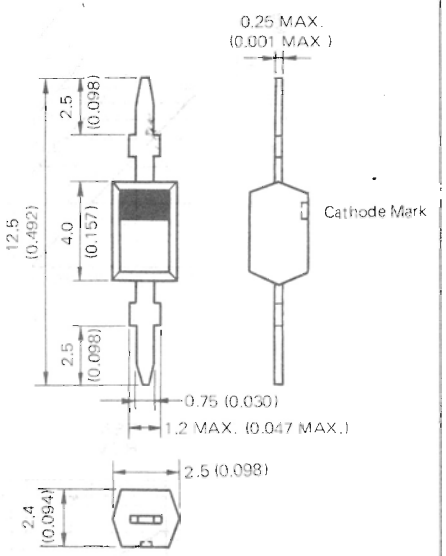
VARACTOR DIODE
1SV50S

DESCRIPTION The 1SV50S is designed for AFC circuit applications in FM and VHF bands.

FEATURES

- High Q : Excellent Q values at FM and VHF frequencies.
- High capacitance ratio.
- 3 % capacitance tolerance.
- Low leakage current.
  $I_R \leqq 10$ nA at $V_R = 28$ V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Maximum Voltages (Ta = 25 °C)			
Peak Reverse Voltage	V_{RM}	30	V
Reverse Voltage	V_R	30	V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	30			V	$I_R = 1.0\ \mu A$
I_{R1}	Reverse Current			10	nA	$V_R = 28$ V, Ta = 25 °C
I_{R2}	Reverse Current			50	nA	$V_R = 28$ V, Ta = 70 °C
C_{t3}	Capacitance	23.0		36.0	pF	f = 1.0 MHz, $V_R = 3.0$ V
C_{t6}	Capacitance	14.0		22.0	pF	f = 1.0 MHz, $V_R = 6.0$ V
N	Capacitance Ratio	1.3		2.1		C_{t3} / C_{t6}
r_s	Series Resistance			0.5	Ω	C = 30 pF, f = 50 MHz

TYPICAL CHARACTERISTICS (Ta = 25 °C)

TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

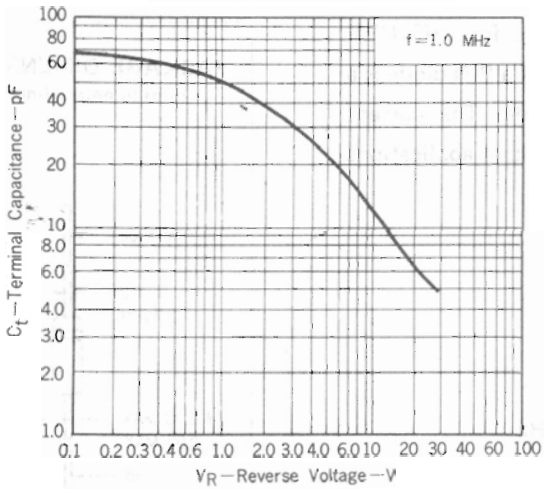
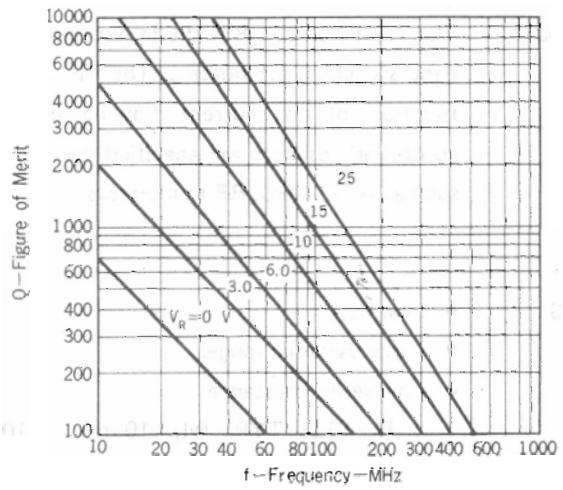
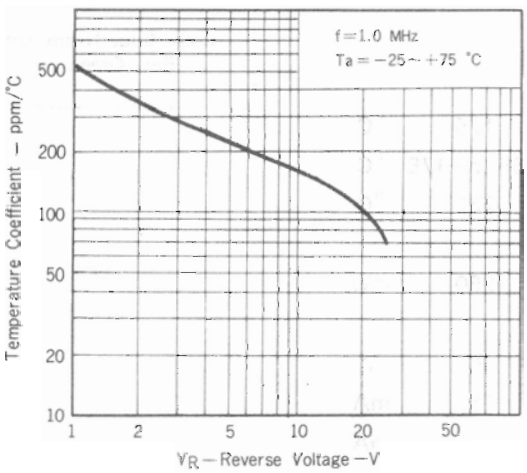


FIGURE OF MERIT vs. FREQUENCY



TEMPERATURE COEFFICIENT vs. REVERSE VOLTAGE



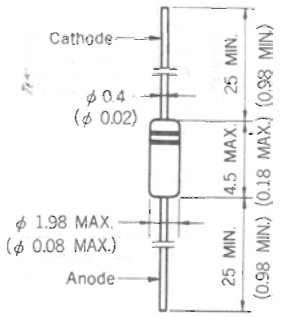
NEC
ELECTRON DEVICE

SILICON PIN DIODE
1SV80

DESCRIPTION

The 1SV80 silicon PIN diode, especially designed for VHF/UHF band switching attenuating. The RF resistance of a PIN diode is a function of the current flowing in the diode. The current controlled resistors are specified for use in control applications such as ATT, AGC, RF modulators.

PACKAGE DIMENSIONS
in millimeters (inches)



Color Code (from cathode)
Red, Green

FEATURES

- Low cost.
- Large dynamic range.
- Low series resistance.
  R_s=10 Ω TYP. @I_F=10 mA, f=100 MHz
- Low capacitance
  C_t=0.5 pF MAX. @V_R=15 V, f=1 MHz

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Solder Temperature (Note)		260	°C
Maximum Power Dissipation (Ta=25 °C)			
Power Dissipation	P_T	250	mW
Maximum Voltage and Currents (Ta=25 °C)			
Reverse Voltage	V_R	30	V
Peak Forward Current (1 μs)	I_{FM}	150	mA
Forward Current	I_F	50	mA

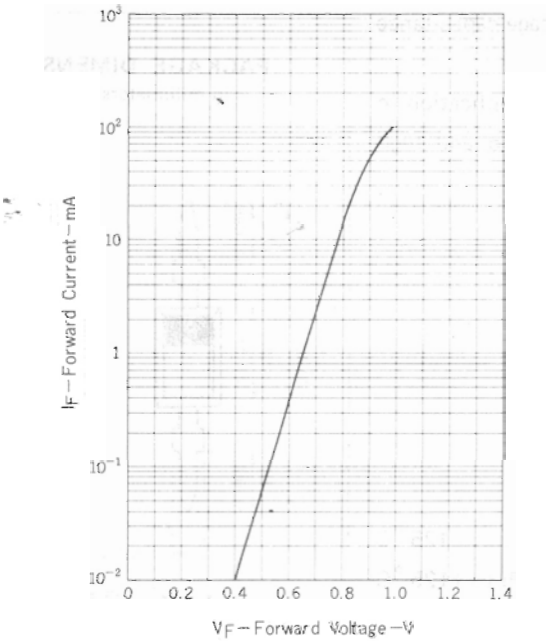
Note : Less than 5 seconds, more than 1.5 mm off the lead connection.

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

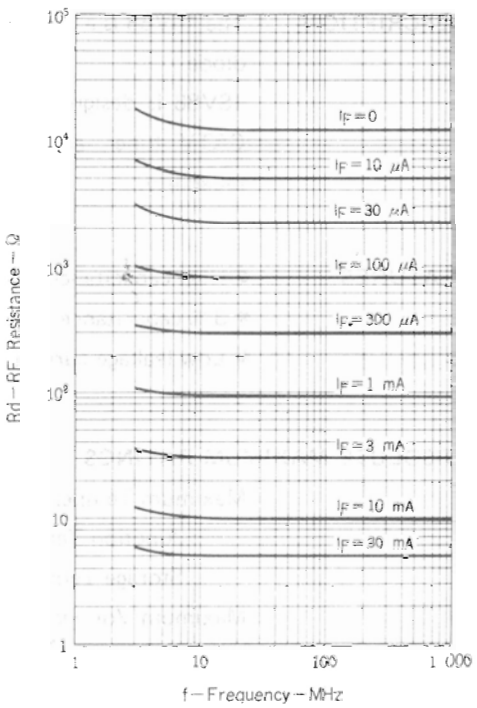
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.95	1.1	V	I_F=50 mA
V_R	Reverse Voltage	30			V	I_R=10 μA
C_t	Capacitance		0.3	0.5	pF	V_R=15 V, f=1.0 MHz
R_{ds}	Series Resistance		10	15	Ω	I_F=10 mA, f=100 MHz
R_{dp}	Parallel Resistance	1.0	3.0		kΩ	I_F=10 μA, f=100 MHz
τ	Life Time		2.0		μs	I_F=10 mA
t_{rr}	Recovery Time		1.0		μs	I_F=10 mA, I_R=6 mA

TYPICAL CHARACTERISTICS (Ta=25 °C)

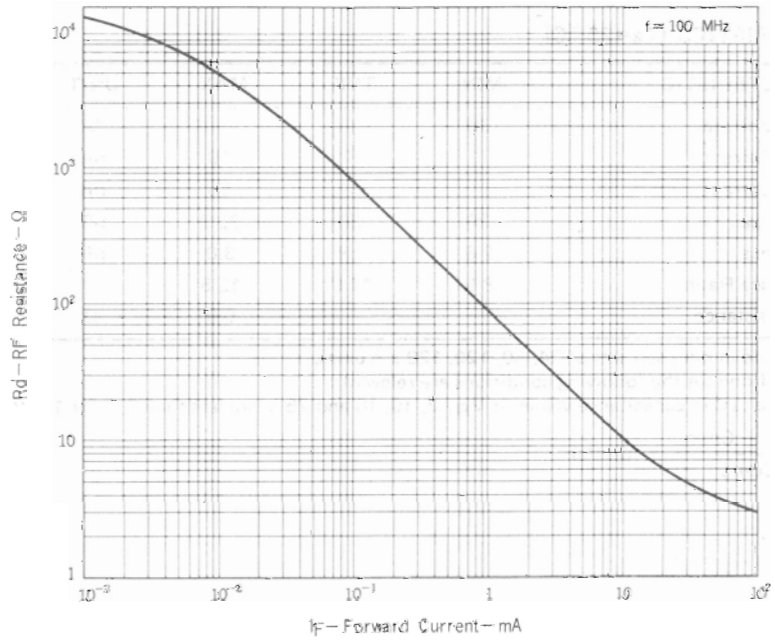
FORWARD CURRENT vs. FORWARD VOLTAGE



RF RESISTANCE vs. FREQUENCY



RF RESISTANCE vs. FORWARD CURRENT



NEC
ELECTRON DEVICE

VARACTOR DIODE
1SV88

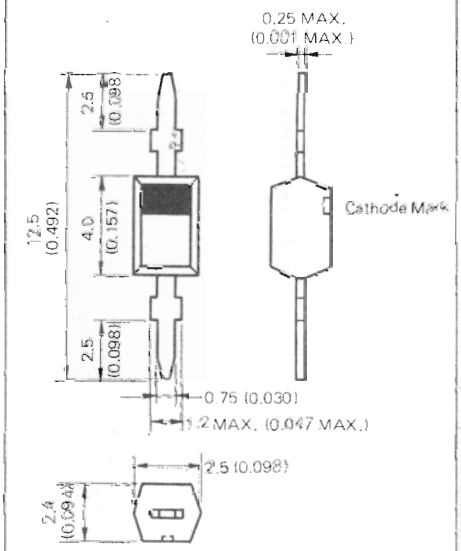
DESCRIPTION The 1SV88 is a hyper-abrupt junction type voltage capacitance diode.

1SV88 is designed for electronic tuning circuit application in CATV tuner, and features high capacitance ratio and high reliability.

FEATURES

- High capacitance ratio. N : 11 at C_3/C_{25} (TYP.)
- 3 % capacitance tolerance.
- Low leakage current. I_R = 10 pA at V_R = 28 V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature . . . . . 125 °C

Storage Temperature . . . . . −55 to +125 °C

Maximum Voltages (Ta = 25 °C)

V_{RM} Peak Reverse Voltage . . . . . 30 V

V_R Reverse Voltage . . . . . 30 V

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	30			V	I_R = 1.0 μA
I_{R1}	Reverse Current			10	nA	V_R = 28 V, Ta = 25 °C
I_{R2}	Reverse Current			50	nA	V_R = 28 V, Ta = 70 °C
C_{t3}	Capacitance	26	29	32.0	pF	V_R = 3.0 V, f = 1.0 MHz
C_{t25}	Capacitance	2.6	2.8	3.0	pF	V_R = 25 V, f = 1.0 MHz
N	Capacitance Ratio	8.5	11.0	12.5		C_{t3}/C_{t25}
r_s	Series Resistance			0.9	Ω	C = 9.0 pF, f = 50 MHz

NOTE : Diodes are available in matched sets of 24, 60, 120, 120 x n units.
For two diodes of one set the following conditions are relevant :
The variations ΔC in capacitance values at V_R = 3, 10, 18 and 25 V are less than 3 % for 1SV88.

$$\Delta C = \frac{C_{max.} - C_{min.}}{C_{min.}} \times 100\ (\%)$$

TYPICAL CHARACTERISTICS (Ta=25 °C)

TERMINAL CAPACITANCE vs. REVERSE VOLTAGE

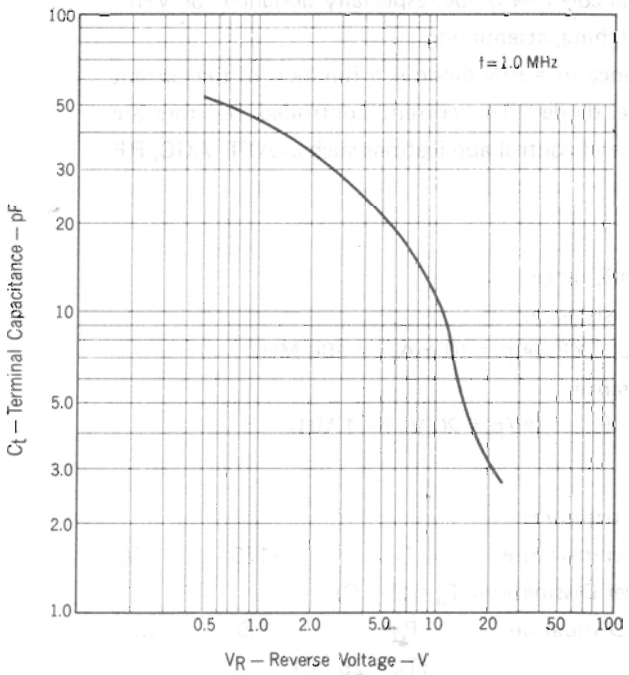
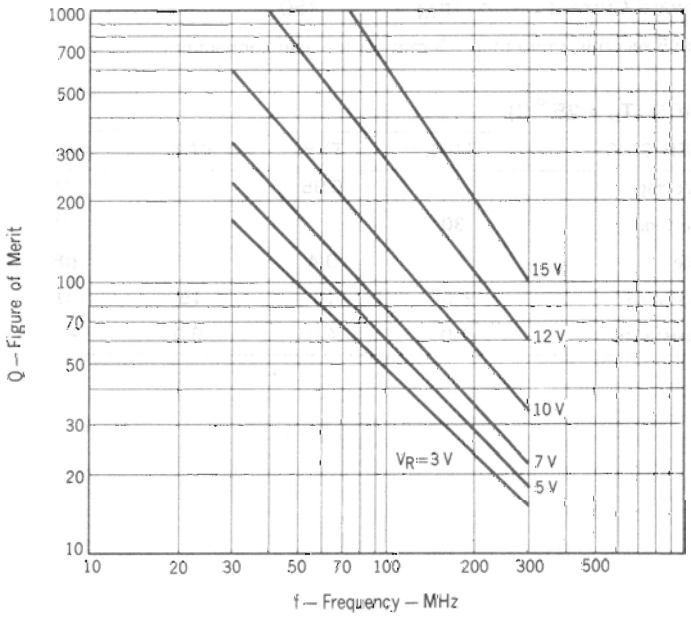


FIGURE OF MERIT vs. FREQUENCY



NEC
ELECTRON DEVICE

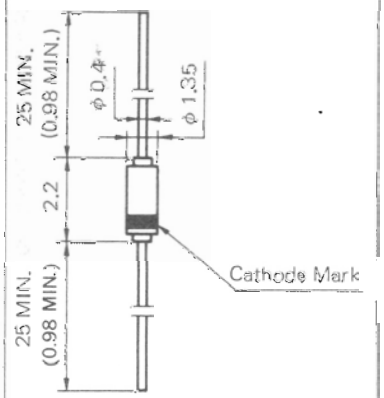
PIN DIODE
1SV156

DESCRIPTION

The 1SV156 silicon PIN diode, especially designed for VHF/UHF band switching, attenuating.

The RF resistance of a PIN diode is a function of the current flowing in the diode. The current controlled resistors are specified for use in control applications such as ATT, AGC, RF modulations.

PACKAGE DIMENSIONS
in millimeters (inches)



FEATURES

- Low cost.
- Large dynamic range.
- Low series resistance.
  R_s = 10 Ω TYP. @I_F = 10 mA, f = 100 MHz
- Low capacitance.
  C_t = 0.4 pF @V_R = 20 V, f = 1 MHz

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	+175	°C
Maximum Power Dissipation (T_a = 25 °C)			
DC Power Dissipation	P_d	250	mW
Maximum Voltages and Currents (T_a = 25 °C)			
Reverse Voltage	V_R	30	V
Forward Current	I_F	50	mA
Peak Forward Current	I_{FM}	150	mA

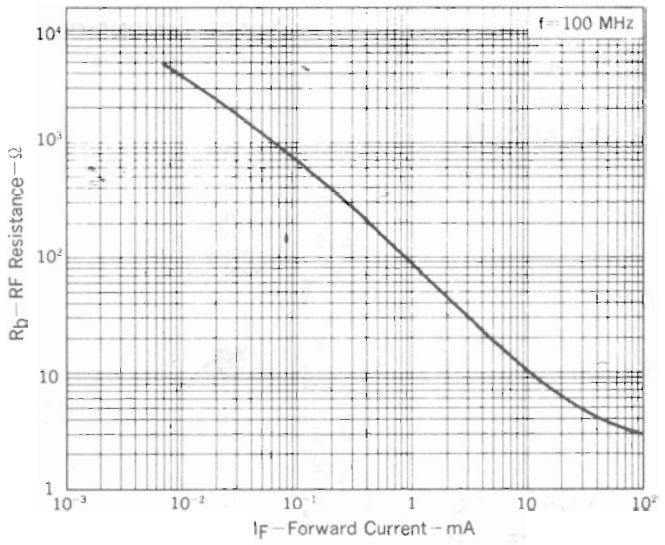
Note : Less than 5 seconds, more than 1.5 mm off the lead connection.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

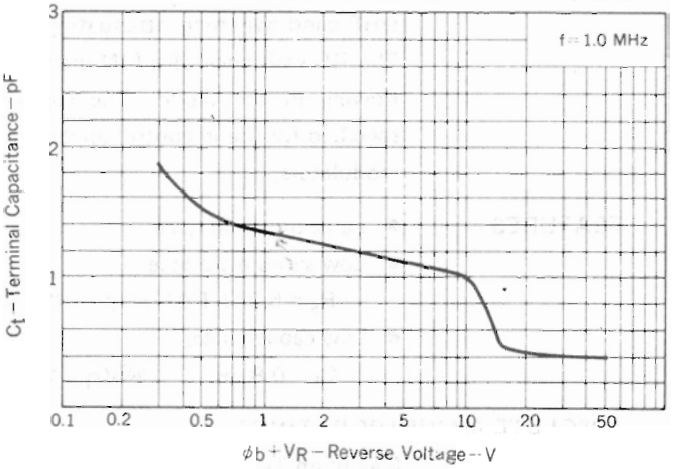
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.95		V	I_F=50 mA
V_R	Reverse Voltage	30			V	I_R=10 μA
C_t	Capacitance		0.4		pF	V_R=20 V, f=1.0 MHz
r_{ds}	Series Resistance	6.0	10	15	Ω	I_F=10 mA, f=100 MHz
r_{dp}	Parallel Resistance	1.0	4.0	6.0	kΩ	I_F=10 μA, f=100 MHz

TYPICAL CHARACTERISTICS (T_a = 25 °C)

RF RESISTANCE vs. FORWARD CURRENT



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

PIN DIODE
1SV157

DESCRIPTION

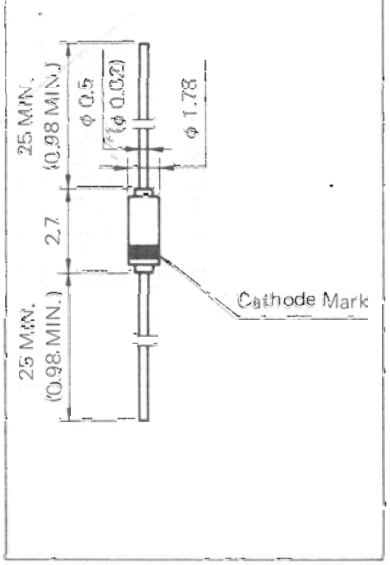
The 1SV157 silicon PIN diode, especially designed for VHF/UHF band switching, attenuating.

The RF resistance of a PIN diode is a function of the current flowing in the diode. The current controlled resistors are specified for use in control applications such as ATT, AGC, RF modulators.

FEATURES

- Large dynamic range.
- Low series resistance.
  R_s = 5.0 Ω TYP. @ I_F = 10 mA, f = 100 MHz
- Low capacitance.
  C_t = 0.8 pF @ V_R = 20 V, f = 1 MHz

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	+175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Solder Temperature (Note)		260	°C
Maximum Power Dissipation (T_a = 25 C)			
DC Power Dissipation	P_d	250	mW
Maximum Voltages and Currents (T_a = 25 °C)			
Reverse Voltage	V_R	50	V
Forward Current	I_F	50	mA
Peak Forward Current	I_{FM}	150	mA

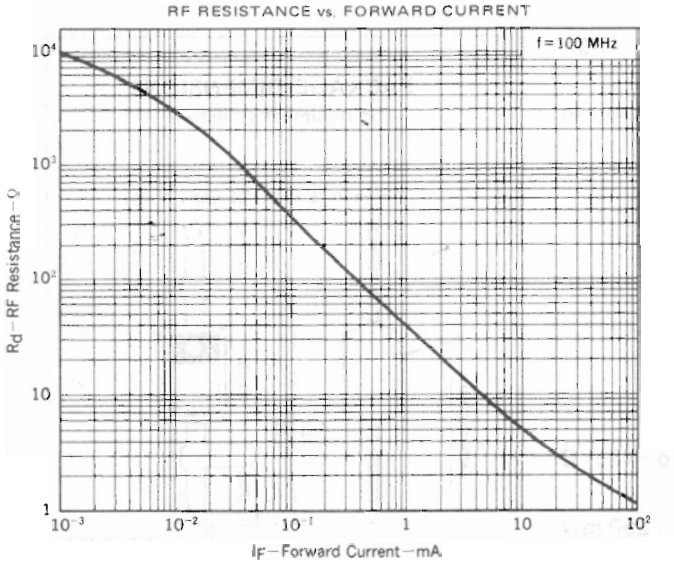
Note : Less than 5 seconds, more than 1.5 mm off the lead connection.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

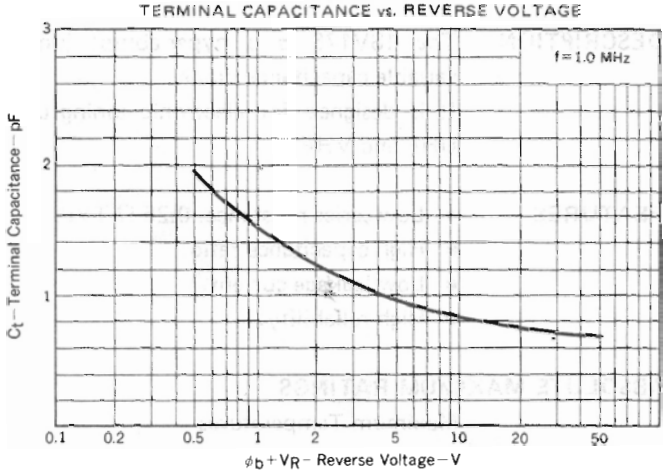
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_F	Forward Voltage		0.85		V	I_F=50 mA
V_R	Reverse Voltage	50			V	I_R=10 μA
C_t	Capacitance		0.8		pF	V_R=20 V, f=1.0 MHz
r_{ds}	Series Resistance	3.0	5.0	7.0	Ω	I_F=10 mA, f=100 MHz
r_{dp}	Parallel Resistance	1.0	3.0	5.0	kΩ	I_F=10 μA, f=100 MHz

TYPICAL CHARACTERISTICS (Ta = 25 °C)

RF RESISTANCE vs. FORWARD CURRENT



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

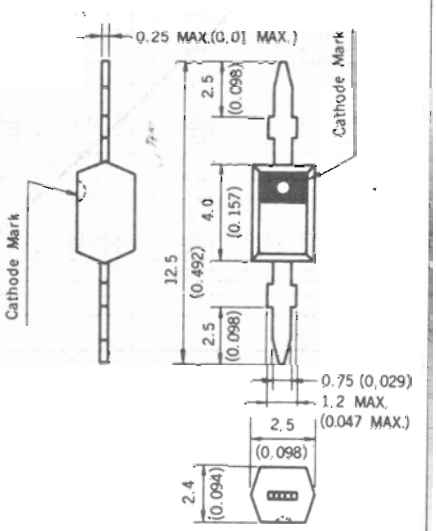
VARACTOR DIODE
1SV175

DESCRIPTION The 1SV175 is a hyper-abrupt junction type voltage-variable capacitance diode.
It is designed for electronic tuning circuit application in UHF and VHF.

FEATURES

- Low series resistance. 0.25 Ω TYP.
- High capacitance ratio.
- Low leakage current.
- High reliability.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages (T_a = 25 °C)

Peak Reverse Voltage	V_{RM} (NOTE1)	35	V
DC Reverse Voltage	V_R	30	V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{R1}	Reverse Current			10	nA	V_R = 30 V
I_{R2}	Reverse Current			50	nA	V_R = 30 V, T_a = 70 °C
V_R	Reverse Voltage	30			V	I_R = 1.0 μA
C_{t2}	Capacitance	14.00		16.35	pF	V_R = 2.0 V, f = 1.0 MHz
C_{t25}	Capacitance	2.10		2.45	pF	V_R = 25 V, f = 1.0 MHz
N	Capacitance Ratio	6.00		8.00		C_{t2}/C_{t25}
r_s	Series Resistance		0.25	0.5	Ω	f = 1.0 MHz, C_t = 9 pF
ΔC	Capacitance Tolerance			3.0	%	NOTE 2

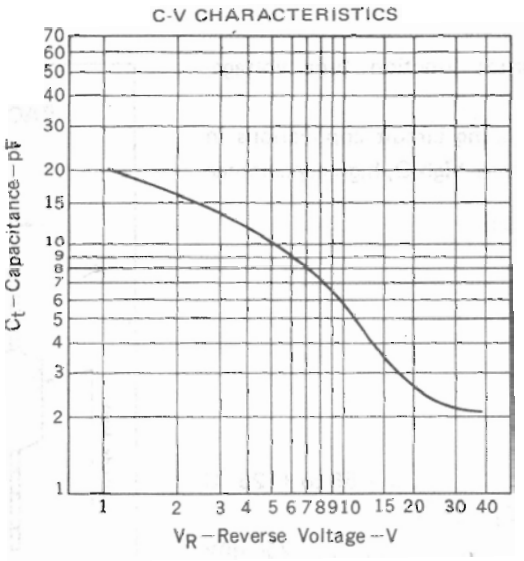
NOTE 1: When it is used with 10 kΩ series resistance.

NOTE 2: Diodes are available in matched sets of 24, 60, 120, 120 x n units.
For two diodes of one set, the following conditions are relevant:
The variations ΔC in capacitance values at V_R = 2, 10, 18 and 25 V are less than 3 % for 1SV175

$$\Delta C = \frac{C_{max.} - C_{min.}}{C_{min.}} \times 100\ (\%)$$

NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)



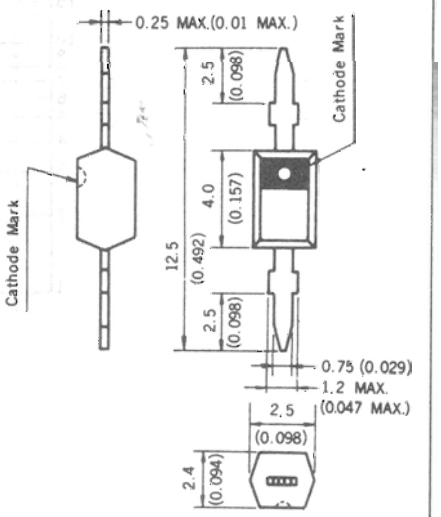
NEC
ELECTRON DEVICE

VARACTOR DIODE
1SV176

DESCRIPTION The 1SV176 is a hyper-abrupt junction type voltage-variable capacitance diode.
It is designed for electronic tuning circuit applications in VHF and UHF bands and features high Q, high capacitance ratio and high reliability.

FEATURES
- High Q.
- High capacitance ratio.
- Low leakage current.

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature . . . . . −55 to +125 °C

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages (T_a = 25 °C)

Peak Reverse Voltage	V_{RM} (NOTE)	35	V
DC Reverse Voltage	V_R	30	V

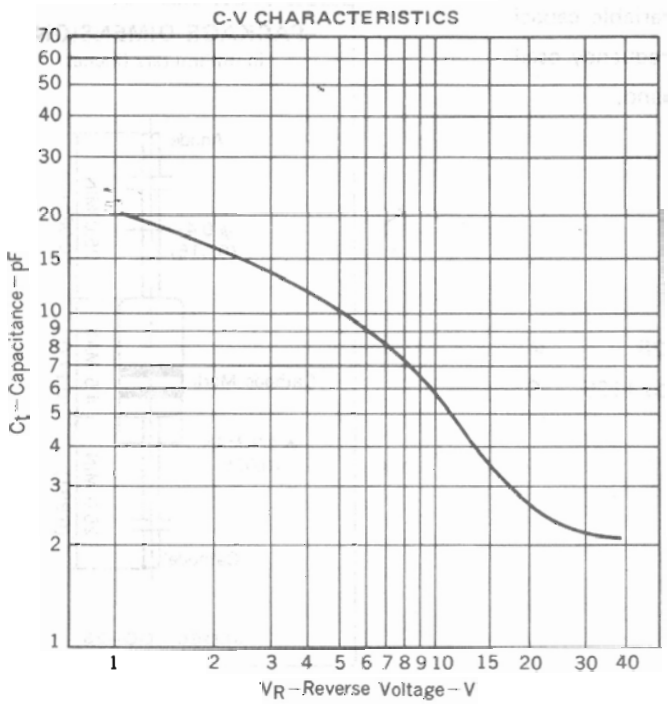
NOTE: V_{RM} is the case that Diode has series protected resistance that is more than 10 kΩ.

NEW DEVICE

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	30			V	I_R = 1.0 μA
C_{t2}	Capacitance	13.65		17.00	pF	V_R = 2.0 V, f = 1.0 MHz
C_{t10}	Capacitance	4.95		6.3	pF	V_R = 10 V, f = 1.0 MHz
N	Capacitance Ratio	2.5		3.5		C_{t2}/C_{t10}
r_s	Series Resistance			0.6	Ω	C_t = 9.0 pF, f = 50 MHz

TYPICAL CHARACTERISTICS (T_a = 25 °C)



NEC
ELECTRON DEVICE

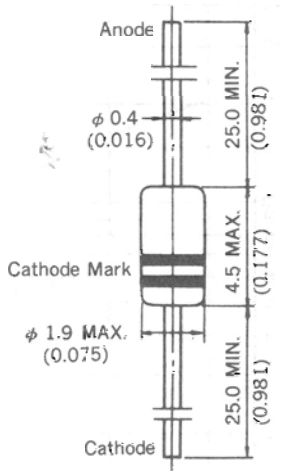
VARACTOR DIODE
1SV183

DESCRIPTION 1SV183 is a hyper-abrupt junction type variable capacitance diode which is designed for variable frequency oscillator and tunable filter applications in UHF band.

FEATURES

- High quality value.
- High capacitance ratio.

PACKAGE DIMENSIONS
in millimeters (inches)



JEDEC : DO–35

ABSOLUTE MAXIMUM RATINGS

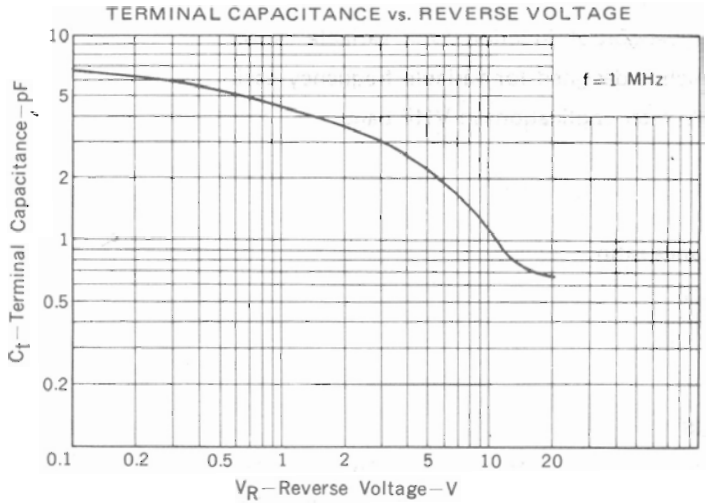
Reverse Voltage	V_R	28	V
Storage Temperature	T_{stg}	−55 to +125	°C

NEW DEVICE

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	28			V	I_R = 10 μA
C_{t2}	Capacitance	3.2		4.0	pF	V_R = 2 V, f = 1 MHz
C_{t10}	Capacitance	0.75		1.9	pF	V_R = 10 V, f = 1 MHz
C_{t20}	Capacitance	0.58		0.73	pF	V_R = 20 V, f = 1 MHz
N	Capacitance Ratio	4.3		6.9		C_{t2}/C_{t20}
C	Capacitance Tolerance			15	%	$\frac{C_{max.} - C_{min.}}{C_{min.}} \times 100$
Q	Quality Value	150				C_t = 4 pF, f = 50 MHz

TYPICAL CHARACTERISTICS (T_a = 25 °C)



NEC
ELECTRON DEVICE

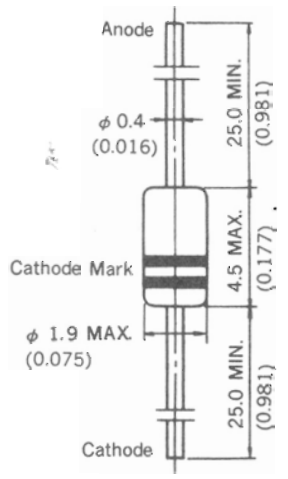
VARACTOR DIODE
1SV184

DESCRIPTION 1SV184 is a hyper-abrupt junction type variable capacitance diode which is designed for variable frequency oscillator and tunable filter applications in VHF band.

FEATURES

- High capacitance ratio.
- Small package.

PACKAGE DIMENSIONS
in millimeters (inches)



JEDEC : DO–35

ABSOLUTE MAXIMUM RATINGS

Reverse Voltage	V_R	15	V
Storage Temperature	T_{stg}	−55 to +125	°C

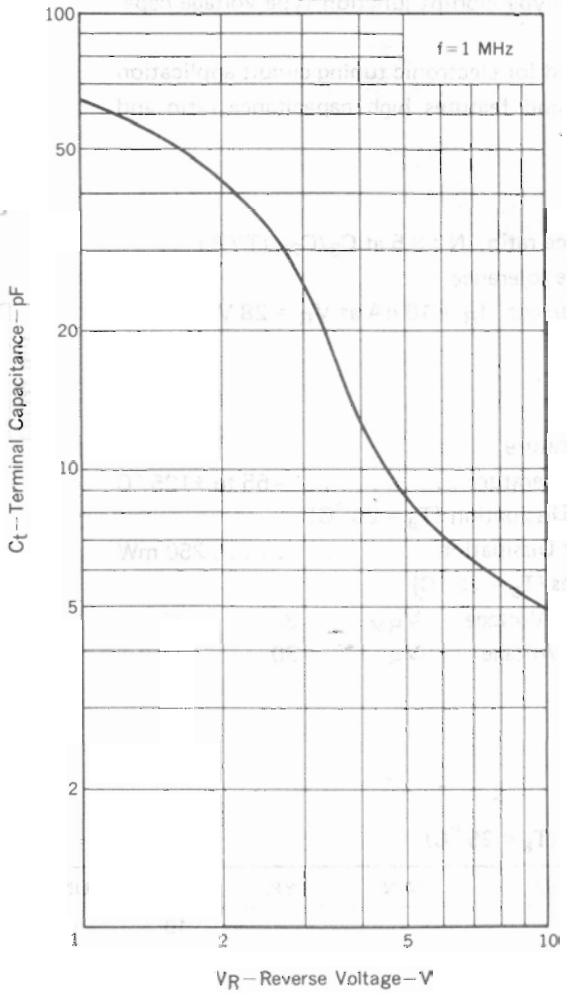
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_R	Reverse Voltage	15			V	I_R = 10 μA
C_{t2}	Capacitance	40	45	50	pF	V_R = 2 V, f = 1 MHz
C_{t5}	Capacitance	7	9	11	pF	V_R = 5 V, f = 1 MHz
C_{t10}	Capacitance	4	5	6	pF	V_R = 10 V, f = 1 MHz
N	Capacitance Ratio	6.5				C_{t2}/C_{t10}
Q	Quality Value	100				C_t = 10 pF, f = 50 MHz

NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

TERMINAL CAPACITANCE vs.
REVERSE VOLTAGE



NEC
ELECTRON DEVICE

VARACTOR DIODE
1SV190

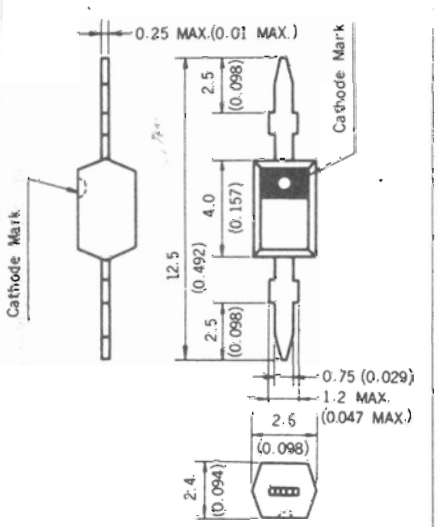
NEW DEVICE

DESCRIPTION The 1SV190 is a hyper-abrupt junction type voltage capacitance diode.
1SV190 is designed for electronic tuning circuit application in CATV tuner, and features high capacitance ratio and high reliability.

FEATURES

- High capacitance ratio. N : 8.5 at C_3/C_{25} (TYP.)
- 3 % capacitance tolerance.
- Low leakage current. I_R = 10 nA at V_R = 28 V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperature
- Storage Temperature . . . . . −55 to +125 °C

Maximum Power Dissipation (T_a = 25 °C)
- Total Power Dissipation . . . . . 250 mW

Maximum Voltages (T_a = 25 °C)

Peak Reverse Voltage	V_{RM}	30	V
DC Reverse Voltage	V_R	30	V

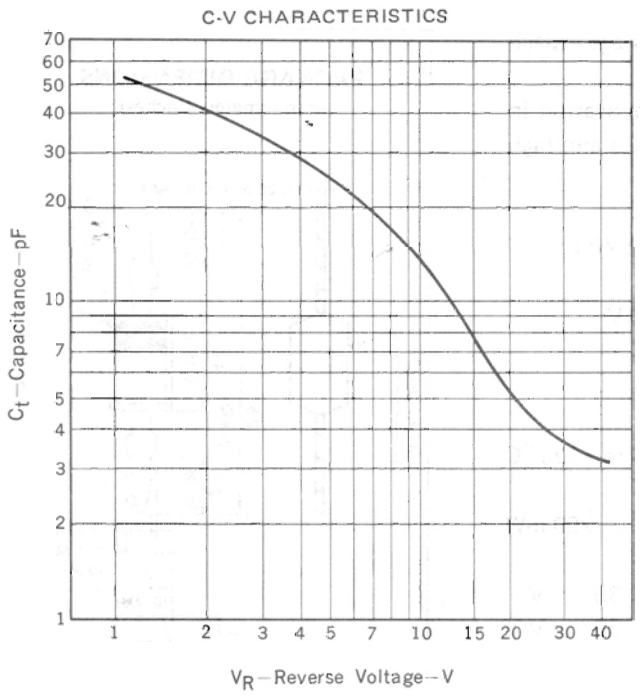
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{R1}	Reverse Current			10	nA	V_R = 28 V
I_{R2}	Reverse Current			50	nA	V_R = 28 V, T_a = 80 °C
V_R	Reverse Voltage	30			V	I_R = 1.0 μA
C_{t3}	Capacitance	31	33	35	pF	V_R = 3.0 V, f = 1.0 MHz
C_{t25}	Capacitance	3.72	4.0	4.28	pF	V_R = 25 V, f = 1.0 MHz
N	Capacitance Ratio	7.8	8.5	9.5		C_{t3}/C_{t25}
r_s	Series Resistance		0.4	0.8	Ω	f = 1.0 MHz, C_t = 9 pF
ΔC	Capacitance Tolerance			3.0	%	NOTE

NOTE: Diodes are available in matched sets of 24, 60, 120, 120 x n units.
For two diodes of one set the following conditions are relevant:
The variations ΔC in capacitance values at V_R = 3, 10, 18 and 25 V are less than 3 % for 1SV190

$$\Delta C = \frac{C_{max.} - C_{min.}}{C_{min.}} \times 100\ (\%)$$

TYPICAL CHARACTERISTICS (T_a = 25 °C)



NEC
ELECTRON DEVICE

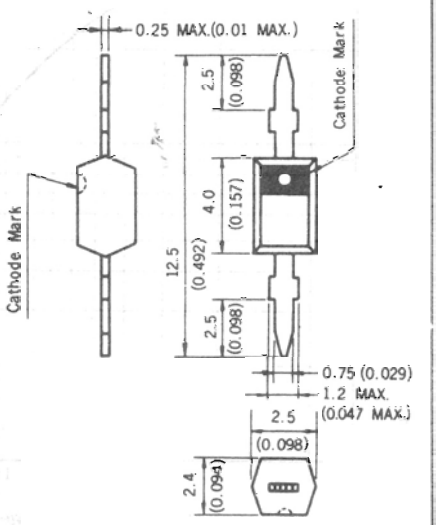
VARACTOR DIODE
1SV208

DESCRIPTION The 1SV208 is a hyper-abrupt junction type voltage capacitance diode.
It is designed for electronic tuning circuit application in CATV tuner, and features high capacitance ratio and high reliability.

FEATURES

- High capacitance ratio. N : 11.0 at C_2/C_{25} (TYP.)
- 3 % capacitance tolerance.
- Low leakage current. I_R = 10 nA at V_R = 30 V

PACKAGE DIMENSIONS
in millimeters (inches)



ABSOLUTE MAXIMUM RATINGS

Maximum Temperature
Storage Temperature . . . . . −55 to +125 °C
Maximum Power Dissipation (T_a = 25 °C)
Total Power Dissipation . . . . . 250 mW
Maximum Voltages (T_a = 25 °C)

Peak Reverse Voltage	V_{RM} (NOTE)	35	V
DC Reverse Voltage	V_R	30	V

NOTE: V_{RM} is the case that Diode has series protected resistance that is more than 10 kΩ.

NEW DEVICE

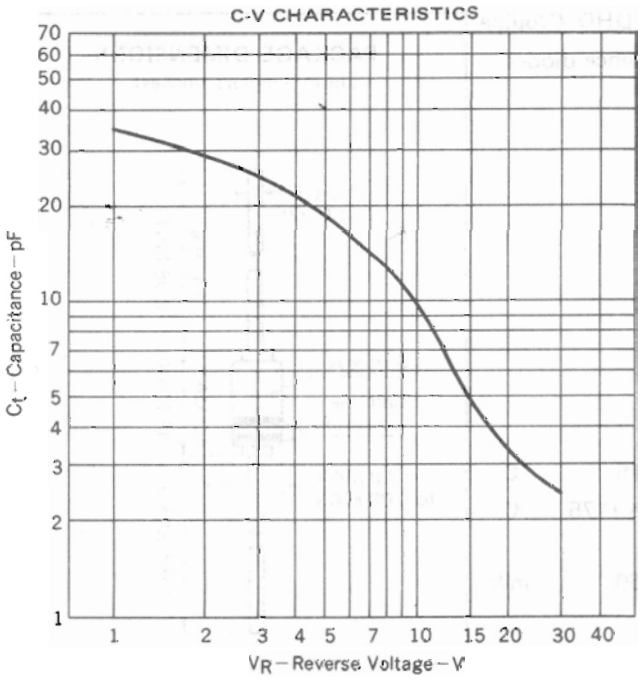
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I_{R1}	Reverse Current			10	nA	V_R = 30 V
I_{R2}	Reverse Current			50	nA	V_R = 30 V, T_a = 70 °C
V_R	Reverse Voltage	30			V	I_R = 1.0 μA
C_{t2}	Capacitance	26.6		32.03	pF	V_R = 2.0 V, f = 1.0 MHz
C_{t25}	Capacitance	2.61		3.04	pF	V_R = 25 V, f = 1.0 MHz
N	Capacitance Ratio	10.0				C_{t2}/C_{t25}
r_s	Series Resistance		0.5	0.8	Ω	f = 1.0 MHz, C_t = 9 pF
ΔC	Capacitance Tolerance			3.0	%	NOTE

NOTE: Diodes are available in matched sets of 24, 60, 120, 120 x n units.
For two diodes of one set the following conditions are relevant:
The variations ΔC in capacitance values at V_R = 2, 10, 18 and 25 V are less than 3 % for 1SV208

$$\Delta C = \frac{C_{max.} - C_{min.}}{C_{min.}} \times 100\ (\%)$$

TYPICAL CHARACTERISTICS (T_a = 25 °C)



NEC
ELECTRON DEVICE

REFERENCE DIODES

1SZ45A~1SZ47A,1SZ46,1SZ47,1SZ48

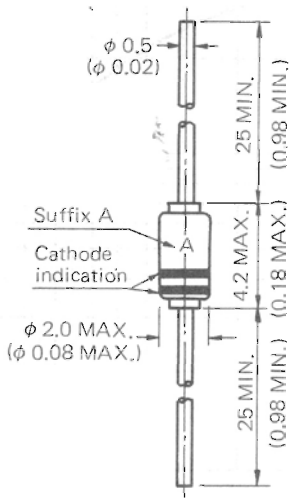
DESCRIPTION The 1SZ45A~1SZ47A, 1SZ46 and 1SZ47 are DHD (Double Heatsink Diode) construction high stability reference diodes.

FEATURES

- DHD (Double Heatsink Diode) Construction
- High Stability and High Reliability
- Low zener current (I_Z = 1 mA)
- DO-35 Glass sealed package

APLLICATIONS Circuits for, Constnat Voltage, Constant Current

PACKAGE DIMENSIONS
in millimeters (inches)



MAXIMUM RATINGS

Maximum Temperature			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation			
Power Dissipation	P	250	mW

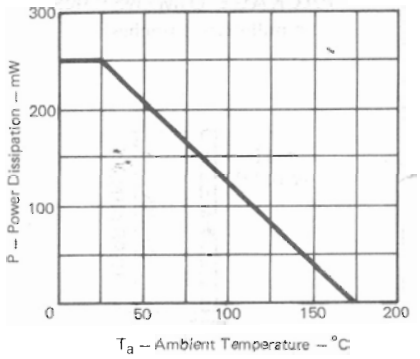
Color Code

Black	Red	Green	Blue
1SZ45A	1SZ46A	1SZ47A	—
—	—	1SZ47	1SZ48

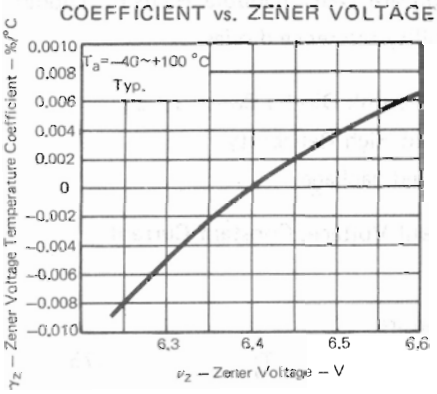
ELECTRICAL CHARACTERISTICS (T_a = 25 ±2 °C)

Type	Zener Voltage V_Z (V)		Zener Impedance Z_Z (Ω)	Zener Curent I_Z (mA)	Zener Voltage Temperature Coefficient γ_Z (%/°C)	Temperature Range T_a (°C)
	MIN.	MAX.	MAX.		MAX.	
1SZ45A	6.1	6.7	100	1	±0.01	−40~100
1SZ46A					±0.005	
1SZ47A					±0.002	
1SZ47					±0.002	−10~60
1SZ48					±0.001	

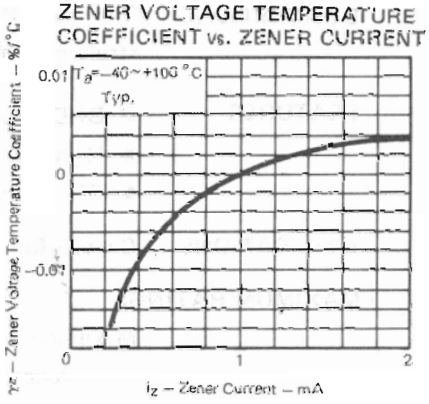
POWER DISSIPATION vs. AMBIENT TEMPERATURE



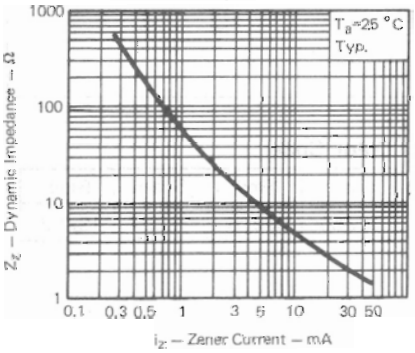
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



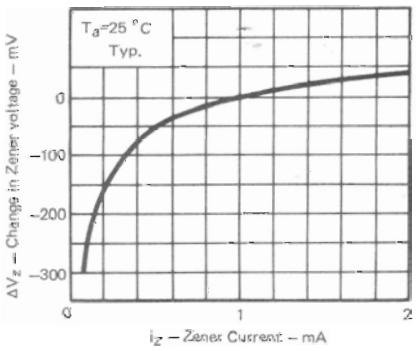
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER CURRENT



DYNAMIC IMPEDANCE vs. ZENER CURRENT



CHANGE OF ZENER VOLTAGE vs. ZENER CURRENT



NEC
ELECTRON DEVICE

REFERENCE DIODES

1SZ50~1SZ53

DESCRIPTION The 1SZ50~1SZ53 are DHD (Double Heatsink Diode) construction high stability reference diodes.

FEATURES

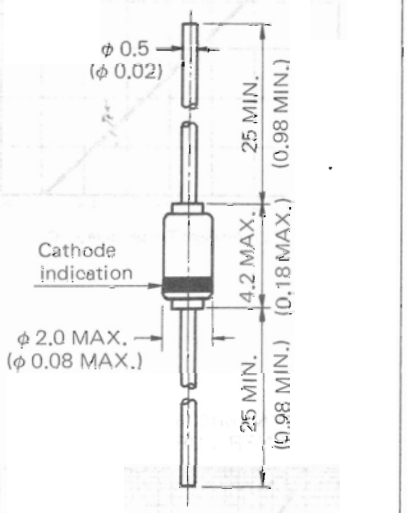
- DHD (Double Heatsink Diode) Construction
- High Stability and High Reliability
- DO-35 Glass sealed package

APPLICATIONS Circuits for, Constant Voltage, Constant Current

MAXIMUM RATINGS

Maximum Temperature			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +157	°C
Maximum Power Dissipation			
Power Dissipation	P	250	mW

PACKAGE DIMENSIONS
in millimeters (inches)



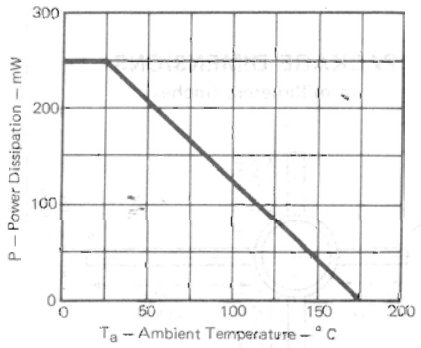
Color Code

Black	Red	Green	Blue
1SZ50	1SZ51	1SZ52	1SZ53

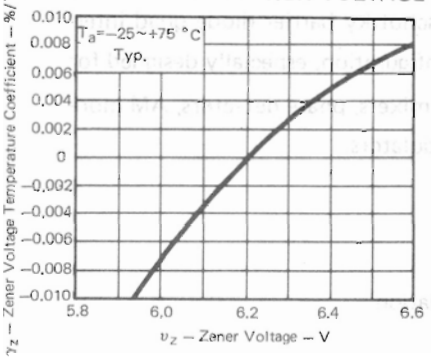
ELECTRICAL CHARACTERISTICS (T_a = 25 ±2 °C)

Type	Zener Voltage V_Z (V)		Zener Impedance Z_Z (Ω)	Zener Current I_Z (mA)	Zener Voltage Temperature Coefficient γ_Z (%/°C)	Temperature Range T_a (°C)
	MIN.	MAX.	MAX.		MAX.	
1SZ50	5.9	6.5	15	7.5	±0.01	−25~75
1SZ51					±0.005	
1SZ52					±0.002	
1SZ53					±0.001	0~75

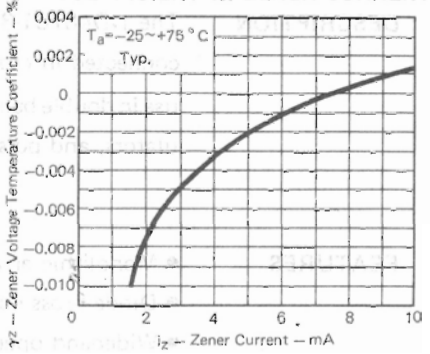
POWER DISSIPATION vs. AMBIENT TEMPERATURE



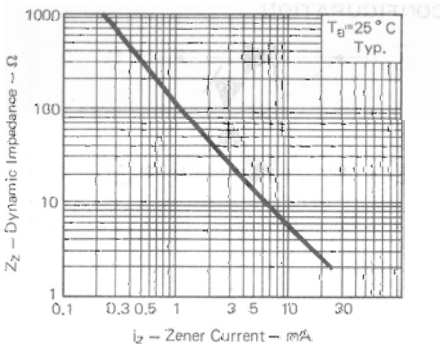
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



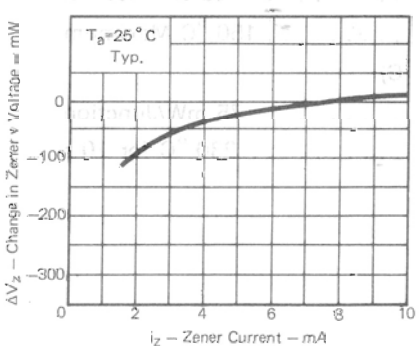
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER CURRENT



DYNAMIC IMPEDANCE vs. ZENER CURRENT



CHANGE OF ZENER VOLTAGE vs. ZENER CURRENT



NEC
ELECTRON DEVICE

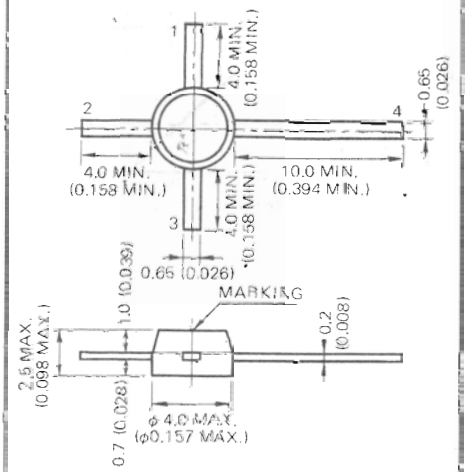
UHF MODULATOR DIODE QUAD
ND487C1-3R

DESCRIPTION The ND487C1-3R is schottky barrier diode quad interconnected in cross configuration, especially designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators.

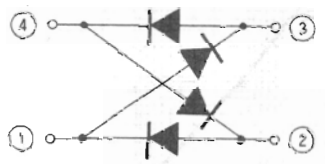
FEATURES

- Monolithic array
- Diode cross configulation
- Wideband operation
- Small size package (disk mold)
- Low cost

PACKAGE DIMENSIONS
in millimeters (inches)



CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- DC Power Dissipation . . . . . 75 mW/Junction
- Soldering Temperature . . . . . 230 °C for 10 s

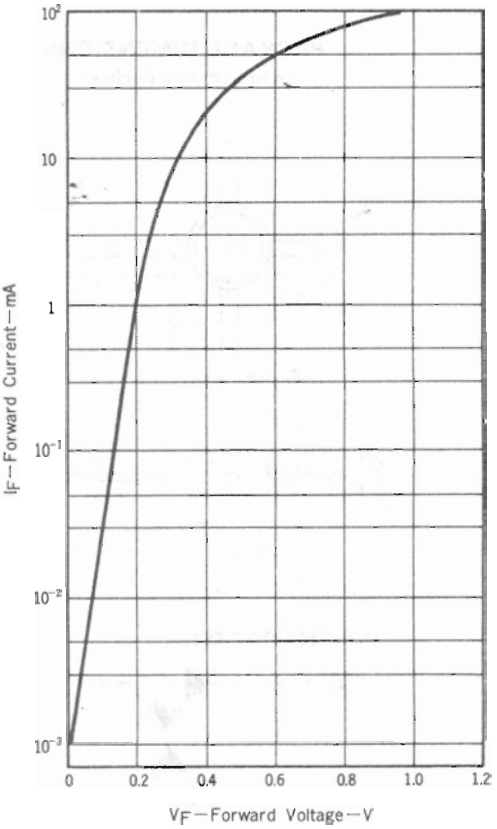
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{F1}	Forward Voltage			0.7	V	I_F = 50 mA
V_{F2}	Forward Voltage		0.2	0.3	V	I_F = 1.0 mA
ΔV_{F2} (NOTE 1)	Delta Forward Voltage			0.02	V	I_F = 1.0 mA
C_t (NOTE 2)	Terminal Capacitance		0.9	1.2	pF	V_R = 0, f = 1.0 MHz
ΔC_t (NOTE 1)	Delta Terminal Capacitance			0.2	pF	V_R = 0, f = 1.0 MHz

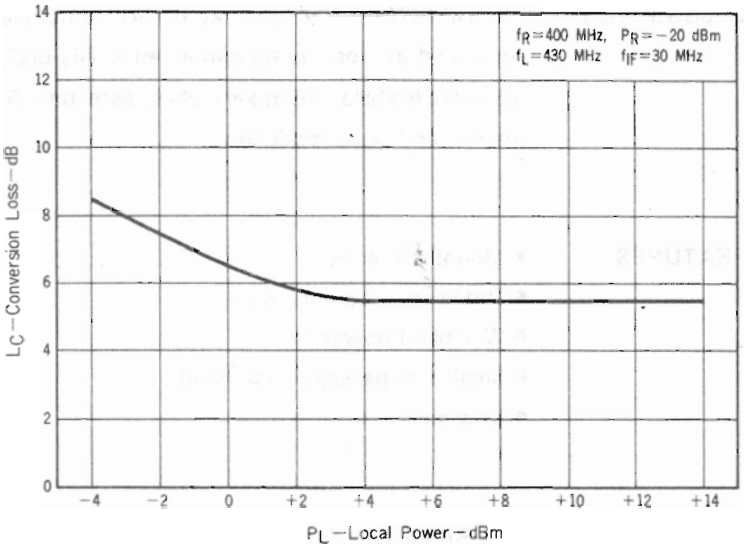
NOTE 1: Difference V_F, C_t
2: Measurement terminal ① − ④, ② − ③

TYPICAL CHARACTERISTICS (Ta = 25 °C)

FORWARD CURRENT vs.
FORWARD VOLTAGE



CONVERSION LOSS vs. LOCAL POWER



NEC
ELECTRON DEVICE

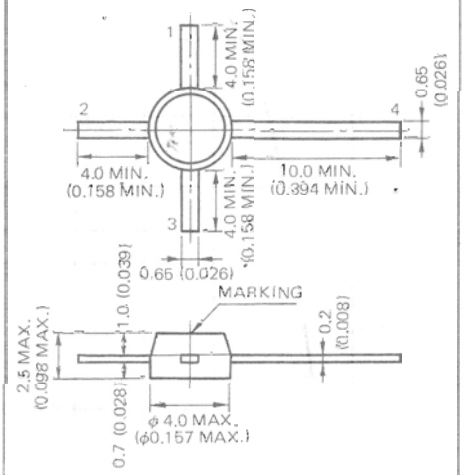
UHF MODULATOR DIODE QUAD
ND487C2-3R

DESCRIPTION The ND487C2-3R is schottky barrier diode quad interconnected in cross configuration, especially designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators.

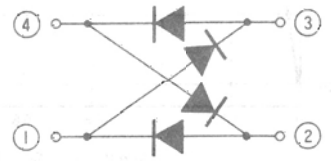
FEATURES

- Monolithic array
- Diode cross configuration
- Wideband operation
- Small size package (disk mold)
- Low cost

PACKAGE DIMENSIONS
in millimeters (inches)



CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- DC Power Dissipation . . . . . 75 mW/Junction
- Soldering Temperature . . . . . 230 °C for 10 s

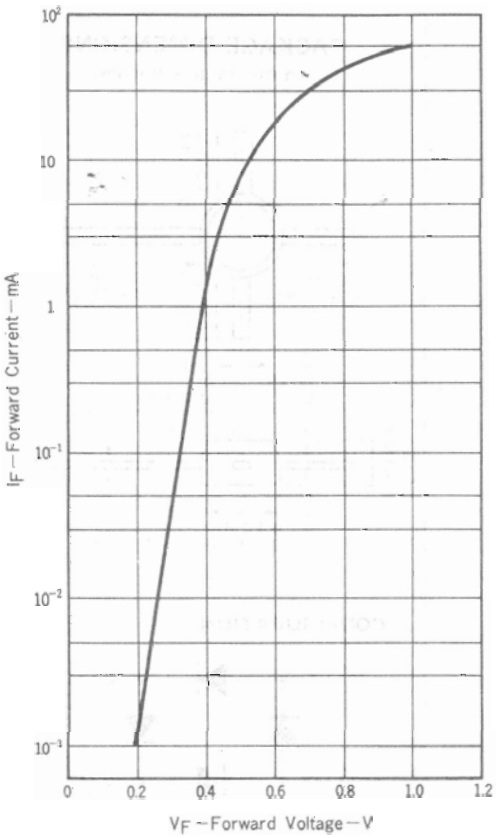
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{F1}	Forward Voltage			1.0	V	I_F = 50 mA
V_{F2}	Forward Voltage		0.4	0.5	V	I_F = 1.0 mA
ΔV_{F2} (NOTE 1)	Delta Forward Voltage			0.02	V	I_F = 1.0 mA
C_t (NOTE 2)	Terminal Capacitance		0.9	1.2	pF	V_R = 0, f = 1.0 MHz
ΔC_t (NOTE 1)	Delta Terminal Capacitance			0.2	pF	V_R = 0, f = 1.0 MHz

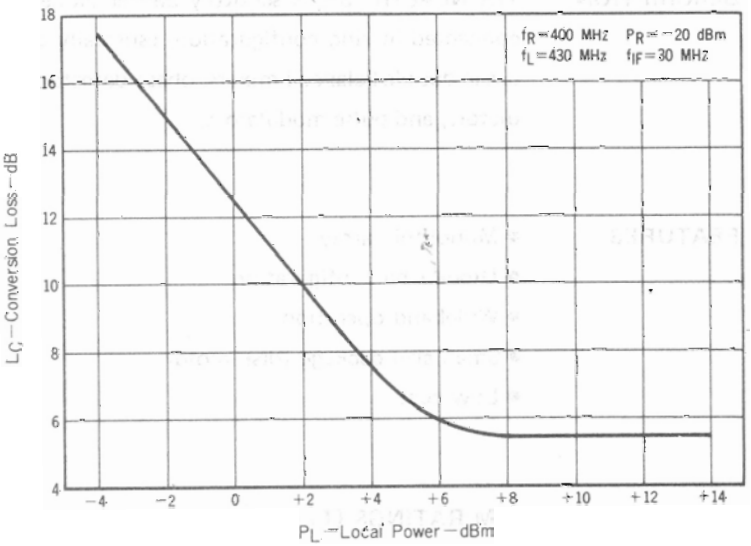
NOTE 1: Difference of V_F, C_t
2: Measurement terminal ① − ④, ② − ③

TYPICAL CHARACTERISTICS (Ta = 25 °C)

FORWARD CURRENT vs. FORWARD VOLTAGE



CONVERSION LOSS vs. LOCAL POWER



NEC
ELECTRON DEVICE

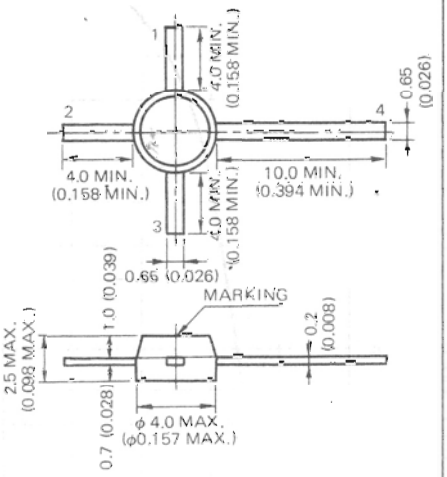
UHF MODULATOR DIODE QUAD
ND487R1-3R

DESCRIPTION The ND487R1-3R is schottky barrier diode quad interconnected in ring configuration, especially designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators,

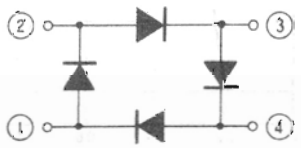
FEATURES

- Monolithic array
- Diode ring configuration
- Wideband operation
- Small size package (disk mold)
- Low cost

PACKAGE DIMENSIONS
in millimeters (inches)



CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- DC Power Dissipation . . . . . 75 mW/Junction
- Soldering Temperature . . . . . 230 °C for 10 s

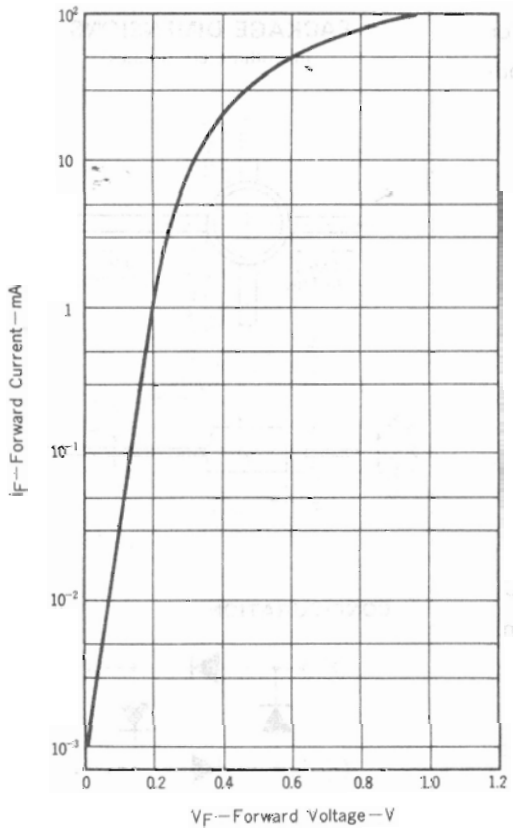
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{F1}	Forward Voltage			0.7	V	I_F = 50 mA
V_{F2}	Forward Voltage		0.2	0.3	V	I_F = 1.0 mA
ΔV_{F2} (NOTE 1)	Delta Forward Voltage			0.02	V	I_F = 1.0 mA
C_t (NOTE 2)	Terminal Capacitance		0.9	1.2	pF	V_R = 0, f = 1.0 MHz
ΔC_t (NOTE 1)	Delta Terminal Capacitance			0.2	pF	V_R = 0, f = 1.0 MHz

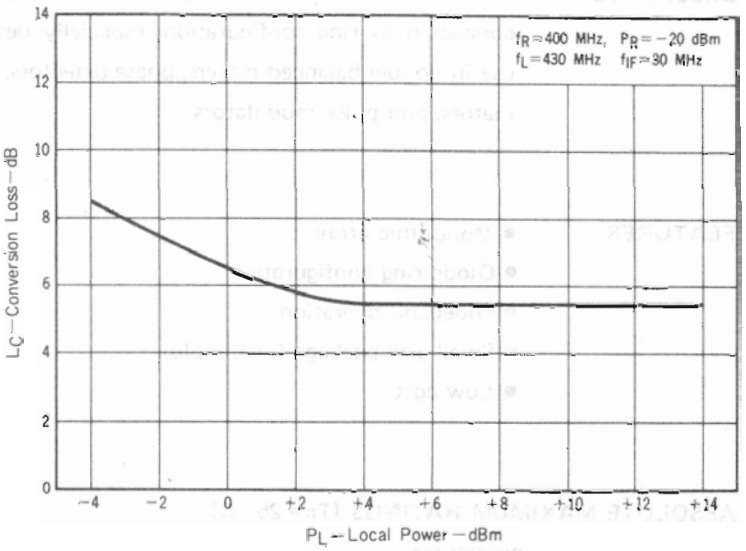
NOTE 1: Difference of V_F, C_t
2: Measurement terminal ① − ③, ② − ④

TYPICAL CHARACTERISTICS (Ta = 25 °C)

FORWARD CURRENT vs.
FORWARD VOLTAGE



CONVERSION LOSS vs. LOCAL POWER



NEC
ELECTRON DEVICE

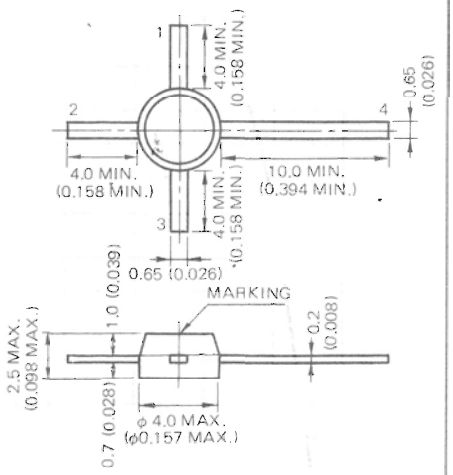
UHF MODULATOR DIODE QUAD
ND487R2-3R

DESCRIPTION The ND487R2-3R is schottky barrier diode quad interconnected in ring configuration, especially designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators.

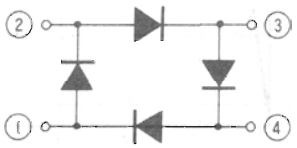
FEATURES

- Monolithic array
- Diode ring configuration
- Wideband operation
- Small size package (disk mold)
- Low cost

PACKAGE DIMENSIONS
in millimeters (inches)



CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)

- DC Power Dissipation . . . . . 75 mW/Junction
- Soldering Temperature . . . . . 230 °C for 10 s

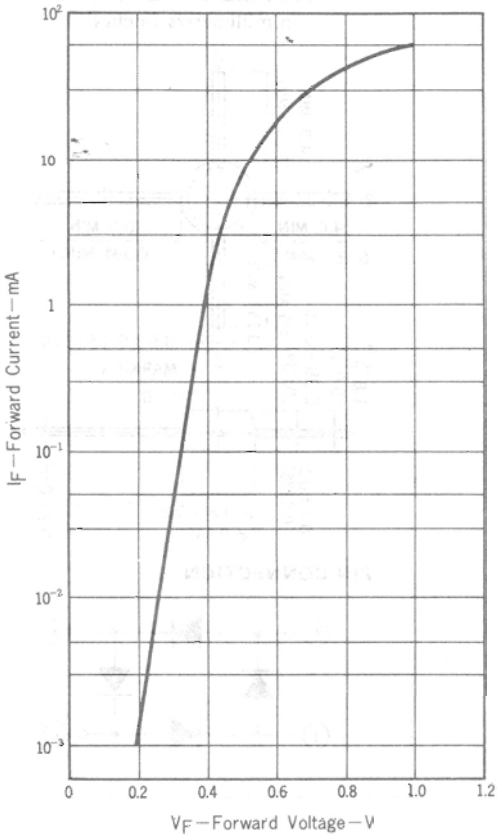
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{F1}	Forward Voltage			1.0	V	I_F = 50 mA
V_{F2}	Forward Voltage		0.4	0.5	V	I_F = 1.0 mA
ΔV_{F2} (NOTE 1)	Delta Forward Voltage			0.02	V	I_F = 1.0 mA
C_t (NOTE 2)	Terminal Capacitance		0.9	1.2	pF	V_R = 0, f = 1.0 MHz
ΔC_t (NOTE 1)	Delta Terminal Capacitance			0.2	pF	V_R = 0, f = 1.0 MHz

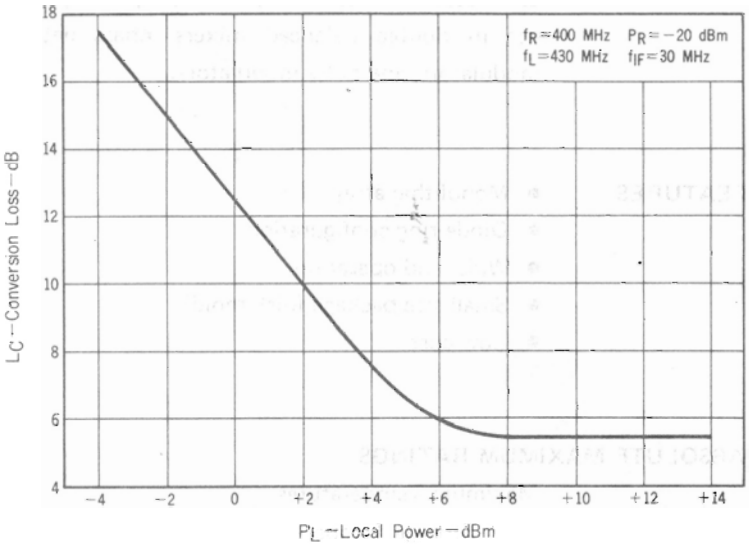
NOTE 1: Difference of V_F, C_t
2: Measurement terminal ① − ③, ② − ④

TYPICAL CHARACTERISTICS (Ta = 25 °C)

FORWARD CURRENT vs. FORWARD VOLTAGE



CONVERSION LOSS vs. LOCAL POWER



NEC
ELECTRON DEVICE

GaAs EPITAXIAL SCHOTTKY BARRIER DIODE QUAD

ND587R-3R

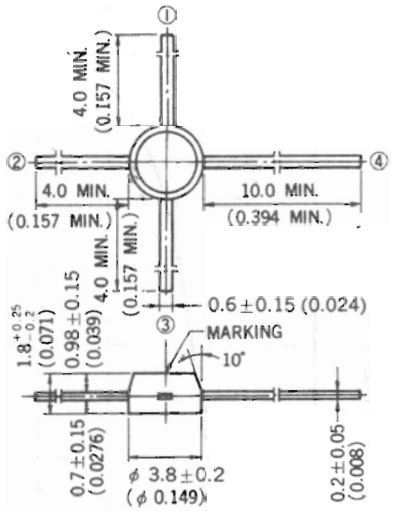
NEW DEVICE

DESCRIPTION The ND587R-3R is schottky barrier diode quad interconnected in quad configuration, especially designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators.

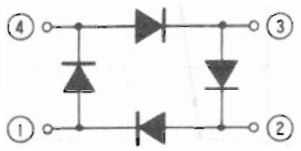
FEATURES

- Monolithic array
- Diode ring configuration
- Wideband operation
- Small size package (disk mold)
- Low cost

PACKAGE DIMENSIONS
in millimeters (inches)



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

- Storage Temperature . . . . . −65 to +150 °C
- Junction Temperature . . . . . 150 °C Maximum

Maximum Power Dissipation (T_a = 25 °C)

DC Power Dissipation	P_d	75	mW/Junction
Soldering Temperature		230	°C for 10 s

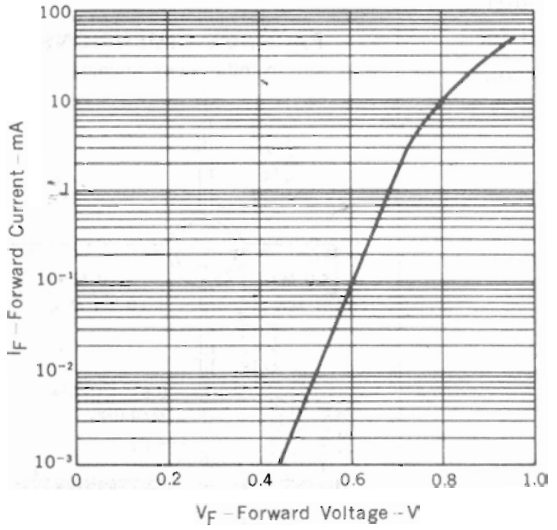
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{F1}	Forward Voltage			1.0	V	I_F = 50 mA
V_{F2}	Forward Voltage		0.67	0.8	V	I_F = 1.0 mA
ΔV_{F2} (NOTE 1)	Delta Forward Voltage			0.02	V	I_F = 1.0 mA
C_t (NOTE 2)	Terminal Capacitance		0.3	0.5	pF	V_R = 0, f = 1.0 MHz
ΔC_t (NOTE 1)	Delta Terminal Capacitance			0.2	pF	V_R = 0, f = 1.0 MHz

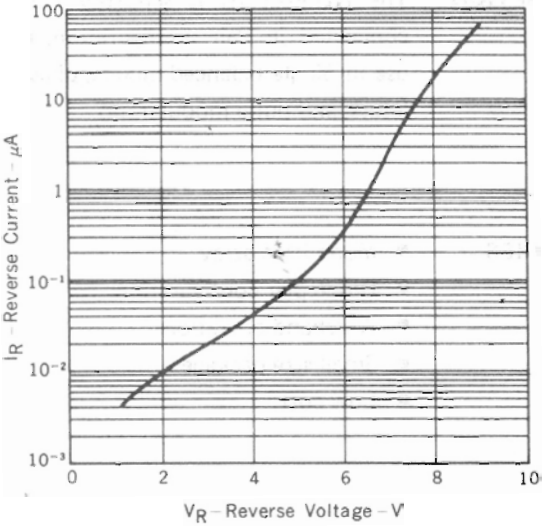
NOTE 1 : Difference of V_F, C_t
2 : Measurement terminal ① − ③, ② − ④

TYPICAL CHARACTERISTICS (T_a = 25 °C)

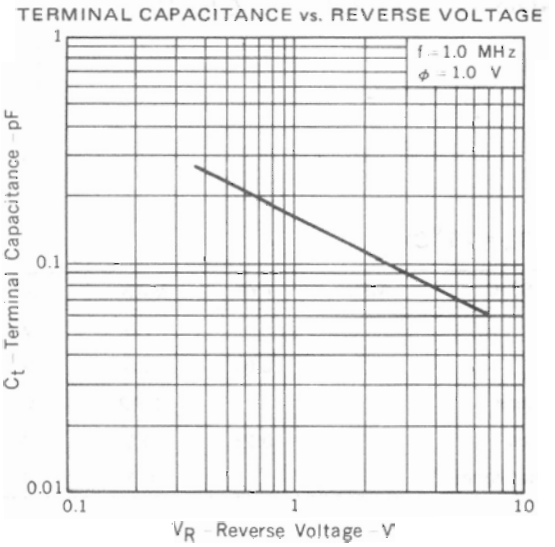
FORWARD CURRENT vs. FORWARD VOLTAGE



REVERSE CURRENT vs. REVERSE VOLTAGE



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



NEC
ELECTRON DEVICE

GaAs EPITAXIAL SCHOTTKY BARRIER DIODE PAIR

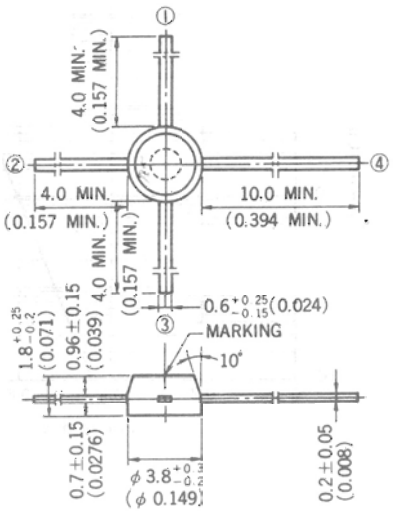
ND587T-3R

DESCRIPTION The ND587T-3R is schottky barrier diode pair interconnected in Pair configuration, especially designed for use in Single balanced mixers, phase detectors, AM modulators, and pulse modulators.

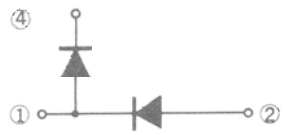
FEATURES

- Monolithic array
- Diode pair configuration
- Wideband operation
- Small size package
- Low cost

PACKAGE DIMENSIONS
in millimeters (inches)



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

DC Power Dissipation	P_d	75	mW/Junction
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Soldering Temperature		230	°C for 10 s

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

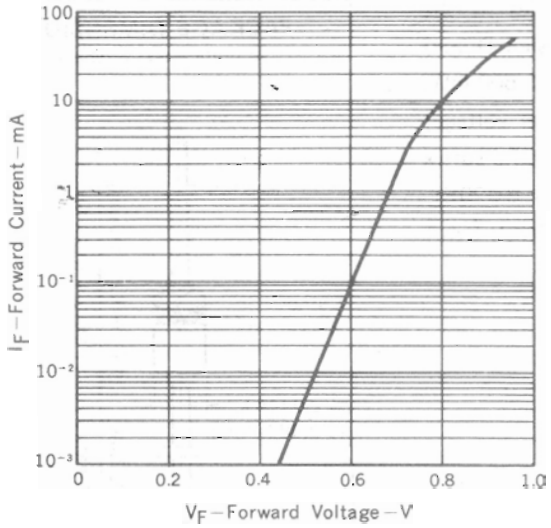
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{F1}	Forward Voltage			1.0	V	I_F = 50 mA
V_{F2}	Forward Voltage		0.67	0.8	V	I_F = 1.0 mA
ΔV_{F2} (NOTE 1)	Delta Forward Voltage			0.02	V	I_F = 1.0 mA
C_t (NOTE 2)	Terminal Capacitance		0.25	0.5	pF	V_R = 0, f = 1.0 MHz
ΔC_t (NOTE 1)	Delta Terminal Capacitance			0.1	pF	V_R = 0, f = 1.0 MHz

NOTE 1 : Difference of V_F, C_t
2 : Measurement terminal ① – ②, ① – ④

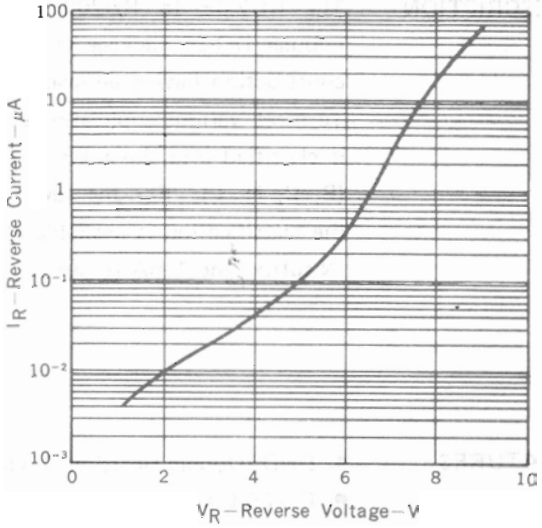
NEW DEVICE

TYPICAL CHARACTERISTICS (T_a = 25 °C)

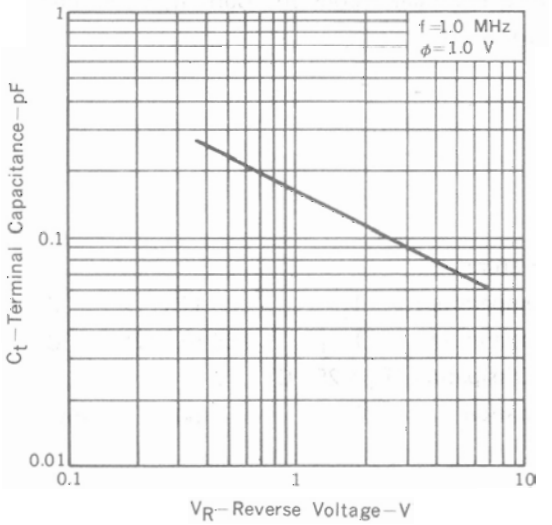
FORWARD CURRENT vs. FORWARD VOLTAGE



REVERSE CURRENT vs. REVERSE VOLTAGE



TERMINAL CAPACITANCE vs. REVERSE VOLTAGE



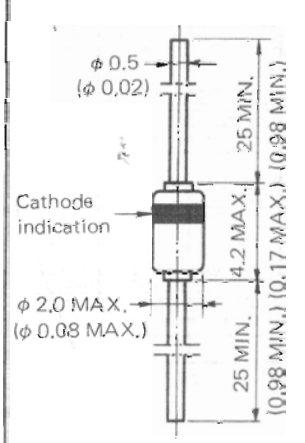
NEC
ELECTRON DEVICE

ZENER DIODES
RD2.0E ~ RD200E

DESCRIPTION

The RD2.0E to RD200E Series are zener diodes in the popular DO-35 package with DHD (Double Heatsink Diode) construction having allowable power dissipation of 500 mW. To meet various application at customers, V_Z (zener voltage) is classified into the tight torelance under the specific suffix (B, C, N, L). For the low voltage types (up to RD20E), the classification is available at 20 mA (B or C suffix), 5 mA (N suffix) and 1 mA (L suffix).

PACKAGE DIMENSIONS
in millimeters (inches)



FEATURES

- DHD (Double Heatsink Diode) Construction
- DO-35 Glass sealed package

APPLICATIONS

Circuits for Constant Voltage, Constant Current, Waveform Clipper, Surge absorber, etc.

MAXIMUM RATINGS

Maximum Temperatures			
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C
Maximum Power Dissipation (T_a = 25 °C)			
Power Dissipation	P	500	mW

ELECTRICAL CHARACTERISTICS (T_a = 25±2 °C)

(1) RD [ ] E B Series (2.0 ~ 39 V)

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD2.0E	B	1.88	2.20	20	140	20	2000	1	120	0.5
	B1	1.88	2.10							
	B2	2.02	2.20							
RD2.2E	B	2.09	2.41	20	120	20	2000	1	120	0.7
	B1	2.12	2.30							
	B2	2.22	2.41							
RD2.4E	B	2.30	2.64	20	100	20	2000	1	120	1.0
	B1	2.33	2.52							
	B2	2.43	2.63							
RD2.7E	B	2.5	2.9	20	100	20	1000	1	100	1.0
	B1	2.54	2.75							
	B2	2.69	2.91							
RD3.0E	B	2.8	3.2	20	80	20	1000	1	50	1.0
	B1	2.85	3.07							
	B2	3.01	3.22							
RD3.3E	B	3.1	3.5	20	70	20	1000	1	20	1.0
	B1	3.16	3.38							
	B2	3.32	3.53							
RD3.6E	B	3.4	3.8	20	60	20	1000	1	10	1.0
	B1	3.47	3.68							
	B2	3.62	3.83							
RD3.9E	B	3.7	4.1	20	50	20	1000	1	5	1.0
	B1	3.77	3.98							
	B2	3.92	4.14							
RD4.3E	B	4.0	4.5	20	40	20	1000	1	5	1.0
	B1	4.05	4.26							
	B2	4.20	4.40							
	B3	4.34	4.53							
RD4.7E	B	4.4	4.9	20	25	20	900	1	5	1.0
	B1	4.47	4.65							
	B2	4.59	4.77							
	B3	4.71	4.91							
RD5.1E	B	4.8	5.4	20	20	20	800	1	5	1.5
	B1	4.85	5.03							
	B2	4.97	5.18							
	B3	5.12	5.35							
RD5.6E	B	5.3	6.0	20	13	20	500	1	5	2.5
	B1	5.29	5.52							
	B2	5.46	5.70							
	B3	5.64	5.88							
RD6.2E	B	5.8	6.6	20	10	20	300	1	5	3.0
	B1	5.81	6.06							
	B2	5.99	6.24							
	B3	6.16	6.40							
RD6.8E	B	6.4	7.2	20	8	20	150	0.5	2	3.5
	B1	6.32	6.59							
	B2	6.52	6.79							
	B3	6.70	6.97							
RD7.5E	B	7.0	7.9	20	8	20	120	0.5	0.5	4.0
	B1	6.88	7.19							
	B2	7.11	7.41							
	B3	7.33	7.64							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD8.2E	B	7.7	8.7	20	8	20	120	0.5	0.5	5.0
	B1	7.56	7.90							
	B2	7.82	8.15							
	B3	8.07	8.41							
RD9.1E	B	8.5	9.6	20	8	20	120	0.5	0.5	6.0
	B1	8.33	8.70							
	B2	8.61	8.99							
	B3	8.89	9.29							
RD10E	B	9.4	10.9	20	8	20	120	0.5	0.2	7.0
	B1	9.19	9.59							
	B2	9.48	9.90							
	B3	9.82	10.30							
RD11E	B	10.4	11.6	10	10	10	120	0.5	0.2	8.0
	B1	10.18	10.63							
	B2	10.50	10.95							
	B3	10.82	11.26							
RD12E	B	11.4	12.6	10	12	10	110	0.5	0.2	9.0
	B1	11.13	11.63							
	B2	11.50	11.92							
	B3	11.80	12.30							
RD13E	B	12.4	14.1	10	14	10	110	0.5	0.2	10
	B1	12.18	12.71							
	B2	12.59	13.16							
	B3	13.03	13.62							
RD15E	B	13.8	15.6	10	16	10	110	0.5	0.2	11
	B1	13.48	14.09							
	B2	13.95	14.56							
	B3	14.42	15.02							
RD16E	B	15.3	17.1	10	18	10	150	0.5	0.2	12
	B1	14.87	15.50							
	B2	15.33	15.96							
	B3	15.79	16.50							
RD18E	B	16.8	19.1	10	23	10	150	0.5	0.2	13
	B1	16.34	17.06							
	B2	16.90	17.67							
	B3	17.51	18.30							
RE20E	B	18.8	21.6	10	28	10	200	0.5	0.2	15
	B1	18.11	18.92							
	B2	18.73	19.57							
	B3	19.38	20.22							
	B4	19.88	20.72							
RD22E	B	20.8	23.3	5	30	5	200	0.5	0.2	17
	B1	20.23	21.08							
	B2	20.76	21.65							
	B3	21.22	22.09							
	B4	21.68	22.61							
RD24E	B	22.8	25.6	5	35	5	200	0.5	0.2	19
	B1	22.26	23.12							
	B2	22.75	23.73							
	B3	23.29	24.27							
	B4	23.81	24.81							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD27E	B	25.1	28.9	5	45	5	250	0.5	0.2	21
	B1	24.26	25.52							
	B2	24.97	26.26							
	B3	25.63	26.95							
	B4	26.29	27.64							
RD30E	B	28.0	32.0	5	55	5	250	0.5	0.2	23
	B1	26.99	28.39							
	B2	27.70	29.13							
	B3	28.36	29.82							
	B4	29.02	30.51							
RD33E	B	31.0	35.0	5	65	5	250	0.5	0.2	25
	B1	29.68	31.22							
	B2	30.32	31.88							
	B3	30.90	32.50							
	B4	31.49	33.11							
RD36E	B	34.0	38.0	5	75	5	250	0.5	0.2	27
	B1	32.14	33.79							
	B2	32.79	34.49							
	B3	33.40	35.13							
	B4	34.01	35.77							
RD39E	B	37.0	43.0	5	85	5	250	0.5	0.2	30
	B1	34.68	36.47							
	B2	35.36	37.19							
	B3	36.00	37.85							
	B4	36.63	38.52							
	B5	37.36	39.29							
	B6	38.14	40.11							
	B7	38.94	40.80							

* Suffix B : tested with D.C.
Suffix B1 ~ B7 : tested with pulse (40 ms)

** Z_Z and Z_{ZK} are measured at I_Z by given a very small A.C. current signal.

(2) RD [ ] E B Series (43 ~ 120 V)

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD43E	B	40	45	5	90	5	0.2	33
RD47E	B	44	49	5	90	5	0.2	36
RD51E	B	48	54	5	110	5	0.2	39
RD56E	B	53	60	5	110	5	0.2	43
RD62E	B	58	66	2	200	2	0.2	47
RD68E	B	64	72	2	200	2	0.2	52
RD75E	B	70	79	2	300	2	0.2	57
RD82E	B	77	87	2	300	2	0.2	63
RD91E	B	85	96	2	400	2	0.2	69
RD100E	B	94	106	2	400	2	0.2	76
RD110E	B	104	116	1	750	1	0.2	84
RE120E	B	114	126	1	900	1	0.2	91

* tested with pulse (40 ms)

** Z_Z are measured at I_Z by given a very small A.C. current signal.

(3) RD [ ] E B Series (130 ~ 200 V)

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD130E	B	120	140	1	1100	1	0.2	100
RD140E	B	130	150	1	1300	1	0.2	110
RD150E	B	140	160	1	1500	1	0.2	120
RD160E	B	150	170	1	1700	1	0.2	130
RD170E	B	160	180	1	1900	1	0.2	140
RD180E	B	170	190	1	2200	1	0.2	140
RD190E	B	180	200	1	2400	1	0.2	150
RD200E	B	190	210	1	2500	1	0.2	160

* tested with pulse (40 ms).

** Z_Z are measured at I_Z by given a very small A.C. current signal.

(4) RD [ ] E L Series

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD2.7E	L	2.54	2.91	1	100	20	1000	1	100	1.0
	L1	2.54	2.75							
	L2	2.69	2.91							
RD3.0E	L	2.85	3.22	1	80	20	1000	1	50	1.0
	L1	2.85	3.07							
	L2	3.01	3.22							
RD3.3E	L	3.16	3.53	1	70	20	1000	1	20	1.0
	L1	3.16	3.38							
	L2	3.32	3.53							
RD3.6E	L	3.47	3.83	1	60	20	1000	1	10	1.0
	L1	3.47	3.68							
	L2	3.62	3.83							
RD3.9E	L	3.77	4.14	1	50	20	1000	1	5	1.0
	L1	3.77	3.98							
	L2	3.92	4.14							
RD4.3E	L	4.05	4.53	1	40	20	1000	1	5	1.0
	L1	4.05	4.26							
	L2	4.20	4.40							
	L3	4.34	4.53							
RD4.7E	L	4.47	4.91	1	25	20	900	1	5	1.0
	L1	4.47	4.65							
	L2	4.59	4.77							
	L3	4.71	4.91							
RD5.1E	L	4.85	5.35	1	20	20	800	1	5	1.5
	L1	4.85	5.03							
	L2	4.97	5.18							
	L3	5.12	5.35							
RD5.6E	L	5.29	5.88	1	13	20	500	1	5	2.5
	L1	5.29	5.52							
	L2	5.46	5.70							
	L3	5.64	5.88							
RD6.2E	L	5.81	6.40	1	10	20	300	1	5	3.0
	L1	5.81	6.06							
	L2	5.99	6.24							
	L3	6.16	6.40							
RD6.8E	m	6.32	6.97	1	8	20	150	0.5	2	3.5
	L1	6.32	6.59							
	L2	6.52	6.79							
	L3	6.70	6.97							
RD7.5E	L	6.88	7.64	1	8	20	120	0.5	0.5	4.0
	L1	6.88	7.19							
	L2	7.11	7.41							
	L3	7.33	7.64							
RD8.2E	L	7.56	8.41	1	8	20	120	0.5	0.5	5.0
	L1	7.56	7.90							
	L2	7.82	8.15							
	L3	8.07	8.41							
RD9.1E	L	8.33	9.29	1	8	20	120	0.5	0.5	6.0
	L1	8.33	8.70							
	L2	8.61	8.99							
	L3	8.89	9.29							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD10E	L	9.19	10.30	1	8	20	120	0.5	0.2	7.0
	L1	9.19	9.59							
	L2	9.48	9.90							
	L3	9.82	10.30							
RD11E	L	10.18	11.26	1	10	10	120	0.5	0.2	8.0
	L1	10.18	10.63							
	L2	10.50	10.95							
	L3	10.82	11.26							
RD12E	L	11.13	12.30	1	12	10	110	0.5	0.2	9.0
	L1	11.13	11.63							
	L2	11.50	11.92							
	L3	11.80	12.30							
RD13E	L	12.18	13.62	1	14	10	110	0.5	0.2	10
	L1	12.18	12.71							
	L2	12.59	13.16							
	L3	13.03	13.62							
RD15E	L	13.48	15.02	1	16	10	110	0.5	0.2	11
	L1	13.48	14.09							
	L2	13.95	14.56							
	L3	14.42	15.02							
RD16E	L	14.87	16.50	1	18	10	150	0.5	0.2	12
	L1	14.87	15.50							
	L2	15.33	15.96							
	L3	15.79	16.50							
RD18E	L	16.34	18.30	1	23	10	150	0.5	0.2	13
	L1	16.34	17.06							
	L2	16.90	17.67							
	L3	17.51	18.30							
RD20E	L	18.11	20.72	1	28	10	200	0.5	0.2	15
	L1	18.11	18.92							
	L2	18.73	19.57							
	L3	19.38	20.22							
	L4	19.88	20.72							
RD22E	L	20.23	22.61	1	30	5	200	0.5	0.2	17
	L1	20.23	21.08							
	L2	20.76	21.65							
	L3	21.22	22.09							
	L4	21.68	22.61							
RD24E	L	22.26	24.81	1	35	5	200	0.5	0.2	19
	L1	22.26	23.12							
	L2	22.75	23.73							
	L3	23.29	24.27							
	L4	23.81	24.81							
RD27E	L	24.26	27.64	1	45	5	250	0.5	0.2	21
	L1	24.26	25.52							
	L2	24.97	26.26							
	L3	25.63	26.95							
	L4	26.29	27.64							
RD30E	L	26.99	30.51	1	55	5	250	0.5	0.2	23
	L1	26.99	28.39							
	L2	27.70	29.13							
	L3	28.36	29.82							
	L4	29.02	30.51							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD33E	L	29.68	33.11	1	65	5	250	0.5	0.2	25
	L1	29.68	31.22							
	L2	30.32	31.88							
	L3	30.90	32.50							
	L4	31.49	33.11							
RD36E	L	32.14	35.77	1	75	5	250	0.5	0.2	27
	L1	32.14	33.79							
	L2	32.79	34.49							
	L3	33.40	35.13							
	L4	34.01	35.77							
RD39E	L	34.68	38.52	1	85	5	250	0.5	0.2	30
	L1	34.68	36.47							
	L2	35.36	37.19							
	L3	36.00	37.85							
	L4	36.63	38.52							

* tested with pulse (40 ms).

** Z_Z and Z_{ZK} are measured by I_Z by given a very small A.C. current signal.

(3) RD [ ] E N Series

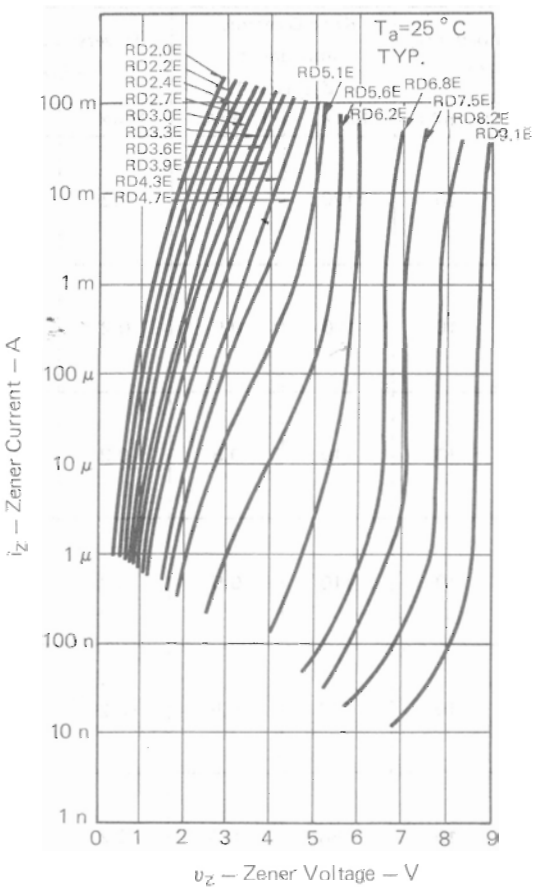
Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD2.7E	N	2.54	2.91	5	100	20	1000	1	100	1.0
	N1	2.54	2.75							
	N2	2.69	2.91							
RD3.0E	N	2.85	3.22	5	80	20	1000	1	50	1.0
	N1	2.85	3.07							
	N2	3.01	3.22							
RD3.3E	N	3.16	5.53	5	70	20	1000	1	20	1.0
	N1	3.16	3.38							
	N2	3.32	3.53							
RD3.6E	N	3.47	3.83	5	60	20	1000	1	10	1.0
	N1	3.47	3.68							
	N2	3.62	3.83							
RD3.9E	N	3.77	4.14	5	50	20	1000	1	5	1.0
	N1	3.77	3.98							
	N2	3.92	4.14							
RD4.3E	N	4.05	4.53	5	40	20	1000	1	5	1.0
	N1	4.05	4.26							
	N2	4.20	4.40							
	N3	4.34	4.53							
RD4.7E	N	4.47	4.91	5	25	20	900	1	5	1.0
	N1	4.47	4.65							
	N2	4.59	4.77							
	N3	4.71	4.91							
RD5.1E	N	4.85	5.35	5	20	20	800	1	5	1.5
	N1	4.85	5.03							
	N2	4.97	5.18							
	N3	5.12	5.35							
RD5.6E	N	5.29	5.88	5	13	20	500	1	5	2.5
	N1	5.29	5.52							
	N2	5.46	5.70							
	N3	5.64	5.88							
RD6.2E	N	5.81	6.40	5	10	20	300	1	5	3.0
	N1	5.81	6.06							
	N2	5.99	6.24							
	N3	6.16	6.40							
RD6.8E	N	6.32	6.97	5	8	20	150	0.5	2	3.5
	N1	6.32	6.59							
	N2	6.52	6.79							
	N3	6.70	6.97							
RD7.5E	N	6.88	7.64	5	8	20	120	0.5	0.5	4.0
	N1	6.88	7.19							
	N2	7.11	7.41							
	N3	7.33	7.64							
RD8.2E	N	7.56	8.41	5	8	20	120	0.5	0.5	5.0
	N1	7.56	7.90							
	N2	7.82	8.15							
	N3	8.07	8.41							
RD9.1E	N	8.33	9.29	5	8	20	120	0.5	0.5	6.0
	N1	8.33	8.70							
	N2	8.61	8.99							
	N3	8.89	9.29							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD10E	N	9.19	10.30	5	8	20	120	0.5	0.2	7.0
	N1	9.19	9.59							
	N2	9.48	9.90							
	N3	9.82	10.30							
RD11E	N	10.18	11.26	5	10	10	120	0.5	0.2	8.0
	N1	10.18	10.63							
	N2	10.50	10.95							
	N3	10.82	11.26							
RD12E	N	11.13	12.30	5	12	10	110	0.5	0.2	9.0
	N1	11.13	11.63							
	N2	11.50	11.92							
	N3	11.80	12.30							
RD13E	N	12.18	13.62	5	14	10	110	0.5	0.2	10
	N1	12.18	12.71							
	N3	12.59	13.16							
	N3	13.03	13.62							
RD15E	N	13.48	15.02	5	16	10	110	0.5	0.2	11
	N1	13.48	14.09							
	N2	13.95	14.56							
	N3	14.42	15.02							
RD16E	N	14.87	16.50	5	18	10	150	0.5	0.2	12
	N1	14.87	15.50							
	N2	15.33	15.96							
	N3	15.79	16.50							
RD18E	N	16.34	18.30	5	23	10	150	0.5	0.2	13
	N1	16.34	17.06							
	N2	16.90	17.67							
	N3	17.51	18.30							
RD20E	N	18.11	20.72	5	28	10	200	0.5	0.2	15
	N1	18.11	18.92							
	N2	18.73	19.57							
	N3	19.38	20.22							
	N4	19.88	20.72							

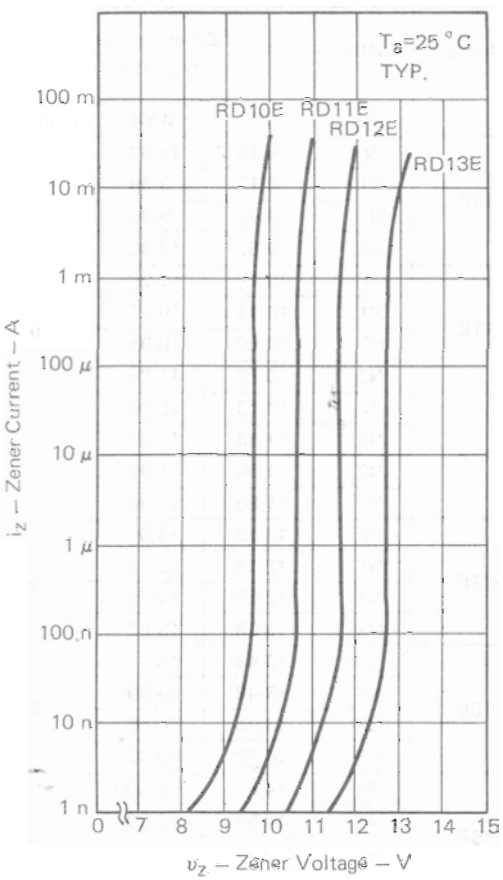
* tested with pulse (40 ms).

** Z_Z and Z_{ZK} are measured at I_Z by given a very small A.C. current signal.

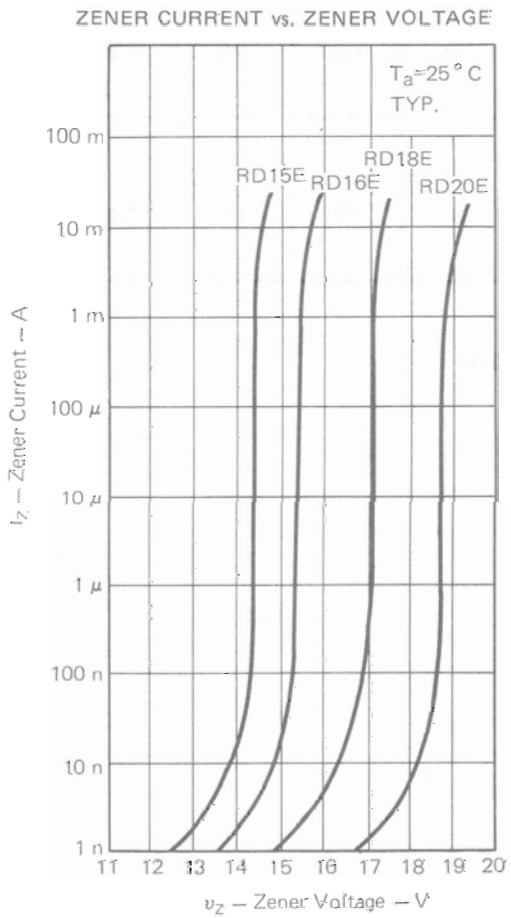
ZENER CURRENT vs. ZENER VOLTAGE



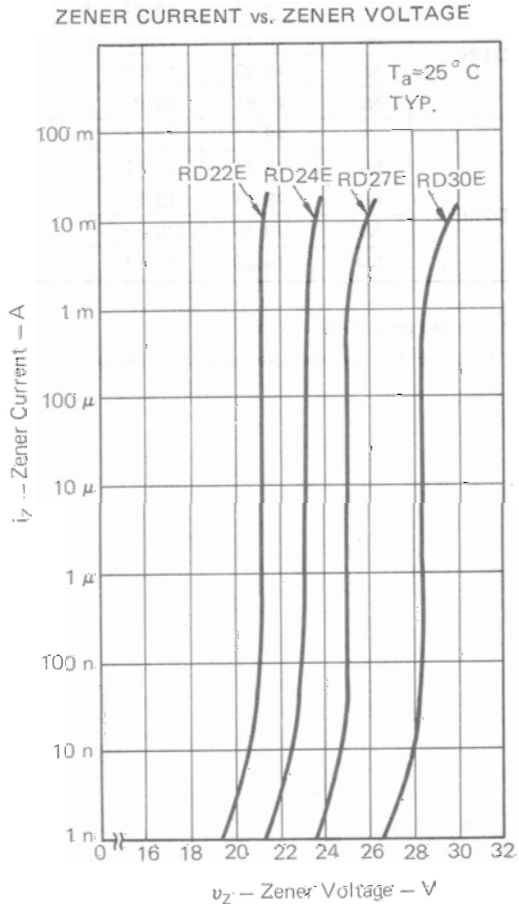
ZENER CURRENT vs. ZENER VOLTAGE



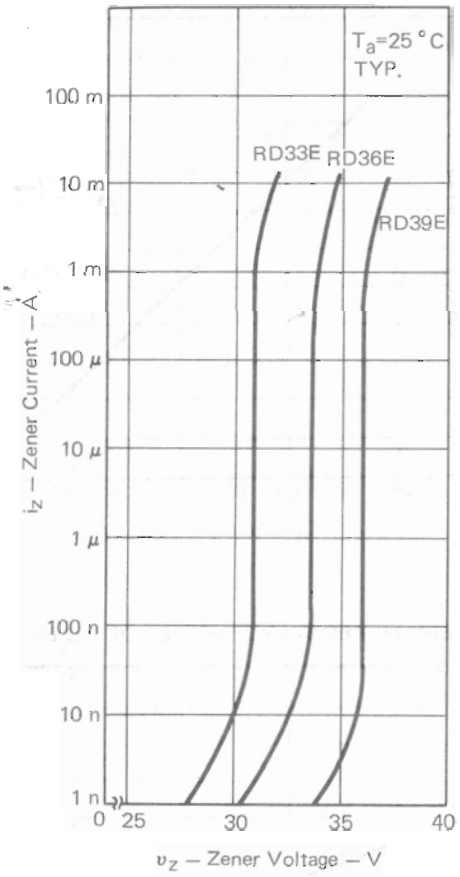
ZENER CURRENT vs. ZENER VOLTAGE



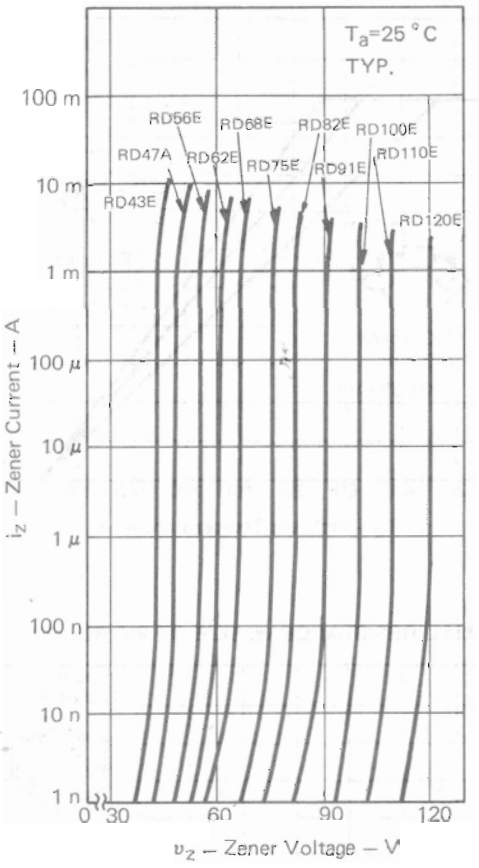
ZENER CURRENT vs. ZENER VOLTAGE



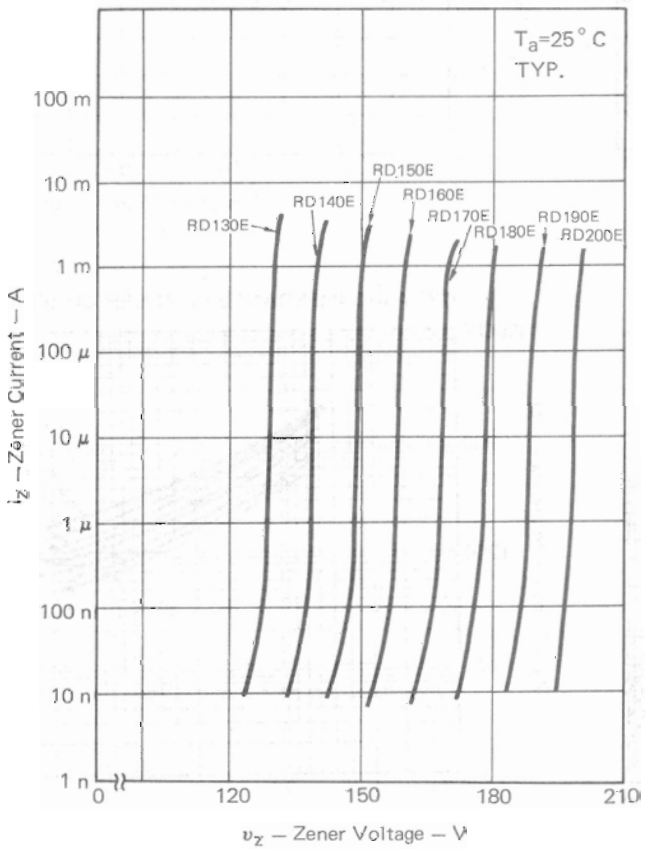
ZENER CURRENT vs. ZENER VOLTAGE



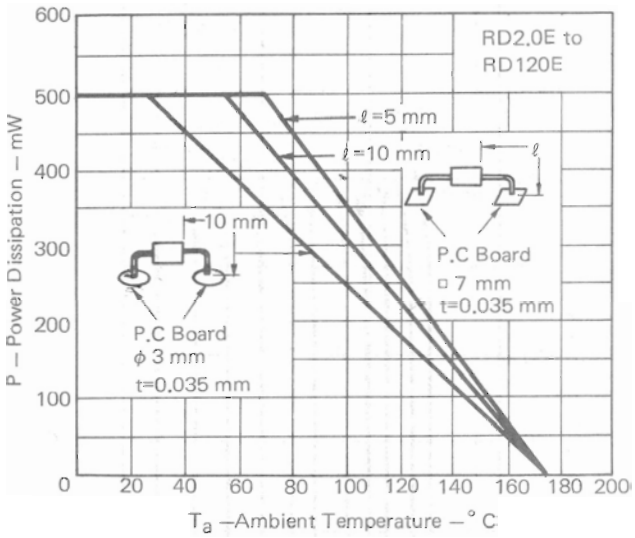
ZENER CURRENT vs. ZENER VOLTAGE



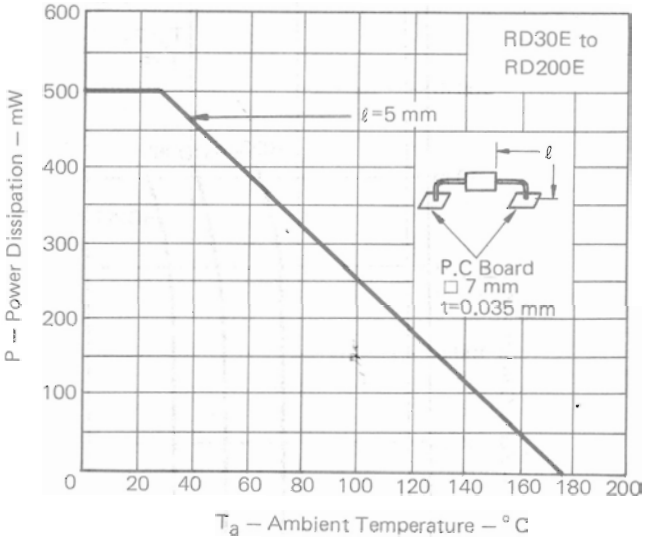
ZENER CURRENT vs. ZENER VOLTAGE



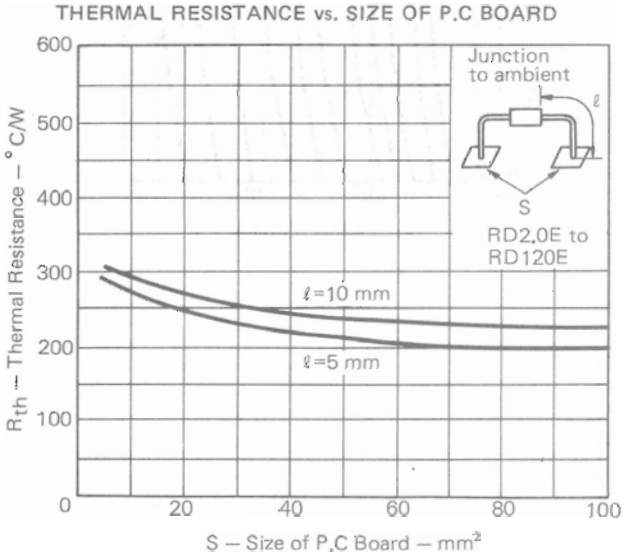
POWER DISSIPATION vs. AMBIENT TEMPERATURE



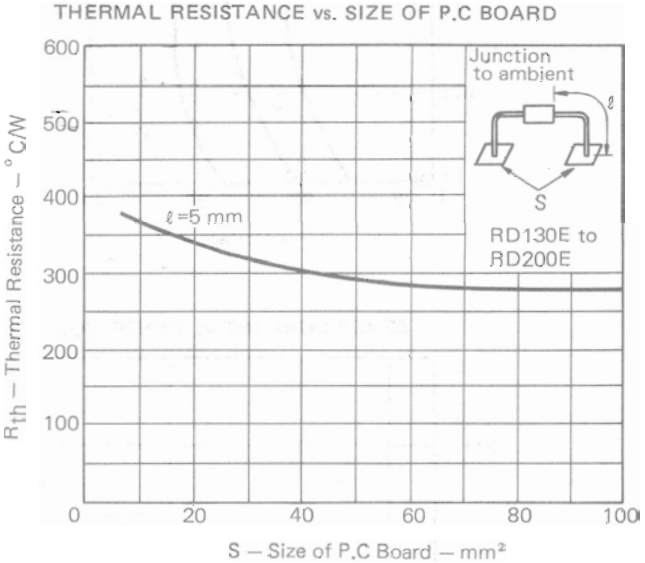
POWER DISSIPATION vs. AMBIENT TEMPERATURE



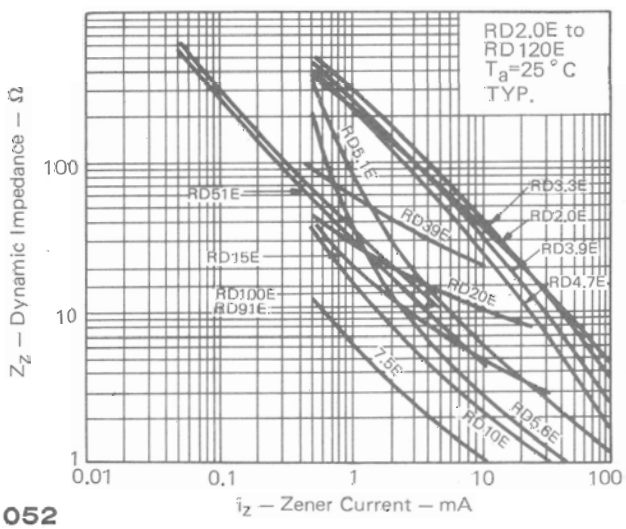
THERMAL RESISTANCE vs. SIZE OF P.C BOARD



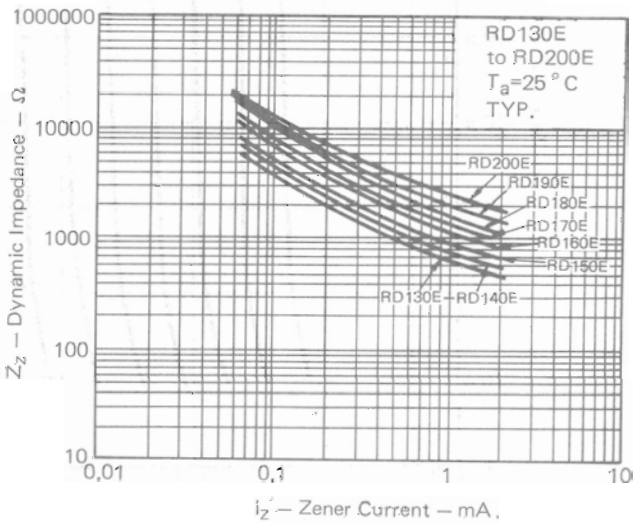
THERMAL RESISTANCE vs. SIZE OF P.C BOARD



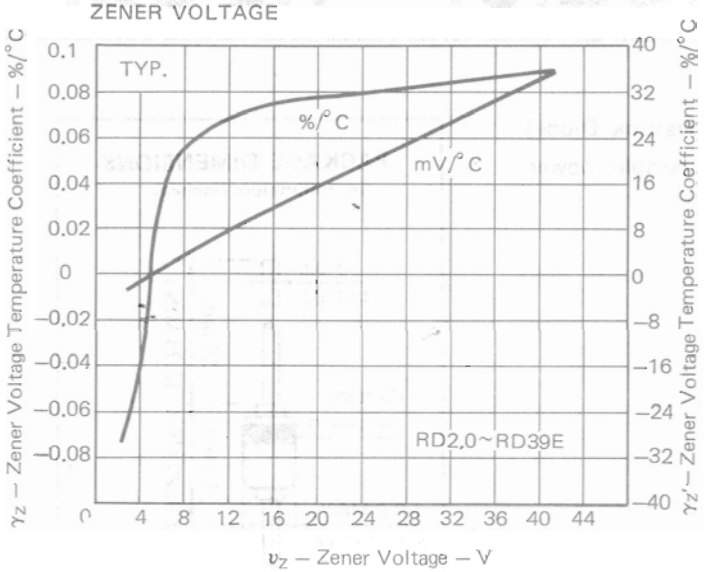
DYNAMIC IMPEDANCE vs. ZENER CURRENT



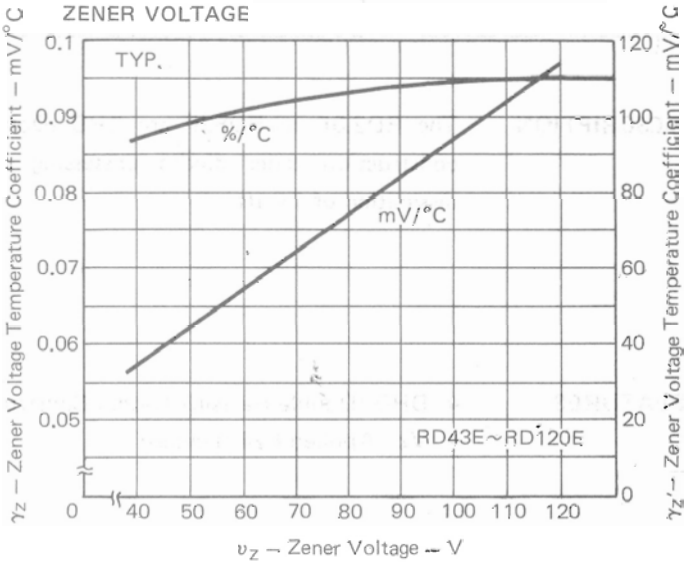
DYNAMIC IMPEDANCE vs. ZENER CURENT



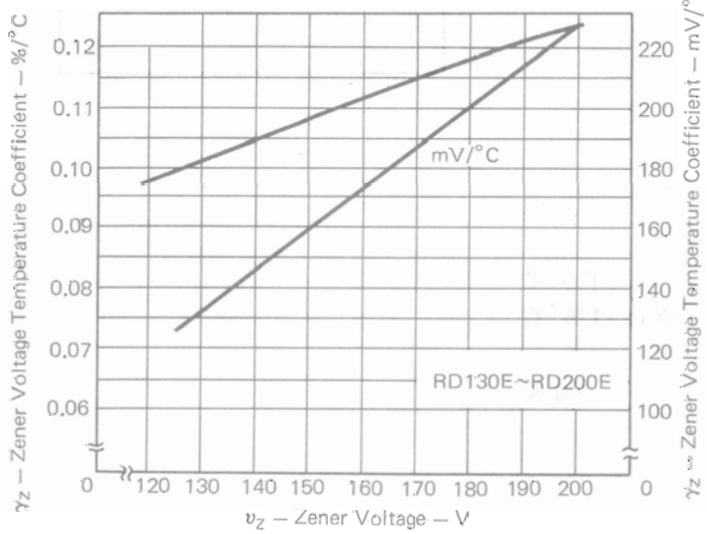
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



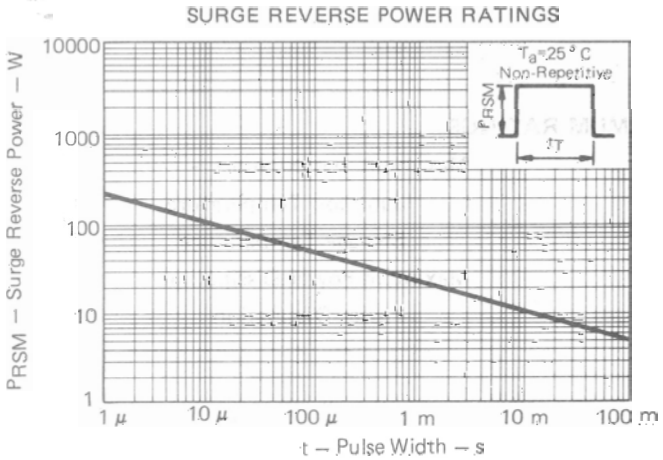
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



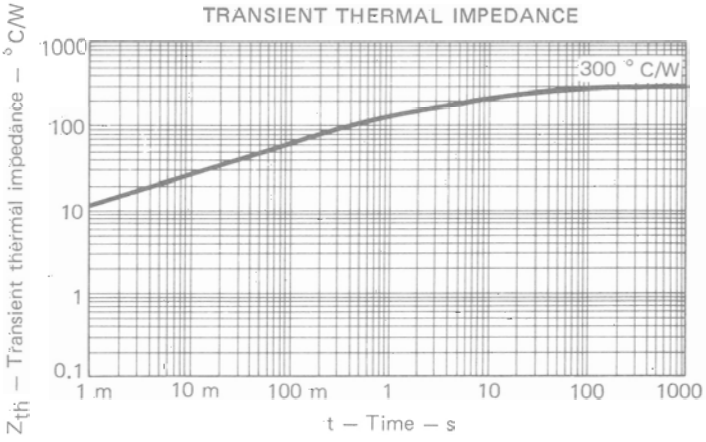
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



SURGE REVERSE POWER RATINGS



TRANSIENT THERMAL IMPEDANCE

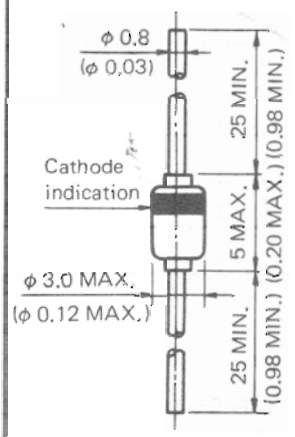


NEC
ELECTRON DEVICE

ZENER DIODES
RD2.0F ~ RD82F

DESCRIPTION The RD2.0F to RD82F are DHD (Double Heatsink Diode) construction zener diodes possessing an allowable power dissipation of 1 watt.

PACKAGE DIMENSIONS
in millimeters (inches)



FEATURES

- DHD (Double Heatsink Diode) Construction
- Vz : Applied E24 standard

APPLICATIONS Circuits for, Constant Voltage, Constant Current, Waveform clipper, Surge absorber, etc.

MAXIMUM RATINGS

Maximum Temperature		
Junction Temperature	T_j	175 °C
Storage Temperature	T_{stg}	−65 to +175 °C
Maximum Power Dissipation		
Power Dissipation	P	1.0 W

ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 2\,^{\circ}C$)

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD2.0F	B	1.88	2.24	40	25	40	200	0.5
	B1	1.88	2.12					
	B2	2.01	2.25					
RD2.2F	B	2.08	2.45	40	20	40	200	0.7
	B1	2.11	2.34					
	B2	2.21	2.45					
BD2.4F	B	2.28	2.70	40	15	40	200	1.0
	B1	2.31	2.55					
	B2	2.41	2.65					
RD2.7F	B	2.5	2.9	40	15	40	150	1.0
	B1	2.52	2.78					
	B2	2.68	2.93					
RD3.0F	B	2.8	3.2	40	15	40	100	1.0
	B1	2.83	3.07					
	B2	2.97	3.22					
RD3.3F	B	3.1	3.5	40	15	40	80	1.0
	B1	3.13	3.37					
	B2	3.27	3.51					
RD3.6F	B	3.4	3.8	40	15	40	60	1.0
	B1	3.43	3.68					
	B2	3.58	3.83					
RD3.9F	B	3.7	4.1	40	15	40	40	1.0
	B1	3.73	4.00					
	B2	3.88	4.15					
RD4.3F	B	4.0	4.5	40	15	40	20	1.0
	B1	4.03	4.28					
	B2	4.15	4.41					
	B3	4.28	4.55					
RD4.7F	B	4.4	4.9	40	10	40	20	1.0
	B1	4.41	4.65					
	B2	4.53	4.78					
	B3	4.66	4.91					
RD5.1F	B	4.8	5.4	40	8	40	20	1.0
	B1	4.79	5.05					
	B2	4.95	5.22					
	B3	5.10	5.38					
RD5.6F	B	5.3	6.0	40	8	40	20	1.5
	B1	5.28	5.56					
	B2	5.46	5.75					
	B3	5.65	5.95					
RD6.2F	B	5.8	6.6	40	6	40	20	3.0
	B1	5.76	6.14					
	B2	5.98	6.33					
	B3	6.17	6.52					
RD6.8F	B	6.4	7.2	40	6	40	20	3.5
	B1	6.35	6.71					
	B2	6.55	6.90					
	B3	6.74	7.10					
RD7.5F	B	7.0	7.9	40	4	40	20	4.0
	B1	6.93	7.33					
	B2	7.17	7.55					
	B3	7.39	7.80					

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD8.2F	B	7.7	8.7	40	4	40	20	5.0
	B1	7.58	8.03					
	B2	7.87	8.28					
	B3	8.12	8.54					
RD9.1F	B	8.5	9.6	40	6	40	20	6.0
	B1	8.34	8.80					
	B2	8.64	9.08					
	B3	8.91	9.38					
RD10F	B	9.4	11.1	40	6	40	10	7.0
	B1	9.16	9.67					
	B2	9.50	9.99					
	B3	9.83	10.40					
RD11F	B	10.4	11.6	20	8	20	10	8.0
	B1	10.22	10.75					
	B2	10.54	11.09					
	B3	10.87	11.43					
RD12F	B	11.4	12.6	20	8	20	10	8.0
	B1	11.19	11.77					
	B2	11.50	12.09					
	B3	11.80	12.41					
RD13F	B	12.4	14.1	20	10	20	10	10
	B1	12.19	12.85					
	B2	12.63	13.30					
	B3	13.11	13.83					
RD15F	B	13.8	15.6	20	10	20	10	11
	B1	13.55	14.28					
	B2	14.05	14.77					
	B3	14.52	15.26					
RD16F	B	15.3	17.1	20	12	20	10	12
	B1	14.98	15.75					
	B2	15.44	16.23					
	B3	14.89	16.71					
RD18F	B	16.8	19.1	20	12	20	10	13
	B1	16.37	17.27					
	B2	17.03	17.91					
	B3	17.64	18.55					
RD20F	B	18.8	22.2	20	14	20	10	15
	B1	18.26	19.21					
	B2	18.93	19.91					
	B3	19.59	20.84					
RD22F	B	20.8	23.3	10	14	10	10	17
	B1	20.45	21.51					
	B2	21.10	22.18					
	B3	21.75	22.86					
RD24F	B	22.8	25.6	10	16	10	10	19
	B1	22.44	23.59					
	B2	23.17	24.36					
	B3	23.90	25.14					
RD27F	B	25.1	28.9	10	16	10	10	21
	B1	24.63	26.10					
	B2	25.70	27.12					
	B3	26.72	28.43					

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD30F	B	28.0	32.0	10	18	10	10	23
	B1	27.43	29.09					
	B2	28.64	30.10					
	B3	29.57	31.26					
RD33F	B	31.0	35.0	10	18	10	10	25
	B1	30.35	31.97					
	B2	31.49	33.06					
	B3	32.39	34.15					
RD36F	B	34.0	38.0	10	20	10	10	27
	B1	33.24	34.94					
	B2	34.26	36.01					
	B3	35.19	37.01					
RD39F	B	37.0	43.0	10	20	10	10	30
	B1	36.11	38.00					
	B2	37.14	39.04					
	B3	38.13	40.80					

* Suffix B : tested with D.C.
Suffix B1 ~ B3 : testes with pulse (40 ms).

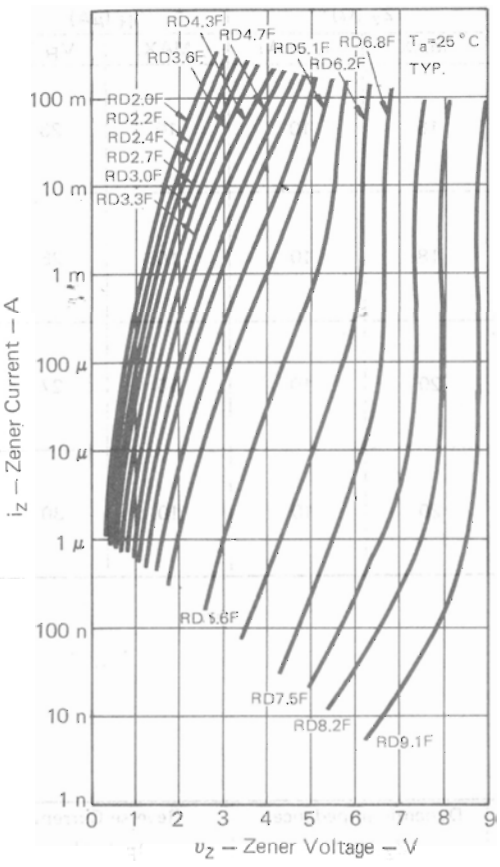
** Z_Z is measured at I_Z by given a very small A.C. current signal.

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD43F	B	40	45	10	50	10	5	33
RD47F	B	44	49	10	50	10	5	36
RD51F	B	48	54	10	50	10	5	39
RD56F	B	53	60	10	50	10	5	43
RD62F	B	58	66	10	50	10	5	47
RD68F	B	64	72	10	70	10	5	52
RD75F	B	70	79	10	90	10	5	57
RD82F	B	77	87	10	90	10	5	63

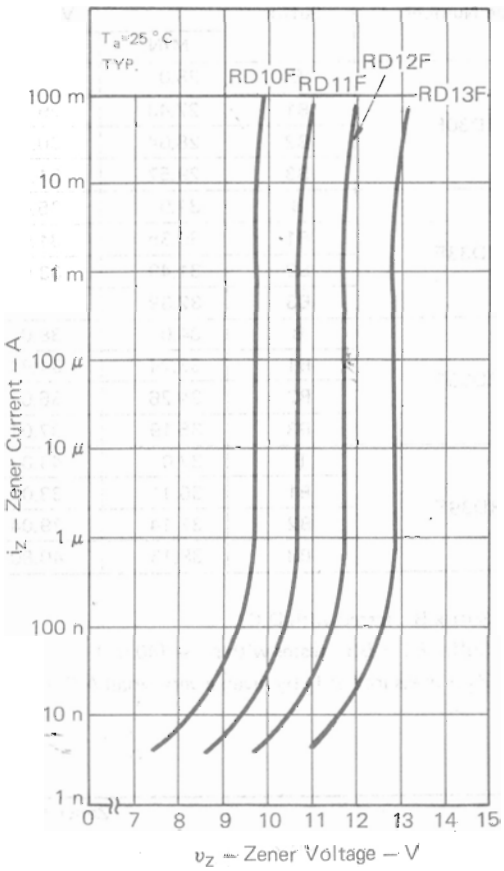
* tested with pulse (40 ms).

** Z_Z is measured at I_Z by given a very small A.C. current signal.

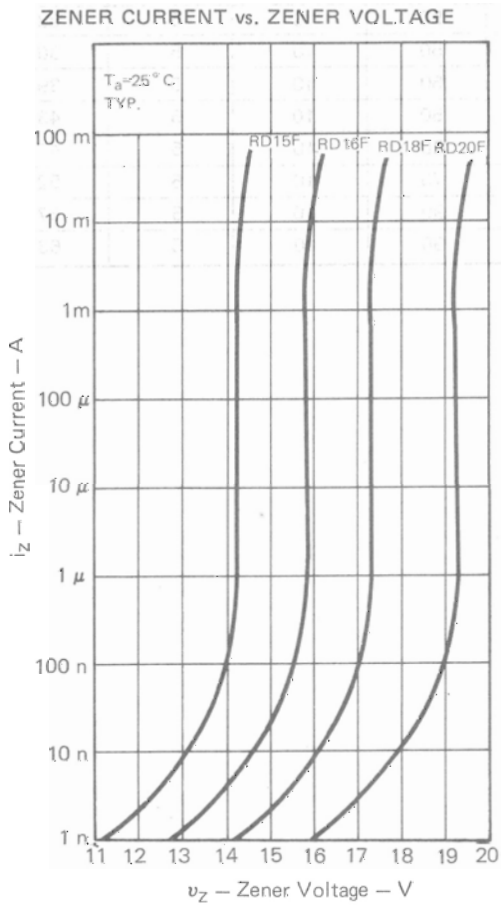
ZENER CURRENT vs. ZENER VOLTAGE



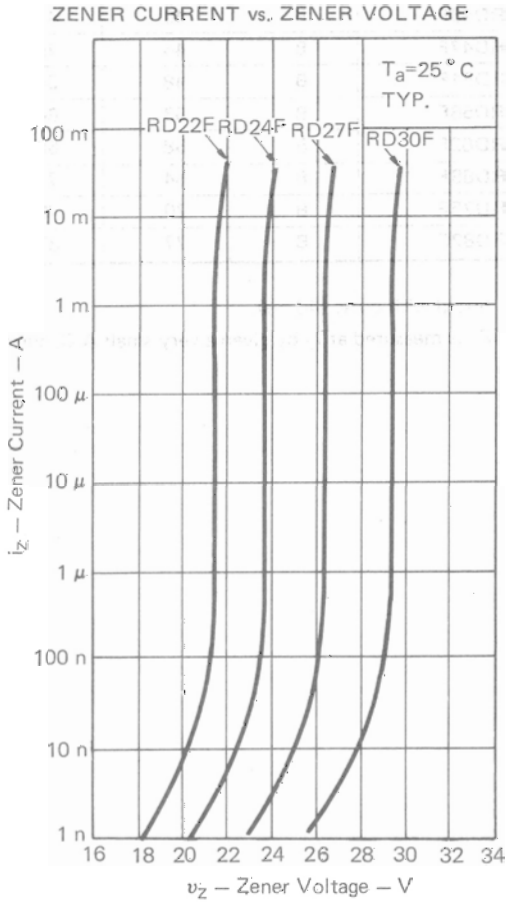
ZENER CURRENT vs. ZENER VOLTAGE



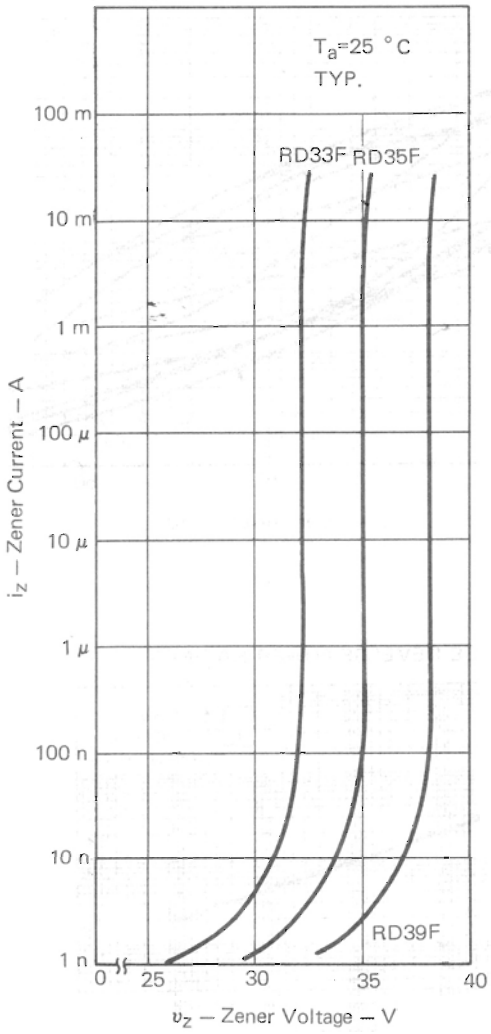
ZENER CURRENT vs. ZENER VOLTAGE



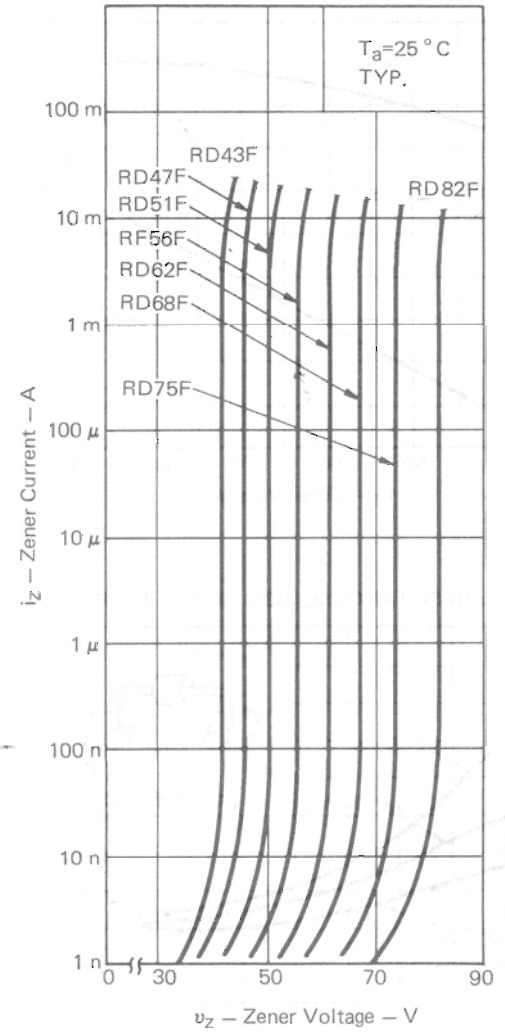
ZENER CURRENT vs. ZENER VOLTAGE



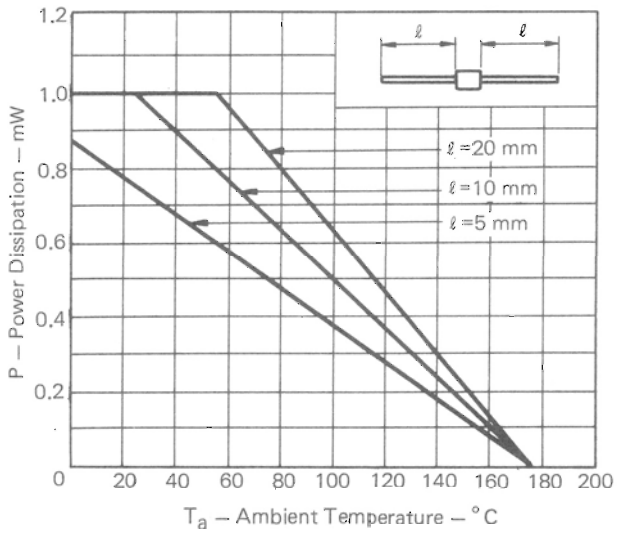
ZENER CURRENT vs. ZENER VOLTAGE



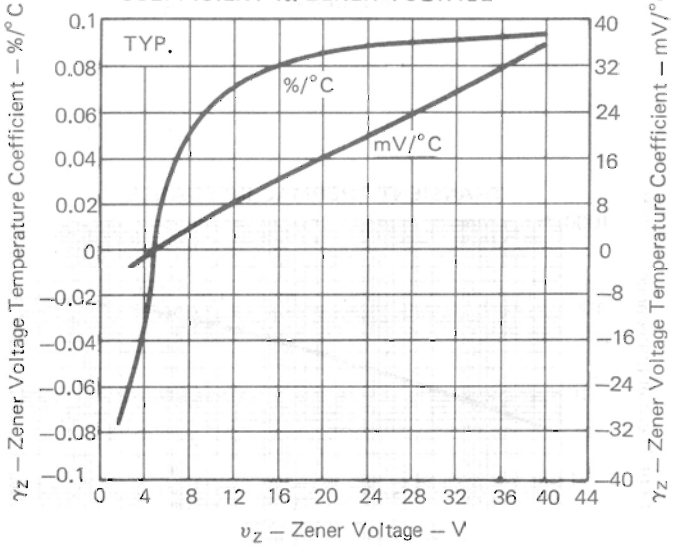
ZENER CURRENT vs. ZENER VOLTAGE



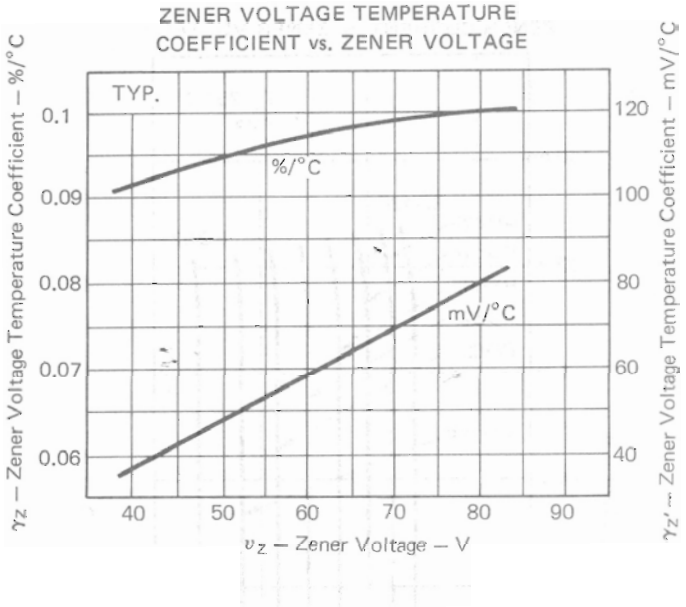
POWER DISSIPATION vs.
AMBIENT TEMPERATURE



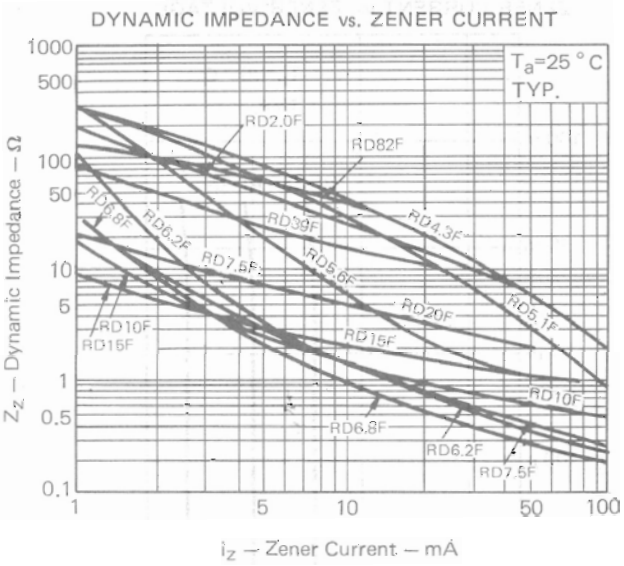
ZENER VOLTAGE TEMPERATURE
COEFFICIENT vs. ZENER VOLTAGE



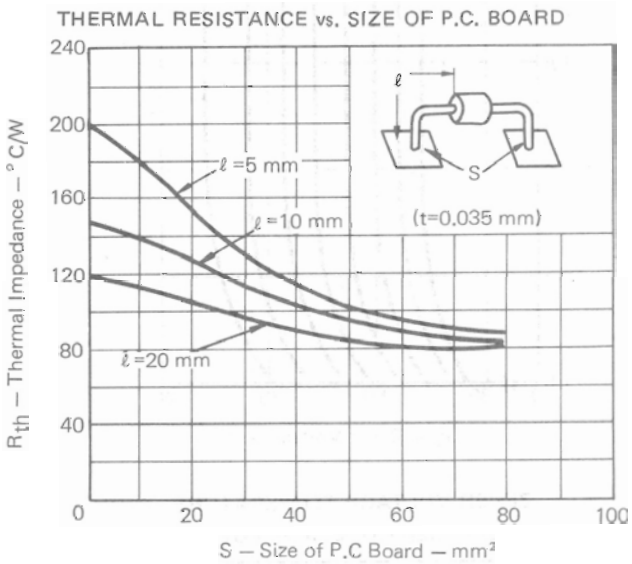
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



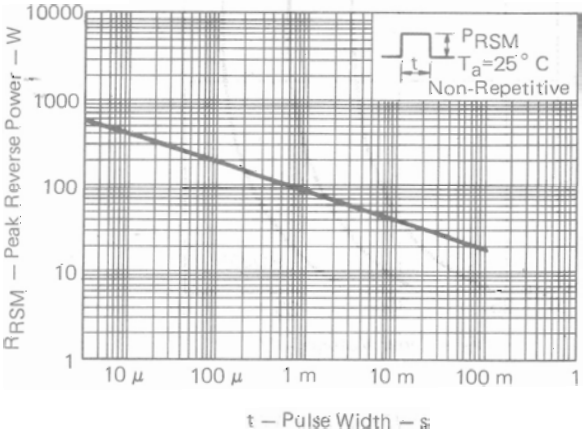
DYNAMIC IMPEDANCE vs. ZENER CURRENT



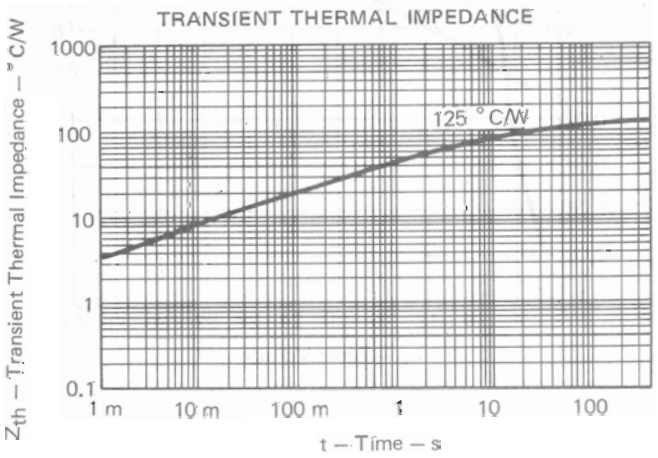
THERMAL RESISTANCE vs. SIZE OF P.C. BOARD



SURGE REVERSE POWER RATINGS



TRANSIENT THERMAL IMPEDANCE



NEC
ELECTRON DEVICE

LOW NOISE SHARP BREAKDOWN CHARACTERISTICS ZENER DIODE

RD4.7JS ~ RD39JS

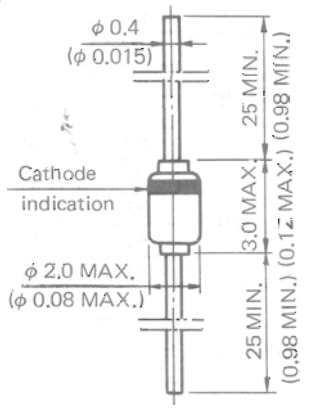
DESCRIPTION The RD4.7JS to RD39JS Series are
DHD (Double Heatsink Diode) construction
Mini Package (DO-34; Body length 3.0 mm Max.)
possessing an allowable power dissipation of 400 mW, featuring low noise, sharp breakdown characteristic.

FEATURES

- DO-34 Glass sealed package
- Low noise
- Sharp Breakdown characteristic
- DHD (Double Heatsink Diode) construction
- V_Z Applied E24 standard

APPLICATIONS Circuits for, Constant Voltage, Constant Current, Waveform clipper, etc.

PACKAGE DIMENSIONS
in millimeters (inches)



MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	175 °C
Storage Temperature	T_{stg}	−65 to +175 °C

Maximum Power Dissipation (T_a = 25 °C)

Power Dissipation	P	400 mW

ELECTRICAL CHARACTERISTICS (T_a = 25 ±2 °C)

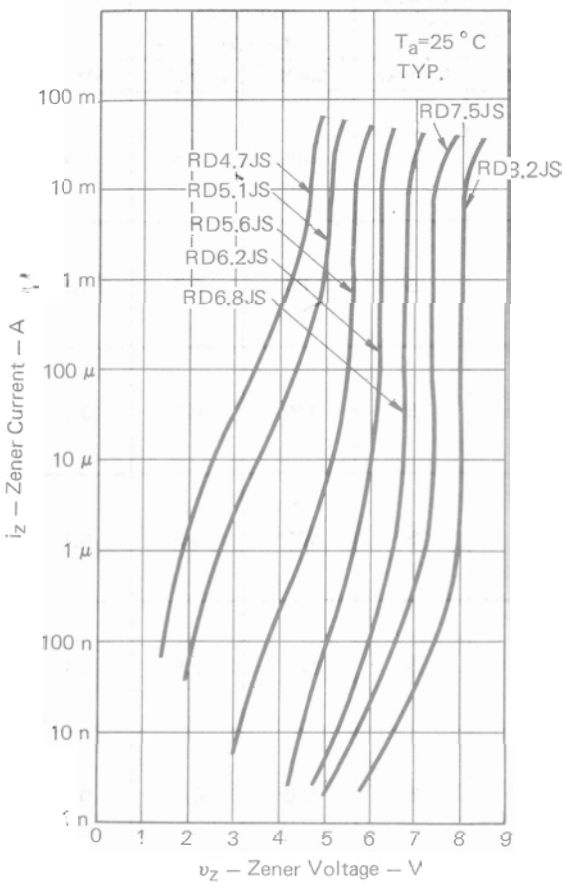
Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD4.7JS	B	4.42	4.90	5	100	5	800	0.5	2	1.0
	B1	4.42	4.61							
	B2	4.55	4.75							
	B3	4.69	4.90							
RD5.1JS	B	4.84	5.37	5	80	5	500	0.5	2	1.5
	B1	4.84	5.04							
	B2	4.98	5.20							
	B3	5.14	5.37							
RD5.6JS	B	5.31	5.92	5	60	5	200	0.5	1	2.5
	B1	5.31	5.55							
	B2	5.49	5.73							
	B3	5.67	5.92							
RD6.2JS	B	5.86	6.53	5	60	5	100	0.5	1	3.0
	B1	5.86	6.12							
	B2	6.06	6.33							
	B3	6.26	6.53							
RD6.8JS	B	6.47	7.14	5	40	5	60	0.5	0.5	3.5
	B1	6.47	6.73							
	B2	6.65	6.93							
	B3	6.86	7.14							
RD7.5JS	B	7.06	7.84	5	30	5	60	0.5	0.5	4.0
	B1	7.06	7.36							
	B2	7.28	7.60							
	B3	7.52	7.84							
RD8.2JS	B	7.76	8.64	5	30	5	60	0.5	0.5	5.0
	B1	7.76	8.10							
	B2	8.02	8.36							
	B3	8.28	8.64							
RD9.1JS	B	8.56	9.55	5	30	5	60	0.5	0.5	6.0
	B1	8.56	8.93							
	B2	8.85	9.23							
	B3	9.15	9.55							
RD10JS	B	9.45	10.55	5	30	5	60	0.5	0.1	7.0
	B1	9.45	9.87							
	B2	9.77	10.21							
	B3	10.11	10.55							
RD11JS	B	10.44	11.56	5	30	5	60	0.5	0.1	8.0
	B1	10.44	10.88							
	B2	10.76	11.22							
	B3	11.10	11.56							
RD12JS	B	11.42	12.60	5	30	5	80	0.5	0.1	9.0
	B1	11.42	11.90							
	B2	11.74	12.24							
	B3	12.08	12.60							
RD13JS	B	12.47	13.69	5	37	5	80	0.5	0.1	10
	B1	12.47	13.03							
	B2	12.91	13.49							
	B3	13.37	13.96							
RD15JS	B	13.84	15.52	5	42	5	80	0.5	0.1	11
	B1	13.84	14.46							
	B2	14.34	14.98							
	B3	14.85	15.52							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		K Knee Dynamic Impedance Z_{ZK} (Ω)		Reverse Current I_R (μ)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD16JS	B	15.37	17.09	5	50	5	80	0.5	0.1	12
	B1	15.37	16.01							
	B2	15.85	16.51							
	B3	16.35	17.09							
RD18JS	B	16.94	19.03	5	65	5	80	0.5	0.1	13
	B1	16.94	17.70							
	B2	17.56	18.35							
	B3	18.21	19.03							
RD20JS	B	18.86	21.08	5	85	5	100	0.5	0.1	15
	B1	18.86	19.70							
	B2	19.52	20.39							
	B3	20.21	21.08							
RD22JS	B	20.88	23.17	5	100	5	100	0.5	0.1	17
	B1	20.88	21.77							
	B2	21.54	22.47							
	B3	22.23	23.17							
RD24JS	B	22.93	25.57	5	120	5	120	0.5	0.1	19
	B1	22.93	23.96							
	B2	23.72	24.78							
	B3	24.54	25.57							
RD27JS	B	25.10	28.90	5	150	5	150	0.5	0.1	21
	B1	25.20	26.50							
	B2	26.19	27.53							
	B3	27.21	28.61							
RD30JS	B	28.00	32.00	5	200	5	200	0.5	0.1	23
	B1	28.22	29.66							
	B2	29.19	30.69							
	B3	30.20	31.74							
RD33JS	B	31.00	35.00	5	250	5	250	0.5	0.1	25
	B2	32.18	32.78							
	B2	32.15	33.79							
	B3	33.13	34.83							
RD36JS	B	34.00	38.00	5	300	5	300	0.5	0.1	27
	B1	34.12	35.86							
	B2	35.07	36.87							
	B3	36.07	37.91							
RD39JS	B	37.00	41.00	5	360	5	360	0.5	0.1	30
	B1	37.04	38.94							
	B2	38.00	39.94							
	B3	38.99	40.99							

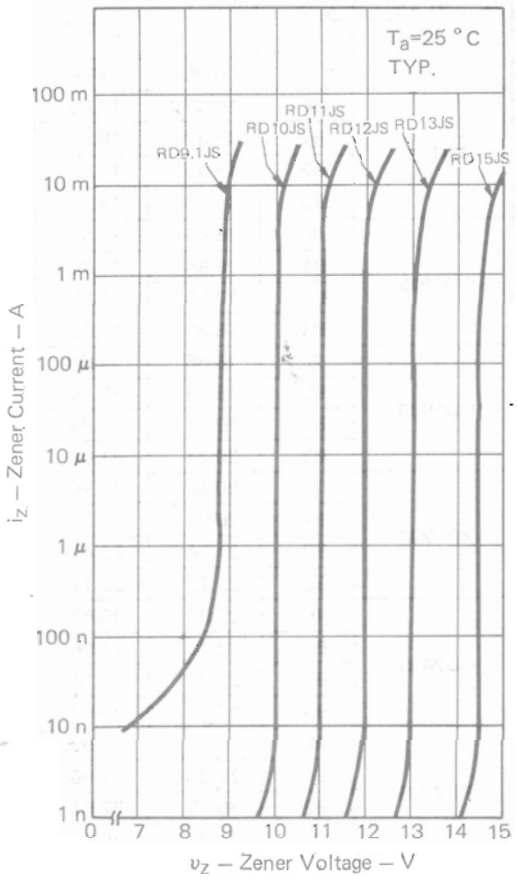
* tested with pulse (40 ms).

** Z_Z and Z_{ZK} are measured at I_Z by given a very small A.C. current signal.

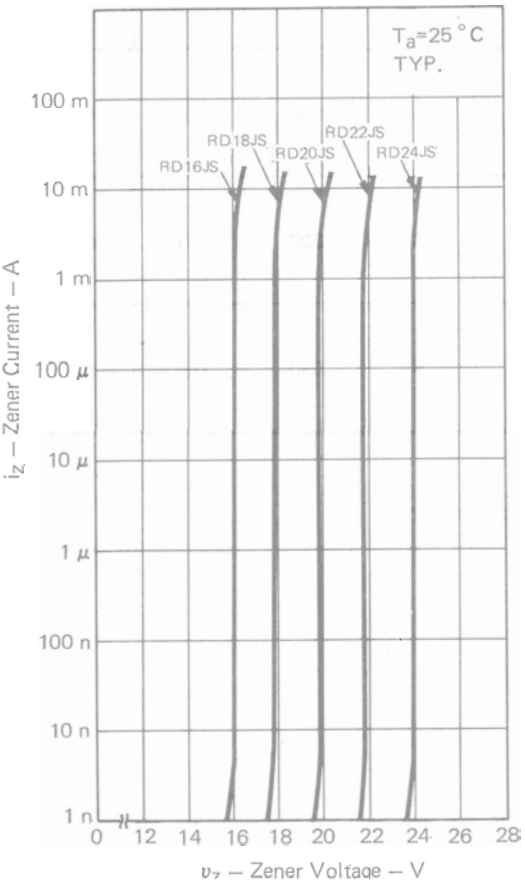
ZENER CURRENT vs. ZENER VOLTAGE



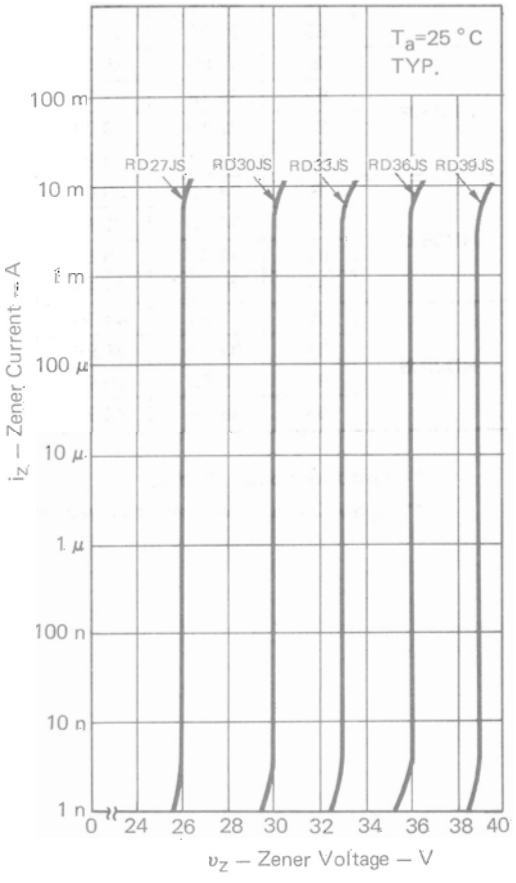
ZENER CURRENT vs. ZENER VOLTAGE



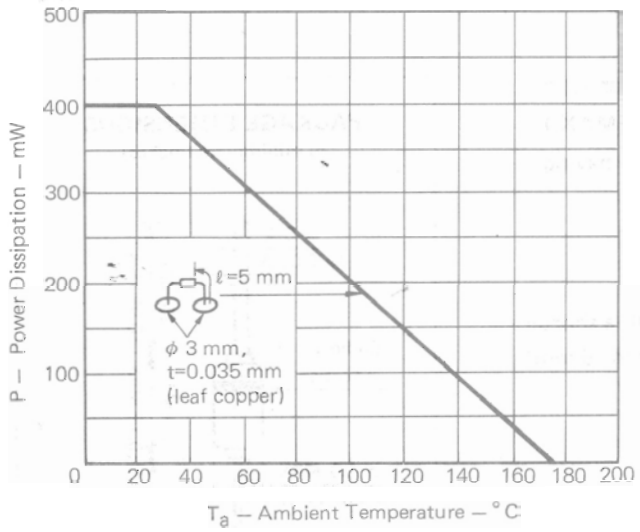
ZENER CURRENT vs. ZENER VOLTAGE



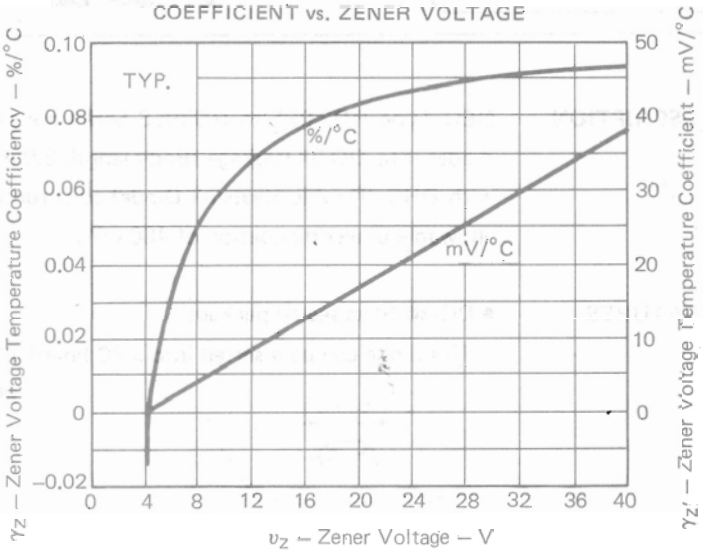
ZENER CURRENT vs. ZENER VOLTAGE



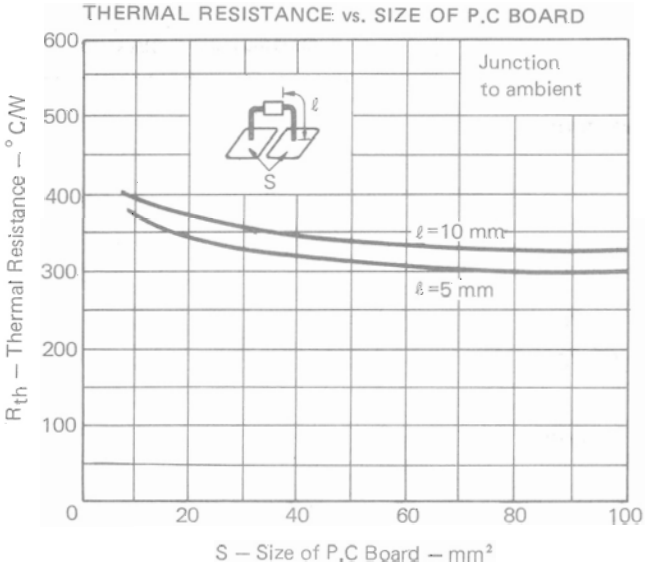
POWER DISSIPATION vs. AMBIENT TEMPERATURE



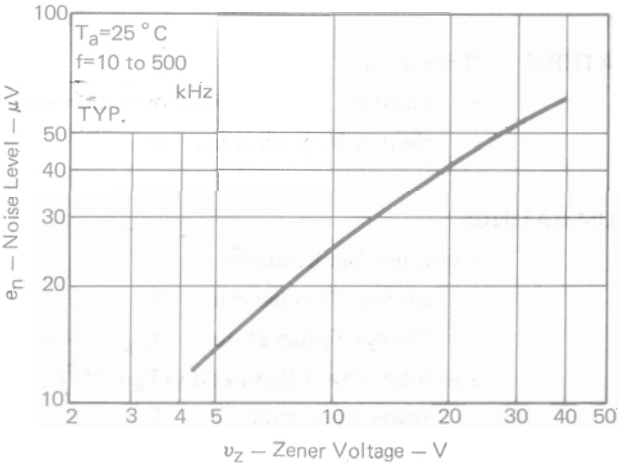
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs. ZENER VOLTAGE



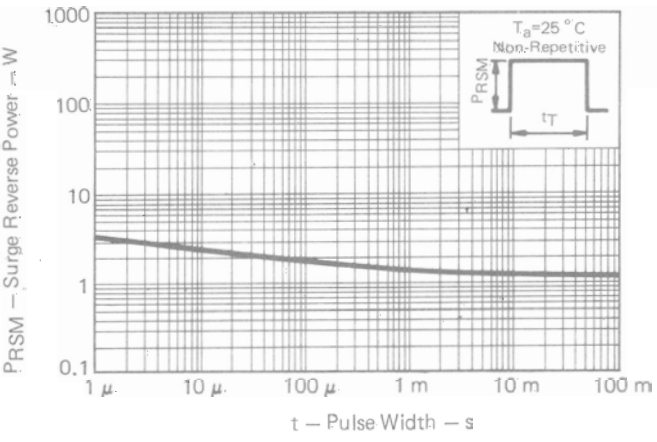
THERMAL RESISTANCE vs. SIZE OF P.C BOARD



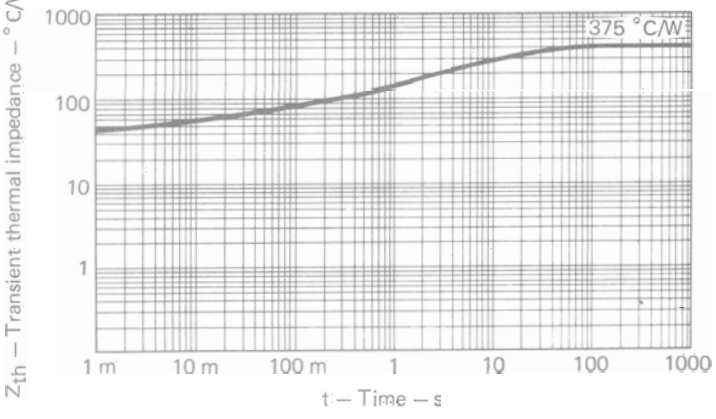
NOISE LEVEL vs. ZENER VOLTAGE



SURGE REVERSE POWER RATINGS



TRANSIENT THERMAL IMPEDANCE



NEC
ELECTRON DEVICE

ZENER DIODES

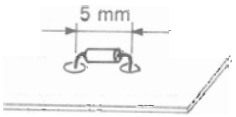
RD2.0ES to RD39ES

DESCRIPTION NEC Type RD2.0ES to RD39ES Series are planar type diodes into DO-34 Package (Body length 3.0 mm MAX.) with DHD (Double Heatsink Diode) construction having allowable power dissipation of 400 mW.

FEATURES

- DO-34 Glass sealed package

  This diode can be inserted into a PC board with a shorter pitch (5 mm)

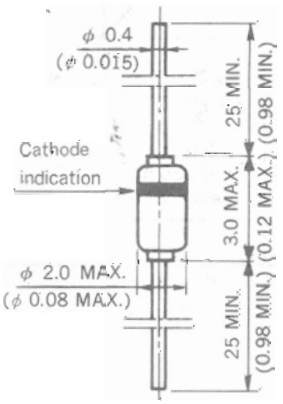


- Planar process
- DHD (Double Heatsink Diode) construction
- V_Z Applied E24 standard

APPLICATIONS Circuits for,

Constant Voltage, Constant Current, Wave form clipper, Surge absorber, etc.

PACKAGE DIMENSIONS
in millimeters (inches)



Marking color : Black

MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C

Maximum Power Dissipation (T_a = 25 °C)

Power Dissipation	P	400	mW

ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 2\ ^\circ C$)

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD2.0ES	B	1.88	2.20	5	100	5	1000	0.5	120	0.5
	B1	1.88	2.10							
	B2	2.02	2.20							
RD2.2ES	B	2.12	2.41	5	100	5	1000	0.5	120	0.7
	B1	2.12	2.30							
	B2	2.22	2.41							
RD2.4ES	B	2.33	2.63	5	100	5	1000	0.5	120	1.0
	B1	2.33	2.52							
	B2	2.43	2.63							
RD2.7ES	B	2.54	2.91	5	110	5	1000	0.5	100	1.0
	B1	2.54	2.75							
	B2	2.69	2.91							
RD3.0ES	B	2.85	3.22	5	120	5	1000	0.5	50	1.0
	B1	2.85	3.07							
	B2	3.01	3.22							
RD3.3ES	B	3.16	3.53	5	120	5	1000	0.5	20	1.0
	B1	3.16	3.38							
	B2	3.32	3.53							
RD3.6ES	B	3.47	3.83	5	120	5	1100	0.5	10	1.0
	B1	3.47	3.68							
	B2	3.62	3.83							
RD3.9ES	B	3.77	4.14	5	120	5	1200	0.5	5	1.0
	B1	3.77	3.98							
	B2	3.92	4.14							
RD4.3ES	B	4.05	4.53	5	120	5	1200	0.5	5	1.0
	B1	4.05	4.26							
	B2	4.20	4.40							
	B3	4.34	4.53							
RD4.7ES	B	4.47	4.91	5	100	5	1200	0.5	5	1.0
	B1	4.47	4.65							
	B2	4.59	4.77							
	B3	4.71	4.91							
RD5.1ES	B	4.85	5.35	5	70	5	1200	0.5	5	1.5
	B1	4.85	5.03							
	B2	4.97	5.18							
	B3	5.12	5.35							
RD5.6ES	B	5.29	5.88	5	40	5	900	0.5	5	2.5
	B1	5.29	5.52							
	B2	5.46	5.70							
	B3	5.64	5.88							
RD6.2ES	B	5.81	6.40	5	30	5	500	0.5	5	3.0
	B1	5.81	6.06							
	B2	5.99	6.24							
	B3	6.16	6.40							
RD6.8ES	B	6.32	6.97	5	25	5	150	0.5	2	3.5
	B1	6.32	6.59							
	B2	6.52	6.79							
	B3	6.70	6.97							
RD7.5ES	B	6.88	7.64	5	25	5	120	0.5	0.2	4.0
	B1	6.88	7.19							
	B2	7.11	7.41							
	B3	7.33	7.64							

Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)
RD8.2ES	B	7.56	8.41	5	20	5	120	0.5	0.5	5.0
	B1	7.56	7.90							
	B2	7.82	8.15							
	B3	8.07	8.41							
RD9.1ES	B	8.33	9.29	5	20	5	120	0.5	0.5	6.0
	B1	8.33	8.70							
	B2	8.61	8.99							
	B3	8.89	9.29							
RD10ES	B	9.19	10.30	5	20	5	120	0.5	0.2	7.0
	B1	9.19	9.59							
	B2	9.48	9.90							
	B3	9.82	10.30							
RD11ES	B	10.18	11.26	5	20	5	120	0.5	0.2	8.0
	B1	10.18	10.63							
	B2	10.50	10.95							
	B3	10.82	11.26							
RD12ES	B	11.13	12.30	5	25	5	110	0.5	0.2	9.0
	B1	11.13	11.63							
	B2	11.50	11.92							
	B3	11.80	12.30							
RD13ES	B	12.18	13.62	5	25	5	110	0.5	0.2	10
	B1	12.18	12.71							
	B2	12.59	13.16							
	B3	13.03	13.62							
RD15ES	B	13.48	15.02	5	25	5	110	0.5	0.2	11
	B1	13.48	14.09							
	B2	13.95	14.56							
	B3	14.42	15.02							
RD16ES	B	14.87	16.50	5	25	5	150	0.5	0.2	12
	B1	14.87	15.50							
	B2	15.33	15.96							
	B3	15.79	16.50							
RD18ES	B	16.34	18.30	5	30	5	150	0.5	0.2	13
	B1	16.34	17.06							
	B2	16.90	17.67							
	B3	17.51	18.30							
RD20ES	B	18.14	20.45	5	30	5	200	0.5	0.2	15
	B1	18.14	18.96							
	B2	18.80	19.68							
	B3	19.52	20.45							
RD22ES	B	20.23	22.61	5	30	5	200	0.5	0.2	17
	B1	20.23	21.08							
	B2	20.76	21.65							
	B3	21.22	22.09							
	B4	21.68	22.61							
RD24ES	B	22.26	24.81	5	35	5	200	0.5	0.2	19
	B1	22.26	23.12							
	B2	22.75	23.73							
	B3	23.29	24.27							
	B4	23.81	24.81							

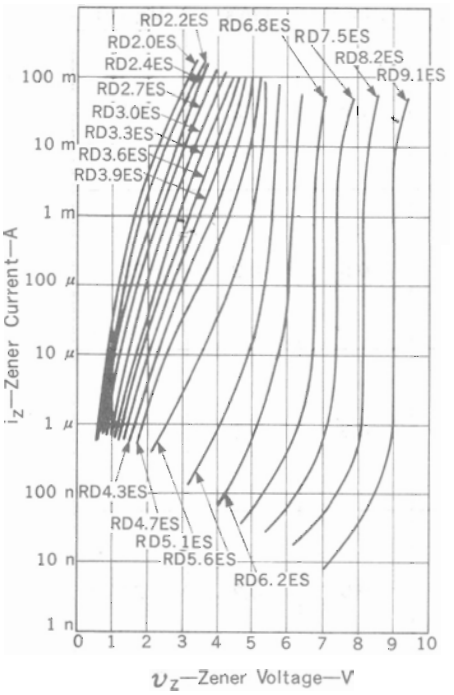
Type Number	Suffix	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Current I_R (μA)	
		MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	V_R (V)
RD27ES	B	24.26	27.64	5	45	5	250	0.5	0.2	21
	B1	24.26	25.52							
	B2	24.97	26.26							
	B3	25.63	26.95							
	B4	26.29	27.64							
RD30ES	B	26.99	30.51	5	55	5	250	0.5	0.2	23
	B1	26.99	28.39							
	B2	27.70	29.13							
	B3	28.36	29.82							
	B4	29.02	30.51							
RD33ES	B	29.68	33.11	5	65	5	250	0.5	0.2	25
	B1	29.68	31.22							
	B2	30.32	31.88							
	B3	30.90	32.50							
	B4	31.49	33.11							
RD36ES	B	32.14	35.77	5	75	5	250	0.5	0.2	27
	B1	32.14	33.79							
	B2	32.79	34.49							
	B3	33.40	35.13							
	B4	34.01	35.77							
RD39ES	B	34.68	38.52	5	85	5	250	0.5	0.2	30
	B1	34.68	36.47							
	B2	35.36	37.19							
	B3	36.00	37.85							
	B4	36.63	38.52							

* tested with pulse (40 ms).

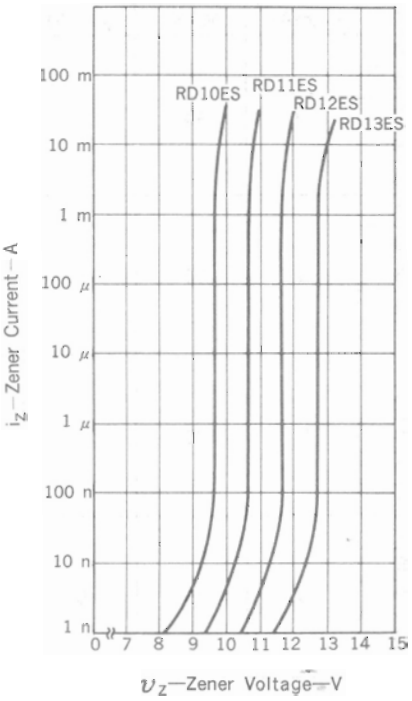
** Z_Z and Z_{ZK} are measured at I_Z by given a small A.C. current signal.

TYPICAL CHARACTERISTICS

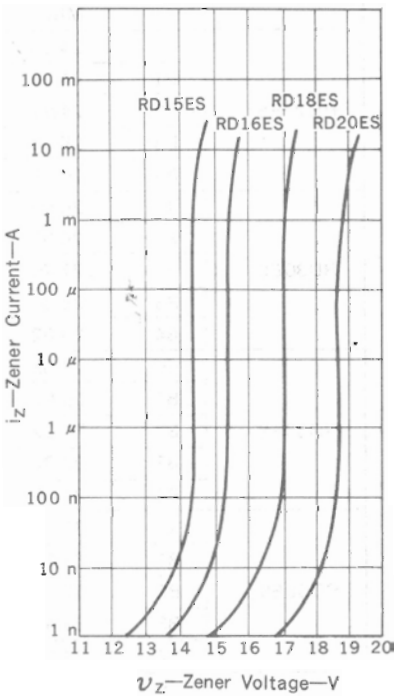
ZENER CURRENT vs. ZENER VOLTAGE



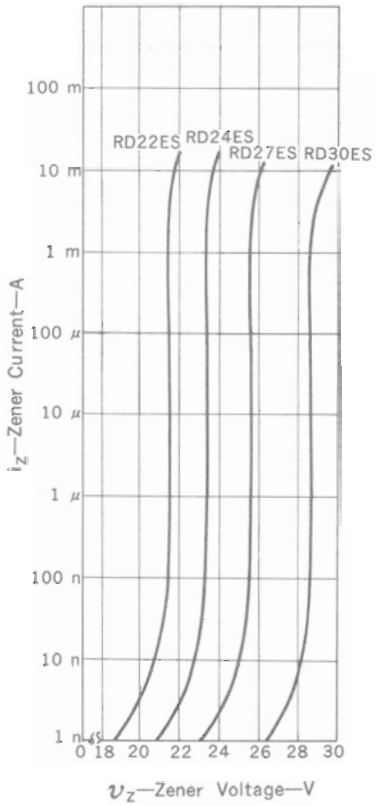
ZENER CURRENT vs. ZENER VOLTAGE



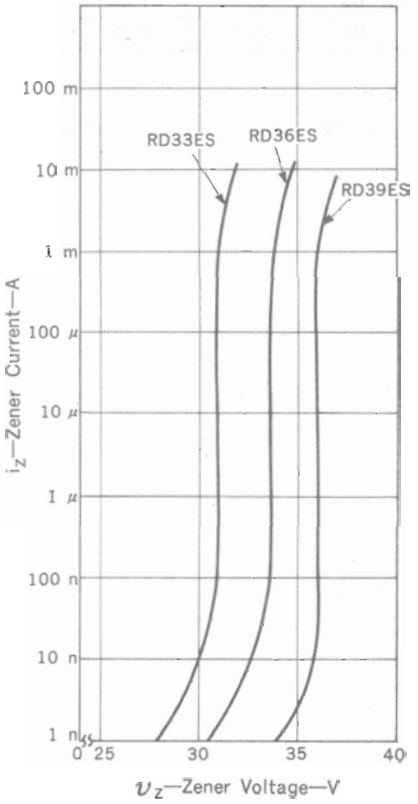
ZENER CURRENT vs. ZENER VOLTAG



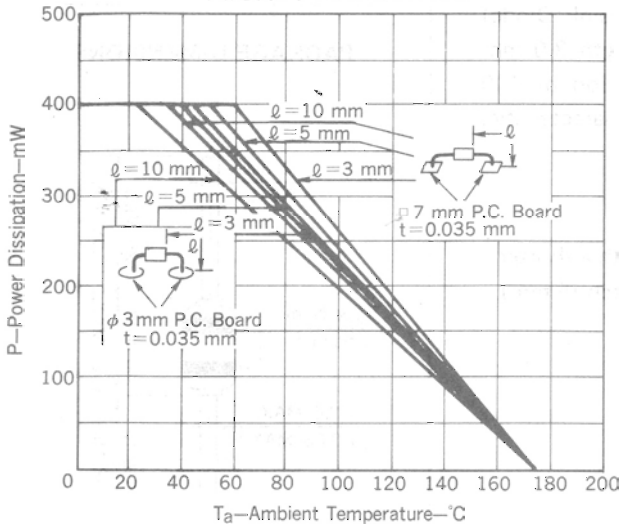
ZENER CURRENT vs. ZENER VOLTAGE



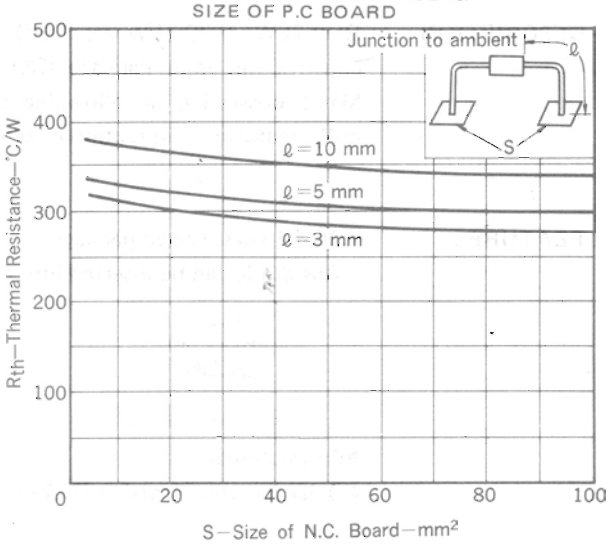
ZENER CURRENT vs. ZENER VOLTAGE



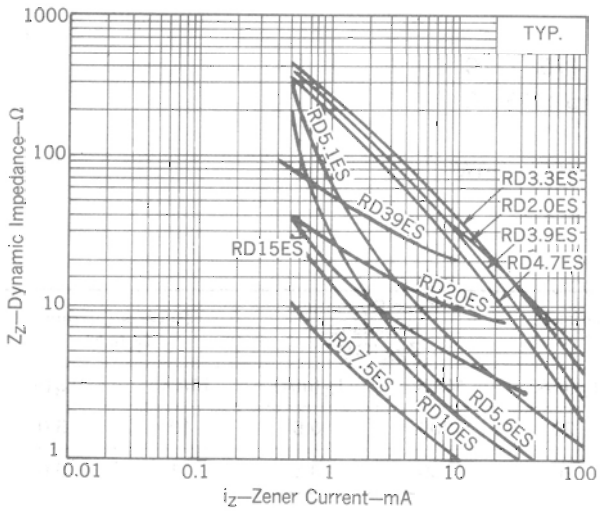
POWER DISSIPATION vs.
AMBIENT TEMPERATURE



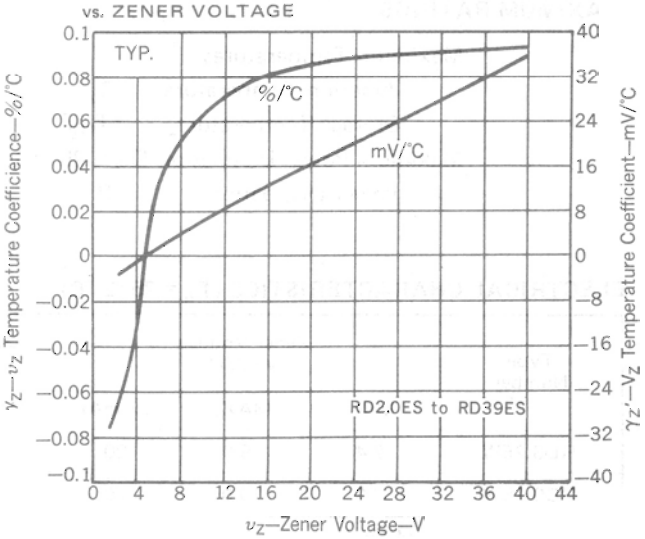
THERMAL RESISTANCE vs.
SIZE OF P.C BOARD



DYNAMIC IMPEDANCE vs.
ZENER CURRENT



ZENER VOLTAGE TEMPERATURE COEFFICIENT
vs. ZENER VOLTAGE



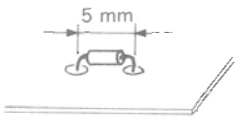
NEC
ELECTRON DEVICE

BIDIRECTIONAL ZENER DIODES
RD8.2EW, RD9.1EW

DESCRIPTION RD8.2EW, RD9.1EW are DHD (Double Heatsink Diode) construction Mini Package (DO-34: Body length 3.0 mm Max.) possessing an allowable power dissipation of 400 mW, featuring bidirectional zener voltage characteristic.

FEATURES

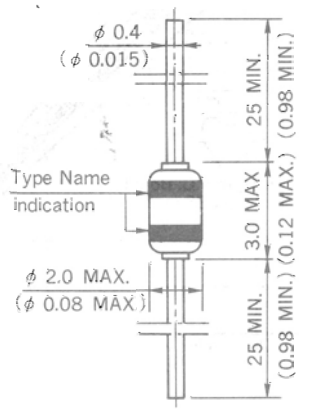
- DO-34 Glass sealed package
  This diode can be inserted into a PC board with a shorter pitch (5 mm)



- Bidirectional
- DHD (Double Heatsink Diode) construction

APPLICATIONS Circuit for Surge absorber, Limitter

PACKAGE DIMENSIONS



Color
RD8.2EW : Blue
RD9.1EW : Black

MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	175 °C
Storage Temperature	T_{stg}	−65 to +175 °C

Maximum Power Dissipation (T_a = 25 °C)

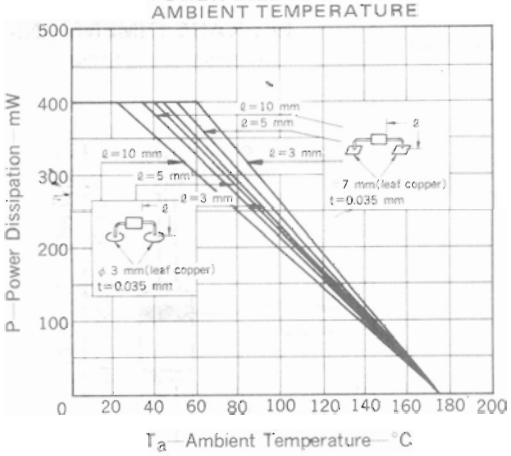
Power Dissipation	P	400 mW

ELECTRICAL CHARACTERISTICS (T_a = 25±2 °C)

Type Number	Zener Voltage V_Z(V)*			Dynamic Impedance $Z_Z(\Omega)$**		Knee Dynamic Impedance $Z_{ZK}(\Omega)$**		Reverse Current $I_R(\mu A)$	
	MIN.	MAX.	I_Z(mA)	MAX.	I_Z(mA)	MAX.	I_Z(mA)	MAX.	V_R(V)
RD8.2EW	7.4	9.0	20	8	20	300	0.5	10	5.0
RD9.1EW	8.2	10.0	20	8	20	150	0.5	1	6.0

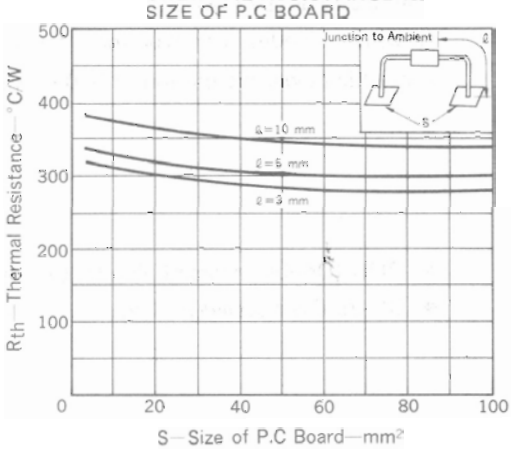
* Tested with pulse (40 ms)
** Z_Z & Z_{ZK} are measured at I_Z by given a very small A.C. current signal.

POWER DISSIPATION vs.
AMBIENT TEMPERATURE



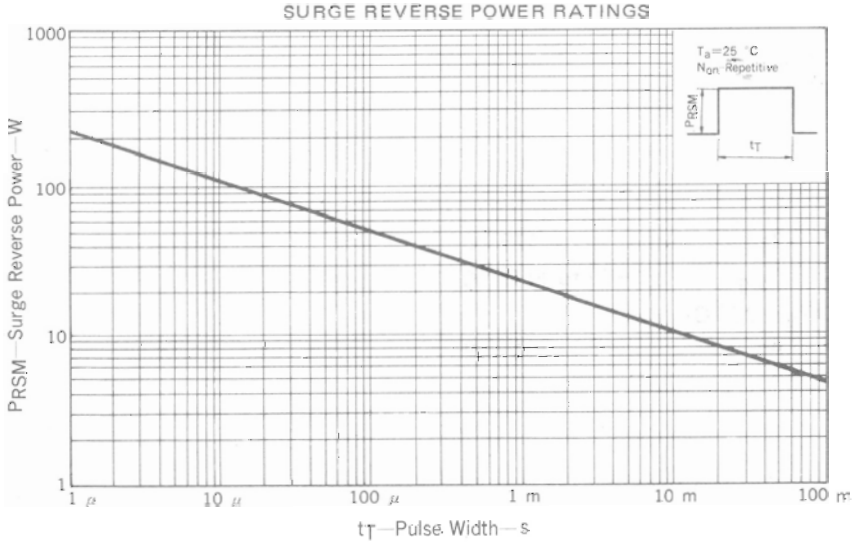
T_a—Ambient Temperature—°C

THERMAL RESISTANCE vs.
SIZE OF P.C BOARD



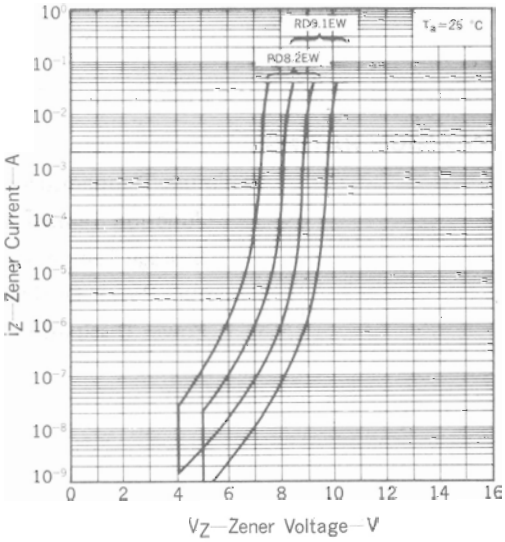
S—Size of P.C Board—mm²

SURGE REVERSE POWER RATINGS



tT—Pulse Width—s

ZENER CURRENT vs.
ZENER VOLTAGE



V_Z—Zener Voltage—V

NEC
ELECTRON DEVICE

ZENER DIODES

BZY88-C2V7 ~ BZY88-C33

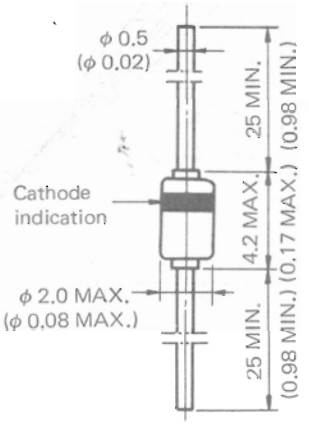
DESCRIPTION The BZY88-C2V7 to BZY88-C33 Series are DHD (Double Heatsink Diode) construction zener diodes possessing an allowable power dissipation of 500 m watt.

FEATURES

- DHD (Double Heatsink Diode) Construction
- DO-35 Glass sealed package

APPLICATIONS Circuits for, Constant voltage, Constant current, Waveform clipper, Surge absorber, etc.

PACKAGE DIMENSIONS
in millimeters (inches)



MAXIMUM RATINGS

Maximum Temperatures		
Junction Temperature	T_j	175 °C
Storage Temperature	T_{stg}	−65 to +175 °C
Maximum Power Dissipation (T_a = 25 °C)		
Power Dissipation	P	500 mW

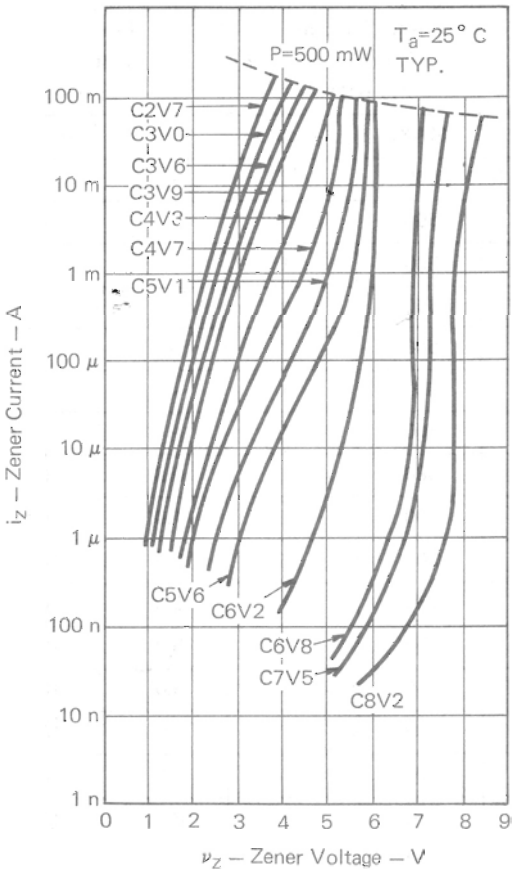
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

Type Number	Zener Voltage V_Z (V)*			Dynamic Impedance Z_Z (Ω)**		Knee Dynamic Impedance Z_{ZK} (Ω)**		Reverse Voltage V_R (V)	
	MIN.	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MAX.	I_Z (mA)	MIN.	I_R (nA)
BZY88-C2V7	2.5	2.9	5	83	5	500	1	–	–
BZY88-C3V0	2.8	3.2	5	90	5	500	1	–	–
BZY88-C3V3	3.1	3.5	5	90	5	500	1	–	–
BZY88-C3V6	3.4	3.8	5	90	5	500	1	–	–
BZY88-C3V9	3.7	4.1	5	90	5	500	1	–	–
BZY88-C4V3	4.0	4.6	5	90	5	500	1	–	–
BZY88-C4V7	4.4	5.0	5	78	5	500	1	–	–
BZY88-C5V1	4.8	5.4	5	60	5	480	1	0.8	100
BZY88-C5V6	5.2	6.0	5	40	5	400	1	1.0	100
BZY88-C6V2	5.8	6.6	5	10	5	200	1	2.0	100
BZY88-C6V8	6.4	7.2	5	8	5	150	1	3.0	100
BZY88-C7V5	7.0	7.9	5	7	5	50	1	5.0	100
BZY88-C8V2	7.7	8.7	5	7	5	50	1	6.0	100
BZY88-C9V1	8.5	9.6	5	10	5	50	1	7.0	100
BZY88-C10	9.4	10.6	5	15	5	70	1	7.5	100
BZY88-C11	10.4	11.6	5	20	5	70	1	8.5	100
BZY88-C12	11.4	12.7	5	20	5	90	1	9.0	100
BZY88-C13	12.4	14.1	5	25	5	110	1	10.0	100
BZY88-C15	13.8	15.6	5	30	5	110	1	11.0	100
BZY88-C16	15.3	17.1	5	40	5	170	1	12.0	100
BZY88-C18	16.8	19.1	5	50	5	170	1	14.0	100
BZY88-C20	18.8	21.2	5	50	5	220	1	15.0	100
BZY88-C22	20.8	23.3	5	55	5	220	1	17.0	100
BZY88-C24	22.8	25.6	5	80	5	220	1	18.0	100
BZY88-C27	25.1	28.9	5	80	5	250	1	20.0	100
BZY88-C30	28.0	32.0	5	80	5	250	1	22.5	100
BZY88-C33	31.0	35.0	5	80	5	250	1	25.0	100

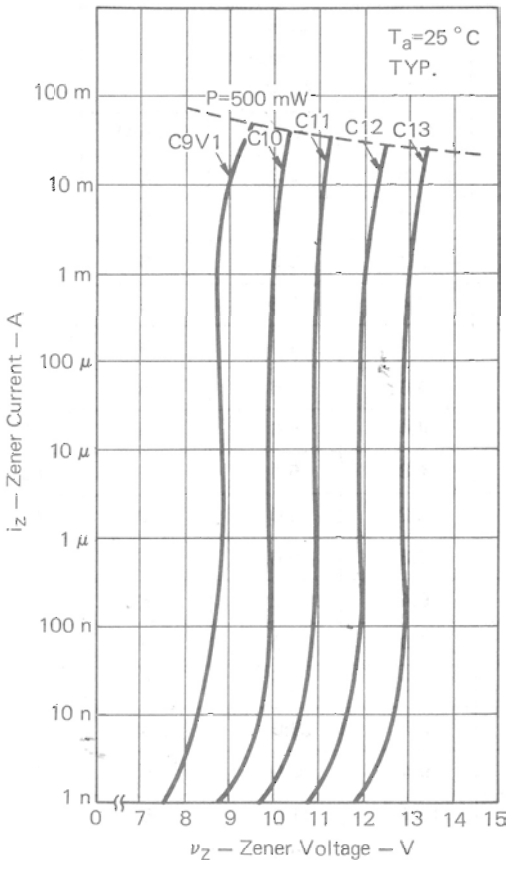
* tested with DC.

** Z_Z and Z_{ZK} are measured at I_Z by given a very small A.C. current signal.

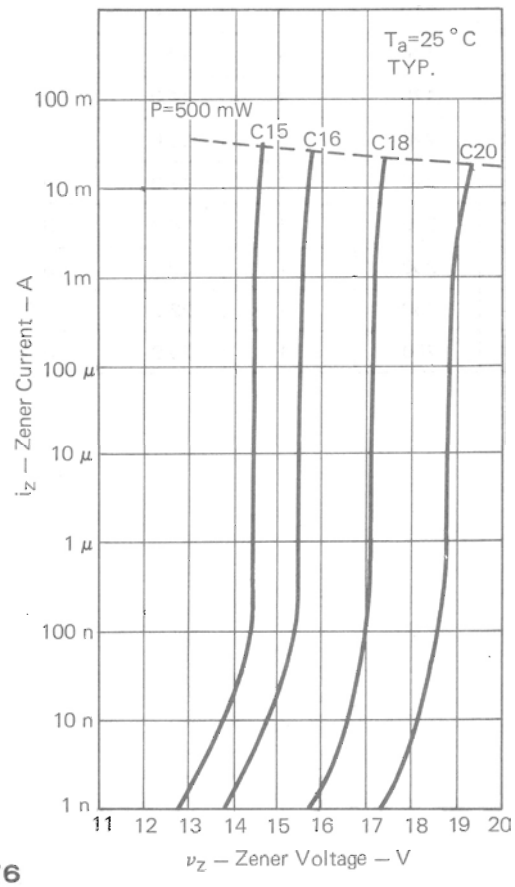
ZENER CURRENT vs. ZENER VOLTAGE



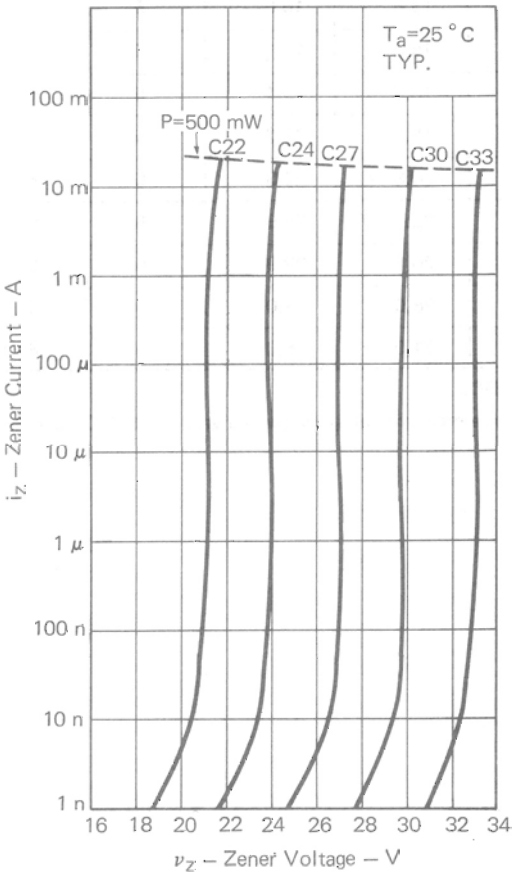
ZENER CURRENT vs. ZENER VOLTAGE



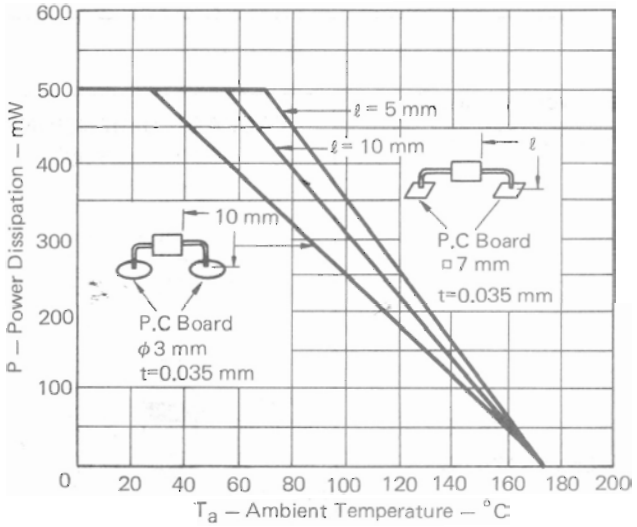
ZENER CURRENT vs. ZENER VOLTAGE



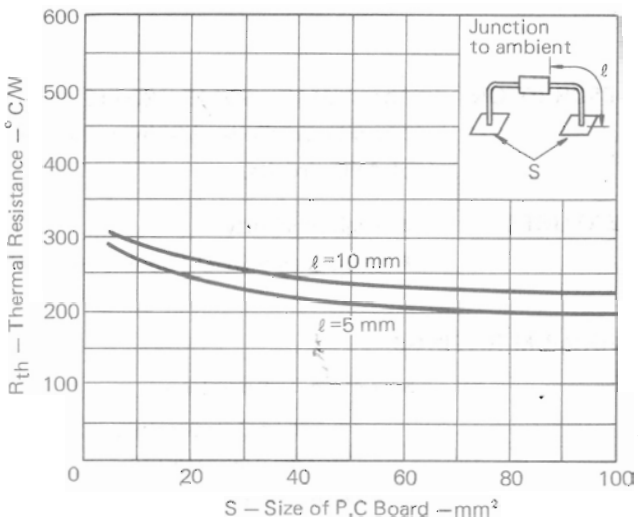
ZENER CURRENT vs. ZENER VOLTAGE



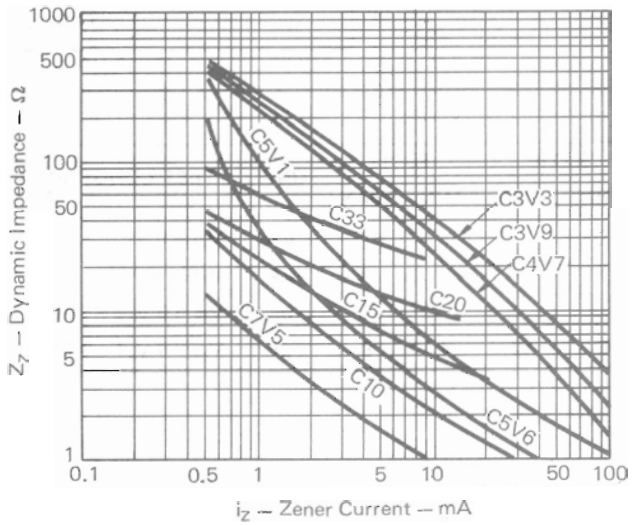
POWER DISSIPATION vs.
AMBIENT TEMPERATURE



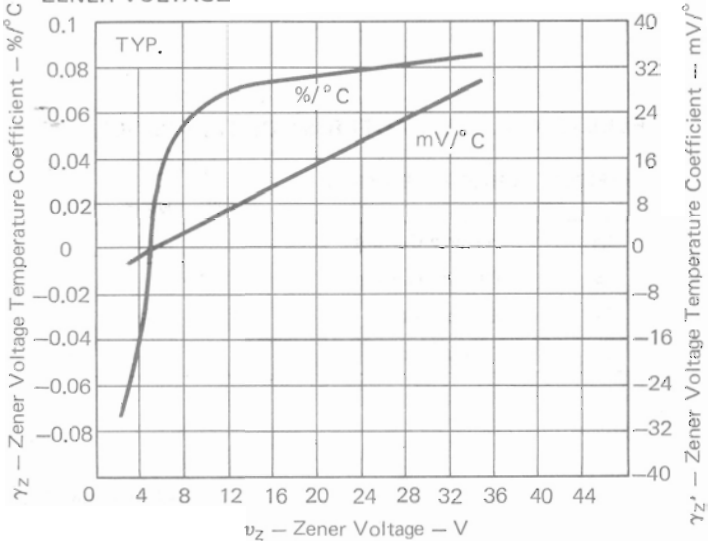
THERMAL RESISTANCE vs.
SIZE OF P.C BOARD



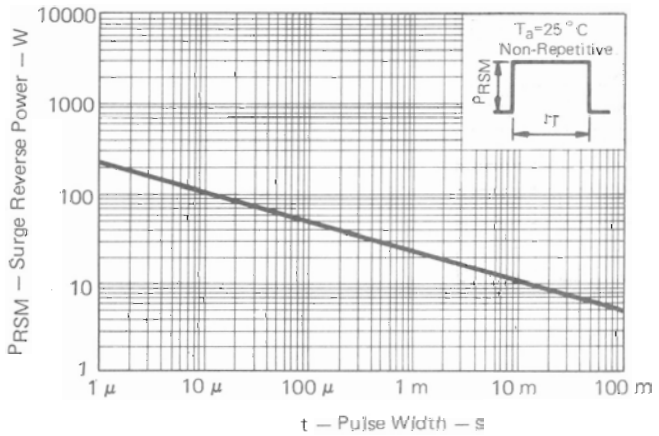
DYNAMIC IMPEDANCE vs.
ZENER CURRENT



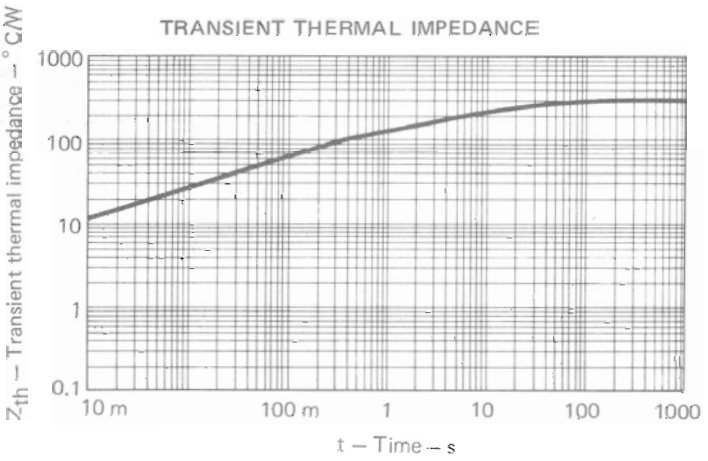
ZENER VOLTAGE TEMPERATURE COEFFICIENT vs.
ZENER VOLTAGE



SURGE REVERSE POWER RATINGS



TRANSIENT THERMAL IMPEDANCE



NEC
ELECTRON DEVICE

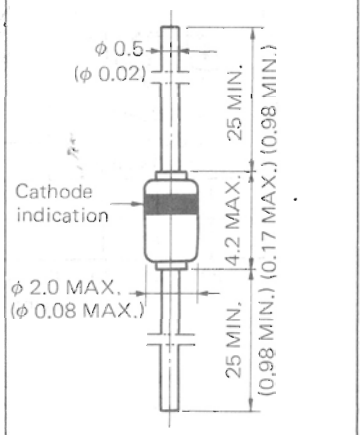
VARICAP DIODES
SD113,SD115,SD116,SD117

DESCRIPTION The SD113, SD115, SD116 and SD117 are voltage-variable capacitance diodes ideally suited to applications for FM tuners of AFC circuits.

FEATURES

- High reliability
- Glass sealed DHD (Double Heatsink Diode)

PACKAGE DIMENSIONS
in millimeters (inches)



MAXIMUM RATINGS

Maximum Temperatures

Junction Temperature	T_j	175 °C
Storage Temperature	T_{stg}	−65 to +175 °C

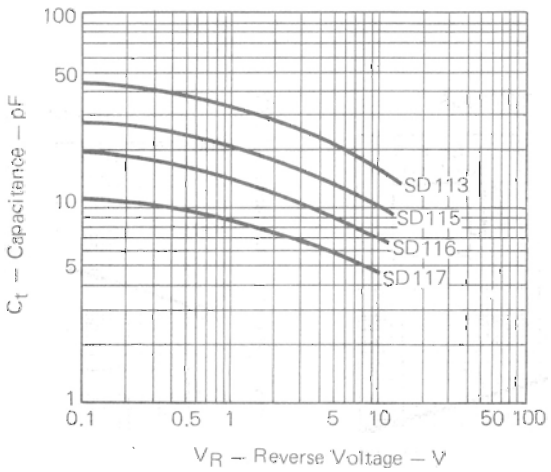
Maximum Voltages and Currents (T_a = 25 °C)

		SD113	SD115 to SD117	
Peak Reverse Voltage	V_{RM}	10	15	V
DC Reverse Voltage	V_R	5	10	V

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	SD113		SD115		SD116		SD117		UNIT	TEST CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
I_R	Reverse Current		0.1							μA	V_R = 5 V
I_R	Reverse Current				1		1		1	μA	V_R = 10 V
C_t	Capacitance	35	55							pF	V_R = 0 V, f = 1 MHz
C_t	Capacitance			10	16	6	12	4	8	pF	V_R = 4 V, f = 1 MHz

CAPACITANCE vs. REVERSE VOLTAGE



ENGINEERING NOTES

TECHNICAL NOTES

BLOCK DIAGRAM FOR ENTERTAINMENT EQUIPMENT

APPLICATION NOTES

ENGINEERING INDEX

TECHNICAL NOTES

BIASING OF TRANSISTORS 1081
HIGH FREQUENCY SMALL SIGNAL CIRCUIT DESIGN 1098
THE USE OF SAFE OPERATING AREA 1103
4 V GATE-DRIVEN POWER MOS FET WITH LOW DRAIN-TO-SOURCE ON STATE RESISTANCE 1109
h_{FE} AND NOISE FIGURE DETERIORATION CAUSED BY E-B JUNCTION BREAKDOWN IN TRANSISTORS 1117
TRANSISTORS WITH EXCELLENT IN "ELECTROSTATIC-DISCHARGE-RESISTANT (ESDR)" 1123
CAUTIONS TO BE TAKEN IN MEASUREMENT AND TESTING OF TRANSISTOR 1129
OPTIMUM METHOD OF USE OF LOW FREQUENCY-LOW NOISE TRANSISTOR 1131
NEC'S ELECTRONIC TUNING VARACTOR DIODES 1137
ZENER DIODE RD[ ]JS, RD[ ]E, RD[ ]F CHARACTERISTICS & RELIABILITY 1143

BLOCK DIAGRAM FOR ENTERTAINMENT EQUIPMENT

1. RADIO RECEIVER 1166
2. TAPE RECORDER 1167
3. RADIO CONTROL SYSTEM FOR TOYS 1168
4. PURE COMPLEMENTARY P-P AMPLIFIER 1170
5. PURE COMPLEMENTARY DARLINGTON SEPP AMPLIFIER 1171
6. VHF/UHF TV SET 1173
7. OTHER EQUIPMENT 1176

APPLICATION NOTES

EXAMPLE OF Po=3 W PURE COMPLEMENTARY OTL AUDIO POWER AMPLIFIER CIRCUIT USING JE9000 SERIES 1178
TYPICAL AUDIO AMPLIFIER WITH A CONTINUOUS OUTPUT POWER OF 10 W 1182
TYPICAL MAIN AMPLIFIER WITH A CONTINUOUS OUTPUT POWER OF 20 W 1190
TYPICAL APPLICATION OF 3SK74 TO VHF TUNER RF AMPLIFIER 1192
TYPICAL APPLICATION OF 3SK74 TO VHF TUNER MIXER 1198
TYPICAL APPLICATION OF 3SK87 TO UHF TUNER RF AMPLIFIER 1203
TYPICAL APPLICATION OF 3SK88 TO UHF TUNER RF AMPLIFIER 1213
TYPICAL APPLICATION OF 2SC2352 TO VHF TUNER MIXER CIRCUIT OF HIGH CONVERSION GAIN 1219
TYPICAL APPLICATION OF 2SC2353 FOR UHF TV TUNER MIXER 1225
HIGH FREQUENCY LOW-NOISE TRANSISTORS FOR VHF AND UHF BAND APPLICATIONS .. 1229
PLASTIC MOLD-PACKAGED LOW-NOISE MICROWAVE TRANSISTORS FOR CONSUMER MICROWAVE APPLICATIONS 1245
NEC PIN DIODES AND APPLICATIONS 1264
DOUBLE BALANCED MIXER USING NEC'S SCHOTTKY BARRIER DIODE 1SS97 OR 1SS99 1275
NEC'S SCHOTTKY BARRIER DIODE QUAD AND APPLICATIONS (ND487 Series) 1281
CHARACTERSITICS OF 2 GHz BAND MIXER USING 1SS97, 1SS98 AND 1SS99 1291

BIASING OF TRANSISTORS

1. BASIC BIASING CIRCUIT

The biasing of transistor circuits is liable to shifts due to environmental condition changes and the range of allowed biasing is narrower than that of vacuum tube circuits. Thus as the biasing of transistor circuits is a common and basic problem in various transistor applications. This document deals with the essential matters related to this biasing.

1.1 What Biasing Means

With zero voltage between base and emitter, the application of normal collector voltage (positive for NPN type and negative for PNP type) induces no collector current except a very small amount of leakage current. That means that, with zero biasing between base and emitter, the transistor works only when a certain forward voltage is applied to the base and the collector current can flow during half cycle of signal as shown in Fig. 1 to result in C-class operation. Whereas in vacuum tube circuits, the zero-biased circuit works as shown in Fig. 2 and a certain plate current flows even without biasing. Normally the A-class operation of a vacuum tube circuit is provided with a negative bias voltage $-V_G$ at the control grid. This negative biasing is applied for preventing the grid current from flowing. The value $-V_G$ is so determined that the plate current flows through the entire cycle and the grid voltage never reaches a positive value. This is shown in Fig. 3, where the bias voltage $-V_G$ is located nearly the middle point of I_{p}-V_g characteristic curve and the operation center is shifted to the negative side by $-V_G$.

Since no collector current flows in a zero-biased transistor, it is necessary to apply a slight forward voltage across the base-emitter junction in order to obtain the collector current for a whole cycle of input signal. i.e., it is the application of a forward bias voltage V_{BE} between the base and the emitter. In transistor circuits, contrasted to its vacuum tube counter part, the operation point is shifted by V_{BE} until a sufficient amount of collector current flows and the input signals are superimposed on the bias voltage. Forward bias voltages for germanium transistors and silicon transistors are 0.1 through 0.2 V and 0.6 through 0.7 V, respectively, as shown in examples in Fig. 4.

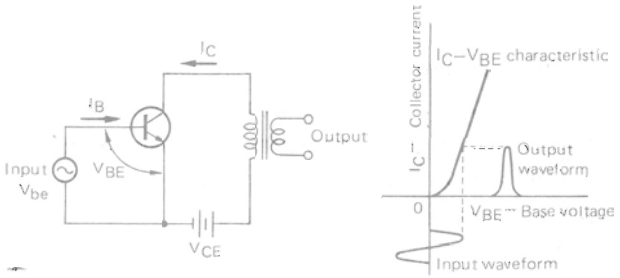


Fig. 1 Operational Description of Transistor at Zero Biasing.

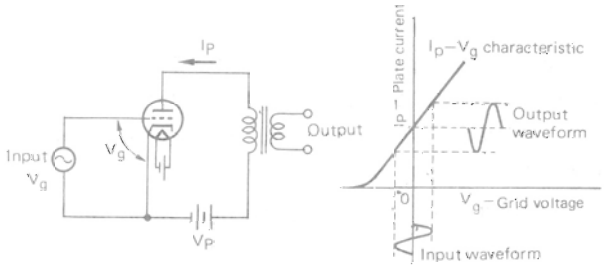


Fig. 2 Operational Description of Vacuum Tube at Zero Biasing.

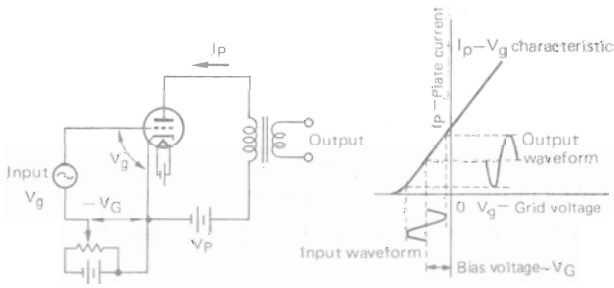


Fig. 3 A-class Operation of Vacuum Tube Circuit with a Bias Voltage– V_G.

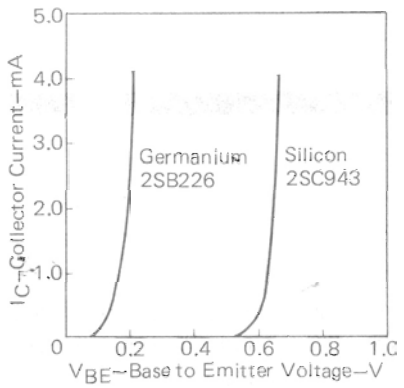


Fig. 4 V_{BE}'s for a Germanium Transistor and for a Silicon Transistor.

The forward biasing of base-emitter junction means the application of base voltage positive to the emitter for an NPN transistor and negative to the emitter for a PNP transistor, respectively. Fig. 5 shows an example of NPN transistor.

Since the input resistance of a transistor is small, the application of forward bias voltage V_{BE} between the base and the emitter makes the base current (I_B) flow and the collector current (I_C), which is h_{FE} times I_B, flow through the collector circuit. Consequently the emitter current (I_E), which is nearly the same as I_C, will flow through the emitter circuit. h_{FE} is the common-emitter current gain of a transistor.

Therefore, either of a particular value of V_{BE}, I_B, I_C, or I_E may be defined as the transistor bias. Usually, collector current (I_C) or emitter current (I_E) is considered to be the typical bias.

Transistor characteristics are not as drastically influenced by collector voltage as by collector current. However, voltage V_{CB} between collector and base or voltage V_{CE} between collector and emitter is still frequently regarded as one of biasing conditions.

On most transistor data sheets which describe characteristics and specifications, the biasing conditions are voltage V_{CB} or V_{CE} and current I_C or I_E.

1.2 Optimum Bias Point

The amount of bias voltage or of collector current necessary for operating a transistor depends upon the type of transistor operation, as described below.

(1) For C-class amplification, no special biasing circuit is needed in principle.

(2) For B-class amplification, the transistor should be biased up to the rise point of I_C-V_{BE} characteristic curve.

(3) For A-class amplification, the transistor should be forward biased for beyond the rise point of I_C-V_{BE} characteristic curve so that the appropriate amount of collector current flows when no input signal is applied.

These modes are shown in Fig. 6.

Consider, the A-class small signal amplification which is the most basic operation of a transistor. The biasing condition may, from the standpoint of the maximum gain, be the choice of collector current at which h_{fe} is the maximum, where h_{fe} is the common emitter small-signal current gain, However, actually restricted by other conditions such as heating-up of a transistor, the use in the range of 0.5 through 3 mA is normal. Conversely, transistor makers design their transistors in such a manner that, when used as small-signal, A-class amplifier transistors, h_{fe} will acheive the maximum value at a collector current of a few milliamperes. When high input impedance or low noise is desired, sometimes the collector current is made as small as a few tens of microamperes at the sacrifice of gain. These transistors having h_{fe} of 100 through 200 at the collector current of a few tens of microamperes will frequently show h_{fe} of 500 through 1,000 at a few milliamperes.

Since transistor characteristics are not largely influenced by collector voltage, the voltage is usually settled to several volts for the convenience of battery or power supply.

When a fairly large output power is needed as in a driver stage, the bias point should be large enough to be matched to the output power even in an A-class operation. Therefore, in such a case, it is necessary to choose a transistor with sufficiently large h_{fe} at the bias point and for the signal swing.

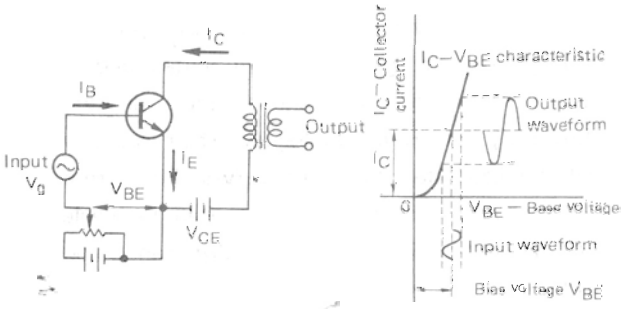


Fig. 5 Biasing of NPN Transistor.

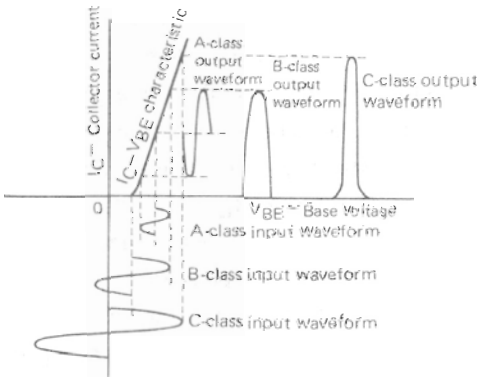


Fig. 6 Bias Points for Typical Operations.

In B-class push-pull operation for low-frequency and large output, the biasing up to the cutoff point of I_C-V_{BE} characteristics curve is only needed in theory and no collector current flow is required when no signal is applied, actually, in order to reduce nonlinear distortion in small current region, a slight amount of collector current is used for the biasing when no signal is applied. This current is called no-signal bias current or idling current.

When a particular transistor and a class of its operation is chosen, the appropriate collector current as the biasing means depends primarily upon signal level and power level and secondly upon the transistor characteristics. Some transistors need high collector current and others need less for their optimum operations. The collector current at which a transistor works optimally has been determined by the transistor maker who has designed the transistor to be used at various signal and power levels.

Fig. 7 shows the h_{FE} impact of various transistors upon collector current I_C. Transistors of grown junction type which is fairly classic example exhibit a fast rise up in the small current region and the maximum point can be put at 1 through 2 mA. But they are by no means suitable for high current use. Transistors of alloy junction and diffusion junction types can be designed to put the maximum point fairly close to the desired value by choosing an appropriate electrode area. So they can be designed for different uses including small signal, medium power, and high power uses. For small signal use, the rapid rise in small current range is fully utilized, whereas the decrease of h_{FE} in large current region is considered nonessential. For high power applications, the small h_{FE} decrease in large current region as well as the possibility of a high collector current is essential whereas the slow rise in small current region may be forgiven. Therefore, transistors for high power use often do not present good characteristics in small current region. "The larger, the better" is not necessarily true. Furthermore, h_{FE} of a transistor becomes maximum at a certain value of collector current and beyond that point it decreases with the increasing collector current. This is the reason why biasing of a transistor at a small current tends to result in the increase of distortion.

In reality, the biasing condition of a transistor circuit are often affected by the power supply (i.e. the type and number of batteries and the common use of a supply with other devices) rather than determined at the optimum point of transistor operation. In an A-class small signal amplification, the bias current of about 1 mA is often used for a transistor whose collector current at the maximum h_{fe} is as much as a few tens of milliamperes. This type of operation is used for avoiding too much power consumption and unnecessary heating-up due to too high bias point, because enough power gain can be obtained at about 1 mA with this transistor.

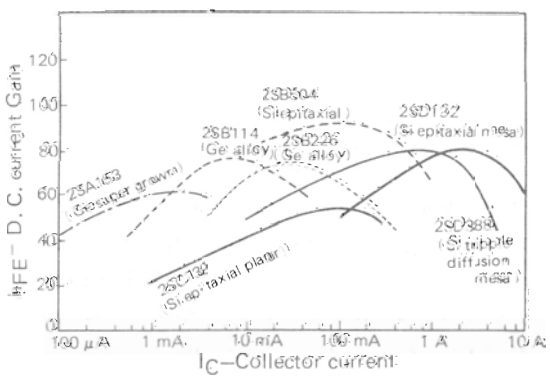


Fig. 7 Depeudencies of Transistor Current Amplification Upon Collector Current.

1.3 Actual Biasing Circuit and Formula for Biasing

Fig. 8 shows a typical low frequency amplifier with an NPN transistor. C_1 is the capacitor for the coupling with the preceding stage, C_2 is the by-passing capacitor of the power supply, and C_E is the by-passing capacitor of the emitter circuit. The output side is transformer-coupled with the following stage for impedance matching. The d.c. circuit related to the biasing is as shown in Fig. 9. Although the principle of the operation has been described with the separate power sources to collector and base respectively, most actual circuits are formed with a single power source as shown in the figure.

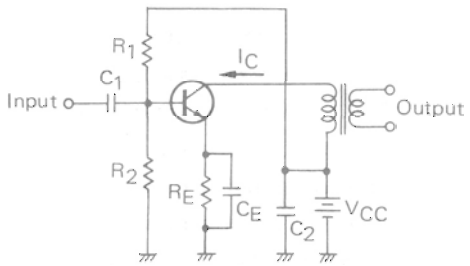


Fig. 8 Typical Low-Frequency Amplifier.

This biasing is the most popular system which is called current feedback system or breeder system.

Since I_C is h_{FE} times I_B, a biasing circuit which feeds I_B equal to I_C/h_{FE} is supposed sufficient to make the necessary bias current I_C flow. But, in actual transistors, beside I_B, a leakage current I_{CBO} between base and collector and a voltage drop V_{BE} between base and emitter should also be taken into account as factors affecting I_C.

Assume transistor parameters h_{FE} for d.c. current amplification, V_{BE} for base-emitter voltage, and I_{CBO} for collector cutoff current respectively, and the biasing collector current I_C is given by

$$I_C = \frac{\frac{R_2}{R_1+R_2}V_{CC} - V_{BE} + \left(R_E + \frac{R_1 \times R_2}{R_1+R_2}\right)I_{CBO}}{R_E + \frac{R_1 \times R_2}{(R_1+R_2)h_{FE}}}$$

This formula tells that I_C is influenced by transistor parameters h_{FE}, V_{BE}, and I_{CBO} when fixed circuit elements R_1, R_2, and R_E are used. This formula is based on the assumption that $h_{FE} \gg 1$ and interprets measured values very well. When this formula is used to design a biasing circuit, do not use h_{FE}, V_{BE}, and I_{CBO} as described in transistor catalogues, but use their actual values around the biasing point. Either of h_{FE}, V_{BE}, or I_{CBO} varies with voltage and current and in most cases, the trends of their variations are shown by curves in catalogues. Their actual values will be estimated from the curves. For germanium transistors, the term V_{BE} can often be neglected. For silicon transistors, the term V_{BE} cannot be neglected but the term I_{CBO} can be neglected in most cases.

R_1 and R_2 form a breeder that can apply base voltage independent of base current. This is because this circuit is called breeder system.

To select R_1, R_2, and R_E for a germanium transistor, follow the general rule that, for the sake of temperature stability, the smaller R_1 and R_2 the better, and the larger R_E the better. In particular, R_E has current feedback action and the larger R_E brings about better temperature stability, the less I_C variance, and the better stability against decrease of voltage. On the other hand, as R_E increases, the voltage drop across R_E increases to decrease the effective voltage between collector and emitter of the transistor. Therefore, R_E may not be increased too much when the collector current is high or when the collector current variation is high (e.g., in B-class or C-class operation).

For silicon transistors, it is desirable for temperature stability, that either of R_1, R_2, and R_E is high.

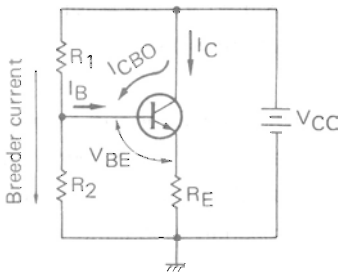


Fig. 9 D. C. Equivalent Circuit Related to Biasing.

1.4 Fixed Biasing and Self Biasing

Fig. 10 shows a biasing system called fixed biasing which is a modification of breeder biasing by putting $R_2 = \infty$ and $R_E = 0$. If the voltage drop V_{BE} between base and emitter can be neglected, the biasing resistance R_1 is obtained by

$$R_1 = \frac{V_{CC}}{I_B} = \frac{V_{CC} \times h_{FE}}{I_C}$$

It is the most simple biasing circuit and its temperature stability is bad. In particular, transistors with large I_{CBO}, such as Germanium transistors, are susceptible to run-away due to ambient temperature rise or self heating. In addition, in the fixed biasing, I_C variation is as wide as h_{FE} variation. Thus this biasing system can only be applied to small-signal and small power circuits where I_C may vary to some limited extent and run-away seldom happens.

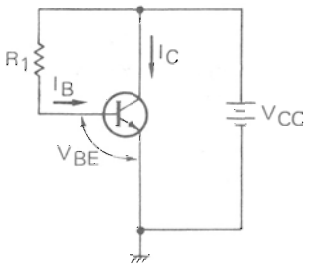


Fig. 10 Fixed Biasing Circuit.

The fixed biasing is superior to the breeder biasing in stability against voltage drop, i.e. a degree of decrease of biasing due to depression of power source voltage. There is a general tendency that silicon transistors are likely inferior to germanium transistors in stability against voltage drop because V_{BE} in the former is higher than the latter. In order to improve the situation as much as possible, sometimes this fixed biasing is used. As described above, I_C varies as much as h_{FE} does in the fixed biasing. Therefore, it is necessary to classify transistors by h_{FE} values beforehand in such a manner that I_C variation according to h_{FE} variation can be tolerated.

When the collector side has a load resistance (coil resistance, in cases of transformer coupling), the bias resistance R_1 setting not in power supply circuit but in collector circuit as shown in Fig. 11 can improve temperature stability and suppress I_C variation. This is called self biasing. When I_C tends to rise for any reason, the voltage drop is increased through the load resistance R_L, and V_{CE} is depressed to decrease I_B and accordingly, I_C increase is suppressed. Such an action may be regarded as a type of negative feedback through R_1 and R_L. Although the gain in the self biasing is decreased because of negative feedback through R_1, the self biasing is more practical than the fixed biasing. Fig. 12 summarizes characteristics of the three biasing circuit systems for transistor.

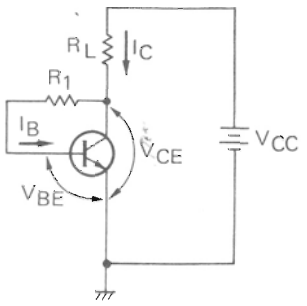


Fig. 11 Self Biasing Circuit.

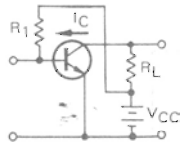
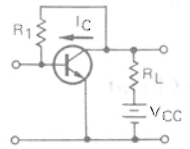
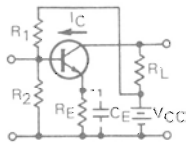
	Biasing Circuit	Formulas for I_C and V_{CE}	Characteristics	Applicable Circuits
(a) Fixed Biasing		$I_C = \frac{h_{FE}(V_{CE}-V_{BE})}{R_1} + h_{FE} \cdot I_{CBO}$ $V_{CE} = V_{CC} - I_C \cdot R_L$	• Simple circuitry • Low power consumption • Inferior temperature stability • Large I_C variation	• Cheap circuits • Low voltage and small current • Not so much temperature rise expected • Bias variation allowed to a considerable extent • Good stability against voltage drop required (particularly when Si transistor is used) • R_1 adjustable by means of h_{FE}
(b) Self Biasing		$I_C = \frac{h_{FE}(V_{CC}-V_{BE}) + h_{FE}(R_1+R_L)I_{CBO}}{R_1 + h_{FE} \cdot R_L}$ $V_{CE} = V_{CC} - I_C \cdot R_L$	• Simple circuitry • Low power consumption • Temperature stability better than (a) • I_C variation less than (a) • Low input and output impedance • Low distortion • Gain smaller than (a)	Same as above, and, • Low input impedance required • Distortion to be improved
(c) Current Feedback Biasing		$I_C = \frac{\frac{R_2}{R_1+R_2}V_{CC} - V_{BE} + (R_E + \frac{R_1 \cdot R_2}{R_1+R_2})I_{CBO}}{R_E + \frac{R_1 \cdot R_2}{(R_1+R_2)h_{FE}}}$ $V_{CE} = V_{CC} - I_C(R_1 + R_L)$	• Complex circuitry with a lot of circuit elements • Good temperature stability • Small I_C variation • High power consumption • By-passing C is necessary parallel to R_E • Inferior stability against voltage depression unless R_E is large (particularly for Si transistors)	• Good temperature stability required • Small I_C variation needed (i.e., wide range of h_{FE} value to be allowed) • High input impedance expected without C_E

Fig. 12 Characteristics of Biasing Circuits.

1.5 Polarity of Transistor

The biasing circuits which have been described up to this point are d.c. circuits concerned to biasing and extracted from actual circuits with NPN transistors for the sake of convenience. However, real circuits often use PNP and NPN transistors together, and the grounding points and bias polarities vary according to circuit configuration. This complex feature sometimes makes the identification of a biasing circuit difficult on circuit diagrams.

Since the polarity of transistor is, the most elementary, characteristic to transistors and is not seen in vacuum tube circuits, the description about the polarity will be given here.

Biasing of a transistor is done in two ways, namely, as shown in Fig. 13, NPN and PNP polarities of transistor require biasings which are totally complementory. The polarity rules are: the voltage polarity shall be determined from a grounded electrode potential and the current shall be positive when the current flows into a transistor and negative when it flows out. If referred to NPN types, I_E is measured as a negative value since I_E flows out of transistor, whereas I_E of PNP is positive since it flows into transistor. In symbols of transistor, the arrow mark at emitter designates the direction of emitter current flow.

The presence of transistors with either of both polarities is a major difference between transistors and vacuum tubes and it allows utilization in circuits, such as direct-coupled multistage circuits and push-pull circuits that need no phase inversion, that cannot be conceived with vacuum tubes.

However, when the polarity distinction is not so effectively used, the mixed use of NPN and PNP types may cause a demerit because of complicated biasing circuits.

2. TEMPERATURE STABILITY OF BIASING

Silicon transistors are often considered more stable than germanium transistors at high temperatures. But this is not an accurate statement.

Silicon transistors have small I_{CBO} and high maximum junction temperature Tj at which they can operate properly, and they are certainly stable when they are subject to life tests at high temperatures or at high power levels. But this feature is really true only for the transistor itself. In actual circuits, if circuit design is improper, the merit of silicon transistor may sometimes be ineffective.

Following the above mentioned basic biasing concept, descriptions will be given on the temperature stability of biasing, the largest problem in the biasing circuit design, in typical biasing circuit systems, and the cautions to be paid in biasing circuit design will be referred.

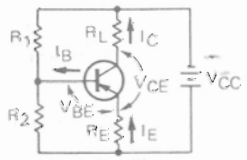
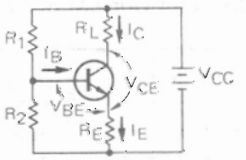
Polarity	PNP	NPN
Name of transistor	2SA ---- or 2SB ----	2SC ---- or 2SD ----
Symbol		
Biasing		
Collector voltage V_{CE} (to emitter)	−	+
Base voltage V_{BE} (to emitter)	−	+
Collector Current I_C	− (flowing out of transistor)	+ (flowing into transistor)
Base Current I_B	− (flowing out of transistor)	+ (flowing into transistor)
Emitter Current I_E	+ (flowing into transistor)	− (flowing out of transistor)

Fig. 13 Comparison of Biasing According to Transistor Polarities.

2.1 Temperature Stability of Biasing

The temperature drift of any transistor characteristics are unavoidable due to contruction semiconductor material. However, much more variation of transistor constants are often expected as the result of bias point shift due to temperature variation. Therefore, it is important to design biasing circuit in such a manner that it suffers from little bias point shift with temperature variation. This concept is called temperature stability of biasing.

I_{CBO} increases , V_{BE} decreases, and in general h_{FE} increases occur with temperature rise. Either factor will increase collector current I_C as the biasing at higher temperatures and will decrease I_C at lower temperatures.

Fig. 14 and 15 show examples of h parameter variation due to variation of biasing in a silicon transistor. When the biasing is shifted according to the temperature variation, input impedance, output impedance, and gain vary at the same time.

Since transistor parameters are largely susceptible to the biasing change, the bias point shift due to changes in environmental or power conditions may lead device performance very far from that initially expected when the device was designed. Furthermore, in cases of large amplitude operation, the bias point set optimum at the normal temperature may be shifted upward to generate too early, causing top clipping of output waveform at higher temperatured or shifted downward to produce too early bottom clipping at lower

temperatures, thus resulting in larger distortion. If the shift is too much, thermal run away, might occur at higher temperatures and damage the transistor.

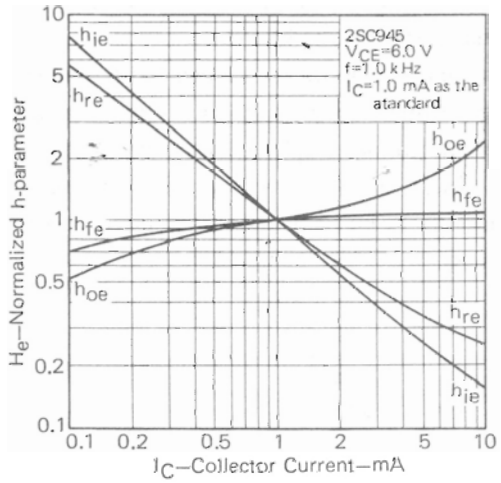


Fig. 14 Example of h-parameter Variation with Collector Current Shift.

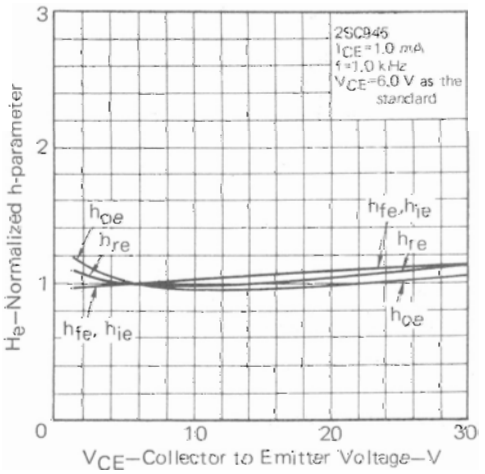


Fig. 15 Example of h-parameter Vareation with Collector Voltage.

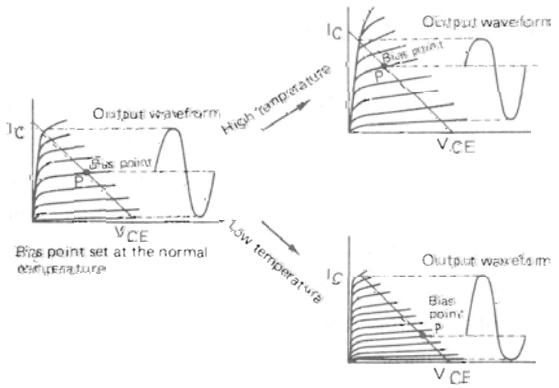


Fig. 16 Bias Point Shift Due to Temperature Change and Distortions in Output Waveform.

2.2 Quantitative Analysis of Temperature Stability

Take collector current I_C as the transistor biasing. Assume that dI_C is the variation of I_C . It can be said that

$$dI_C = \left(\frac{\partial I_C}{\partial I_{CBO}}\right) dI_{CBO} + \left(\frac{\partial I_C}{\partial V_{BE}}\right) dV_{BE} + \left(\frac{\partial I_C}{\partial h_{FE}}\right) dh_{FE} \quad (1)$$

This formula tells us the variation of I_C when I_{CBO}, V_{BE}, and h_{FE} are varied by dI_{CBO}, dV_{BE}, and dh_{FE}, respectively, for some reason.

The terms in paraentheses of the formula are stability coefficients for I_{CBO}, V_{BE}, and h_{FE} respectively and they are defined as follows.

$$S_1 = \left(\frac{\partial I_C}{\partial I_{CBO}}\right), \text{ stability coefficient for } I_{CBO}, \quad (2)$$

$$S_2 = \left(\frac{\partial I_C}{\partial V_{BE}}\right), \text{ stability coefficient for } V_{BE}, \quad (3)$$

$$S_3 = \left(\frac{\partial I_C}{\partial h_{FE}}\right), \text{ stability coefficient for } h_{FE}. \quad (4)$$

Assuming that the major factor that affects biasing is temperature, we can describe dI_C due to temperature variation dt as

$$\frac{dI_C}{dt} = S_1 \frac{dI_{CBO}}{dt} + S_2 \frac{dV_{BE}}{dt} + S_3 \frac{dh_{FE}}{dt} \quad (5)$$

The rate of I_{CBO} variation I_{CBO}/dt, the rate of V_{BE} variation dV_{BE}/dt, or the rate of h_{FE} variation dh_{FE}/dt according to temperature change is dependent on the transistor used. Therefore, for the transistor determined for the use, the minimization of dI_C/dt, the rate of I_C change due to temperature, will be reduced to the design of a biasing circuit that makes the three stability coefficients S_1, S_2, and S_3 as small as possible.

The stability coefficients S_1, S_2, and S_3 are calculated, in accordance with the respective definitions (2), (3), and (4), by partially differentiating the formula that gives I_C with I_{CBO}, V_{BE}, and h_{FE}, respectively.

The bias current I_C for the most popular biasing circuit of current feedback system as shown in Fig. 17 can be obtained by the formula

$$I_C = \frac{\frac{R_2}{R_1 + R_2} V_{CC} - V_{BE} + \left(R_E + \frac{R_1 \times R_2}{R_1 + R_2}\right) I_{CBO}}{R_E + \frac{R_1 \times R_2}{(R_1 + R_2) h_{FE}}} \quad (6)$$

The stability coefficients are derived from this formula as follows.

$$S_1 = \frac{\partial I_C}{\partial I_{CBO}} = \frac{R_E + \frac{R_1 \times R_2}{R_1 + R_2}}{R_E + \frac{R_1 \times R_2}{(R_1 + R_2) h_{FE}}} \quad (7)$$

$$S_2 = \frac{\partial I_C}{\partial V_{BE}} = \frac{-1}{R_E + \frac{R_1 \times R_2}{(R_1 + R_2) h_{FE}}} \quad (8)$$

$$= \frac{-S_1}{R_E + \frac{R_1 \times R_2}{R_1 + R_2}} \quad (9)$$

$$S_3 = \frac{\partial I_C}{\partial h_{FE}} = \frac{S_1 (I_C - I_{CBO})}{h_{FE}^2} \quad (10)$$

What is understood at a glance at the formulas is that minimizations of S_1, S_2, and S_3 are reduced to the minimization of S_1. Further detailed inspections result in Table 1.

Thus the stability of biasing circuit is known by knowing three stability coefficients S_1, S_2, and S_3. However, I_{CBO}, V_{BE}, and h_{FE}, the causes which affect biasing, do not vary in the same manner. In germanium transistors with large I_{CBO}, the influence of I_{CBO} predominates over those of V_{BE} and h_{FE}, and the reduction of S_1 is emphasized in biasing circuit design. This is why, in germanium transistor circuit, the ratio of I_C variation to I_{CBO} variation, dI_C/dI_{CBO}, or S_1 above described, is called temperature stability factor of biasing, and denoted by a symbol S. In silicon transistors for small signal, I_{CBO} is mostly so small that it can be neglected, and V_{BE} normally predominates over I_{CBO} as the cause to change biasing condition.

Table 1 Influence of Circuit Constant on Stability Coefficients

	R_1, R_2	R_E	h_{FE}
To reduce S_1	The smaller the better	The larger the better	The smaller the better
To reduce S_2	The larger the better	The larger the better	The smaller the better
To reduce S_3	The smaller the better	The larger the better	The larger the better

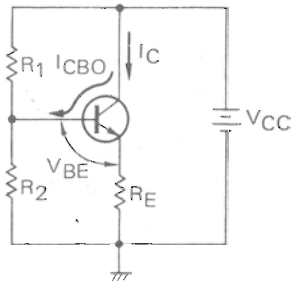


Fig. 17 Biasing Circuit of Current Feedback System.

Temperature Stability of Germanium Transistor Biasing

I_{CBO} of germanium transistors are usually a few microamperes, whereas V_{BE} is 0.1 – 0.2 V. So, if a voltage drop across R_E can be made sufficiently larger than V_{BE}, the effect of V_{BE}'s temperature dependency can be neglected and only the I_{CBO}'s temperature dependency is left for the circuit design consideration. Thus, the smaller the value of the stability factor S, the term given by $S_1 = \partial I_C/\partial I_{CBO}$, the more stable is the biasing against temperature change.

When S is obtained from Equation (7) above, the variation ΔI_C of collector current I_C due to variation ΔI_{CBO} of I_{CBO} is calculated with the following formula.

$$\Delta I_C = S \cdot \Delta I_{CBO} \quad (11)$$

Although the variation of I_{CBO} with temperature cannot be avoided as far as transistors are concerned due to contruction, the biasing circuit design can contribute to reduce the effect of inevitable change of I_{CBO} on bias current I_C as much as possible. How far this reduction will be is expressed by the value of S. The most stable state corresponds to S = 1, when the I_C variation is caused only by I_{CBO} variation.

S depends on biasing resistances R_1, R_2, and R_E as well as on transistor h_{FE}. Fig. 18 shows curves for immediate estimation of S value with the biasing resistances and the transistor h_{FE} through the formulas below obtained by the modification of Equation (7) for S,

$$S = \frac{1 + X}{1 + \frac{X}{h_{FE}}} \quad (12)$$

where

$$X = \frac{R_1 \times R_2}{R_E(R_1 + R_2)}$$

When the biasing resistances are kept constant (that is, for constant X), S is the larger for the larger h_{FE}, therefore the temperature stability is worse. That means that, from the viewpoint of temperature stability of biasing, a transistor with the larger h_{FE} is not necessarily the better one.

By using Equation (11), the variation ΔI_C of the biasing collector current in the biasing circuit for a germanium transistor can be calculated from the known variation ΔI_{CBO} of I_{CBO} and the stability factor S, or S_1, obtained from the biasing circuit constants. I_{CBO} of a transistor largely depends on the temperature, and it is doubled for a temperature rise of 8 to 10 °C. The problem is the design of a biasing circuit with S that limits ΔI_C within a tolerable bias shift range when the temperature rise is estimated as the sum of environmental temperature variation and temperature rise due to collector input power (a product of collector voltage and collector current) and then the variation ΔI_{CBO} of I_{CBO} is estimated with the expected temperature rise. Since the emitter circuit resistance R_E affects S greatly, the use of as large R_E as possible results in a biasing circuit with a small S and a good temperature stability when the power supply voltage has a good margin and the collector current is not so high. If, like in fixed biasing, a single biasing resistance is used in base circuit and $R_E = 0$ and $R_2 = \infty$, the relationship

$$S_1 = h_{FE}$$

holds and the variation of I_{CBO} is amplified h_{FE} times to influence on collector current I_C.

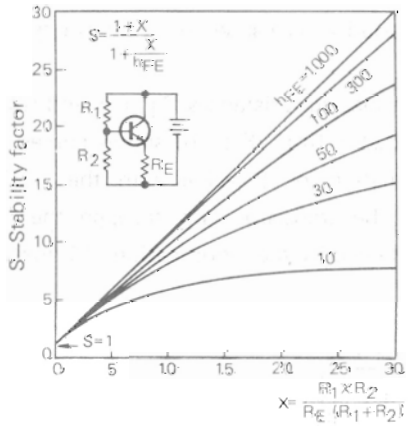


Fig. 18 Relationship of S to Biasing Resistances and h_{FE}.

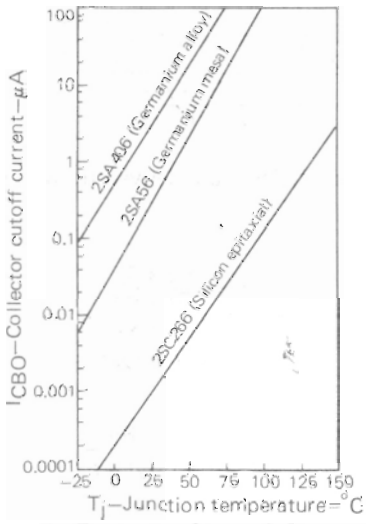


Fig. 19 Example of I_{CBO}'s Temperature Dependency.

2.3 Example of Temperature Stability in Actual Biasing Circuit

Fig. 20 shows an example of CR coupled low frequency amplifier using a germanium transistor 2SB326. The circuit is set to V_{CC} of 12 V and I_C of 2.8 mA as shown in the operation diagram of Fig. 21. Using h_{FE}(= I_C/I_B) value of 56 (which is different from the value shown in catalogues because of the difference in measuring conditions) and circuit constants R_1 = 8 kΩ, R_2 = 4 kΩ, and R_E = 1.4 kΩ in the biasing circuit, Equation (7) gives S_1 as follows.

$$S_1 = \frac{1.4\ \text{k}\Omega + \dfrac{8\text{k}\Omega \times 4\ \text{k}\Omega}{8\ \text{k}\Omega + 4\ \text{k}\Omega}}{1.4\ \text{k}\Omega + \dfrac{8\ \text{k}\Omega \times 4\ \text{k}\Omega}{(8\ \text{k}\Omega + 4\ \text{k}\Omega) \times 56}} \fallingdotseq 2.8$$

According to catalogues, 2SB326 is supposed to have I_{CBO} at 25 °C of 10 μA max. This will make ΔI_{CBO} of about 80 μA across the temperature range of 25 ± 30 °C for the circuit, and the maximum variation ΔI_C of collector current I_C will be 2.8 × 80 μA = 224 μA, namely, 8 % variation in I_C.

For a fixed biasing circuit as shown in Fig. 22, with the same transistor 2SB326 and I_C of 2.8 mA,

$$S_1 = h_{FE} = 56,$$

and ΔI_C becomes as large as 56 × 80 μA = 4.48 mA which is too far from the design of I_C = 2.8 μA at 25 °C.

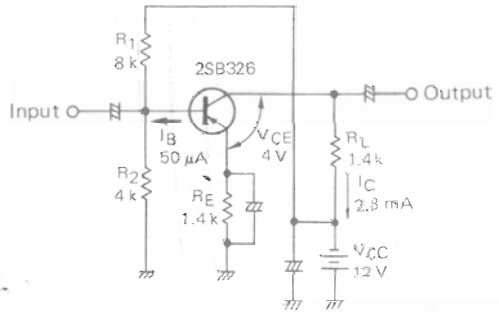


Fig. 20 CR Coupled Low Frequency Amplifier with a Germanium Transistor 2SB326

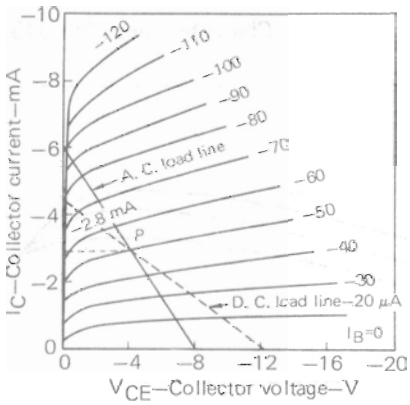


Fig. 21 Bias Point Setting and Operation Diagram on I_C–V_{CE} Characteristics.

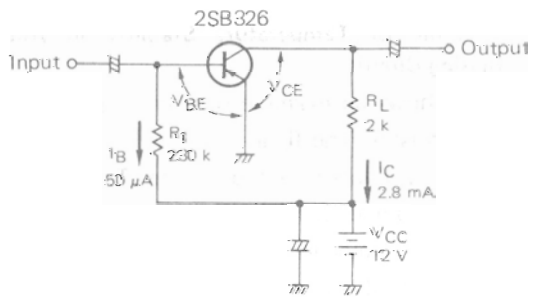


Fig. 22 Circuit with Fixed Biasing.

2.4 Thermal Runaway (Runaway)

The biasing I_C in a transistor circuit is increased with the temperature rise, and this I_C increase necessarily makes the d.c. input power to the transistor larger. This power increase again raises the temperature Tj at the collector junction of the transistor. In some biasing circuit configurations, triggered by I_C increase due to the rise of environmental temperature or due to some other reasons, the collector current may be increased cyclically without limit as shown in Fig. 23 and finally resulting in the breakdown of the transistor. This is called thermal runaway, or runaway, and this phenomenon should be the most carefully considered when designing biasing of transistor circuits that handle large power.

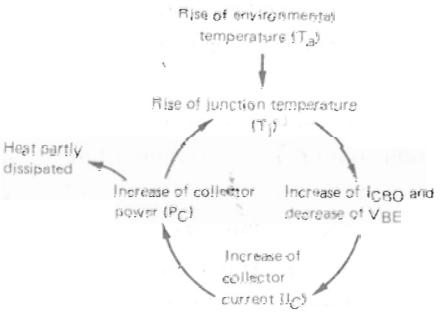


Fig. 23 Causes of Thermal Runaway.

The possibility of thermal runaway depends on the temperature rise due to transistor input power (or also called heat resistance) and of the inverse of input power increase due to temperature rise if larger than the other. From the stand point of biasing circuit design, it is necessary to suppress as much as possible the rate of input power increase to the transistor due to temperature rise for preventing thermal runaway. For this purpose, it is essential to make S small.

Since, in germanium transistors, I_{CBO} is increased with temperature rise, I_C is also increased to result in thermal runaway. In silicon transistors, the temperature rise causes V_{BE} depression and consequently I_C is increased also to thermal runaway. Therefore, in order to prevent the thermal runaway, it is necessary to design circuit so as to obtain small S_1 for germanium transistors and small S_2 for silicon transistors, respectively.

2.5 Temperature Stability of Silicon Transistor Biasing

In the most rigorous sense, the temperature stability of a transistor biasing circuit should be considered with regard to all temperature dependent effects of I_{CBO}, V_{BE}, and h_{FE}. However, this makes the analysis very complicated. Therefore, like in germanium transistors where only I_{CBO} is taken into account and other factors are neglected, the temperature stability of silicon transistor biasing will be considered only with the most effective factor whereas other factors are neglected.

Although some silicon transistors for power use have I_{CBO} as low as a few nanoamperes, through a few microamperes, the small signal transistors that require biasing are generally provided with very small I_{CBO} of a few nanoamperes, and it seems that the term of I_{CBO} can be neglected in biasing circuit design.

Be aware that d.c. base voltage V_{BE} of silicon transistor is about 0.6 or 0.7 V and three times as large as that of germanium transistor. Therefore V_{BE} cannot be neglected unlike in the biasing circuit design for germanium transistors. The temperature dependency of I_C-V_{BE} characteristics is almost a parallel shifting as shown in Fig. 24 and its rate of shift is about −2 mV per 1 °C.

Because the I_C-V_{BE} characteristic curves have very steep rise and they are shifted with the variation of temperature, the temperature variation affects biasing and sometimes thermal runaway results according to operating conditions.

The variation of h_{FE} with temperature is about 0.1 − 1 % as shown in Fig. 25 and it is rather gross to neglect the effect of h_{FE} variation. But let us take V_{BE} which is the most effective to temperature stability of biasing as the sole parameter in order to simplify calculations.

When the variation of I_C with V_{BE} variation which is $S_2 = \partial I_C/\partial V_{BE}$ is taken as the measure demonstrating the temperature stability of silicon transistor, the variation ΔI_C of collector current for a variation ΔV_{BE} of V_{BE} is calculated as

$$\Delta I_C = S_2 \cdot \Delta V_{BE} \qquad (13)$$

Or, for a temperature variation ΔT,

$$\frac{\Delta I_C}{\Delta T} = S_2 \frac{\Delta V_{BE}}{\Delta T} \qquad (14)$$

where $\Delta V_{BE}/\Delta T$ is the rate of V_{BE} temperature dependency, δ, which is about −2 mV/°C for silicon transistors.

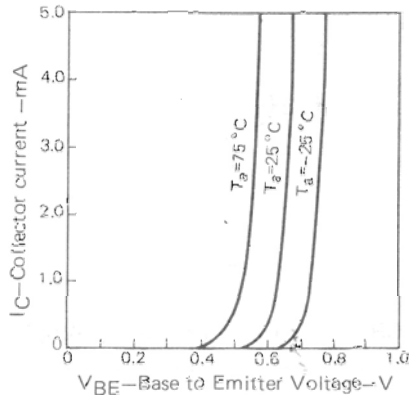


Fig. 24 Example of Temperature Dependency of I_C–V_{BE} Characteristics. (2SC943)

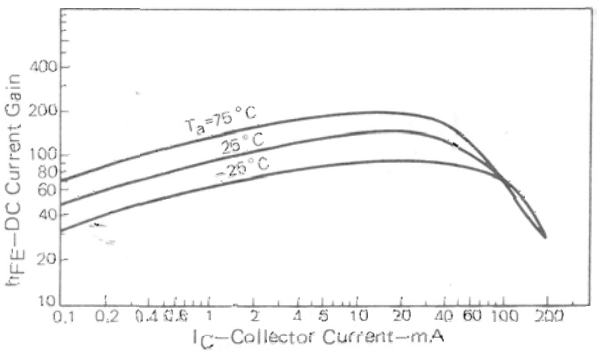


Fig. 25 Example of Temperature Dependency of h_{FE}. (2SC943)

2.6 Example of Temperature Stability in Actual Biasing Circuit

Fig. 26 shows an example of a biasing circuit for a silicon transistor. The figure is drawn only for a d.c. circuit directly related to the biasing. The transistor used, is 2SC943 and its h_{FE} at I_C = 1 mA is approximately 90 by catalogue. When the biasing current is designed for I_C of about 1 mA, R_1 = 6.8 kΩ, R_2 = 4.7 kΩ, and R_E = 3 kΩ.

The stability coefficient S_2 of this biasing circuit against V_{BE} variation is calculated as

$$S_2 = \frac{-1}{3\,\text{k}\Omega + \dfrac{6.8\,\text{k}\Omega \times 4.7\,\text{k}\Omega}{(6.8\,\text{k}\Omega + 4.7\,\text{k}\Omega)\times 90}} \fallingdotseq -0.33 \times 10^{-3}\ \text{A/V}$$

This means that, if V_{BE} is shifted by 1 mV, I_C varies by −0.33 μA. If the temperature range is considered 25 ± 30 °C, or if ΔT is within 60 °C, ΔV_{BE} of −120 mV results with δ of −2 mV/°C, and

$\Delta I_C = -0.33 \times 10^{-3} \times (-120 \times 10^{-3}) = 39.6\ \mu\text{A}$,

namely, the variation ΔI_C is about 4 % of I_C.

3. VOLTAGE DROP CHARACTERISTICS AND CHARACTERISTIC DISTRIBUTION

Continuing with the descriptions on the temperature stability, which is the most important factor in the formula for biasing and in biasing circuit design, descriptions are given on the voltage drop characteristics and the characteristic distribution which is the next problem to be solved in biasing circuit design.

3.1 Voltage Drop Characteristic of Biasing

Devices with battery power source should be so designed that their characteristics do not vary too much according to the drop of source voltage. When the source voltage falls, the collector voltage as a biasing also falls and, if the biasing circuit constants (biasing resistances) are fixed, the collector current also decreases accordingly. Since the change in transistor characteristics with the depression of collector voltage is rather slight, the change in characteristics with the drop of source voltage is chiefly due to the decrease of collector current. The rate of collector current variation in biasing circuit of transistor is usually larger than the rate of source voltage variation if no special measure is taken such as the use of non-linear elements in the biasing circuit. The aspect of this variation is as shown in Fig. 27, and when the biasing resistances are linear (that is, when neither thermister nor varistor is used), the rate of collector current decrease is necessarily greater than the rate of source voltage drop. It is necessary in biasing circuit design to reduce the rate of collector current decrease to the rate of source voltage depression as far as possible and to make the ratio as close to 1 : 1 as possible. This is called voltage depression characteristic of biasing.

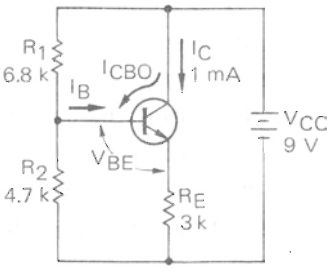


Fig. 26 Biasing Circuit of Current Feedback System with Silicon Transistor 2SC943.

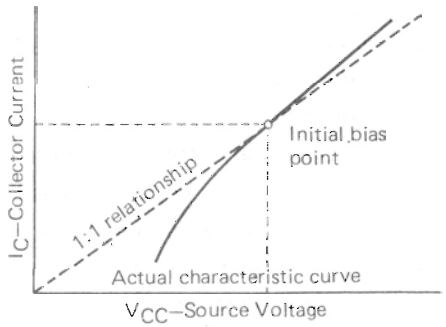


Fig. 27 The ratio of Collector Current Variation to Source Voltage Variation.

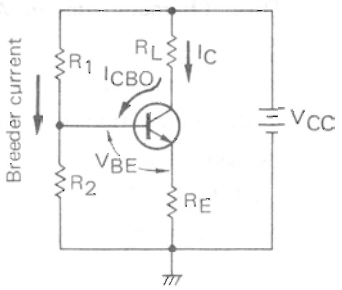


Fig. 28 Biasing Current of Breeder System.

Fig. 28 shows the biasing circuit of a breeder system. The formula for the collector current is beforementioned Eq. (6). Let us consider how the depression of source voltage affects the collector current I_C. It is understood that, the larger is $R_2 \times V_{CC}/(R_1 + R_2)$ compared with V_{BE}, the less is the effect. When $R_2 \times V_{CC}/(R_1 + R_2) \gg V_{BE}$ and V_{BE} can be neglected, the rate of collector current variation ought to be nearly the same as the rate of variation of source voltage V_{CC}. Let us explain it in mathematical formulas.

Differentiate Eq. (6), the formula for I_C, with V_{CC}.

$$\frac{dI_C}{dV_{CC}} = \frac{\dfrac{R_2}{R_1 + R_2}}{R_E + \dfrac{R_1 \times R_2}{(R_1 + R_2)h_{FE}}} \tag{15}$$

Then divide by I_C, or by Eq. (6), and modify the expression to obtain

$$\frac{dI_C}{I_C} \fallingdotseq \frac{dV_{CC}}{V_{CC}} \cdot \frac{1}{1 - \dfrac{V_{BE}}{V_{CC}} \times \dfrac{(R_1 + R_2)}{R_2}} \tag{16}$$

This equation tells us that the variation rate of I_C is larger than that of V_{CC}, and if the condition $R_2 \times V_{CC}/(R_1 + R_2) \gg V_{BE}$ is satisfied, dI_C/I_C approaches to dV_{CC}/V_{CC} asymptotically. Generally V_{BE} of silicon transistor is too large to be neglected and this fact

is the inherent cause of voltage drop characteristics of silicon transistor which is worse than those of germanium transistor. The selection of large $R_2/(R_1 + R_2)$ for improving the voltage depression characteristics implies the setting of emitter point at a high voltage in a biasing circuit of breeder system. This corresponds to the use of large R_E and leads to a conclusion that a biasing current with good temperature stability is also good in voltage depression characteristics.

3.2 Voltage Drop Characteristics in Actual Biasing Circuits

Fig. 29 shows the comparison of voltage drop characteristics of a germanium transistor and of a silicon transistor in the same biasing circuit. The collector current is first set to 1 mA at the initial voltage of 12 V. It decreases with the source voltage drop as shown in the figure. The germanium transistor is 2SB226 and the silicon transistor is 2SC943. Other transistors will also give the similar results.

Due to large V_{BE}, the voltage drop characteristics of silicon transistor are inferior to those of germanium transistor. This disadvantage is partly compensated by using a large emitter resistance R_E as shown in Fig. 30. These are examples of biasing circuit according to the breeder system which is the most popular type.

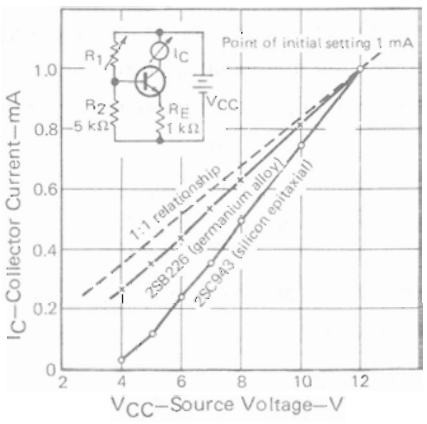


Fig. 29 Comparison of Voltage Depression Characteristics of a Silicon Transistor and a Germanium Transistor.

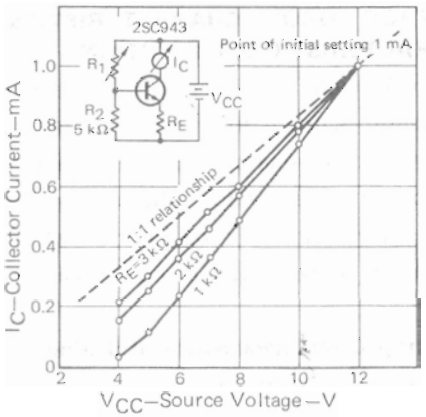


Fig. 30 Voltage Depression Characteristics for Various Values of R_E

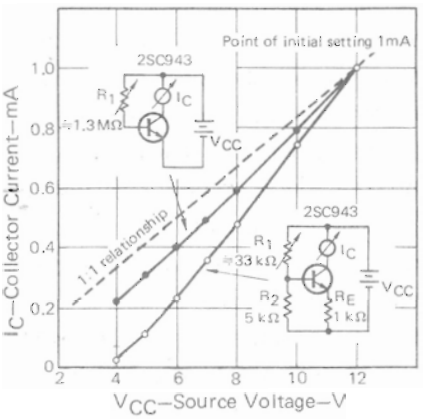


Fig. 31 Comporison of Voltage Deprcssion Characteristics for Breeder Biasing and Fixed Biasing Systems.

Examine the fixed biasing system that means $R_2 = \infty$ as another method for improving the voltage drop characteristics. Fig. 31 shows an example. It is evident that the fixed biasing system is better in the voltage drop characteristics. The reason is interpreted as follows. The voltage drop characteristics are dependent on the relationship between the voltage supplying base current and V_{BE} of transistor. The base side voltage in the breeder system is given by dividing source voltage by R_1 and R_2, whereas the counterpart in the fixed biasing system is connected to source voltage V_{CC} itself. Thus, the fixed biasing system is a method for improving the voltage drop characteristics when R_E cannot be taken so large because of low source voltage. Instead, the collector current variation in the fixed biasing system is higher than in the breeder system. Therefore, it is necessary to take a measure

such as cut-and-try trimming of biasing resistance R_1 in accordance with the transistor characteristics or combination of transistor grouped according to h_{FE} and grouped R_1 which is appropriate to the h_{FE} value.

3.3 Biasing Circuit with Varistor Diode

Biasing circuit according to the breeder system is advantageous in voltage drop characteristics and disadvantageous in collector current variation distribution and fixed biasing circuit or vice versa. The biasing circuit which seems to solve both problems at one time is the one with a varistor diode. Fig. 32 shows its basic circuit. Its collector current is given below when the effect of I_{CBO} is neglected.

$$I_C = \frac{V_F - V_{BE}}{R_E} \qquad (17)$$

where V_F is the forward voltage of the varistor.

Usually, a varistor diode is inherently a common semiconductor diode as shown in Fig. 33. Therefore most semiconductor diodes not bearing the name of varistor can be used as varistors. The substantial characteristics of varistor are forward voltage and its temperature coefficient. The nature of almost constant forward voltage V_F over a wide range of forward current I_F is utilized. The biasing by a varistor is based on an idea that a forward current I_F which is sufficiently higher than the transistor base current I_B flows through the varistor diode in order to keep nearly constant V_F as the voltage source to base against the decrease of varistor current I_F due to the source voltage drop. In a breeder type biasing circuit, the decrease of the voltage across R_2 which is nearly proportionate to the source voltage drop makes the collector current decrease more markedly than the source voltage drop if V_{BE} of transistor cannot be neglected. The process is explained below using Fig. 34. Take an example of initial I_C value of 1 mA and R_E of 1 kΩ. Since the voltage a between emitter and ground is $R_E \times I_E$ = 1 kΩ × 1 mA = 1 V, the breeder resistance is previously so set that the voltage b between base and ground is 1.6 V, the sum of V_{BE} = 0.6 V of the transistor and the voltage a. This situation is demonstrated by the straight line drawn from the point of 1.6 V with a slope corresponding to R_E = 1 kΩ crossing the I_C-V_{BE} curve of transistor at the point where I_C = 1 mA. When the power supply voltage is depressed to half the initial value, the breeder current is also proportionately decreased to nearly half and the voltage between the base and the ground of the transistor, that is, voltage b across R_2, is also halved to 0.8 V. Since the value of R_E remains the same, the cross point of the straight line drawn from the point of 0.8 V with the slope of 1 kΩ and the I_C-V_{BE} curve of the transistor determines I_C for the halved power source voltage. This is estimated about 0.2 mA from the figure and it is much smaller than half the initial value of 1 mA.

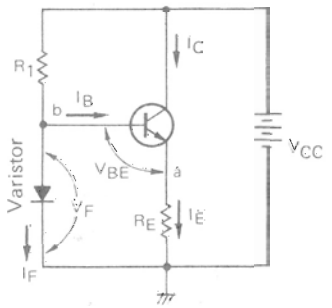


Fig. 32 Biasing Circuit with a Varistor Diode.

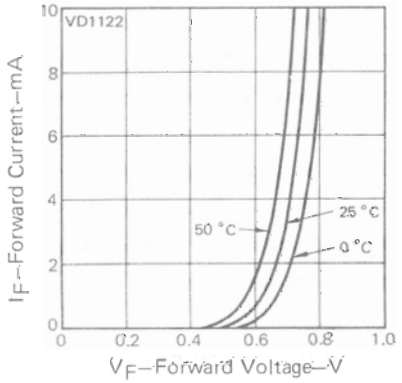


Fig. 33 Characteristics of a Varistor Diode.

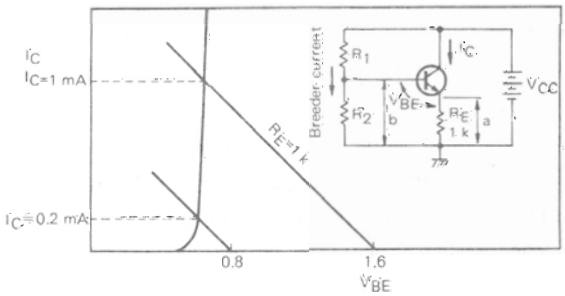


Fig. 34 Graphic Interpretation of I_C Decrease When V_{CC} is decrease to ½

Whereas, if a varistor diode is used instead of R_2, the voltage V_F across the varistor diode is kept almost unchanged even when the breeder current, or the forward current I_F of the varistor diode is decreased to half, and the collector current is kept almost constant. Fig. 35 shows this performance. Actually the voltage V_F across the varistor terminals are more or less decreased with the decrease of the forward current and a slight decrease of transistor collector current results from the source voltage drop. Nevertheless, the degree of decrease in this system is much less than that in the breeder system biasing.

The temperature stability in the varistor diode biasing system is given by

$$S_2 = \frac{-1}{R_E} \qquad (18)$$

This formula tells that, in the varistor diode biasing system, the larger the R_E, the better thermal stability is expected. Since V_F of one varistor diode is about 0.6 V even for silicon diodes and the use of large R_E leads to the large voltage at point b which is the sum of transistor's V_{BE} and voltage depression across R_E, the series connection of several varistor diodes is necessary for obtaining the required voltage. Therefore, when the maximum number of varistors is limited to, two or so from an economical point of view, the value of R_E should range from a few hundreds ohms to 1 kΩ and the temperature characteristics of this biasing system is generally worse than those of breeder system biasing or of fixed biasing.

3.4 Collector Current Scattering Distribution

Although various parameter values are listed on transistor catalogues, the value which is measured with one transistor is not necessarily consistent with the catalogued standard value (or average value). Examinations of many transistors reveals that the transistor characteristics are always distributed around the catalogue standard value with some scattering. This is called the scattering of characteristics. When those transistors are used with some identical biasing circuit, the biasing collector currents vary from one to another and the scattering is generated.

Among parameters I_{CBO}, V_{BE}, and h_{FE} that affect the biasing collector current I_C, the scattering of V_{BE} for silicon diffused type transistors is generally very small and the effect of h_{FE} scattering is the sole factor affecting the scattering of collector current I_C. In the biasing circuits of a conventional breeder system, the numerators in Eq. (6) for I_C are supposed to be constants and the denominator dominates the I_C scattering. This leads to the conclusion that, the larger is R_E relative to $R_1 \times R_2/(R_1 + R_2)h_{FE}$, the smaller is the I_C scattering.

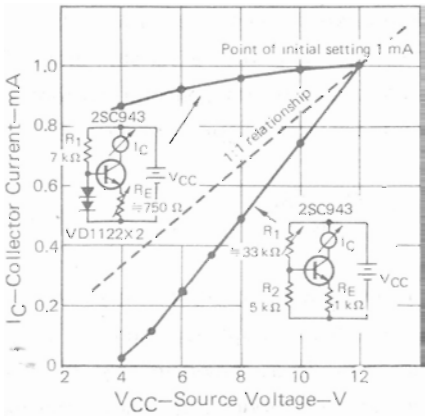


Fig. 35 Voltage Depression Characteristics of Biasing Circuits with Varistor Diode.

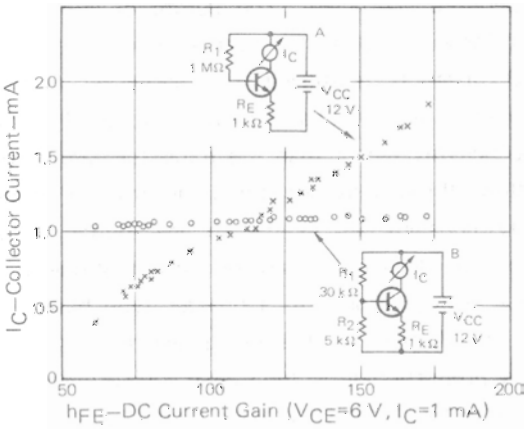


Fig. 36 Examples of Collector Current Scattering in Actual Circuits,.

The mathematical examination of h_{FE}'s effect on I_C can be carried out by differentiating Eq. (6) with h_{FE} to obtain dI_C/dh_{FE} which is S_3 and then modifying dI_C/dh_{FE} to express dI_C/I_C in terms of dh_{FE}/h_{FE}. This process is considerably complicated. Only the result is described as

$$\frac{dI_C}{I_C} = \frac{dh_{FE}}{h_{FE}} \cdot \frac{S_1}{h_{FE}} \qquad (19)$$

This equation tells that a larger reduction of I_C scattering is achieved by the selection of the larger R_E for the circuit constant and of the larger h_{FE} for the transistor.

The h_{FE} values of transistors as produced are scattered from the minimum to the maximum which is ten times larger.

This scattering as it is will render the use of transistors difficult because of too great of scattering. Therefore, the classification of the transistors according to their h_{FE} values are performed. This is called ranking. The ranking was not published on catalogues and only disclosed in sales contracts between semiconductor makers and the large OEM users. But, recently, the ranking is often published in catalogues or in data books, where the h_{FE} ranks are usually referred to in such a manner that the maximum value is double the minimum value in each rank, for example, 30–60, 50–100, 80–160, 125–250, and 200–300. This equal ratio ranking is more rational than equal difference ranking as far as the h_{FE} effects on biasing and on amplifier characteristics are concerned. However, when the scattering of biasing is considered as the primary concern, a h_{FE} ratio wider than double can be allowed for larger h_{FE}.

The examples of actual effects of R_1, R_2, and R_E which are the constants of biasing circuit on the collector current scattering are shown in Fig. 36. Circuit A is a fixed biasing circuit and Circuit B is a breeder system biasing circuit and the both are designed to have collector current of about 1 mA at h_{FE} value of about 100. The transistor used is 2SC943 and measurements are taken over all h_{FE} ranks. The mark X represents circuit A and the mark O circuit B, respectively. The data evidently demonstrate that the use of the breeder system and large R_E will reduce temperature stability coefficient S_1 of biasing and leads to very small scattering of collector current.

HIGH FREQUENCY SMALL SIGNAL CIRCUIT DESIGN

1. GENERAL DESCRIPTION

In the case of high frequency, small signal circuits, unlike low frequency circuits, the small capacities of elements and component parts have influence upon circuit operation, and their characteristics depend entirely upon the grounding point of a printed circuit substrate. Therefore, it applies to general high frequency circuits that the circuit obtained by computation remarkably vary according to the conditions of its mounting.

Hence, it is not too much to say that whether or not the circuit normally operates depends upon how it is corrected on the experimental stages after mounting. The point is that the work of "cut and try" is essential. However, it should persistently be insisted that the fundamental theory described in the following is the basis, and the procedure of correction at the time of mounting is indispensable.

2. HIGH FREQUENCY CIRCUIT AND TYPES OF TRANSISTORS

The characteristics of high frequency small signal transistors and FFT's are listed in Table 1. As is clear from this table, MOS FFT is advantageous from a characteristical point of view, though transistors are favorable as to the cost and electrostatic breakdown.

The cascode FET shown in the table is a junction type FET, which was contrived as an FET provided with the same characteristics as those of MOS FET.

Table 1 Elements for high Frequency Small Signal Amplification and Their Characteristics

Type	Characteristics
Bipolar transistor	Endurable against electrostatic breakdown and low in the cost though inferior to FET in stability, cross modulation and spurious characteristic.
Junction type single gate FET	Low in stability though intermediate between MOS FET and bipolar transistor as to gain, noise, cross modulation, spurious characteristic, breaking strength and cost
Junction type cascode FET	The cost is same as that of single gate FET, the characteristics are similar to those of MOS FET, and the breaking strength is equivalent to that of single gate FET.
MOS type FET	The high frequency characteristics are superior to those of other elements, though it has the defects that the cost is high and that it is not endurable against electrostatic breakdown.

3. EXAMPLE OF TRANSISTOR HIGH FREQUENCY AMPLIFYING CIRCUIT DESIGN

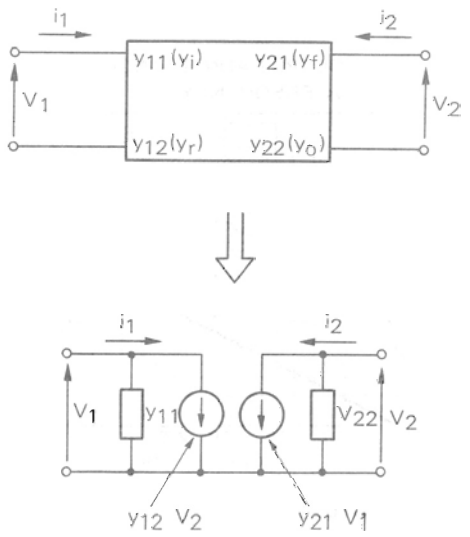
In this section, the design of a high frequency amplifying circuit by general bipolar transistors is described. In the case of the transistors for high frequency (above the FM band), the y-parameter is described in the catalogue.

This is because the parameter of the transistor at high frequency is a complex volume, because the transistor is regarded as a 4-terminal circuit network for it is diffecult to analyze the transistor at high frequency by means of an equivalent circuit so that circuit indication can be made only by the electric characteristics viewed from the outside regardless of the physical phenomena on the inside, and so on.

In this section, it is described how to obtain the standards of the characteristics of a certain device used in a high frequency circuit.

3.1 Indicating Method of y-parameter

The y-parameter refers to an element equivalently indicated by parallel admittance, as shown in Fig. 1.



y (yi) .... input admittance
y (yr) .... reverse transadmittance
y (yf) .... foward transadmittance
y (yo) .... output admittance

Fig. 1 Element Equivalent Circuit of y-parameter

In the case of the actual catalogue, i, f, r and o are followed by a grounding symbol: e for emitter grounding as y_{ie}, y_{fe}, y_{re}, y_{oe}; b for base grounding as y_{ib}, y_{fb}, y_{rb}, y_{ob}.

Moreover, since the y-parameter is a complex volume, it is indicated by either of the following methods:

1) The method of indication by an absolute value and a phase angle
   ..... $y = |y| \angle \phi$
2) The method of indication by a real number part (conductance) and an imaginary number part (susceptance)
   ..... $y = g + jb$
3) The method of indication as a capacity by dividing the imaginary number part described in Item 2) by an angle frequency
   ..... $y = g + j\omega c$ (Indicated as a negative capacity in the case of an inductive circuit)

   Generally, Item 2) is often employed by a graphical manner.

3.2 Design of High Frequency Amplifying Circuit

Then, we will show an example of actual RF amplifier design in the following, citing an instance of 2SC 1674 for FM RF amplifier.

At first, it is necessary to know not only the characteristics of the RF amplifier using 2SC1674 under the aimed frequency and bias conditions but also the circuit for obtaining those characteristics.

When an RF amplifier in a completely one-way state is assumed, disregarding the feedback component of elements, MAG (Maximum Available Gain) is represented by the following equation (for $g_S = g_i$ and $g_O = g_L$):

$$MAG = \frac{|y_f|^2}{4g_i g_o} \quad \text{..... Eq. 1}$$

On the other hand, the power gain in an unmatched state is represented by the following equation:

$$G_p = \frac{4|y_f|^2 g_S g_L}{(g_i + g_S)^2 (g_O + g_L)^2} \quad \text{..... Eq. 2}$$

where

g_i . . . Input conductance of element

g_o . . . Output conductance of element

g_s . . . Signal source conductance

g_L . . . Load conductance

When the y-parameters of 2SC1674 are read out of Fig. 2 in order to know the standards of the characteristics in the case where 2SC1674 is used as an RF amplifier by means of the above equation, Table 2 will be given.

From Eq. 1, the following maximum available power gain of 2SC1674 is derived:

$$G_{pe(max)} = \frac{|Y_f|^2}{4g_i g_o} = \frac{31.3^2}{4 \times 1.2 \times 0.07} = 2915$$

$$(\fallingdotseq 34.6\ dB)$$

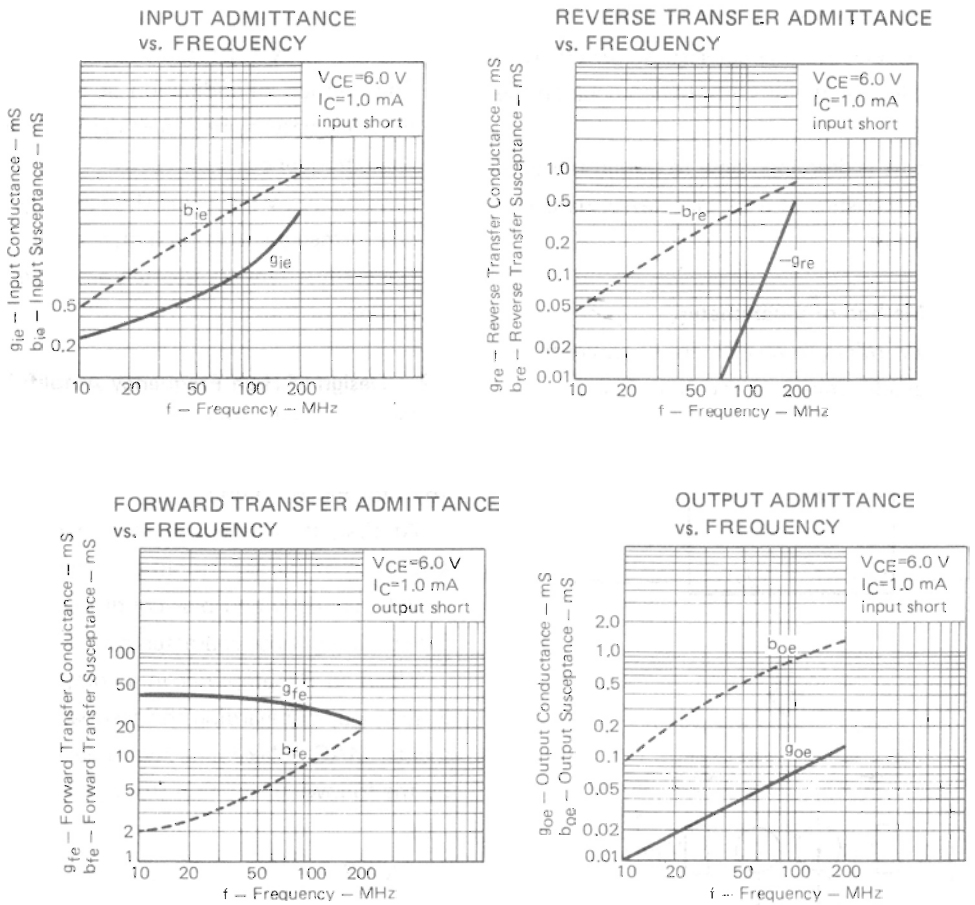


Fig. 2 y-parameter of 2SC1674

Table 2 y-parameter of 2SC1674

*y = g + jb

g_{ie}	b_{ie}	g_{fe}	b_{fe}	g_{re}	b_{re}	g_{oe}	b_{oe}
1.2	5.0	30	9.0	–0.04	–0.45	0.07	0.85

Conversion

*y = |y| ∠ϕ

$\|y_{ie}\|$	$\angle\phi_{ie}$	$\|y_{fe}\|$	$\angle\phi_{fe}$	$\|y_{re}\|$	$\angle\phi_{re}$	$\|y_{oe}\|$	$\angle\phi_{oe}$
5.14	76.5	31.3	16.7	0.45	–95.0	0.85	85.3

Test Conditions: V_{CE}=6 V, I_C=1 mA, f=100 MHz

In actual circuits, however, it is necessary to make mismatching between the signal source of the circuit, the load conductance and the input/output conduactance of elements in order to minimize the required band width, stability and NF.

Therefore, it is impossible from a practical point of view to obtain the maximum available power gain of elements.

When 2SC1674 is used as an RF amplifier, in the second place, the characteristics as a circuit are as follows:

Although it is preferable in essence to provide a tuning circuit in input/output in order to better the characteristics as a circuit, tuning is often made only on the output side in general cases. Accordingly, the tuning system is mostly determined.

Fig. 3 is the circuit diagram of an RF amplifier using 2SC1674, and the condition is that V_{CC} = 6 V, I_C = 1 mA, f = 100 MHz and it is a circuit of emitter grounding and output tuning type.

The constants of C_1 and C_2 in Fig. 3 are variable on the experimental stages, and they are finally made concentrated constants, selecting a state in which the synthetic characteristics as a circuit is good.

(Normally, the minimum point of NF is found out, and it is replaced with a concentrated constant.)

As clear from the above description, it is necessary in designing a high frequency circuit not to design a circuit by computation but to confirm the basis of experimentally obtained characteristics by computation.

Upon the consideration of this, it is computed as follows, how far the power gain can be obtained by the circuit shown in Fig. 3:

At first, the signal source conductance and the load conductance of the circuit are obtained.

Although the signal source conductance is determined by the coupling condensor of input and by the terminating resistance of 50 Ohms, it is determined in principle solely by the terminating resistance of 50 Ohms (20 mS) for thecoupling condensor is nearly shortcircuited at f = 100 MHz because it is 10 000 pF. The load conductance is determined by the tank circuit, coupling condensor and terminating resistance.

At first, the tank circuit is tuned to 100 MHz, and if it is assumed that the impedance in this case is infinite, then it can be disregarded. Therefore, the load conductance is determined by the coupling condensor of 4 pF and the terminating resistance of 50 Ohms.

In consequence, the load conductance can be obtained, as shown in Fig. 4.

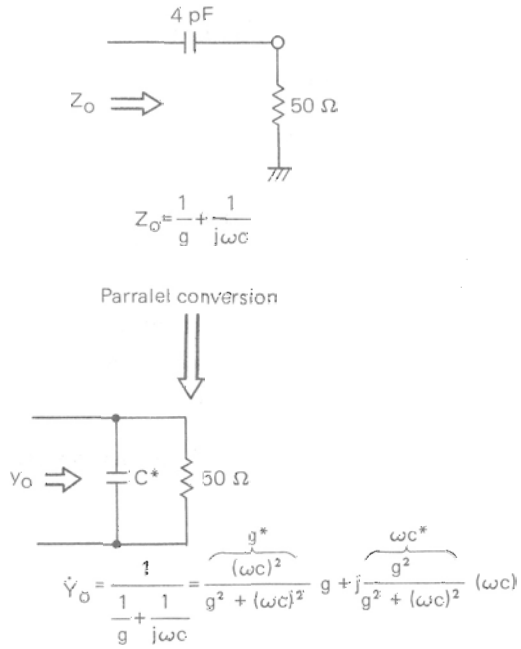


Fig. 4 Parallel Conversion of Load Conductance

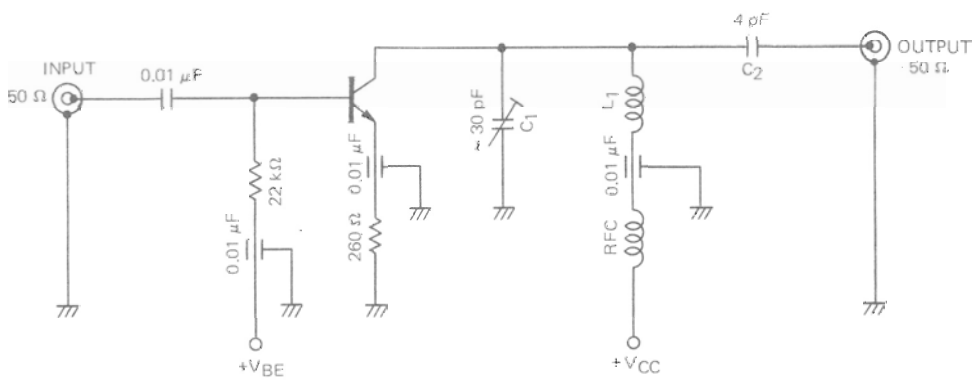


Fig. 3 100 MHz G_{pe}, NF Test Circuit

When the load conductance is obtained, taking the real number part (g*) of the equation in Fig. 4 into consideration,

$$g^* = \frac{(\omega c)^2}{g^2 + (\omega c)^2}\, g$$

$$= \frac{(2\times\pi\times100\times10^6\times4\times10^{-12})^2\times20\times10^{-3}}{(20\times10^{-3})^2 + (2\times\pi\times100\times10^6\times4\times10^{-12})^2}$$

$$= 0.31 \text{ mS.}$$

Thus, the power gain for the circuit of 2SC1674

$$G_{pe} = \frac{4|y_f|^2 g_S g_L}{(g_i + g_S)^2 (g_O + g_L)^2}$$

$$= \frac{4\times31.3^2\times20\times0.31}{(1.2 + 20)^2\times(0.07 + 0.31)^2}$$

$$= 374.4 \ (\fallingdotseq 25.7 \text{ dB})$$

is derived from Eq. 2. Therefore, the power gain of 25.7 dB can be obtained.

However, since Eq. 2 does not include the insertion loss of feedback loss of the tank circuit, the power gain in actuality is less than 25.7 dB.

As a result of the measurement of the characteristics in the case where 2SC1674 is used as an RF amplifier, the following values are obtained.

G_{pe}	@V_{CE}=6 V, I_C=1 mA, f=100 MHz	22 dB
NF	"	3.0 dB

THE USE OF SAFE OPERATING AREA

NEC Silicon Signal transistors are used for vorious drivers and output circuits in audio applications. This document describes outlines of their transient safe operating areas.

1. DESCRIPTION OF SOA (SEE FIG. 1.)

1-1 Current limit

- This is the limitation imposed by h_{FE} and V_{CE} (sat) characteristics against collector current and by to levable current through bonding wire.

1-2 Dissipation Limit

- This is the limitation imposed by thermal resistance (total dissipation).
- Derate the limit according to ambient temperature Ta and duty cycle.

1-3 S-B Limit

- This is the limitation imposed by current concentration.
- Since the thermal resistance rapidly increases around this limit, the repetitive pulse application is needed, derate collector current by 40%.
- Derate the limit according to ambient temperature.

1-4 Voltage Limit

- This is the limitation imposed by V_{CEO} max.

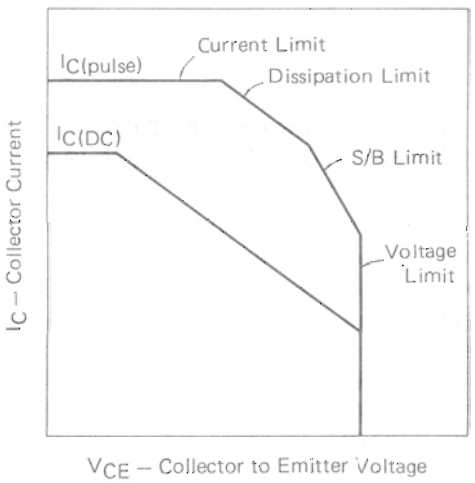


Fig. 1 EXAMPLE OF SAFE OPERATING AREA

2. DERATING ACCORDING TO AMBIENT TEMPERATURE

- The safe operating area (SOA) described in catalogue is for ambient temperature Ta of 25 °C. Therefore, for ambient temperature higher than 25°C, derating is needed. For example, let us derate for Ta of 50°C. First, use safe operating area derating curve in Fig. 2, and obtain a derating factor K of 0.8. Multiply this value to the current in the safe operating area.

  Fig. 3 shows the examples of derating.

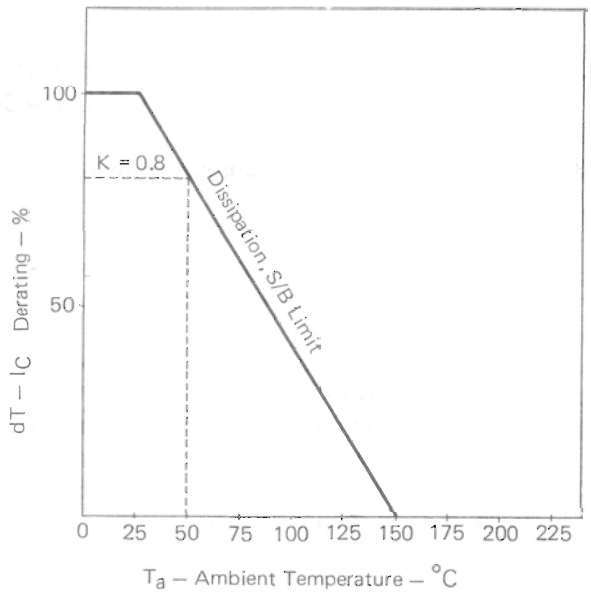


Fig. 2 DERATING CURVE FOR SAFE OPERATING AREA

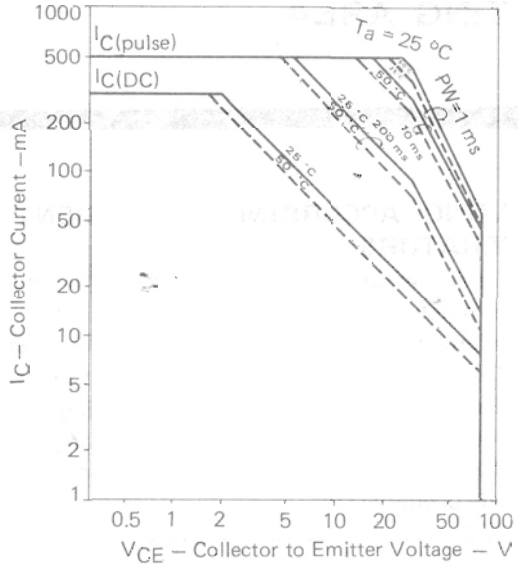


Fig. 3 EXAMPLE OF DERATING WITH AMBIENT TEMPERATURE

3. SIMPLE CALCULATION OF JUNCTION TEMPERATURE IN TRANSIENT CHARACTERISTICS

3-1 Rectangular Waveform Approximation of Transient Power Waveform

- The descriptions given above only apply to rectangular power waveform application. While, the actual waveform is not necessarily be rectangular but usually complex.
  In an actual application, the complex waveform is approximated with a rectangular waveform of which peak value is kept to the original peak value and of which mean power loss is the same as that of the original waveform. Then the calculation described in 3-2 is applied to obtain junction temperature. Fig. 4 shows an example of the approximation.

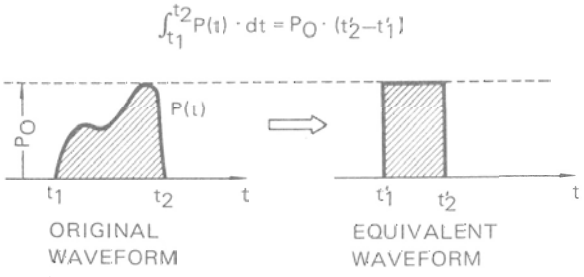


Fig. 4 EXAMPLE OF TRANSFORM TO EQUIVALENT RECTANGULAR WAVEFORM FROM COLLECTOR POWER LOSS WAVEFORM

3-2 Junction Temperature Calculation with Approximated Rectangular Waveform

3-2-1. Variation of Junction Temperature Tj (t) when Single Shot Power Pulse is Applied and the Calculation Example

- When a pulsive power loss as shown in Fig. 5 is applied, T_{j1} (t) for $t_o < t < t_1$ will be

$$T_{j1}(t) = R_{th}(t_1) \cdot P + T_a \quad (1)$$

For the period $t > t_1$, the situation is considered to be the same as the case where an infinitely long positive stepwise power loss P were applied from $t = t_o$ and another infinitely long negative stepwise power loss were applied from $t = t_1$. Superposition principle leads to T_{j3} (t) for $t > t_1$ such that

$$T_{j3}(t) = P \cdot [R_{th}(t) - R_{th}(t - t_1)] + T_a \quad (2)$$

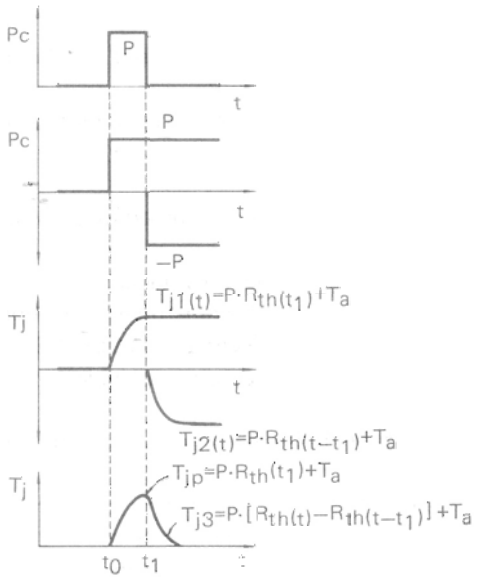


Fig. 5 CALCULATION OF JUNCTION TEMPERATURE WHEN PULSE IS APPLIED

3-2-2 Calculation of Junction Temperature When Repetitive pulsive Power Loss is Applied

- Also in this case, the procedure described in 3-2-1 applies, and the following formulas can be deduced.

$$T_j(t1) = P \cdot R_{th}(t_1) + T_a \quad (3)$$

$$T_j(t_2) = P[R_{th}(t_2) - R_{th}(t_2 - t_1)] + T_a \quad (4)$$

$$T_j(t_3) = P[R_{th}(t_3) - R_{th}(t_3 - t_1) + R_{th}(t_3 - t_2)] + T_a \quad (5)$$

The maximum peak junction temperature T_{jp} reaching the equilibrium with continuous pulse application will be

$$T_{jp} = P[t_p/t_o \cdot R_{th}(j-a) + (1 - t_p/t_o) \cdot R_{th}(t_p + t_o) - R_{th}(t_o) + R_{th}(t_p)] + T_a \quad (6)$$

Fig. 6 shows the junction temperature variation for continuously repetitive pulse application. Rth (t_0), Rth (t_1), Rth (t_2), ——— Rth (t_p) are obtained from the transient thermal resistance characteristic curve ΔR_{th}—PW as shown in Fig.7.

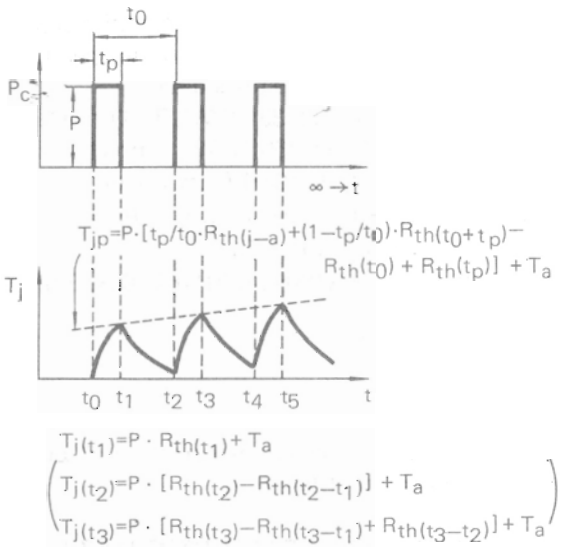


Fig. 6 METHOD OF DETERMINING JUNCTION TEMPERATURE WHEN POWER IS REPEATLY APPLIED

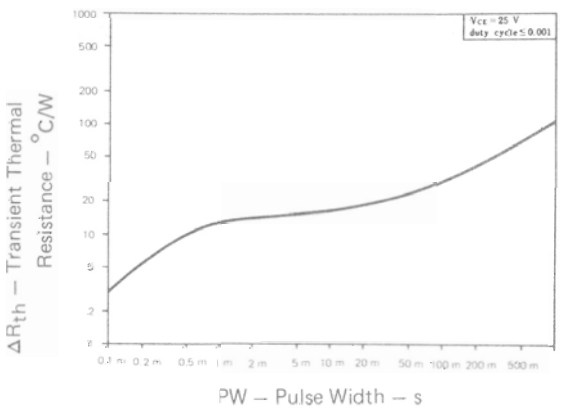


Fig. 7 EXAMPLE OF TRANSIENT THERMAL RESISTANCE CHARACTERISTICS

4. SOA CONFIRMATION BY MEANS OF EXAMPLES

4-1 Example of Lamp Drive

○ The operation model of Fig. 8 (a) is approximated by (b) of the figure where mean power loss is the same and the junction peak temperature is calculated. Equation (6) is used for the calculation.

$$T_{jp}=P[t_p/t_o \cdot Rth\ (j–a)+(1–t_p/t_o)\cdot Rth\ (t_p+t_o) –Rth\ (t_o) + Rth\ (t_p)] + Ta$$

2SC2001 is taken as an example. The transient thermal resistance for t_p=1 ms, t_o=100 ms, and $t_o + t_p$=101 ms from (a) of Fig. 12

P=5 W, Rth (j–a)=208.33 (°C/W)
Rth (t_p=1 ms)=12.2 (°C/W)
Rth (t_o=100 ms)=30(°C/W)
Rth (t_p+t_o=101 ms) ≒ 30 (°C/W)
t_p/t_p=1/100=0.01 (duty cycle)

$$T_{jp}=5x[0.01x208.33+(1–0.01)x30–30+12.2] +Ta$$
$$=5x13.98+Ta$$
$$=70+Ta$$

This means that the transistor can be continously used up to an ambient temperature Ta=150–70= 80 °C, provided that $T_{jp} \leqq 150$ °C is satisfied. The fact that requires cautions the most in lamp drive is the rush current for lamp on. But, since the hold time of I_{cp} is, in most cases, several tens μs through several hundred μs, I_{cp} of up to about 3 A is tolerable if the junction temperature obtained above is less than 150 °C.

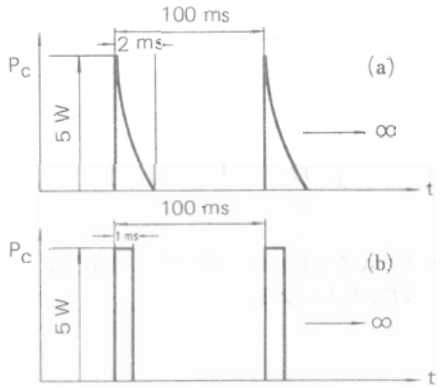


Fig. 8 EXAMPLE OF TYPICAL OPERATING LOCUS FOR LAMP DRIVE

4-2 Example of Relay Drive

○ In this case, similar to the lamp drive, the rectangular waveform approximation is carried out, and, transient thermal resistance is derived from transient thermal resistance characteristics for obtaining the junction peak temperature. The operating locus such as shown in Fig. 9 can be assumed to the relay drive.

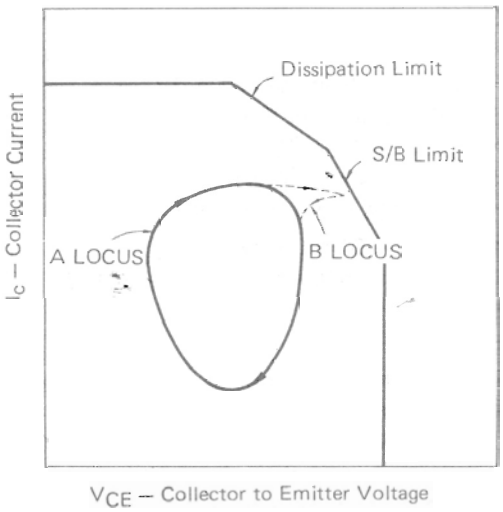


Fig. 9 EXAMPLE OF TYPICAL OPERATING LOCUS FOR RELAY DRIVE

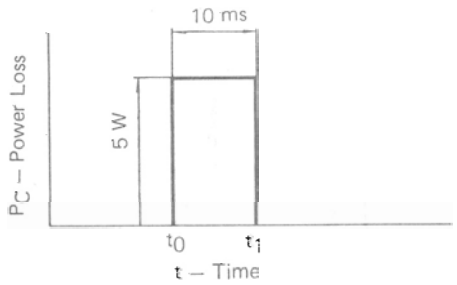


Fig. 10 EXAMPLE OF TYPICAL SINGLE SHOT POWER LOSS

4-2-1

- For A-locus in Fig.9, the locus is in the dissipation limit region and, if the calculated peak junction temperature is lower than 150 °C, the repetitive power loss can be applied.

4-2-2

- For B-locus in Fig. 9, which is close to S/B limit, the operating should be considered as follows.
  2SC2002 or 2SC 2003 is taken as example, in here.
  (1) When a single shot power loss such as shown is Fig. 10 is applied, use Equation (1) of 3-2-1 to obtain instantaneous junction temperature ΔT_j (t_1).
  $\Delta T_j(t_1)=Rth(t_1)\cdot P+Ta$
  Obtain transient thermal resistance Rth (10 ms) from transient thermal resistance characteristic curve (B currse) shown in Fig. 12 (c).
  $\Delta T_j(t_1)=5x19+Ta$
  $=95+Ta$
  This means that a single shot power loss application is permitted for an ambient temperature of up to Ta=150–95=55 °C. The condition of single shot pulse is actually realized if the junction temperature after the power loss application is satisfactorily lowered to the level before the application when the next pulse comes.
  (2) When pulses are repetitively applied, obtain transient thermal resistance from transient thermal resistance characteristic curve (curve C) in Fig. 12 (C) and use Equation (6) for the repetitive application to calculate the peak junction temperature. In here, a model of Fig. 8 (b) is used.
  [P=5.0 W, Rth(j–a)=208.33(°C/W), Rth(1 ms)=23.5 (°C/W), Rth(100 ms)=69(°C/W), Rth (100 ms+ 1 ms)=69(°C/W), t_p/t_o=0.01 (duty cycle)]
  $T_{jp}=P[t_p/t_o\cdot Rth(j-a)+(1-t_p/t_o)\cdot Rth(t_p+t_o)-Rth(t_o)+Rth(t_p)]+Ta$
  $=5.0x[0.01x208.33+(1-0.01)x69-69+23.5]+Ta$
  $=5.0x24.89+Ta$
  $\fallingdotseq 124+Ta$
  This means that repetitive power loss application is permitted for an ambient temperature of up to $Ta=T_{jp}-124=150-124=26$ °C

5. OTHER CHARACTERISTIC DATA

(1) SOA data (Ta=25 °C) and breakdown data for PW=10 ms of 2SC2001–2SC2003 and 2SA952–2SA954 are shown in Fig. 11, (a) through (d).
(2)Transient thermal resistance characteristics Rth-PW of 2SC2001 to 2SC2003 and 2SA952 to 2SA954 are shown in Fig. 12, (a) through (d).

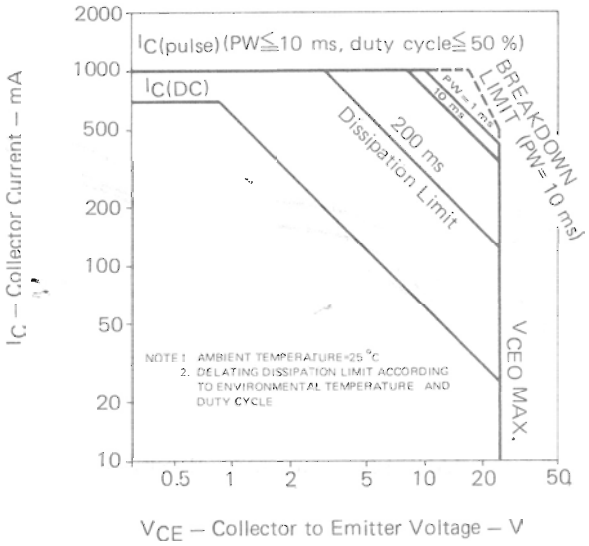


Fig. 11 (a) SAFE OPERATING AREA OF 2SC2001

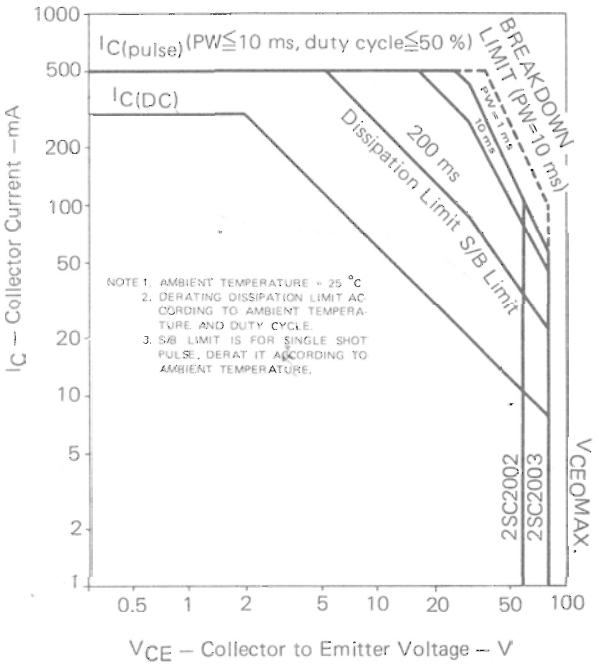


Fig. 11 (c) SAFE OPERATING AREA OF 2SC2002, 2SC2003

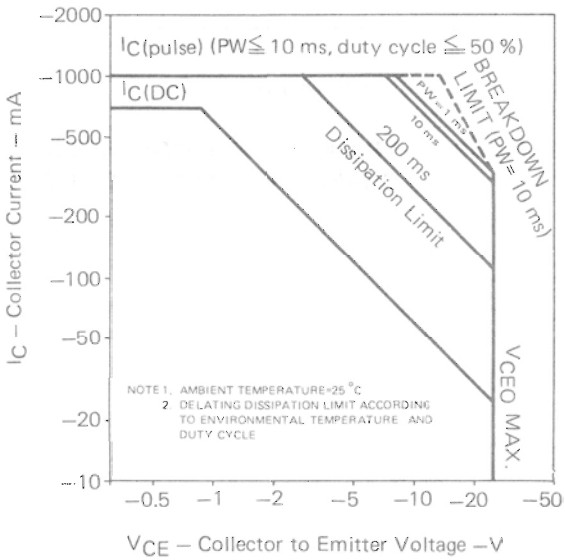


Fig. 11 (b) SAFE OPERATING AREA OF 2SA952

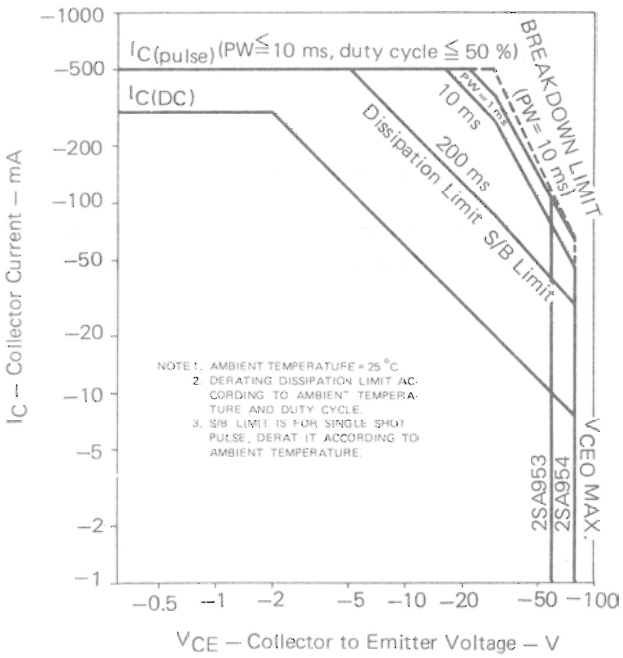


Fig. 11 (d) SAFE OPERATING AREA OF 2SA953, 2SA954

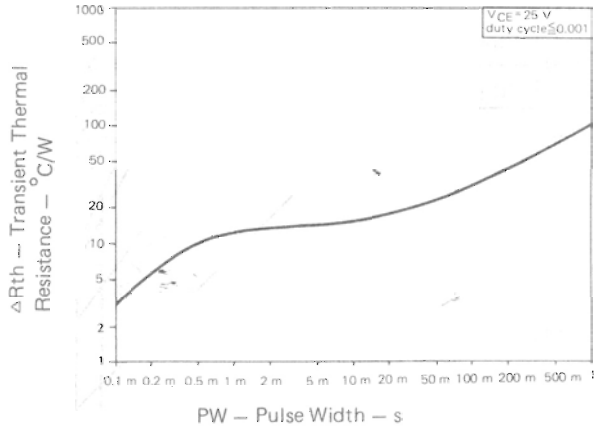


Fig. 12 (a) TRANSIENT THERMAL RESISTANCE CHARACTERISTIC OF 2SC2001

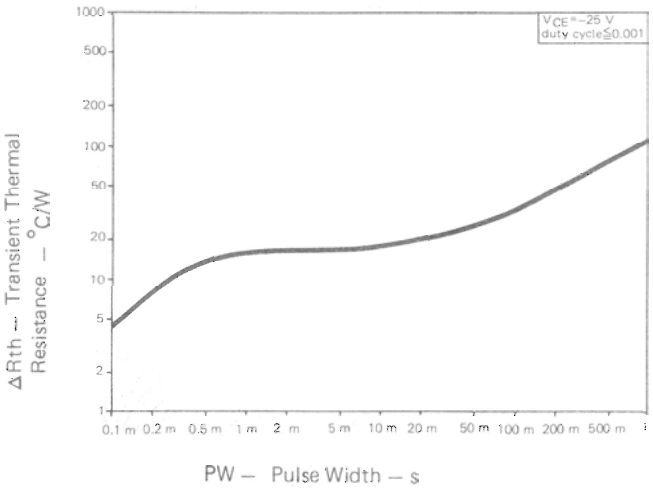


Fig. 12 (b) TRANSIENT THERMAL RESISTANCE CHARACTERISTIC OF 2SA952

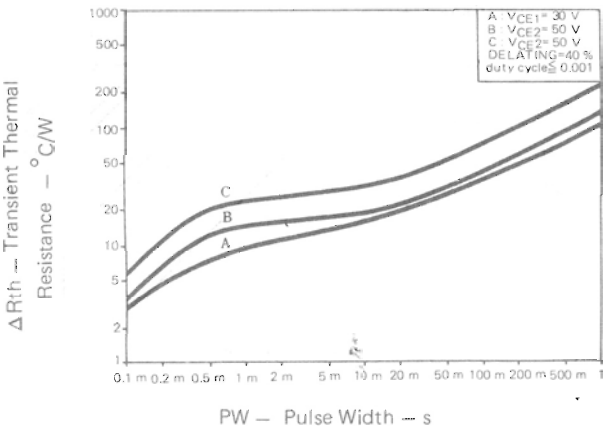


Fig. 12 (c) TRANSIENT THERMAL RESISTANCE CHARACTERISTIC OF 2SC2002, 2SC2003

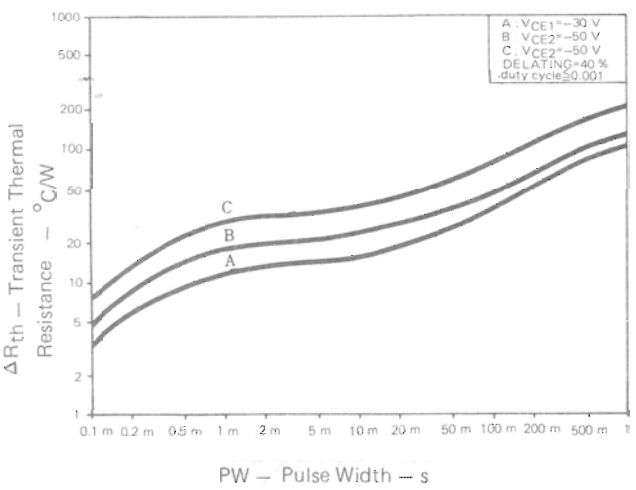


Fig. 12 (d) TRANSIENT THERMAL RESISTANCE CHARACTERISTIC OF 2SA952, 2SA953

4 V GATE-DRIVEN POWER MOS FET WITH LOW DRAIN TO SOURCE ON-STATE RESISTANCE

1. INTRODUCTION

2. DEVICE STRUCTURE

3. FEATURES

4. ABSOLUTE MAXIMUM RATINGS AND CHARACTERISTICS

5. APPLICATION EXAMPLES FOR POWER MOS FET

6. HANDLING NOTES

7. CONCLUSION

1. INTRODUCTION

This manual introduces NEC's 4 V Gate-Driven Power MOS FET devices with low drain-to-source on-state resistance. These devices feature miniaturization, low power dissipation, and multiple functions.

2. DEVICE STRUCTURE

A power MOS FET (Metal Oxide Silicon Field Effect Transistor) device has several thousand to several ten thousand MOS FET cells (one MOS FET transistor) that are connected in parallel. See Photo 1.

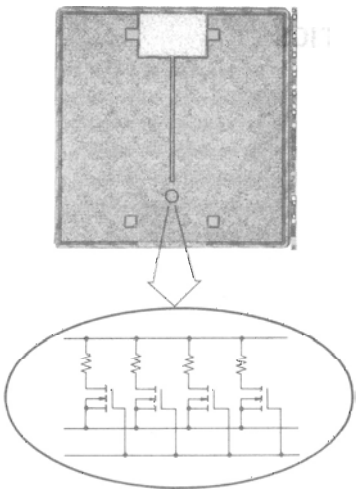


Photo 1. Power MOS FET Device and Individual Circuits

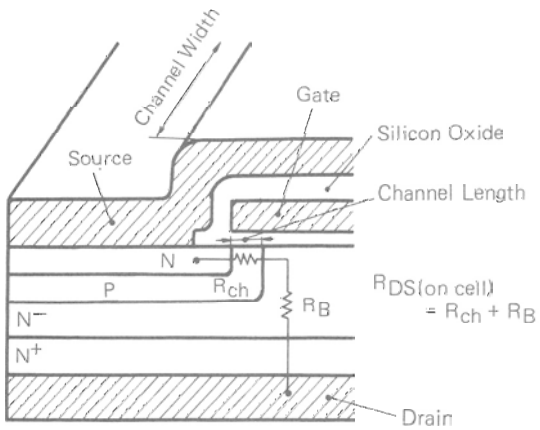


Fig. 1 Cross Section of Power MOSFET Cell

The combined drain-to-source on-state resistance $R_{DS(on)}$ of an MOS FET device, shown in figure 1 equals the resistance of one branch (MOS FET cell) divided by the number of branches.

$$R_{DS(on)} = 1/n \times R_{DS(on)} \text{ of one cell}$$

Where n = the number of MOS FET cells

The drain-to-source on-state resistance of a single MOS FET cell $R_{DS(on)cell}$ is given by

$$R_{DS(on)cell} = R_{ch} + R_B$$

where

R_{ch} = on-state resistance of the inversion channel formed by the bias voltage between the gate and the source, and

R_B = resistance inversely proportional to the amount of impurity in the N^- silicon layer.

Resistance R_B is the factor most dependent upon impurities in the N^- silicon layer. Generally, the break voltage BV_{DSS} increases with impurity of the N^- layer. Accordingly, there is a tradeoff between resistance R_B and break voltage BV_{DSS}.

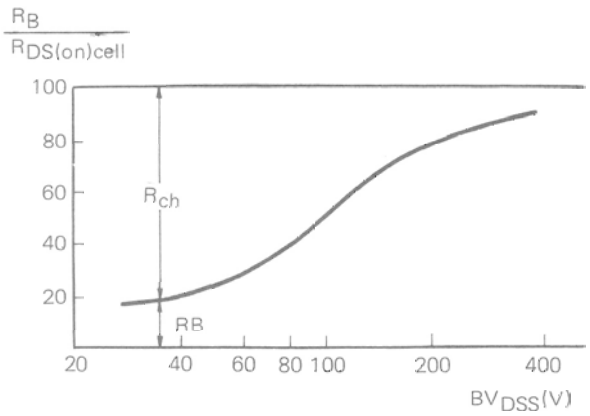


Fig. 2 $R_B/R_{DS(on)cell}$ versus BV_{DSS}

Figure 2 shows the relationship between break voltage, BV_{DSS}, of the power MOS FET device and drain-to-source on-state resistance of the MOS FET cell, $R_{DS(on)\ cell}$. When BV_{DSS} is 200 volts or higher, R_B is dominant. When BV_{DSS} is 100 volts or lower, R_{ch} is dominant.

The drain-to-source on-state resistance of a MOS FET device is represented by the product of chip area and drain-to-source resistance ($A \times R_{DS(on)}$; $mm^2 \cdot \Omega$).

Figure 3 shows the $A \cdot R_{DS(on)}$ versus BV_{DS} characteristic of the 4 V Gate-Driven Low on-state Resistance MOS FET device. The $A \cdot R_{DS(on)}$ value of this MOS FET device is 55 % higher than that of conventional devices.

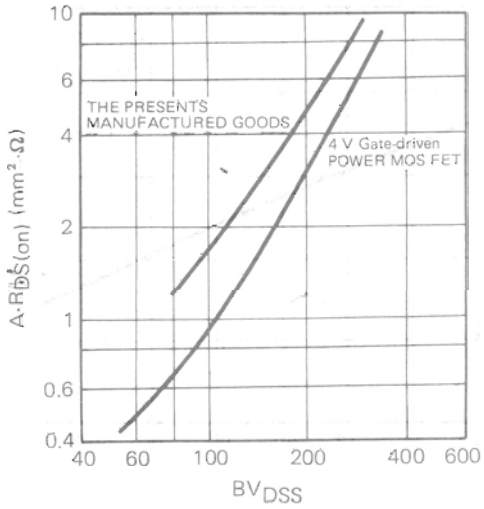


Fig. 3 $A \cdot R_{DS(on)}$ Versus BV_{DSS}

To drive a power device with a voltage level of 4 volts, it is necessary to lower the threshold voltage (or the minimum operating voltage if the gate-to-source voltage, V_{GS}, is higher than the threshold voltage). For this purpose, it is necessary to precisely control the amount of impurity in the channel layers and the thickness of the gate oxide. NEC achieved a 4-volt device drive and reduced drain-to-source on-state resistance by:

- Optimum design based on computer simulation and experiments, and
- Up-to-date precision processing techniques for LSI devices.

NEC's 4 V Gate-Driven Low On-State Resistance Power MOS FET devices have the best performance achieved to date.

3. FEATURES

The NEC 4 V Gate-Driven Low On-State Resistance MOS FET device features:

1) Ability to be driven directly by 5-volts power ICs, such as HCMOS ICs;
2) Low drain-to-source On-State Resistance in this new generation of power MOS FET devices having higher chip efficiency; and
3) Wider safe operating range without secondary breakdown.

4. ABSOLUTE MAXIMUM RATINGS AND CHARACTERISTICS

This section describes only those ratings and characteristics that differ from those of conventional power MOS FET devices.

1) Absolute Maximum Ratings

Table 3 shows absolute maximum ratings of the 2SK591 power MOS FET (drain current of 15 A and drain-to-source voltage level of 60 V). The 2SK591 differs from bipolar transistors and conventional power MOS FET devices in its pulse drain current, with an I_D (pulse) of 60 A and I_D (DC) of 15 A.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	60 V
Gate to Source Voltage	V_{GSS}	20 V
Drain Current (DC)	I_D(DC)	15 A
Drain Current (pulse)	I_D(pulse)	60 A
Total Power Dissipation	P_T *1	35 W
Total Power Dissipation	P_T *2	2.5 W
Channel Temperature	T_{ch}	150 °C
Storage Temperature	T_{stg}	55~150 °C

*1; T_C = 25 °C *2; T_a = 25 °C

Table 3. 2SK591 Absolute Maximum Ratings

The drain-to-source On-State Resistance of each MOS FET cell (see section 2) has a positive temperature coefficient. If one MOS FET cell is supplied current exclusively, the drain-to-source on-resistance, $R_{DS(on)cell}$, of the cell increases to suppress the incoming current. Thus the cell is protected against destruction due to local heating. Contrarily, bipolar transistors suffer local breakdown (secondary breakdown) if one specific part is fed current exclusively; temperature dependence of the DC current gain, h_{FE}, is positive and the heated part accepts more current.

Accordingly, the power MOS FET device is more resistant to overload than are bipolar transistor devices.

Figure 4 shows forward bias Safe operating area of the 2SK591.

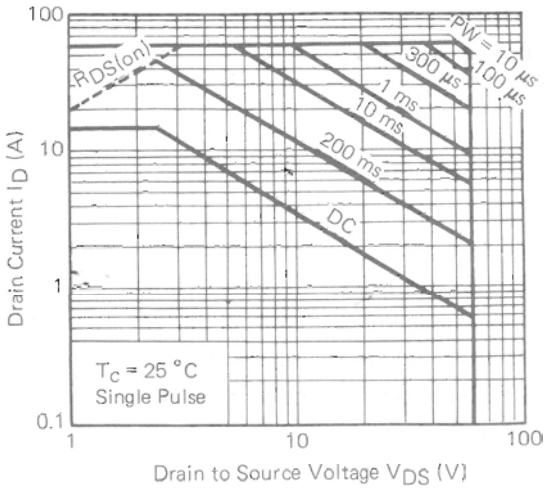


Fig. 4. Forward Bias Safe Operating Area

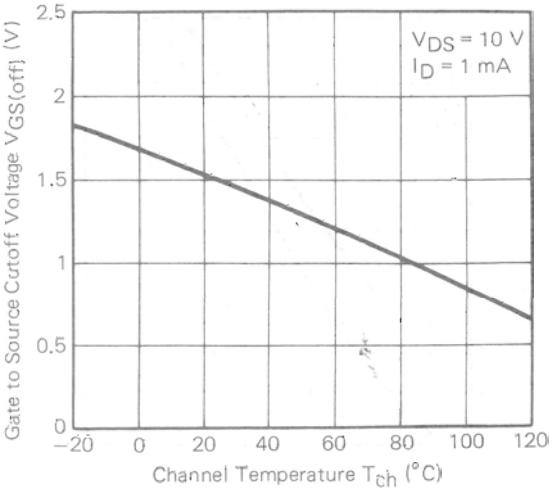


Fig. 6. Gate to Source Cutoff Voltage vs. Channel Temperature T_{ch} (°C)

2) Characteristics

Figure 5 shows the drain-to-source on-state resistance versus gate-to-source voltage, $R_{DS(on)}$—V_{GS}. The drain-to-source on-state resistance of the MOS FET device is fully saturated at 4 V.

Figure 6 shows the gate-to-source cutoff voltage versus channel temperature. A 4 V Gate-Driven MOS FET device having low threshold voltage has an adequate noise margin in the range of −40 to 150 °C.

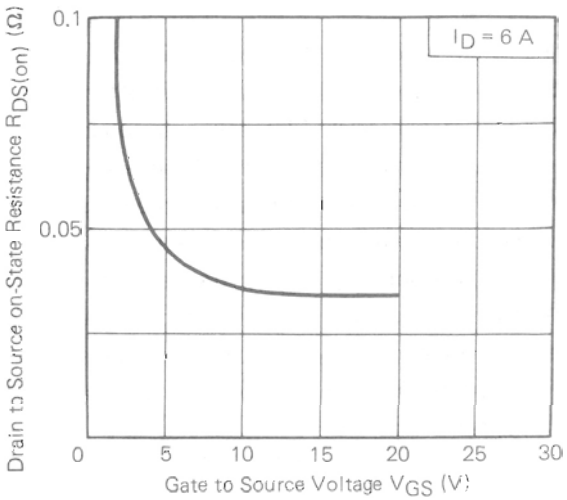


Fig. 5. Drain to Source On-State Resistance vs. Gate to Source Voltage

Figure 7 shows drain-to-source on-state resistance versus channel temperature. As already described, the temperature dependence of the MOS FET device is positive. Accordingly, MOS FET cells connected in parallel in the MOS FET device operate stably, and MOS FET devices connected in parallel operate stably.

Figure 8 shows the saturation voltage versus current characteristics of Darlington transistors 2SD560 and 2SK702, which are compatible with the 2SD560. The saturation voltage of the 2SK702 is lower than that of the 2SD560 in the range of two-thirds or less of the rated current. It is apparent that the 2SK702 has lower power dissipation. Because the drain-to-source on-state resistance of the power MOS FET device is inversely related to breakdown voltage, BV_{DSS}, the saturation voltage of the 2SK704 (for 60 V) is much lower.

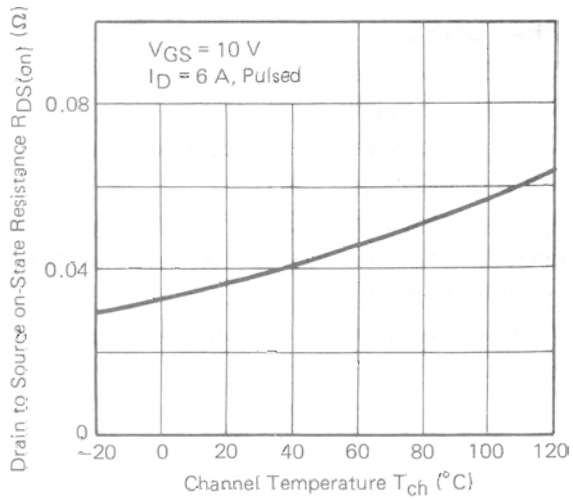


Fig. 7 Drain to Source on-State Resistance vs. Channel Temperature

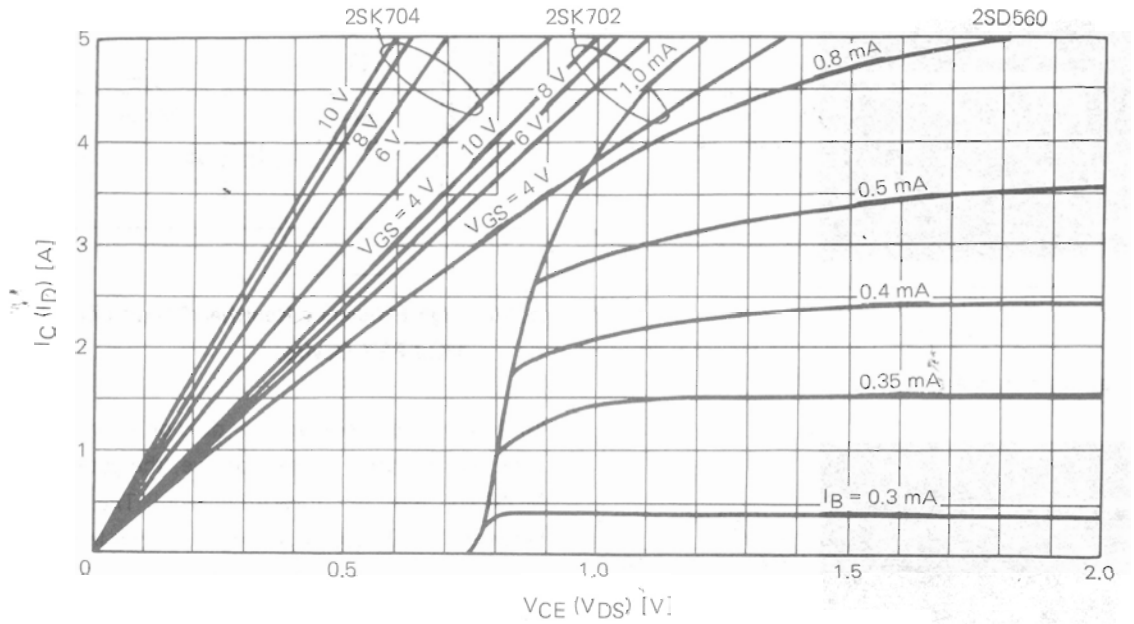


Fig. 8 V_{CE}–I_C and V_{DS}–I_D of Bipolar Transistor Power MOSFET

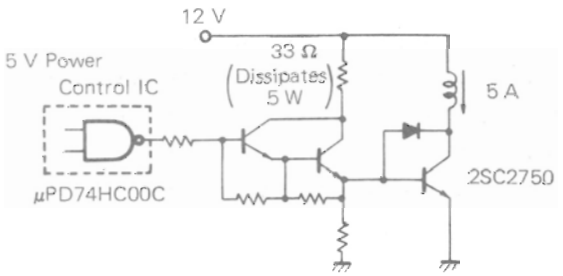
5. APPLICATION EXAMPLES FOR POWER MOS FET

1) Actuator Driving Circuit

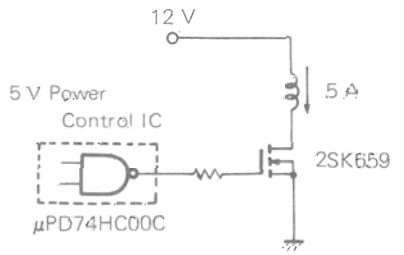
The 4 V Gate-Driven Low On-State Resistance Power MOS FET, which can be directly driven by a 5-V power IC, can be used as a driver for a switching regulator, actuator (such as solenoid, relay, motor, etc.), or indicator. Figure 9 shows a solenoid driver using the MOS FET device (power supply of 12 V) and a solenoid driver using bipolar transistors. The solenoid driver using bipolar transistors requires a base current strong enough to lower the saturation voltage of the main transistor. Accordingly, the base resistor dissipates 5 W of energy. Semiconductor devices should be kept well away from this base resistor. A rather large installation space is thus required by this circuit. Another stage of a Darlington transistor is required to control the main transistor by the control IC because the DC current gain h_{FE} is not sufficient.

The solenoid driver using the 4 volts Gate-Driven MOS FET device, on the other hands enables the control IC to drive the solenoid directly, through only one gate input resistor. This configuration reduces the installation space and power dissipation of the drive circuit and the main circuit.

Photo 2 shows the switching waveforms of the power MOS FET for various gate input resistances. Switching is performed in proportion to the product of gate input resistance, R_G and the power MOS FET gate's input capacitance, C_{ISS}. To eliminate radio frequency noise from peripherals (if any), reduce the switching speed by increasing the input resistance and adding a low-value capacitor.

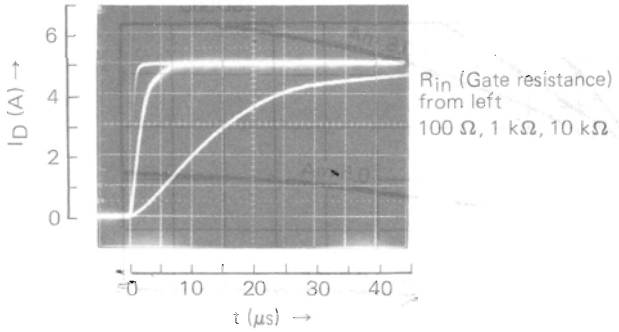


a) Solenoid Driver Using Bipolar Transistor

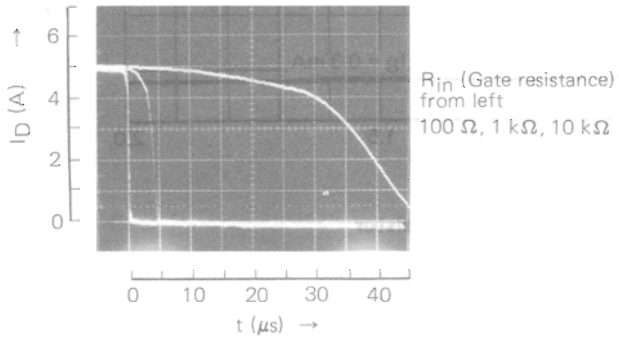


b) Solenoid Driver Using 4 V Gate-Driven MOS FET

Fig. 9 Solenoid Drivers



a) turn-on characteristic



b) turn-off characteristic

Photo 2 Switching Time and Gate Input Resistances of Power MOS FET

2) Rectifier Circuit

As the efficiency of the switching power source improves because of the use of power MOS FET devices, the resulting power dissipation of the secondary rectifier circuit becomes significant. The reduction of the power dissipation is now required.

Figure 10 shows a typical high-efficiency rectifier circuit using two MOSFET devices. Before discussing the operation of the rectifier circuit, we must explain the inversion characteristics between the drain and source caused by gate-biasing of the power MOS FET. Figure 11 shows the inversion characteristics of the power MOS FET. If the gate is reverse-biased or is not biased, the inversion characteristic of the power MOS FET is the forward-voltage versus current characteristic of the body diode. If the gate is forward-biased, the MOS FET in parallel with the body diode conducts and the resistance characteristic of the power MOS FET is the same as the forward on-state resistance characteristic. The rectifier circuit shown in figure 10 uses the above characteristics properly.

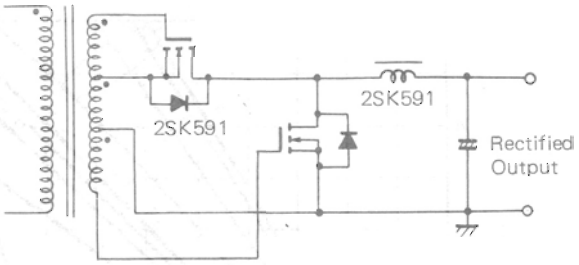


Fig. 10. High-Efficiency Rectifier Circuit Using Power MOS FET Devices

While the points indicated by dots on the transformer windings in figure 10 are positive, the gate of power MOSFET Q_1 is forward-biased. The resistance between the Q_1 source and drain is then low (low on-resistance) and the body diode conducts. The gate of another power MOS FET, Q_2, being reverse-biased, is cut off. Current therefore flows in the sequence of points on the secondary winding of the transformer, power MOS FET Q_1, smoothing coil, and the smoothing capacitor. While the transformer points indicated by dots are negative, the gate of power MOS FET Q_1 is reverse-biased and cut off. A flywheel current intended to flow through the smoothing coil, smoothing capacitor, and body diode of power MOS FET Q_2 is forward-biased and the source-drain resistance is low.

The power MOS FET devices perform rectification in this manner. The body diode is inactive and the resulting inversion recovery time of the body diode is not generated because the voltage drop created by the drain-to-source resistance is much smaller than that of the body diode (when the gate is forward-biased). The 2SK591 4 V Gate-Driven Low On-State Resistance Power MOS FET ($R_{DS(on)}$ of 35 mΩ/45 mΩ, at V_{GS} of 10 V/4 V), with a voltage drop of about 0.2 V at a current of 5 A, is more efficient than any other Schottky-barrier diode (voltage drop of 0.5 V). Figure 12 shows a typical high-efficiency rectifier circuit using two MOS FET devices of a negative power source. This rectifier requires no auxiliary secondary winding of the transformer.

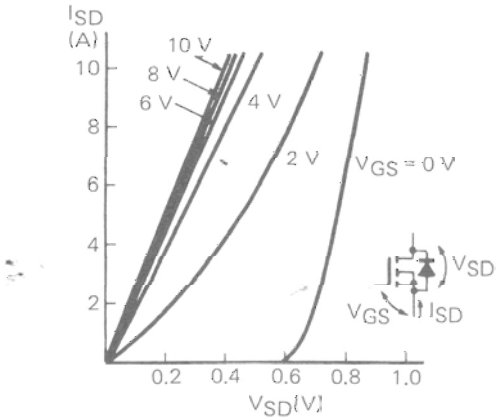


Fig. 11. I_{SD} Versus V_{SD} Characteristics of 2SK591

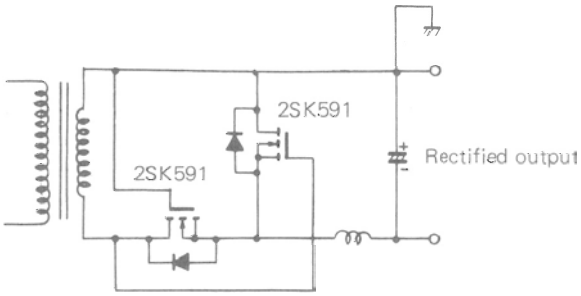


Fig. 12. High-Efficiency Rectifier Circuit Using Power MOS FETs

3) Parallel Connection of Power MOS FET Devices

Power MOS FET devices, which have a positive temperature coefficient for drain-to-source resistance, can be connected in parallel.

Figure 13 shows a typical circuit with power MOS FET devices in parallel. A resistor of less than 100 Ω is connected to the gate of each MOS FET to suppress oscillation. In this circuit, three power MOS FETs are connected in parallel. The combined drain-to-source on-state resistance of this circuit, assuming a load current of 10 A flows, is calculated as follows:

$R_{DS(on)} = 45 \div 3 = 15$ (mΩ)

(V_{GS} of 2SK591 = 4 A)

The overall power dissipation is

$P3 = 10 \times 0.015 = 1.5$ (W)

The power dissipation of one power MOS FET is

$P1 = 1.5 \div 3 = 0.5$ (W)

Note:

The power dissipation of a single power MOS FET is

$P01 = 45 \times 10 = 4.5$ (W)

No cooling fin is required by a circuit having three power MOS FETs in parallel (free-air cooling is sufficient).

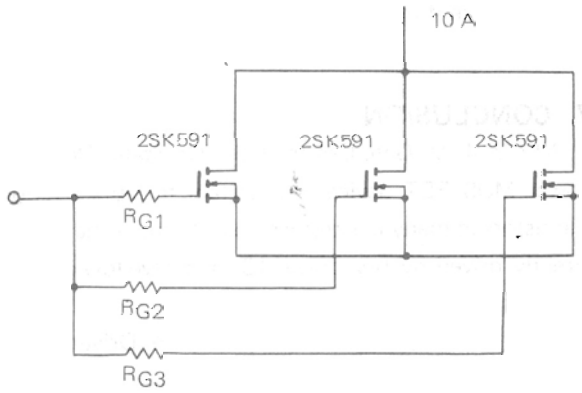


Fig. 13. Circuit with Parallel MOS FETs

6. HANDLING NOTES

1) Avoid Static Electricity.

A surge voltage such as static electricity will destroy the thin insulating silicon oxide between the gate and source of the power MOS FET. Note the following:

a. For storage and transfer of power MOS FET

Always put each device in a bag or wrapper made of conductive material or place it on black conductive foam or aluminum foil.

b. For handling of power MOS FET

Do not touch the gate lead of the power MOS FET.

Hold the body of the device.

Be sure to ground the workbench and floor. It is best to use a wrist strap to dissipate any static charge when handling the devices. A ceramic-tip soldering iron is recommended for soldering device leads. If a surge voltage may possibly be applied to the mounted device, a constant-voltage diode is recommended between the gate and the source of the device.

2) Avoid Overvoltage Between Drain and Source of Power MOSFET.

As already described, the drain-to-source on-resistance of the power MOS FET and breakdown voltage BV_{DSS}, are closely related to each other in an inverse relationship. In design of power MOS FET devices, drain-to-source resistance is made as low as possible, and breakdown voltage is set low in the specified

range. Accordingly the breakdown voltage margin of the power MOS FET is narrower than that of a bipolar transistor. Be careful not to apply any over-voltage to the device. Connect a protective circuit to the device if necessary.

7. CONCLUSION

NEC's 4 V Gate-Driven Low On-State Resistance Power MOS FET devices are certain to replace bipolar transistors in many electronics fields because they can be directly driven by 5-V power ICs and have low drain-to-source on-state resistance.

NEC is ready to provide 4 V Gate Driven power MOS FET devices with lower drain-to-source resistance, using our unique, up-to-date LSI technology.

h_{FE} AND NOISE FIGURE DETERIORATION CAUSED BY E-B JUNCTION BREAKDOWN IN TRANSISTORS

CHARACTERISTIC DETERIORATION CAUSED BY E-B JUNCTION BREAKDOWN IN TRANSISTORS[1)]

When breakdown (avalanche breakdown) is generated by the application of reverse voltage exceeding BV_{EBO} between E-B of transistor, leakage current increases as well as h_{FE} and NF (noise figure) deterioration may result.

The h_{FE} deterioration is considered to be effected by trap centers generated on and around silicon surface by the avalanche breakdown.

When the surface recombination-generation current, (a component of transistor base current) is increased, especially when the recombination-generation current is increased by the recombination-generation centers produced in E-B junction depletion layer around the surface, I_B is increased, and if collector current I_C is kept constant and because $h_{FE} = I_C/I_B$, h_{FE} deterioration results. Another cause of the deterioration is the fact that the surface potential variation due to the avalanche breakdown induced movement of the charge carriers supposed to be present on the boundary of the oxide film and the silicon, or in the oxide film. However it is reported that this is not so dominant. Anyway, h_{FE} deterioration is caused by the trap density increase around the surface of E-B junction. Therefore, for making transistor structures not so susceptible to h_{FE} deterioration, it is fairly useful to reduce crystal dislocation generated during impurity diffusion and reduce impurity concentration on base surface slightly (because too much reduction induces channel generation) in the transistor production processes.

Noise figure deterioration, one of the subjects of this document, arises from h_{FE} deterioration. It is considered as a phenomenon created by h_{FE} linearity deterioration caused by the increase of surface recombination-generation current and the following marked deterioration of h_{FE} in low current region due to avalanche breakdown.

This is evident from the fact that, among equivalent input noise components, only current noise source: i_n (shot noise) is increased and voltage noise source: e_n (thermal noise) is unchanged.

How far these h_{FE} and noise figure deteriorations are influenced by breakdown current and time and to what extent the deteriorated characteristics are recovered by high temperature storage and power aging are described by using measured data of small signal transistors 2SC945 and 2SA733.[2)]

Note: 1) The description of the deterioration applies to silicon epitaxial planer transistors.

2) Because structures are somewhat different between type to type, the deterioration tendencies in other types may be different from the data that will be shown here. Furthermore, the data shown here is obtained from samples picked at random and they predict nothing of the dispersion.

1. h_{FE} DETERIORATION DUE TO E-B JUNCTION BREAKDOWN

Fig. 1 through 3 show how far h_{FE} deteriorates with the current and the duration of E-B breakdown. Fig. 4 and 5 show the degree of recovery of degraded transistor h_{FE} by means of high temperature storage and power aging.

The breakdown duration described in the figures is the total time. h_{FE1}, h_{FE2}, and h_{FE3} as defined by the measured h_{FE} under the following conditions. (Other sections are also defined in the same manner unless otherwise specified.)

Item	Test Conditions
h_{FE1}	V_{CE} = 6.0 V, I_C = 0.1 mA
h_{FE2}	V_{CE} = 6.0 V, I_C = 1.0 mA
h_{FE3}	V_{CE} = 6.0 V, I_C = 10 mA

(Negative sign for PNP type is omitted.)

1-1 h_{FE} Deterioration with Breakdown Duration

The h_{FE} deteriorations relative to breakdown duration time are shown in Fig. 1-1 through 1-3 taking breakdown current I_{break} as a parameter.

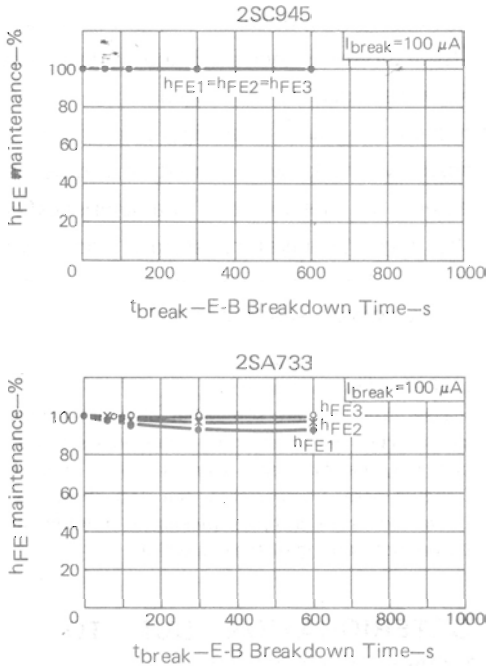


Fig. 1-1 I_{break} = 100 μA

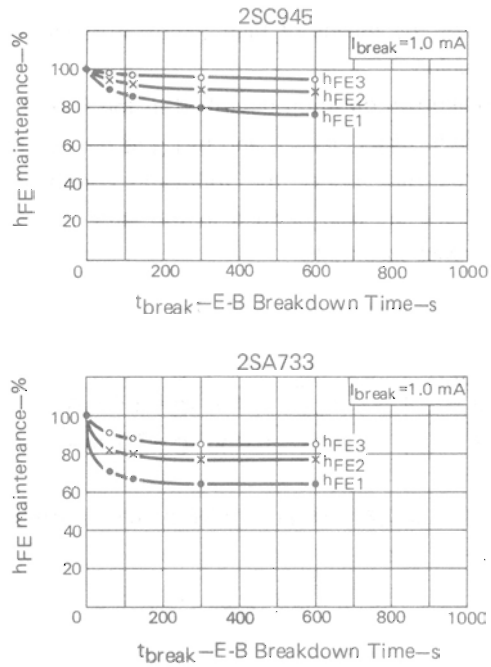


Fig. 1-2 I_{break} = 1.0 mA

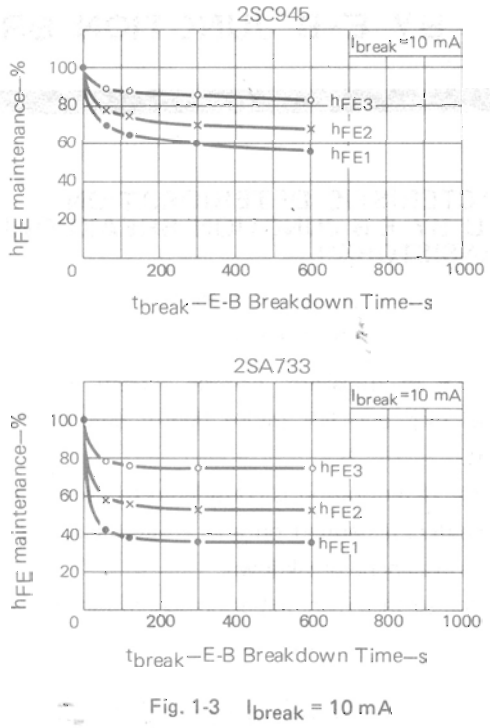
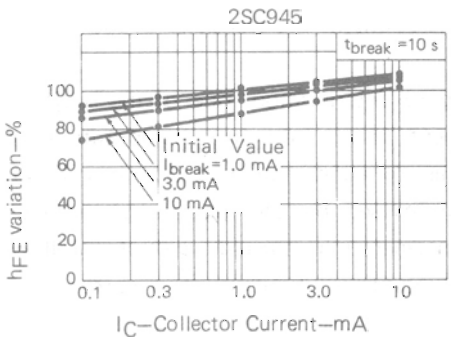


Fig. 1-3 I_{break} = 10 mA

Fig. 1 h_{FE} Deterioration vs. Breakdown Time

1-2. h_{FE} Deterioration with Collector Current Where h_{FE} Is Measured

The h_{FE} deteriorations relative to collector current where f_{FE} measurement is taken as shown in Fig. 2-1 through 2-3 taking t_{break} and I_{break} as parameters, and normalizing with the value at I_C = 1.0 mA.



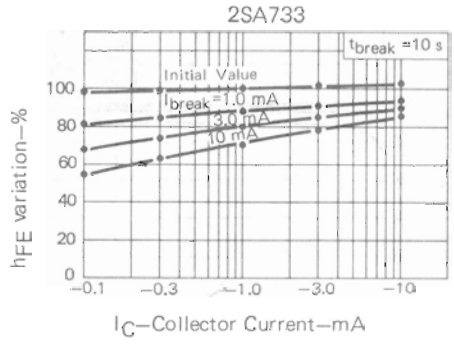
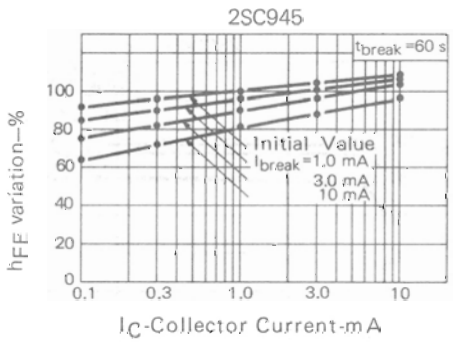


Fig. 2-1 t_{break} = 10 s



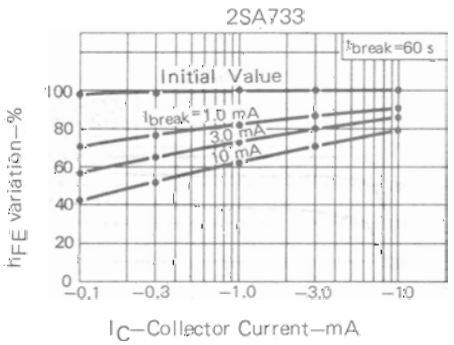
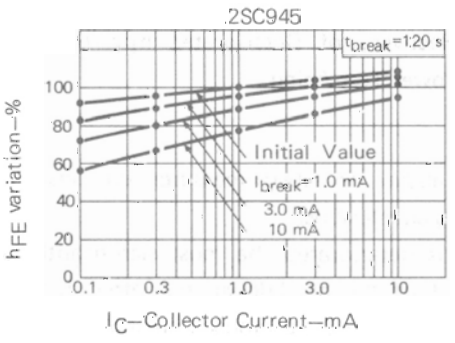


Fig. 2-2 t_{break} = 60 s



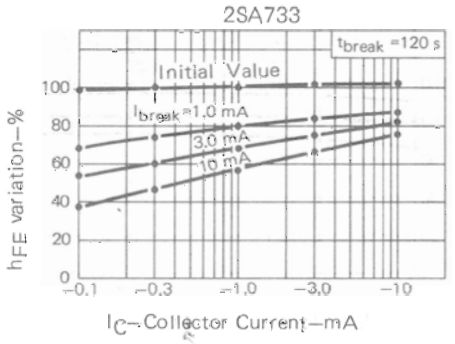
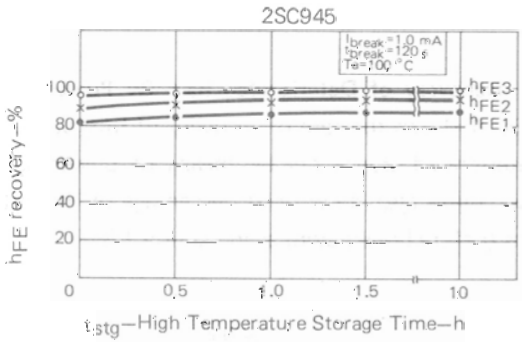


Fig. 2-3 t_{break} = 120 s

Fig. 2 Dependency of h_{FE} Deterioration on h_{FE} Measuring Point

1-3. Recovery of Deteriorated h_{FE} By High Temperature Storage

Fig. 3 shows to what percentage deteriorated h_{FE} can be recovered by high temperature storage of the deteriorated transistors, with initial values (before breakdown) as 100 %.



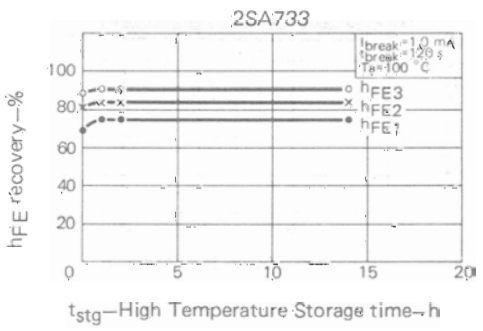
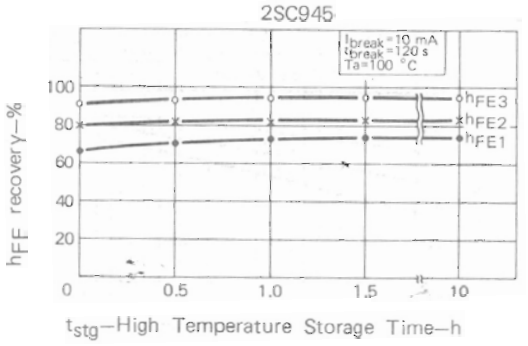


Fig. 3-1 I_{break} = 1.0 mA



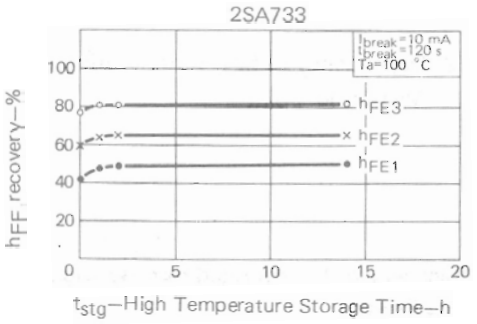
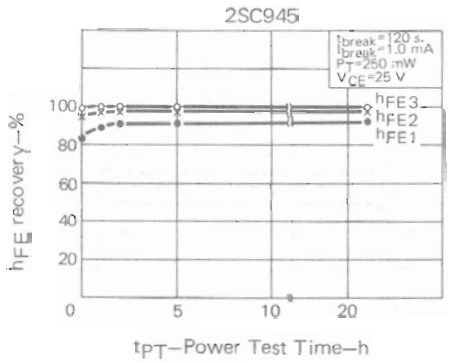


Fig. 3-2 I_{break} = 10 mA

Fig. 3 Recovery of Deteriorated h_{FE} by *Means of* High Temperature Storage

1-4. Recovery of Deteriorated h_{FE} By Power Aging

Fig. 4 shows the rate of recovery of h_{FE} values of a deteriorated transistors by means of power aging. These curves also show what percentage of the initial values (before breakdown) as in Section 1-3.



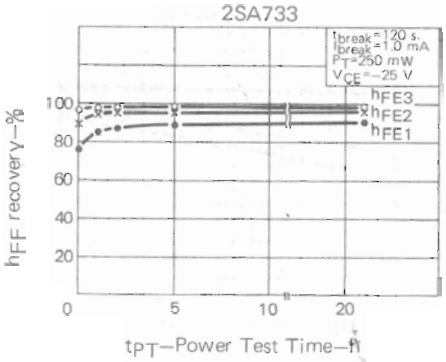
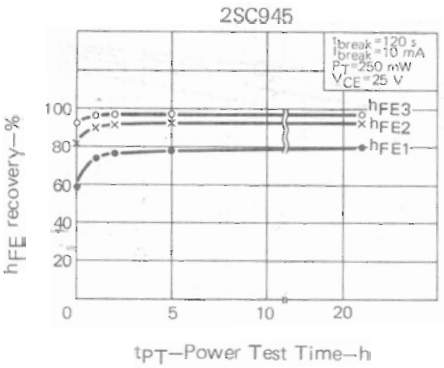


Fig. 4-1 I_{break} = 1.0 mA



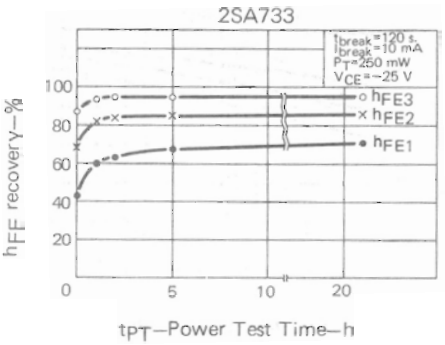


Fig. 4-2 I_{break} = 10 mA

Fig. 4 Recovery of Deteriorated h_{FE} by Means of Power Test Aging

The above described measurements lead to the following conclusions.

1) h_{FE} is deteriorated the most significantly at the instant of the breakdown, but after that, it does not degrade by the prolonged breakdown.
2) h_{FE} deterioration is more dependent on breakdown current than on breakdown time.

3) h_{FE} is significantly deteriorated in smaller current region.

4) Since the deteriorated h_{FE} can be recovered by means of high temperature storage and power aging[3], the deterioration is not permanent. However the recovery to the initial values is hardly seen.

5) To recover h_{FE}, the power aging is more effective than the high temperature storage.

Note 3) Beside the above, the flow of large $I_{F(BE)}$ can recover deteriorated h_{FE} in a short time. But since this method might induce E-B shortening, it is not a good method.

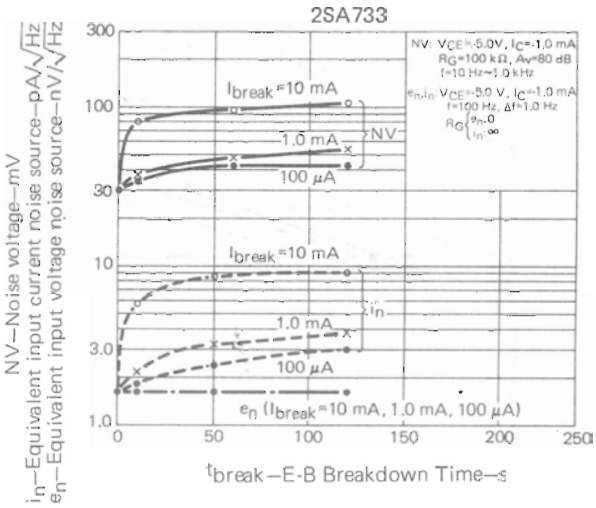
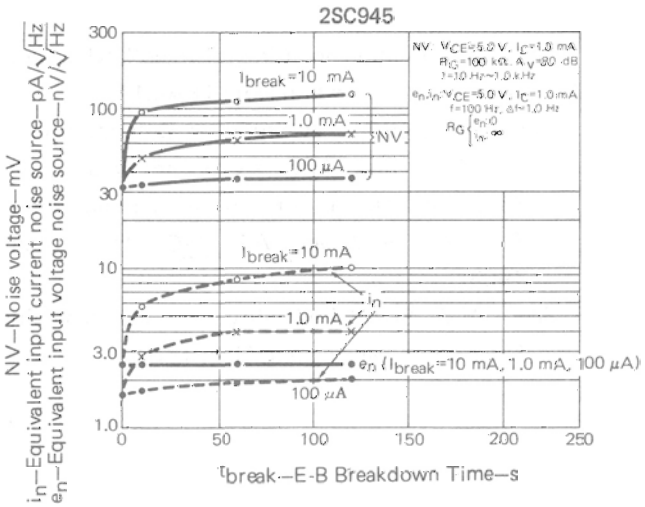


Fig. 5-1 Deterioration of NV, i_n and e_n vs. E-B Breakdown Time

2. NOISE FIGURE DETERIORATION CAUSED BY E-B BREAKDOWN

The h_{FE} deterioration due to E-B breakdown has a secondary effect of noise figure deterioration. This effect is shown in Fig. 5.



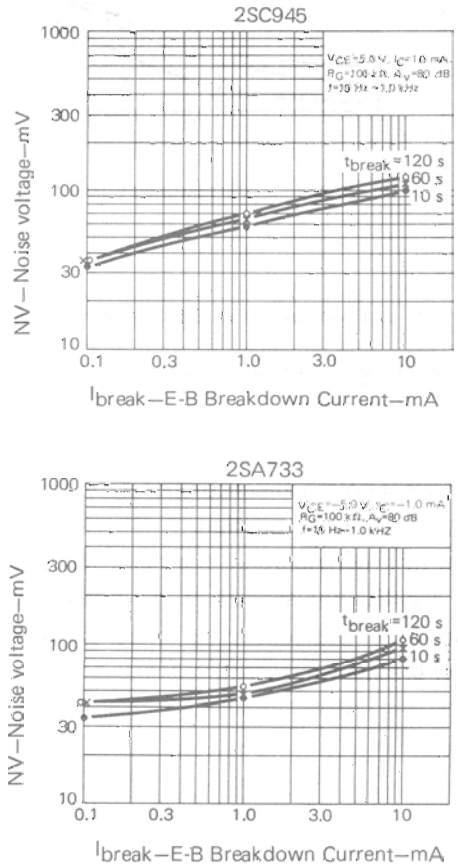
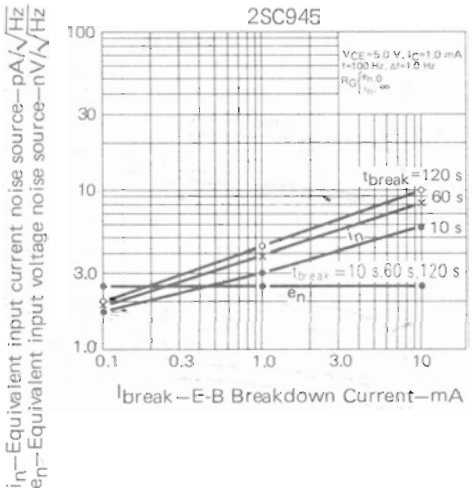


Fig. 5-2 NV Deterioration vs. E-B Breakdown Current



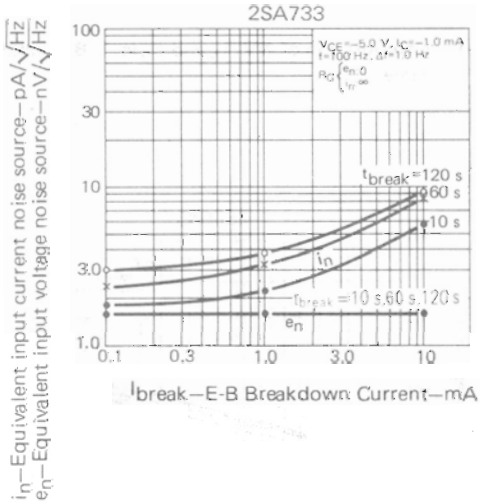


Fig. 5-3 i_n Deterioration vs. E-B Breakdown Current

Fig. 5 Noise Figure Deterioration Due to E-B Breakdown

The following conclusions can be drawn from Fig. 5.

1) i_n (current noise source) component the contributes to noise figure deterioration.
2) As in h_{FE} deterioration, the noise figure degradation significantly appears at the instant of breakdown. The degradation is more significant for higher breakdown current.

3. CAUTIONS AGAINST CHARACTERISTIC DETERIORATION DUE TO E–B BREAKDOWN

breakdown causes deterioration dependent on the breakdown current, and once deteriorated the characteristics can never be recovered to their initial values. Therefore, it is essential to design circuits in such a manner that breakdown cannot take place. Particularly, when transistors are used under the following conditions, it is necessary of the most careful consideration be given.

1) Circuits operating a transistor in its low current region.
2) Circuits containing a transistor with large h_{FE} value.
3) Circuits that use a low-noise transistor or circuit where low noise is required, and a particular circuit with high source resistance (because this component contributes to noise figure).

h_{FE} deterioration and shorting can be caused not only by inadequate circuit designs but also by reversed terminal connection and application of voltage or current beyond the ratings of acceptance inspections of purchased transistors.

References (Japanese version)

"h_{FE} Deterioration and Circuit Design", NEC Semiconductor Application Note TEA-511.

Nakao, Irie, etal : "A Study on Deterioration of Transistor h_{FE} After Avalanche Breakdown", Papers of Institute of Electronic Communication Engineers of Japan, Vol. 52-C, No. 6, (Jun. 1969)

Sess. IV-7, Sixth Reliability and Maintenability Symposium, Nikkagiren, (Jun. 1976)

TRANSISTORS WITH EXCELLENT IN "ELECTROSTATIC-DISCHARGE-RESISTANT(ESDR)"

1. THE NECESSITY FOR TRANSISTORS WITH EXCELLENT IN "ELECTROSTATIC-DISCHARGE-RESISTANT."

When designing circuits, an ample consideration is given on the SOA, thermal problems and the scatterings in various characteristics of transistors. However, it appears that a consideration on electrostatic-discharge (ESD) is frequently neglected. Furthermore, it has been ascertained that, not only due to circuit design, ESD will occur even during the manufacturing process of equipment depending on the storage conditions of the transistors.

Recently, among the total failures of transistors, though differing according to the application field and period (due to the effect of humidity), the percentage of failures presumed to be due to ESD reach a considerable number. When the reliability and market failure rate of transistors are discussed, failures due to ESD cannot be disregarded.

Then, **"What kind of transistors are excellent in ESDR?"** Since the relationship between the structural parameters of transistors and ESD is so complicated that only a simple explanation of these parameters shall be given here, and the explanation shall be mainly about a simple estimation on ESD through electrical parameters given in catalogs, etc. Furthermore, the explanation shall be focussed on: **"Failure when the E-B is reverse-biased, that is the main failure mode of a transistor in ESD."**

2. WHAT IS ESD ORIENTED FAILURE?

The ESD oriented failure is a phenomenon that a PN junction is destroyed or partially deteriorated when a capacitor note 1) having a charge Q is discharged into a transistor causing the junction temperature to rise due to the impulse current and then the temperature rise reaches the melting point of silicon. The maximum value and decay time of the impulse current will vary depending on the CR time constant of the test circuit, bulk resistance, stray capacity, etc., but the destruction energy has a constant value $1/2CV^2$ (J).

Therefore, it can be said that the larger the value of $1/2CV^2$ of a transistor, the superior the ESDR of a transistor.

When transistors are subjected to ESD, in slight cases the result may only be an increased I_{EBO}, decrease of h_{FE} or deterioration of V_{EBO}, but in extreme cases, not only will E-B be short-circuits, but it may even result in a deterioration of C-E and an increase in I_{CEO} and I_{CBO}. An examination of the deterioration or destruction mode shows that it happens in a particular direction approximately perpendicular to the E-B junction plane. Also, it has been ascertained that in most cases approximately the same spot of the PN junction is destroyed depending on the type a transistor, and according to the pattern of the transistor there are spots where current is liable to be concentrated. Transistors that have destroyed at levels near the destruction energy are frequently overlooked during visual inspection of the pellet (dice). But, by removing the aluminum metallization and oxide film, the destruction spot can be discovered. (See photos 1 to 3).

Note 1) When broadly interpreted, not only the charges of capacitors, but the electro static resulting from contact friction between two different materials should be included.
Actually, ESD's due to work benches, belt conveyors, and transistor-storage-trays during assembly of equipment have been reported.

3. TEST METHODS AND RESULTS OF "ESDR."

Roughly divided, there are two test methods as follows.

1) Discharging the charge of a capacitor into the transistor under test.
2) Applying a single pulse from a pulse generator to the transistor under test.

Here, thinking about the actual destruction mode and the correlation in question, the method 1) is applied and the data are utilized.

3-1 Testing by direct supply of charge note 2).

1) Capacitor C is charge up to a desired voltage V_D as shown in Fig. 1.

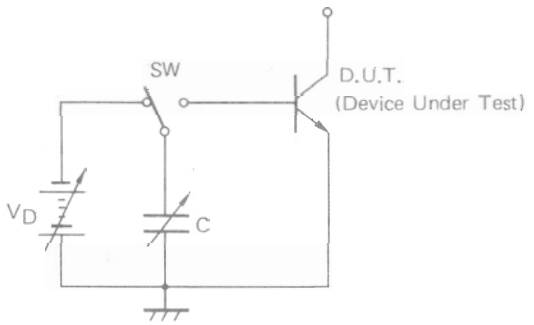


Fig. 1

2) The stored charge is applied by turning SW to the transistor side, and then the BV_{EBO} waveform of the transistor is checked.
3) If no deterioration of the waveform can be discerned, the capacitor is charged to a higher voltage and the test is repeated until deterioration of the waveform is discerned.
4) Next, the capacitor C is changed to any different capacity and the test is repeated.

3-2 Testing with base series resistor.

Since in actual high frequency circuits a resistor of several tens of ohms is often added in series with the base, as shown in Fig. 2., this is a method for measuring the ESDR in this state. The testing method is the same as 3-1., and the test is repeated with different values of R_B.

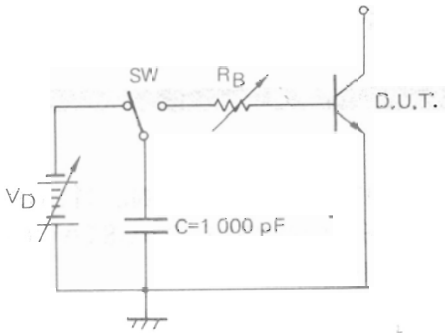


Fig. 2

3-3 Testing with emitter load.

This is a method for measuring the ESDR with an emitter resistor and bypass capacitor as shown in Fig. 3.

The testing method is the same as 3-1., and the test is repeated while changing C_E.

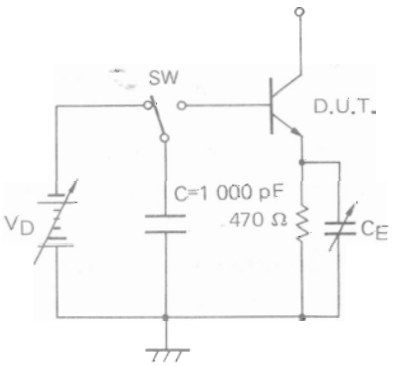


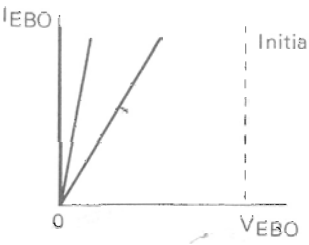
Fig. 3

Note 2) The testing methods described here are methods employed particularly by the company for the evaluation of ESDR, and are not standardized. These three testing methods are aimed for examining the ESDR of the transistor itself; the deviation when the base series resistor is added; and the effect of different capacities of the emitter bypass capacitor respectively.

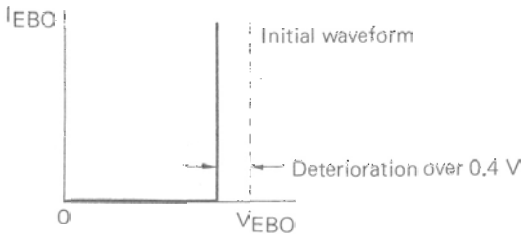
3-4 Criteria of "ESDR" note 3).

"ESD" is judged to have taken place, when the E-B breakdown waveform becomes as shown in Fig. 4, compared to the initial. The voltage V_D applied to the capacitor C at that time is called the "Electrostatic-Discharge-Resistant (ESDR)".

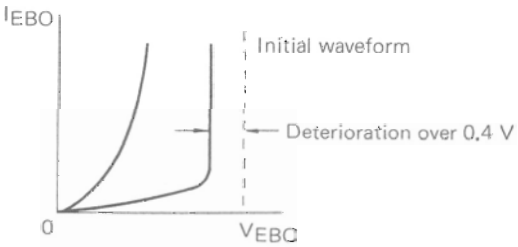
a) Complete short, ohmic short.



b) Hard deterioration



c) Soft deterioration



d) Soft deterioration

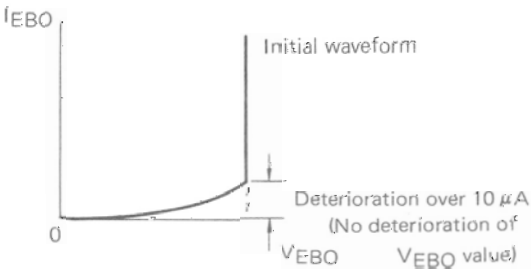


Fig. 4 Waveforms of ESDR criteria.

Note 3) Similarly to note 2), these criteria are of independent use by the company.

3-5 Test results of ESDR.

The data of tests performed by the methods of 3-1. to 3-3. are as shown in Fig. 5 to 7.

The ESDR on various types of transistors by the method 3-1. are shown in Fig. 8.

Fig. 5 shows that the destruction energy ($1/2CV^2$) is constant. Therefore, by measuring the ESDR at a certain capacity, the ESDR at any capacity may be easily determined.

Fig. 6 shows that the effect of the protective resistor appears the more marked the stronger the ESDR of the transistor itself. The same results as Fig. 6 are obtained, when the protective resistors are connected to the emitter side.

From Fig. 7 it can be seen that, even bypass capacitors, from the standpoint of ESDR, an indiscriminately large capacity should not be used. Though the rate of change is the same, the absolute value of the ESDR will differ so that the more care must be taken the weaker the ESDR of the transistor.

The surfaces of destructed 2SC945 are shown in photos 1 to 3.

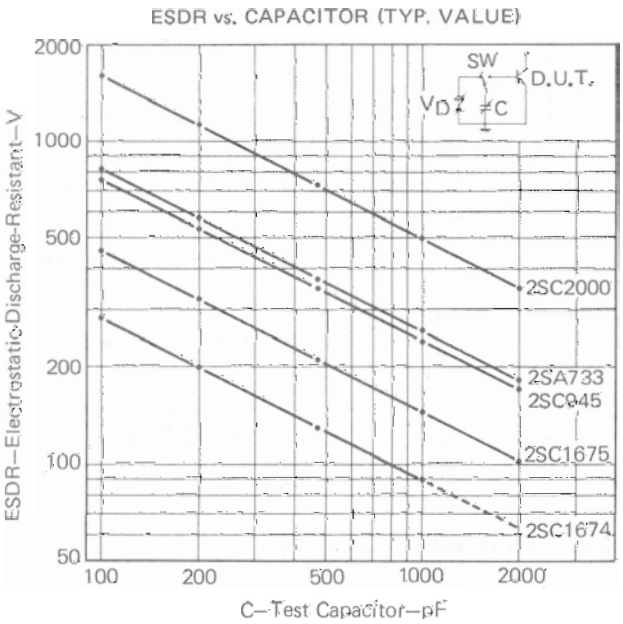


Fig. 5 ESDR by direct supply of charge

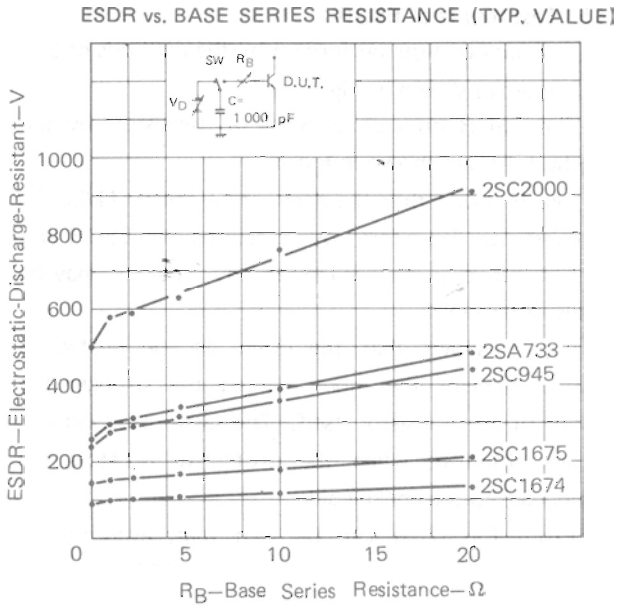


Fig. 6 ESDR with base series resistance added

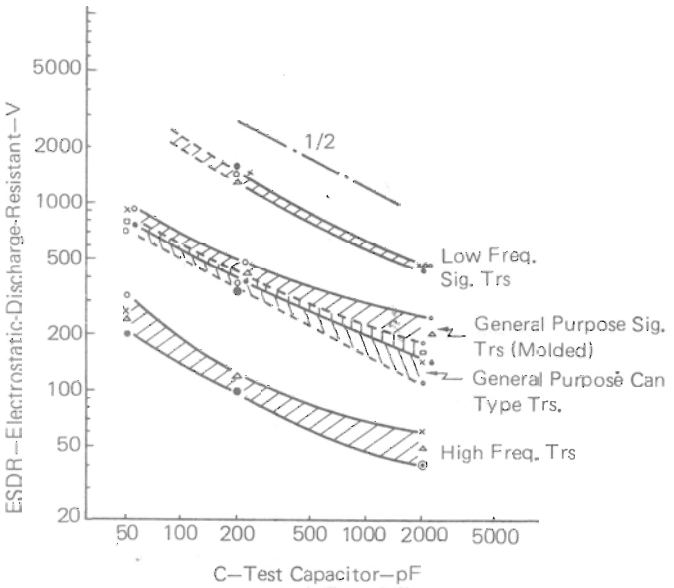


Fig. 8 ESDR of various types of transistors

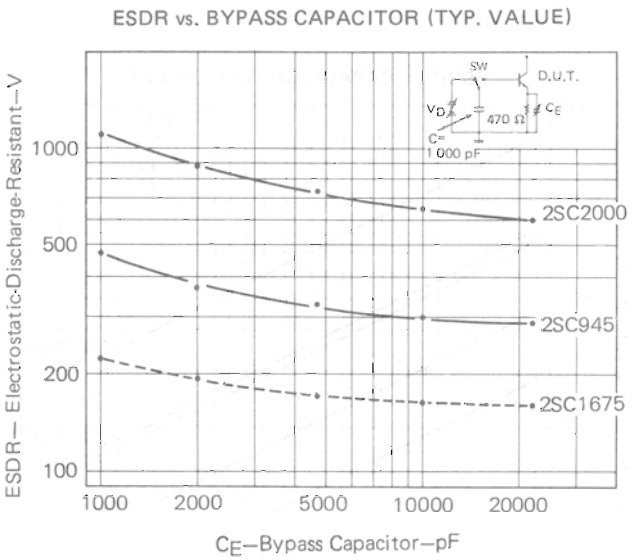


Fig. 7 ESDR with emitter load

Destruction mode of a 2SC945 (Portion marked is destruction spot)

V_D=220 V, C=1 000 pF

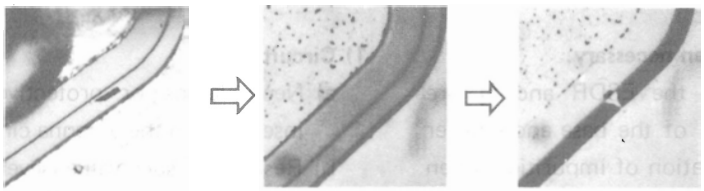


Photo 1-1 Sealing opened | Photo 1-2 Aluminum metallization removed | Photo 1-3 Oxide layer etchid off

V_D=260 V, C=1 000 pF

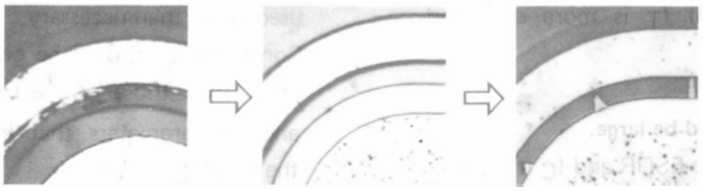


Photo 2-1 Sealing opened | Photo 2-2 Aluminum metallization removed | Photo 2-3 Oxide layer etchid off

V_D=370 V, C=470 pF

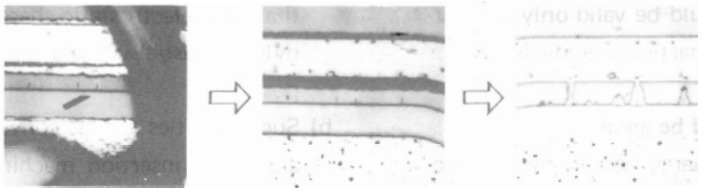


Photo 3-1 Sealing opened | Photo 3-2 Aluminum metallization removed | Photo 3-3 Oxide layer etchid off

4. WHAT KIND OF TRANSISTOR IS SUPERIOR IN "ESDR."?

As can be seen from the test results of 3-5., among small signal molded transistors, the ESDR of the 5 types of transistors used in the experiments are in the order of:

2SC2000>2SA733>2SC945>2SC1675>2SC1674

From the above, a study is done about the major parameters of these transistors, as listed in Table 1. below, in order to determine which parameters should be noted when selecting a transistor excelling in ESDR.

TYPE NO.	ESDR (V) @C=1 000 pF TYP.	P_T (mW)	I_C (mA)	V_{EBO}(V) @I_C=100 μA Effective value.	h_{FE} ratio @V_{CE}=6.0 V I_C=0.1 mA/1.0 mA TYP.	f_T (MHz) @V_{CE}=6.0 V I_C=1.0 mA TYP.	APPLICATION FIELD
2SC2000	500	600	200	7.5	0.93	70	General purpose. (Specially designed for high ESDR.)
2SA733	260	250	−100	−9.5	0.93	70	General purpose.
2SC945	240	250	100	8.4	0.93	100	General purpose.
2SC1675	145	250	30	6.8	0.83	250	FM/IF, AM/Con.
2SC1674	90	250	20	5.9	0.83	600	FM/RF

Table 1. Principal parameters of various transistors.

From the above Table it can be seen that for transistors to excell in ESDR.

1) f_T should not be higher than necessary.

This is because both the ESDR and f_T are proportional th the depth of the base and emitter junction and the concentration of impurities, when diffusing the base and emitter reagions.

The value of V_{EBO} is also an approximate indication but, it is effected by other parameters so that judging the value of f_T is more easy and accurate.

2) The value of I_C max. should be large.

This is because both the ESDR and I_C max. have a proportional relationship with the area or length of periphery of the emitter. However, since this condition is also proportional to the size of the pellet, the comparison would be valid only comparing transistors for use of a particular application.

3) The linearity of h_{FE} should be good.

When electrostatic discharge occurs, the destruction spots will be concentrated in places where there are crystal defects (lattice defects) in the emitter-base region. Since the linearity of h_{FE} is made worse when there are crystal defects, it is an indication for judging ESDR.

5. COUNTERMEASURES AGAINST ESD.

As has been described, ESDR will differ greatly according to the type of transistor and the conditions of use. Furthermore, since electrostatic discharges occur everyday in all places, it is necessary to pay attention to this fact when designing circuits or during the manufacture of equipment.

Therefore, it is important to keep in mind what degree of ESDR will be necessary.

Basic countermeasures against ESD are described following:

1) Circuit design.

a) Neon lamps or protective diodes should be inserted into the antenna circuits.

b) Resistor of such value (several tens of ohms) that will not effect the S/N or NF should be inserted in series with the transistor base.

c) The value of the bypass capacitor should not be used larger than necessary.

d) Consideration should be given to characteristics other than those of the bias point being used, and to parameters that have correlation with the ESDR.

2) Manufacturing processes.

a) For storing transistors, containers of materials that keep electrostatic charges strongly (celluloid, nylon, plastic) should be avoided as much as possible.

b) Such facilities as belt conveyors, soldering baths, automatic insertion machines should be grounded.

c) The keeping of electrostatic charges by workers should be prevented.

d) Humidity should be thoroughly controlled, and a low humidity condition should be avoided.

REFERENCES:

1) NEC Integrated Circuits Application Note: IEP–001

2) Fujie, et al. "Electrostatic Interference Countermeasure Data Anthology." Published by Daiichi International Co.

3) D.C. Wunsch and R.R. Bell, "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to pulse Voltage." IEEE Trans. Nucl. Sci., NS-15, 1968.

CAUTIONS TO BE TAKEN IN MEASUREMENT AND TESTING OF TRANSISTOR

In the case of measurement or testing of a transistor, it can happen that the transistor is destroyed or deteriorated inadvertently due to troubles in such measurement or testing. With regard to such troubles, this material enumerates points of caution taken at our company especially in respect of high-frequency transistors. It is our desire that this manual be utilized effectively on the occasion of acceptance inspection or reliability test.

1. CAUTIONS REQUIRED IN MEASUREMENT OF CHARACTERISTICS

1-1 Prevention of Oscillation

In case where a transistor does not indicate a true value due to oscillation in the measurement of h_{FE} or withstand voltage, etc., for the purpose of preventing oscillation insert resistance of approx. 5 Ω in series with the emitter terminal of the measuring jig (transistor socket) at a point nearest to the emitter lead wire of a specimen as in Fig. 1.

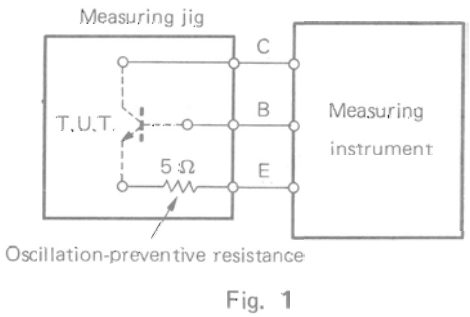


Fig. 1

1-2 Surge Protection

When measuring a transistor with an automatic measuring instrument or the like, there are cases where improper contact is caused between a lead wire of the specimen and the measuring jig (transistor socket) and high voltage is produced thereby and such high voltage destroys the transistor. As a preventive measure in such a case, put Zener diodes commensurate with withstand voltage of the transistor in between the respective terminals as in Fig. 2. However, at time of measurement of h_{FE}, $V_{CE(sat)}$ and $V_{BE(sat)}$, remove the Zener diode between base and emitter. Such surge protection by means of Zener diodes also serves for surge protection in a practical circuit.

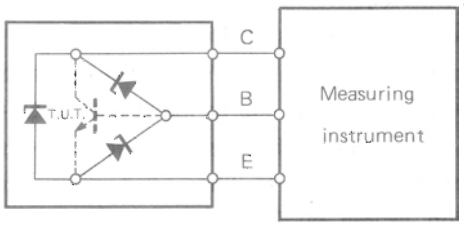


Fig. 2

In the meantime, at our company, for detection of such improper contact, low-level h_{FE} (such as V_{CE} = 3 V, I_C = 1 mA) is measured beforehand and after confirming that the value is indicated, measurement is made.

2. CAUTIONS REQUIRED IN LIFE TEST

2-1 Cuations Required in Performance Test

Use a test circuit provided with oscillation inhibition and surge protection as in Fig. 3.

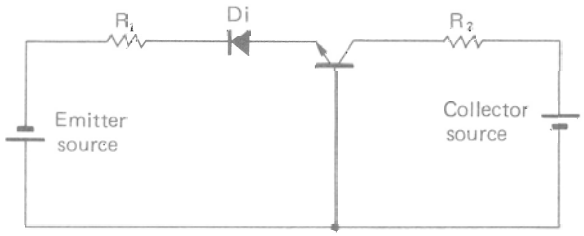


Fig. 3

R_1 : Resistor to suppress dispersion of current among specemens
(Resistance to cause voltage drop of approx. 10 V at both ends of resistor)

R_2 : Resistor to prevent overcurrent due to surge voltage

(Resistance to cause voltage drop of approx. 10 V at both ends of resistor)

Di : Oscillation-preventive diode (Place in the vicinity of the emitter lead wire of a specimen. As for this diode, we recommend our F14A – F14D)

On the other hand, in the case of a continuous performance test, synchronize power-on on the collector side with the emitter side (to prevent oscillation).

2-2 Cautions Required in Reverse Bias Test

Use the test circuit as in Fig. 4. Shorting B – E is intended for prevention of impression of reverse bias between emitter and base due to the effects of C – E capacity and E – B capacity. For the effect of reverse bias on transistor refer to "h_{FE} and noise figure deterioration caused by E-B junction breakdown in transistors" in NEC Transistor Engineering Bulletin (TEB–3011).

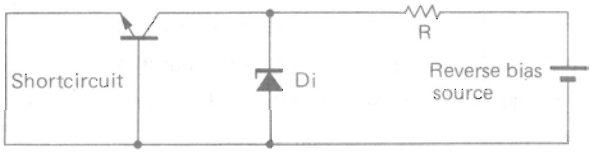


Fig. 4

R : Resistance of approx. 10 kΩ

Di : Zener diode for surge voltage absorption (with voltage rating higher than impressec voltage)

3. TEST PROCEDURES

It is recommended that when conducting various tests, C–B and E–B waveforms be checked with a curve tracer before and after each process as in Fig. 5.

This serves, in case a specimen has become defective halfway in testing, to make clear in which process has it become defective and, by doing this, whether the speciman has been made defective inadvertently due to abnormal oscillation, etc. at time of measurement of characteristics or whether the speciment has become defective due to the test itself is also made clear.

On the other hand, in the case of waveform check, current should be less than 100 μA.

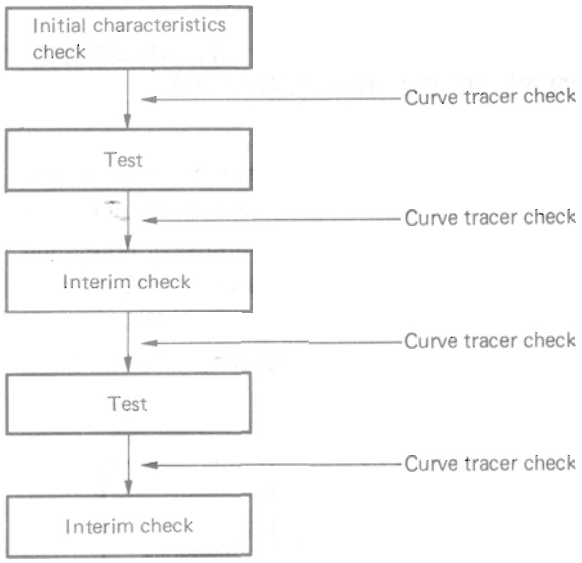


Fig. 5

OPTIMUM METHOD OF USE OF LOW FREQUENCY-LOW NOISE TRANSISTORS

There are products having characteristics suited to circuit functions available for low frequency-low noise transistors and field effect transistors (hereinafter, referred to as FET) used on audio units.

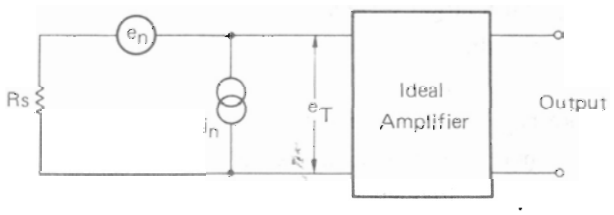
Here, noise of transistors and FET at low frequency is described and a method of selection of products corresponding to circuit functions is introduced.

1. NOISE

1-1 Equivalent input noise source method

To determine noise at low frequency it is advisable to utilize this equivalent input noise source method.

This method is to express noise electrically by dividing noise into two components of voltage noise source e_n and current noise source i_n, inputing and converting them into electrical values. When noise of a transistor is expressed electrically using this method, it can be considered equivalently as shown in the following diagram:



From this, overall input-converted noise voltage e_T can be expressed as follows:

$$e_T^2 \doteqdot e_{RS}^2 + e_n^2 + i_n^2 \cdot Rs^2 \quad \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

where, e_{RS}^2 is thermal noise of signal source resistance Rs expressed by 4 KTRs.

Noise figure NF much used in catalogs is expressed by the following equation on the basis of Equation (1), above:

$$NF = \frac{e_T^2}{e_{RS}^2} = 10 \log_{10} \left[1 + \frac{1}{4KT}\left(\frac{e_n^2}{Rs} + i_n^2 \cdot Rs\right)\right]$$

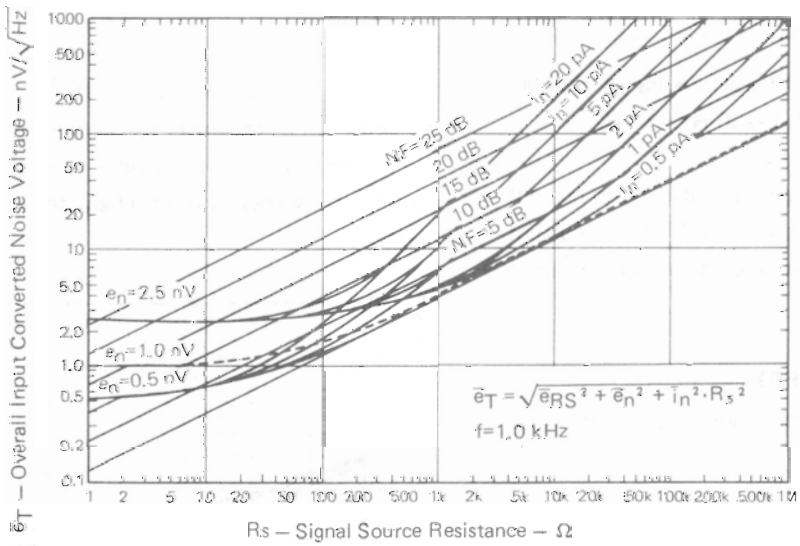


Fig. 1 Overall Input Converted Noise Voltage $\bar{e}_T$ - Signal Source Resistance Rs Characteristic

Where, K is Boltzman's constant (1.38054×10^{-23}) and T is absolute temperature (273.15 + Ta K).

According to e_n and i_n, e_T will have a relation with Rs as shown in Fig. 1.

1-2 Noise characteristic of transistor

e_n and i_n of a transistor at emitter grounding are expressed as follows and their current characteristics are as shown in Fig. 2.

$$e_n^2 = 4\,KT(r_{bb'} + 1/2\,gm)\cdot\Delta f$$
$$i_n^2 = 2\,qIb\cdot f$$

where, $r_{bb'}$: base resistance
gm : mutual conductance
Δf : frequency band
q : electron charge

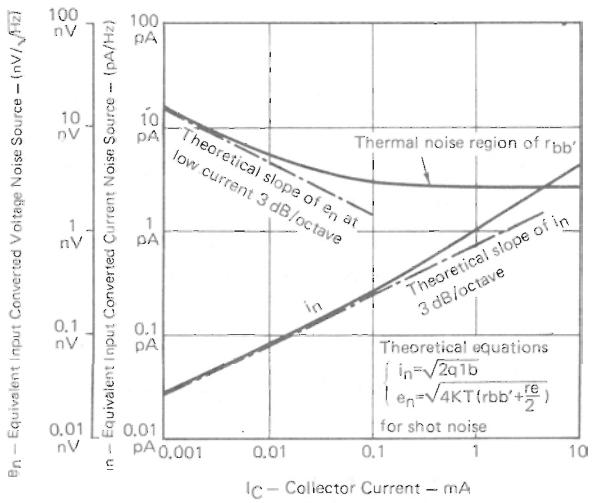


Fig. 2 e_n and i_n Current Characteristics of Bipolar Transistor (V_{CE}=3V, f=100 Hz, f=1 Hz)

Of transistor noise, i_n largely depends upon current and e_n depends upon 1/2 gm (= re/2) at low current while it is decided by base resistance $r_{bb'}$ at large current.

1-3 Noise characteristic of FET

e_n and i_n of FET at source grounding are expressed as follows:

$$e_n^2 = 4KT\cdot 1/gm\cdot\Delta f$$
$$i_n^2 = 2qI_G\cdot\Delta f$$

where, I_G is gate leak current.

Gate leak current at this time is leak current at normal bias as shown in Fig. 3 and shows voltage characteristic shown in Fig. 4.

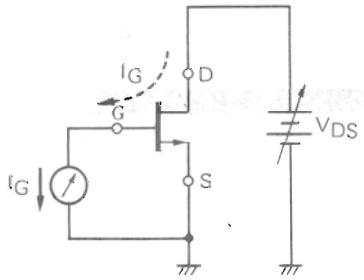


Fig. 3 Gate Leak Current Measuring Circuit

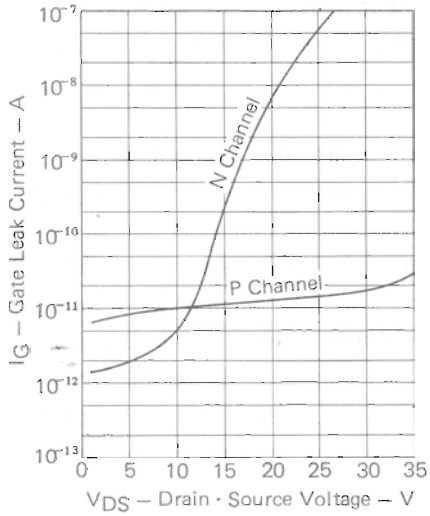


Fig. 4 Voltage Characteristic of Gate Leak Current I_G

Therefore, i_n is almost negligible at low voltage (generally, 10 V or less) as I_G is 10^{-10} – 10^{-13} A, and the larger gm is, the lower e_n becomes.

Further, as gm will become large with increase in current, e_n shows current characteristic as shown in Fig. 5.

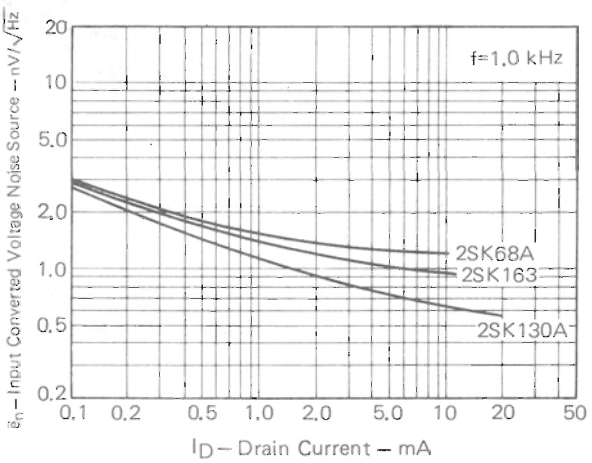


Fig. 5 Current Characteristic of FET Input Converted Voltage Noise Source e_n

However, i_n cannot be disregarded at high voltage as N channel type I_G increases rapidly.

1-4 Frequency characteristic of noise

Frequency characteristic of noise generally shows characteristic as shown in Fig. 6.

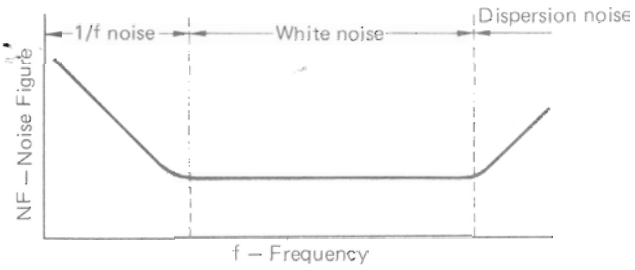


Fig. 6 General Frequency Characteristic of Noise

As noise changes in inverse proportion to frequency, noise in low frequency band is generally called 1/f noise.

The medium frequency band is a thermal noise region that has no frequency dependency and noise in this band is called white noise.

Noise in high frequency band is that generates in relation to transistor cut-off frequency and FET gate cut-off frequency.

At present, the primary problem for transistor is 1/f noise from the viewpoint of its principle of operation, while on junction FET 1/f noise is generally satisfactory but white noise is a problem.

2. EFFECTIVE WAY OF LOOKING AT CATALOGS

Any catalogs for low frequency-low noise transistors and low frequency-low noise FET list as a matter of course specifications and data for noise. Before using transistors or FET, it is advisable to effectively utilize these data and specifications in selecting optimum products.

2-1 NF Map

This NF Map (Fig. 7 & Fig. 8) is the most effective data relative to noise of transistors. This NF Map shows the relation between signal soruce resistance and collector current with NF used as a parameter. It may said that NF Map covers all items governing noise of transistors, for instance, "To obtain optional NF on a transistor, at what degree should we design signal source resistance and collector current?" or "To obtain optional NF at optional signal source resistance, where should we set collector current?".

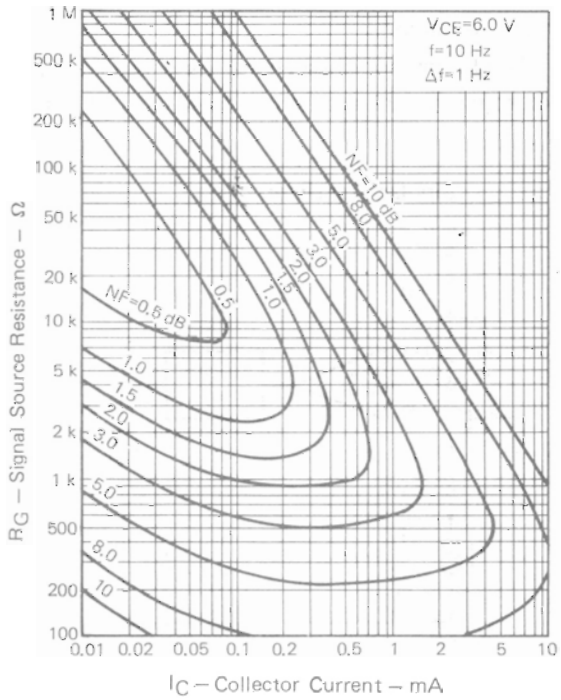


Fig. 7 NF Map

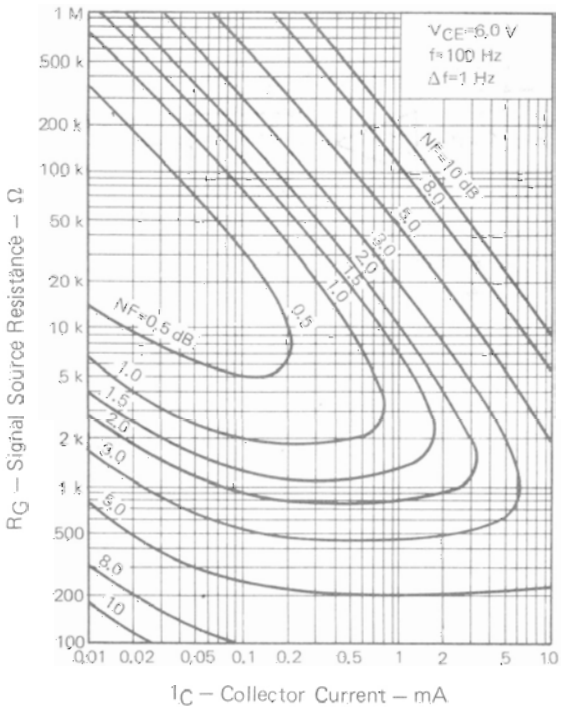


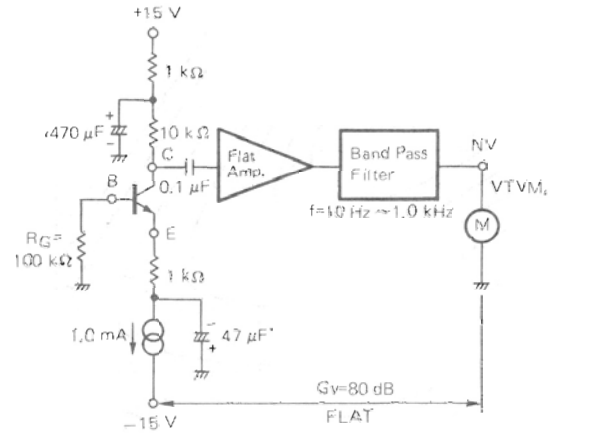
Fig. 8 NF Map

2-2 Noise voltage (NV) regulation

This regulation has been developed on the basis of actual state of use of transistors and FET. Manufacturers sort and control noises according to items listed in this regulation.

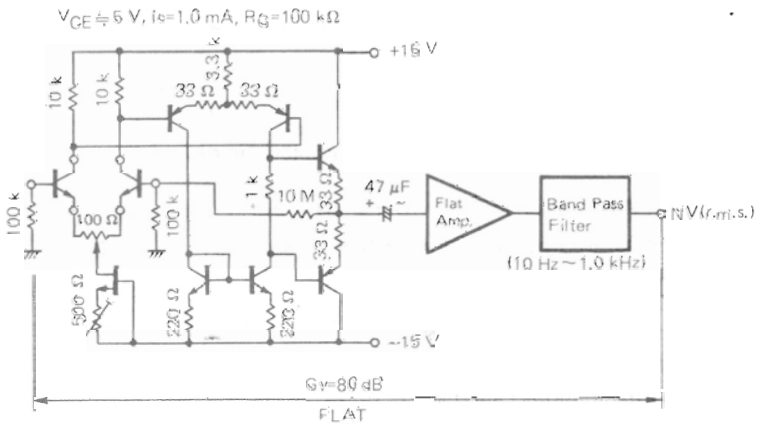
Conditions for these items have been established according to characteristics, uses, etc. of respective transistors and FET. In the case of transistor, signal source resistance is set at high level (R_G=100 kΩ) so that i_n component can be detected remarkably. In the case of FET, in contrast with this, signal source resistance is set at low level (0 – 1 kΩ) so as to make it easy to detect e_n component.

○ Bipolar Transistor

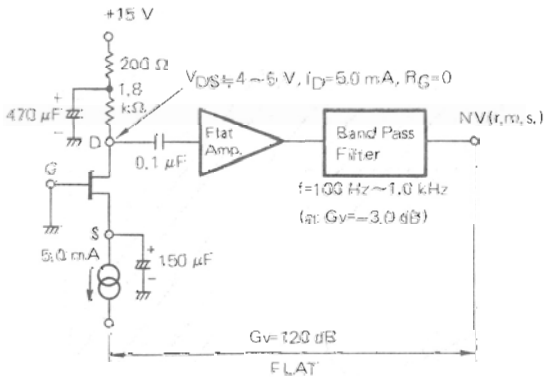


V_{CE} ≒ 5 V, I_C=1.0 mA, R_G=100 kΩ, Gv=80 dB, FLAT (f=10 Hz ~ 1.0 kHz)

○ Twin Transistor



○ FET



○ Twin FET

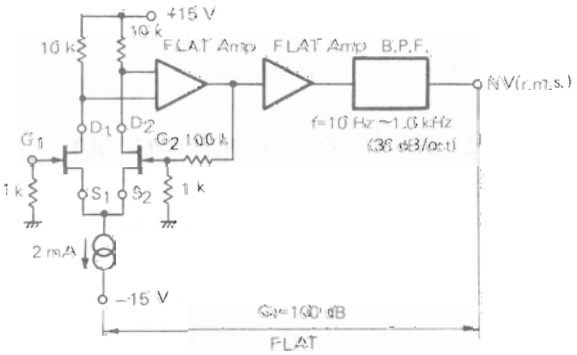


Fig. 9 Example of Noise Voltage Measuring Circuit

2-3 Other Data

In addition to above data, some catalogs may list current characteristics of e_n and i_n depending upon products. If these data are available, noise characteristic of a particular transistor can be grasped more effectively.

3. SELECTION OF TRANSISTOR SUITED TO CIRCUIT FUNCTION

Here, let's consider what transistor and FET should be selected for circuit function.

3-1 MC head amplifier

As impedance of MC cartridge is as low as several — several ten ohm, it is presumed that there will be no problem of effect of i_n on so-called low noise transistors, and transistors having lower e_n shall be used.

Standard e_n values are listed on catalogs for so-called low base resistance (low $r_{bb'}$) products. It is advisable to use these values as refereces.

Further, in the case of FET it is advisable to select products having large gm ($|Yfs|$) which are called Super High Gm or Super Low Noise FET.

3-2 Reproducing head amplifier

As impedance of reproducing head is as high as several hundred ohm — ten-oddkohm i_n cannot be ignored. However, e_n also cannot be neglected. As low noise transistors currently available in the market have been manufactured with $e_n \leqq 3.0\ nV/\sqrt{Hz}$ (at f = 1 kHz), ordinary low noise transistors can be used without any trouble but low base resistance-low noise transistors may be used.

In the case of FET, Super High gm FET is considered best when gain is considered.

3-3 EQ amplifier and main amplifier

In selecting EQ amplifier and main amplifier, frequency characteristic as well as noise must be carefully checked. As mentioned above, in the case of transistor, e_n is less than $3.0\ nV/\sqrt{Hz}$ and therefore, products of low capacity (low Cob) using low noise transistor with well suppressed i_n (good NV standard) are advisable.

3-4 High impedance amplification

On buffer amplifiers using such high impedance elements in excess of several M ohm as electrostatic induction element, it is difficult to use transistor from a viewpoint of input impedance and i_n, and FET is best after al .

However, when impedance is at this high level, i_n must be taken into consideration. So, it is advisable to add gate leak current I_G to the review items for selecting products of low gate leak current.

Further, it is also necessary to pay attention not to allow high supply voltage. In the event that high supply voltage is required, P-channel FET may be used.

Fig. 10 NEC Bipolar Low Frequency-Low Noise Transistor Family

Package	Characteristic / Product Name	Absolute Max. Rating			Electric Characteristic					Main Recommended Uses
		V_{CEO} (V)	I_C (mA)	P_T (mW)	(note 1) h_{FE} classification V_{CE}=6.0 V, I_C=1.0 mA)	Cob (pF) TYP.	e_n ($nV\sqrt{Hz}$) TYP.	i_n ($pA\sqrt{Hz}$) TYP.	NV (mV) MAX.	
TO-92 (Iron Lead)	2SC1842	35	100	250	U, E, F, P	3.0	2.5	0.9	50	Preamplifier for radio, tape recorder
	2SA990	−50	100	250	E, F, P	4.5	2.3	0.7	40	Popular type stereo music center
	2SC1843	50	−100	250	E, F, P	3.0	2.5	0.7	40	
TO-92 (Copper Lead)	2SA991	−60	100	500	E, F, P	5.5	0.65	0.8	45	MC head amplifier Reproducing head amplifier Other low impedance amplification
	2SC1844	60	100	500	E, F, P	4.8	0.7	0.8	45	
	2SA992	−120	−50	500	E, F, P	2.0	2.0	0.7	40	EQ amplifier Initial stage of main amplifier Other Hi-Fi stereo low noise amplification
	2SC1845	120	50	500	U, E, F, P	1.6	2.6	0.7	40	
9 pin V-DIP	μPA74V	80	50	300/ unit	E, F, P	3.0	2.6	0.9	80	Low noise differential amplification Active load
	μPA75V	−80	−50	300/ unit	E, F, P	3.5	2.0	0.9	80	

Note 1: h_{FE} standards P: 200 – 400, F: 300 – 600, E: 400 – 800, u: 600 – 1200

Fig. 11 NEC Low Frequency-Low Noise FET Family

Characteristic / Product Name	Absolute Max. Rating			Electric Characteristic				Features and Main Uses
	V_{DSX} (V)	I_D (mA)	P_T (mW)	(note 1) I_{DSS} classification	$\lvert Y_{fs} \rvert$ (mS) TYP.	Ciss (pF) TYP.	e_n ($nV\sqrt{Hz}$) TYP.	NV (mV) MAX.	
2SJ44	−40	−30	400	K, L, M, N	25	50	1.2	20	Complementary use is possible. Various kind low noise amplifications. High impedance amplification.
2SK163	50	30	400	K, L, M, N	25	13	1.0	20	
2SK162	40	30	400	K, L, M, N	75	55	0.65	35	Super High gm with low noise. MC head amplifier, reproducing head amplifier.
2SK194	40	50	400/ unit	K, L, M	75	55	0.65	35	A pair of 2SK162. Eq and main amplifier initial stage.
μPA68H	50	50	250/ unit	K, L, M, N	18	15	1.3	35	1 chip point symmetrical construction with excellent pair performance. Optimum product for use at initial stage of main amplifier.

Note 1: I_{DSS} standards

2SJ44, 2SK163, μPA68H (V_{DS}=10 V, V_{GS}=0)

K: 1.0 ~ 6.0 mA, L: 5.0~10 mA, M: 9.0~14 mA, N: 13~18 mA

2SK162, 2SK194 (V_{DS}=5.0 V , V_{GS}=0)

K: 5.0~12 mA, L: 11~18 mA, M: 17~24 mA, N: 23~30 mA

NEC'S ELECTRONIC TUNING VARACTOR DIODES

Radio receiver sets equipped with PLL frequency synthesizer are frequently seen today for car-radios, car-stereos, home-use stereos, radios with audio cassette, and TV receivers. Varactor diodes are the essential elements for these sets. In the early stage of their development, the diodes suffered from large variances in capacitance variation and Q value, low Q values, and high cost, thus limiting their use for consumer appliances. Recently, a rapid advancement in semiconductor technology has enabled varactor diodes to have much improved characteristics and has freed them from the above mentioned demerits. This document describes features, principle of operation, and precautions for use of varactor diodes.

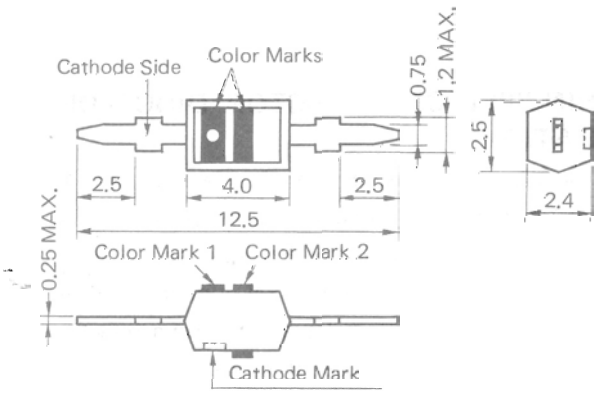
1. FEATURES OF VARACTOR DIODES

A varactor diode is characterized by the junction capacitance of a reverse-biased PN junction. This junction capacitance is inversely proportional to the exponential of the reverse bias voltage.

The use of varactor diode for electronic tuning has the following advantages.

(1) No mechanically operated tuning element such as a variable capacitor is needed.
(2) Miniaturization or light weight of sets is allowed.
(3) Automatic or preset station selection is allowed.
(4) Novel station selection techniques such as preset memory scan can be applied.
(5) Remote control can be applied.

NEC's electronic tuning varactor diodes includes many types of product covering ranges of UHF, VHF, CATV, and FM. Table 1 shows a list-up of the products and Figs. 1, 2 shows the outer dimensions of them.



Type name is printed on the package.

Fig. 1

Cathode Marking Format

	Color Mark 1	Color Mark 2
Front	Orange	Blue
Rear	—	Blue

Table 1 List of NEC's Electronic Tuning Varactor Diodes

Type	Outer dimension	Principal characteristics				Principal application
		V_R(1 μA)	Ct(MAX.)	Ct(MIN.)	Ct(MAX.)/Ct(MIN.)	
1S2207(B)	Fig. 1	25 V	9.5–14.0 pF	3.8–6.4 pF	2.2–2.6	AFC in UHF and VHF bands
1S2208(B)	Fig. 2	28 V	11–12.65 pF	2.0–2.3 pF	4.5	Tuning in UHF and VHF bands
1S2209(B)	Fig. 2	28 V	10.3–12.9 pF	2.0–2.5 pF	4.0	Tuning in UHF and VHF bands
1SV50	Fig. 2	30 V	28.0–32.5 pF	4.9–5.8 pF	5.0–6.5	Tuning in FM/VHF band
1SV50(1)	Fig. 2	30 V	29.0–34.0 pF	4.9–5.8 pF	5.5–7.5	Tuning in FM/VHF band
1SV50S	Fig. 2	30 V	23.0–36.0 pF	14.0–22.0 pF	1.3–2.1	AFC in FM/VHF band
1SV88	Fig. 2	30 V	26.0–32.0 pF	2.6–3.0 pF	8.5–12.5	Tuning in VHF band

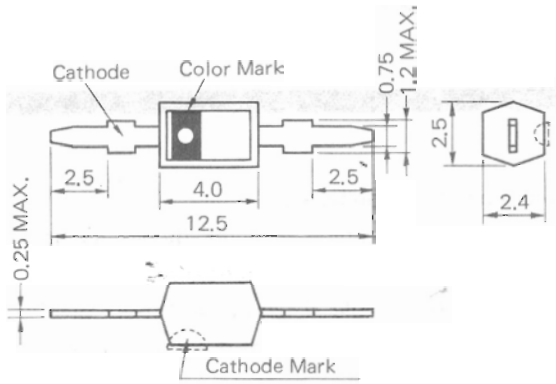


Fig. 2

2. PRINCIPLE OF VARACTOR DIODE OPERATION

A varactor diode is, as stated above in Sec. 1, characterized by the junction capacitance at the reversely biased semiconductor PN junction. A junction capacitance exists in the PN junction of PN junction diode or transistor. Usually this capacitance is unfavorable for ordinary use of diode or transistor. However, this capacitance is well utilized in varactor diodes.

The junction capacitance C_J of a varactor diode is obtained from reverse bias voltage V_R, junction capacitance C_O when $V_R=0$, and contact potential ϕ across the junction by the formula.

$$C_J = C_O \left(1 + \frac{V_R}{\phi}\right)^{-\gamma}$$

This relationship tells that the junction capacitance decreases exponentially with the increase of reverse bias voltage. The exponent γ in the formula depends on the impurity concentration distribution around the junction and it has a value ranging from 1/3 to 2. The dependency of the exponent γ on the impurity concentration distribution is shown in Fig. 5. The dependency of the junction capacitance to reverse bias voltage characteristic on exponent γ is shown in Fig. 6, which demonstrates that a large γ will result in a large capacitance variation.

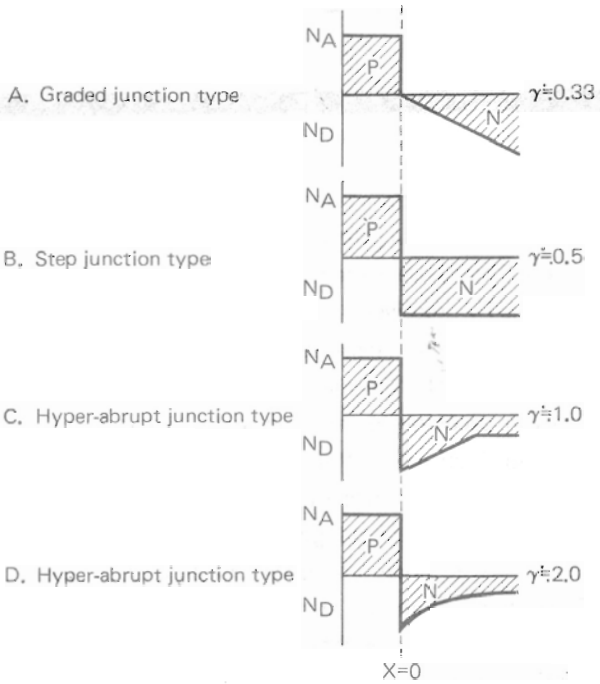


Fig. 5 Dependency of Exponent γ on Impurity Concentration Distribution

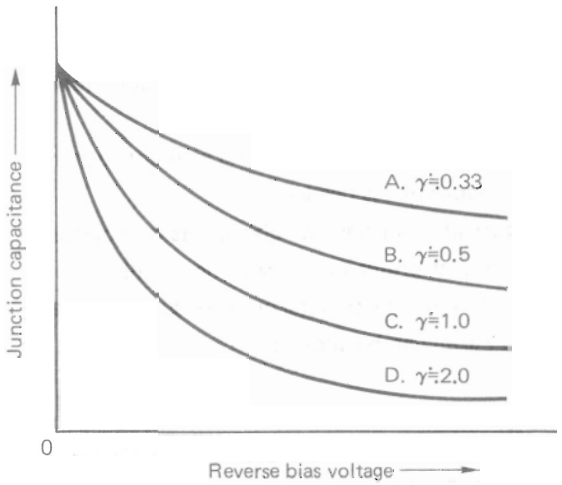


Fig. 6 Dependency of Junction Capacitance to Reverse Bias Voltage Characteristics on Exponent γ

3. CAPACITANCE VARIATION RATIO

Capacitance variation ratio N is defined as a ratio between the junction capacitances at two voltage values. It is expressed in the following formula.

$$N = \frac{C_J(V2)}{C_J(V1)} = \left(\frac{V_1+\phi}{V_2+\phi}\right)^{\gamma} \qquad (V_1 > V_2)$$

where $C_J(V1)$ and $C_J(V2)$ are junction capacitances at reverse bias voltages V_R of V_1 and V_2, respectively.

The specified inter-terminal capacitance C_t(MAX.) in Table 1 is the value for V_R=3 V. Care should be taken if the reverse bias voltage is further decreased for a larger capacitance variation ratio, because, when a signal of large amplitude is applied to the varactor diode held at the lowered reverse bias voltage, the diode might be forward-biased and a signal distortion might be produced.

Since normally ϕ is small, the above formula can be rewritten as

$$N = \frac{C_t(MAX.)}{C_t(MIN.)} = \left(\frac{V_R(MAX.)}{V_R(MIN.)}\right)^{\gamma}$$

The range of tunable frequency with a varactor diode used as a variable capacitance in a tuning circuit is proportional to the square root of capacitance variation ratio N, provided that the floating capacitance can be neglected. Therefore, since a wider frequency range is expected for a large γ, it is necessary to use a hyper-abrupt junction varactor diode with γ=1–2 if a wide freqeuncy adjustment range is needed as in TV bands.

4. EQUIVALENT CIRCUIT OF VARACTOR DIODE

Fig. 7 shows the equivalent circuit of varactor diode.

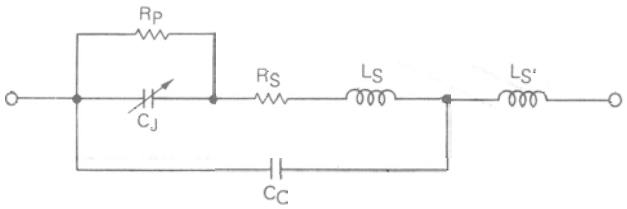


Fig. 7 Equivalent Circuit of Varactor Diode

In the figure,

R_P is resistance parallel to the diode,

R_S is resistance series to the diode,

L_S is lead inductance inside the diode,

L_S' is lead inductance outside the diode, and

C_C is case capacitance.

Since usually the lead inductance L_S and the case capacitance C_C can be neglected, the equivalent circuit diagram in Fig. 7 is simplified to a diagram shown in Fig. 8.

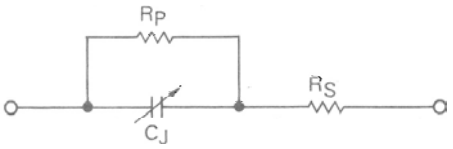


Fig. 8 Simplified Equivalent Circuit

5. Q OF VARACTOR DIODE

The Q of varactor diode will be obtained according to the equivalent circuit shown in Fig. 8.

$$Z = R_S + \frac{R_P \cdot \frac{1}{J\omega C_J}}{R_P + \frac{1}{J\omega C_J}}$$

$$= R_S + \frac{R_P}{1 + j\omega C_J R_P}$$

$$= \frac{R_S + R_P + j\omega C_J R_P R_S}{1 + j\omega C_J R_P}$$

$$= \frac{R_S + R_P + \omega^2 C_J^2 R_P^2 R_S - j\omega C_J R_P^2}{1 + \omega^2 C_J^2 R_P^2}$$

$$= R' - j\frac{1}{\omega C'}$$

where

$$R' = \frac{R_S + R_P + \omega^2 C^2 R_P^2 R_S}{1 + \omega C_J^2 R_P^2}$$

and

$$\omega C' = \frac{1 + \omega^2 C_J^2 R_P^2}{\omega C_J R_P^2}$$

Therefore,

$$Q = \frac{1}{\omega C' R'}$$

$$= \frac{1}{\frac{1+\omega^2 C_J^2 R_P^2}{\omega C_J R_P^2} \cdot \frac{R_S + R_P + \omega^2 C_J^2 R_P^2 R_S}{1+\omega^2 C_J^2 R_P^2}}$$

or

$$Q = \frac{\omega C_J R_P^2}{R_S + R_P + \omega^2 C_J^2 R_P^2 R_S}$$

Since $R_S \ll R_P$ in usual cases, Q takes the form

$$Q \fallingdotseq \frac{\omega C_J R_P}{1+\omega^2 C_J^2 R_P R_S}.$$

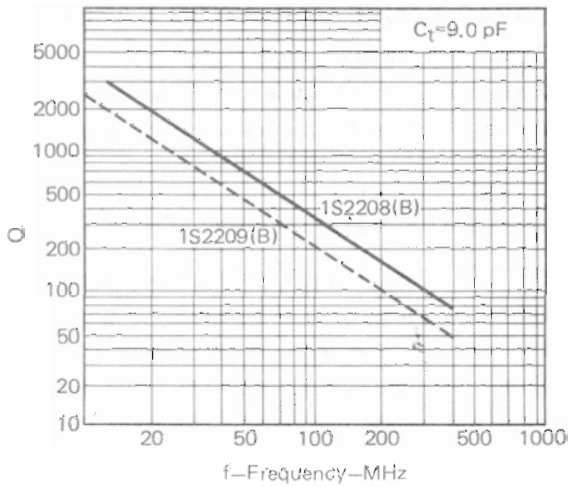
For very low frequencies where $1 \ll \omega^2 C_J^2 R_P R_S$ holds,

$Q \fallingdotseq Q_P = \omega C_J R_P$,

and, on the contrary, for very high frequencies where $1 \ll \omega^2 C_J^2 R_P R_S$ holds,

$$Q \fallingdotseq Q_S = \frac{1}{\omega C_J R_S}$$

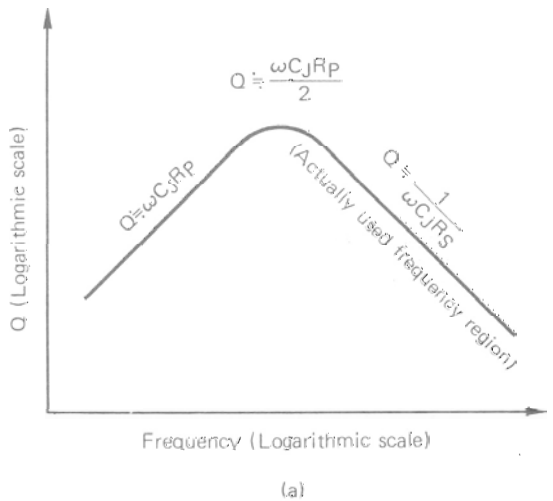
This means that, when the frequency is increased from a very low value, Q increases proportional to the frequency up to a certain frequency, but, beyond this frequency, Q decreases with increasing frequency. This frequency corresponds to the condition $1=\omega^2 C_J R_P R_S$. It is about 30 kHz with 1S2208(B) in which C_J=9 pF, $R_P=1\times10^{12}\,\Omega$, and R_S=0.5 Ω, typically. Thus, in actually used frequency bands, R_P scarcely affects Q and Q is approximated by $1/\omega C_J R_S$. Fig. 9 shows the Q to frequency relationship.



(b)

Fig. 9 Frequency Characteristics of Q

Q is dependent not only on frequency but also on voltage and temperature. At higher reverse bias voltages, Q is large because the capacitance as well as R_S are smaller. On the contrary, at lower voltages, Q is small since the capacitance and R_S are larger. At higher temperatures leakage current increases (R_P decreases) to result in a smaller Q. Conversely, if temperature is lowered, Q is raised. These natures are graphically shown in Figs. 10 and 11.



(a)

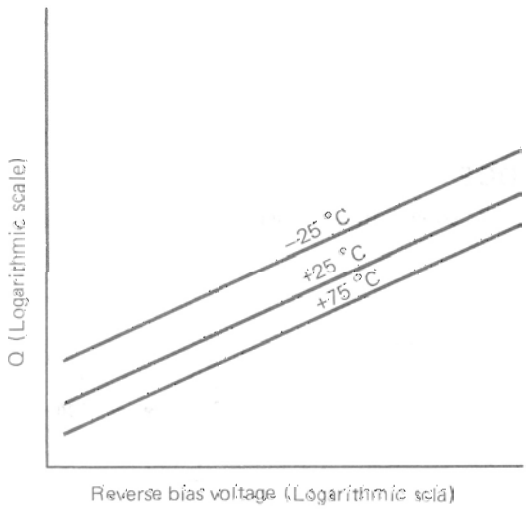


Fig. 10 Temperature Dependency of Q

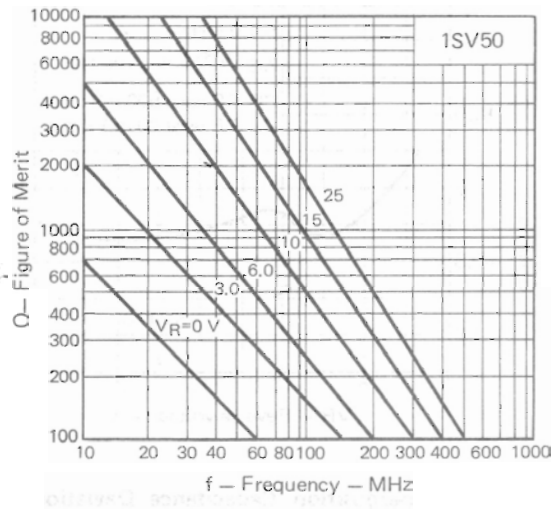


Fig. 11 Reverse Voltage Dependency of Q

6. TEMPERATURE DEPENDENCY OF VARACTOR DIODE

The capacitance of varactor diode is dependent on temperature. The thermal coefficient T_C of the capacitance is a function of reverse bias voltage. The coefficient of 1SV50 is 600 ppm/°C at V_R=1 V. This leads to a thermal coefficient –300 ppm/°C of tuning frequency. Without any temperature compensation, the thermal drift of –30 kHz/°C will be suffered at about 100 MHz. In actual cases, temperature compensation using a capacitor or the like with a negative thermal coefficient (≒–300 ppm/°C) is carried out to suppress the thermal drift to minus several kHz/°C. In receivers operated with a PLL frequency synthesizer, the temperature compensation is automatically carried out. No thermal drift problem is suffered in these receivers.

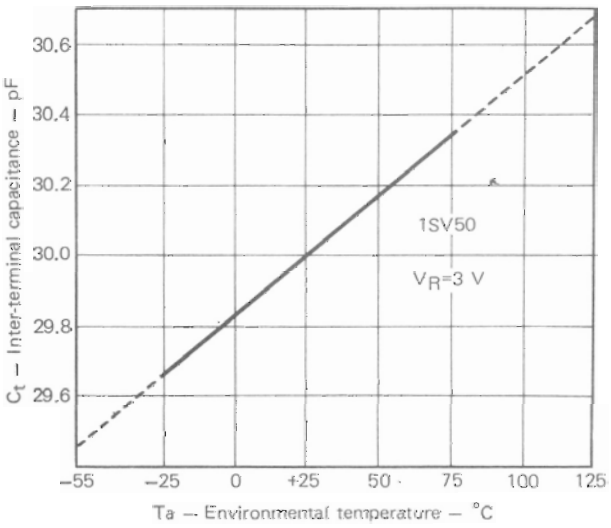


Fig. 12 Temperature Dependency of Capacitance

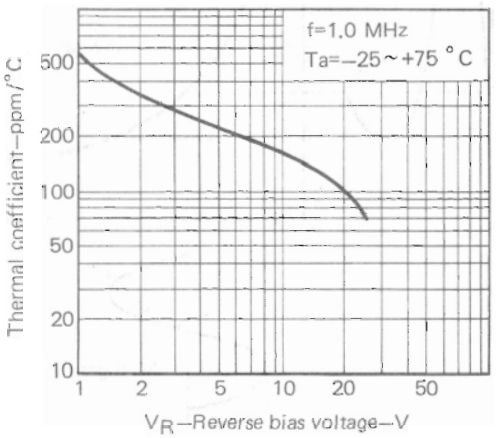


Fig. 13 Thermal Coefficient to Reverse Voltage Characteristic

7. CAPACITANCE DEVIATION IN VARACTOR DIODE BY RF SUPERPOSITION

Since the capacitance of varactor diode generally varies nonlinearly with reverse bias voltage, the application of ac signal having a large amplitude on top of the reverse voltage causes the modulation of the capacitance by the ac signal and the capacitance deviation ΔC is produced with respect to the capacitance for a small amplitude ac signal. The magnitude of ΔC is dependent on the amplitude of the ac signal as well as on the voltage dependency of capacitance. The capacitance modulation by ac signal and the RF-superposition capacitance deviation to reverse voltage characteristic curve are shown in Fig. 14 and 15, respectively.

This effect is marked especially when reverse bias voltage is low. Since this tendency is related to increases in tracking error and distortion, as small oscillation amplitude as possible is desirable. However,

too small an oscillation amplitude deteriorates the receiver sensitivity since the gain of mixer amplifier is reduced. Furthermore the oscillation might be unstable. The application of the oscillator output to the mixer amplifier through a buffer amplifier is recommended. This configuration is also effective to suppress oscillator lock-in caused by a strong input.

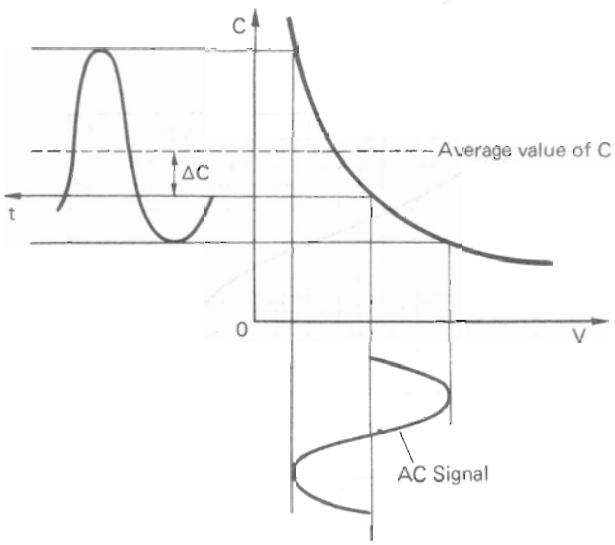


Fig. 14 Capacitance Modulation by AC Signal

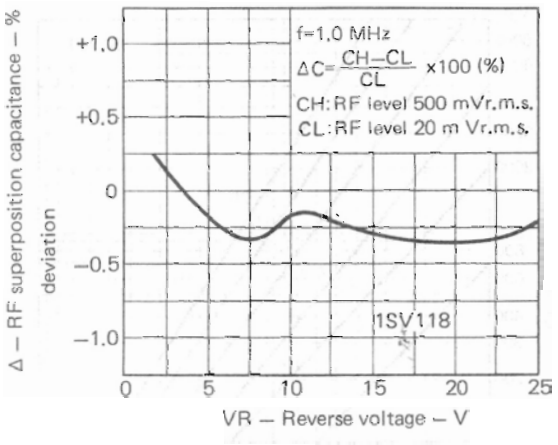


Fig. 15 RF Superposition Capacitance Deviation to Reverse Voltage Characteristic

ZENER DIODE RD[ ]JS, RD[ ]E, RD[ ]F CHARACTERISTICS & RELIABILITY

1. INTRODUCTION

NEC introduced products of Zener diodes in RD[ ] Series early in Japan and then increased their product lines from RD[ ]A to RD[ ]D. High reliability performance proved with our Zener diodes has been highly evaluated by the users in various application fields.

NEC has added new product lines of DHD structure Zener diodes. They are: RD[ ]E Series and RD[ ]F Series, general purpose Zener diodes of 500 mW and 1 W respectively, and RD[ ]JS Series, Zener diodes of 400 mW with sharp V_Z-I_Z characteristics and low noise. At the same time, existing B Standard, in which Zener voltage tolerance is ±5 %, is subdivided into B_1 to B_4 in order to meet requirements for narrower tolerance. Moreover, for RD[ ]E Series, of general purpose 500 mW Zener diodes, product lines which correspond to the subdivided B Standard at different Zener current conditions are added. They are L, L_1 to L_4 (@I_Z= 1 mA) and N, N_1 to N_4 (@I_Z=5 mA).

The Zener diodes in these newly established product lines have improved reliability due to their planar type, small size and light weight realized by the DHD structure, and uniform quality as a result of improved mass production processes. They are, we believe, most appropriate for communications equipment, instruments, various industrial machines, and general appliances.

Following sections explain their characteristics and reliability in detail for recommending users to use them.

2. STRUCTURE

The structure of this new product Zener diode is shown in Fig. 1. As can be seen in the figure, a Zener diode chip is squeezed between two lead terminals (heat sinks) and they are enclosed in a glass tube. They are fused at a temperature as high as 600 °C to 800 °C and then cooled to be fixed. Expansion coefficients of the materials, or the terminals and glass, are properly selected so that the chip and terminlas are, when cooled to a room temperature, strongly pressed.

This Zener diode has, although it is very small and light weight, the feature of low thermal resistance because the silicon chip is cooled to both sides by two heat sinks.

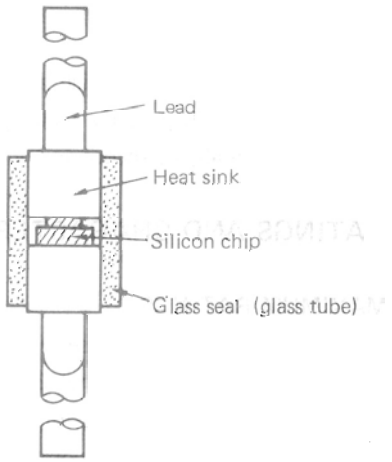
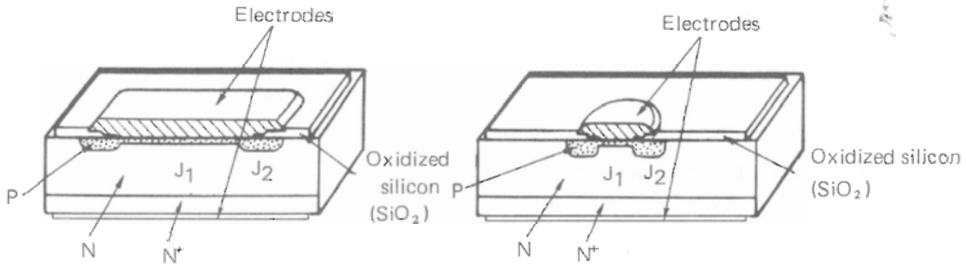


Fig. 1 Structure of DHD Type Zener Diode

In the Zener diode chip, the peripheral portion of the PN junction has, as shown in Figs. 2(a) and 2(b), a double diffusion structure. The breakdown voltage is higher at junction J_2, where the diffusion layer is thicker, than at J_1. Therefore, breakdown on a normal Zener current occurs only in main junction J_1. Under normal operating condition, junction J_2 is kept at a voltage lower than the breakdown voltage of main junction J_1 to permit flow of a slight reverse current. However, the junction is quite stable because its surface is protected by a silicon oxide (SiO_2) passivation. This means that the Zener voltage is hard to be affected by the surface condition of the junction because breakdown occurs always at the junction J_1.



(a) RD[ ] E Series, RD[ ] F Series (b) RD[ ] JS Series

Fig. 2 Zener Diode Chip

In RD[ ]JS Series, low noise and the sharp V_Z-I_Z characteristic are achieved by making the main junction area very small, as shown in Fig. 2(b), increasing current density, uniforming the junction and reducing dynamic impedance which are achieved by the design of high dope.

3. RATINGS AND CHARACTERISTICS

1) MAXIMUM RATINGS

Table 1 lists ratings of these DHD structure Zener diodes in various series. The Zener diodes have, as has been described above, bigger heat radiating effect by lead terminals in comparison with glass-sealed or silkhat-shaped ones and the thermal resistance between the junction and ambient varies with length of leads and area of printed foil.

Fig. 3 shows relationship between junction-to-periphery thermal resistance and printed foil area when packaged with lead length as a parameter in RD2.0E to RD120E Series. Fig. 4 gives P–T_a rating curves under actual packaging conditions obtained from data shown in above figures. (Ex; RD2.0E to RD120E)

Table 1 Maximum Ratings

Items	Symbols	Types			Units	Remarks
		RD[ ]JS	RD[ ]E	RD[ ]F		
Power Dissipation	P	400	500	1000	mW	T_a=25 °C
Junction Temperature	T_j	175			°C	
Storage Temperature	Tstg	−65 to +175			°C	
Surge Reverse Power	P_{RSM}	See Fig. 5				

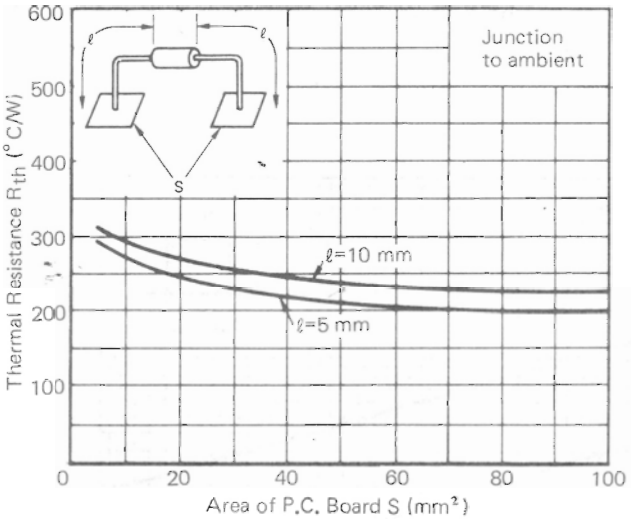


Fig. 3 R_{th}-S Characteristic (Ex; RD2.0E to RD120E)

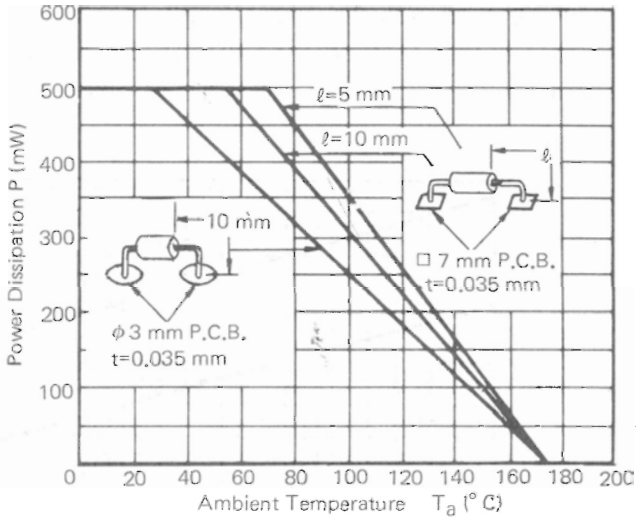


Fig. 4 P-T_a Rating (Ex; RD2.0E to RD120E)

Fig. 5 shows reverse surge power ratings for RD[ ]JS Series, RD[ ]E Series, and RD[ ]F Series. Pay attention to that ratings in RD[ ]JS Series are smaller because junction area is small as mentioned above.

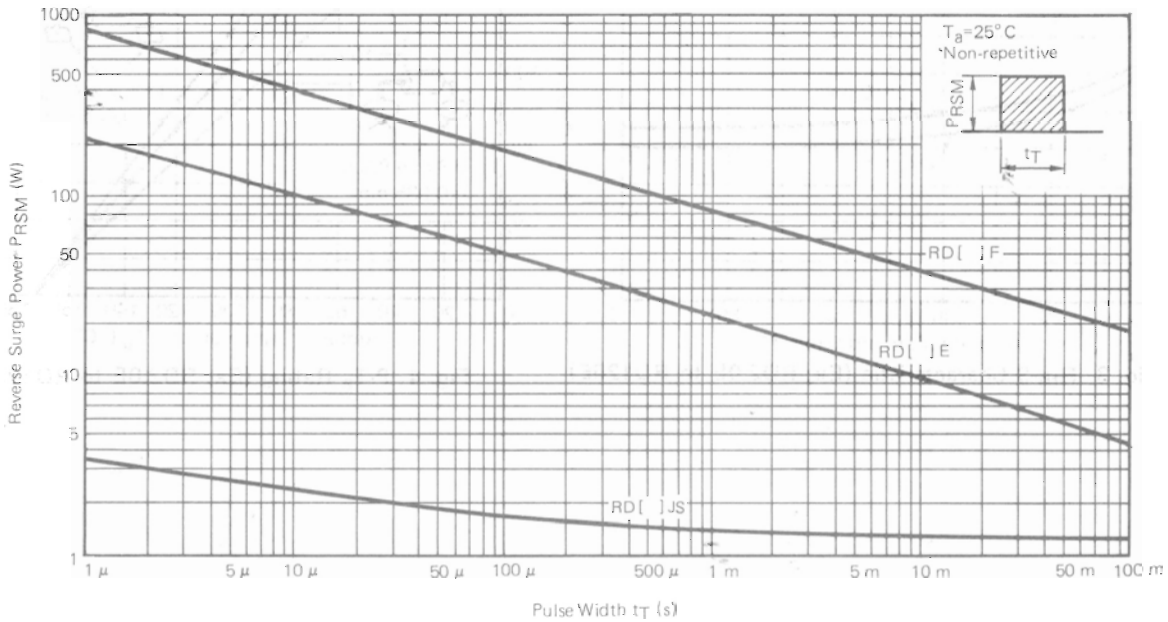


Fig. 5 P_{RSM} Rating

2) ELECTRICAL CHARACTERISTICS

(i) Zener voltage (Vz)

(a) Family

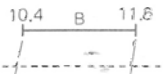
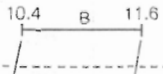
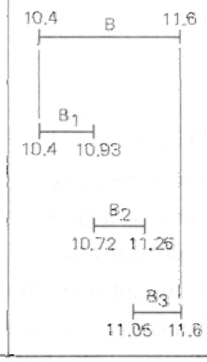
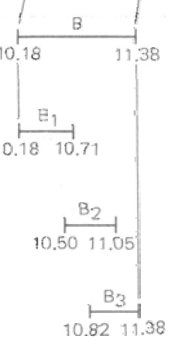
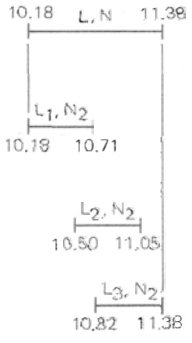
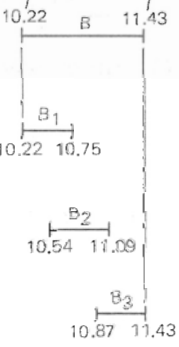
Nominal voltage value of E24 Series is adopted in RD[ ]JS Series, RD[ ]E Series (except RD130E to RD200E), and RD[ ]F Series. For Zener voltages, a family of standards with nominal voltage value ±5 % is provided. Also, subdivided standards where voltages are subdivided into 2, 3, or 4 subdivisions of ±2.5 % are provided.

(b) Subdivided Zener voltage standards

With Zener diodes used for the power source of electronic equipment, narrower Zener voltage tolerance has become demanded year by year in order to improve precision, make compact, and reduce cost.

Series of subdivided standards listed in Table 2 have been established by NEC to meet this demand.

Table 2 System of V_Z Subdivided

Zener Voltage V_Z		RD[ ]JS Suffix B	RD[ ]E Suffix B, C	RD[ ]E Suffix L	RD[ ]E Suffix N	RD[ ]F Suffix B, C
Voltage ranges		4.7 to 39 V	2.0 to 200 V	2.7 to 39 V	2.7 to 20 V	2.0 to 82 V
Subdivided Voltage ranges			2.7 to 39 V			2.7 to 39 V
Subdivided number		3 divisions	2.7 to 3.9 V : 2 divisions 4.3 to 20 V : 3 divisions 22 to 39 V : 4 divisions 10 V, 20 V : 4 divisions 39 V : 7 divisions		— — —	4.3 to 39 V 3 divisions
I_Z conditions		5 mA	2 to 10 V: 20 mA 11 to 20 V: 10 mA 22 to 56 V: 5 mA 62 to 100 V: 2 mA 110 to 200 V: 1 mA	1 mA	5 mA	2 to 10 V: 40 mA 11 to 20 V: 20 mA 22 to 56 V: 10 mA 62 to 82 V: 5 mA
Example V_Z=11 V	DC					
	Pulse (40 ms)					

(c) Zener voltage test method

A Zener diode shows different Zener voltages in initial state of energizing and in steady state. The difference between them depends on temperature rise caused by the current and on temperature coefficients. Zener voltage test methods are specified for Zener diodes. Table 3 lists those test methods.

Table 3 Zener Voltage Test Methods

Types	Test Methods	
	Pulse (40 ms)	DC
RD2.0E to RD39E Suffix B, C		○
RD43E 60 RD200E Suffix B	○	
RD[ ]E Suffix B, C (Subdivided)	○	
RD[ ]E Suffix L & L (Subdivided)	○	
RD[ ]E Suffix N & N (Subdivided)	○	
RD2.0F to RD39F Suffix B, C		○
RD43F to RD82F Suffix B	○	
RD[ ]F Suffix B, C (Subdivided)	○	
RD[ ]JS Suffix B & B (Subdivided)	○	

○ Drift of Zener voltage

$$V_Z' = V_Z + I_Z \cdot V_Z \cdot Z_{th\ (t'-t)} \cdot \gamma_Z'$$

$$\gamma_Z' = \frac{\gamma_Z \cdot V_Z}{100}$$

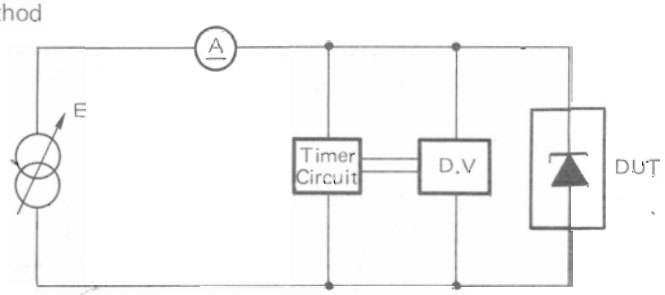
t, t' : Time (ms)
V_Z : Zener voltage at t (V)
V_Z' : Zener voltage at t' (V)
I_Z : Zener current (A)
$Z_{th\ (t)}$: Transient thermal impedance at t (°C/W)
$Z_{th\ (t')}$: Transient thermal impedance at t' (°C/W)
$Z_{th\ (t'-t)}$: $Z_{th\ (t')} - Z_{th(t)}$ (°C/W)
γ_Z : Zener voltage temperature coefficient (%/°C)
γ_Z' : Zener voltage temperature coefficient (V/°C)

○ Zener voltage test circuit

Symbol mark

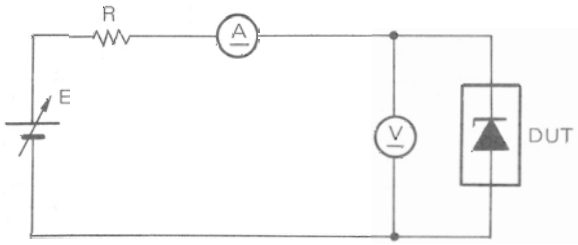
Mark		Term
	E	Constant voltage source
	E	Constant current source
	R	Resistance
Ⓐ		D.C current meter
Ⓥ		Digital voltage meter (D.V)
	DUT	Sample

① 40 ms, 1 s method

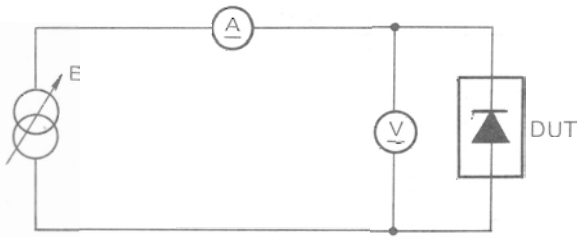


② D.C. method

a)



b)



(d) Tables 4, 5, and 6 give Zener voltages under different Zener current conditions for RD[ ]JS Series, RD[ ]E Series, and RD[ ]F Series.

These tables are specially useful for Zener diodes of which Zener voltages are lower than 5 to 6 V because shifts of Zener Voltage at the different Zener Current become larger in those diodes.

In RD[ ]E Series, Subdivided Zener Voltage Standards L (L_1 to L_4) at 1 mA and N (N_1 to N_4) at 5 mA which are similar to the Zener Voltage tolerance of B Standard mentioned the above are provided. Utilizing of these Series is recommended as they are very convenient.

Table 4-1/2 RD[ ]JS Zener Voltage Subdivided

Type Number	Suffix	Zener Voltage (V) ☐ Values for reference Pulse 40 ms							
		I_Z = 0.1 mA		I_Z = 0.5 mA		I_Z = 1 mA		I_Z = 5 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD4.7JS	B1	3.10	3.60	3.72	4.20	3.94	4.37	4.42	4.61
	B2	3.39	4.01	4.02	4.48	4.21	4.60	4.55	4.75
	B3	3.77	4.42	4.30	4.75	4.45	4.82	4.69	4.90
RD5.1JS	B1	4.14	4.64	4.60	4.96	4.69	4.99	4.84	5.04
	B2	4.49	4.96	4.83	5.15	4.89	5.17	4.98	5.20
	B3	4.86	5.23	5.07	5.33	5.09	5.34	5.14	5.37
RD5.6JS	B1	5.14	5.46	5.24	5.51	5.27	5.52	5.31	5.55
	B2	5.38	5.65	5.42	5.69	5.45	5.71	5.49	5.73
	B3	5.59	5.85	5.60	5.89	5.63	5.88	5.67	5.92
RD6.2JS	B1	5.79	6.05	5.79	6.09	5.82	6.10	5.86	6.12
	B2	5.99	6.26	5.99	6.30	6.60	6.93	6.06	6.33
	B3	6.19	6.46	6.19	6.50	6.22	6.51	6.26	6.53
RD6.8JS	B1	6.40	6.66	6.40	6.70	6.43	6.71	6.47	6.73
	B2	6.58	6.86	6.58	6.90	6.61	6.91	6.65	6.93
	B3	6.79	7.07	6.79	7.11	6.82	7.12	6.86	7.14
RD7.5JS	B1	7.00	7.28	7.00	7.32	7.03	7.33	7.06	7.36
	B2	7.22	7.52	7.22	7.56	7.25	7.57	7.28	7.60
	B3	7.45	7.76	7.45	7.80	7.49	7.81	7.52	7.84
RD8.2JS	B1	7.68	8.01	7.70	8.06	7.73	8.07	7.76	8.10
	B2	7.94	8.27	7.95	8.32	7.98	8.33	8.02	8.36
	B3	8.19	8.54	8.21	8.59	8.24	8.60	8.28	8.64
RD9.1JS	B1	8.46	8.83	8.49	8.89	8.51	8.90	8.56	8.93
	B2	8.75	9.12	8.77	9.18	8.80	9.18	8.85	9.23
	B3	9.03	9.42	9.06	9.48	9.09	9.49	9.15	9.55
RD10JS	B1	9.33	9.75	9.35	9.82	9.39	9.83	9.45	9.87
	B2	9.64	10.08	9.67	10.15	9.70	10.16	9.77	10.21
	B3	9.98	10.42	10.00	10.49	10.04	10.50	10.11	10.55

Table 4-2/2 RD[ ]JS Zener Voltage Subdivided

Type Number	Suffix	Zener Voltage (V) ☐ Values for reference Pulse 40 ms							
		I_Z = 0.1 mA		I_Z = 0.5 mA		I_Z = 1 mA		I_Z = 5 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD11JS	B1	10.31	10.74	10.34	10.81	10.37	10.82	10.44	10.88
	B2	10.63	11.07	10.65	11.14	10.69	11.16	10.76	11.22
	B3	10.95	11.41	10.89	11.56	11.01	11.50	11.10	11.56
RD12JS	B1	11.28	11.81	11.30	11.82	11.34	11.83	11.42	11.90
	B2	11.60	12.15	11.62	12.15	11.65	12.16	11.74	12.24
	B3	11.92	12.50	12.84	12.53	11.98	12.52	12.08	12.60
RD13JS	B1	12.31	12.94	12.32	12.94	12.36	12.95	12.47	13.03
	B2	12.74	13.39	12.75	13.39	12.78	13.40	12.91	13.49
	B3	13.19	13.84	13.20	13.85	13.23	13.86	13.37	13.96
RD15JS	B1	13.65	14.34	13.66	14.34	13.69	14.35	13.84	14.46
	B2	14.14	14.85	14.15	14.85	14.17	14.86	14.34	14.98
	B3	14.64	15.36	14.65	15.36	14.68	15.38	14.85	15.52
RD16JS	B1	15.14	15.84	15.16	15.84	15.18	15.86	15.37	16.01
	B2	15.59	16.32	15.62	16.33	15.64	16.34	15.85	16.51
	B3	16.08	16.89	16.10	16.90	16.13	16.91	16.35	17.09
RD18JS	B1	16.63	17.49	16.66	17.50	16.69	17.52	16.94	17.70
	B2	17.22	18.13	17.25	18.14	17.28	18.16	17.56	18.35
	B3	17.83	18.78	17.81	17.84	17.91	18.81	18.21	19.03
RD20JS	B1	18.46	19.42	18.53	19.43	18.57	19.46	18.86	19.70
	B2	19.07	20.10	19.15	20.11	19.18	20.14	19.52	20.39
	B3	19.73	20.79	19.82	20.81	19.86	20.83	20.21	21.08
RD22JS	B1	20.36	21.46	20.48	21.48	20.52	21.50	20.88	21.77
	B2	21.00	22.14	21.14	22.17	21.18	22.18	21.54	22.47
	B3	21.66	22.82	21.82	22.86	21.86	22.88	22.23	23.17
RD24JS	B1	22.30	23.65	22.50	23.68	22.53	23.69	22.93	23.96
	B2	23.13	24.47	23.34	24.49	23.36	24.51	23.72	24.78
	B3	23.92	25.26	24.14	25.28	24.16	25.30	24.54	25.57

Table 5-1/3 RD[ ]E Zener Voltage Subdivided

Type Number	Suffix	Zener Voltage (V) ▭ Values for reference Pulse 40 ms							
		I_Z = 1 mA		I_Z = 5 mA		I_Z = 10 mA		I_Z = 20 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD2.0E	B1	1.24	1.38	1.55	1.73	1.69	1.89	1.88	2.10
	B2	1.32	1.45	1.66	1.82	1.80	1.98	2.02	2.20
RD2.2E	B1	1.38	1.51	1.73	1.89	1.89	2.08	2.12	2.30
	B2	1.45	1.59	1.83	2.00	2.00	2.18	2.22	2.41
RD2.4E	B1	1.52	1.64	1.91	2.08	2.10	2.28	2.33	2.52
	B2	1.59	1.72	1.99	2.17	2.18	2.38	2.43	2.63
RD2.7E	B1	1.65	1.83	2.08	2.27	2.28	2.50	2.54	2.75
	B2	1.76	1.94	2.21	2.42	2.43	2.65	2.69	2.91
RD3.0E	B1	1.87	2.08	2.34	2.57	2.58	2.80	2.85	3.07
	B2	2.00	2.18	2.49	2.70	2.72	2.94	3.01	3.22
RD3.3E	B1	2.12	2.31	2.67	2.84	2.87	3.09	3.16	3.38
	B2	2.26	2.42	2.78	2.98	3.03	3.24	3.32	3.53
RD3.6E	B1	2.35	2.54	2.90	3.13	3.17	3.40	3.47	3.68
	B2	2.47	2.69	3.05	3.28	3.32	3.55	3.62	3.83
RD3.9E	B1	2.64	2.86	3.22	3.46	3.48	3.72	3.77	3.98
	B2	2.75	3.01	3.36	3.62	3.63	3.88	3.92	4.14
RD4.3E	B1	2.91	3.15	3.52	3.77	3.78	4.03	4.05	4.26
	B2	3.07	3.34	3.68	3.95	3.95	4.19	4.20	4.40
	B3	3.27	3.54	3.87	4.13	4.11	4.35	4.34	4.53
RD4.7E	B1	3.38	3.69	4.03	4.27	4.26	4.48	4.47	4.65
	B2	3.51	3.84	4.15	4.40	4.38	4.60	4.59	4.77
	B3	3.65	4.14	4.29	4.65	4.56	4.84	4.71	4.91
RD5.1E	B1	3.85	4.31	4.49	4.81	4.70	4.94	4.85	5.03
	B2	4.16	4.74	4.69	5.10	4.85	5.15	4.97	5.18
	B3	4.43	4.96	4.90	5.32	5.02	5.34	5.12	5.35
RD5.6E	B1	4.77	5.16	5.15	5.43	5.23	5.49	5.29	5.52
	B2	5.19	5.60	5.38	5.65	5.42	5.69	5.46	5.70
	B3	5.43	5.77	5.58	5.85	5.61	5.88	5.64	5.88
RD6.2E	B1	5.70	6.00	5.75	6.04	5.77	6.05	5.81	6.06
	B2	5.90	6.22	5.94	6.23	5.96	6.24	5.99	6.24
	B3	6.06	6.37	6.09	6.38	6.12	6.39	6.16	6.40
RD6.8E	B1	6.20	6.53	6.20	6.55	6.28	6.57	6.32	6.59
	B2	6.39	6.72	6.43	6.75	6.47	6.77	6.52	6.79
	B3	6.56	6.90	6.63	6.91	6.65	6.95	6.70	6.97

Table 5-2/3 RD[ ]E Zener Voltage Subdivided

Type Number	Suffix	Zener Voltage (V) ☐ Values for reference Pulse 40 ms							
		I_Z = 1 mA		I_Z = 5 mA		I_Z = 10 mA		I_Z = 20 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD7.5E	B1	6.76	7.11	6.80	7.14	6.84	7.16	6.88	7.19
	B2	6.99	7.33	7.03	7.35	7.07	7.38	7.11	7.41
	B3	7.21	7.56	7.25	7.59	7.29	7.61	7.33	7.64
RD8.2E	B1	7.40	7.79	7.45	7.82	7.50	7.85	7.56	7.90
	B2	7.66	8.04	7.70	8.07	7.76	8.10	7.82	8.15
	B3	7.91	8.30	7.96	8.33	8.01	8.36	8.07	8.41
RD9.1E	B1	8.24	8.64	8.27	8.67	8.30	8.67	8.33	8.70
	B2	8.51	8.95	8.53	8.96	8.56	8.96	8.61	8.99
	B3	8.79	9.25	8.82	9.26	8.85	9.26	8.89	9.29
RD10E	B1	9.05	9.51	9.08	9.52	9.11	9.54	9.19	9.59
	B2	9.35	9.82	9.35	9.83	9.41	9.85	9.48	9.90
	B3	9.70	10.23	9.72	10.24	9.75	10.26	9.82	10.30
RD11E	B1	9.99	10.59	10.04	10.63	10.18	10.63		
	B2	10.41	10.88	10.46	10.92	10.50	10.95		
	B3	10.73	11.20	10.78	11.22	10.82	11.26		
RD12E	B1	11.03	11.55	11.08	11.59	11.13	11.63		
	B2	11.40	11.84	11.45	11.88	11.50	11.92		
	B3	11.70	12.22	11.75	12.26	11.80	12.30		
RD13E	B1	12.07	12.62	12.12	12.66	12.18	12.71		
	B2	12.48	13.77	12.53	13.11	12.59	13.16		
	B3	12.92	13.53	12.97	13.57	13.03	13.62		
RD15E	B1	13.34	13.99	13.40	14.03	13.48	14.09		
	B2	13.81	14.46	13.87	14.50	13.95	14.56		
	B3	14.28	14.92	14.34	14.96	14.42	15.02		
RD16E	B1	14.70	15.38	14.77	15.42	14.87	15.50		
	B2	15.16	15.84	15.23	15.88	15.33	15.96		
	B3	15.61	16.38	15.68	16.42	15.79	16.50		
RD18E	B1	16.10	16.88	16.21	16.97	16.34	17.06		
	B2	16.66	17.49	16.77	17.58	16.90	17.67		
	B3	17.27	18.12	17.39	18.31	17.51	18.30		
RD20E	B1	17.83	18.69	17.95	18.81	18.11	18.92		
	B2	18.46	19.34	18.58	19.46	18.73	19.57		
	B3	19.14	20.02	19.26	20.14	19.38	20.22		
	B4	19.63	20.52	19.79	20.64	19.88	20.72		

Table 5-3/3 RD[ ]E Zener Voltage Subdivided

Type Number	Suffix	Zener Voltage (V) ☐ Values for reference Pulse 40 ms							
		I_Z = 1 mA		I_Z = 5 mA		I_Z = 10 mA		I_Z = 20 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD22E	B1	20.10	20.95	20.23	21.08				
	B2	20.63	21.53	20.76	21.65				
	B3	21.09	21.97	21.22	22.09				
	B4	21.55	22.49	21.68	22.61				
RD24E	B1	22.08	22.98	22.26	23.12				
	B2	22.57	23.59	22.75	23.73				
	B3	23.11	24.13	23.29	24.27				
	B4	23.63	24.67	23.81	24.81				
RD27E	B1	24.02	25.32	24.26	25.52				
	B2	24.73	26.06	24.97	26.26				
	B3	25.39	26.75	25.63	26.95				
	B4	26.05	27.44	26.29	27.64				
RD30E	B1	26.71	28.15	26.99	28.39				
	B2	27.42	28.89	27.70	29.13				
	B3	28.08	29.58	28.36	29.82				
	B4	28.74	30.27	29.02	30.51				
RD33E	B1	29.36	30.88	29.68	31.22				
	B2	30.00	31.61	30.32	31.88				
	B3	30.58	32.23	30.90	32.50				
	B4	30.88	32.84	31.49	33.11				
RD36E	B1	31.78	33.48	32.14	33.79				
	B2	32.43	34.18	32.79	34.49				
	B3	33.04	34.82	33.40	35.13				
	B4	33.65	35.46	34.01	35.77				
RD39E	B1	34.28	36.13	34.68	36.47				
	B2	34.96	36.85	35.36	37.19				
	B3	35.60	37.51	36.00	37.85				
	B4	36.23	38.18	36.63	38.52				
	B5	36.96	38.95	37.36	39.29				
	B6	37.67	39.77	38.14	40.11				
	B7	38.54	40.46	83.94	40.80				

Table 6-1/3 RD[ ]F Zener Voltage Subdivided

Type Number	Suffix	Zener Voltage (V) ☐ Values for reference Pulse 40 ms							
		I_Z = 1 mA		I_Z = 10 mA		I_Z = 20 mA		I_Z = 40 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD2.0F	B1	1.11	1.39	1.58	1.84			1.88	2.12
	B2	1.20	1.48	1.69	1.95			2.01	2.25
RD2.2F	B1	1.27	1.54	1.76	2.03			2.11	2.34
	B2	1.33	1.62	1.84	2.13			2.21	2.45
RD2.4F	B1	1.39	1.69	1.93	2.22			2.31	2.55
	B2	1.46	1.76	1.98	2.31			2.41	2.65
RD2.7F	B1	1.54	1.85	2.15	2.43			2.52	2.78
	B2	1.65	1.97	2.27	2.57			2.68	2.93
RD3.0F	B1	1.75	2.08	2.42	2.71			2.83	3.07
	B2	1.86	2.19	2.55	2.85			2.97	3.22
RD3.3F	B1	1.97	2.31	2.71	3.00			3.13	3.37
	B2	2.10	2.43	2.85	3.14			3.27	3.51
RD3.6F	B1	2.23	2.58	3.01	3.32			3.43	3.68
	B2	2.36	2.71	3.17	3.49			3.58	3.83
RD3.9F	B1	2.50	2.87	3.34	3.68			3.73	4.00
	B2	2.64	3.03	3.52	3.85			3.88	4.15
RD4.3F	B1	2.79	3.18	3.69	4.01			4.03	4.28
	B2	2.92	3.34	3.83	4.18			4.15	4.41
	B3	3.05	3.50	3.99	4.34			4.28	4.55
RD4.7F	B1	3.20	3.62	4.14	4.46			4.41	4.65
	B2	3.34	3.83	4.29	4.61			4.53	4.78
	B3	3.49	4.06	4.44	4.76			4.66	4.91
RD5.1F	H1	3.65	4.30	4.60	4.93			4.79	5.05
	B2	3.87	4.60	4.78	5.12			4.95	5.22
	B3	4.00	4.86	4.96	5.30			5.10	5.38
RD5.6F	B1	4.42	5.16	5.16	5.50			5.28	5.56
	B2	4.76	5.46	5.37	5.71			5.46	5.75
	B3	5.12	5.79	5.58	5.92			5.65	5.95
RD6.2F	B1	5.32	6.05	5.71	6.11			5.76	6.14
	B2	5.67	6.27	5.93	6.30			5.98	6.33
	B3	5.95	6.47	6.12	6.49			6.17	6.52
RD6.8F	B1	6.19	6.66	6.30	6.68			6.35	6.71
	B2	6.44	6.85	6.50	6.87			6.55	6.90
	B3	6.63	7.05	6.69	7.07			6.74	7.10

Table 6-2/3 RD[ ]F Zener Voltage Subdivided

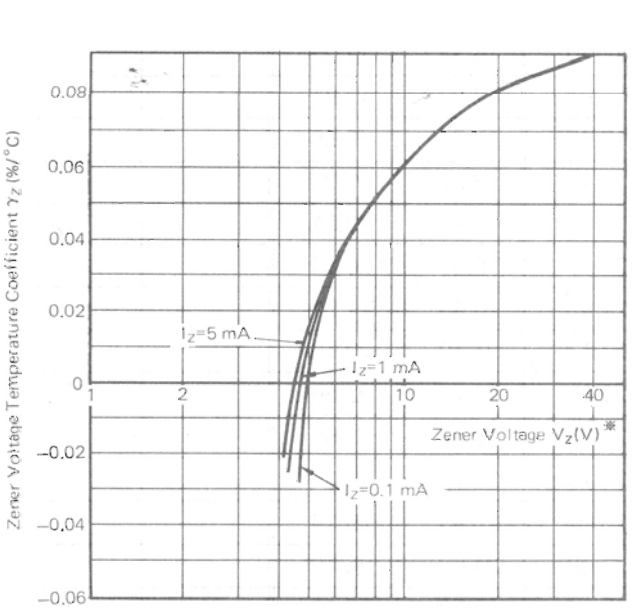
Type Number	Suffix	Zener Voltage (V) ☐ Values for reference Pulse 40 ms							
		I_Z = 1 mA		I_Z = 10 mA		I_Z = 20 mA		I_Z = 40 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD7.5F	B1	6.82	7.28	6.88	7.30			6.93	7.33
	B2	7.06	7.49	7.11	7.52			7.17	7.55
	B3	7.28	7.74	7.33	7.77			7.39	7.80
RD8.2F	B1	7.46	7.97	7.52	8.00			7.58	8.03
	B2	7.75	8.21	7.81	8.24			7.87	8.28
	B3	7.99	8.47	8.05	8.50			8.12	8.54
RD9.1F	B1	8.21	8.72	8.26	8.76			8.34	8.80
	B2	8.50	9.00	8.56	9.03			8.64	9.08
	B3	8.76	9.29	8.82	9.32			8.91	9.38
RD10F	B1	9.01	9.57	9.06	9.61			9.16	9.67
	B2	9.34	9.88	9.39	9.92			9.50	9.99
	B3	9.66	10.29	9.72	10.33			9.83	10.40
RD11F	B1	10.11	10.69	10.17	10.73	10.22	10.75		
	B2	10.43	10.02	10.48	11.06	10.54	11.09		
	B3	10.75	11.36	10.81	11.40	10.87	11.43		
RD12F	B1	11.07	11.69	11.13	11.74	11.19	11.77		
	B2	11.37	12.01	11.44	12.06	11.50	12.09		
	B3	11.67	12.33	11.73	12.38	11.80	12.41		
RD13F	B1	12.05	12.77	12.12	12.81	12.19	12.85		
	B2	12.48	13.21	12.56	13.26	12.63	13.30		
	B3	12.95	13.73	13.03	13.79	13.11	13.83		
RD15F	B1	13.39	14.18	13.47	14.23	13.55	14.28		
	B2	13.88	14.66	13.96	14.72	14.05	14.77		
	B3	14.34	15.14	14.43	15.21	14.52	15.26		
RD16F	B1	14.79	15.63	14.88	15.69	14.98	15.75		
	B2	15.25	16.10	15.34	16.17	15.44	16.23		
	B3	15.69	16.58	15.78	16.65	15.89	16.71		

Table 6-3/3 RD[ ]F Zener Voltage Subdivided

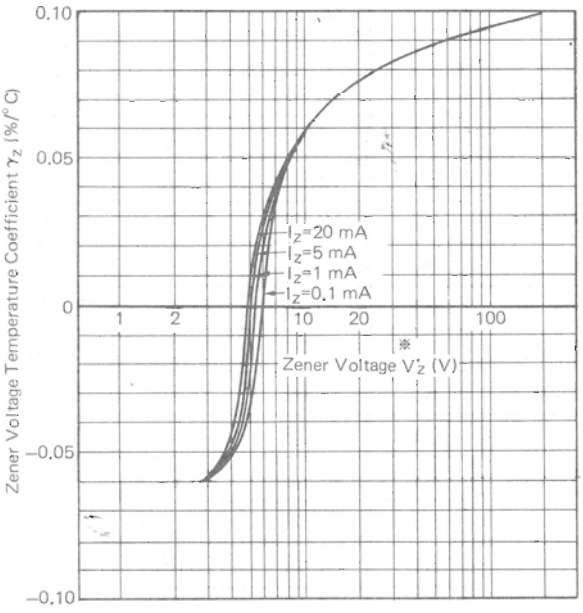
Type Number	Suffix	Zener Voltage (V) ▭ Values for reference Pulse 40 ms							
		I_Z = 1 mA		I_Z = 10 mA		I_Z = 20 mA		I_Z = 40 mA	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
RD18F	B1	16.16	17.13	16.26	17.20	16.37	17.27		
	B2	16.81	17.77	16.91	17.84	17.03	17.91		
	B3	17.41	18.40	17.52	18.47	17.64	18.55		
RD20F	B1	18.02	19.06	18.13	19.13	18.26	19.21		
	B2	18.78	19.75	18.80	19.83	18.93	19.91		
	B3	19.33	20.70	19.46	20.76	19.59	20.84		
RD22F	B1	20.28	21.41	20.36	21.45	20.45	21.51		
	B2	20.92	22.07	21.00	22.12	21.10	22.18		
	B3	21.56	22.74	21.65	22.80	21.75	22.86		
RD24F	B1	22.23	23.47	22.33	23.53	22.44	23.59		
	B2	22.95	24.24	23.06	24.29	23.17	24.36		
	B3	23.67	25.01	23.78	25.07	23.90	25.14		
RD27F	B1	24.49	25.96	24.51	26.03	24.63	26.10		
	B2	25.45	26.98	25.57	27.04	25.70	27.12		
	B3	26.55	28.27	26.59	28.34	26.72	28.43		
RD30F	B1	27.14	28.92	27.29	29.00	27.43	29.09		
	B2	28.33	29.92	28.49	30.00	28.64	30.10		
	B3	29.24	31.07	29.41	31.16	29.57	31.26		
RD33F	B1	30.01	31.78	30.18	31.86	30.35	31.97		
	B2	31.13	32.86	31.31	32.95	31.49	33.06		
	B3	32.01	33.94	32.20	34.03	32.39	34.15		
RD36F	B1	32.85	34.72	33.04	34.82	33.24	34.94		
	B2	33.85	35.77	34.05	35.88	34.26	36.01		
	B3	34.76	36.76	34.97	36.87	35.19	37.01		
RD39F	B1	35.67	37.74	35.88	37.86	36.11	38.00		
	B2	36.68	38.78	36.90	38.89	37.14	39.04		
	B3	37.65	40.59	37.88	40.68	38.13	40.80		

(ii) Temperature coefficient of Zener voltage (γ_Z)

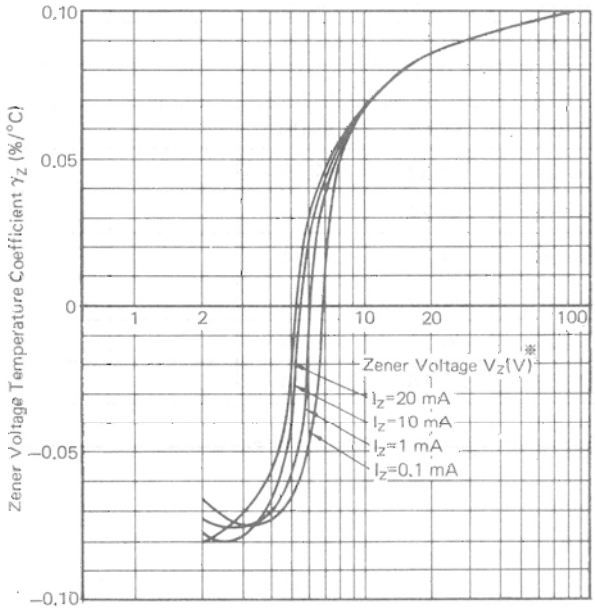
The temperature coefficient of the Zener voltage somewhat varies with the type of PN junction and junction area. Fig. 6 and Table 7 give temperature coefficients of Zener voltages in RD[ ]JS Series, RD[ ]E Series, and RD[ ]F Series.



(a) RD[ ]JS



(b) RD[ ]E



(c) RD[ ]F

Fig. 6 γ_Z-V_Z Characteristics

(*) V_Z: Refer to Table 4, 5 and 6.

Table 7 V_Z Temperature Coefficients (TYP.)

RD[ ]E Series		RD[ ]F Series		RD[ ]JS Series	
Types	Temperature Coefficients of V_Z γ_Z TYP. (%/°C)	Types	Temperature Coefficients of V_Z γ_Z TYP. (%/°C)	Types	Temperature Coefficients of V_Z γ_Z TYP. (%/°C)
RD2.0E	−0.055	RD2.0F	−0.080	RD4.7JS	+0.007
RD2.2E	−0.057	RD2.2F	−0.080	RD5.1JS	+0.018
RD2.4E	−0.058	RD2.4F	−0.078	RD5.6JS	+0.028
RD2.7E	−0.059	RD2.7F	−0.076	RD6.2JS	+0.036
RD3.0E	−0.059	RD3.0F	−0.072	RD6.8JS	+0.043
RD3.3E	−0.056	RD3.3F	−0.068	RD7.5JS	+0.048
RD3.6E	−0.053	RD3.6F	−0.064	RD8.2JS	+0.053
RD3.9E	−0.048	RD3.9F	−0.058	RD9.1JS	+0.057
RD4.3E	−0.038	RD4.3F	−0.049	RD10JS	+0.061
RD4.7E	−0.022	RD4.7F	−0.035	RD11JS	+0.064
RD5.1E	+0.010	RD5.1F	−0.009	RD12JS	+0.067
RD5.6E	+0.024	RD5.6F	+0.011	RD13JS	+0.070
RD6.2E	+0.033	RD6.2F	+0.032	RD15JS	+0.073
RD6.8E	+0.038	RD6.8F	+0.042	RD16JS	+0.076
RD7.5E	+0.044	RD7.5F	+0.051	RD18JS	+0.079
RD8.2E	+0.049	RD8.2F	+0.057	RD20JS	+0.081
RD9.1E	+0.053	RD9.1F	+0.062	RD22JS	+0.082
RD10E	+0.057	RD10F	+0.067	RD24JS	+0.084
RD11E	+0.061	RD11F	+0.071	RD27JS	+0.086
RD12E	+0.064	RD12F	+0.074	RD30JS	+0.087
RD13E	+0.067	RD13F	+0.077	RD33JS	+0.088
RD15E	+0.069	RD15F	+0.079	RD36JS	+0.089
RD16E	+0.071	RD16F	+0.081	RD39JS	+0.090
RD18E	+0.073	RD18F	+0.083		
RD20E	+0.075	RD20F	+0.085		
RD22E	+0.077	RD22F	+0.086		
RD24E	+0.079	RD24F	+0.087		
RD27E	+0.081	RD27F	+0.089		
RD30E	+0.082	RD30F	+0.090		
RD33E	+0.083	RD33F	+0.091		
RD36E	+0.084	RD36F	+0.092		
RD39E	+0.085	RD39F	+0.093		
RD43E	+0.087	RD43F	+0.094		
RD47E	+0.088	RD47F	+0.094		
RD51E	+0.089	RD51F	+0.095		
RD56E	+0.090	RD56F	+0.096		
RD62E	+0.090	RD62F	+0.097		
RD68E	+0.091	RD68F	+0.098		
RD75E	+0.092	RD75F	+0.098		
RD82E	+0.093	RD82F	+0.099		
RD91E	+0.094				
RD100E	+0.095				
RD110E	+0.095				
RD120E	+0.096				
RD130E	+0.099				
RD140E	+0.102				
RD150E	+0.105				
RD160E	+0.108				
RD170E	+0.111				
RD180E	+0.114				
RD190E	+0.117				
RD200E	+0.120				

Note: I_Z : Refer to Table 4, 5 and 6.

(iii) Dynamic impedance (Z_Z)

Fig. 7 shows comparison of dynamic impedance among RD[ ]JS Series, RD[ ]E Series, and RD[ ]F Series. In RD[ ]JS Series, where the junction area is small, the dynamic impedance is lower in the low current range and in RD[ ]F Series, where the junction area is large, the dynamic impedance is lower in the larger current range.

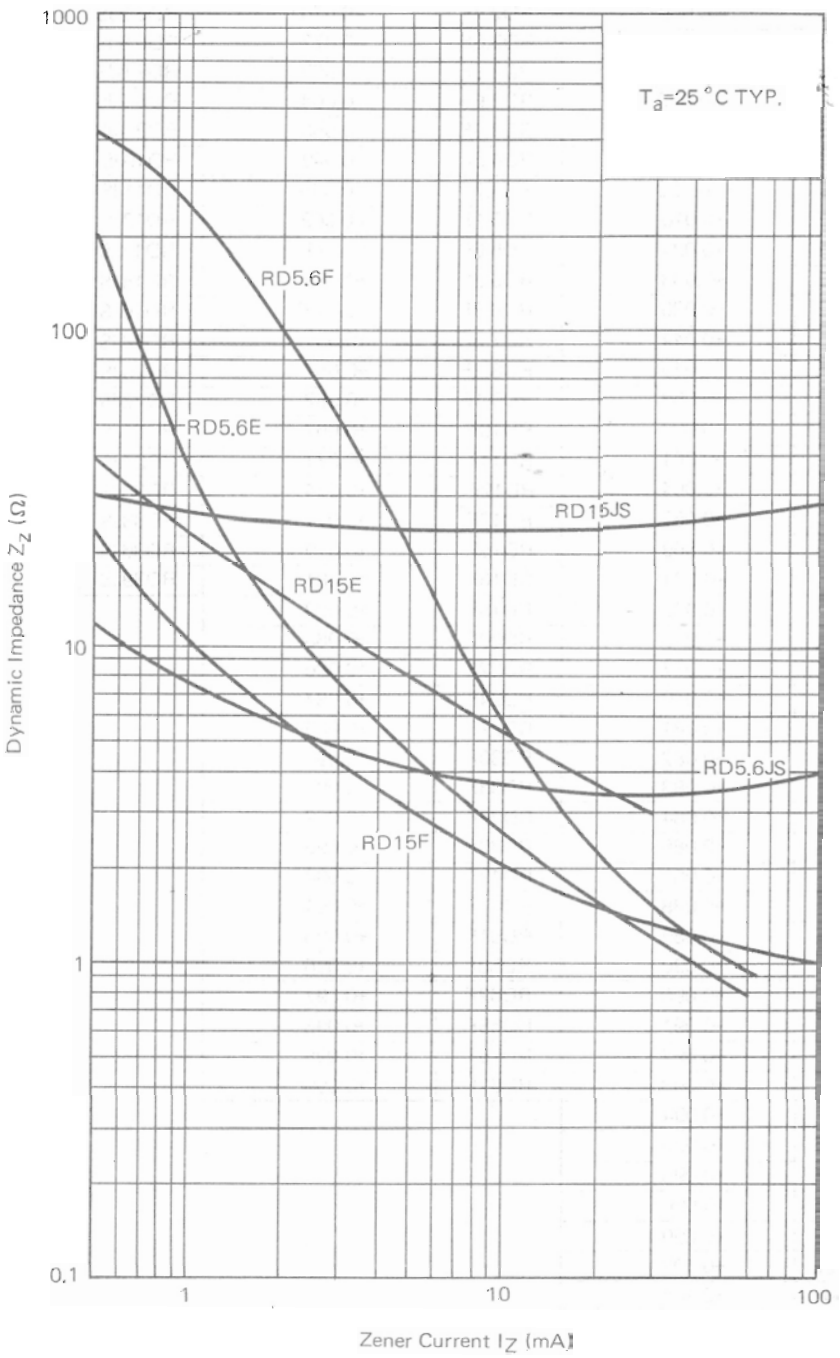


Fig. 7 Comparison of Z_Z-I_Z Characteristics

(iv) Reverse current (I_R)

In Fig. 8, comparison of Zener voltage vs. Zener Current (reverse current) characteristics among RD[ ] JS Series, RD[ ]E Series, and RD[ ]F Series are shown. On Zener voltages below 5 to 6 V in RD[ ] JS Series, the V_Z-I_Z characteristics are obviously sharp in comparison with those in RD[ ]E Series and RD[ ]F Series.

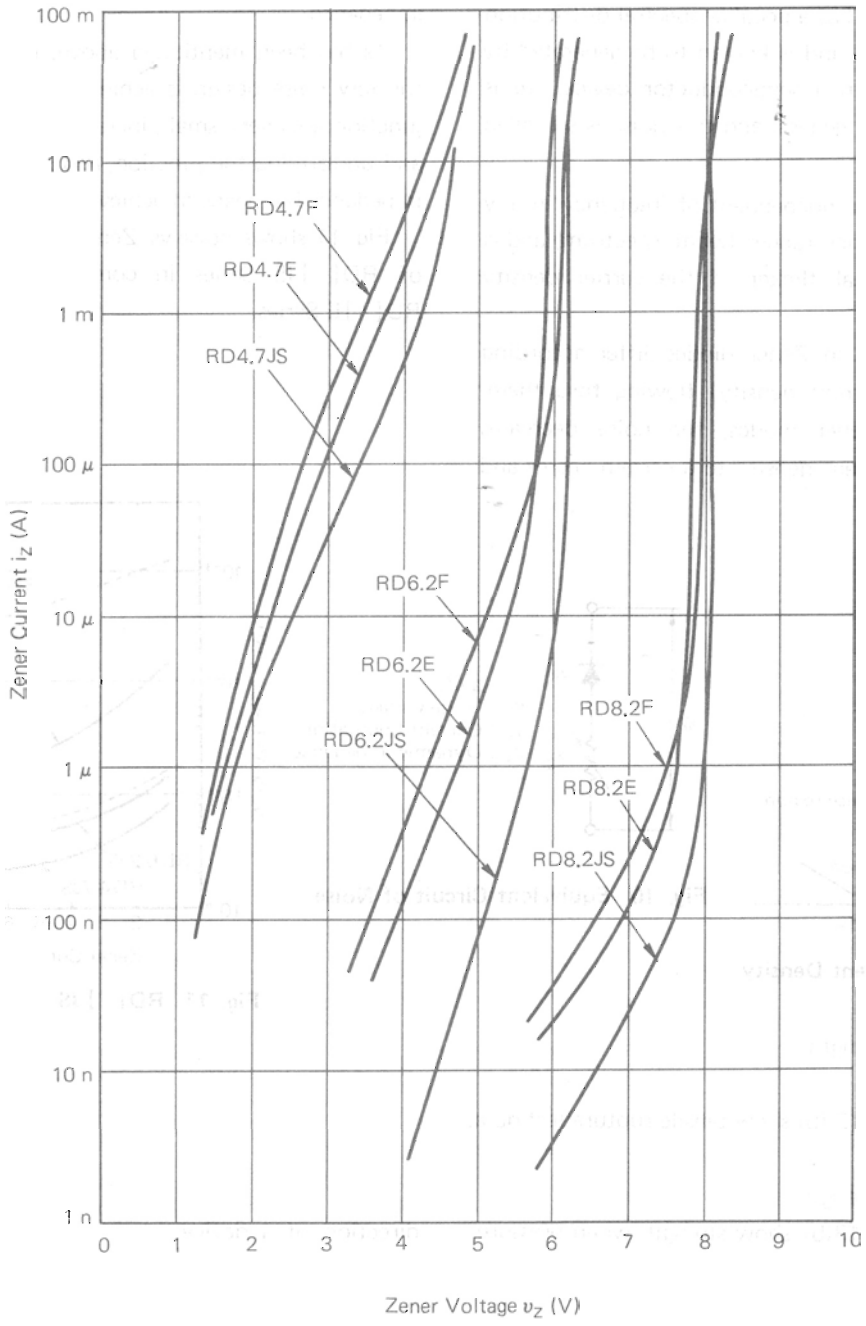


Fig. 8 Comparison of V_Z-I_Z(I_R) Characteristics

(v) Noise

Noises occurring in semiconductor devices are generally divided into the thermal noise, flicker noise, and shot noise.

The thermal noise occurs in all semiconductors and is generated by irregular motion of the carrier.

The flicker noise has a peculiar spectral distribution proportional to $1/f\alpha$ and is known to be generated by the surface effect in a semiconductor device. (α is nearly equal to 1 in general and this noise is so called "1/f noise".]

The shot noise is independent of frequency in low and medium frequency ranges (white spectrum) and is caused by the local flicker of the carrier density in a junction.

Types of noises in Zener diodes differ according to the current (current density) flowing thru them. Generally, with Zener diodes, the noise decreases with increasing current density to a certain degree and with still higher current density, it goes into the thermal noise region and is increased as shown in Fig. 9. Noises of Zener diodes can be considered as those of an equivalent circuit shown in Fig. 10 which indicates that Noise e_n is the function of the dynamic impedance.

As has been mentioned above, in RD[ ]JS Series, the low noise design is achieved by making the main junction area very small, increasing the current density, and uniforming the junction, and by reducing dynamic impedance by means of achieving high dope.

Fig. 11 shows noise vs. Zener current characteristics of RD[ ]JS Series in comparison with those of RD[ ]E Series.

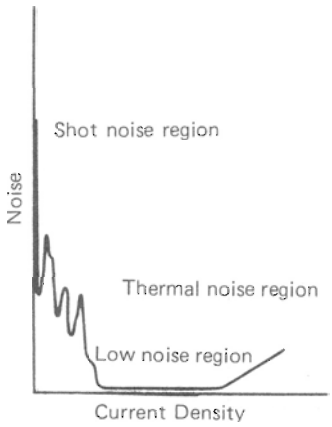


Fig. 9 Noise-Current Density

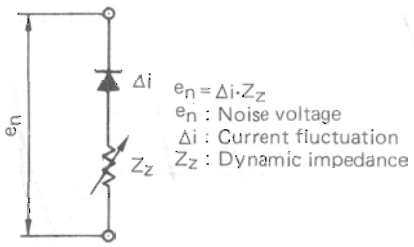


Fig. 10 Equivalent Circuit of Noise

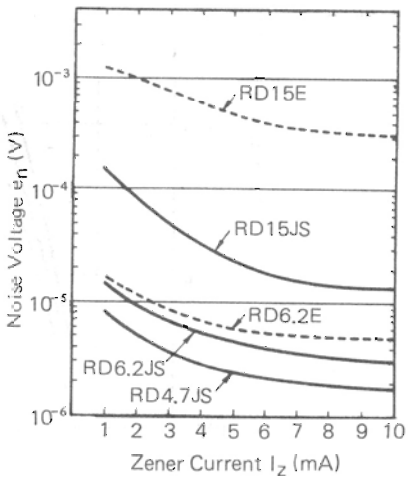


Fig. 11 RD[ ]JS Noise Characteristics

(vi) Mechanical strength

(a) Tensile strength

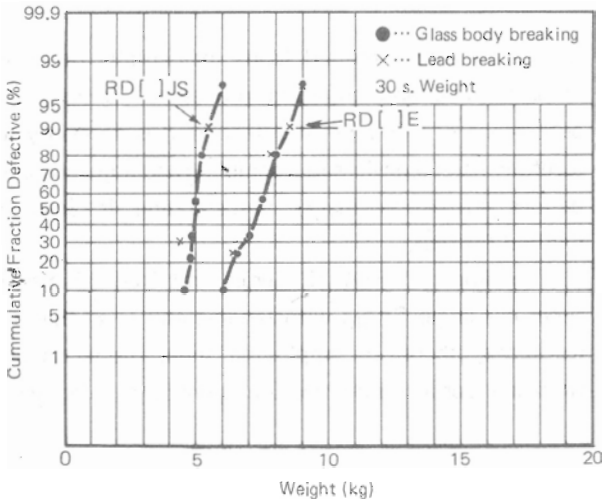
Figs. 12 (a) and 12 (b) show tensile rupture test data.

(b) Compressive strength

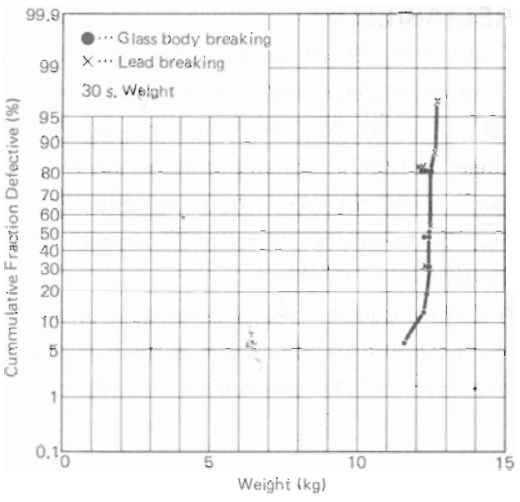
Figs. 13(a) and 13(b) show strength when pressure is applied in a direction perpendicular to the axial direction of a device.

(vii) Overpower withstanding

Fig. 14 shows results of breaking tests with RD[ ]E Series when step power is applied for a time longer than 10 ms. Surge reverse power ratings for short time, 10 μs to 10 ms have already been explained. For RD[ ]E Series, breaking is caused by power four times (ℓ=10 mm) and six times (ℓ=5 mm) the rating. This shows that the ratings have sufficient margins.

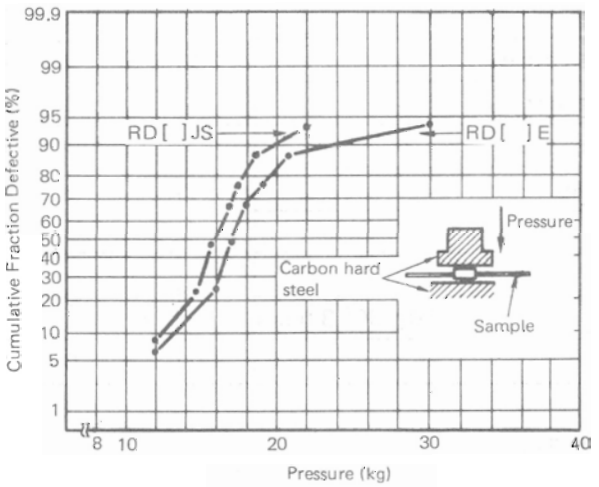


(a) RD[ ]E, RD[ ]JS

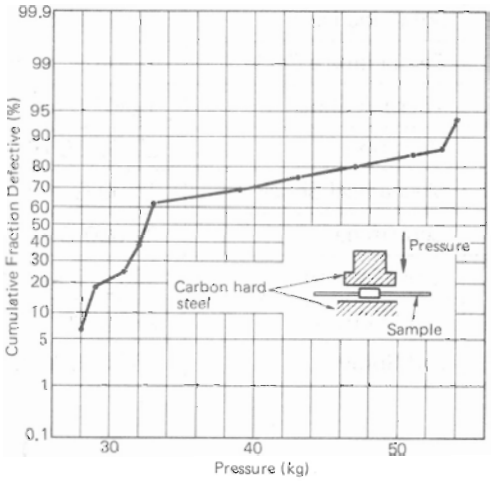


(b) RD[ ]F

Fig. 12 Lead Tension Rupture Distribution (Example)



(a) RD[ ]E, RD[ ]JS



(b) RD[ ]F

Fig. 13 Body Pressure Rupture Distribution (Example)

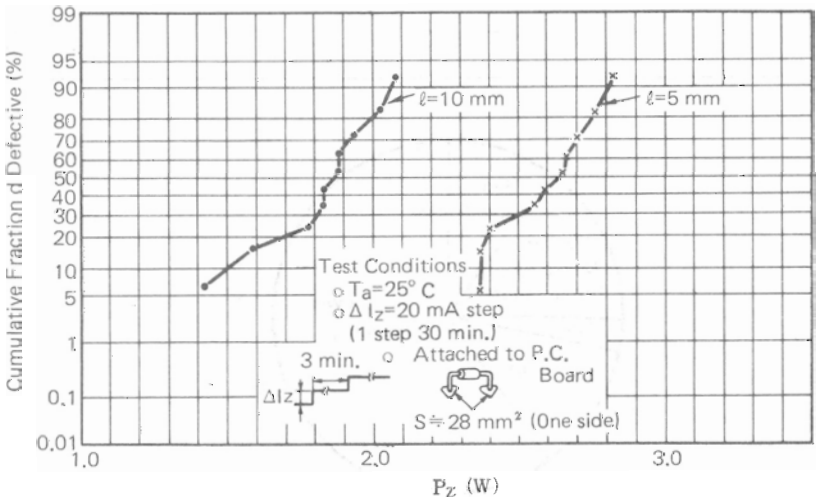


Fig. 14 DC Reverse Power Rupture Distribution (RD[ ]E Example)

4. RELIABILITY

Tables 8 and 9 list results of the reliability test for DHD structure Zener diodes. High reliability of diodes in RD[ ]E Series, RD[ ]F Series, and RD[ ]JS Series has been proved in communications, civil, and light industries since they were introduced in the market.

Fig. 15 shows the defective occurrence index of the Zener diodes in fields.

A Zener diode has greater percentage of overpower breaking because its impedance is small in the breakdown region and the defective is that of short circuit caused by short-circuited loads incidentally occuring in assembling and adjusting processes. To decrease occurrence of this type of defective, it is necessary to carefully handle devices in assembling and adjusting and besides increasing P_{RSM} withstanding is another method for that.

The diode of RD[ ]E Series and RD[ ]F Series types has larger P_{RSM} withstanding and small thermal resistance, therefore employing these diodes is advantageous as a countermeasure against this defective.

Table 8 Environmental Test

Item		Conditions			Samples	Failure
		RD[ ]JS Series	RD[ ]E Series	RD[ ]F Series	n	c
1	Soldering Heat	T_S=260 °C, 10 s			11	0
	Temperature Cycle	T_a=−65 °C to +175 °C, 5 cycles				
	Thermal Shock	T_a=0 °C to +100 °C, 5 cycles				
2	Vibration	20 G, 60 H_Z, 1 H			11	0
	Mechanical Shock	1 500 G, 0.5 ms 5 times				
	Centrifuge	20 000 G, 1 min.				
3	Lead Tention	450 g, 30 s			11	0
	Lead Fatigue	227 g, 90 °, 3 times		450 g, 90°, 3 times		
4	Salt Spray	35 °C, 5 %, 96 H			11	0

Table 9 Life Test

Item	Conditions (1 000 H)			Samples	Failure
	RD[ ]JS Series	RD[ ]E Series	RD[ ]F Series	n	c
Operating Life	P=400 mW	P=500 mW	P=1 W	22	0
High Temperature Life	T_a=175 °C			22	0

Fig. 15 Modes of Defective Obtained from Field (Jan. thru Nov. 1981)

5. APPLICATION

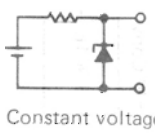
Table 10 lists uses and current ranges of Zener diodes. RD[ ]E Series and RD[ ]F Series feature great surge power and small size and light weight and they are suitable for constant-voltage, constant-current power sources, clipper, limiter, slicer, fixed bias level shift, and surge absorption circuits. For low level (I_Z=1 to 100 μA) constant-voltage, constant-current circuits, level shift circuits, and high impedance surge absorption circuits RD[ ]JS Series is optimum. You are, however, requested to consult us before designing circuits employing the diodes because sharpness of V_Z-I_Z characteristics, dispersion of Zener voltages on low levels, and stability of voltages vary with Zener voltages.

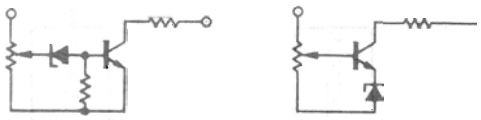
Table 10 Application Zener Diodes

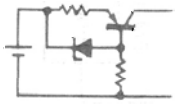
Application	RD[ ]JS		RD[ ]E		RD[ ]F	
	(*) Suitable	(**) Current Ranges	(*) Suitable	(**) Current Ranges	(*) Suitable	(**) Current Ranges
Constant Voltage	◎	10 μA~I_Z MAX.	◎	10 μA~I_Z MAX.	◎	100 μA~I_Z MAX.
Constant Current	◎	10 μA~I_Z MAX.	◎	10 μA~I_Z MAX.	◎	100 μA~I_Z MAX.
Waveform Clipper Limiter Slicer	○	0~I_Z MAX.	◎	0~I_Z MAX.	◎	0~I_Z MAX.
Level Shift	◎	0~I_Z MAX.	Δ	0~I_Z MAX.	Δ	0~I_Z MAX.
Fixed Bias Level Shift	◎	10 μA I_Z MAX.	◎	10 μA~I_Z MAX.	◎	100 μA~I_Z MAX.
Surge Clipper	Δ	0~I_{SM}	◎	0~I_{SM}	◎	0~I_{SM}

Notes: (*) ◎ Very suitable
○ Suitable
Δ Please consult up when using

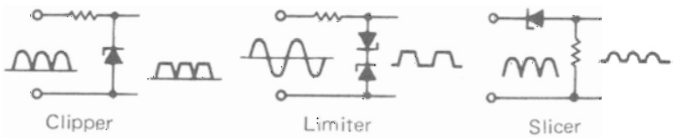
Examples of Circuits

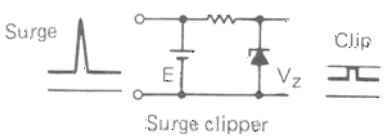

Constant voltage


Level shift


Constant current

Fixed bias level shift

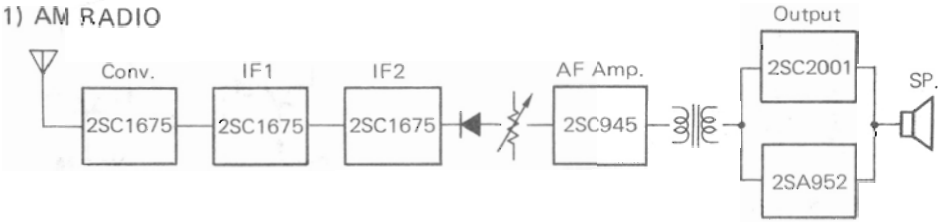


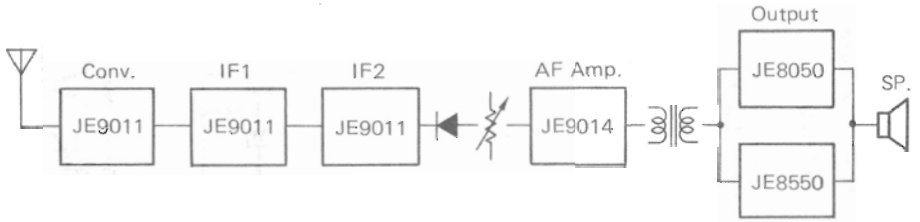


BLOCK DIAGRAM FOR ENTERTAINMENT EQUIPMENT

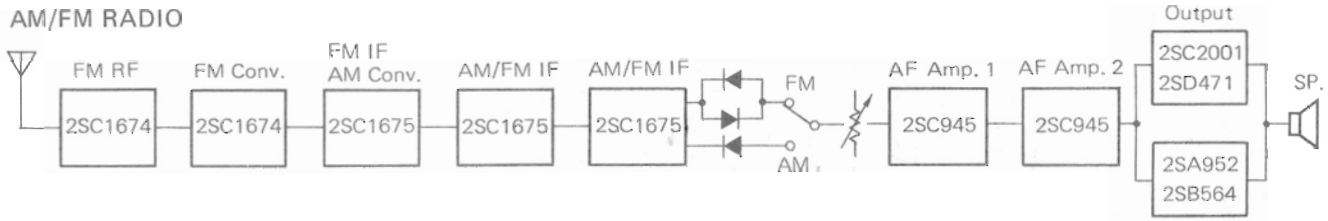
1. RADIO RECEIVER

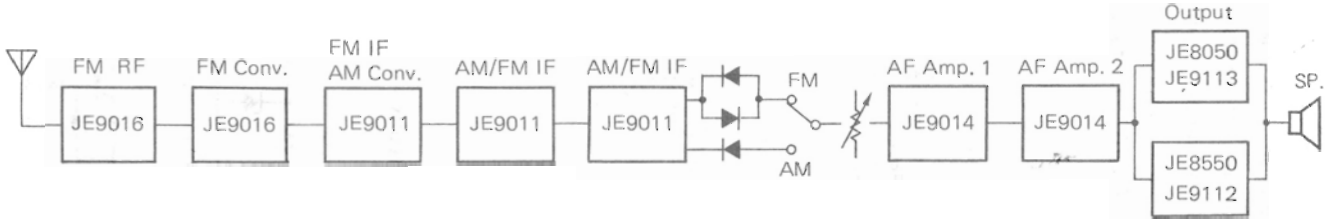
1) AM RADIO



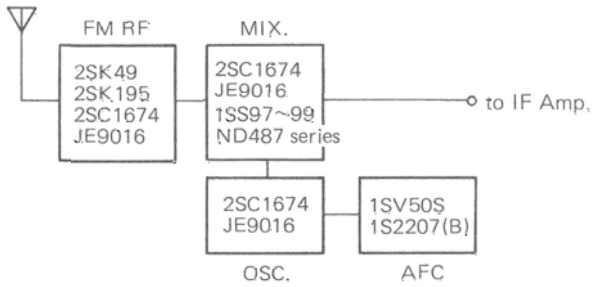


2) AM/FM RADIO

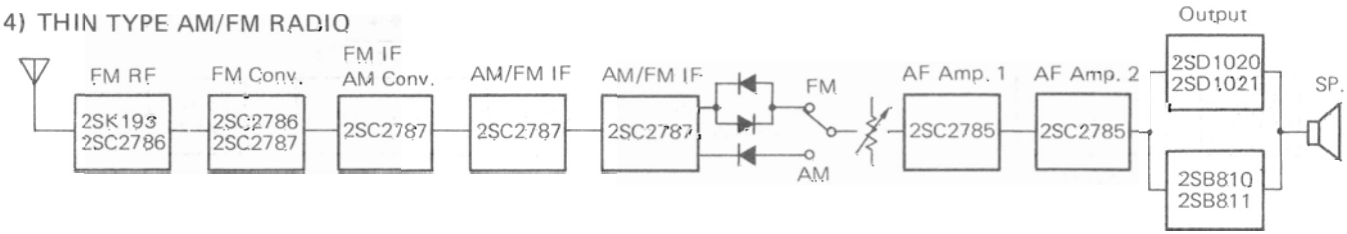




3) FM TUNER

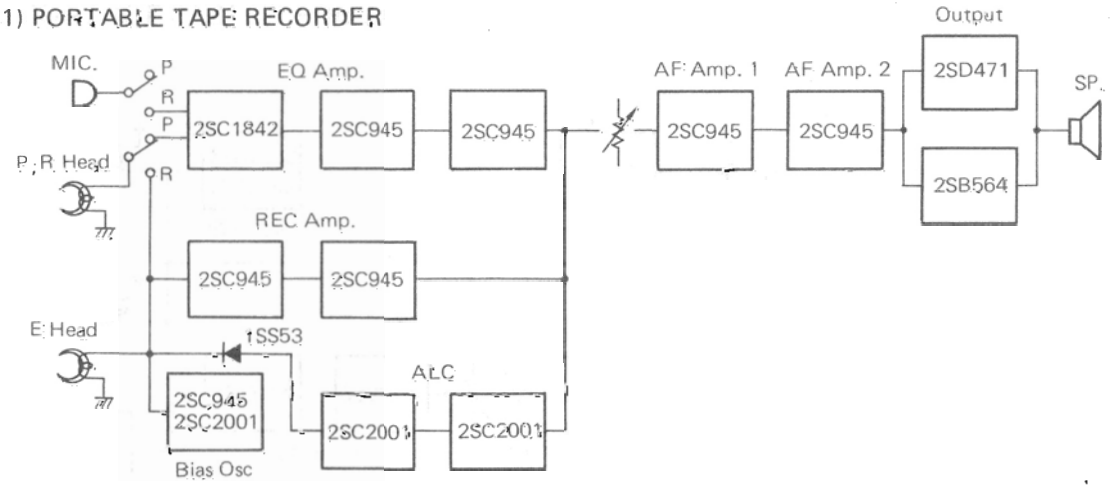


4) THIN TYPE AM/FM RADIO

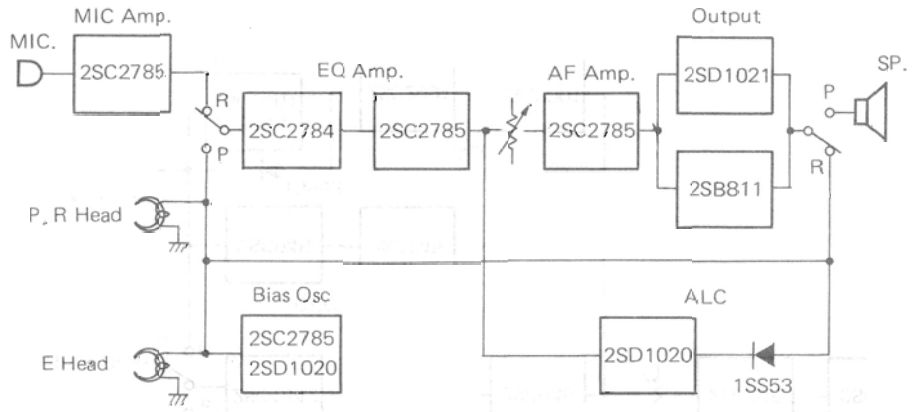


2. TAPE RECORDER

1) PORTABLE TAPE RECORDER



2) MICRO/MINI CASSETTE TAPE RECORDER

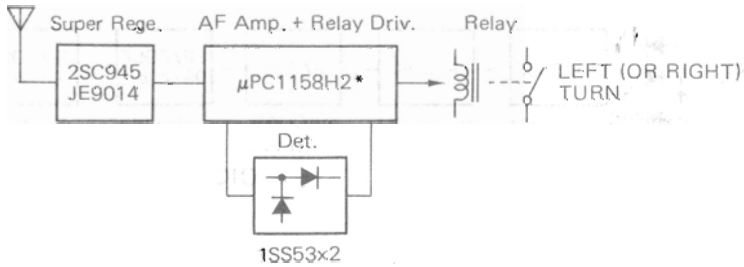


3. RADIO CONTROL SYSTEM FOR TOYS

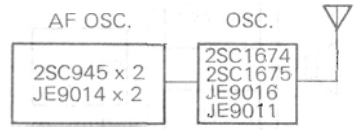
(*Marks: Please refer to another catalogue)

1) LOW END LEFT (OR RIGHT) TURNING CONTROL TYPE

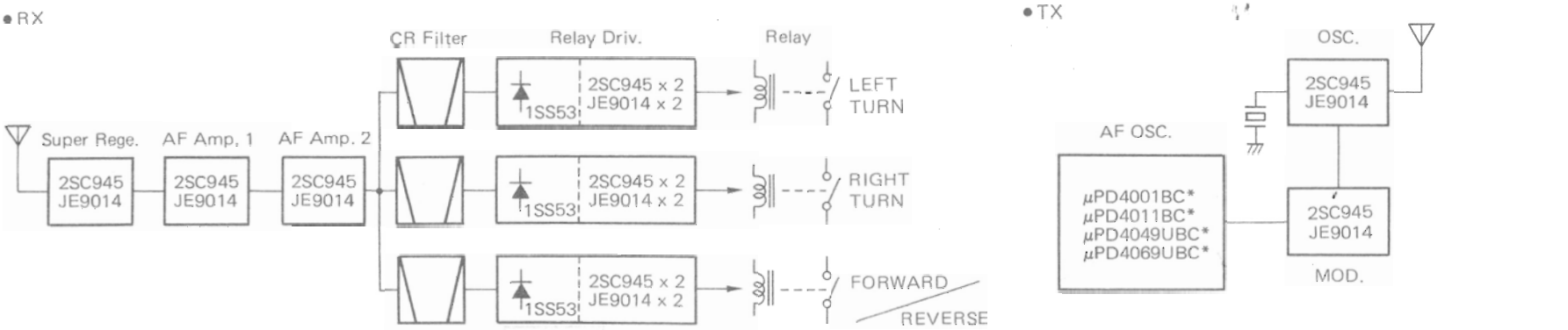
• RX (RECEIVER)



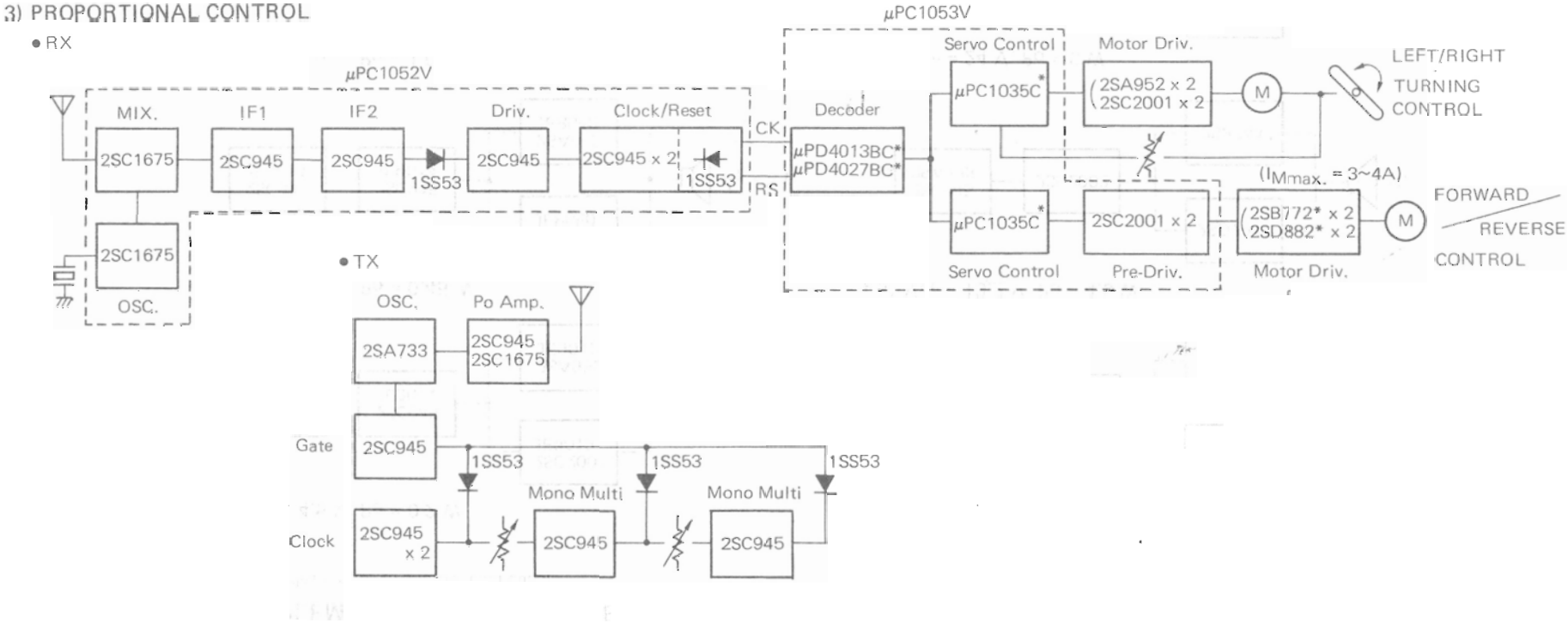
• TX (TRANSMITTER)



2) LEFT/RIGHT & FORWARD/REVERSE CONTROL TYPE



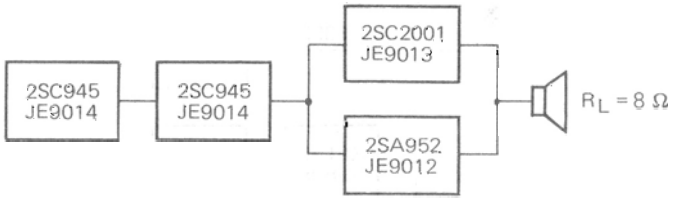
3) PROPORTIONAL CONTROL



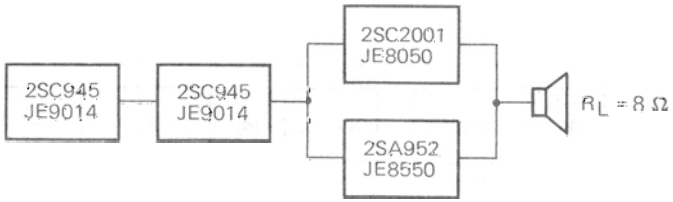
4. PURE COMPLEMENTARY P-P AMPLIFIER

(*Marks: Please refer to another catalogue)

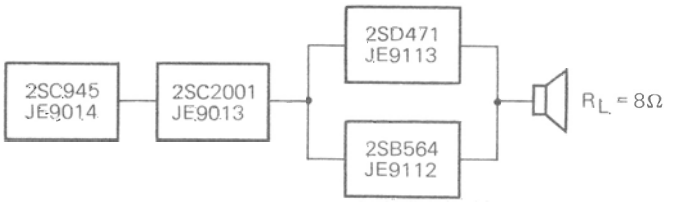
1) Vcc = 4.5 V, Po = 0.2 W



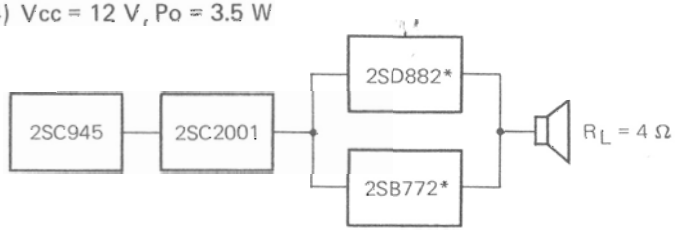
2) Vcc = 6.0 V, Po = 0.45 W



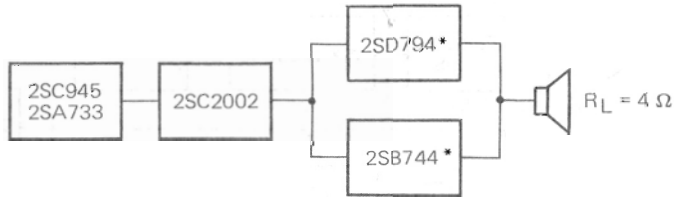
3) Vcc = 9.0 V, Po = 1.0 W



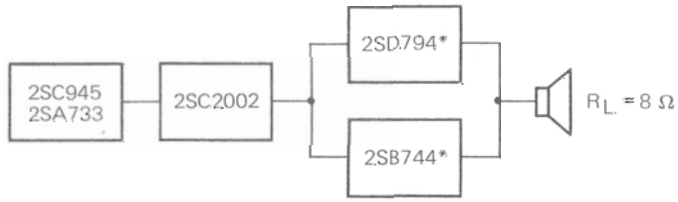
4) Vcc = 12 V, Po = 3.5 W



5) Vcc = 13.2 V, Po = 4.5 W



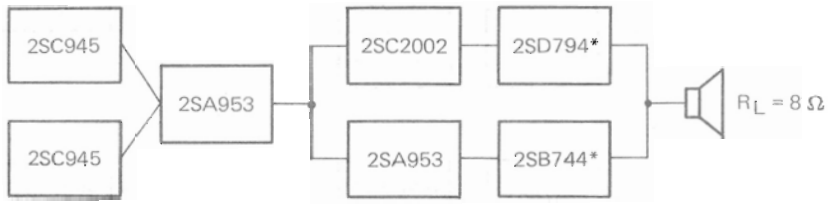
6) Vcc = 24 V, Po = 6 W



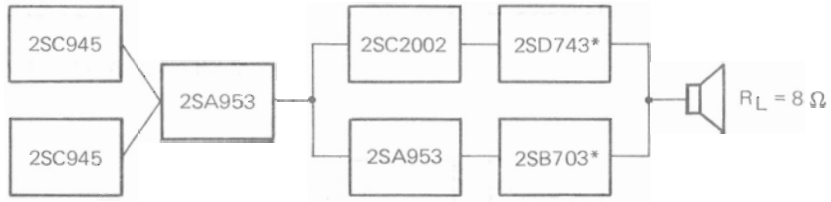
5. PURE COMPLEMENTARY DARLINGTON SEPP AMPLIFIER

(*Marks: Please refer to another catalogue)

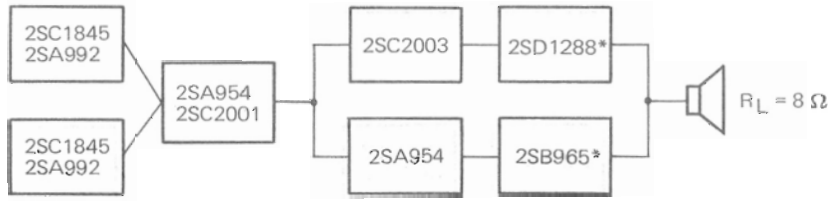
1) Vcc = 33 V, Po = 10 W



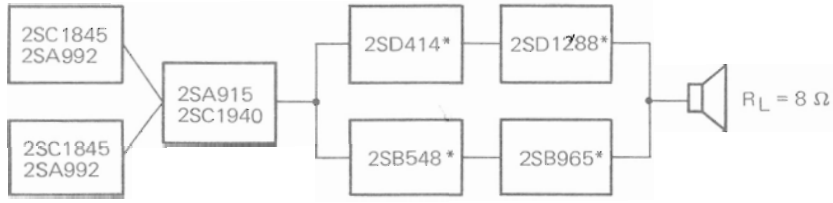
2) Vcc = 43 V, Po = 15 W

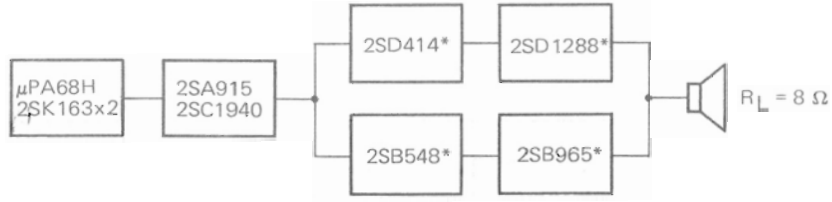


3) Vcc = ±25 V, Po = 25 W

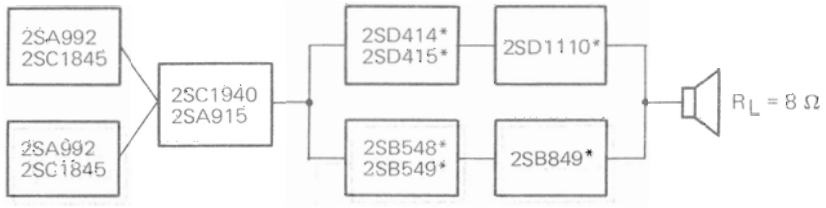


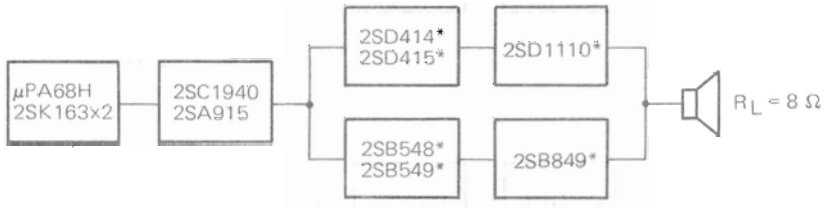
4) Vcc = ±32 V, Po = 35 W



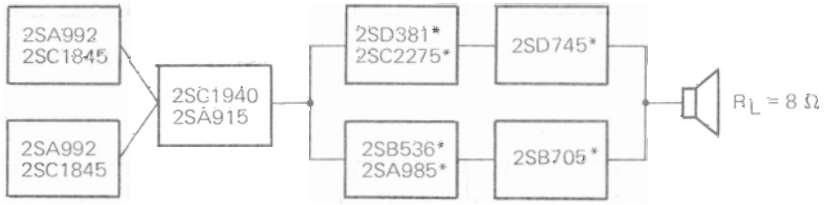


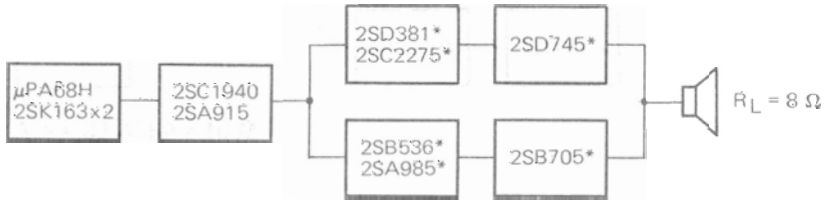
5) Vcc = ±37 V, Po = 45 W



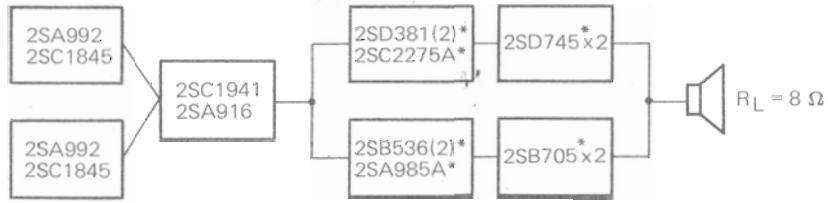


6) Vcc = ±41V, Po = 60 W

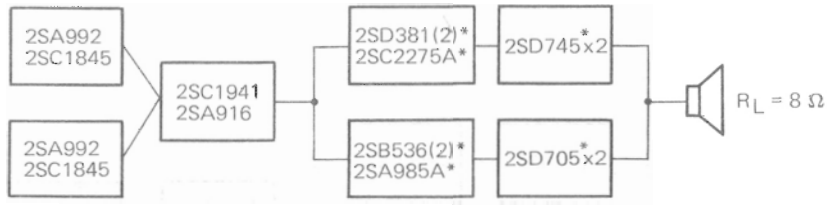




7) Vcc = ±47 V, Po = 80 W



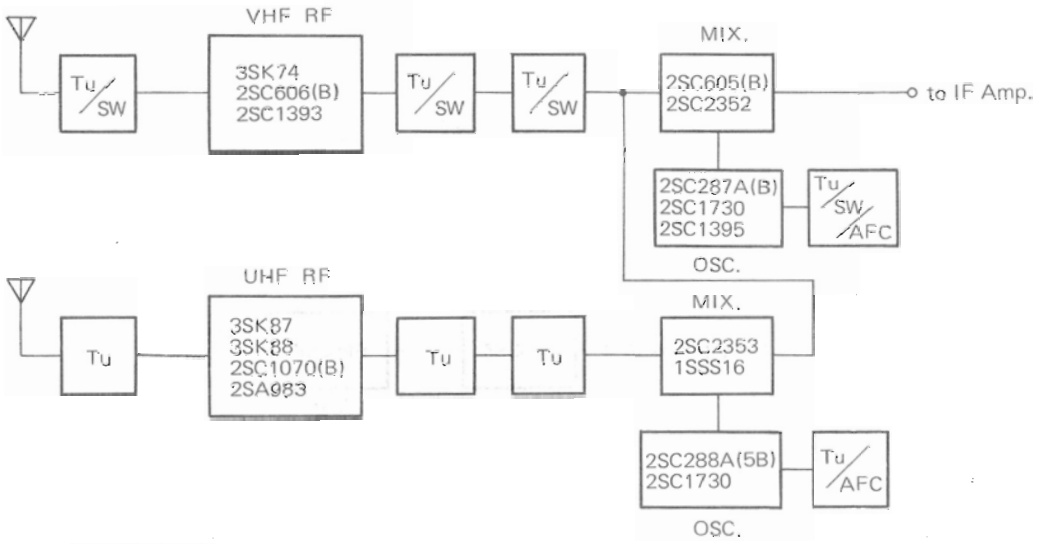
8) Vcc = ±53 V, Po = 100 W



6. VHF/UHF TV SET

(*Marks: Please refer to another catalog)

1) VHF/UHF ELECTRONIC TUNER

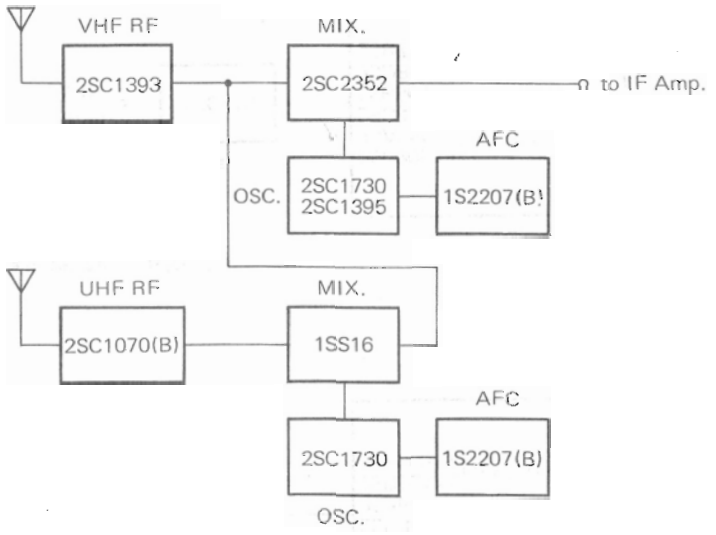


Tu; Tuning Di { VHF: 1SV50, 1SV50(1), 1S2209(B) / UHF: 1S2208(B)

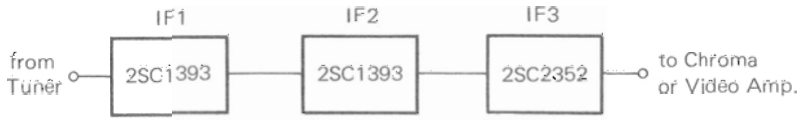
SW; SW Di : 1S2222, 1SS103

AFC Di : 1S2207(B)

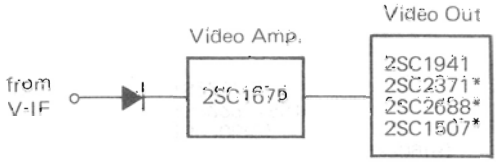
2) LOW END VHF/UHF MECHANICAL TUNER



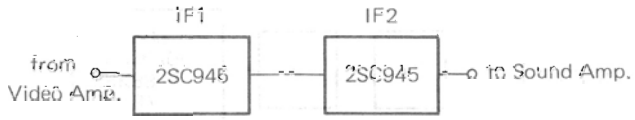
3) VIDEO IF Amp.



4) VIDEO Amp. (B/W)

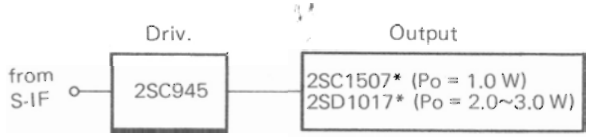


5) SOUND IF Amp.

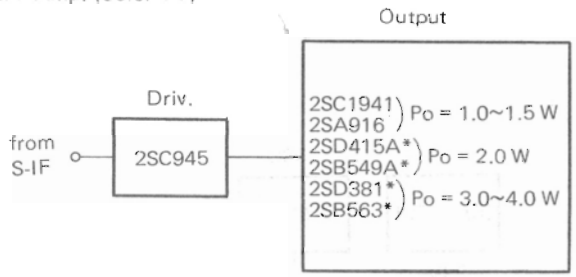


6) SOUND Amp.

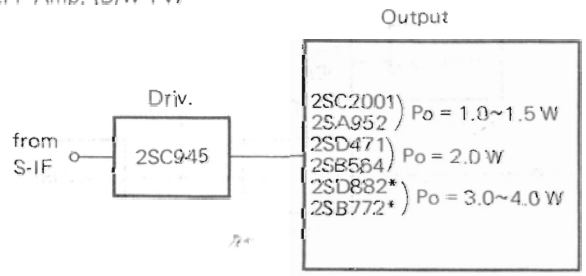
- A-CLASS Amp. (Color TV)



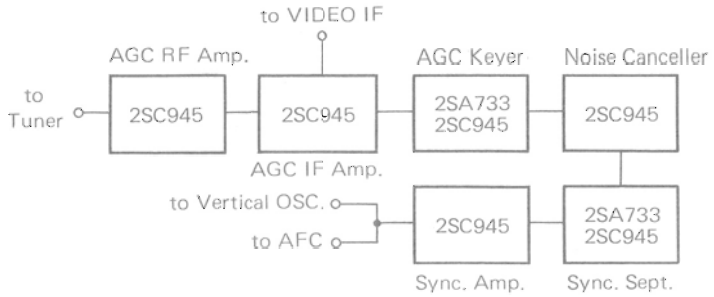
- SEPP Amp. (Color TV)



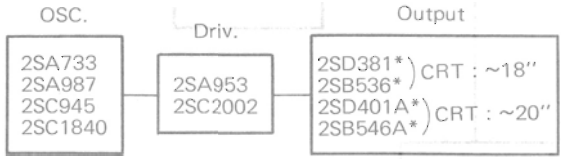
- SEPP Amp. (B/W TV)



7) AGC, SYNCHRONIZATION

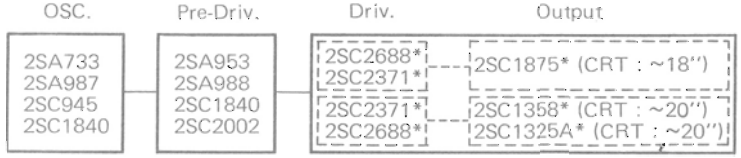


8) VERTICAL DEFLECTION

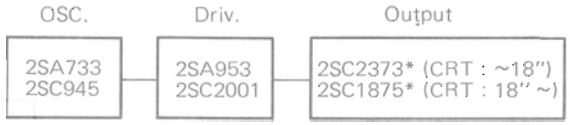


9) HOLIZONTAL DEFLECTION

• Color TV

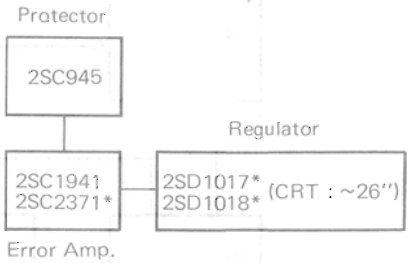


• B/W TV

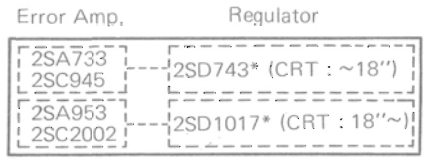


10) POWER SUPPLY

• Color TV

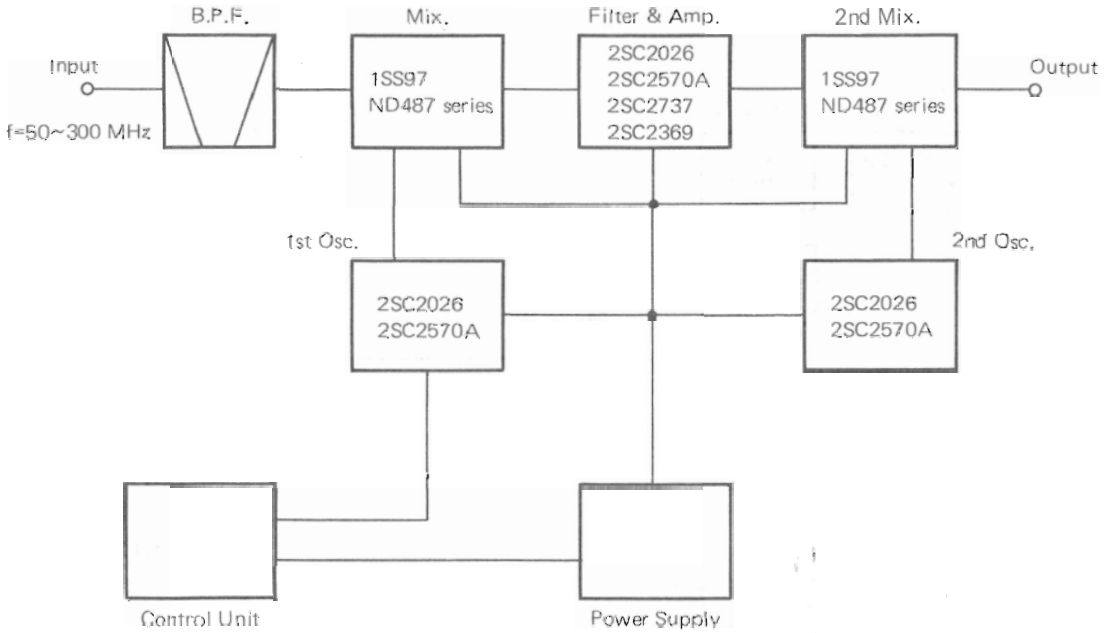


• B/W TV

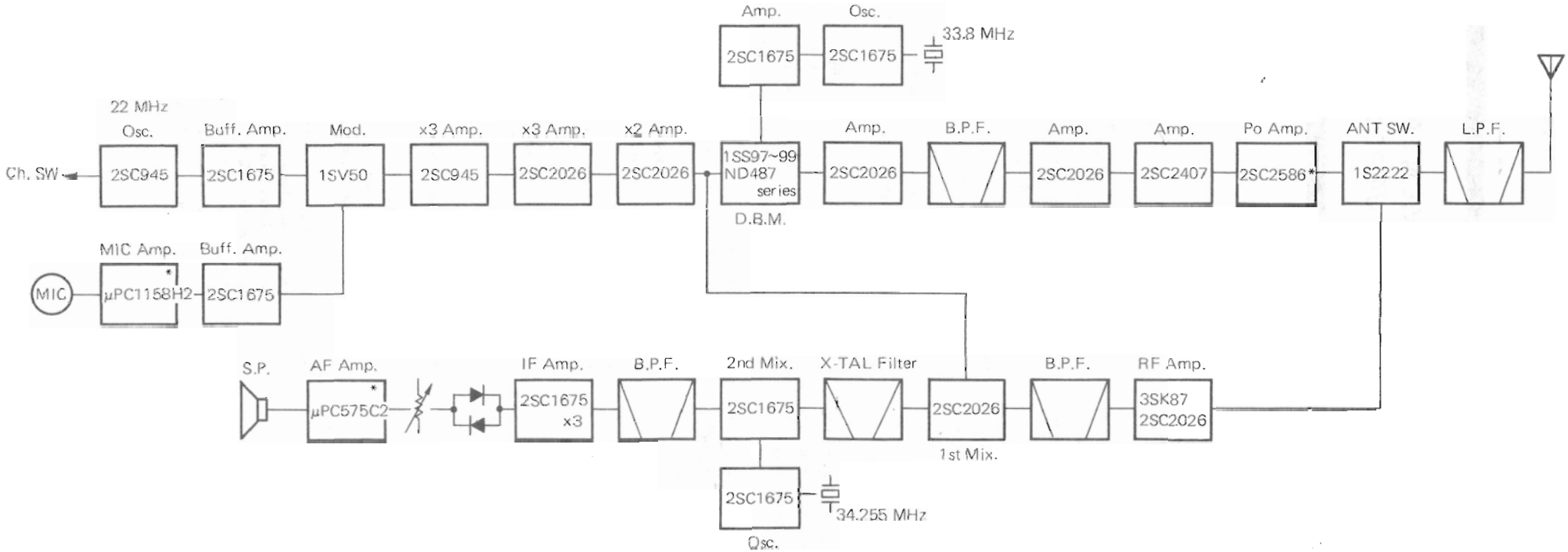


7. OTHER EQUIPMENT

1) CATV CONVERTER



2) HANDY TYPE TRANCSEIVER (430 MHz, P_O=1.0 W, V_{CC}=12 V)
(* Marks : Please refer to another catalogue.)



EXAMPLE OF Po=3 W PURE COMPLEMENTARY OTL AUDIO POWER AMPLIFIER CIRCUIT USING JE9000 SERIES

GENERAL

This paper describes an example of Po=3 W (maximum output) pure complementary OTL audio power amplifier using epitaxial silicon transistor JE9000 series. The amplifier is composed basically of the initial stage, driver stage, and the output stage in 3 stages. The first stage employs JE9014 (NPN), the driver stage employs JE9015 (PNP), and the output stage employs JE8550 (PNP)/JE8050 (NPN).

JE8550/JE8050 are complementary types having characteristics equivalent to each other, except that their polarity differs as PNP/NPN.

These transistors are TO-92 mold type. Since these transistors employ copper alloy for lead frames, their total loss "P_t" is large. In addition, their h_{FE} do not lower to a large current range, and their collector saturation voltages $V_{CE}(sat)$ is low owing to the chips designed for low-voltage large-current use. Accordingly, they can obtain a large output even when they are employed in a low-supply voltage amplifier.

It should be noted, however, that this circuit example is merely an experimental example, and accordingly, neither deviations nor temperature characteristics of parts have been fully examined.

CHARACTERISTICS

1. Supply voltage	: DC 14 V ~ 22 V (Reference voltage 18 V)
2. Load impedance	: R_L = 8 ohms
3. Maximum output	: Po = 3.0 W (@ f=1.0 kHz, T.H.D. ≦ 10 %)
4. Frequency range	: 100 Hz~20 kHz (–3 dB)
5. Total harmonic distortion	: T.H.D. ≦ 10 % (@ f = 1.0 kHz, Po = 3.0 W)
6. Voltage gain	: Avf ≧ 40 dB
7. Input impedance	: Rin ≧ 10 kΩ

CIRCUIT DESCRIPTION

Refer to Fig. 1.

Assuming that the maximum output be 3 W, the power gain in the output stage becomes about 16 dB ≃ 40 times. Accordingly, a driver output Po' of higher than 75 mW is enough. Let I_{C2} be the collector current of transistor Q_2 in the driver stage. Since Q_2 belongs to A class operation type;

$$Po' \simeq 1/8\ (2\ I_{c2} \cdot V_{cc}) \therefore I_{c2} \simeq 4Po'/Vcc\ (Vcc = 18\ V)$$

I_{c2} becomes 16.7 mA, $\therefore I_{c2} \simeq 17.7$ mA.

Collector current I_{c1} of transistor Q_1 in the initial stage is necessary to be five times the base current I_{B2} of Q_2.

$$I_{c1} \simeq 5I_{B2} = 5I_{c2}/h_{FE2(min)}$$

Assume $h_{FE2(min)} = 60$, and $I_{c1} \simeq 1.5$ mA.

It is necessary for reducing the crossover distortion to flow an idle current to transistors Q_3 and Q_4 in the output stage even when no signal enters.

A suitable idle current is about 2 ~ 6 mA in JE8550/JE8050.

If this idle current is too high, it may cause thermal runaway when supply voltage increased. If it is too low, on the contrary, a crossover distortion may be produced to deteriorate the total harmonic distortion when the output is small.

If the idle currents to two B-class push-pull transistors differ from each other, one transistor having a lower idle current controls the crossover distortion. Accordingly, the idle current should be higher than 2 mA to this transistor.

In addition, since the other transistor having a higher idle current may cause thermal runaway, the idle current should not exceed 6 mA even in case of the transistor to which the higher idle current flows.

Note 1. The dispersion of idle current is almost determined by the dispersion of h_{FE} of Q_3 and Q_4. In this circuit constant, the idle current ranges within 2 ~ 6 mA at h_{FE} ranks B ~ D of Q_3 and Q_4. If the idle current is not within the above range, adjust R_7.

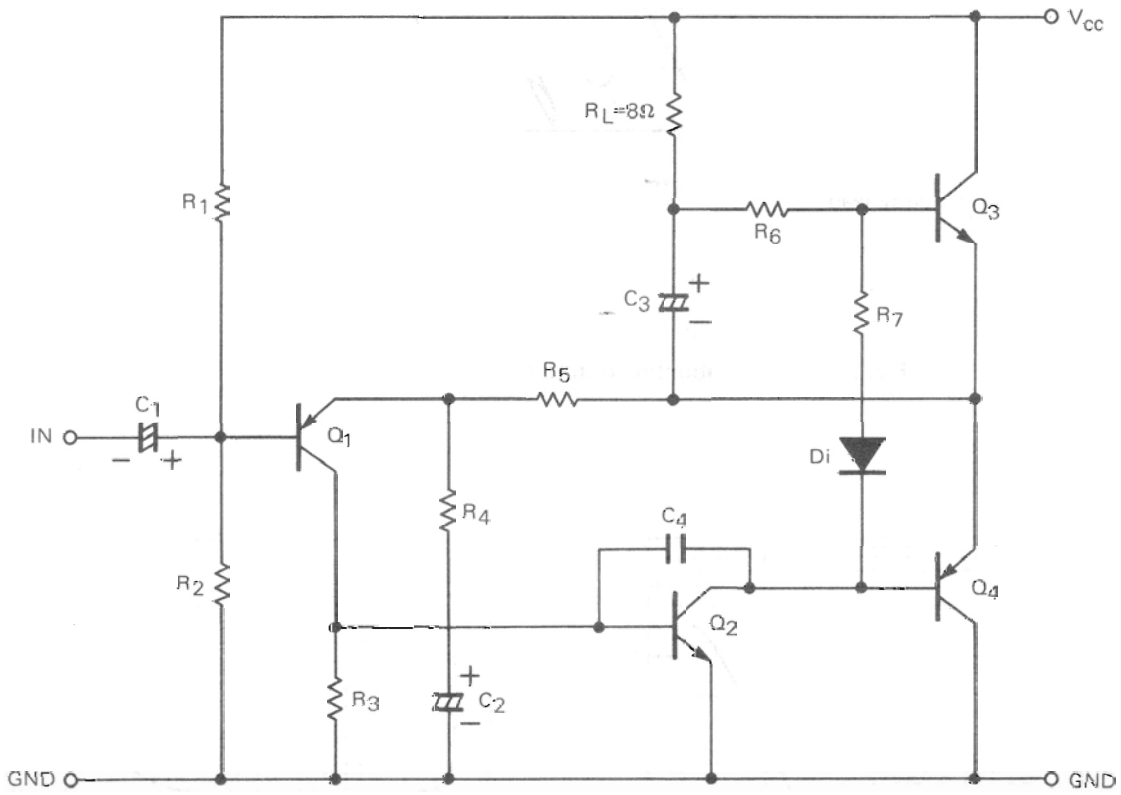
Note 2. It is necessary for obtaining the maximum output to set the neutral point potential to about 1/2 of Vcc. In this circuit example, the neutral point potential ranges within 1/2 Vcc ±5 % even when h_{FE} of Q_1 changes over a range of 60 to 1,000. If this neutral point potential is largely deviated from 1/2 Vcc, adjust R_1, and it can be placed within the specified value.

(When R_1 increases, the neutral point potential decreases. When R_1 decreases, the neutral point potential increases.)

It is necessary for transistors Q_3 and Q_4 in the output stage to mount an aluminum heat sink of exceeding 70 mm x 70 mm x 2 mm using the mounting fixture, respectively, as shown in Fig. 2.

It is recommended to apply grease to the heat sink to obtain a good radiation effect.

This mounting fixture may be substituted by a similar fixture or a radiation fin, since its dimensions are not strictly specified.



Q_1: JE9015	R_1: 56 kΩ	C_1: 2.2 μF
Q_2: JE9014	R_2: 33 kΩ	C_2: 220 μF
Q_3: JE8050	R_3: 470 Ω	C_3: 330 μF
Q_4: JE8550	R_4: 8.2 Ω	C_4: 15 pF
Di : VD1120 ~ VD1123	R_5: 1 kΩ	
	R_6: 470 Ω	
	R_7: 15 Ω	

Fig. 1 Circuit Diagram

Note 1. R_7: Resistor for adjusting idle current
Note 2. R_1 : Resistor for adjusting potential at neutral point.

For details of notes 1 and 2, refer to the text.

Transistors employed (h_{FE} rank)

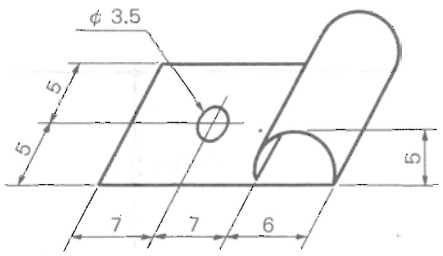
Q_1: JE9014 (A ~ D)　　Q_3: JE8050 (B ~ D)

Q_2: JE9015 (A ~ C)　　Q_4: JE8550 (B ~ D)

Currents when no signal enters.

Q_1: 1.5 mA　　Q_3: 2 ~ 6 mA

Q_2: 17.7 mA　　Q_4: 2 ~ 6 mA



Thickness t=0.5

Unit: mm

Material: Iron or copper alloy lead

Fig. 2 Heat sink mounting fixture (Radiation fin)

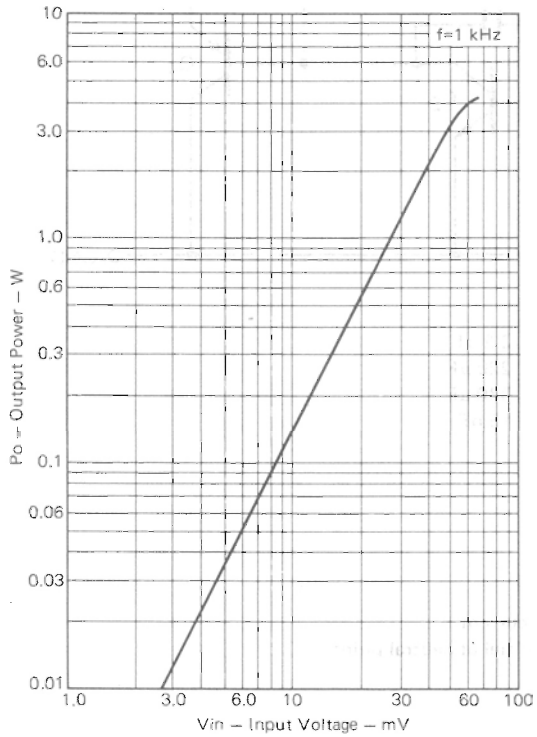


Fig. 3. Output Power vs. Input Voltage

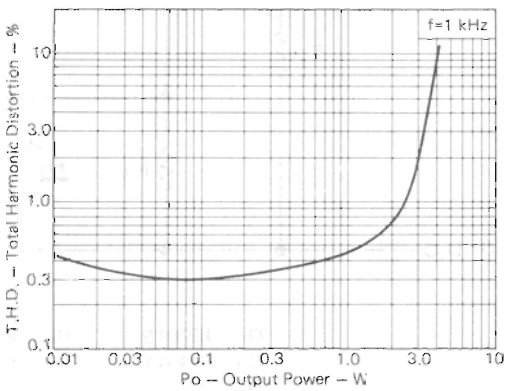


Fig. 4 Total Harmonic Distortion vs. Output Power

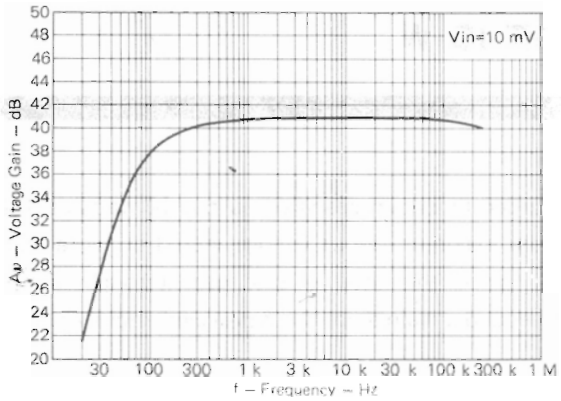


Fig. 5. Frequency Response

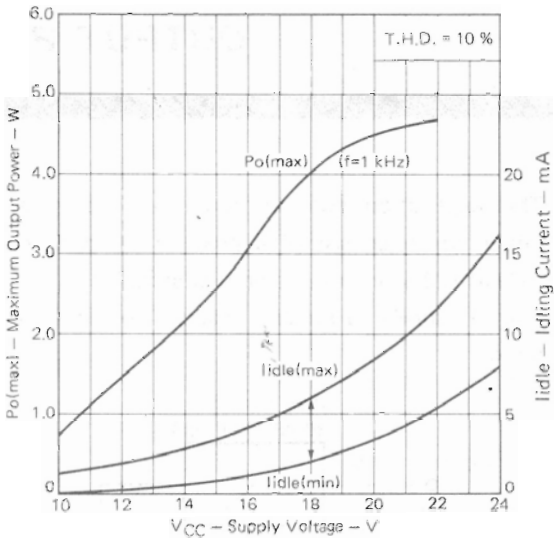


Fig. 6. Maximum Output Power and Idle Current vs. Supply Voltage

TYPICAL AUDIO AMPLIFIER WITH A CONTINUOUS OUTPUT POWER OF IO W

This application note introduses a 10 watt audio amplifier which consist of a preamplifier designed to operate at +22 V and main amplifier at ±22 V.

Fig. 1 shows a system diagram of the audio amplifier.

In order to obtain specified output 10 watts at 8 Ω load, the maximum input voltage should be more than 1.5 mV since the total voltage gain through a pre-amplifier and a main amplifier is designed about 76 dB.

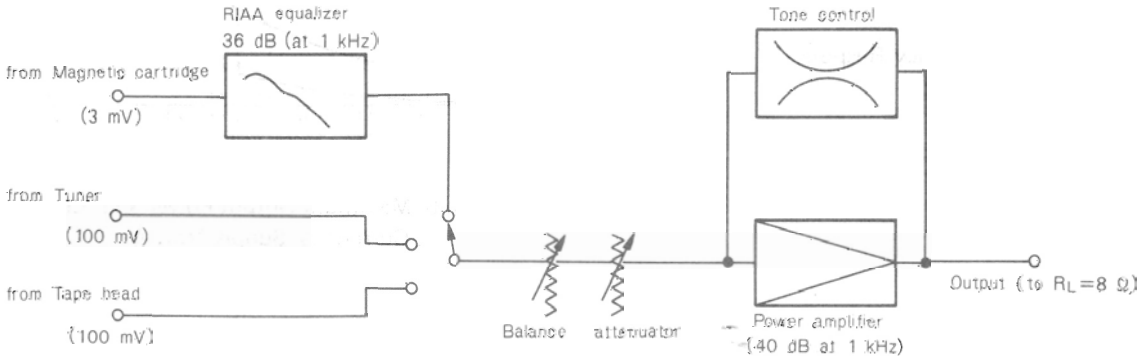


Fig. 1 System Diagram of a Audio Amplifier

1. PREAMPLIFIER

The RIAA equalization elements of C_5, C_6, R_9, R_{10} shown in Fig. 2 should be chosen the values of such time constant C_5R_9, C_5R_{10} and C_6R_{10} as 3 180 μs, 318 μs and 75 μs respectively so as to obtain the accurate RIAA equalization.

The ratio R_{10}/R_4 determines voltage gain in the medium frequency range, which is selected to give about 36 dB in this circuit. The capacitor C_2 connected between the base and the collector of transistor Q_1 is used to prevent parasitic oscillation. A 10 kΩ load resistor is used in the measurement of characteristics.

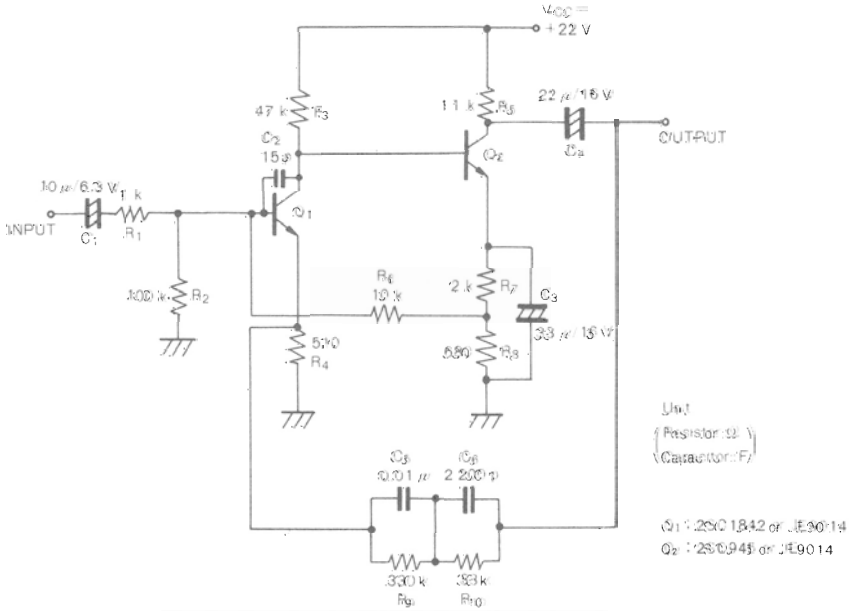


Fig. 2 Circuit of a RIAA Equalized Amplifier

1-1 Frequency Response Characteristics

Fig. 3 shows open loop frequency response and RIAA equalized curve. The voltage gain in medium frequency range is determined by the ratio R_{10}/R_4.

The values for R_4 and R_{10} are chosen to be 510 and 33 kΩ respectively to deliver 36.2 dB voltage gain.

The values for C_5, C_6, R_9 and R_{10} are also chosen as follows.

C_5=0.01 μF, C_6=2 200 pF, R_9=330 kΩ, R_{10}=33 kΩ

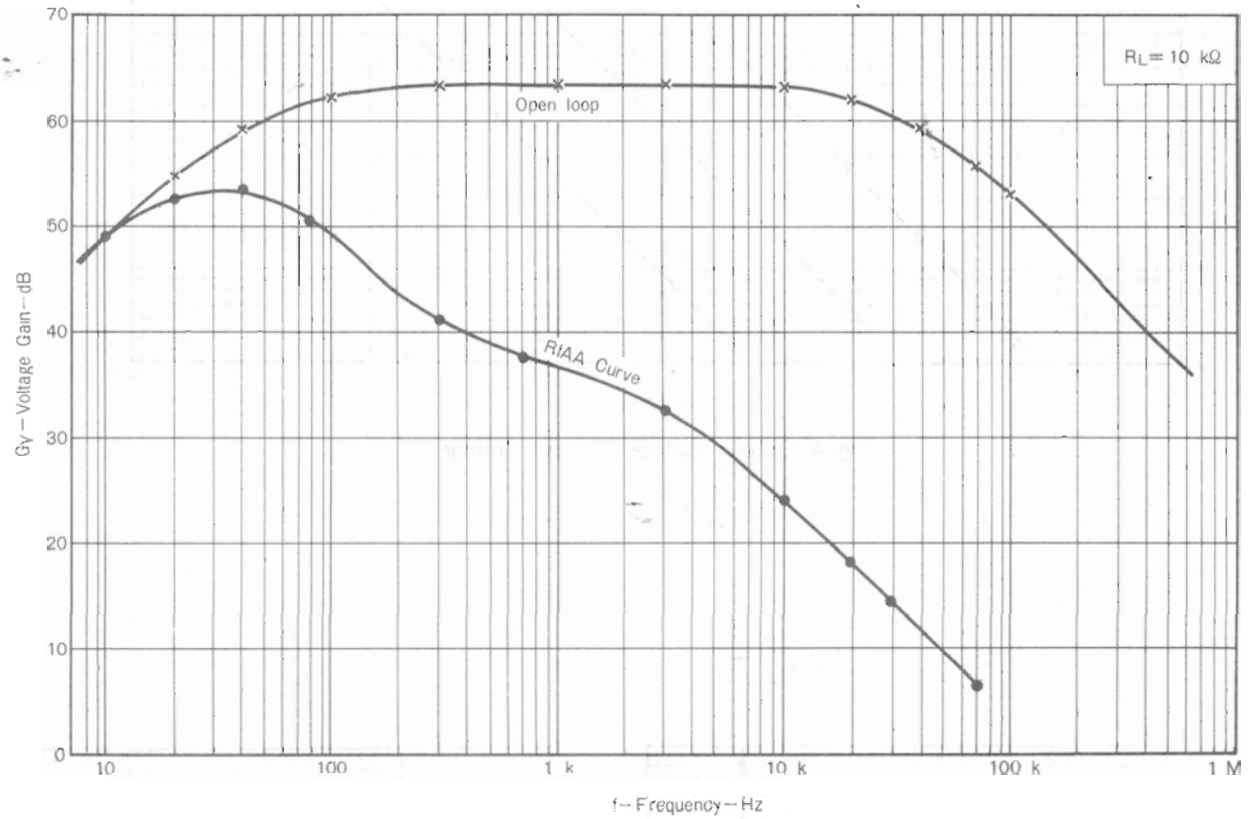


Fig. 3 Frequency Responce

1-2 Input vs. Output Voltage

Input vs. output voltage characteristics are shown in Fig. 4.

The maximum input voltage is about 60 mV.

1-3 Total Harmonic Distortion Characteristics

Fig. 5 and 6 show total harmonic distortion vs. output voltage. The harmonic distortion is minimised by negative feedback loop gain which is proportional to h_{FE} products of transistor Q_1 and Q_2. This indicates that the best way to give minimum distortion is to select the transistors whose h_{FE} ranking is the highest. In Fig. 5 and 6 the worst and typical characteristics are shown respectively.

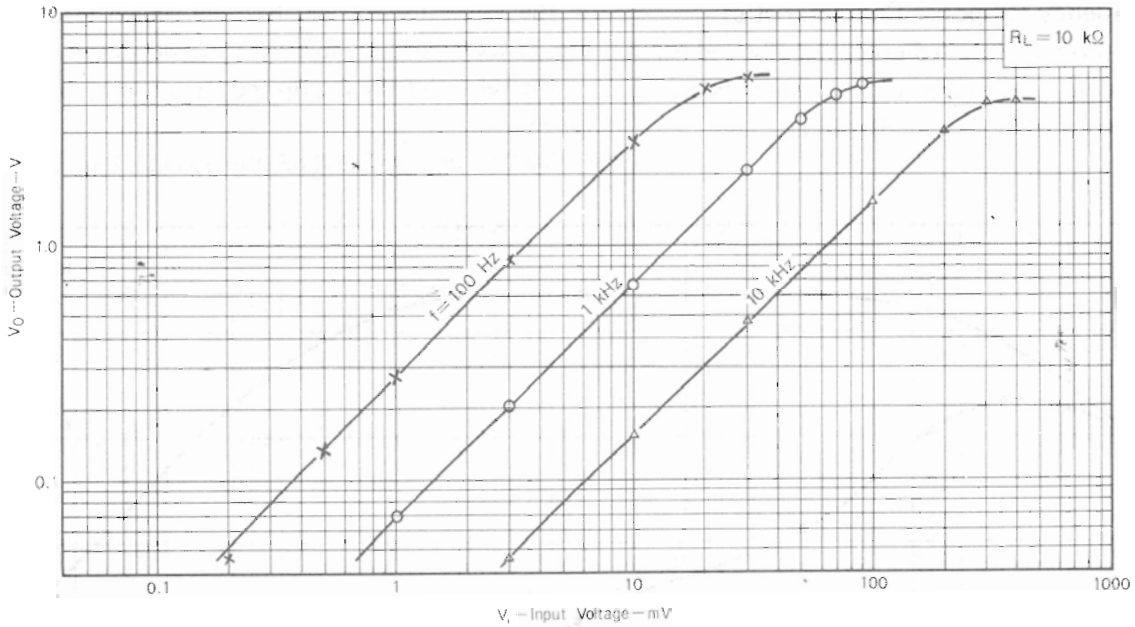


Fig. 4 Output Voltage vs. Input Voltage

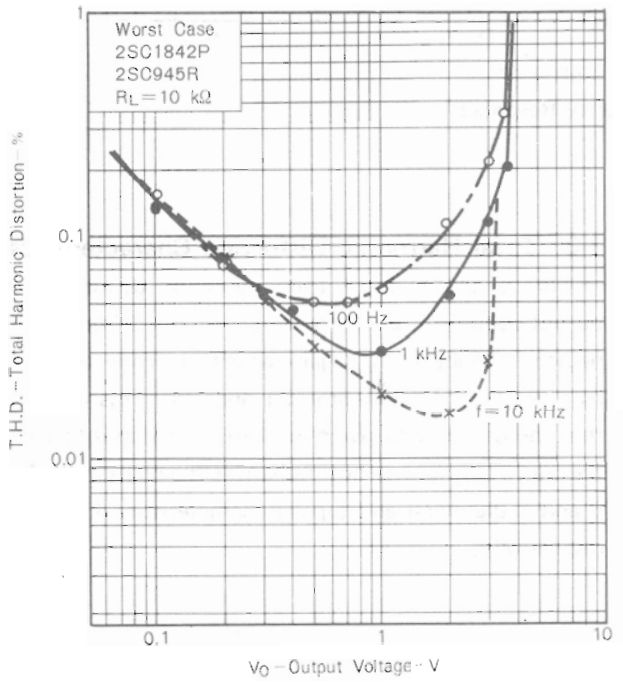


Fig. 5 Total Harmonic Distortion vs. Output Voltage

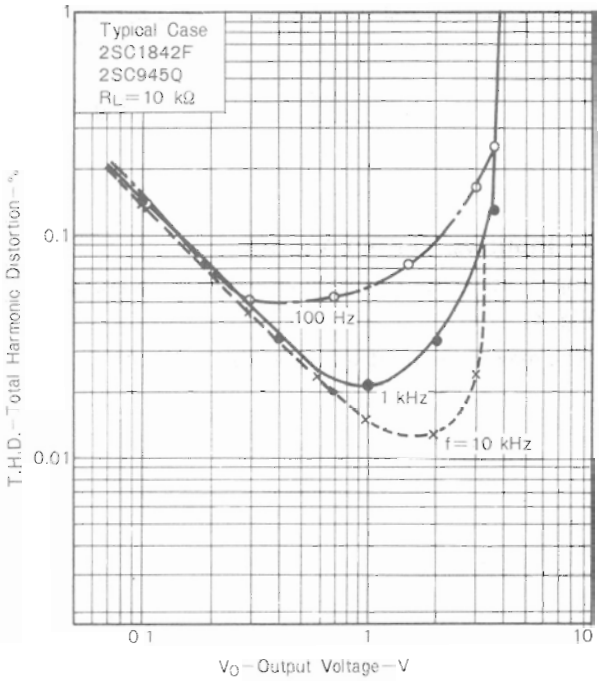


Fig. 6 Total Harmonic Distortion vs. Output Voltage

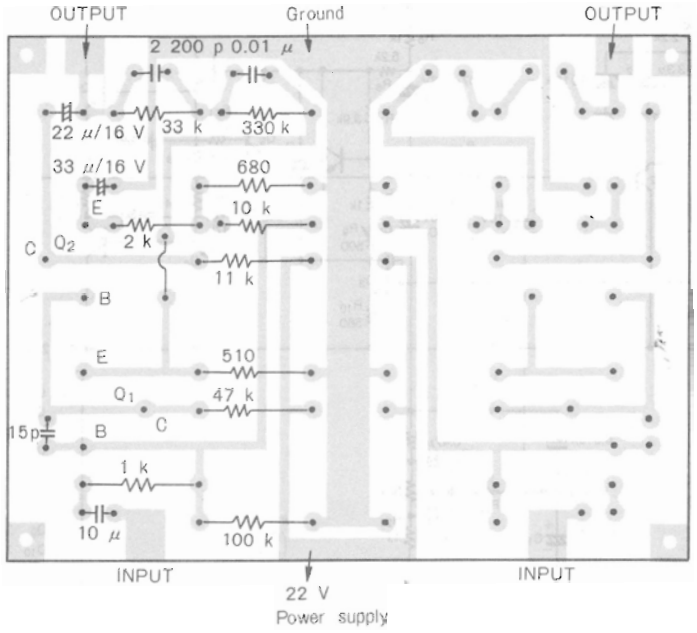


Fig. 7 P.C. Board of a Preamplifier

2. MAIN AMPLIFIER

As shown in Fig. 8, this circuit is designed to operate under a ±22 V power supply.

The output stage consists of a pure complementaly symmetrical circuit employing plastic power transistors which have excellent linearity of h_{FE} characteristics.

This output stage contributes to decrease harmonic distortion.

The optimum idling current which give minimum crossover distortion is designed to be 20 to 30 mA.

If the idling current is designed less than the value, crossover distortion increases when low input voltage is delivered. On the contraly, if the idling current is over the value, it causes unnecessary power consumption that may lead thermal runaway.

The idling current is adjustable with a potentiometer R_9 connected between the emitter and the base of transistor Q_4.

Current limitting circuit is contained in this amplifier.

When the current is overflown by irregular operations, resistors R_{15} and R_{16} are fully biased to turn on transistors Q_9 and Q_{10} so that all of the power transistors Q_5, Q_6, Q_7 and Q_8 are cutoff. And as the fuse is blown away by the irregular current, all of the power transistors are safely protected.

A power transistor should be bolted or clamped to an appropriate heat sink which may be fashioned 10 cm by 8 cm aluminum plate with 1.5 mm thickness.

2-1 Frequency Response Characteristics

Fig. 9 shows frequency response characteristics.

The circuit is designed to obtain about 72 dB voltage gain in medium frequency range at open loop, and 40 dB at closed loop. The negative feedback gain in medium frequency range is about 30 dB, and 20 dB at 10 kHz.

This means that the harmonic distortion in high frequency is worse than that in medium frequency range.

2-2 Frequency Response of Tone Control Circuit

Fig. 10 shows frequency response characteristics of tone control circuit.

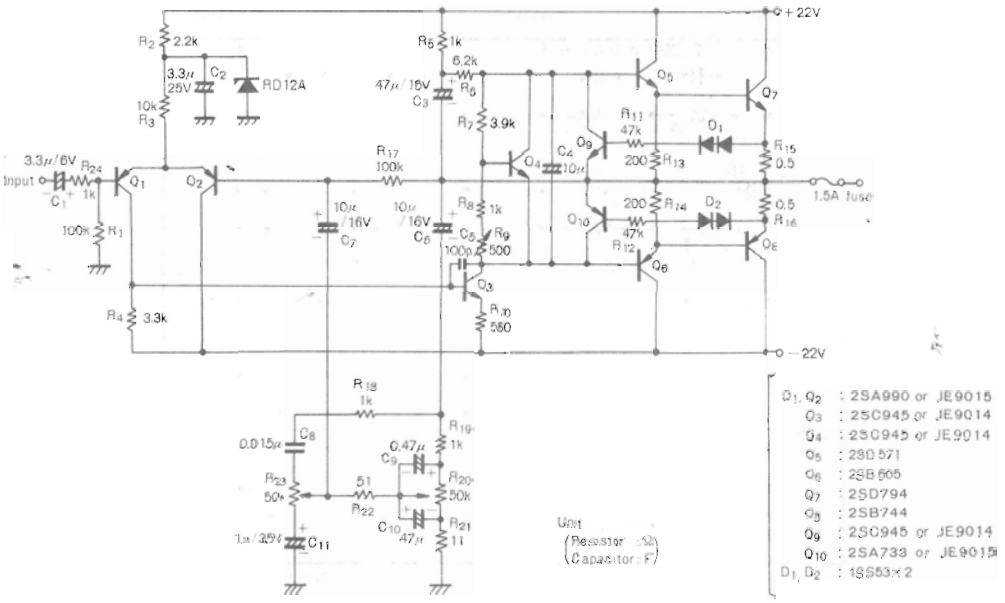


Fig. 8 Circuit of a Main Amplifier

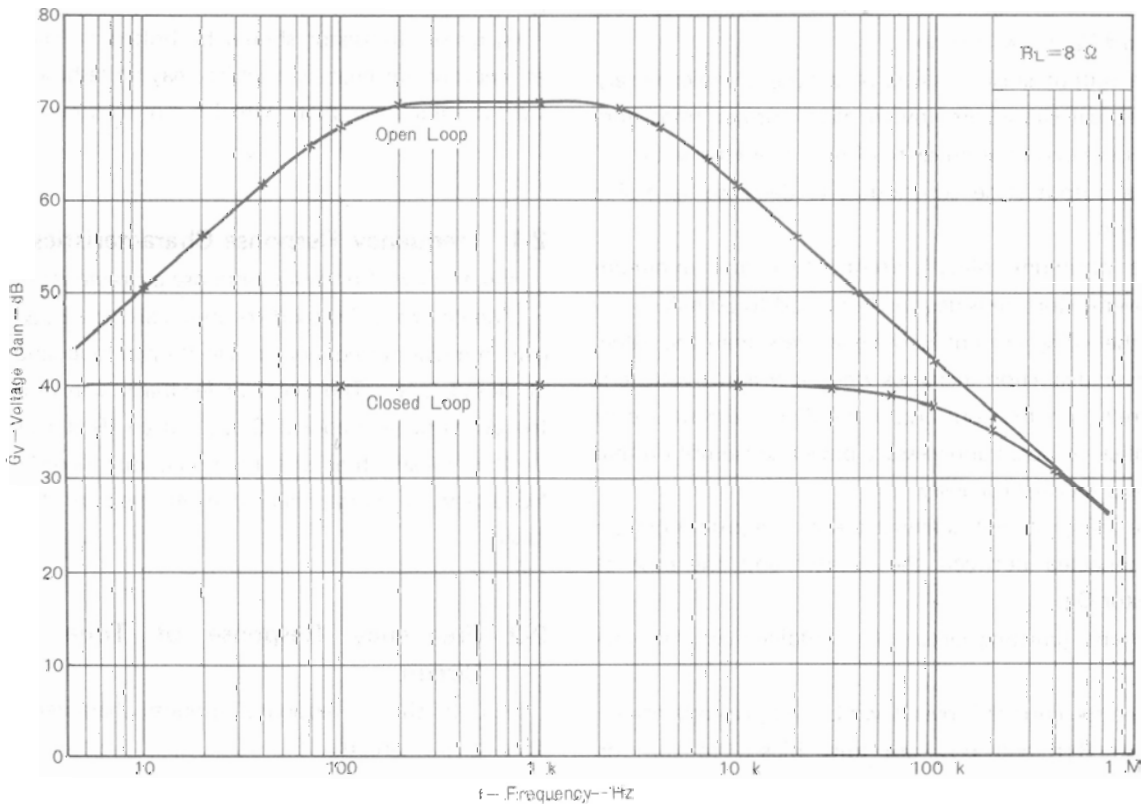


Fig. 9 Frequency Response

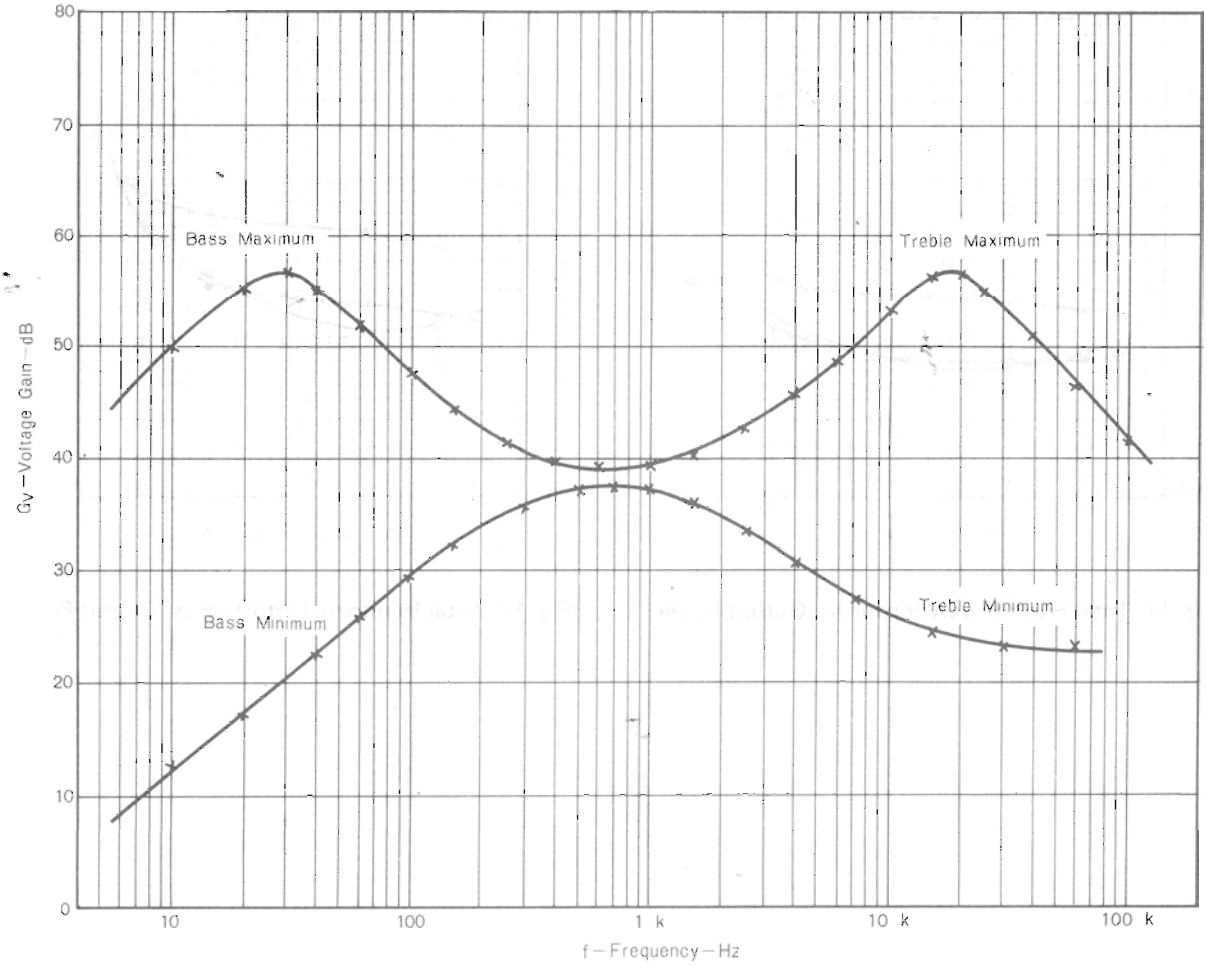


Fig. 10 Tone Control Frequency Response

2-3 Total Harmonic Distortion Characteristics

Fig. 11 and 12 show total harmonic distortion vs. output power. The harmonic distortion mainly depends on the h_{FE} balance between complementaly transistors used in driver and the power stage.

The characteristics for a 8 Ω load and 4 Ω load are shown in Fig. 11 and 12 respectively.

2-4 Power Bandwidth Characteristics

Fig. 14 and 15 show power bandwidth characteristics for a 8 Ω load and 4 Ω load respectively.

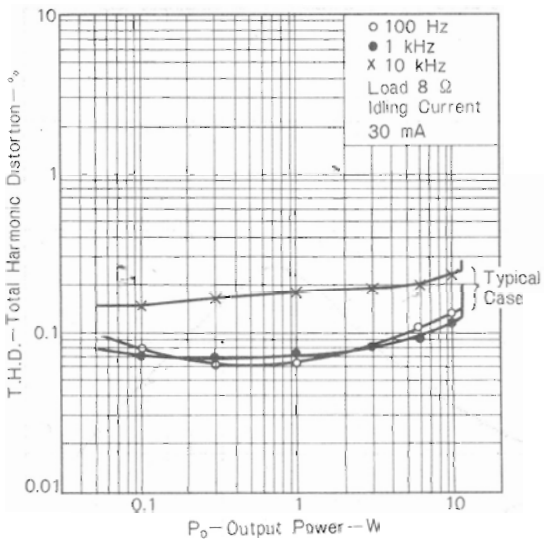


Fig. 11 Total Harmonic Distortion vs. Output Power

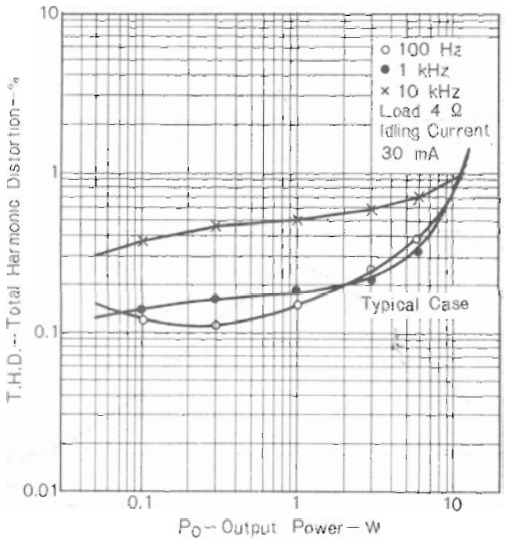


Fig. 12 Total Harmonic Distortion vs. Output Power

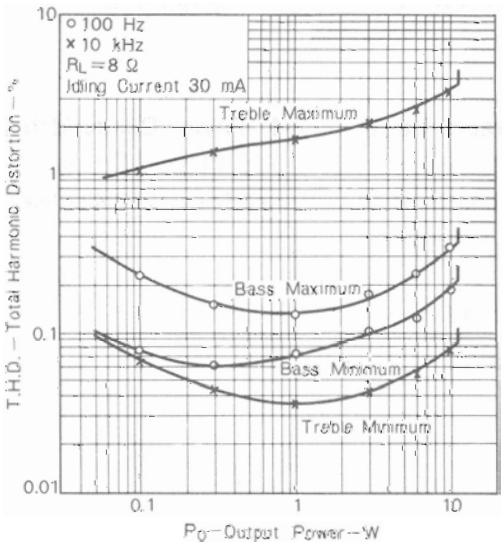


Fig. 13 Total Harmonic Distortion vs. Output Power

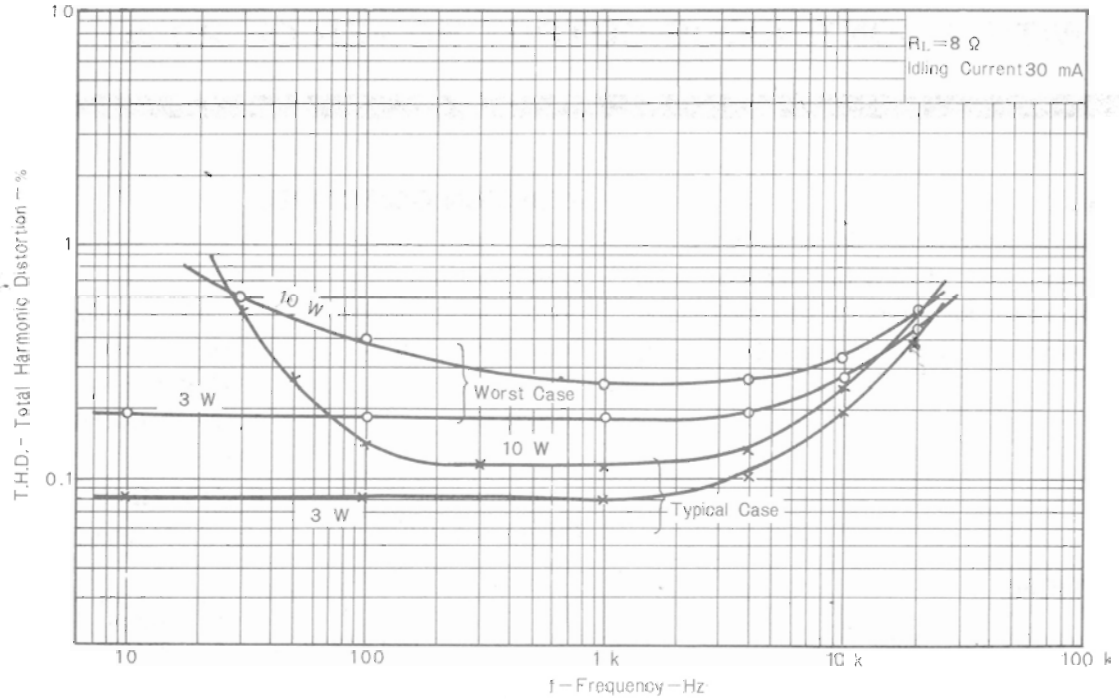


Fig. 14 Power Bandwidth

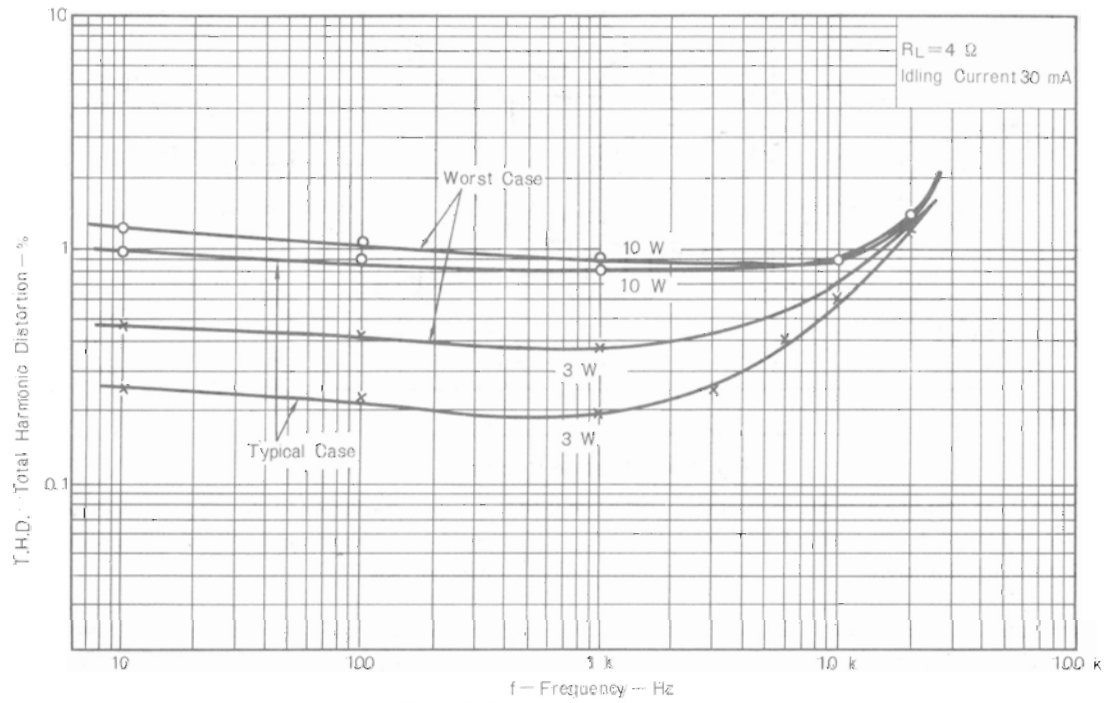


Fig. 15 Power Bandwidth

TYPICAL MAIN AMPLIFIER WITH A CONTINUOUS OUTPUT POWER OF 20 W

1. GENERAL

This circuit is a typical main amplifier of a continuous output power of 20 W (for 8 Ω load) using uni-hole package power transistors (MP-25) 2SB703 and 2SD743 with wide safe operating area (SOA) for its output stage.

2. DESIGN OBJECTIVES

Power Supply Voltage	:	V_{CC}= ±25 V
Load Resistance	:	8 Ω
Continuous Output Power	:	Po=20 W (T.H.D≦0.05 %)
Power Bandwidth	:	20 Hz — 20 kHz (Po=20 W, T.H.D≦0.05 %)
Voltage Gain	:	Av=25 dB (R_G=600 Ω, R_L =8 Ω)
Input Impedance	:	R_{IN}≧50 kΩ
Rated Input Voltage	:	V_{in}=0.7 V(r.m.s.)

3. DESCRIPTIONS

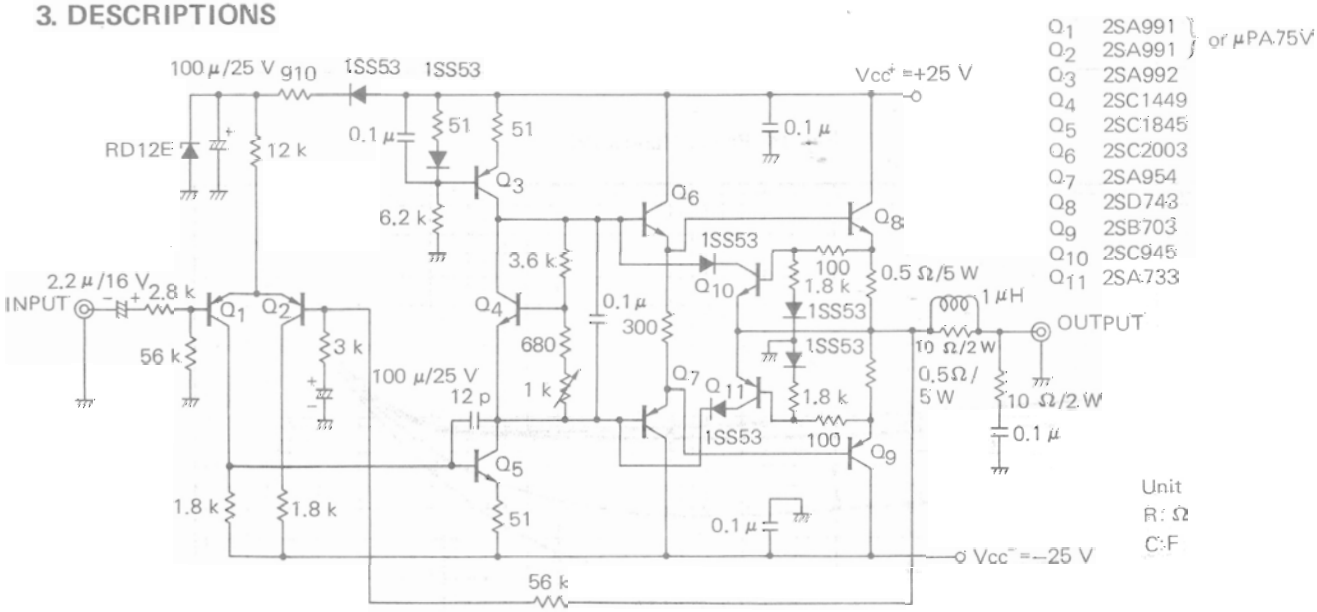


Fig. 1 Application Circuit

note 1) Firmly glue Q_4 to heat-sink with silicon grease.

note 2) Mount Q_8 and Q_9, each on a heat-sink 100 mm x 100 mm x 2 mm approximately.

note 3) All the data shown in the diagram are based on the measured characteristics of transistors with h_{FE} of medium rank.

Fig. 1 shows the application circuit. It is an orthodox amplifier composed of a differentially operated first stage amplifier, a predriver with an active load, and a pure complementary output stage of Darlington connection.

In higher frequency region, the power supply impedance largely influences on the characteristics. Since the current flowing through the voltage amplifier stage is smaller than the current through the output stage, the supply voltage of the voltage amplifier stage is varied with signal level if common feeding is employed. Therefore a separate feeding from the power source to the output stage and the voltage amplifier stage should be observed.

Furthermore, too long a power supply line to the output stage induces a collector voltage fluctuation through power supply impedance and causes an impairment of emitter follower action. Short and thick power

supply line is essential.

The power transistors on the final stage are protected by Q_{10} and Q_{11}. The protection characteristics are shown in Fig. 2.

If a pure resistance of 8 Ω is connected as a load, the protection does not go into action. But, the equivalent impedance of speaker is not purely resistive, and, hence, the circuit can even misoperate.

In such a case, some countermeasure is necessary, for example, the insertion of a small capacitance capacitor between the base and the emitter of Q_{10} or Q_{11}.

Fig. 3, 4 and 5 show the frequency response and the total harmonic distortion due to application circuit (Fig. 1).

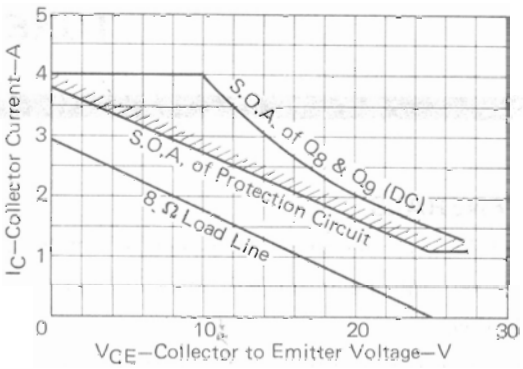


Fig. 2 Safe Operating Areas

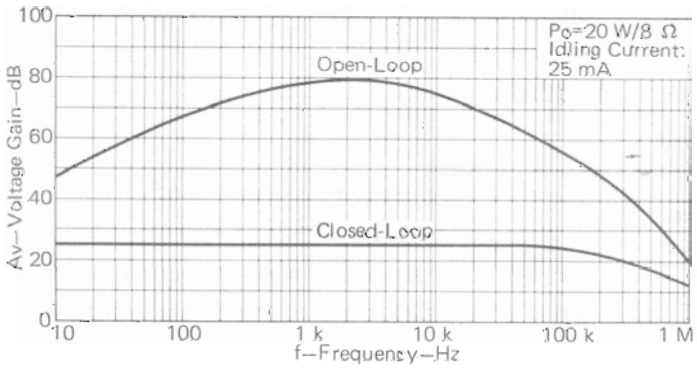


Fig. 3 Frequency Response

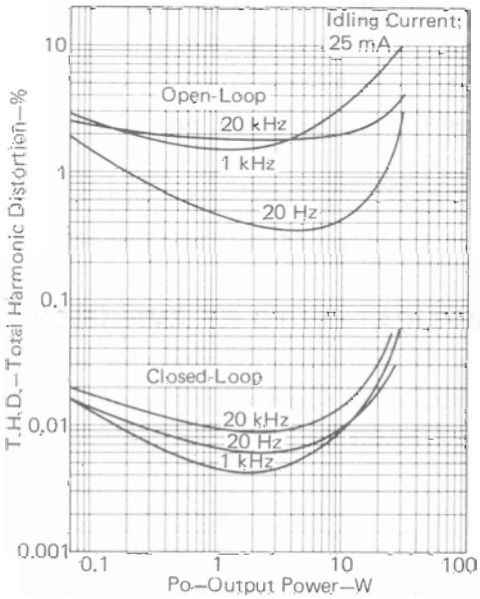


Fig. 4 Total Harmonic Distortion vs. Output Power

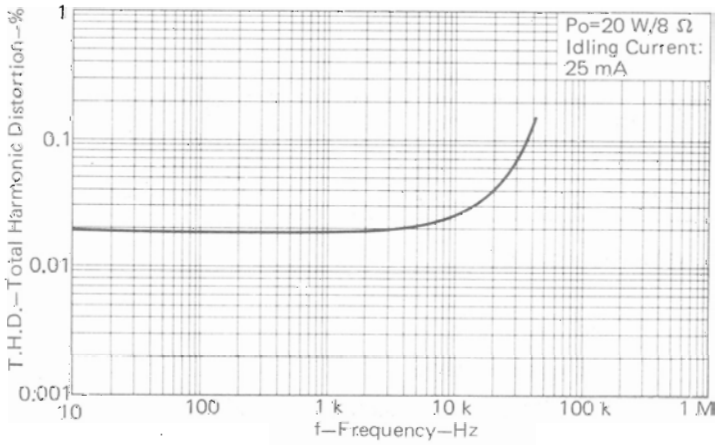


Fig. 5 Power Bandwidth

TYPICAL APPLICATION OF 3SK74 TO VHF TUNER RF AMPLIFIER

1. GENERALS

3SK74 is an N-channel MOS field effect transistor developed principally for RF amplifier and mixer of VHF tuner.

The transistor has the following features. Because of the dual gate structure, its feedback capacitance is very small (0.03 pF typical), and, due to its low input impedance (1.6 kΩ typical at 200 MHz) and its large gm (20 mS typical), y_{fs}/y_{rs} is large. So the transistor works very stably and a high power gain is obtained. Its noise figure is very small, too.

Furthermore, it has an excellent low voltage operating and can be used safely in a low power supply voltage circuit.

The following descriptions will explain the characteristics of 3SK74 applied to RF amplifier of VHF tuner.

2. APPLICATION TO RF AMPLIFIER

The characteristics to be considered generally in RF amplifier include stable gain, noise, AGC characteristic, and cross modulation.

2-1 Stable Gain

The maximum available gain (MAG) of an element is defined as the gain obtainable when the unidirectional use and the input/output matching of the element are perfectly achieved. In actual circuit, any design can hardly attain MAG practically. The concept of stable gain is therefore introduced here. It is a power gain obtained in a circuit containing feedback component by considering the performance stability. The stability index s of element itself is defined through the following formula.

$$s = \frac{2}{1 + \cos(\phi_r + \phi_f)} \cdot \frac{g_i \cdot g_o}{|y_r| \cdot |y_f|}$$

where ϕ is the phase angle of y parameter.

When the stability index s of element itself is such that $s \leq 1$, the stable gain is equal to the product of MAG and s. (When $s > 1$, the circuit works stably regardless of input/output matching conditions.)

The stable gain will be calculated below by using the actualy parameter of 3SK74.

unit: mS

	y_{is}	y_{rs}	y_{fs}	y_{os}
g+jb	0.62+j5.67	0.01−j0.02	20.4−j9.3	0.31+j2.73
$\lvert y\rvert\angle\phi$	5.705∠83.8	0.019∠−62.0	22.418∠−24.5	2.744∠83.5

@ V_{DS} = 10 V
V_{G2S} = 5 V
I_D = 10 mA
f = 200 MHz

(Data are measured with products whose y_{fs} values are typical.)

$$S = \frac{2}{1+\cos(\phi_r+\phi_f)} \cdot \frac{g_i \cdot g_o}{|y_r| \cdot |y_f|}$$

$$= \frac{2}{1+\cos(-62-24.5)} \cdot \frac{0.62 \cdot 0.31}{0.019 \cdot 22.4} = 0.85,$$

$$MAG = \frac{|y_f|^2}{4 g_i \cdot g_o} = \frac{22.4^2}{4 \times 0.62 \times 0.31} = 653 \ (=28.15 \text{ dB}),$$

and

stable gain = MAG x s,

$|G_{ps}| = 653 \times 0.85 = 555 \ (= 27.4 \text{ dB})$.

The result tells that a stable power gain of 27.4 dB would be obtained.

However, in an actual circuit, the Q's of the loads to

the input/output tuning circuits are adjusted in order to get the bandwidth required to the circuit. This adjustment adds an insertion loss in the tuning circuits, and, hence, the measured value of gain is usually lower than the calculated stable gain.

Fig. 1 and Fig. 2 show the measured values of power gain of RF amplifier using 3SK74. The figure gives Gps of 22 dB at about 200 MHz. The stability index of the circuit is calculated as

$$\frac{Gp}{Gp(max)} = \frac{158.5\ (=22\ dB)}{653(=28.15\ dB)} = 0.24$$

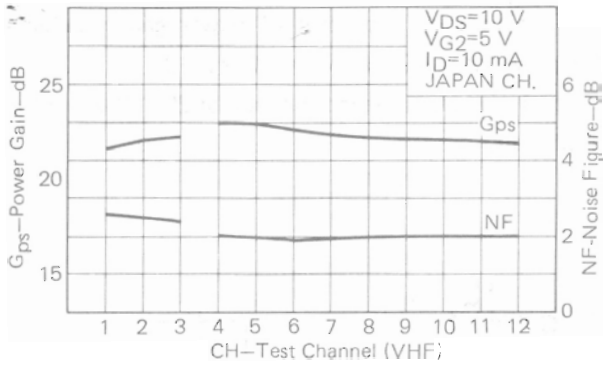


Fig. 1 Power Gain and Noise Figure vs. VHF Channel

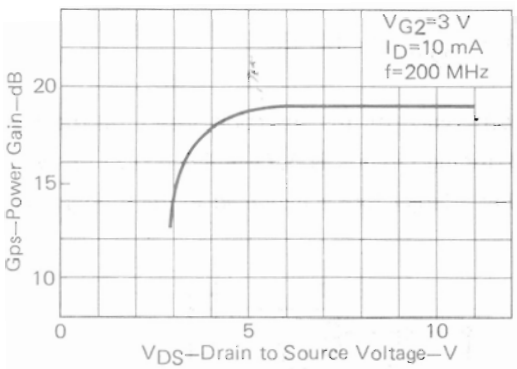


Fig. 2 Power Gain vs. Drain to Source Voltage

Fig. 3 shows about value

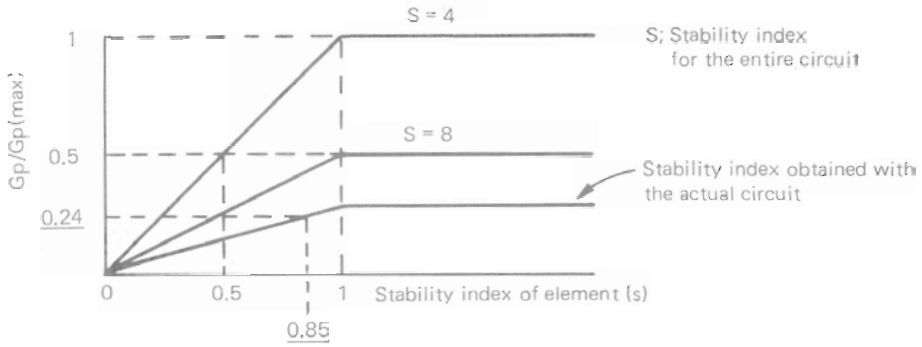


Fig. 3 Stability Index

Thus, it is shown that a very stable and high power gain is obtained.

When 3SK74 is used in an RF amplifier of electronic tuning type tuner, the unloaded Q of the tuning circuit is depressed and the insertion loss is increased as compared with a capacitance type tuner because a variable capacitance diode is used in the electronic tuning circuit.

The insertion loss in the tuning circuit using a variable capacitance diode will be obtained in the following manner. Assume the tuned capacitance as 10 pF and $r_s = 0.5\ \Omega$ at 200 MHz. Q_O of the variable capacitance diode is

$$Q_O = \frac{1}{\omega C_{rs}} = \frac{1}{2\times\pi\times200\times10^6\times10\times10^{-12}\times0.5} = 159.$$

When Q_O of L used in the tuning circuit is assumed 140 (which is a value obtained with an R-X meter at 200 MHz), the Q_O of the tuning circuit takes a value $\frac{159\times140}{159+140} = 74.4$. When Q_L of the circuit is 13.3 (for 3 dB bandwidth of 15 MHz and at 200 MHz), the insertion loss of the tuning circuit using a variable capacitance diode is calculated as

$$20\log\left(1-\frac{Q_L}{Q_O}\right) = 20\log\left(1-\frac{13.3}{74.4}\right) = -1.71\ dB.$$

On the other hand, for a tuning circuit using a capacitor with Q_0 of 1000, the similar calculation leads to Q_0 of the tuning circuit which is

$$\frac{1000 \times 140}{1000 + 140} = 122.8,$$

and the insertion loss which is

$$20 \log \left(1 - \frac{13.3}{122.8}\right) = -1.0 \text{ dB}.$$

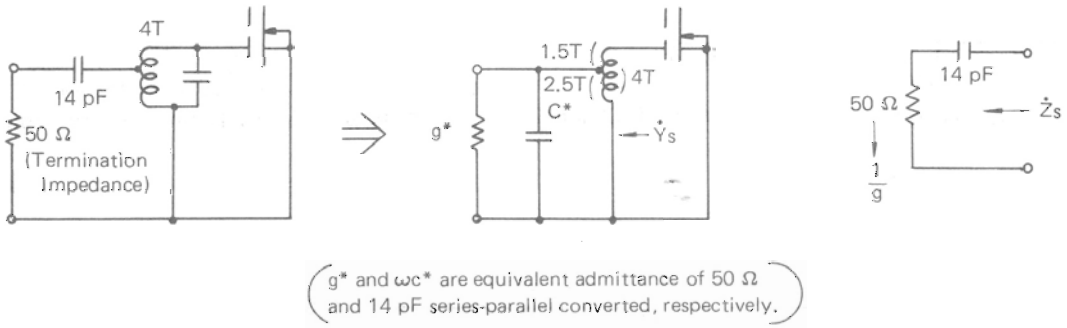
The difference of the insertion losses of the both types of tuning circuits is 1.71 − 1.0 = 0.71 dB which means that a larger loss is expected in the tuning circuit having a variable capacitance diode.

2-2 Noise Characteristics

Fig. 1 shows the noise figure (NF) of 3SK74. NF at about 200 MHz is 2 dB.

Generally the condition for the minimum NF is $g_S > g_i$ (input conductance of element). This condition does not coincide with that of power gain matching. (The power gain is 22 dB when NF is 2 dB.)

Fig. 4 represents the input circuit at 200 MHz and for NF of 2 dB.



(g* and ωc* are equivalent admittance of 50 Ω and 14 pF series-parallel converted, respectively.)

Fig. 4 Equivalent Source Admittance and Impedance

The signal source admittance in this configuration is calculated below.

$$\dot{Z}_S = \frac{1}{g} + \frac{1}{j\omega C}$$

$$\dot{Y}_S = \frac{1}{\frac{1}{g} + \frac{1}{j\omega C}} = \frac{(\omega C)^2}{g^2 + (\omega C)^2}\, g + j\, \frac{g^2}{g^2 + (\omega C)^2}\, \omega C$$

$$\dot{Y}_S = \frac{(2\pi \times 200 \times 10^6 \times 14 \times 10^{-12})^2 \times 20 \times 10^{-3}}{(20 \times 10^{-3})^2 + (2\pi \times 200 \times 10^6 \times 14 \times 10^{-12})^2}$$

$$+ j \frac{(20 \times 10^{-3})^2 \times 2\pi \times 200 \times 10^6 \times 14 \times 10^{12}}{(20 \times 10^{-3})^2 + (2\pi \times 200 \times 10^6 \times 14 \times 10^{-12})^2}$$

$$= 8.73 \times 10^{-3} + j\, 9.9 \times 10^{-3} = 8.73 \text{ mS} + j\, 9.9 \text{ mS}$$

This value is stepped up by L to the signal source admittance seen from FET of

$$(8.73 \times 10^{-3} + j\, 9.9 \times 10^{-3}) \times \left(\frac{2.5}{4}\right)^2 = 3.41 \times 10^{-3} + j\, 3.86 \times 10^{-3}$$

$$= (3.41 \text{ mS} + j\, 3.86 \text{ mS})$$

g_S b_S

The real part of the result leads to the signal source impedance of $\frac{1}{3.41 \times 10^{-3}} = 293\ \Omega$.

2-3 AGC Characteristics

Among AGC characteristics, AGC range and AGC sensitivity are important. AGC range is expressed by the difference of power gains for the maximum sensitivity and for the maximum attenuation. The gain

attenuation capability of an active element reaches its limit at the point of equivalence of forward transfer gain and reverse transfer gain.

Fig. 5 shows the AGC characteristics of 3SK74. The figure demonstrates that the AGC range is 48 dB. This large range is obtained in virtue of a very small feedback capacitance due to the dual gate structure of the FET.

AGC sensitivity is defined by the amount of control voltage required for obtaining a certain amount of attenuation.

Since AGC of 3SK74 is a reverse one, the AGC sensitivity is almost determined by the pinch off voltage of Gate 2. The insertion of a source resistance can raise the AGC sensitivity at a reasonable V_{G2} (V_{AGC}) value.

Fig. 5 shows the AGC characteristics with and without the source resistance: Rs.

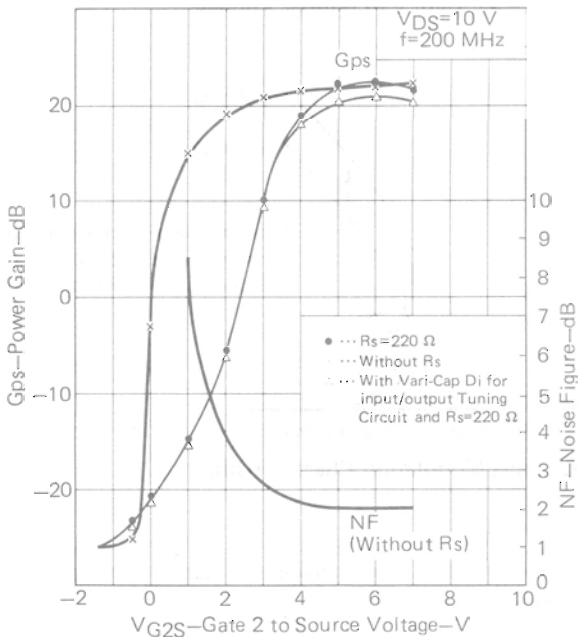


Fig. 5 AGC Characteristics

2-4 Cross Modulation Characteristics

Fig. 6 shows the cross modulation characteristics of 3SK74.

Because of a quasi-square transfer characteristics which are inferent to FET, the cross modulation at a small AGC voltage is for superior to that of bipolar transistor. Also, the remote cutoff transfer characteristics resulted by the dual gate configuration permit no deterioration of cross modulation even for a large AGC voltage.

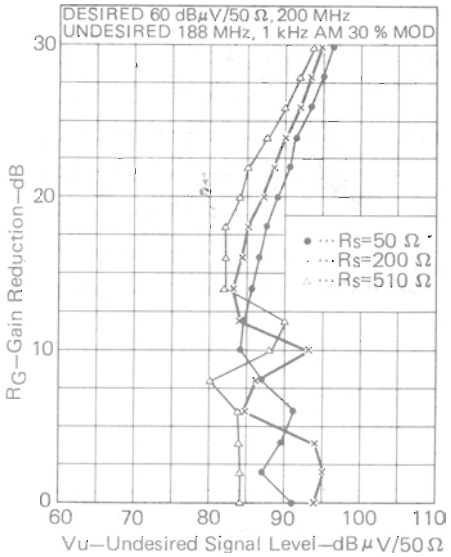


Fig. 6 1 % Cross Modulation

Fig. 7 to 9 provide data with which the dependence of the cross modulation to the biasing condition of the FET are estimated. Fig. 7 shows the relationship of I_D to V_{G1S} with V_{G2S} as a parameter. Load lines coresponding to the source resistances of 50, 200, and 510 Ω at V_{G1}=2 V are drawn in the figure. By using the load lines, V_{G1S} for any V_{G2S} is obtained. Then g_m is obtained from Fig. 8 (g_m vs. V_{G1S}). Fig. 9 shows the g_m to V_{G2S} characteristics when the FET is operated of the load lines for source resistances of 50, 200 and 510 Ω at V_{G1}=2 V. The cross modulation variations for these operation conditions are demonstrated in Fig. 6.

As the result, it can be said, in general, that the cross modulation will depend on the source resistance as schematically shown in Fig. 10.

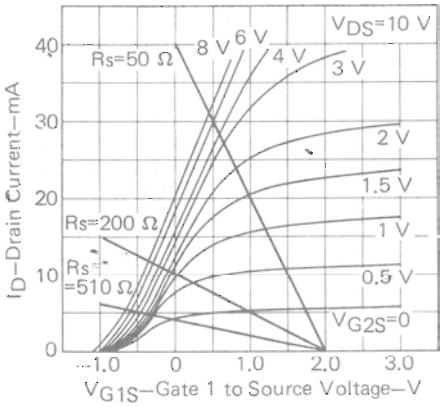


Fig. 7 Drain Current vs. Gate 1 to Source Voltage

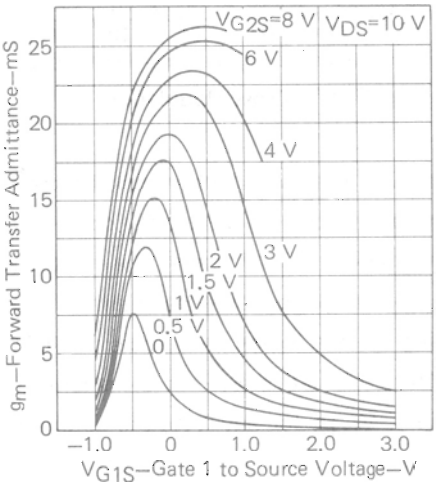


Fig. 8 Forward Transfer Admittance vs. Gate 1 to Source Voltage

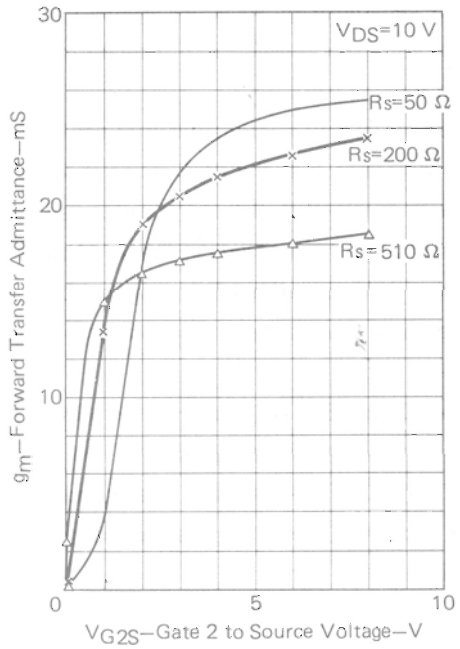


Fig. 9 Forward Transfer Admittance vs. Gate 2 to Source Voltage

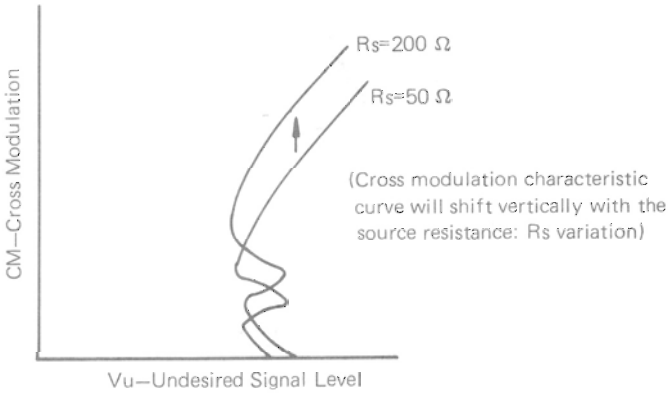


Fig. 10 Cross Modulation Characteristics

Therefore, in order to improve the cross modulation characteristics at a large AGC voltage, a larger source resistance and a smaller I_D are desirable when the distortion produced by FET tends to be deteriorated at a larger AGC voltage, and, a smaller source resistance and a larger I_D are desirable when the distortion produced by FET tends to be ameliorated at a larger AGC voltage, on the contrary.

3SK74 belongs to the latter. But, too small source resistance should be avoided because, at a small source resistance (about 50 Ω), AGC sensitivity is inferior and much more power is consumed.

Concurrently, the appropriate biasing condition for 3SK74 is assumed to be V_{G1}=2 V and source resistance of 220 Ω at V_{DS}=10 V. The cross modulation characteristic will then be;

at full gain, undesired signal level of 94 dBμV/50 Ω,
at 30 dB attenuation, undesired signal level of 95 dBμV/50 Ω,

at the desired frequency of 200 MHz and the undesired frequency of 188 MHz.

2-5 Characteristics of RF Amplifier Using 3SK74

The characteristics of 3SK74 used in the circuit shown in Fig. 11 are summarized, with regard to items up to 2–4.

- Power Gain (Gps) ..... 22 dB
  (stability index of circuit ..... 14.2)
  at 200 MHz.
- Noise Figure (NF) ..... 2 dB at 200 MHz.
- AGC Range ..... 48 dB
  (AGC voltage ..... 5 to −1 V)
  at 200 MHz.
- Cross Modulation
  at full gain 94 dBμV/50Ω
  at 30 dB attenuation 95 dBμV/50Ω
  for $f_{des.}$ = 200 MHz.
  $f_{undes.}$ = 188 MHz, 1 kHz
  AM 30 % modulation.

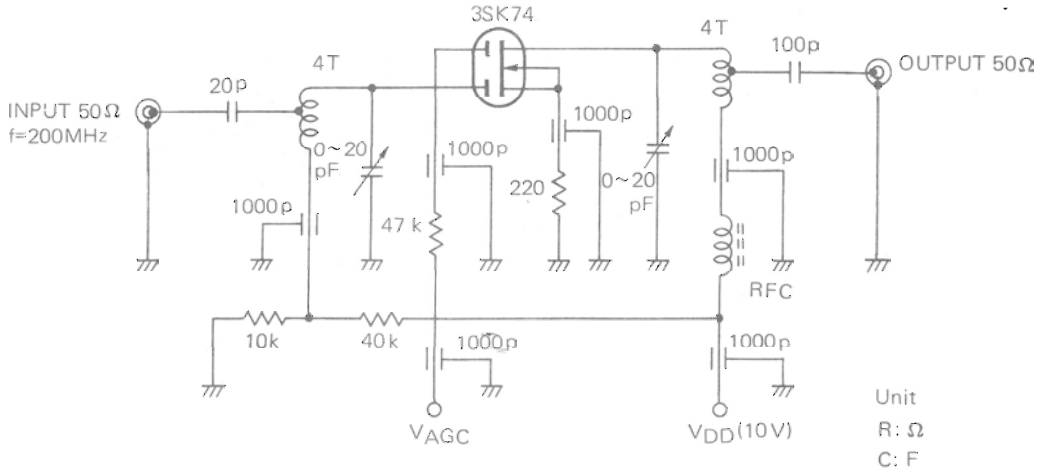


Fig. 11 Application Circuit

TYPICAL APPLICATION OF 3SK74 TO VHF TUNER MIXER

1. GENERALS

3SK74 is an N-channel MOS field effect transistor developed principally for RF amplifier and mixer of VHF tuner.

The transistor has the features that, because of dual gate structure, its feedback capacitance is very small (0.03 pF, typically), and, due to its low input impedance (1.6 kΩ typically at 200 MHz) and its large g_m (20 mS typically), its y_{rs}/y_{rs} is large and very stable. Hence a large power gain and a very small noise figure are obtained. In spite of a demerit that, when FET is used for a mixer, a large local oscillation signal injection level is needed for obtaining a satisfactory conversion gain since its g_m is smaller than that of bipolar transistor, the merit of large improvement in intermodulation characteristics is expected as a substantial one.

The following description will explain the characteristics of 3SK74 used for mixer of VHF tuner.

2. APPLICATION TO MIXER

In an application of a FET to a mixer (MIX), it is expected that the intermodulation and the spurious signal are largely reduced because its transfer characteristic is quasi-square as contrasted to the characteristic of a bipolar transistor. However, it is necessary to boost the local oscillation signal level because the g_m of FET is small. Usually, a dual gate FET is used in either of two ways: Gate 1 input – Gate 1 injection, and, Gate 1 input – Gate 2 injection. Fig. 1 shows G_{cs} vs. local injection level characteristics (conversion power gain). In Gate 1 input – Gate 1 injection type, the smaller is the injection capacitance, the larger is G_{cs}. On the other hand, in Gate 1 input – Gate 2 injection type, the larger is the injection capacitance, the larger is G_{cs}.

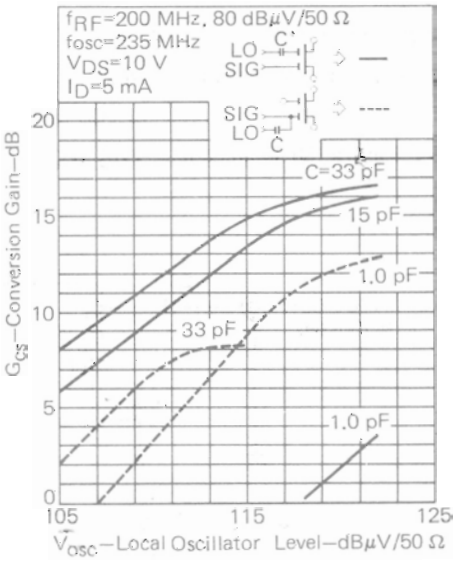


Fig. 1 Conversion Gain vs. Local Oscillator Level

These situations can be illustrated below (Fig. 2) by interpreting the dual gate FET as the equivalent cascode connection of single gate FET's.

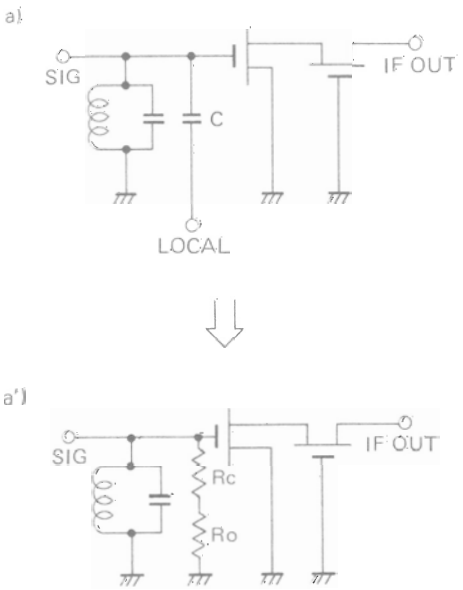


Fig. 2 Interpreting the Dual Gate FET as the Equivalent Cascode Connection of Single Gate FET's

a) represents a Gate 1 input – Gate 1 injection type which is equivalently grounded through the injection capacitance and the output impedance of the local oscillator. (In the experiment, an SG has been used for the local and, hence, the termination impedance of the SG was 50 Ω. In an actual circuit, the impedance will be the output impedance of local oscillator transistor.) This is equivalent to the Q-dumping of the input tuning circuit with R_C (impedance of the capacitance) and R_O (output impedance of local oscillator) as shown in a'). Therefore these R's should be so increased that they can be ignored. This requires the smallness of the injection capacitance C. (Refer to Fig. 3.)

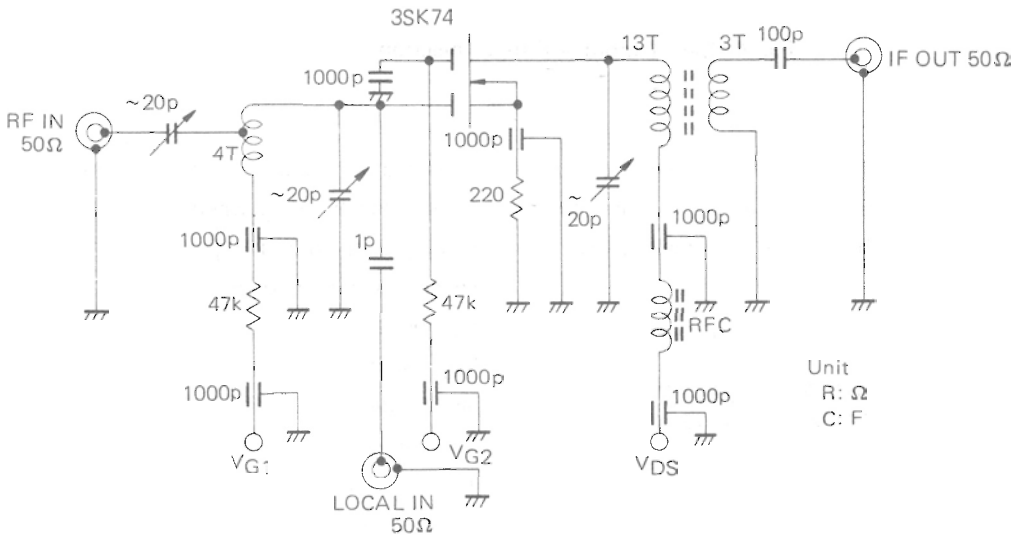


Fig. 3 Gate 1 Input – Gate 1 Injection Type Mixer Circuit

b) represents a Gate 1 input – Gate 2 injection type. Gate 2 must not be perfectly RF-grounded because Gate 2 should receive local signal. In this configuration Gate 2 is equivalently grounded via the injection capacitance and the output impedance of the local oscillator, and these grounding impedances affects the feedback capacitance and, hence, G_{cs}. In order to have a large G_{cs}, it is necessary to use as large a capacitance as possible so that the impedance can be ignored. (Refer to Fig. 4.)

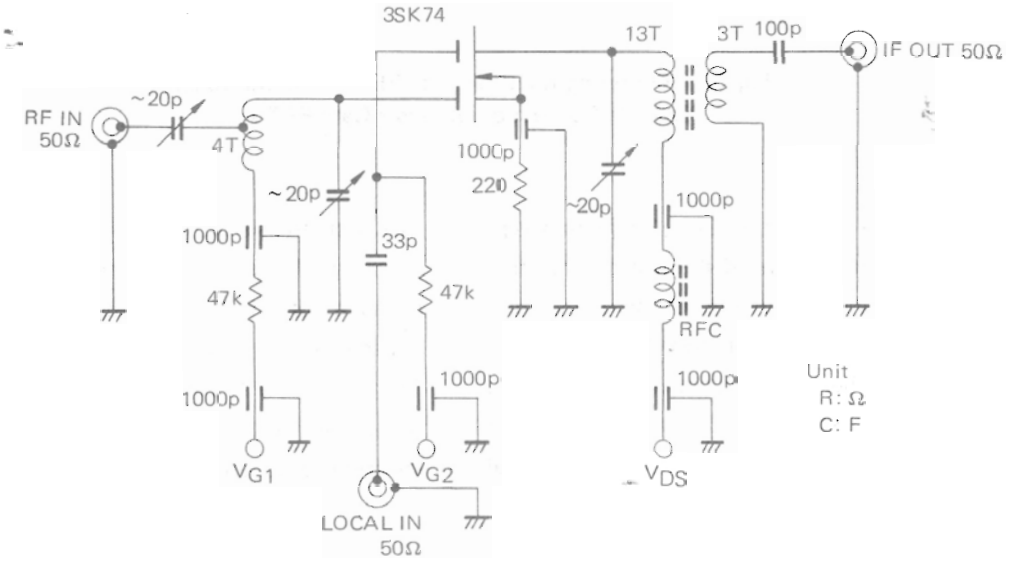


Fig. 4 Gate 1 Input – Gate 2 Injection Type Mixer Circuit

Another measure can be conceived that, for grounding Gate 2 with regard to IF, an IF trap is inserted. But experiment has shown that the measure was not so effective.

Fig. 5 shows the G_{cs} vs. V_{G2} and I_D characteristics.

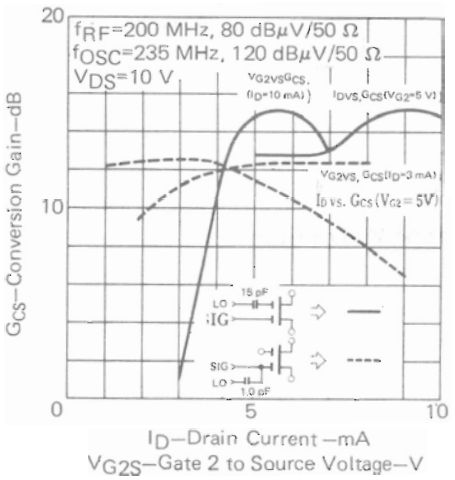


Fig. 5 Conversion Gain vs. Drain Current and Gate 2 to Source Voltage

In Gate 1 input – Gate 1 injection type, G_{cs} is not so affected by V_{G2} when V_{G1} is kept constant. Also, if V_{G2} is fixed and V_{G1} is varied to vary I_D, the G_{CS} change is rather slight. In Gate 1 input – Gate 2 injection type, G_{cs} experiences a rather large effect of V_{G2}, with V_{G1} kept constant. However, G_{cs} does not largely depend on I_D variation caused by V_{G1} shift. Summaries of the above described results are shown in Table 1, which lists the characteristics, merits and demerits of both Gate 1 input – Gate 1 injection and Gate 1 input – Gate.

Table 1 Comparing with Gate 1 Injection and Gate 2 Injection Type

CIRCUIT TYPE	MERIT	DEMERIT	CHARACTERISTICS	TEST CONDITIONS
GATE 1: INPUT GATE 1: INJECTION	① Relatively small dependence on biasing (V_{G2} and I_D). ② The smaller the local injection capacitance, the better (the load for the local oscillator transistor is the lighter).	Gcs is smaller compared with that of Gate 2 injection type	Gcs=12.4 dB Intermodulation = 63 dB (Refer to Fig. 6)	V_{DS}=10 V, V_{G2}=3.0 V I_D=5.0 mA f_{RF}=200 MHz fosc=235 MHz,120 dBμV/50 Ω Cinj=1.0 pF f_{RF1}=199.5 MHz, f_{RF2}=200.5 MHz } 80 dBμV/50 Ω fosc=235 MHz,120 dBμV/50 Ω
GATE 1: INPUT GATE 2: INJECTION	Gcs is larger compared with that of Gate 1 injection type.	① Relatively large dependence on biasing (V_{G2} and I_D). ② The larger the local injection capacitance, the better (the load the local oscillator transistor is the heavier).	Gcs=16.4 dB Intermodulation = 60 dB (Refer to Fig. 6).	Same Conditions as above except that injection capacitor: C_{inj}=33 pF

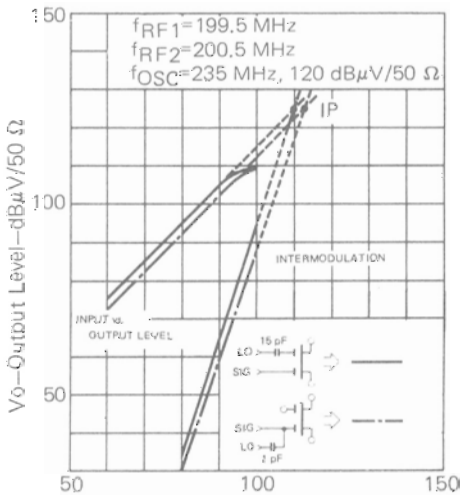


Fig. 6 Intersept Point

Based on the data on Table 1, Gate 1 input – Gate 1 injection type circuit system is recommended for the practical MIX tunner. (Refer to Fig. 7.)

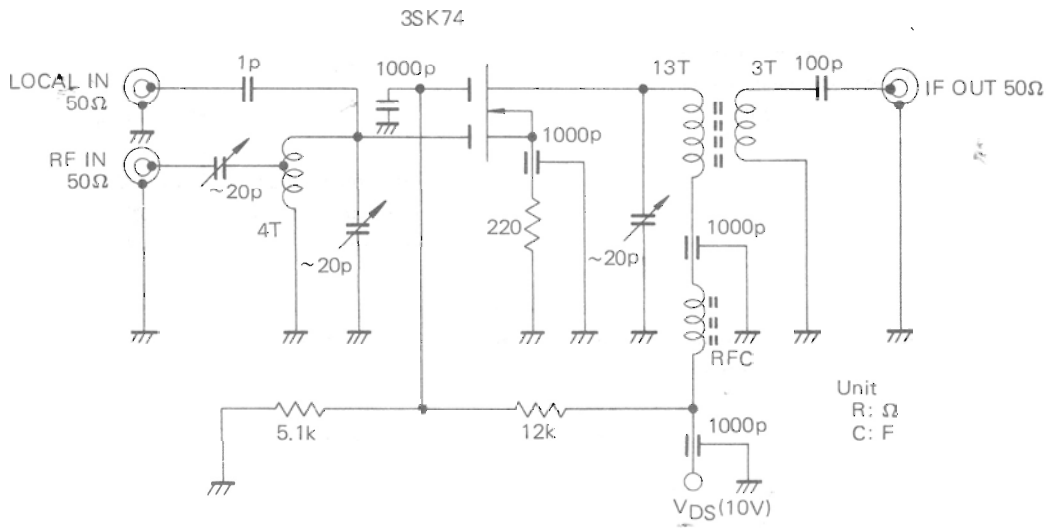


Fig. 7 Useful Mixer Circuit
(Gate 1 Input – Gate 1 Injection Type)

TYPICAL APPLICATION OF 3SK87 TO UHF TUNER RF AMPLIFIER

1. GENERALS

The 3SK87 is an N-channel MOS field effect transistor developed principally for RF amplifiers of UHF tuners.

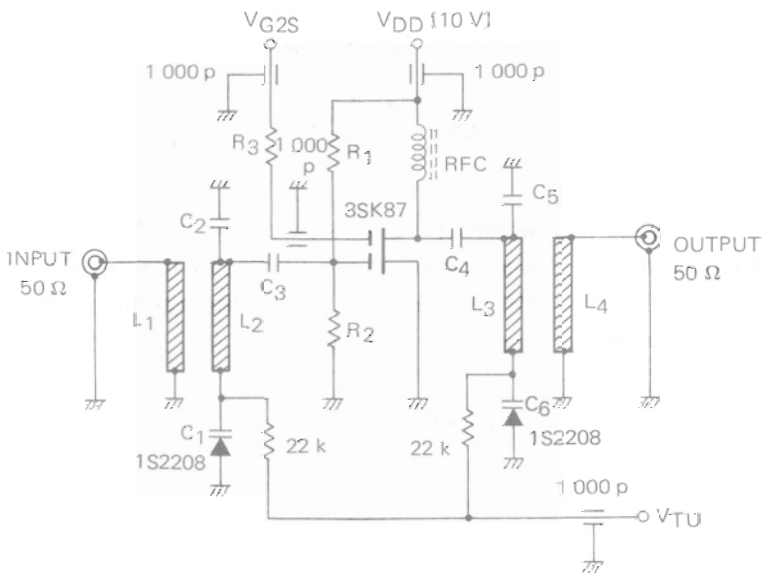
By virtue of a dual gate configuration, the transistor is provided with a small feedback capacitance (0.02 pF typical) and a large g_m (22 mS typical) and, hence, a large y_{fs}/y_{rs}. Therefore it works very stably and yields a high power gain.

The 3SK87 is the FET designed also for providing tuners having λ/2 distributed-constant type tuning circuit with excellent characteristics.

The following sections will describe the characteristics of 3SK87 used for RF amplifiers of UHF tuner.

2. APPLICATIONS TO RF AMPLIFIERS OF UHF TUNER

The circuitries for RF amplifiers of UHF tuner can be categorized into two classes: one is λ/2 distributed-constant tuning circuit and the other is λ/4 distributed-constant tuning circuit. The circuit system here reported is the electronic tuner of λ/2 distributed-constant tuning type which is relatively insensitive to the effect of Ciss of elements. Its circuit diagram is shown in Fig. 1



Unit
R: Ω
C: F

R_1=33 kΩ
R_2=1 kΩ
R_3=47 kΩ
$L_{1\sim4}$=18.5 nH
$C_{1,6}$=2~15 pF
$C_{2,5}$=11 pF
$C_{3,4}$=30 pF

Fig. 1 Application Circuit

The biasing condition is assumed that V_{DD} = 10 V and I_D = 10 mA, Approximately. The value of V_{G1S} for I_D of 10 mA is, as indicated by Fig. 2, 0.3 V when V_{G2S} is 4 V.[note 1)]

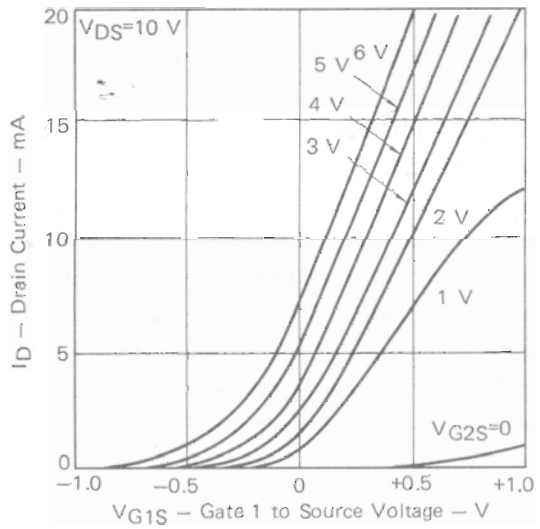


Fig. 2 Drain Current vs. Gate 1 to Source Voltage

note 1) Fig.2 is valid for I_{DSS} of 3.5 mA (Typical).

The resistances of the biasing circuit are concurrently determined as:

R_1 = 33 kΩ, R_2 = 1 kΩ, and R_3 = 47 kΩ.

Since R_1 and R_3 serve also for the protection of gates 1 and 2, it is safer to select them as large as possible.

The next step is the determination of tuner constants. (f = 470 — 890 MHz in U.S.A. channel standard)

The input tuning circuit can be illustrated as shown in Fig. 3.

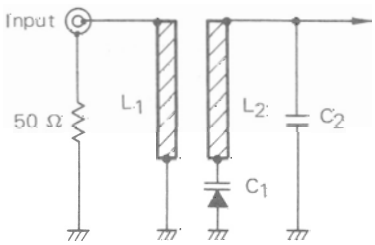


Fig. 3 Input Tuning Circuit

In the drawing, C_1 denotes a variable capacitance diode with the capacitance of about 2–15 pF. (In the present case, 1S2208 is used.) L_2 and C_1 should be determined so that the receiving frequency range of 470 — 890 MHz is obtained finally for the variation the capacitance. Two resonance points are obtained since the tuner shown is of λ/2 distributed-constant type.

The resonance frequencies are given by the follwing formulas.

$$\omega_1 = \frac{1}{\sqrt{L_2 C_1}} \quad \text{(series resonance)} \quad \ldots\ldots\ldots\ldots (1)$$

$$\omega_2 = \sqrt{\frac{1}{L_2 C_1} + \frac{1}{L_2 C_2}} \quad \text{(parallel resonance)} \quad \ldots (2)$$

Since the parallel resonance is used in general, the actual resonance frequency is given by eq. (2). Usually C_2 should be selected much larger than the element input capacitance. For example, if C_2 is determined to about 11 pF, it is almost five times as large as the input capacitance which is typically 2.5 pF. This means that, if the element input capacitance is changed because of temperature or power supply voltage fluctuation, the total capacitance of C_2 and the input capacitance is shifted not so much and, consequently, the stable circuit action results. This feature is one of the characteristics of λ/2 distributed-constant tuning circuit.

When the values of C_1 and assumed C_2 are put into eq.(2) together with the receiving frequency, L_2 can be calculated. The expression can be transformed as:

$$L_2 = \frac{\frac{1}{C_1} + \frac{1}{C_2}}{\omega^2} = \frac{\frac{1}{2 \times 10^{-12}} + \frac{1}{11 \times 10^{-2}}}{(2 \times \pi \times 900 \times 10^6)^2}$$

$$= 18.5 \text{ nH},$$

where C_1 = 2 pF, C_2 = 11 pF, and f = 900 MHz. Also, when frequency is calculated by using L_2 (18.5 nH), C_1 (15 pF), and C_2 (11 pF), through the transformed expression of eq. (2) as

$$f = \frac{\sqrt{\frac{1}{L_2 C_1} + \frac{1}{L_2 C_2}}}{2\pi}$$

$$= \frac{\sqrt{\frac{1}{18.5 \times 10^{-9} \times 15 \times 10^{-12}} + \frac{1}{18.5 \times 10^{-9} \times 11 \times 10^{-12}}}}{2\pi}$$

$$= 464 \text{ MHz}$$

Therefore, the constants of the tuner for the receiving frequency range of 470--890 MHz are:

L_2 = 18.5 nH, C_1 = 2 – 15 pF, and C_2 = 11 pF

The next step is the determination of the constants of the matching circuit to match the input and output impedances of the element signal source and load impedances.

For that purpose, the information of input and output impedances and the maximum available gain of the element is necessary.

The characteristics of 3SK87 will be concurrently explained below in terms of its y-parameters.

Table 1 Typical Y-Parameter of 3SK87

freq. (MHz)	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
	$\lvert y_{11}\rvert$(mS)	$\angle\phi_{11}$(deg.)	$\lvert y_{21}\rvert$(mS)	$\angle\phi_{21}$(deg.)	$\lvert y_{12}\rvert$(mS)	$\angle\phi_{12}$(deg.)	$\lvert y_{22}\rvert$(mS)	$\angle\phi_{22}$(deg.)
400	6.77	80.3	24.30	−24.1	0.036	−46.6	2.53	78.0
500	8.59	78.2	25.08	−29.4	0.040	−24.4	3.22	76.6
600	10.51	76.5	26.19	−35.5	0.079	11.3	3.72	78.5
700	12.28	74.8	26.87	−41.8	0.123	22.6	4.23	81.9
800	13.79	72.8	28.58	−48.6	0.187	32.7	4.57	82.2
900	15.51	68.5	30.53	−58.7	0.269	39.3	5.08	83.2

(V_{DS}=10 V, V_{G2S}=4 V, I_D=10 mA. The values in this table are measured on the products whose y_{21} values are typical.)

Table 2 Y_{11} and Y_{22} of 3SK87

freq. (MHz)	Y_{11}		Y_{22}*	
	g_{11} (mS)	b_{11} (mS)	g_{22} (mS)	b_{22} (mS)
400	1.14	6.67	0.53	2.48
500	1.76	8.41	0.75	3.13
600	2.45	10.22	0.74	3.65
700	3.22	11.85	0.60	4.19
800	4.08	13.17	0.62	4.53
900	5.68	14.43	0.60	5.03

(*The data of output admittance are only for reference because the accuracy of NETWORK ANALYSER is deteriorated due to the very high output impedance.)

Transformation of input and output admittances (Y_{11} and Y_{22}) given in the table into a form of $Y = g + jb$ leads to Table 2.

Referring to Tables 1 and 2, Gp (max) and stability index S are calculated as follows in order to know the RF characteristics of 3SK87.

$$G_p(\max) = \frac{|y_f|^2}{4 g_i g_o} \quad \cdots\cdots (3)$$

$$S = \frac{2}{1 + \cos(\phi_f + \phi_r)} \cdot \frac{g_i g_o}{|y_f|\,|y_r|} \quad \cdots\cdots (4)$$

where $|y_f|$ —— forward transfer admittance ($=|y_{21}|$),
$|y_r|$ —— reverse transfer admittance ($=|y_{12}|$),
ϕ_f —— forward transfer admittance phase angle ($=\phi_{21}$),
ϕ_r —— reverse transfer admittance phase angle ($=\phi_{12}$),
g_i —— element input conductance ($=g_{11}$), and
g_o —— element output conductance ($=g_{22}$).

Gp (max) (maximum available power gain) and S (stability index of element alone) at 900 MHz are obtained from eqs. (3) and (4) as

$$G_p(\max) = \frac{|y_f|^2}{4 g_i g_o} = \frac{(30.53 \times 10^{-3})^2}{4 \times 5.68 \times 10^{-3} \times 0.60 \times 10^{-3}}$$

$$= 68.4\ (= 18.4\ \text{dB}).$$

$$S = \frac{2}{1 + \cos(\phi_f + \phi_r)} \cdot \frac{g_i g_o}{|y_f|\,|y_r|}$$

$$= \frac{2}{1 + \cos(-58.7 + 39.3)} \cdot \frac{5.68 \times 10^{-3} \times 0.60 \times 10^{-3}}{30.53 \times 10^{-3} \times 0.269 \times 10^{-3}}$$

$$= 0.43$$

Similarly, at f = 500 MHz,

$$G_p(\max) = \frac{(25.08 \times 10^{-3})^2}{4 \times 1.76 \times 10^{-3} \times 0.75 \times 10^{-3}} = 119.1\ (= 20.8\ \text{dB})$$

$$S = \frac{2}{1 + \cos\{-29.4 + (-24.4)\}} \cdot \frac{1.76 \times 10^{-3} \times 0.75 \times 10^{-3}}{25.08 \times 10^{-3} \times 0.04 \times 10^{-3}}$$

$$= 1.65$$

The result tells that, at 500 MHz, the circuit works stably with Gp (max) of 20.8 dB regardless of the input/output matching conditions, while, at 900 MHz there is a possibility of oscillation for some input/output matching conditions and Gp (max) of 18.4 dB is obtain-

ed.

An example of the method for setting constants of input/output impedance matching circuits will be described, referring to the data above shown. According to Fig. 2, the input and output impedances of the element are:

at f= 900 MHz, $R_i=1/g_i=1/5.68\times10^{-3}$ =176 Ω,
$R_o=1/g_o=1/0.6\times10^{-3}$ =1.67 kΩ, and
at f=500 MHz, $R_i=1/g_i=1/1.76\times10^{-3}$ =568 Ω, and
$R_o=1/g_o=1/0.75\times10^{-3}$ =1.33 kΩ.

With these values as referrence, C_3, and C_4, and coupling coefficients of inductors are determined, and the signal source and the load impedances are calculated as explained below.

Because the frequencies dealt with here belong to UHF band and the circuit is of a distributed – constant nature, the following explanation is only for a rough estimation. The optimization is left to experiments. First of all, the input circuit is regarded as illustrated by the Fig. 4.

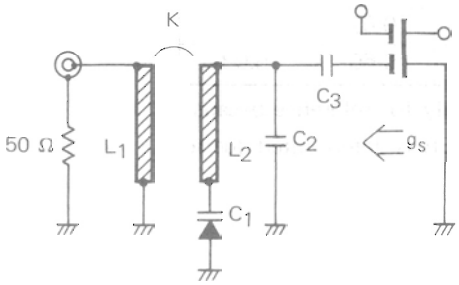


Fig. 4 Input Tuning Circuit

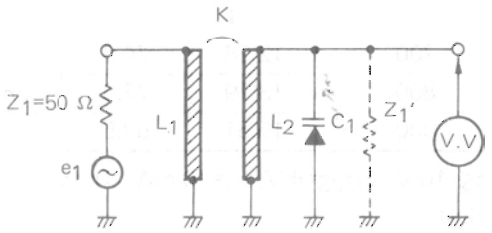
The parameters determining the signal source impedance will be explained and the process how to optimize them for the more matched state will be described.

The signal source impedance seen from FET input can be interpreted in the following sequence.

1) Input terminating 50 Ω resistance (primary side) is transferred to the secondary side through the coupling coefficient K between $L_1$and L_2
2) The impedance transferred on the both ends of L_2 is further modified by varying C_1.
3) The signal source impedance seen from FET input is determined by C_3 and the impedance transferred on the secondary side through processes 1) and 2).

The signal source impedance thus determined through the above mentionned processes will be calculated below in actual figures by entering the actual values of parameters.

First perform a following experiment to know the effect of 1). The circuit shown in Fig. 5, the measurement of Q-characteristics of the secondary tuning circuit with an RF voltmeter (open) on the secondary side by applying voltage on the primary side from a signal generator terminated by a resistance of 50 Ω.



$L_1=L_2$=18 nH, C_1=2~15 pF

Fig. 5 Measurement of Q Characteristics of the Secondary Tuning Circuit

The result is that, the stronger is the coupling of L_1 and L_2 ($K \fallingdotseq 1$), the closer is Z_1' to 50 Ω, and, the weaker the coupling ($K \fallingdotseq 0$), the closer is Z_1' to infinity.

Z_1' is obtained through the Q characteristics of secondary side, namely

$$Q = Z_1'/\omega L = \omega C Z_1' \quad \ldots\ldots\ldots (5)$$

The result of the experiment based on the scheme illustrated above is shown in Fig. 6.

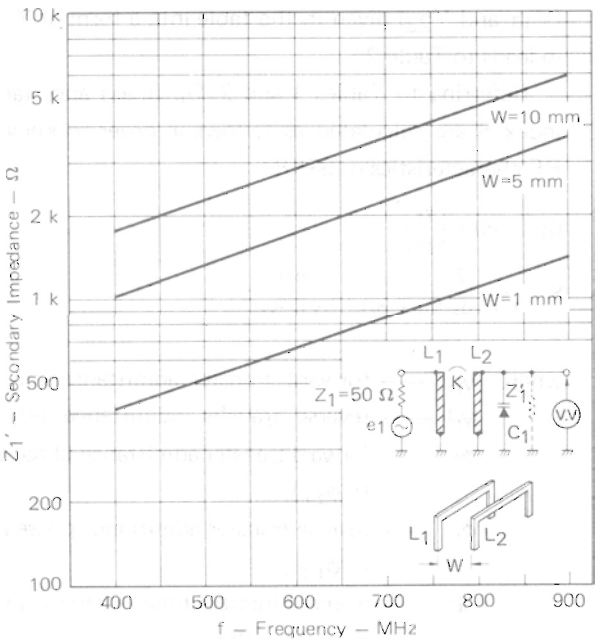


Fig. 6 Secondary Impedance vs. Frequency

According to the figure, the secondary side impedance Z_1' for the $L_1 - L_2$ distance of 1 mm is

530 Ω at 500 MHz and 1 400 Ω at 900 MHz,

whereas the input impedance of the element is

568 Ω at. 500 MHz and 176 Ω at 900 MHz.

That is, even with the $L_1 - L_2$ distance which is as close as 1 mm, no perfect impedance matching is expected since the coupling constant K is only 0.4 as shown in Fig. 7 and the secondary side impedance (signal source impedance) is too high.

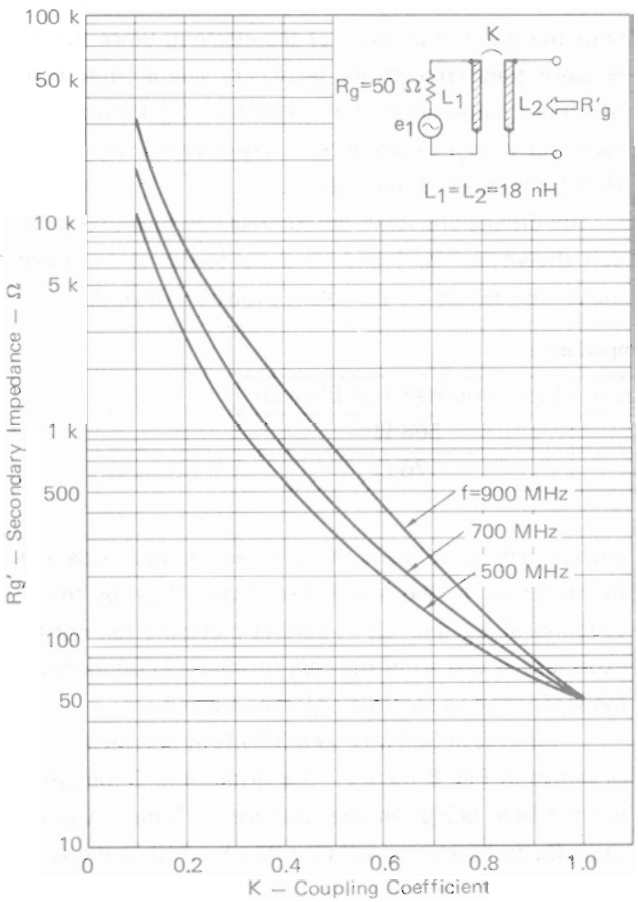


Fig. 7 Secondary Impedance vs. Calculated Coupling Coefficient[note2)]

Note 2)

In a circuit containing a mutual inductance M, the impedance seen from the primary circuit is given by the following formula. (refer to Fig. 8)

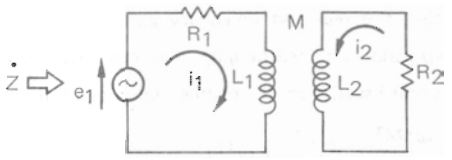


Fig. 8

$$\dot{Z} = \left(R_1 + \frac{\omega^2 M^2}{R_2^2 + \omega^2 L_2^2} \cdot R_2\right) + j\omega\left(L_1 - \frac{\omega^2 M^2}{R_2^2 + \omega^2 L_2^2} L_2\right) \quad \ldots (6)$$

This formula shows that the resistive component of $\dot{Z}$ increases by

$\frac{\omega^2 M^2}{R_2^2 + \omega^2 L_2^2} R_2$ apparently.

The primary circuit is equivalent to one shown in Fig. 9.

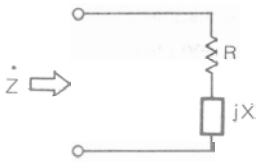


Fig. 9

The circuit shown above is transformed into a parallel circuit and the susceptance component is taken away by tuning. Only component left to be considered is the conductance. Therefore eq. (6) can be interpreted as follows (refer to Fig. 10)

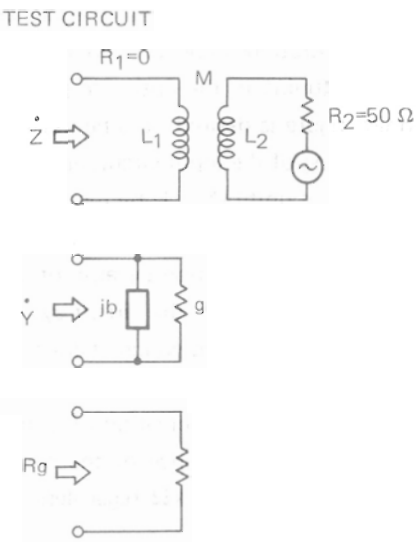


Fig. 10

$$Z = R + jX$$

$$\dot{Y} = \frac{1}{\dot{Z}} = \frac{1}{R + jX} = \frac{R - jX}{R^2 + X^2} = \underbrace{\frac{R}{R^2 + X^2}}_{g} - j\underbrace{\frac{X}{R^2 + X^2}}_{jb}$$

$$R_g = \frac{1}{g} = \frac{R^2 + X^2}{R}$$

Substituting the real and imaginary parts of eq. (6) into the above expression and rearranging, you can find the impedance (real part only) seen from the primary circuit as follows.

$$R_g = \frac{\left(\frac{\omega^2 M^2}{R_2^2 + \omega^2 L_2^2} R_2\right)^2 + \omega^2 \left(L_1 - \frac{\omega^2 M^2}{R_2^2 + \omega^2 L_2^2} L^2\right)^2}{\frac{\omega^2 M^2}{R_2^2 + \omega^2 L_2^2} R_2} \left[\frac{\frac{K^2}{\left(\frac{R_2}{\omega L}\right)^2 + 1} R_2}{}\right]^2 + \omega^2 L^2 \left[1 - \frac{K^2}{\left(\frac{R_2}{\omega L}\right)^2 + 1}\right]^2 \quad \cdots\cdots\cdots\cdots (7)$$

$$\frac{\frac{K^2}{\left(\frac{R_2}{\omega L}\right)^2 + 1} R_2}{}$$

where, $M = K\sqrt{L_1 L_2}$, and because $L_1 = L_2$,

$M = KL$

K is the coupling constant, $-1 \leqq K \leqq 1$.

Fig. 7 is obtained by calculating eq. (7) with the values:

f = 500, 700, and 900 MHz,

L = 18 nH,

R = 50 Ω, and

K = 0.1 – 1.

Therefore, in order to attain a much more matched state, it is necessary to use technique such as the coupling of L_1 and L_2 through a capacitor of 1 pF or so.

As stated before in 2), the impedance transferred to the secondary side is affected by C_1. However, this influence is not substantial because the impedance of C_1 is much less than the transferred impedance. Further step is the determination of the constant of C_3 which acts for the coupling of the transferred impedance of 1) and 2) with the input impedance of the element. Since the impedance transferred to the secondary side is larger than the input impedance of the element, C_3 should be a capacitor with a capacitance of a negligible impedance. Here C_3 is assumed to be 30 pF.

The discussions above are summarized to an input circuit shown in Fig. 1 and its signal source and element input impedances are the values shown in Table 3.

Table 3 Signal Source and Input Impedance

Frequency	Signal Source Impedance	Input Impedance of Element
500 MHz	530 Ω	568 Ω
900 MHz	1400 Ω	176 Ω

Due to mismatching increase with the increase of frequency, the deteriorations in power gain and noise figure result. When the tuning to the optimum point of power gain and noise figure is desired, it is necessary to abandon the M coupling of the input circuit and to make the coupling constant of unity (K = 1) by means of a tap, or, to have the input untuned. But these measures lead to the increase of cross modulation because of decrease in Q of input circuit. Therefore, the circuit system should be determined by considering which characteristic is of the first priority.

The next step is the determination of output circuit constants. The output impedance of the element is, as shown in Table 2, about 1.5 kΩ regardless of RF frequency. The circuitry is the same as the input side and the matching to the load impedance is taken by the M coupling of L_3 and L_4. A perfect matching can not be expected, as was so in the case of input circuit, because the secondary side (across L_3) impedance is

1 350 Ω at 500 MHz and 3.7 kΩ at 900 MHz

as shown in Fig. 6 for $L_3 - L_4$ distance of 5 mm. But, for the time being, let the distance be 5 mm. Also assume C_4 to have a capacitance 30 pF which is the same as in the input circuit.

Table 4 shows the output impedance of the element and the load impedance obtained through the discussions.

Table 4 Load and Output Impedance

Frequency	Load Impedance	Output Impedance of Element
500 MHz	1.35 kΩ	1.33 kΩ
900 MHz	3.7 kΩ	1.67 kΩ

3. CHARACTERISTICS OF UHF RF AMPLIFIERS USING 3SK87

3.1 Power Gain

Fig. 11 shows the Gps to frequency characteristics. According to the figure, the power gain is 14.5 dB at 500 MHz and 11.4 dB at 900 MHz, namely, the amplifier has a flat and high power gain.

Although the maximum available power gain Gps (max) of 3SK87 is, as described above, 20.8 dB at 500 MHz and 18.4 dB at 900 MNz, it cannot be reached because the actual circuit is operated in an unmatched condition for an increased circuit stability.

The realized power gain in the unmatched state will be calculated below.

$$Gps = \frac{4 \cdot |y_{fs}|^2 \cdot g_S g_L}{(g_S + g_i)^2 (g_L + g_o)^2} \quad \cdots\cdots\cdots (8)$$

Where g_S and g_L are signal source and load conductances. The values obtained in Sec. 2–1 are:

$|y_{fs}|$ = 25.08 mS,
g_S = 1.89 mS (Ri = 530 Ω),
g_i = 1.76 mS (Ri = 568 Ω),
g_L = 0.74 mS (R_L = 1.35 kΩ), and
g_o = 0.75 mS (Ro = 1.33 kΩ) at 500 MHz, and,
$|y_{fs}|$ = 30.53 mS,
g_S = 0.71 mS (Rs = 1 400 Ω),
g_i = 5.68 mS (Ri = 176 Ω),
g_L = 0.27 mS (R_L = 3.7 kΩ), and
g_o = 0.59 mS (Ro = 1.67 kΩ) at 900 MHz.

The power gain is calculated through eq. (8) as

$$Gps = \frac{4 \cdot 25.08^2 \cdot 1.89 \cdot 0.74}{(1.89 + 1.76)^2 \cdot (0.74 + 0.75)^2} = 119 \ (20.75 \text{ dB})$$

at 500 MHz, and,

$$Gps = \frac{4 \cdot 30.53^2 \cdot 0.71 \cdot 0.27}{(0.71 + 5.68)^2 \cdot (0.27 + 0.59)^2} = 23.67 \ (13.7 \text{ dB})$$

at 900 MHz. The values above demonstrate the power gain decrease in higher frequency region because of increased mismatching.

The power gain obtained through eq. (8) does not take into account of the losses of input/output coupling circuits and the loss due to the insertion of variable capacitance diode. Hence, the actual power gain is further reduced.

The resultant is shown in Fig. 11.

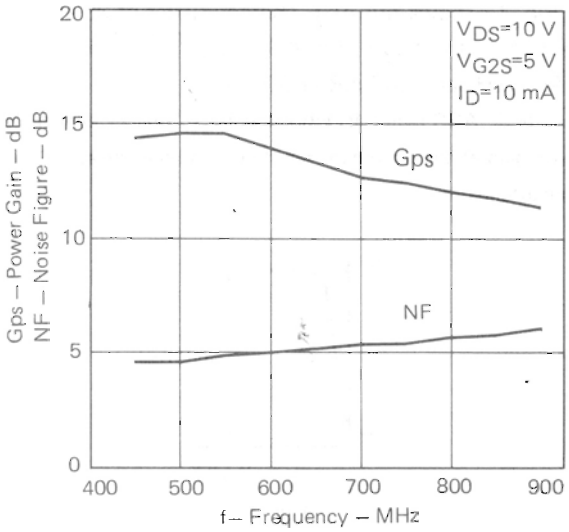


Fig. 11 Power Gain and Noise Figure vs. Frequency

3.2 AGC Characteristics

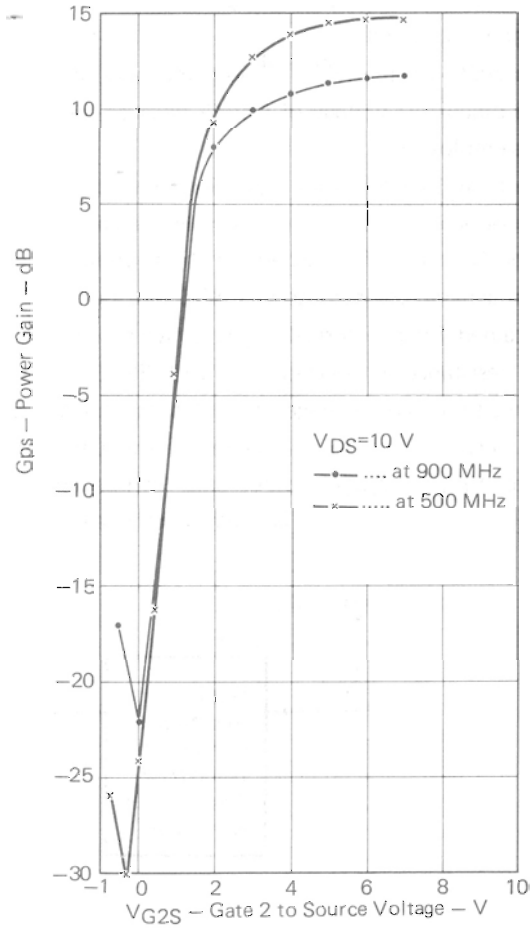


Fig. 12 Power Gain vs. Gate 2 to Source Voltage

Fig. 12 shows the AGC characteristics of 3SK87. According to the figure, the AGC range[note 3] is 33.4 dB at 900 MHz and 44.5 dB at 500 MHz.

note 3) AGC region is defined as the difference between the power gain at the maximum sensitivity and the one at the maximum attenuation.

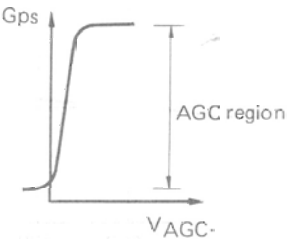


Fig. 13

The region is usually reduced with the incerase of frequency due to the increase in feedback component. However, since a dual gate configuration is adopted and the feedback capacitance is very small, the large AGC region can be obtained.

The AGC sensitivity[note 4] is principally dependent on the pinch—off voltage of Gate 2 because the reverse AGC is employed.

note 4) AGC sensitivity is a parameter compared by the control voltage necessary for obtaining a certain attenuation.

In an N-channel FET where pinch-off voltage is negative in general, the satisfactory AGC sensitivity cannot be obtained for a practical V_{G2S} (V_{AGC}) range if no source resistance is inserted. But, with 3SK87 having a very small pinch-off voltage of −0.4 V typical, the control is performed up to the maximum attenuation with positive V_{G2S} (V_{AGC}) only, and, consequently no source resistance insertion is needed practically. This is noe of the features of 3SK87.

3.3 Noise Figure

The noise figure of RF amplifier is given by the following formula by A. vander Ziel

$$NF = 10 \log \left[1 + \frac{g_i}{g_s} + \frac{R_n}{g_s} (g_s + g_i)^2 \right], \quad \cdots\cdots\cdots\cdots\cdots (9)$$

where Rn is the equivalent noise resistance of the element.

For example, when the matching is taken at the input and put $g_s = g_i$, then eq. (9) gives

$$NF = 10 \log (2 + 4 g_i R_n), \quad \cdots\cdots\cdots\cdots\cdots (10)$$

that means that even if the noise of the element is zero,

$$NF = 10 \log 2 = 3 \text{ dB}.$$

Therefore, the necessary condition of signal source conductance for NF_{OPT} is $g_s > g_i$, which is inconsistent with the condition for getting G_{PS} (max).

Fig. 11 shows the NF versus frequency characteristics. According to the curve, NF is 4.6 dB at 500 MHz and 6.0 dB at 900 MHz,
showing the deterioration with the increasing frequency. This is caused by the increased mismatching between the signal source conductance and the input conductance of element in the higher frequency region. The conductances are:

$g_s = 1.89$ mS (530 Ω) $> g_i = 1.76$ mS (568 Ω) at 500 MHz, and,
$g_s = 0.71$ mS (1 400 Ω) $< g_i = 5.68$ mS (176 Ω) at 900 MHz.

At 500 MHz, the condition $g_s > g_i$ is fulfilled and the NF matching is well maintained, but, at 900 MHz, the relationship is shifted to $g_s < g_i$ and NF becomes larger than 3 dB even if the noise of the element is nore.

Based upon the above analysis, NF of a tuner set using 3SK87 for the RF amplifier is estimated Fig. 14.

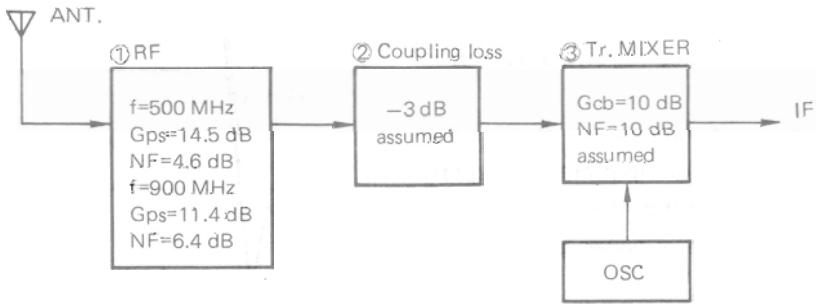


Fig. 14 Gain and Noise Figure Distribution

$$NF_{TOTAL} = 10 \log \left(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}\right) \quad \cdots\cdots\cdots\cdots (11)$$

at 500 MHz,

$$NF_{TOTAL} = 10 \log \left(2.88 + \frac{2-1}{28.2} + \frac{10-1}{28.2 \times 0.5}\right) = 5.5 \text{ dB}$$

and, at 900 MHz,

$$NF_{TOTAL} = 10 \log \left(3.98 + \frac{2-1}{13.8} + \frac{10-1}{13.8 \times 0.5}\right) = 7.3 \text{ dB}.$$

3.4 Cross Modulation

Fig. 15 shows the cross modulation characteristics. Because of the quasisquare transfer characteristics inherent to FET's, the cross modulation characteristics at small AGC levels are much improved from those of bipolar transistors.

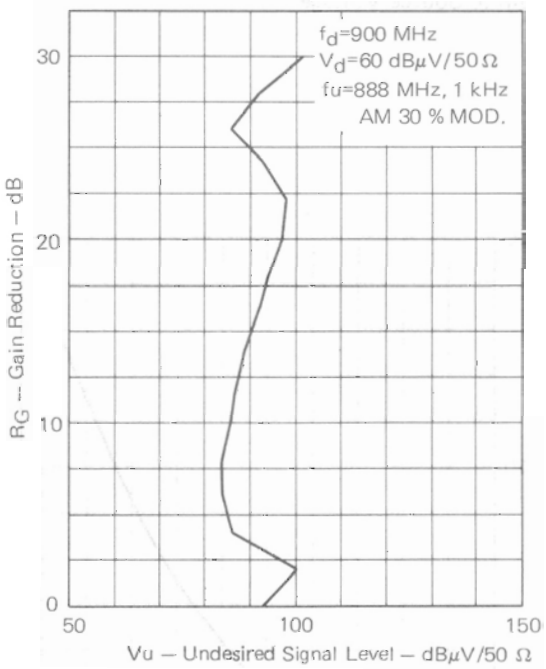


Fig. 15 1 % Cross Modulation

Since the transfer characteristics are remote-cutoff by virtue of a dual gate structure, the cross modulation is not deteriorated when AGC is increased.

The cross modulation characteristics of 3SK87 are:

- at full gain, interfering signal level is 93 dBμV/50 Ω, and,
- at 30 dB attenuation, interfering signal level is 102 dBμV/50 Ω.

3.5 Characteristics of UHF Tuner RF Amplifier Using 3SK87.

The characteristics discussed in Sections up to 3–4 are summarized as follows for the 3SK87 circuit shown in Fig. 1.

- Power Gain: Gps — 14.5 dB at 500 MHz; 11.4 dB at 900 MHz
- Noise Figure: NF — 4.6 dB at 500 MHz; 6.0 dB at 900 MHz
- AGC Region — 44.5 dB at 500 MHz; 33.4 dB at 900 MHz
- Crossmodulation — 93 dBμV/50 Ω at fullgain, 102 dBμV/50 Ω at 30 dB attenuation, for desired frequency of 900 MHz and undesired frequency of 912 MHz.

4. REFERENCE

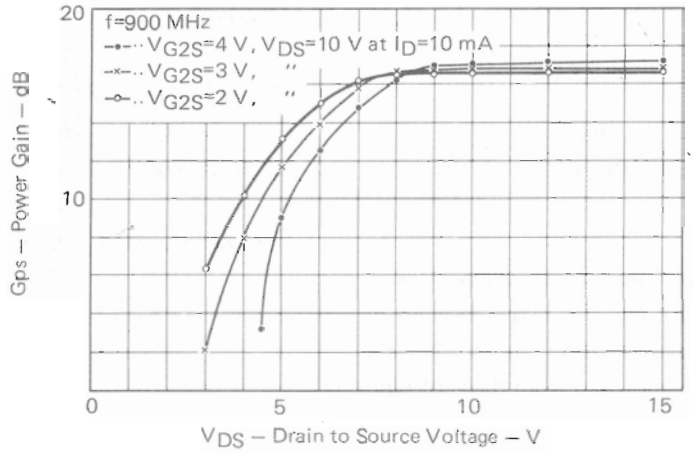


Fig. 16 Power Gain vs. Drain to Source Voltage

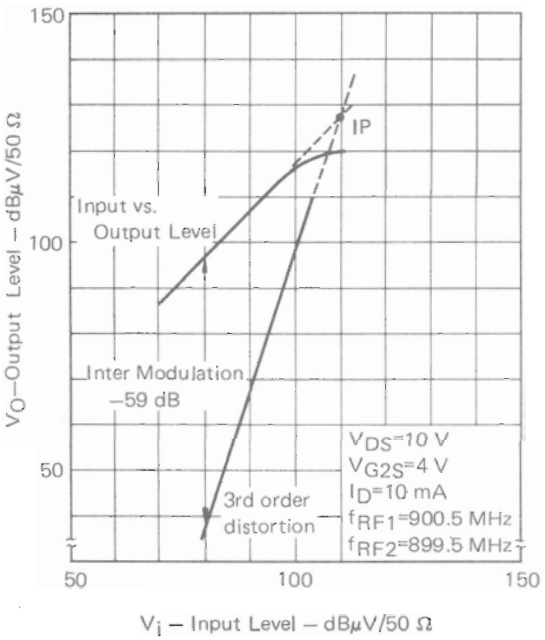


Fig. 17 Intercept Point

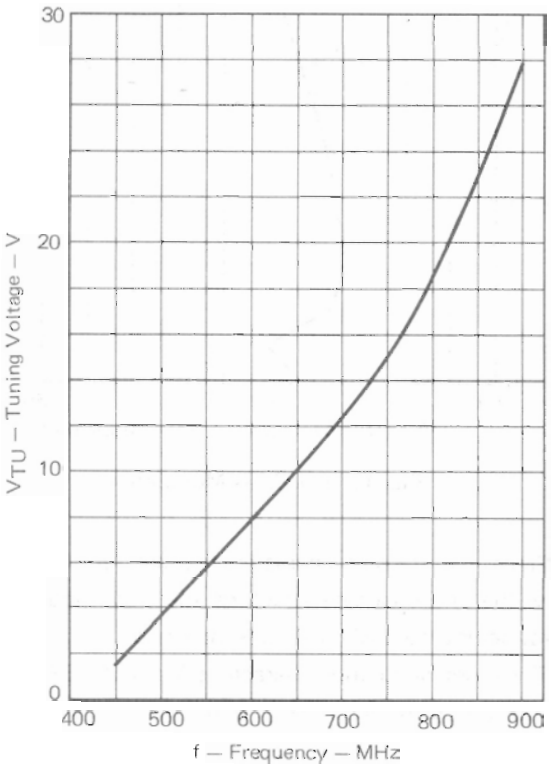


Fig. 18 Tuning Curve due to Fig. 1.

TYPICAL APPLICATION OF 3SK88 TO UHF TUNER RF AMPLIFIER

1. GENERALS

3SK88 is an N-Channel MOS field effect transistor developed principally for RF amplifier of UHF TV tuner. Its features include a very small feedback capacitance Crss (0.02 pF, typically) because of a dual gate structure and a large y_{fs} / y_{rs} because of a large g_m, and, hence it can be operated very stably with a high power gain (Gps).

Furthermore, it has a small input capacitance that enables it to have excellent characteristics even for a wider frequency bandwidth (as in U.S.A.).

The following description will explain the characteristics of 3SK88 applied to RF amplifier of UHF TV tuner.

2. APPLICATION TO UHF TUNER RF AMPLIFIER

2.1 Typical Design of UHF Tuner RF Amplifier

There are two types of RF amplifier circuit system of UHF tuner, one is λ/2 distributed — constant tuning and the other is λ/4 distributed — constant tuning. This document deals with experiments on an electronic tuning type employing the λ/4 distributed — constant tuning system which is relatively susceptible to the influence of Ciss of element. The circuitry is shown in Fig. 1.

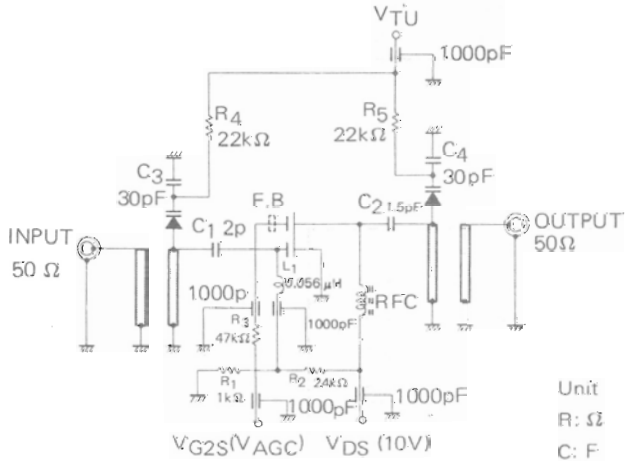


Fig. 1 Test Circuit

The biasing condition is determined through Fig.2, the static characteristics of 3SK88.

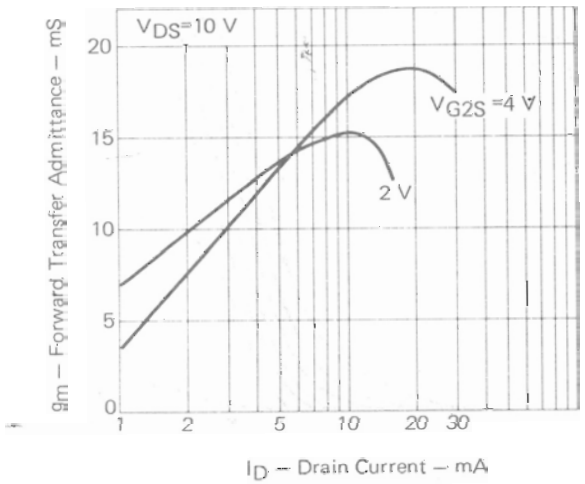


Fig. 2 Forward Transfer Admittance vs. Drain Current

When $V_{G2S}(V_{AGC})$ = 4 V (full gain) is assumed, I_D for which g_m is the maximum is 20 mA. Since this value leads to too much power consumption, I_D is set to about 10 mA. (When V_{G2S} = 2 V, I_D for the maximum g_m is 10 mA.) V_{DD} is set to 10 V.

The value of V_{G1S} for obtaining I_D of 10 mA is about 0.4 V as shown in Fig. 3 when V_{G2S}=4 V.[note 1] The resulted biasing circuit resistances are

R_1 = 1 kΩ, R_2 = 24 kΩ, and R_3 = 47 kΩ.

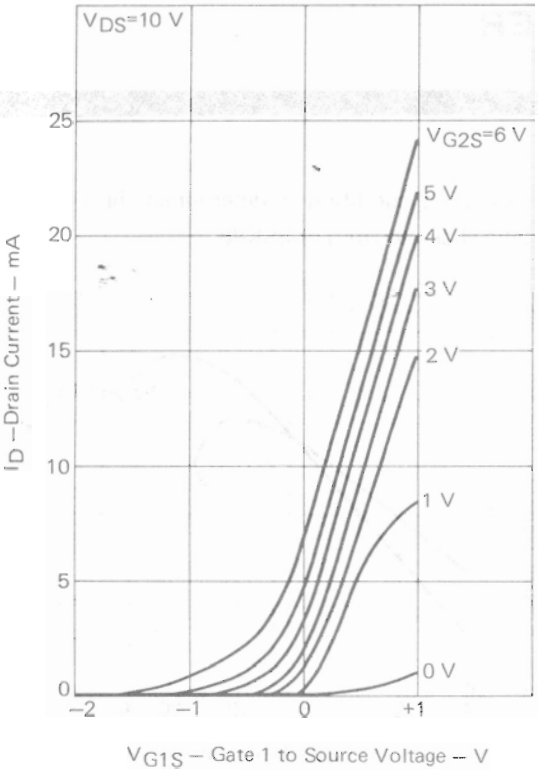


Fig. 3 Drain Current vs. Gate 1 to Source Voltage

note 1) Fig.3 shown the measured values with products whose typical I_{DSS} is 3 mA.

Since the resistances also serve to protect Gates 1 and 2, it is safe to use as large resistances as possible.

Next step is the acquisition of reference data for the introduction of constants from element's y-parameter. The y-parameter of the elements is as shown below.

The input / output admittances (Y11, Y22) in Table 1 are converted to the form of y = g + jb and shown in Table 2.

Based on Tables 1 and 2, Gps(max) and stability index of 3SK88 are calculated as follows for the information of RF characteristics of the FET.

$$Gps = \frac{|y_f|^2}{4g_i g_o} \quad (1)$$

$$S = \frac{2}{1 + \cos(\phi_f + \phi_r)} \cdot \frac{g_i g_o}{|y_s||y_r|}, \quad (2)$$

where, $|y_f|$ ——— forward transfer admittance (= $|y_{21}|$),
$|y_r|$ ——— reverse transfer admittance (= $|y_{12}|$),
$|\phi_f|$ ——— forward transfer admittance phase angle (= ϕ_{21}),

Table 1 Y-Parameter of A 3SK88

freq. (MHz)	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
	$\|y_{11}\|$(mS)	$\angle\phi_{11}$(deg.)	$\|y_{21}\|$(mS)	$\angle\phi_{21}$(deg.)	$\|y_{12}\|$(mS)	$\angle\phi_{12}$(deg.)	$\|y_{22}\|$(mS)	$\angle\phi_{22}$(deg.)
400	5.735	81.5	18.023	−22.7	0.021	−64.5	2.263	77.2
500	7.333	79.9	18.502	−28.0	0.029	−25.5	2.823	76.6
600	8.926	78.6	19.303	−33.0	0.048	4.4	3.387	76.5
700	10.496	76.8	20.046	−38.9	0.087	21.7	3.866	76.7
800	11.948	74.5	20.864	−46.2	0.128	29.4	4.141	77.3
900	13.622	70.5	22.091	−54.8	0.185	36.1	4.574	77.7

Conditions: V_{DS}=10 V, V_{GS}=4.0 V, I_D=10 mA
The values are measured on the products whose $|y_{21}|$ are typical.

Table 2 Y-Parameter of A 3SK88

freq. (MHz)	Y_{11}		Y_{22}	
	g_{11} (mS)	b_{11} (mS)	g_{22} (mS)	b_{22} (mS)
400	0.85	5.67	0.50	2.21
500	1.29	7.22	0.65	2.75
600	1.76	8.75	0.79	3.29
700	2.40	10.22	0.89	3.76
800	3.19	11.51	0.91	4.04
900	4.55	12.84	0.97	4.47

$|\phi_r|$ ——— reverse transfer admittance phase angle ($=\phi_{12}$),

$|g_i|$ ——— input conductance ($=g_{11}$), and

$|g_o|$ ——— output conductance (g_{22}).

From eq. (1), at 900 MHz,

$$Gps\ (max) = \frac{22.091^2}{4 \times 4.55 \times 0.97} = 27.6\ (14.4\ dB),$$

and from eq. (2),

$$S = \frac{2}{1 + \cos(-54.8 + 36.1)} \cdot \frac{4.55 \times 0.97}{22.091 \times 0.185} = 1.11$$

(Because $S \geqq 1$, the performance is stable regardless of the input / output matching condition.) Similarly at 500 MHz,

$$Gps\ (max) = \frac{18.502^2}{4 \times 1.29 \times 0.65} = 102.06\ (20.1\ dB),$$

and

$$S = \frac{2}{1 + \cos\{-28.0 + (-25.5)\}} \cdot \frac{1.29 \times 0.65}{18.502 \times 0.029} = 1.96$$

Also, in this case, $S \geqq 1$ is fulfilled and the performance is stable regardless of the input / output matching condition. The high G_{ps} operation is also shown.

The determination of input / output matching circuit constants based on these data will be explained by an example. Table 2 tells that the element input / output impedances are, at 900 MHz,

$$R_i = \frac{1}{g_i} = \frac{1}{4.55 \times 10^{-3}} = 220\ \Omega \text{ and } R_o = \frac{1}{g_o} = \frac{1}{0.97 \times 10^{-3}} = 1\,030\ \Omega,$$

and, at 500 MHz,

$$R_i = \frac{1}{g_i} = \frac{1}{1.29 \times 10^{-3}} = 775\ \Omega \text{ and } R_o = \frac{1}{g_o} = \frac{1}{0.65 \times 10^{-3}} = 1\,538\ \Omega.$$

The capacitances of input / output coupling capacitors C_1 and C_2 shown in Fig. 1 are determined using the above mentioned impedance values.

The input circuit can be interpreted by Fig. 4. The impedance of signal source and element input impedance are matched through C_1. Too large a value of C_1 is unfavorable because the series capacitance of C_1 and of element input capacitance is inserted parallel to the variable capacitance diode and limits the variable frequency range.

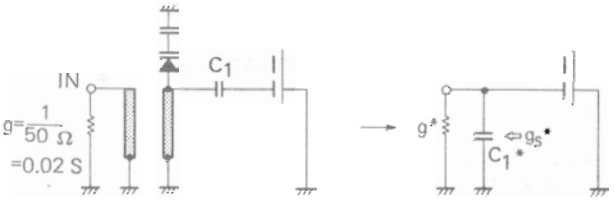


Fig. 4 Equivalent Input Circuit

Assume C_1=2 pF. The signal source conductance at 900 MHz is

$$g_s^* = \frac{(\omega c)^2}{g^2 + (\omega c)^2} \cdot g \qquad \text{note 2)}$$

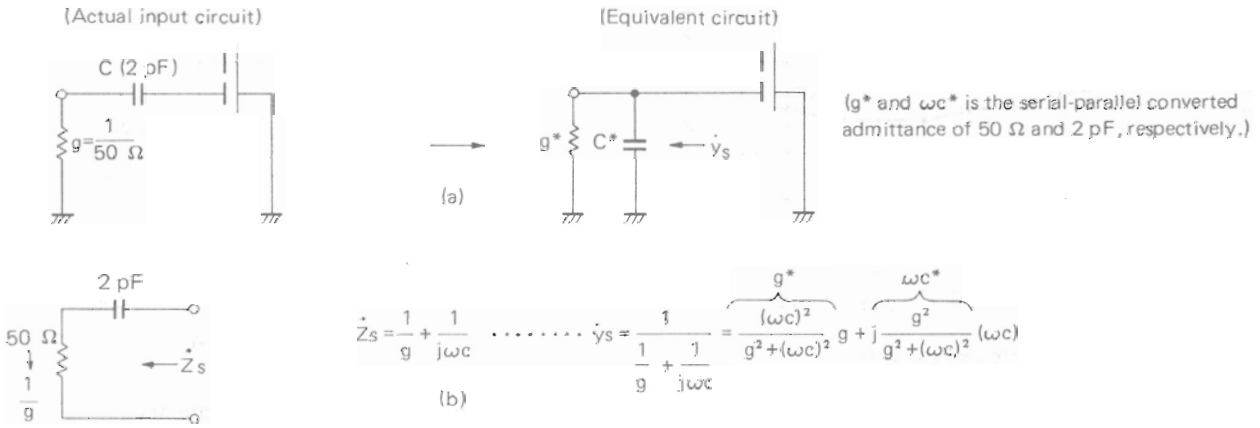
$$= \frac{(2\times\pi\times900\times10^6\times2\times10^{-12})^2}{(0.02)^2 + (2\times\pi\times900\times10^6\times2\times10^{-12})^2} \times 0.02$$

$$= 4.85\ mS\ (R_S = 206.25\ \Omega).$$

note 2) Signal source and lead conductances are calculated in Fig. 5.

The real part g^* of the formula is used to calculate signal source conductance. In a similar way, load conductance is calculated.

This signal source conductance is nearly matched to the input conductance. Similarly, the signal source con-



$$\dot{Z}_S = \frac{1}{g} + \frac{1}{j\omega c} \quad \cdots\cdots \quad \dot{y}_S = \frac{1}{\frac{1}{g} + \frac{1}{j\omega c}} = \frac{\overbrace{g}^{g^*}}{\underbrace{g^2 + (\omega c)^2}} + j\frac{\overbrace{\omega c}^{\omega c^*}}{\underbrace{g^2 + (\omega c)^2}}$$

Fig. 5 Equivalent Circuit

ductance at 500 MHz is 1.8 mS (R_S = 556 Ω), and the element input conductance is 1.29 mS (R_i = 775 Ω).

The output circuit is interpreted Fig. 6

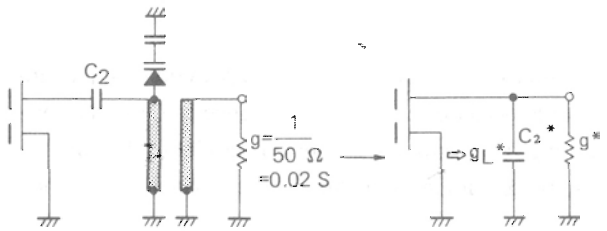


Fig. 6 Equivalent Output Circuit

The load conductance at 900 MHz is, for C_2 of 1.5 pF,

$$g_L^* = \frac{(\omega c)^2}{g^2 \times (\omega c)^2} \cdot g$$

$$= \frac{(2 \times \pi \times 900 \times 10^6 \times 1.5 \times 10^{-12})^2}{(0.02)^2 \times (2 \times \pi \times 900 \times 10^6 \times 1.5 \times 10^{-12})^2} \times 0.02$$

$$= 3.05 \text{ mS} (R_L = 328 \ \Omega).$$

The element output conductance is 0.97 mS (R_O = 1 030 Ω). Similarly, at 500 MHz, the load conductance is 1.05 mS (R_L = 951 Ω) and the element output conductance is 0.65 mS (R_O = 1 538 Ω).

The capacitances of the input / output capacitors C_1 and C_2 has been thus calculated. The optimization of the values are left to experiments.

2.2 Characteristics of UHF Tuner RF Amplifier Using 3SK88

Fig. 7 shows the Gps and NF vs. frequency characteristics, which tells that Gps is 15 dB and 12 dB at 900 MHz and at 500 MHz respectively.

The power gain is flat and high.

This characteristics is obtained when L_1 is inserted in the Gate 1 on the circuit shown in Fig. 1 The characteristics variation with L_1 is shown in Fig. 8. Without L_1 inserted, Gps is so low that it is 14.5 dB at 900 MHz and 7 dB at 500 MHz.

The cause of the characteristics deterioration is that the variation of inter terminal capacitance of the variable capacitance diode is much more than the variation of frequency. When the characteristics at 900 MHz and at 500 MHz are compared, the inter terminal capacitance of the variable capacitor diode at 500 MHz is too large and the Q-depression as well as the insertion loss increase are resulted[note 3]. The weakening of coupling due to the impedance decrease in input / output coupling L's can be included in the causes.

note 3) Unloaded Q of variable capacitance diode is calculated as follows.

$$Q = \frac{1}{\omega c r_s}$$

Assume that r_s = 0.5 Ω and inter terminal capacitance is 2.5 pF and 11 pF at 900 MHz and at 500 MHz, respectively. The unloaded Q at 900 MHz is, through the

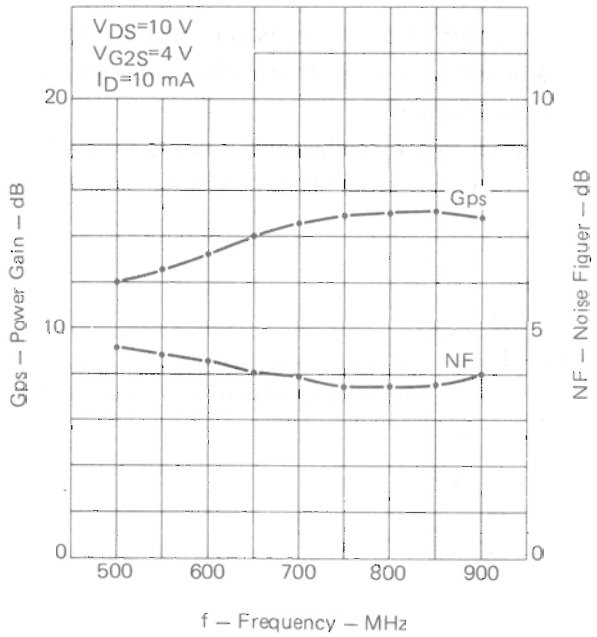


Fig. 7 Power Gain and Noise Figuer vs. Frequency

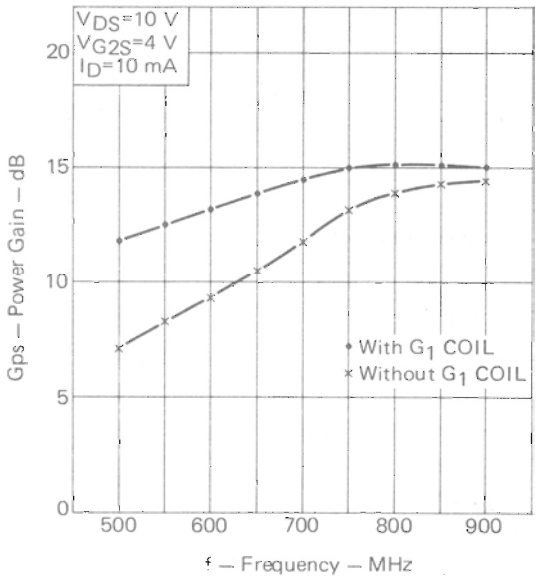


Fig. 8 Power Gain vs. Frequency

formula given above,

$$Q = \frac{1}{2\times\pi\times900\times10^{6}\times2.5\times10^{-12}\times0.5} \fallingdotseq 141,$$

and, at 500 MHz,

$$Q = \frac{1}{2\times\pi\times500\times10^{6}\times11\times10^{-12}\times0.5} \fallingdotseq 58$$

L_1 is inserted for the compensation. The role of L_1 is the power gain boost due to the parallel resonance produced by L_1 and the input capacitance, by utilizing the capacitive input admittance of the element used source grounded.

The resonance frequency is calculated below. The input capacitance of the element C_{iss} is calculated, by using b_{11} value of 7.22 mS as indicated in Table 2,

$$\frac{b_{11}}{\omega} = \frac{7.22\times10^{-3}}{2\times\pi\times500\times10^{6}} = 2.3 \text{ pF}.$$

With L_1 of 0.056 μH, the resonance frequency is

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.056\times10^{-6}\times2.3\times10^{-12}}} = 443 \text{ MHz}.$$

Fig. 9 shows the AGC characteristics of 3SK88. According to the figure, the AGC range at 900 MHz is about 41 dB[note 4], and at 500 MHz, it is about 46 dB. These values show that the small feedback capacitance by virtue of the dual gate structure is effective for obtaining a large AGC range.

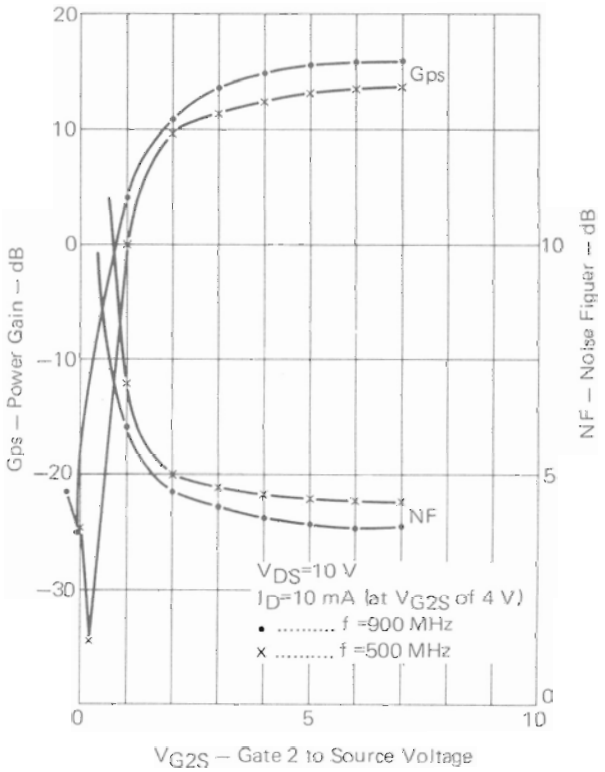


Fig. 9 Power Gain and Noise Figuer vs. Gate 2 to Source Voltage

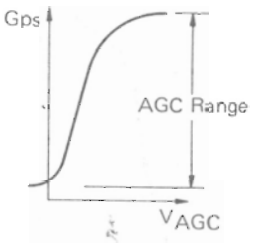


Fig. 10 Power Gain vs. Automatic Gain Control

note 4) AGC range is difference of power gain at the maximum sensitivity are one at the maximum attenuation.

The AGC sensitivity[note 5] is almost determined by the pinch-off voltage of Gate 2 because reverse AGC system is applied. The insertion of a source resistance can raise the AGC sensitivity within a practical V_{G2} (V_{AGC}) range.

note 5) AGC sensitivity is a parameter which will be compared with each other in the control voltages needed to obtain a certain attenuation.

However, the AGC sensitivity enhancement within a practical V_{G2S} (V_{AGC}) range by inserting a source resistance is really unnecessary because the typical Gate 2 pinch-off voltage V_{G2S}(off) is as small as −0.1 V and the gain control almost up to the maximum attenuation can be performed with only positive V_{G2S}(V_{AGC}) as shown in Fig. 9. This is one of features of 3SK88.
As shown in the G_{ps} and NF vs. Frequency characteristics of Fig. 7, NF is considerably small as 4 dB and 4.5 dB at 900 MHz and 500 MHz, respectively.

Generally, the condition for the NF minimum is $g_s > g_i$. This condition does not coincide with the power gain matching condition. (The G_{ps} values in Fig. 4 are those when NF is minimum.) The relationship between g_s and g_i is the same as before. The conductances are:

g_s = 4.85 mS (Rs = 206 Ω) and g_i = 4.55 mS (R_i = 220 Ω) at 900 MHz, and

g_s = 1.8 mS (Rs = 556 Ω) and g_i = 1.29 mS (R_i = 775 Ω) at 500 MHz.

Fig. 11 shows the cross modulation of 3SK88.

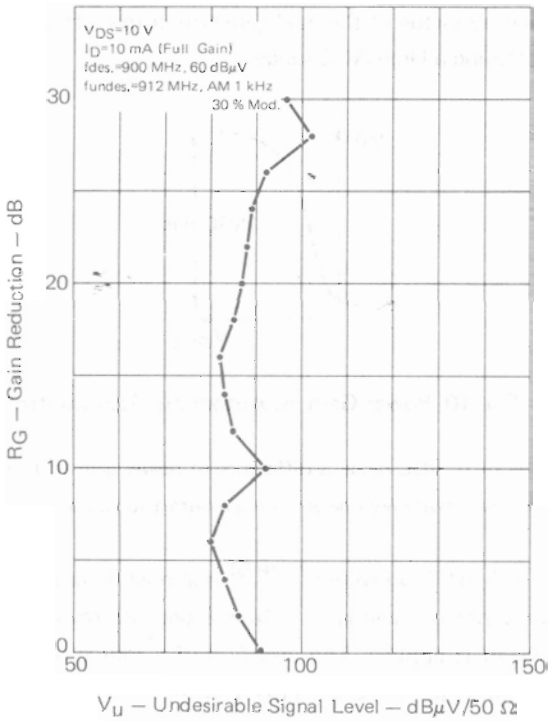


Fig. 11 1 % Cross Modulation

Being an FET, it has quasi-square transfer characteristic. Therefore its cross modulation is largely reduced at a small AGC voltage, compared with bipolar transistors.

Furthermore, because of dual gate structure and the resulted remote cutoff transfer characteristics, the cross modulation is not deteriorated even when AGC voltage is large.

The cross modulation of 3SK88 is such that at full gain, undesired signal level is 91 dBμV / 50 Ω, and at 30 dB attenuation, undesired signal level is 97 dBμV/50 Ω.

2.3 Characteristics of UHF Tuner RF Amplifier Using 3SK88

The above mentioned characteristics obtained when 3SK88 is used in the circuit shown in Fig. 1 are summarrized as:

- Power Gain (Gps) ——— 14.8 dB
- Noise Figure (NF)——— 4 dB } at 900 MHz,
- AGC Range ——————— 41 dB
- Cross Modulation——— at full gain, 91 dBμV/50 Ω
  at 30 dB attenuation,
  97 dBμV/50 Ω

for $f_{des.}$ =900 MHz
$f_{undes.}$ =912 MHz, modulated 30 % by AM with 1 kHz.

TYPICAL APPLICATION OF 2SC2352 TO VHF TUNER MIXER CIRCUIT OF HIGH CONVERSION GAIN

1. GENERALS

2SC2352 is an NPN epitaxial silicon transistor developed principally for VHF tuner mixer.

Its features include a stable performance due to small feedback capacitance (0.4 pF, typically), a high conversion power gain and a low third order distortion.

This document will describe the experimental results about the variations of characteristics (such as conversion gain, noise figure, and intermodulation) essential to MIX with the impedance matching condition and the biasing condition, and the design and the characteristics of 2SC2352 application circuit as a VHF tuner MIX with a good overall performance.

2. TRANSISTOR MIX

A transistor MIX works on the principle that, when an oscillation voltage v_O and a signal voltage v_S with different frequencies to each other are applied to a nonlinear circuit at the same time, the input conductance is periodically varied by v_O and signals with the sum and the difference frequencies of the both input frequencies.

The circuit configuration of the MIX using 2SC2352 is an emitter grounded and base injection type. The performance is illustrated by Fig. 1.

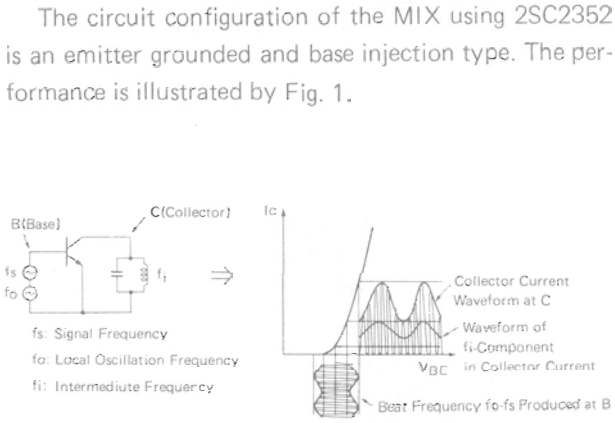
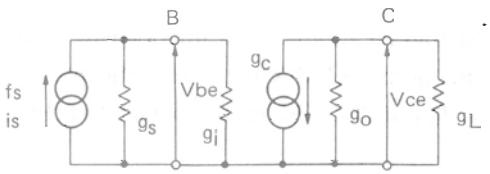


Fig. 1 Operating Principle of Mixer

3. APPLICATION OF 2SC2352 TO MIX

3.1 Conversion Power Gain



g_S: Signal Source Conductance g_i: Input Conductance
g_L: Load Conductance g_o: Output Conductance
g_C: Conversion Conductance g_m: Mutual Conductance

Fig. 2 Equivalent Circuit of Mixer

A MIX is usually represented with the above equivalent circuit (refer to Fig. 2). The conversion gain (Gc) under the condition $g_i=g_S$ and $g_o=g_L$ is given by the formula below.

$$Gc\ max = \frac{g_C{}^2}{4g_i g_o} \qquad (1)$$

If the circuit is unmatched,

$$Gc = \frac{4g_C{}^2 g_S g_L}{(g_i+g_S)^2 (g_o+g_L)^2} \qquad (2)$$

If the above formulas, g_C is the conversion conductance and is related to g_m as

$g_C = K \cdot g_m$,

where K is an proportion coefficient dependent on the local oscillation voltage and takes a volue $K \leqq \frac{1}{2}$.

The Gce of 2SC2352 is estimated as follows by calculating with y-parameter (refer to Table-1).

Table 1 Y-Parameters of A 2SC2352

	Y_{ie}		Y_{fe}		Y_{re}		Y_{oe}	
Measured value	$\lvert y_{ie}\rvert$(mS)	ϕ_{ie}(deg.)	$\lvert y_{fe}\rvert$(mS)	ϕ_{fe}(deg.)	$\lvert y_{re}\rvert$(mS)	ϕ_{re}(deg.)	$\lvert y_{oe}\rvert$(mS)	ϕ_{oe}(deg.)
	21.29	60.8	88.0	−37.0	0.40	−83.5	2.12	83.5
Converted value	g_{ie} (mS)	b_{ie} (mS)	g_{fe} (mS)	b_{fe} (mS)	g_{re} (mS)	b_{re} (mS)	g_{oe} (mS)	b_{oe} (mS)
	10.39	18.58	70.28	−52.96	0.05	−0.40	0.24	2.11

Test Condition: V_{CE}=10 V, I_E=−3.0 mA, f=200 MHz

The Y-parameters are obtained with the transistors having typical Y_{fe} value.

The point to be marked is that the output conductance g_o should be a value at the intermediate frequency because the output of MIX is tuned to the intermediate frequency (g_o of 2SC2352 is approximately 0.15 mS at 50 MHz.).

From eq. (1),

$$G_c \max = \frac{g_c^2}{4g_i g_o} = \frac{44^2}{4 \times 10.39 \times 0.15} = 310.6\ (\fallingdotseq 24.9\ \text{dB}),$$

where g_c is assumed to be 1/2 g_m. Similarly the power gain at RF is

$$G_p \max = \frac{|y_f|^2}{4g_i g_o} = \frac{88^2}{4 \times 10.39 \times 0.24} = 776.4\ (=28.9\ \text{dB}).$$

This means that, provided that $g_c = \frac{1}{2} g_m$, Gc would fall to 1/4 of Gp at RF. (776.4/4=194.1 ——22.9 dB). But, actually, since the output is tuned to the intermediate frequency and the output impedance is raised, the simple reduction to 1/4 does not take place.

Fig. 3 shows the Gce to local level characteristics for varied signal source impedance (varied by the input capacitance).

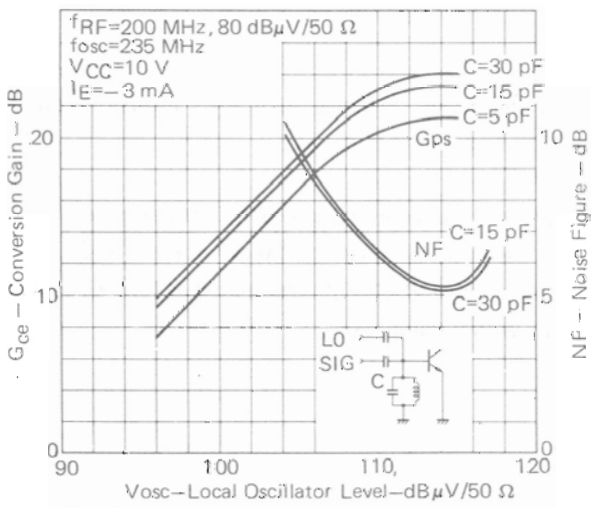


Fig. 3 Conversion Gain And Noise Figure vs. Local Oscillator Level

According to the Fig. 3, Gce takes the maximum value at 115 dBμV/50 Ω (in SG output level) and it is 24 dB at C=30 pF (Rs=64 Ω)[note 1]. The impedance matching condition then is;

signal source impedance ——— 64 Ω,

input impedance of element —— 96 Ω,

load impedance ———————— 2.1 kΩ[note1], and

output impedance of element —— 4.2 kΩ.

The input is nearly matched but the output is mismatched to obtain a wide bandwidth. (B.W. = 15 MHz)

note 1) Signal source and load impedances are calculated as Fig.4 and Fig.5.

$$\dot{Z}_S = \frac{1}{g} + \frac{1}{j\omega c}$$

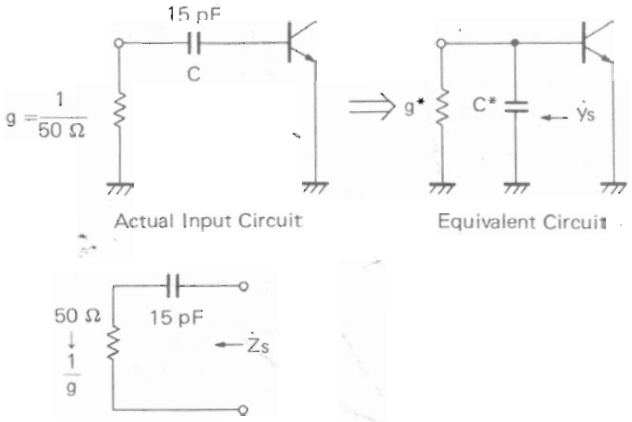
$$\dot{Y}_S = \frac{1}{\frac{1}{g} + \frac{1}{j\omega c}} = \overbrace{\frac{(\omega c)^2}{g^2 + (\omega c)^2}}^{g^*} g + j \overbrace{\frac{g^2}{g^2 + (\omega c)^2}}^{\omega c^*} \omega c$$

By using the real part (g*) of the formula, and calculating the signal source conductance of the actual input circuit,

$$\frac{(\omega c)^2}{g^2 + (\omega c)^2}\ g = \frac{g}{1 + \left(\frac{g}{\omega c}\right)^2}$$

$$= \frac{20 \times 10^{-3}}{1 + \left(\frac{20 \times 10^{-3}}{2\pi \times 200 \times 10^6 \times 15 \times 10^{-12}}\right)^2}$$

= 9.4 mS (Rs = 106 Ω)



g* and ωC^* are the serial-parallel transformed

Fig. 4 Equivalent Circuit

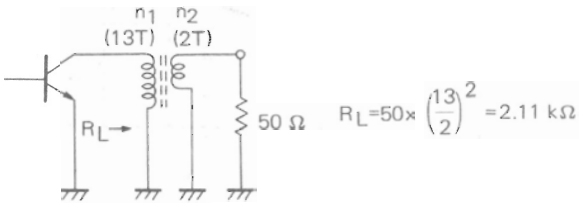


Fig. 5 Actual Output Circuit

Fig.6 is the biasing dependency of Gce (Gce vs. I_E), and G_{ce} is the largest at I_E of about 5 mA.

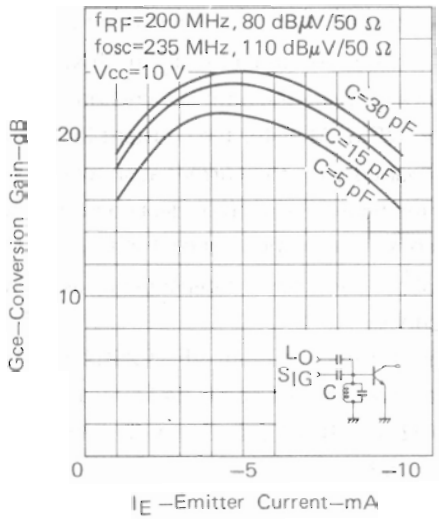


Fig. 6 Conversion Gain vs. Emitter Current

3.2 Noise Figure

Using the equivalent circuit as 2SC2352, it is estimated the noise figure (NF) in RF and MIX. Fig. 7 shows the equivalent circuit as noise model.

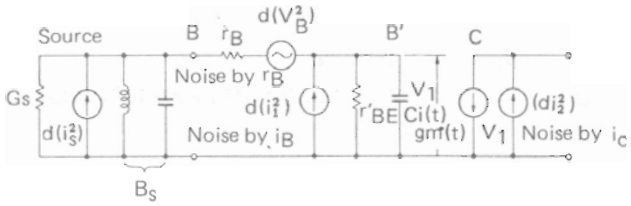


Fig. 7 Noise Model Circuit

$d(i_S^2)$ is the signal source noise current, $d(V_B^2)$ the noise generated by the base resistance, and $d(i_1^2)$ the noise due to the base current. They are amplified and appears on the collector side. $D(i_2^2)$ is the noise generated by the collector current. Assume these noise components i_{01}^2, i_{02}^2, i_{03}^2, and i_{04}^2, respectively.

The total noise N is

$$N = \frac{i_{01}^2 + i_{02}^2 + i_{03}^2 + i_{04}^2}{i_{01}^2} \qquad \text{----------(3)}$$

The noise in MIX is expressed by

$$N = 1 + \frac{g_{mA} R_S}{2B_{N'}} \left\{ \left(1 + \frac{r_B}{R_S}\right)^2 + \left(\frac{r_B}{X_i}\right)^2 \right\} + \frac{1}{2g_{mA}} \left(1 + \frac{R_S}{R_i}\right)^2 \frac{1}{P^2 R_S}$$

$$+ \frac{r_B}{R_S} \left\{ 1 + \left(\frac{R_S}{X_i}\right)^2 \right\} \quad \text{note 2)} \qquad \text{----------(4)}$$

and the noise in amplifier by

$$N = 1 + \frac{g_m R_S}{2B_{N'}} \left\{ \left(1 + \frac{r_B}{R_S}\right)^2 + \left(\frac{r_B}{X_i}\right)^2 \right\}$$

$$+ \frac{1}{2g_m} \left(1 + \frac{R_S}{R_i}\right)^2 \frac{1 + Q^2}{R_S}$$

$$+ \frac{r_B}{R_S} \left\{ 1 + \left(\frac{R_S}{X_i}\right)^2 \right\} \quad \text{note 2)} \qquad \text{----------(5)}$$

note 2) References to NF of RF and MIX.

PROC. IEE, vol.115, No 4, APR. 1968

The values of noises are calculated by putting parameters of 2SC2352 into the formulas above. The parameters are:

- $g_{mA} = qI_A/kT$ (I_A: dc collector current) = 3 mA/26 mV = 115 mS.
- R_S = 64 Ω note 1)
- $B_{N'}$: dc current gain at large amplitude (h_{FE}=100)
- r_B : base resistance (19 Ω as estimated from Fig.8)
- X_i : input reactance ($1/b_i$ = 53.8 Ω from y-parameter)
- R_i : input impedance ($1/g_i$ = 96.2 Ω from y-parameter)

○P : g_C/g_{mA} (g_C is conversion conductance, and, when assumed as $g_C=\frac{1}{2}g_m$, $g_C=\frac{1}{2}\times 88$ mS=44 mS from y-parameter), and $g_C/g_{mA}=44/115=0.38$.

○Q : $g_m r_B f_s/f_T = 88\times10^{-3}\times19\times200\times10^6/(800\times10^6)=0.42$.

NF value of MIX is, from eq.(4),

$$N = 1+\frac{115\times10^{-3}\times64}{2\times100}\left\{\left(1+\frac{19}{64}\right)^2+\left(\frac{19}{53.8}\right)^2\right\}$$
$$+\frac{1}{2\times115\times10^{-3}}\left(1+\frac{64}{96.2}\right)^2\frac{1}{0.38^2\times64}$$
$$+\frac{19}{64}\left\{1+\left(\frac{64}{53.8}\right)^2\right\}=3.09\ (\fallingdotseq 4.9\ \text{dB}).$$

Also, NF value of RF is, from eq. (5),

$$N = 1+\frac{88\times10^{-3}\times64}{2\times100}\left(1+\frac{19}{64}\right)^2+\left(\frac{19}{53.8}\right)^2$$
$$+\frac{1}{2\times88\times10^{-3}}\left(1+\frac{64}{96.2}\right)^2\frac{1+0.42^2}{64}$$
$$+\frac{19}{64}\left\{1+\left(\frac{64}{53.8}\right)^2\right\}=2.06\ (\fallingdotseq 3.1\ \text{dB}).$$

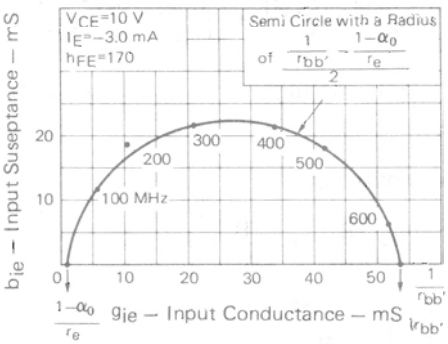


Fig. 8 Frequency Locus of 2SC2352 Yie

The above estimation of NF when 2SC2353 is used in RF and MIX respectively, shows that NF of MIX is inferior to NF by about 2 dB.

Fig. 3 shows NF vs. local level relationship. NF of 2SC2352 has a minimum at the local level of about 115 dBμV/50 Ω and takes a value of 5.2 dB when C=30 pF (R_S=64 Ω). (NF of about the same value is obtained when C=15 pF and R_S=106 Ω)

Fig. 9 shows the NF vs. I_E characteristics when 2SC2352 is used in RF and in MIX, respectively. According to the figure, when C=30 pF (R_S=64 Ω), NF of RF at 3 mA is 3.0 dB and NF of MIX is 5.2 dB. This fact tells that NF of MIX is inferior to NF of RF by 2.2 dB, and a relatively good afreement with the calculated result is obtained.

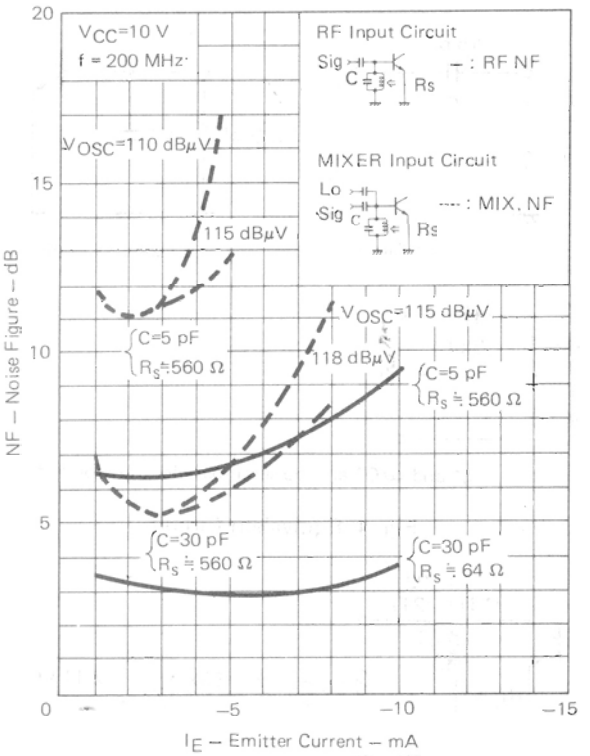


Fig. 9 RF And Mix. Circuit Noise Figure vs. Emitter Current

When C=5 pF (R_S=560 Ω) (mismatched input), NF's at 3 mA are 6.2 dB in RF and 11.4 dB in MIX, telling that the difference between the both is increased.

The measured NF of MIX for the constant local level is rather largely varied with the current as shown by the solid curves of the figure. Since NF is dependent to have the optimum conversion conductance for any current level will bring about a less current dependency as shown by the dashed curves.

The condition fot the minimum NF of 2SC2352 MIX is; signal source impedance of about 64 Ω, local level of 115 dBμV/ 50 Ω and I_E of 2.5–3 mA. The minimum value of NF is 5.2 dB.

3.3 Intermodulation

Fig.10 shows the intermodulation of 2SC2352.[note 3] According to the figure, it takes the optimum at I_E of 5 mA, and it is

41 dB for C = 30 pF (Rs=64 Ω),
45 dB for C = 15 pF (Rs=106 Ω), and
62 dB for C = 5 pF (Rs=560 Ω).

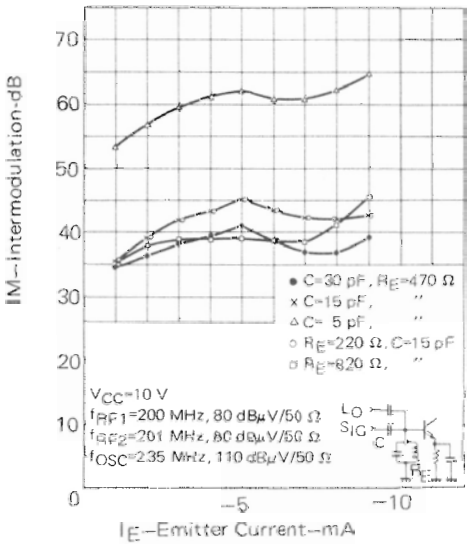


Fig. 10 Intermodulation vs. Emitter Current

note 3) Intermodulation is defined as Fig. 11.

Fig. 11 Definition of Intermodulation

As shown above, the more the input impedance is getting mismatched ($R_s > R_i$), the better becomes the intermodulation characteristics. But this is not favorable because it causes the deterioration of Gce and NF. (The increase of I_E tends to reduce the intermodulation, but this is also discarded as impractical because this leads to the inferior Gce and NF as well as the increase of power consumption.)

The intermodulation dependency on the emitter resistance R_E is shown in Fig.10. (Variation in R_E causes the change in the emitter voltage and concurrently in V_{CE}.) According to the figure, for R_E of 220 Ω and of 470 Ω, the same intermodulation is obtained when I_E is 1–9 mA whereas for R_E of 820 Ω, the larger is I_E (I_E= 5–8 mA), the smaller becomes V_{CE} (for I_E of 5 mA V_{CE}=5.9 V and for I_E of 8 mA V_{CE}=3.44 V) and the intermodulation tends the worse. Therefore, it is practical to set V_{CE} as $V_{CE} > \frac{1}{2} V_{CC}$.

With regard to the above described analysis, a circuit condition which is presumably appropriate in intermodulation as well as in Gce and NF will be: signal source impedance of about 106 Ω (C=15 pF) and I_E of 3–5 mA. Then the intermodulation will be 42-45 dB for an input level of 80 dBμV/50 Ω.

4. CHARACTERISTICS OF 2SC2352 MIX

Summarizing descriptions from 3–1 to 3–3, the circuit which is expected as good is overall characteristics will be the one shown in Fig. 12. The circuit condition is:

signal source impedance of about 100 Ω,
load impedance of about 2 kΩ,
(termination impedances of the both of 50 Ω),
local injection level of 110–115 dBμV/50 Ω, and
biasing condition
I_E = 3–5 mA for V_{CC} of 10 V.

The characteristics are then

Gce=23.2 dB (at local level 115 dBμV/50 Ω and I_E= 3 mA),
NF=5.3 dB (at local level 115 dBμV/50 Ω, and I_E= 3 mA),

and

intermodulation=42 dB (at input level of 80 dBμV/50 Ω, local level of 115 dBμV/50 Ω, and I_E=3 mA).

Fig.13 shows basic mixer circuit in order to get each datas used in this application note.

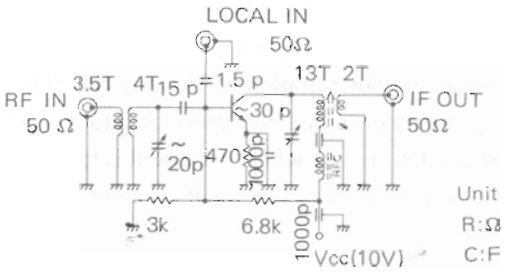


Fig. 12 Recommended Mixer Circuit

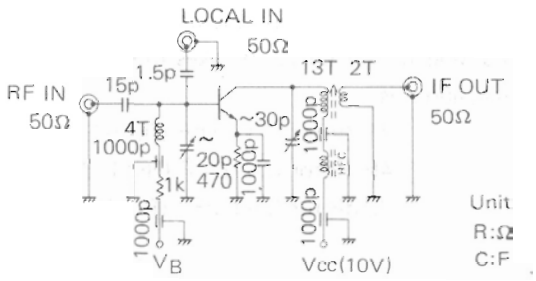


Fig. 13 Basic Test Circuit

TYPICAL APPLICATION OF 2SC2353 FOR UHF TV TUNER MIXER

1. GENERALS

2SC2353 is an NPN epitaxial silicon transistor developed principally for mixers of UHF TV tuner. Provided with features such as high gain bandwidth product f_T and wide current characteristics, it is the most suitable for mixers.

The following descriptions will explain the characteristics of 2SC2353 used in a mixer of a UHF TV tuner.

2. TRANSISTOR MIXERS

A transistor mixer performs frequency conversion on the principle that the signal voltage v_S is applied to the emitter junction of the transistor in series to the oscillator voltage v_O and the input conductance of the transistor is periodically varied by v_O.

The IF voltage generated on the input side is amplified by the transistor and only the IF component is selected by the output side IF tuning circuit and delivered to the next stage.

The merit of transistor UHF TV tuner mixer lies in its higher power gain by 20 dB than that of diode mixer, provided that a conversion gain (G_{cb}) of the transistor mixer is assumed to be 10 dB and a conversion loss of the diode mixer to be 10 dB.

In addition, noise figure (NF) of the transistor mixer is reduced concurrently.

The power gains and NF for a diode mixer and for a transistor mixer can be estimated as Fig. 1 and Fig. 2.

since

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \frac{F_4 - 1}{G_1 \cdot G_2 \cdot G_3}$$

NF of transistor mixer tuner is calculated as

$$F = 2.82(4.5\ \text{dB}) + \frac{2(3\ \text{dB}) - 1}{10(10\ \text{dB})} + \frac{10\ (10\ \text{dB}) - 1}{10(10\ \text{dB}) \times 0.5\ (-3\ \text{dB})} + \frac{1.78(2.5\ \text{dB}) - 1}{10(10\ \text{dB}) \times 0.5\ (-3\ \text{dB}) \times 10(10\ \text{dB})}$$

$$= 4.74,$$

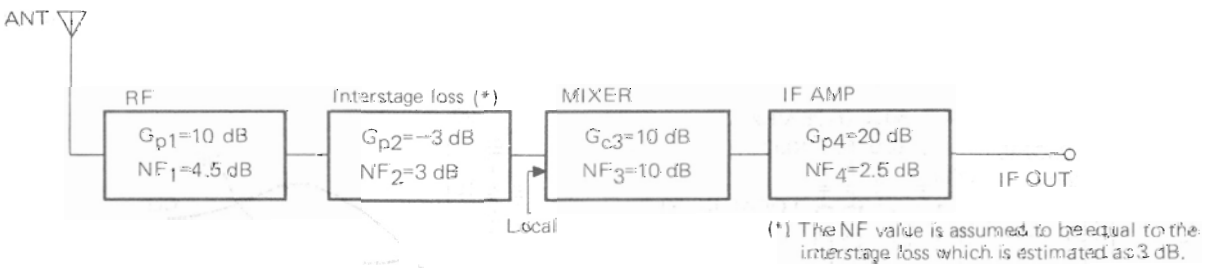


Fig. 1 Gp and NF Distribution of Transistor Mixer

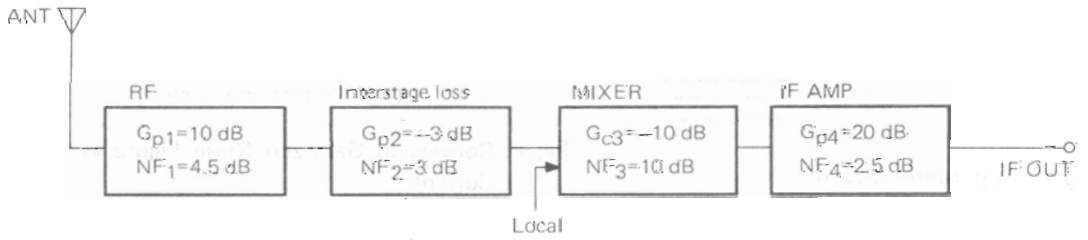


Fig. 2 Gp and NF Distribution of Diode Mixer

and NF = 10 log 4.74=6.75 dB. While, for diode mixer tuner,

$$F = 2.82 + \frac{2-1}{10} + \frac{10-1}{10\times0.5} + \frac{1.78-1}{10\times0.5\times0.1} = 6.28$$

NF = 10 log 6.28 = 7.98 dB.

The power gains of tuner are 37 dB and 17 dB for transistor mixer and for diode mixer, respectively.

The results clearly demonstrate the superiority of transistor mixer tuner to diode mixer tuner.

3. CHARACTERISTICS OF UHF TV TUNER MIXER USING 2SC2353

The characteristics of a UHF TV tuner mixer using 2SC2353 will be described below. The circuitry is as illustrated in Fig. 3. It is a base-grounded, emitter-input and emitter injection type and its IF is 35 MHz. The actual circuit constants have been shown in Fig. 4.

Fig. 5 shows the local level vs. Gcb and Ic relationship. note 1)

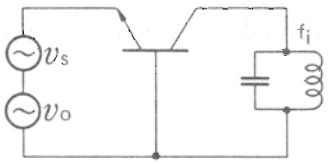


Fig. 3 Emitter Input and Injection Type Mixer for Base Ground

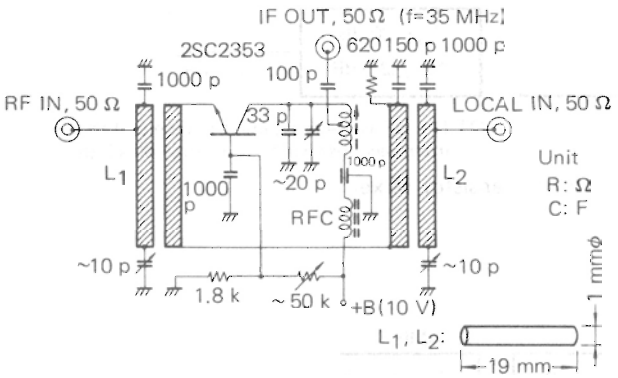


Fig. 4 Application Circuit

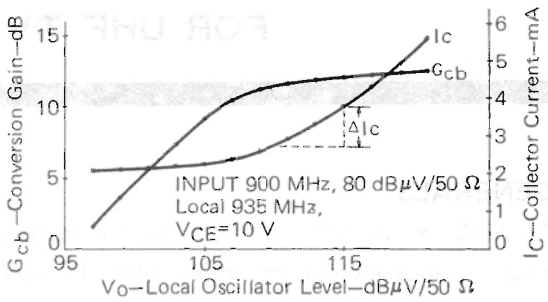


Fig. 5 Conversion Gain and Collector Current vs. Local Oscillator Level

note 1)

local level ..... The output power of the local oscillator. In the experiment, the local oscillator is substituted by an SG (signal generator), and the SG output is used as the local level.

ΔIc ..... The bias current (Ic) variation due to local signal injection.

When the local level is 105 dBμV or more, Gcb is saturated. Gcb cannot be increased any more by raising the local level. Fig. 5, 6 and 7 show the Gcb, NF relationshop to current and frequency response. Fig. 6 tells that Gcb reaches the maximum at Ic of about 10 mA and NF is good for Ic of 3–8 mA. When 2SC2353 is used as an RF amplifier, its NF is about 4.5 dB for Ic of 3–8 mA. This means that the NF reduction by about 5 dB is experienced when the transistor is used as a mixer.

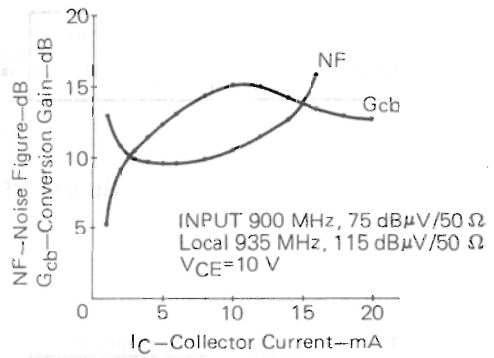


Fig. 6 Conversion Gain and Noise Figure vs. Collector Current

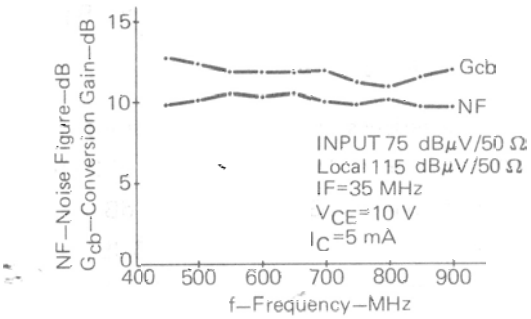


Fig. 7 Conversion Gain and Noise Figure vs. Frequency

The intermodulation (IM) note 2) shown in Fig. 8 is as good as 53 dB for a small current (I_C=1 mA).

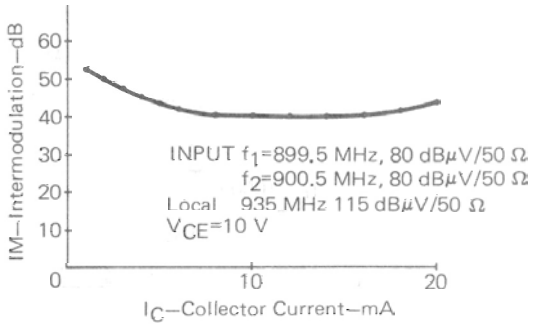


Fig. 8 Intermodulation vs. Collector Current

note 2)

When f_1 (899.5 MHz) and f_2 (900.5 MHz) are input to RFIN of the mixer, third order distortions $2f_1-f_2$ (898.5 MHz) and $2f_2-f_1$ (901.5 MHz) are produced. fosc (935 MHz) is input to those signals to convert then into IF signals. The level difference (X dB) between the converted outputs and the third order distortions is called intermodulation (IM).

Fig. 9 Definition of Intermodulation

But this condition is not favorable because G_{cb} is small there. Hence the optimum current range for G_{cb}, NF, and IM is limited to 3–8 mA. Furthermore, if a local level, which is so small that G_{cb} is not saturated as shown in Fig. 5, could be selected as the optimum, it would be favorable. But, the constancy of the local level cannot be maintained in UHF band having a very wide bandwidth.

Therefore the local level should be set to a point where G_{cb} is hardly affected by the local level variation. This means a local level setting in a region where no G_{cb} increase takes place in spite of possible local level rising, namely in the region of G_{cb} saturation. On the other hand, too high local level is meaningless because of increase in radiation from the antenna. Therefore, the recommended local level setting in conditions shown in Fig. 5 would be 110–115 dBμV, where the bias current increment (Δlc) is 1–2 mA (for R_E=620Ω).

Fig. 10 shows the characteristics of the intermodulation and the collector current versus local oscillation level. Fig. 11 shows the input to output characteristic of the mixer along with the IM characteristic.

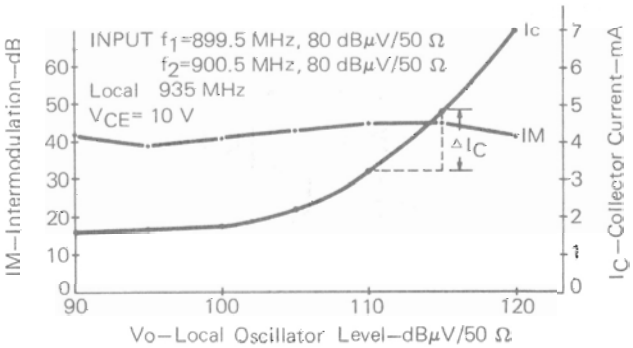


Fig. 10 Intermodulation and Collector Current vs. Local Oscillator Level

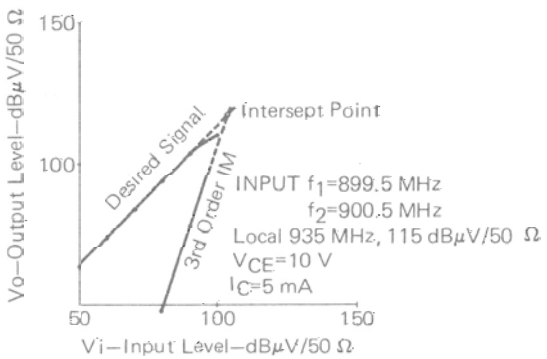


Fig. 11 Output Level vs. Input Level

As the input level is increased, the output level and IM are also increased. Typically, 10 dB increase of the input brings about (10 dB increase of the output and) 20 dB deterioration of IM. Further increase of the input would finally equate the IM level to the output level. (Actually, the transistor must be saturated and it is impossible that the IM level becomes equal to the output level). This point is called intercept-point, IP (refer to Fig. 11). When this IP is known, the IM value for any input or output level can be obtained through the following formula.

|Third order intermodulation (IM)| = 2(IP-Pi), where Pi is the input power. The input level at the intercept point of 2SC2353 is read as 103 dB. So, for an input level of 80 dBμV, IM=2(103−80)=46 dB.

From the above reasoning, a typical condition regarded as optimum is Vcc=10 V(15 V is also usable) for bias and I_C=5 mA. Then Ic includes an additional current increment (Δic) of 2 mA due to the local signal injection. Therefore the biasing circuit should be set to have Ic of about 3 mA before hand.

The final circuit arrangement for the experiment is shown in Fig. 12.

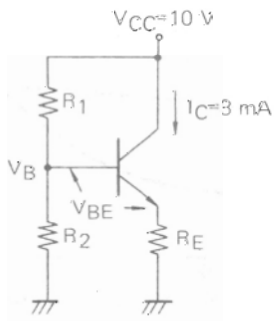


Fig. 12 Biasing Circuit

○ R_E = 620 Ω (since Δic has been measured at R_E of 620 Ω).

○ $V_B - V_{BE} = 620 \times 3 \times 10^{-3} = 1.86$ V,
and for V_{BE} of 0.78 V, V_B = 1.86+0.78=2.64 V

○ Using a relationship $V_B = \frac{R_2}{R_1+R_2} V_{CC}$, R_1=5 kΩ for R_2 of 1.8 kΩ.

The characteristics of the mixer are; at input level of 80 dBμV and local level of 115 dBμV(Δic of 2 mA),

Conversion Gain : G_{cb} ..... 12 dB
Noise Figure : NF ..... 9.6 dB
Intermodulation : IM ..... 46 dB,

Fig. 13 and 14 show UHF RF amplifier circuit use with 2SC2353 and G_{pb}, NF characteristics due to Fig. 13's circuit.

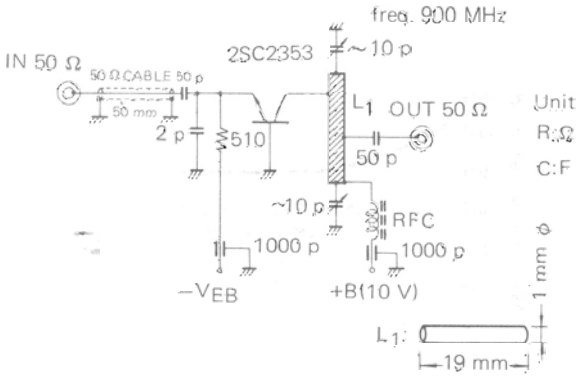


Fig. 13 Application Circuit for UHF/RF Amplifier

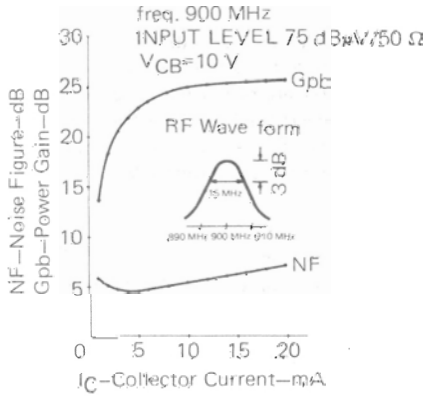


Fig. 14 Power Gain and Noise Figure vs. Collector Current

HIGH FREQUENCY LOW-NOISE TRANSISTORS FOR VHF AND UHF BAND APPLICATIONS
—APPLICATION OF 2SC2570A—

1. INTRODUCTION

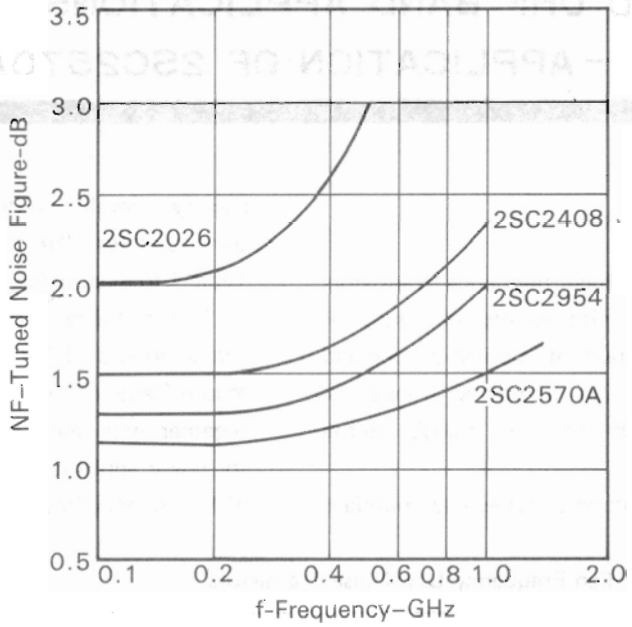
Recently, application of high frequency transistors has been expanded along with variety of consumer products. These wide expanses of application demand various characteristics of high frequency transistors, therefore, a number of high frequency transistors has been developed.

NEC provides enough groups of types and abundant package developments of high frequency low-noise transistors for VHF and UHF band amplifier shown in Table 1 to meet demands from various fields.

This technical report describes in detail electrical characteristics of 2SC2570A that can be used for any requirements of low-noise, high gain, and low distortion together with their optimal characteristics and usages for many application fields as well as design idea of NEC high frequency low-noise transistors.

Table 1 List of High Frequency Low-Noise Transistors

f_T (TYP.) Package	1.1 GHz	2.0 GHz	3.5 GHz	5.0 GHz
TO-92	2SC1730 *1 JE7001 *2	2SC2026	2SC2408	2SC2570A
MINI MOLD	2SC2757	2SC2759	2SC2954 *3	2SC2351
DISK MOLD		2SC2368		2SC2369
MICRO-X		2SC2148		2SC2149
APPLICATIONS	• VHF and UHF band oscillation *1 center-collector *2 center-emitter	• VHF and UHF band oscillation and low-noise amplifier	• Wide-band amplifier • Medium power *3 SOT-89 package f_T (typ.)=4.0 GHz	• VHF and UHF band low-noise amplifier



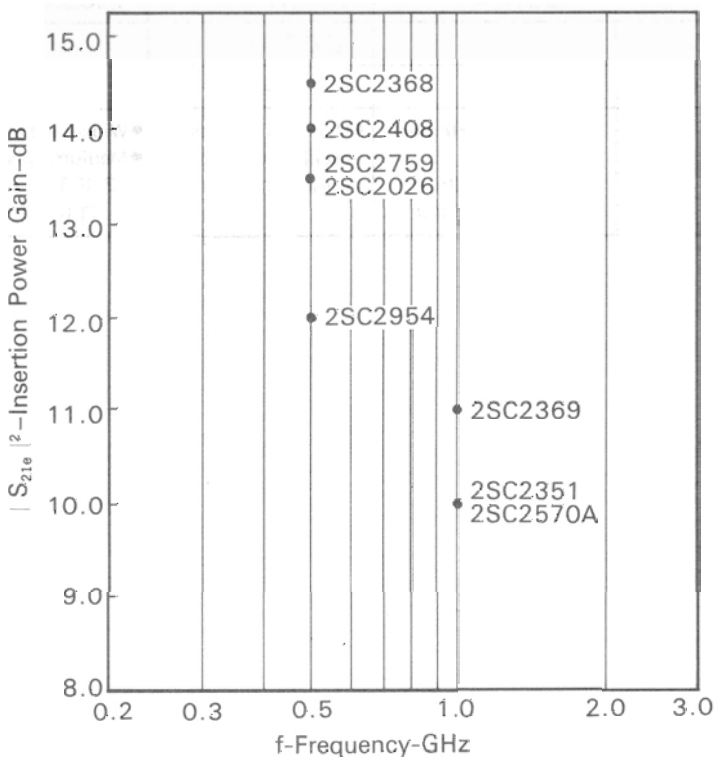


Fig. 1 Frequency Characteristic of Noise Figure and Insertion Power Gain

2. IMPROVEMENT OF HIGH-FREQUENCY TRANSISTOR TOWARDS LOW NOISE

Parameters required for improving high-frequency transistors towards low noise are explained using a numerical expression. The noise figure (NF) is, in general, replaced by the expression shown below:

$$NF \fallingdotseq 1 + 2\left(1 + \frac{r_b}{r_e}\right) \times \left\{\frac{1}{h_{FE}} + \left(\frac{f}{f_T}\right)^2\right\} \quad \cdots\cdots\cdots (1)$$

i.e., larger f_T is better for low noise. Resistance components, r_b, r_e are also important. These parameters are explained in detail in the followings.

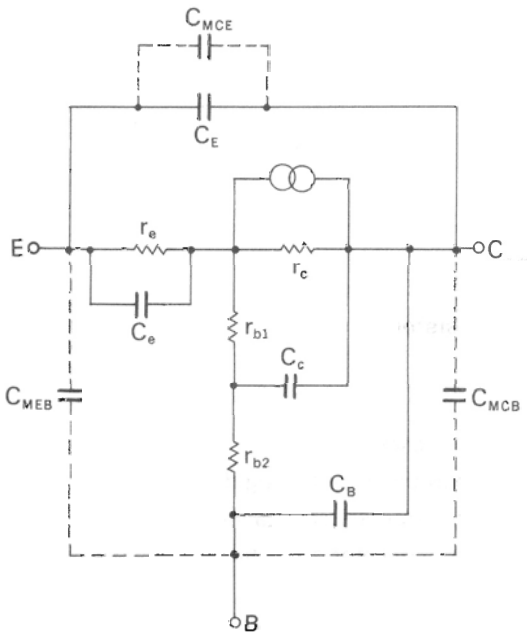
2-1 Explanation of parameters by means of equivalent circuit of a transistor

The parameters in Equation (1) are explained using Fig. 2, Transistor Equivalent Circuit, and Fig. 3, Simple Diagram of Cross Section of Transistor.

As shown in the figures:

r_e : Emitter diffusion resistance
r_{b1} : Base diffusion resistance
r_{b2} : Base spread resistance
r_b : Base resistance ($r_b = r_{b1} + r_{b2}$)

Since $r_b \gg r_e$ can be assumed, minimizing the base diffusion and base spread resistances is important for low noise.



C_C : Collector junction capacitance
C_e : Emitter junction capacitance
C_B : Base electrode MOS capacitance
C_E : Emitter electrode MOS capacitance
C_{MCE} : Resin parasitic capacitance (between collector and emitter)
C_{MCB} : Resin parasitic capacitance (between collector and base)
C_{MEB} : Resin parasitic capacitance (between emitter and base)

Fig. 2 T-type Equivalent Circuit Based on Early's Equivalent Circuit (Equivalent Circuit in which Parastic Capacitance is taken into Consideration)

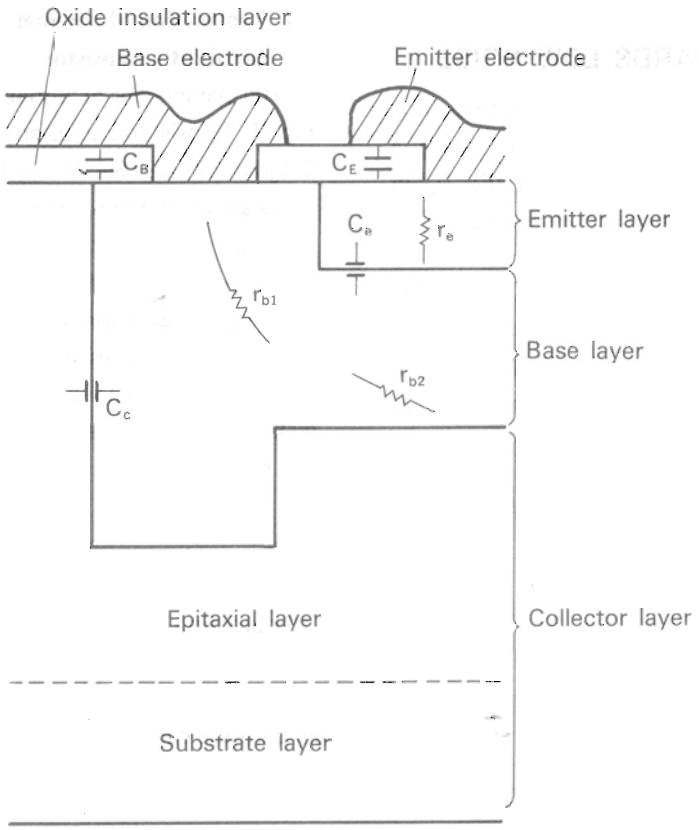


Fig.3 Cross Section of High Frequency Transistor

2-2 Design of High f_T Transistor

The function of f_T is shown below:

$$\frac{1}{2 f_T} = \tau_B + \tau_E + \tau_X + \tau_C \quad \cdots\cdots\cdots\cdots\cdots (2)$$

Wherein:

τ_B : Base running time

τ_E : Emitter capacitance charging time

τ_X : Collector depletion layer signal delay time

τ_C : Collector capacitance charging time

This equation shows that:

- Shorten the base running distance.
- Reduce emitter capacitance.
- Reduce collector capacitance.

To shorten the base running distance, make the base width W_b as narrow as possible. To reduce emitter capacitance, make the emitter layer depth X_{je} shallower and shorten emitter width W_e. Following two factors have relation to collector capacitance:

1) Collector layer resistivity (ρ_C)

2) Collector junction area

1) Collector layer resistivity (ρ_C)

The ρ_C is closely related with the breakdown voltage (BV_{CEO}) and capacitance (C_{ob} . . . C_C).

Although collector capacitance can be reduced by making the ρ_C high and the depletion layer thicker in order to shorten collector charging time, it results in increase of the collector series resistance and also in degradation of current characteristics by reduction of maximum current density and acceleration of the current collecting effect. Too low ρ_C reduces breakdown voltage (BV_{CEO}) and makes the depletion layer thinner to increase the capacity. Therefore, the ρ_C must be optimally set taking the breakdown voltage, collector capacitance, and current characteristic of h_{FE} into account.

2) Collector junction area

The simplest way of reducing the junction area of the collector is, as shown in Fig. 4, to make emitter width W_E as small as possible. With high f_T transistors, the method of reducing the relative collector junction area is applied as well as reducing the actual emitter width. In other words, the ratio of emitter circumferential length l_E to collector junction area A_C is made as large as possible so that the apparent junction area of the collector becomes small in comparison with the emitter circumferential length. Therefore, with transistors of the same collector junction area, the larger the l_E/A_C the lower their noises are.

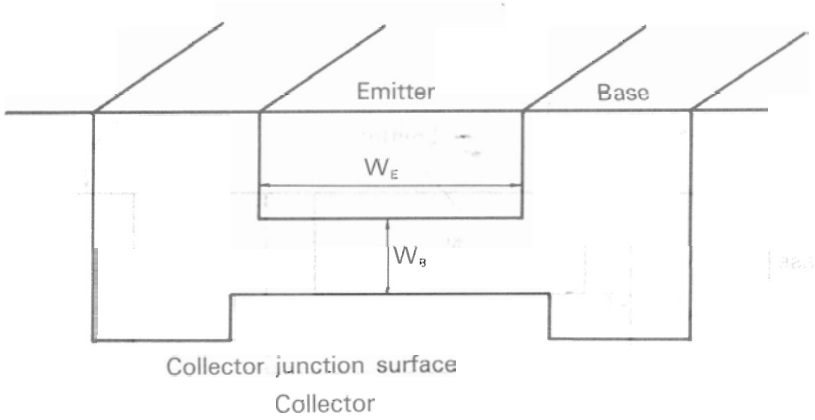


Fig.4 Enlarged view of the Transistor Cross Section

NEC adopts the "interdigital pattern (comb pattern)" as the emitter pattern to obtain the larger l_E/A_C on the limited area (collector junction). Figure 6 is the photograph of the appearance of an NEC high-frequency low noise transistor. Shaping the emitter as a comb form and making each emitter width (W_E) as small as possible, the circumferential length (l_E) is elongated as long as possible. Thus the transistor with the large l_E/A_C, expanded current characteristics, and high f_T has been realized.

2-3 Base Resistance (r_b)

Another parameter for making the high-frequency transistor low noise is base resistance (r_b). As can be seen in Fig. 3, the base resistance is composed of base diffusion resistance (r_{b1}) distributed from the base electrode to around the emitter in the base layer and base spread resistance (r_{b2}) distributed under around the emitter. In this case too, like the case of the collector, the method of improvement depending only on layer resistivity of the whole base layer does not work well. Base layer resistivity (ρ_S) is designed taking the current amplifier ratio, etc., into account.

With NEC high-frequency transistors, base resistance (r_b) has been reduced by employing the graft base structure. The graft base technique is one of high-frequency transistor manufacturing technologies developed by NEC. (Japanese Patent No. 301179/1962)

Figure 5 shows the structure of the graft base transistor. To deal with the base layer, it is divided into the graft base layer and active base layer. Almost of a few carriers injected from the emitter to the base area reach the collector via the active base area. Therefore, the area substantially related to transistor characteristics is considered almost to be the active base area. In this respect, in NEC graft base structure, the layer resistivity of the graft base area, which has little participation in the active area of the transistor, is reduced so that the effect as if the base electrode is directly attached close to the emitter is obtained. This structure greatly reduces diffusion resistance (r_{b1}) and results in reduction of base resistance (r_b).

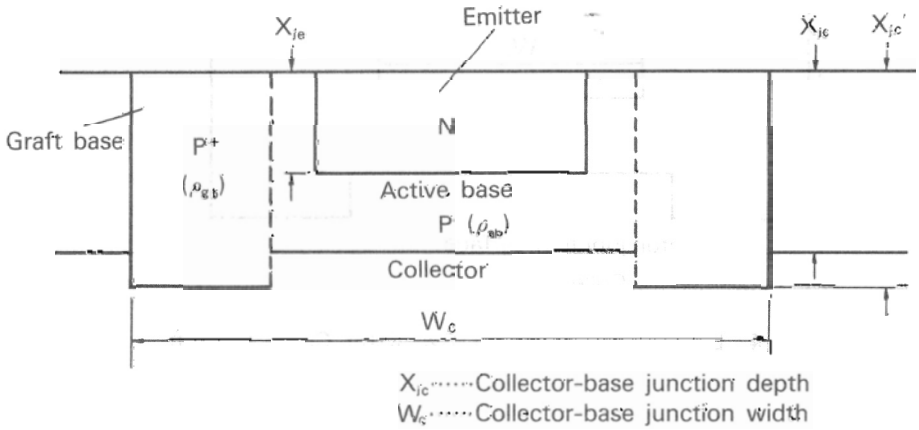


Fig. 5 Graft Base Transistor

NEC has succeeded in realizing high-frequency transistors with high f_T and low noise employing techniques, as explained above, of:

1. Making emitter layer depth (X_{je}) as shallow as possible, and emitter width (W_E) narrow using the ultra-fine diffusion technique.
2. Making I_E/A_C large by means of the interdigital pattern.
3. Making base width (W_B) as small as possible.
4. Making (r_b) small by the graft base structure.

Figure 6 shows the photograph of a high-frequency low-noise transistor.

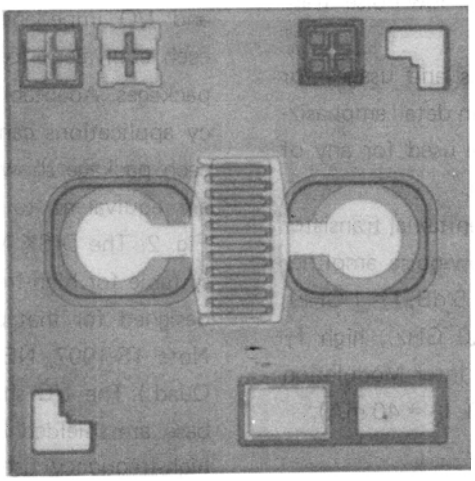


Fig.6 NEC High Frequency Low-Noise Transistor

3. HIGH-FREQUENCY LOW NOISE AMPLIFIER TRANSISTOR — 2SC2570A —

The application field of high-frequency low-noise amplifier transistors has been widened and they are used for:

(1) Low-noise amplifier
(2) High-gain, low-noise amplifier
(3) Wide-band, low-noise amplifier

NEC provides product groups, each of which has specialized features, of high-frequency low-noise transistors as shown in Table 1.

Below, their optimal characteristics and usages for each field of application are described in detail emphasizing those of 2SC2570A which can be used for any of low-noise, high-gain, and low-distortion.

NEC 2SC2570A is an NPN silicon epitaxial transistor designed for VHF and UHF bands low-noise amplifier and has features of low noise (NF = 1.5 dB, f = 1 GHz), high gain ($|S_{21e}|^2$ = 10 dB, f = 1.0 GHz), high f_T (5.0 GHz, I_C = 20 mA), and superior Inter Modulation distortion characteristic (IM_3 = −73 dB, I_C = 40 mA).

2SC2570A is contained in TO-92 package so that the wide dynamic range can be utilized and the material of its frame is changed to copper instead of conventional iron (2SC2570) to obtain the total power dissipation of up to 600 mW. Besides TO-92 package, various packages are provided such as DISK MOLD, MINI MOLD, and MICRO-X packages for transistors equivalent to 2SC2570A as shown in Table 1. Below how to use a type of packages for a particular application is also explained.

3-1 Electrical Characteristics of 2SC2570A Groups and Its Effective Usage of Each Package

Table 2 lists the electrical characteristics of 2SC2570A and Figs. 7 through 9 show the current characteristic of each electrical characteristic. The curves of the gain bandwidth product f_T and insertion gain ($|S_{21e}|^2$) vs. collector current (I_C) extend up to 30 mA to show that this transistor has a very wide dynamic range. (Broken line curves showing the characteristics on the low voltage operating are added for reference.) 2SC2570A has the highest f_T in comparison with 2SC2026 and 2SC2408 and has NF as less as 1.5 dB at the frequency of 1.0 GHz to show that his is a high-frequency transistor with extremely low noise.

Figure 11 shows case capacitance of various packages and I/O impedance characteristics by S-parameter of each equivalent to 2SC2570A that are packed in those packages. Adaptability of each package to high-frequency applications can be known from the capacitance of each package shown in Fig. 11-(1). These capacitances are equivalent to the parasitic capacitance shown in Fig. 2. The DISK MOLD package is mold package most suitable for high-frequency applications as it is specially designed for that purpose. (Refer to NEC Application Note TS-T007, NEC Disk Mold Transistors FET Diode Quad.) The I/O shielding effect in which collector and base are shielded by an emitter electrode, suitable for high-frequency uses gives, when used with the emitter grounded, superior high-frequency characteristics. The MINI-MOLD package has been developed to meet the demand of miniaturizing packages and is used mainly for packaging on a hybrid IC. Its capacitance is small in comparison with TO-92 due to its small package. In view of the total power dissipation, TO-92 is superior as shown in Table 3. About taping and forming for automatic mounting machine, refer to NEC Application Note TEM-3004, Transistors Selection Guide for Non-Industrial and Consumer Use Small-Signal Devices.

Figures 11 (2) to 11 (4) show, by S-parameter, how frequency characteristics of the I/O impedance change due to differences of packages which pack the equivalent chip as 2SC2570A. Input circuit design must be consistent with the package used.

Table 2 Electrical Characteristics of 2SC2570A

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Collector Cutoff Current	I_{CBO}	V_{CB}=15 V, I_E=0			0.1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=2.0 V, I_C=0			0.1	μA
DC Current Gain	h_{FE}	V_{CE}=10 V, I_C=20 mA	40		200	
Gain Bandwidth Product	f_T	V_{CE}=10 V, I_C=20 mA		5.0		GHz
Output Capacitance	C_{ob}*	V_{CB}=10 V, I_E=0, f=1.0 MHz		0.7	0.9	pF
Insertion Power Gain	$\|S_{21e}\|^2$	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz	8	10		dB
Noise Figure	NF	V_{CE}=10 V, I_C=5 mA, f=1.0 GHz		1.5	3.0	dB
Maximum Available Gain	MAG	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz		11.5		dB

*The emitter and case terminal should be connected to the guard terminal of capacitance bridge.

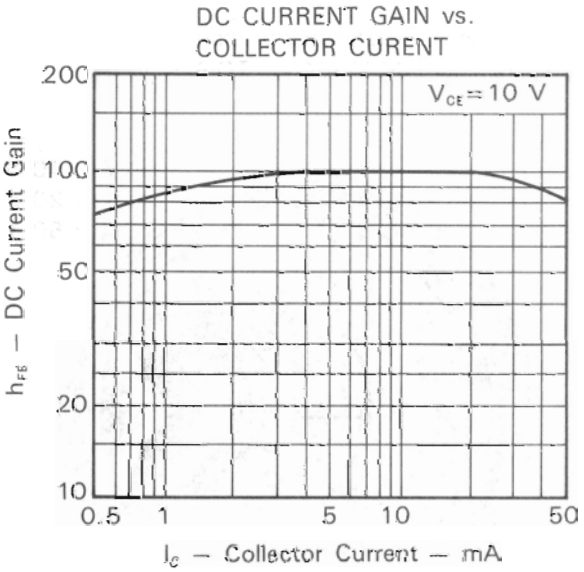


Fig. 7 h_{FE} vs. I_C (2SC2570A)

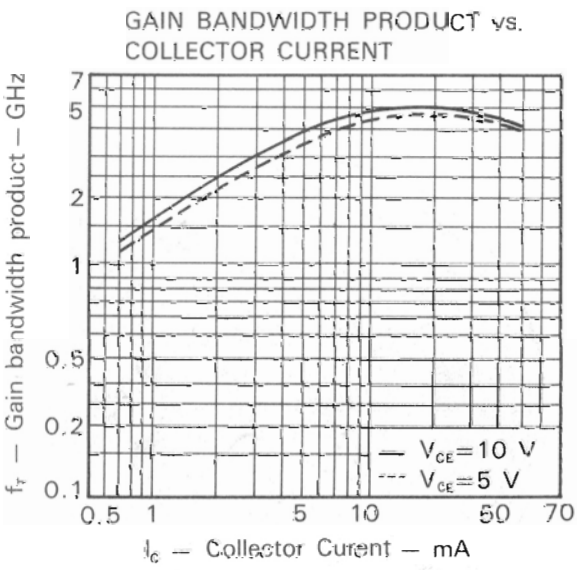


Fig. 8 f_T vs. I_C (2SC2570A)

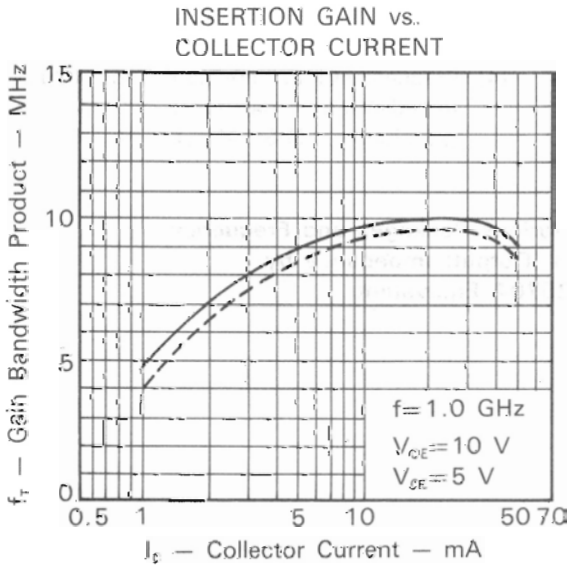


Fig. 9 $|S_{21e}|^2$ vs. I_C (2SC2570A)

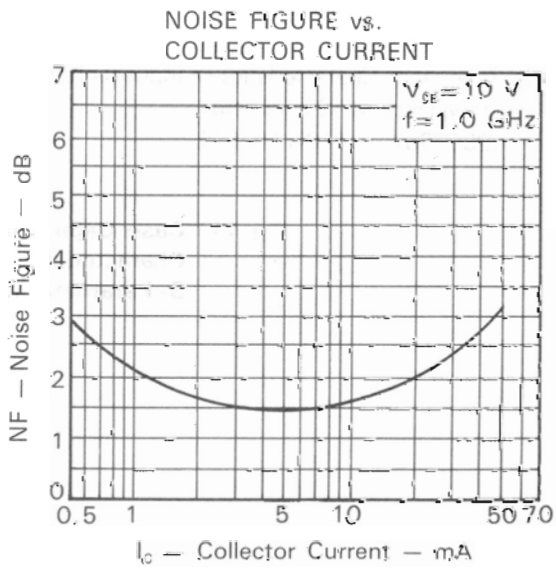
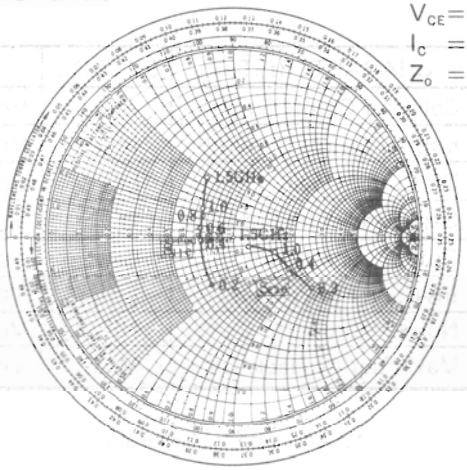


Fig. 10 NF vs. I_C (2SC2570A)

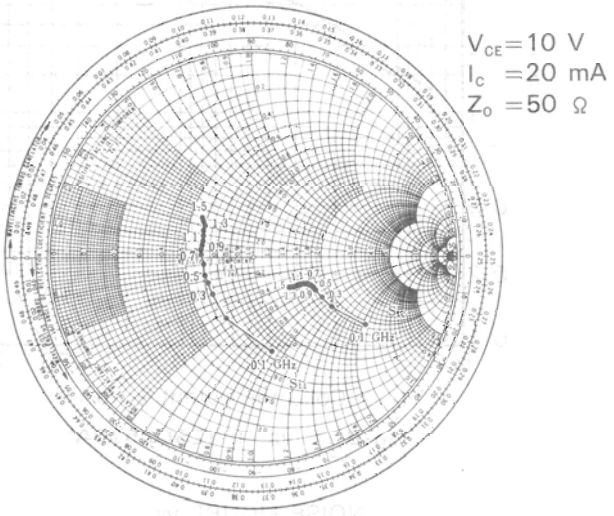
(1) Case Capacitance of Various Packages

Package / (Case Capacitance Between Terminals)	TO-92 (E-center)	DISK MOLD	MINI MOLD
C_{B-E}	0.12	0.15	0.01
C_{C-E}	0.27	0.004	0.10
C_{C-B}	0.18	0.15	0.10

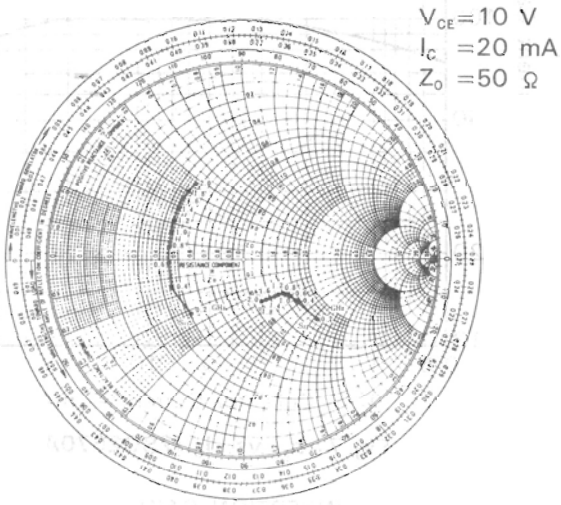
(NOTE) Case capacitance is the capacitance between terminals (these are elctrodes) of the plastic molded package and without a chip (dice). The third terminal, with which no measurement is carried out, is grounded on measurement.



(2) Frequency Characteristics of Input (Output) Impedance by S-parameter (2SC2570A . . . TO-92)



(3) Frequency Characteristics of Input (Output) Impedance by S-parameter (2SC2351 . . . MINI MOLD)



(4) Frequency Characteristics of Input (Output) Impedance by S-parameter (2SC2369 . . . DISK MOLD)

Fig.11 Case Capacitance of Various Packages and Frequency Characteristics of Input (Output) Impedance by S-Parameter for 2SC2570A Equivalent

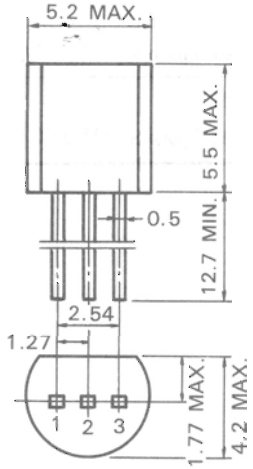
Table 3 Features of Packages

Items / Packages	Features	P_T (mW) (free air)
TO-92	○ Easy handling ○ Good compatibility	250 to 600 (at $T_{jMAX.}$ = 150 °C)
MINI MOLD	○ Ultra-miniature standard outline ○ Small case capacitance	200 to 250 (at $T_{jMAX.}$ = 150 °C)
DISK MOLD	○ High frequency characteristic emphasized ○ Small case capacitance	250 (at $T_{jMAX.}$=150 °C)

Table.4 Groups of Packages And Their Outlines

Unit : mn

TO-92

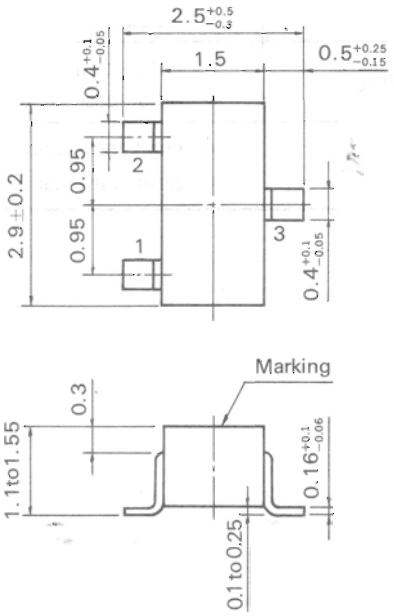


1. Base
2. Emitter
3. Collector

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA-33

• Low cost, good compatibility

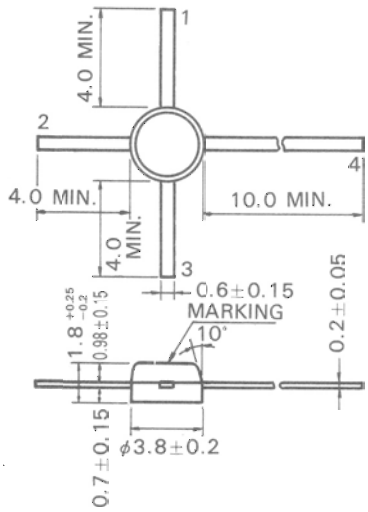
MINI MOLD



1. Emitter
2. Base
3. Collector

• Most suitable for automatic mounting and miniaturization

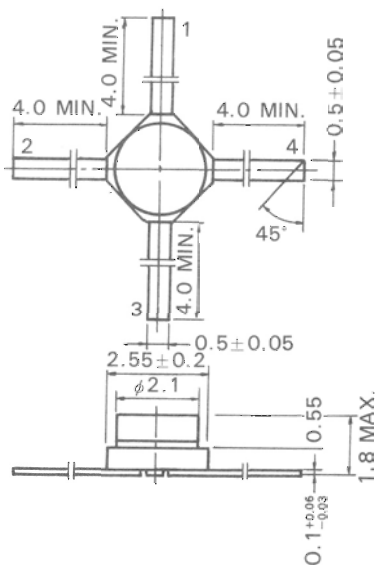
DISK MOLD



1. Emitter
2. Base
3. Emitter
4. Collector

• Automatic mounting and high frequency characteristic emphasized

MICRO-X



1. Emitter
2. Collector
3. Emitter
4. Base

• For micro wave low-noise amplifier

3-2 Application to Low-Noise Amplifier Circuits

The noise figure (NF) reaches its best noise value as low as 1.5 dB (f = 1.0 GHz) at the point where the collector current is 5 mA as shown by the NF vs. collector current in Fig. 10. Since NF begins to increase at the point where collector current is 10 mA because of starting of saturation of the gain (refer to Fig. 9), the bias is set at the collector current in the range from 5 to 10 mA.

Required power is: P = 10 V x (5 to 10 mA) = 50 to 100 mW, as collector voltage V_{CE} is usually 10 V. It is best to adopt the DISK MOLD package in order to give priority to high-frequency characteristics.

3-3 Application to High-Gain and Low-Noise Amplifier Circuits

The gain reaches its maximum value at the collector current 20 mA according to the insertion gain $|S_{21e}|^2$ vs. collector current in Fig. 9. At that point, insertion gain $|S_{21e}|^2$ reaches as high as 10 dB and maximum. Available power gain (MAG) as 11.5 dB (f = 1.0 GHz) are shown. The NF has already risen up there, however, the NF is still as low as 2 to 2.8 dB with a large collector current of 20 to 40 mA. The inter modulation distortion reaches its maximum value at collector current 40 mA and therefore regarding bias setting, value of the collector current is set in the range of from 20 to 40 mA with the best trade-off between the gain, NF, and distortion for particular requirements.

The power dissipation is: P = 10 V x (20 to 40 mA) = 200 to 400 mW with the collector voltage of 10 V, a considerable amount of power consumption so that TO-92 package is required with a few degradation of the high-frequency characteristics.

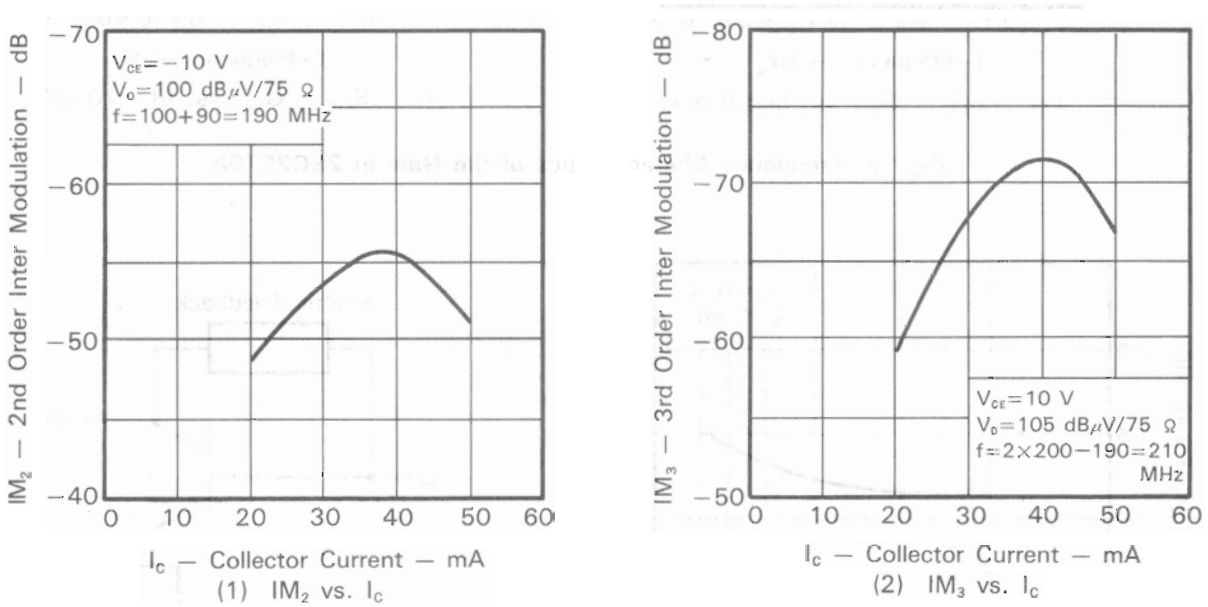


Fig. 12 Current Characteristics of Inter Modulation in 2SC2570A

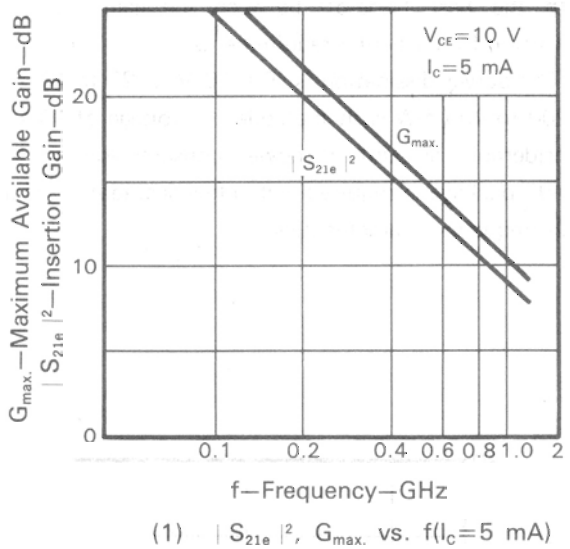
3-4 Application to Wide-Band Low-Noise Amplifier Circuits

Figures 13 and 14 show frequency characteristics of the gain and NF. A wide-band amplifier circuit can easily be designed, as shown in Fig. 15, by providing an RF feedback (high-frequency feedback) and also using an emitter feedback. Figure 16 shows the characteristics of a wide-band amplifier circuit of 2SC2570A.

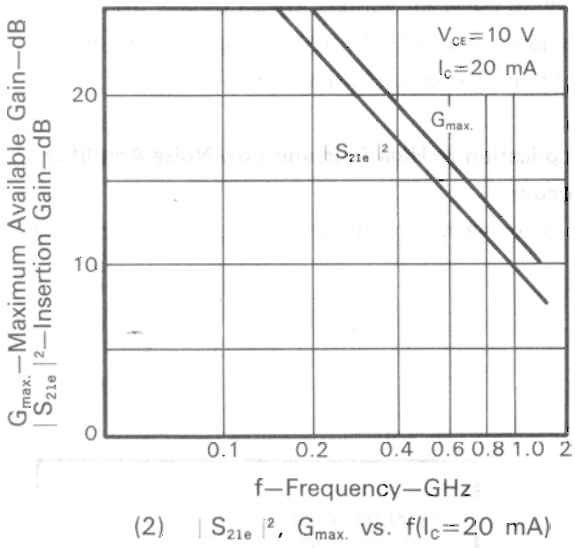
When the bias is set as power supply voltage V_{CC} = 12 V and collector current I_C = 35 mA, values below shown are obtained:

G_V = 7.5 dB, NF = 5.5 dB, and IM_3 = −73 dB

The power dissipation is: P = 12 V x 35 mA = 420 mW. Therefore, the package of TO-92 is used. To make a wide-band amplifier with hybrid IC, a MINI MOLD package is required with sufficient heat-sink design.



(1) $|S_{21e}|^2$, $G_{max.}$ vs. f(I_C=5 mA)



(2) $|S_{21e}|^2$, $G_{max.}$ vs. f(I_C=20 mA)

Fig.13 Frequency Characteristics of the Gain in 2SC2570A

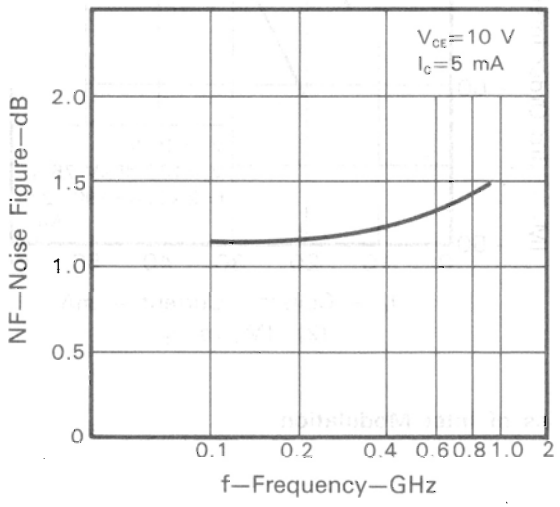


Fig.14 Frequency Characteristic of the Noise figure in 2SC2570A

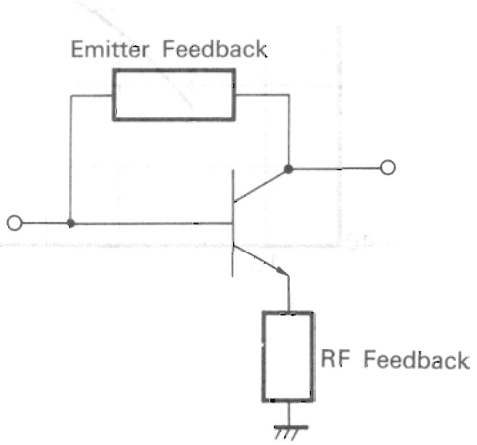
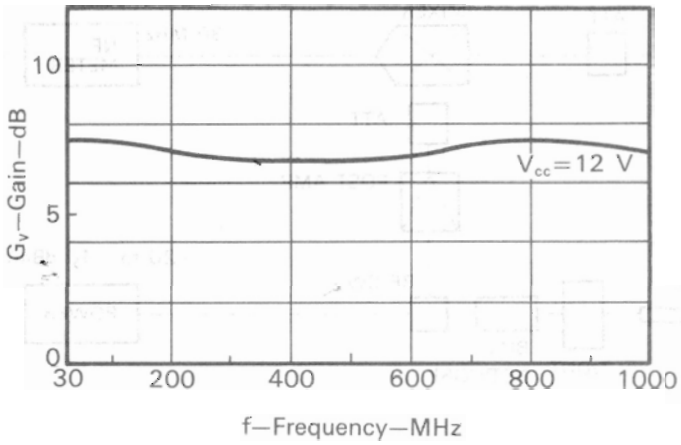
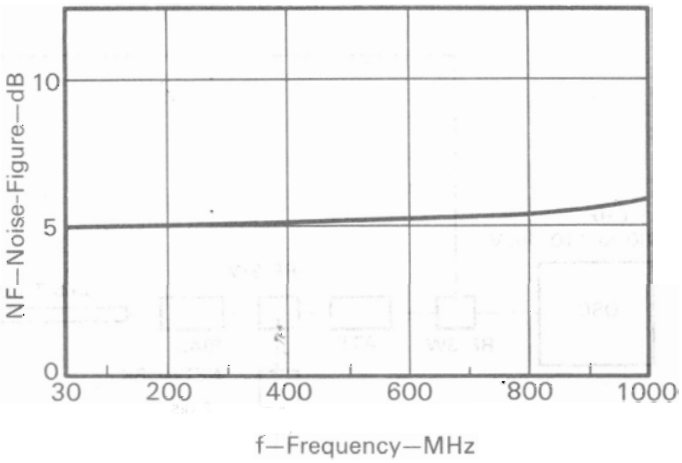


Fig.15 Wide-Band Amplifier Circuit



(1) Gain vs. Frequency



(2) Noise Figure vs. Frequency

Fig. 16 Characteristics of the wide-Band Amplifier Circuit Using 2SC2570A

4. CONCLUSION

Characteristics and applications of 2SC2570A, which can be used for low-noise, high-gain, and low distortion, as well as low-noise design idea of NEC high-frequency low-noise transistors have been described above paying attention to their optimal characteristics and usage for each field of applications. The users are requested to select the most appropriate devices taking their types and packages into account.

APPENDIX

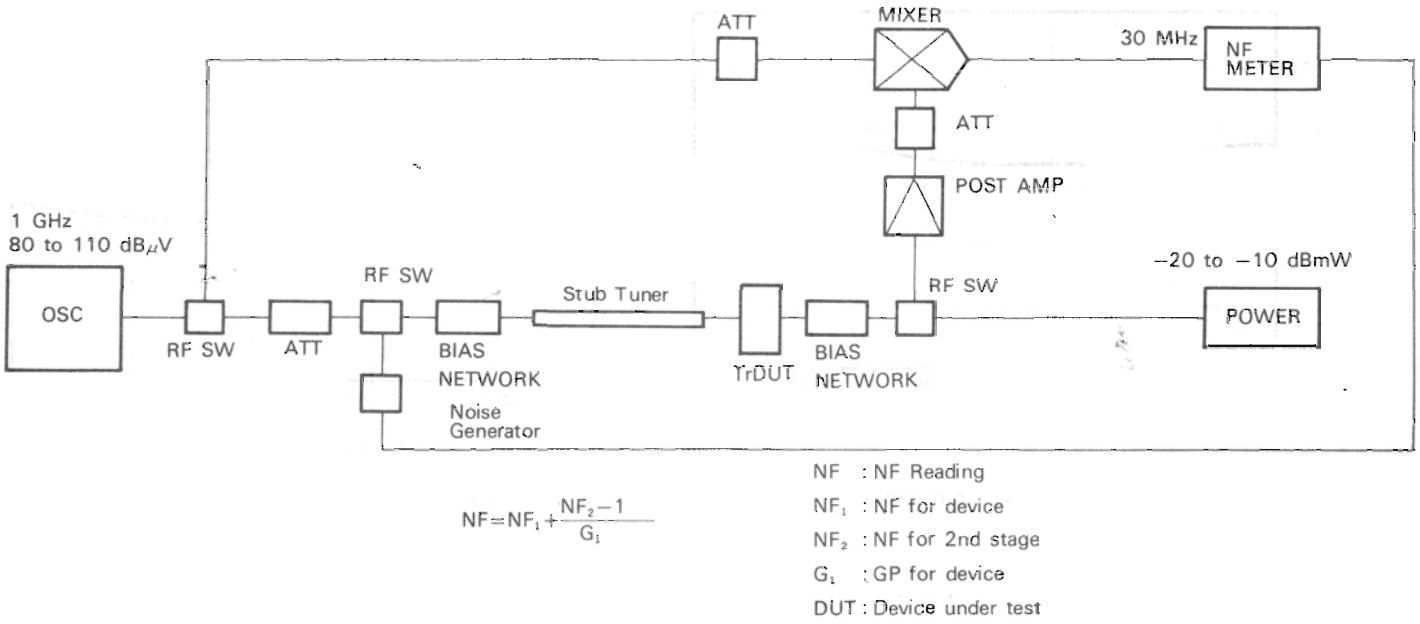
This application note gives only brief description of transistor structures and, in some places, detailed explanations are omitted. Below materials with more detailed descriptions are listed together with those already mentioned in this report.

"Transistor Selection Guide for Non-Industrial and Consumer Use Small-Signal Devices":

NEC Application Note (TEM-3004)

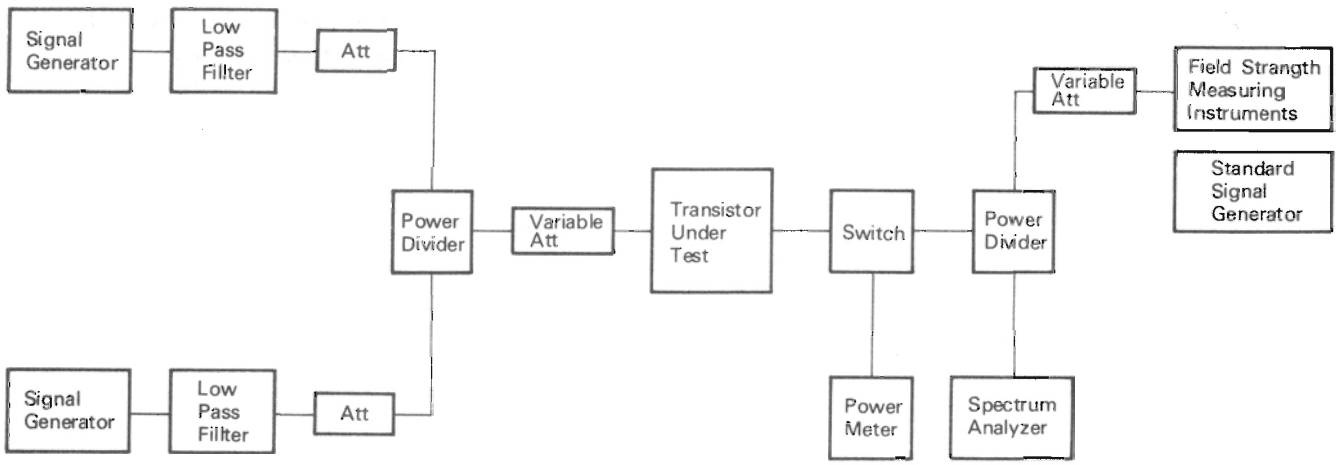
"Disk Mold Transistors, FET, and Diode Quad":

NEC Application Note (TS-1007)



$$NF = NF_1 + \frac{NF_2 - 1}{G_1}$$

Appended Fig.1 Measurement Network of G_s and NF for Wide-Band and Low-Noise Amplifier Transistors



Appended Fig.2 Measurement Network of the Distortion

PLASTIC MOLD-PACKAGED LOW NOISE MICROWAVE TRANSISTORS FOR CONSUMER MICROWAVE APPLICATIONS —APPLICATION OF 2SC3355 SERIES—

1. INTRODUCTION

Recently, the use of ultra high frequency (microwave) transistors has extended to various ultra high frequency products such as IF amplifiers for TV sets, VTR boosters, CATV converters, Personal Radio, Cellular systems and many other consumer products, in addition to the conventional low-noise applications on communication and instrumentation equipment and to the conventional low-noise and low-distortion applications in wideband boosters for TV antenna.

Following an above mentioned consumer use of microwave transistors, development of inexpensive plastic mold-packaged transistors is intensely desired instead of conventional can or ceramic packaged transistors.

This application note describes the optimal electrical characteristics and applications for consumer microwave circuits available with different packages of 2SC3355 series that are developed with one of our new microwave transistor production techniques, it is called Direct Nitride Passivated Base Surface Process (DNP Process) which is given better RF characteristics and reliability.

Photo 1 is transistor chip of 2SC3355 series and Fig. 1 shows NF and collector current response (comparison with our previous products.)

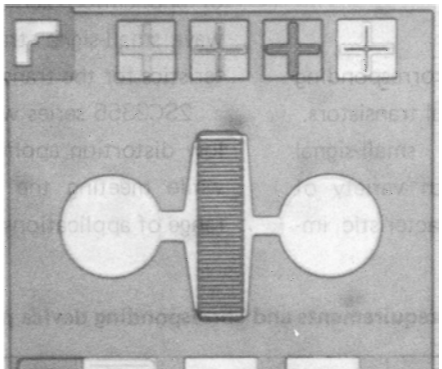


Photo 1 Transistor chip of 2SC3355 series

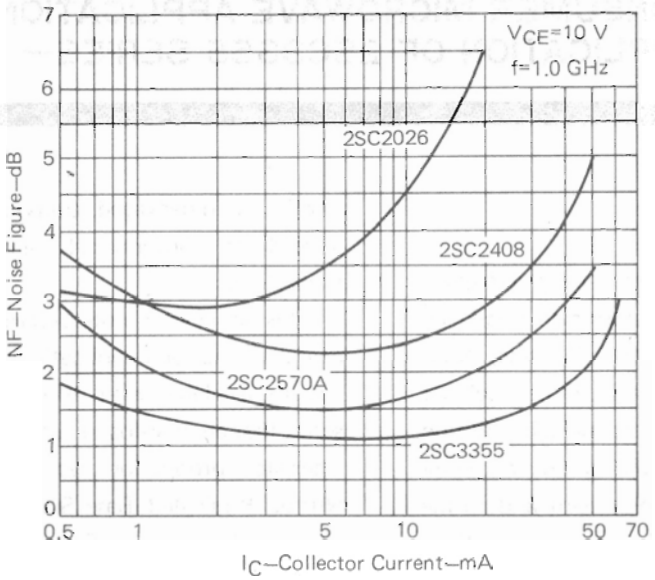


Fig. 1 NF and collector current response (comparison with our previous products)

2. 2SC3355 SERIES – LOW NOISE MICROWAVE TRANSISTORS

Table 1 shows application requests and corresponding device parameters for microwave small-signal transistors.

Application of consumer microwave small-signal transistors has been expanded along with variety of consumer products and requests of characteristic improvement at consumer products. These wide expanses of application demand various characteristic of microwave small-signal transistors, therefore, specific characteristics for the transistor used is intensely required.

2SC3355 series was designed for low noise, high gain, low distortion applications in the VHF and UHF bands while meeting the specific requirements for a broad range of applications.

Table 1 Application requirements and corresponding device parameters

Requirement	Device Parameter
(1) Low Noise Amplifier	Reduced $r_{b'b}$
(2) High Gain Amplifier	Higher f_T
(3) Low Noise, Low Distortion Amplifier	Extended dynamic range and improved NF current response
(4) High power Amplifier	Extended dynamic range

2-1. BASIC CHARACTERISTICS OF 2SC3355

Table 2 shows the features of 2SC3355

Table 2 Feature of 2SC3355

Feature	Note
Good linearity	Flat h_{FE} response in the low current area
Broad dynamic range	1 dB compression is +20 dBm (@ I_C=40 mA). Maximum value of IC is 100 mA.
Low Noise Figure	NF=1.1 dB (@ I_C=7 mA, f=1.0 GHz)
Broad NF dynamic range	NF=1.8 dB (@ I_C=1.5 to 4.0 mA, f=1.0 GHz)
High Gain	$\|S_{21e}\|^2$=9.5 dB (@ I_C=20 mA, f=1.0 GHz)

Table 3 and 4 show the absolute maximum ratings and electrical characteristics of 2SC3355, respectively. Fig. 2 through 12 show the basic characteristics of 2SC3355.

Table 3 Absolute maximum ratings of 2SC3355 (T_a = 25 °C)

Item	Symbol	Rating	Unit
Collector to Base Voltage	V_{CBO}	20	V
Collector to Emitter Voltage	V_{CEO}	12	V
Emitter to Base Voltage	V_{EBO}	3.0	mA
Collector Current	I_C	100	mW
Total Power Dissipation	P_T	600	mW
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Table 4 Electrical characteristics of 2SC3355 (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Cutoff Current	I_{CBO}			1.0	μA	V_{CB}=10 V, I_E=0
Emitter Cutoff Current	I_{EBO}			1.0	μA	V_{EB}=1.0 V, I_C=0
DC Current Gain	h_{FE} *	50	120	300		V_{CE}=10 V, I_C=20 mA
Gain Bandwidth Product	f_T		6.5		GHz	V_{CE}=10 V, I_C=20 mA
Output Capacitance	C_{ob}**		0.65	1.0	pF	V_{CB}=10 V, I_E=0, f=1.0 MHz
Insertion Power Gain	$\|S_{21e}\|^2$		9.5		dB	V_{CE}=10 V, I_C=20 mA, f=1.0 GHz
Noise Figure	NF		1.1		dB	V_{CE}=10 V, I_C=7 mA, f=1.0 GHz
Noise Figure	NF		1.8	3.0	dB	V_{CE}=10 V, I_C=40 mA f=1.0 GHz

* Pulse measured (PW ≤ 350 μs, Duty Cycle ≤ 2 % Pulsed)

** The emitter and case terminal should be connected to the guard terminal of capacitance bridge.

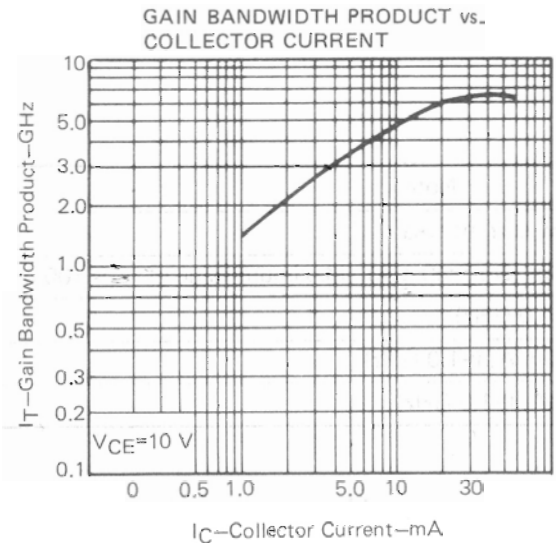


Fig. 2 h_{FE} vs. I_C (2SC3355)

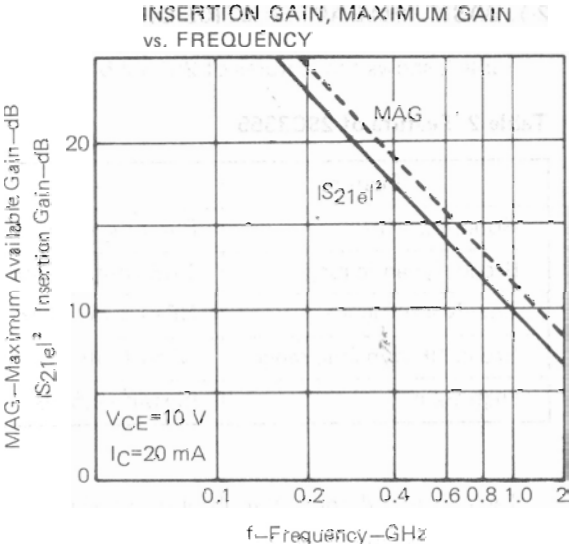


Fig. 3 $|S_{21e}|^2$ vs. I_C (2SC3355)

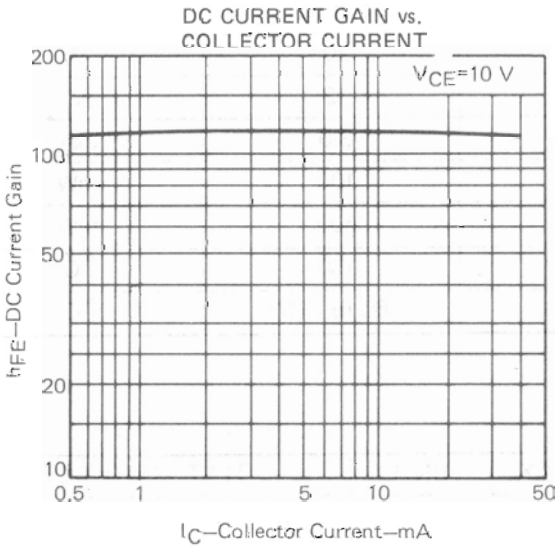


Fig. 4 f_T vs. I_C (2SC3355)

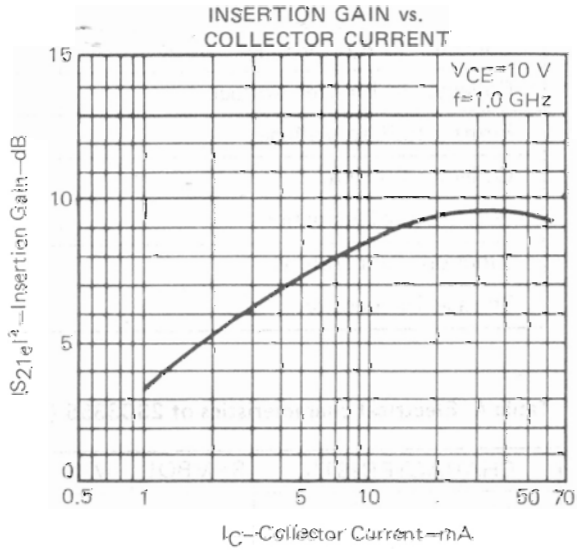
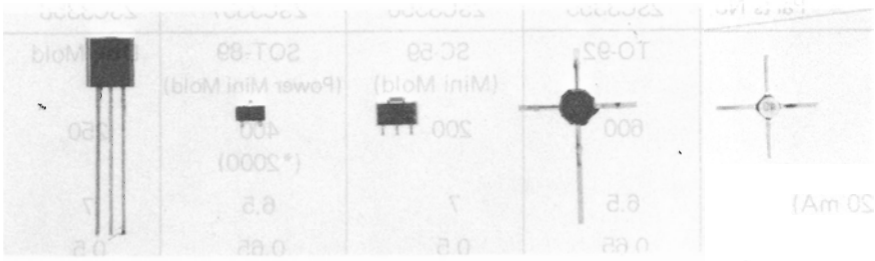


Fig. 5 $|S_{21e}|^2$, MAG vs. I_C (2SC3355)

3. CHARACTERISTICS OF 2SC3355 SERIES AND THE FEATURES OF SEVERAL PACKAGES



2SC3355 (TO-92) 2SC3356 (SC-59) 2SC3357 (SOT-89) 2SC3358 (DISK MOLD) 2SC3603 (μX)

Photo 2 2SC3355 series and outline of each package

Table 5 lists all device types in the 2SC3355 Series. All of these use the same chip. The slight characteristic differences between package types are due to different package capacitances. This section describes the features of the 2SC3355 series devices for each package. For more details for each package type, refer to TS-1007 Disk Mold Tr, FET, Diode Quad, and TEM-3004 Transistor Selection Guide for Non-Industrial and Consumer Use Small-Signal Devices.

Table 6 and 7 show the package capacitances for each package type and outline their features. Table 8 shows the aptitudes of each package type to applications. The RF characteristics vary by package capacitance, package construction, and other factors listed in Table 6 because these factors cause RF Loss. The influence of these factors on RF gain is greatest. The shape of the leads (frame) in the package also significantly influences the device gain. The influence on the noise figures (NF) is not very great, similar NF values were obtained for all package types.

The TO-92 package for RF use has center-emitter electrode construction, and is suited for RF applications that use emitter-common circuits. Because the TO-92 has a relatively high package capacitance, it has a deficiency in gain. The power mini mold package has center-collector construction for thermal resistance. Like the TO-92, it also has a deficiency in RF gain due to its relatively large package capacitance. The mini mold package has slightly better RF gain due to its small package capacitance. The disk mold and micro-X packages are well suited for RF applications. The disk mold type allows emitter-common connection using the emitter lead, and has high RF gain due to the input-output shield effect across the collector and base. The micro-X package, because of ultra-compact design, features low lead inductance and package capacitance, and has good RF gain from several GHz to several tens GHz.

Table 5 Device list of 2SC3355 series (typical value) (V_{CE} = 10 V, f = 1.0 GHz, T_a = 25 °C)

Item \ Parts No.	2SC3355	2SC3356	2SC3357	2SC3358	2SC3603
Package	TO-92	SC-59 (Mini Mold)	SOT-89 (Power Mini Mold)	Disk Mold	μX (Micro-X)
P_T (mW)	600	200	400 (*2000)	250	290
f_T (GHz) (I_C=20 mA)	6.5	7	6.5	7	7.5
C_{re} (pF)	0.65	0.5	0.65	0.5	0.4
G_a (dB) (I_C=7 mA)	9	11	9	12	15
$\|S_{21e}\|^2$ (dB) (I_C=20 mA)	9.5	11.5	9	13	15.5
MAG (dB) (I_C=20 mA)	11	13	11	15	18
NF (1) (dB) (I_C=7 mA)	1.1	1.1	1.1	1.1	1.1
NF (2) (dB) (I_C=20 mA)	1.8	—	1.8	—	—

* When a ceramic substrate of 2.5 cm x 0.7 mm is used.

Table 6 Case capacitance *1 of several packages

Case Capacitance Between Terminlas (pF) \ Package	TO-92 (E-Center)	Mini Mold	Power Mini Mold	Disk Mold *2	Micro-X
C_{B-E}	0.12	0.01	0.01	0.14	0.31
C_{C-E}	0.27	0.10	0.18	0.14	0.42
C_{C-B}	0.18	0.10	0.18	0.02	0.025

*1 Case capacitance is the capacitance between terminlas (there are electrodes) of the plastic molded package and without a chip (dice). The third terminal, with which no measurement is carried out is grounded on measurement.

*2 4 terminal Disk Mold is used, and it has double emitter structure.

Table 7 Features of several packages

Item / Package	Feature	P_T (mW) (Free Air)
TO-92	Easy handling Good compatibility	250 to 600 (at T_j MAX = 150 °C)
MINI MOLD	Ultra-miniature standard outline Small case capacitance	200 to 250 (at T_j MAX = 150 °C)
POWER MINI MOLD	Ultra-miniature standard outline Good thermal resistance	400 (2000*) (at T_j MAX = 150 °C)
DISK MOLD	Good RF characteristic emphasized Small case capacitance	250 (at T_j MAX = 150 °C)
Micro-X	Hermetic strip line structure Small lead inductance High reliability	200 to 300 (at T_j MAX = 150 °C)

* When a ceramic substrate of 2.5 cm x 0.7 mm is used.

Table 8 Aptitude of several packages

Item / Package	RF Response	Compact and Suitable for Automatic Mounting	Total Power Dissipation (P_T)
TO-92	△	△	◎
MINI MOLD	○	◎	△
POWER MINI MOLD	△	◎	◎
DISK MOLD	○	○	○
MICRO-X	◎	○	○

◎ . . . . . Excellent ○ . . . . . Good △ . . . . . Fine

Fig. 6 through 9 show the RF gain for different package types. Fig. 6 and 7 show the response of $|S_{21e}|^2$ and MAG and frequency, respectively. Fig. 8 shows the $|S_{21e}|^2$ and I_C response, and Fig. 16 shows the gain response for minimum NF (optimum NF tuning) and I_C.

The gain for package types were: 0.5 dB between the power mini mold and TO-92, 2 dB between TO-92 and the mini mold, 1.5 dB between the mini mold and disk mold, and 2.5 dB between the disk mold and micro-X. The difference between the power mini mold and micro-X was 6.5 dB. This indicates the importance of optimum package type selection in circuit design because the pellets used in each package are the same.

S-parameters of the 2SC3355 series devices are shown in Fig. 10 through 15. Fig. 10 through 12 show the S-parameter and IC responses, and Fig. 13 through 15 show the differences in the S-parameter between package types when I_C = 20 mA. This data indicates the importance of optimum design for each package type.

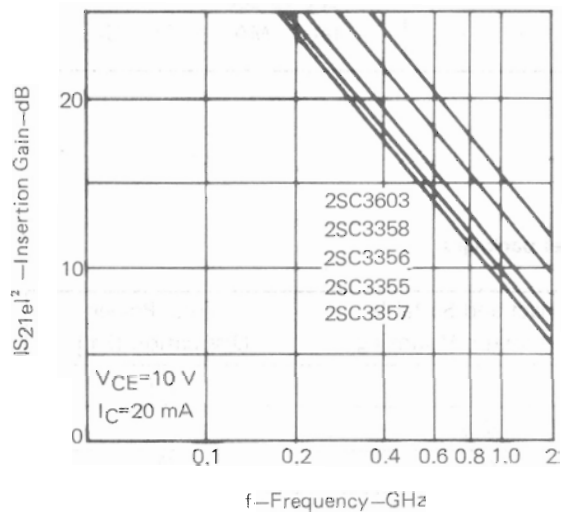


Fig. 6 $|S_{21e}|^2$ vs. Frequency (Several Packages)

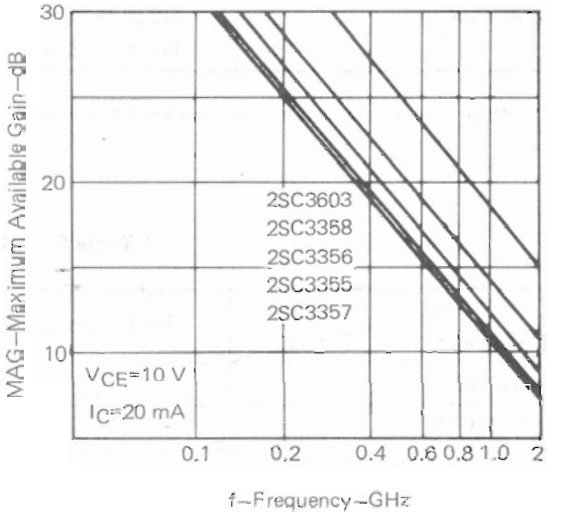


Fig. 7 MAG vs. Frequency (Several Packages)

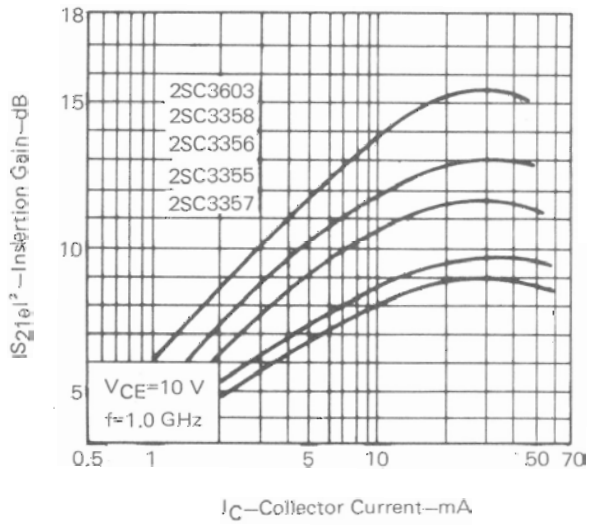


Fig. 8 $|S_{21e}|^2$ vs. I_C (Several Packages)

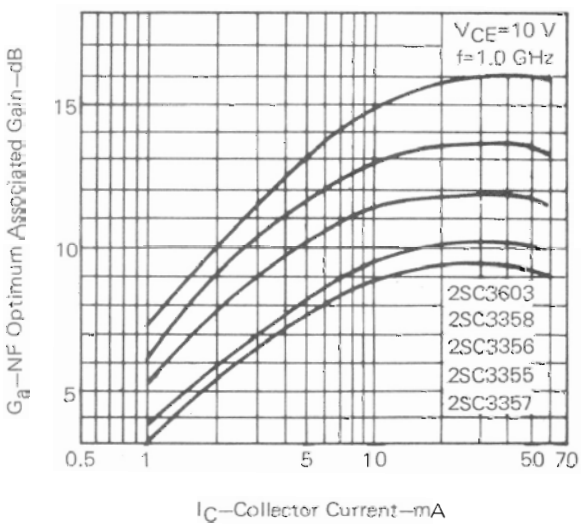


Fig. 9 G_a vs. I_C (Several Packages)

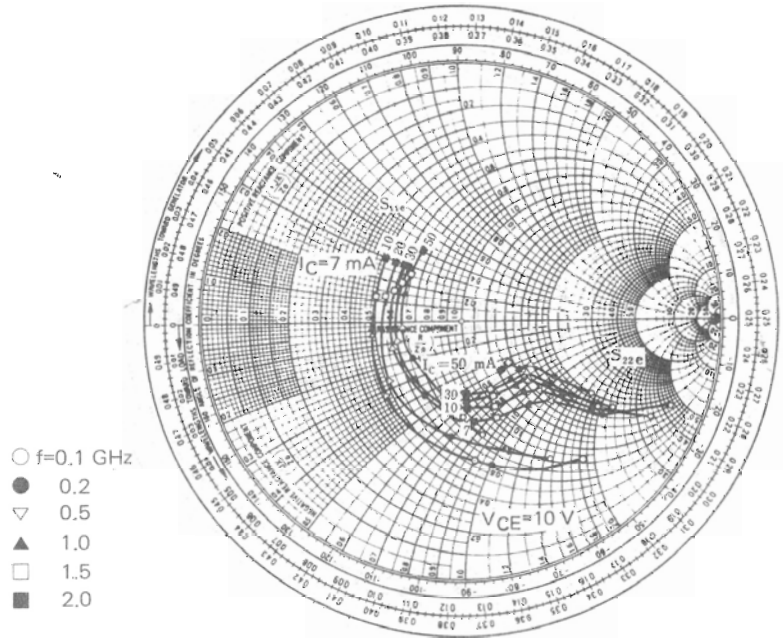


Fig. 10 S_{11e}, S_{22e} vs. I_C and f (2SC3355)

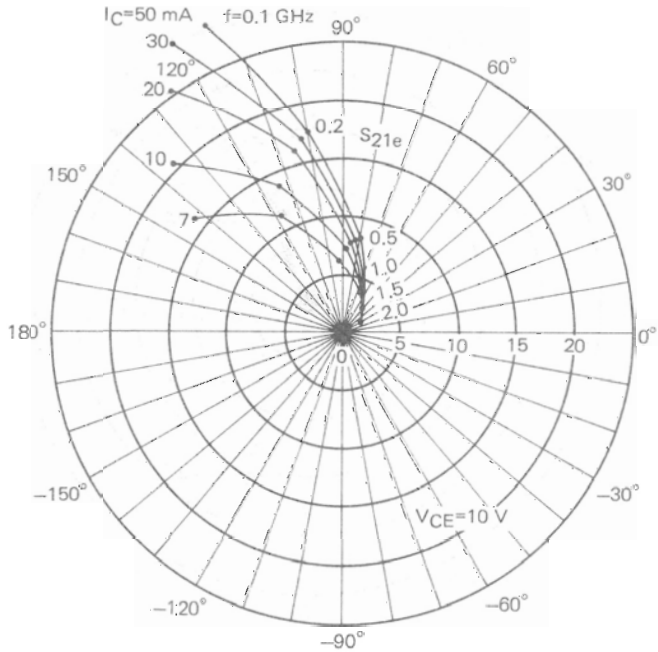


Fig. 11 S_{21e} vs. I_C and f (2SC3355)

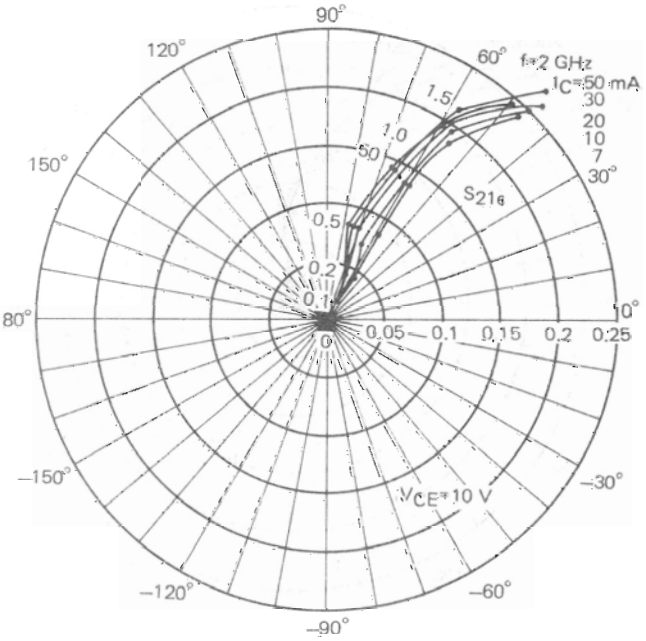


Fig. 12 S_{12e} vs. I_C and f (2SC3355)

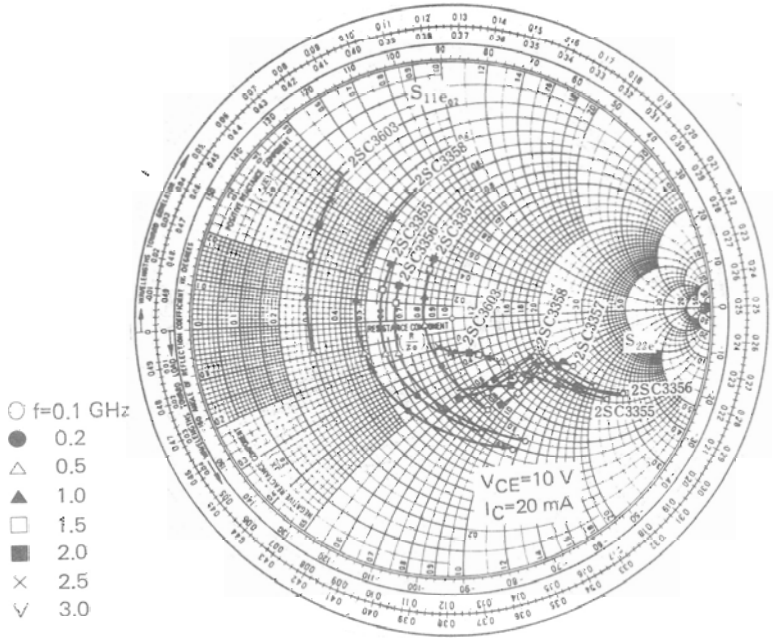


Fig. 13 S_{11e}, S_{22e} vs. f (Several Packages)

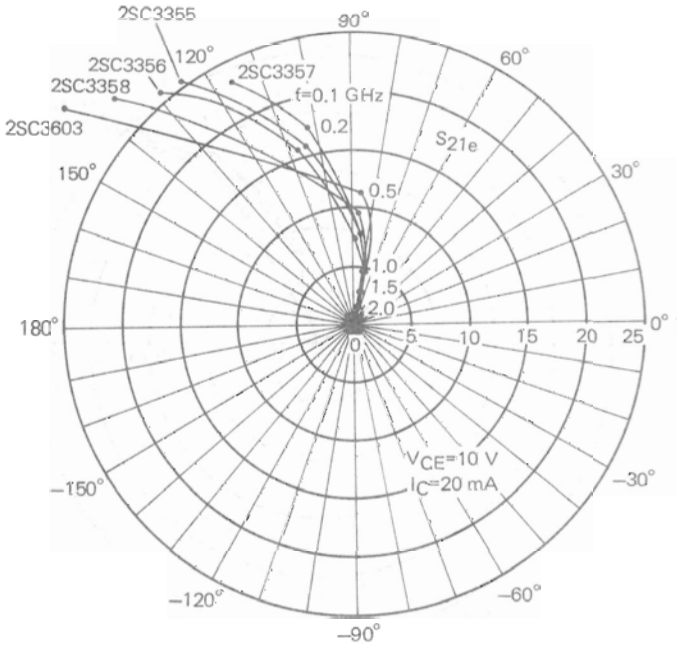


Fig. 14 S_{21e} vs. f (Several Packages)

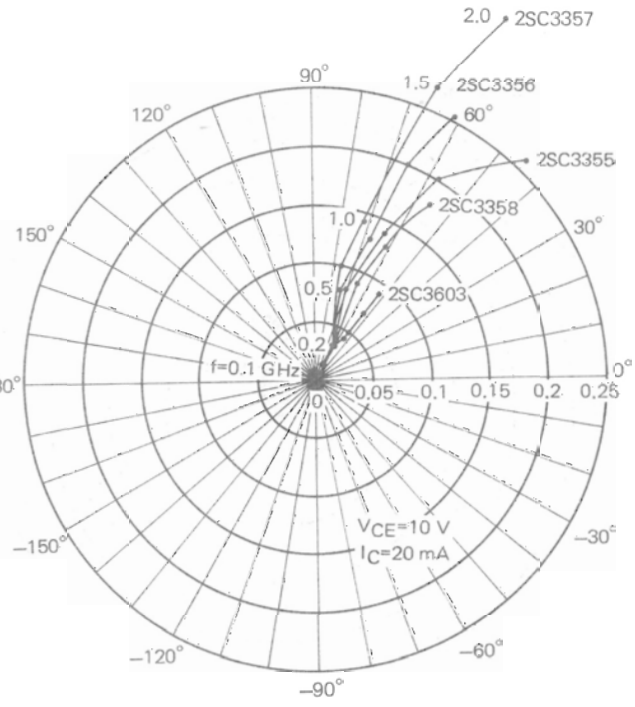


Fig. 15 S_{12e} vs. f (Several Packages)

4. APPLICATION OF THE 2SC3355 SERIES IN RF CIRCUITS

4.1 APPLICATION IN LOW NOISE, HIGH GAIN, LOW DISTORTION AMPLIFIERS

Fig. 16 and 17 show intermodulation IM_2 and IM_3 and collector current, respectively, with noise figures and collector current response. The second order intermodulation distortion IM_2 consists primarily of current and voltage distortions. The peak at around I_C = 50 mA in Fig. 16 is where the current and voltage distortion cancel each other. The third order intermodulation distortion IM_3 is mostly current distortion. The peak at around I_C = 40 to 50 mA in Fig. 17 is due to gain reduction in the device.

Because of the broad NF dynamic range [NF $\leqq$ 1.8 dB (f = 1.0 GHz) from I_C = 1.5 to 40 mA], a low distortion amplifier can be built using the 2SC3355 and 2SC3357 without adversely increasing noise. The devices have a gain saturation point at around over I_C = 30 to 40 mA, as shown in Fig. 3, therefore amplifiers with ultra low noise, low distortion, and high gain can be produced.

For practical applications, however, it is necessary to consider the dispersion of gain saturation point and collector current for individual devices, under the correlation with DC current amplification factor (h_{FE}) and other factors. Circuit design should, therefore, include a margin of 70 to 80 % with respect to the typical values. When distortion is the primary concern, a bias setting of around I_C = 31 to 36 mA seems optimum because the peak of IM_3 is around I_C = 45 mA as shown in Fig. 17. For this bias setting, a low noise, low distortion and high gain design is possible, for example NF = 1.5 to 1.7 dB, IM_2 = −43 dB, IM_3 = −73 dB, and G_a = 10 dB (TO-92).

For 2SC3356 or 2SC3358 devices with low total power dissipation, keeping within the allowable total power dissipation for the device is essential.

Fig. 19 shows the intermodulation distortions IM_2 and IM_3 and collector current, and Fig. 20 shows this distortion for forward insertion gain $|S_{21e}|^2$ and noise figure NF corresponding to collector-emitter voltage. The saturation point of IM_3 is inversely related to $|S_{21e}|^2$ as shown in Fig. 20, and IM_2 has an improved low current range due to a saturation point shift resulting from improved voltage distortion. Because the noise figure is not affected by variations in supply voltage, the NF and collector current response is the primary design factor for bias current setting, and the gain and IM_2, IM_3 to voltage response are the primary design factor for setting bias voltage.

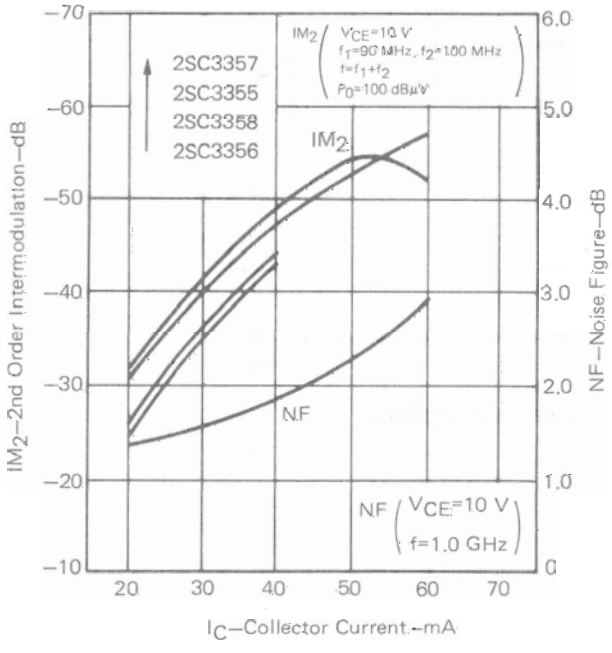


Fig. 16 IM_2, NF vs. I_C

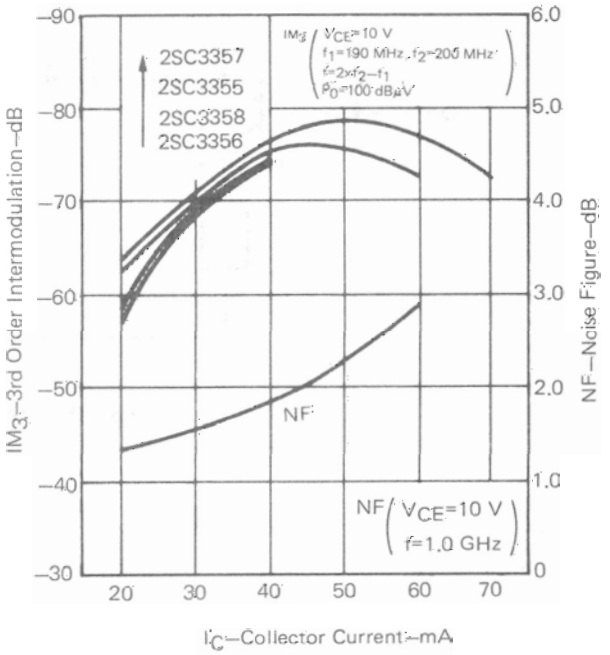


Fig. 17 IM_3, NF vs. I_C

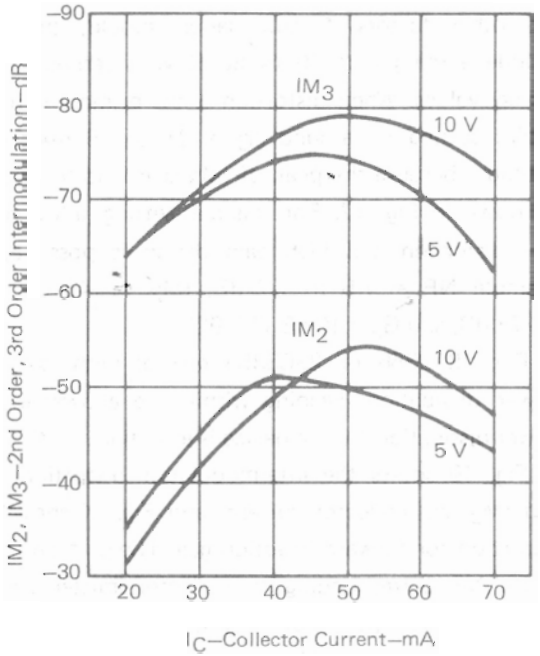


Fig. 18 IM_2, IM_3, vs. I_C and V_{CE}

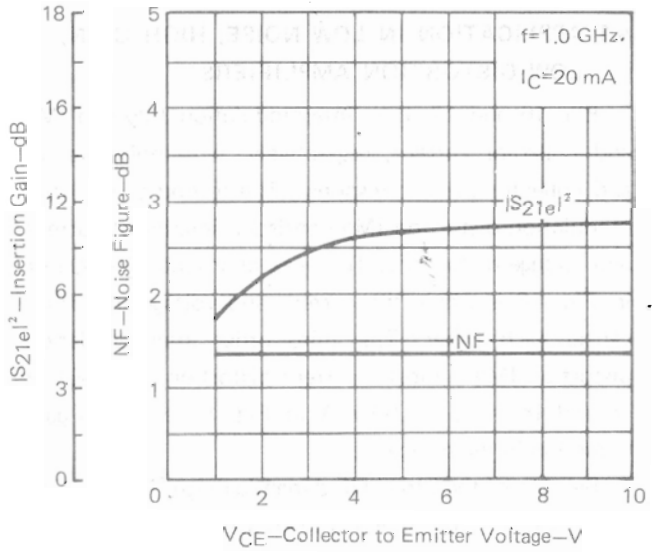


Fig. 19 $|S_{21e}|^2$, NF vs. V_{CE}

4.2 APPLICATION TO WIDE BAND, LOW NOISE AMPLIFIER CIRCUITS

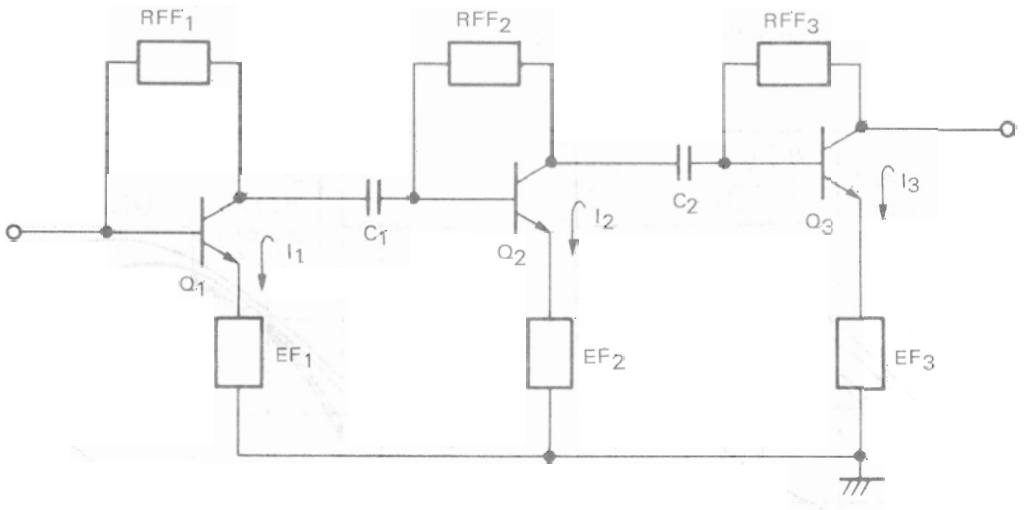


Fig. 20 Three-stage wide band amplifier

The following describes the use of the 2SC3355 Series in three-stage, low noise, wide band amplifiers.

Fig. 20 shows a block diagram of the three-stage amplifier. The amplifier uses RF feedback from the collector to base (RFF_1, RFF_2 and RFF_3), and emitter feedback (EF_1, EF_2 and EF_3) for a wide band. C_1 and C_2 are inter-stage coupling capacitors. The amplifier parameters are calculated using the following equations:

$$\text{Total Gain} = G_{Q1} + G_{Q2} + G_{Q3} \quad \ldots\ldots\ldots\ldots (1)$$

$$\text{Total NF} = NF_{Q1} + \frac{NF_{Q2} - 1}{G_{Q1}} + \frac{NF_{Q3} - 1}{G_{Q2}} \quad \ldots\ldots (2)$$

The third intermodulation distortion is expressed by the following equation:

$$IM_3 = 2\,(I.P. - P_O) \quad \ldots\ldots\ldots\ldots\ldots (3)$$

Where, I.P. : Intercept point

P_O : Output power

The second intermodulation distortion is seriously affected by the input-output matching (phasing) of the transistors.

The gain distribution for each stage, NF distribution, and optimum bias can be determined by using the transistor specifications.

Equation 1 shows that overall gain is the sum of the gain for each transistor. Equation 2 shows that the overall noise (NF) is determined by the first stage.

Distortion can generally be improved by optimizing the collector current for each transistor, and the third intermodulation distortion is correlated to output power, as calculated by equation 3. For example, IM_3 can be improved by 10 dB by suppressing the output power 5 dB.

The above discussions suggest that the following points should be considered when designing a low noise, low distortion, wide band amplifier:

(1) Minimize the noise figure in the first stage (Q_1)

(2) IM_3 of Q_2 and Q_3 are improved by selecting the optimum point for collector current response.

(3) IM_3 of Q_1 is improved by gain distribution based on the following equation: [(Q_1 output power) = (Q_3 output power) − ($G_{Q2} + G_{Q3}$)].

(4) IM_2 is affected primarily by phase matching of input and output.

(5) Select devices with the best specifications.

Table 9 shows a basic design concept for gain, noise figure, and bias for transistor characteristics.

Table 9 Basic circuit design for specific transistor characteristics

Required Performance	Selecting Point of Transistor Feature	Bias Point
Low-Noise	Select the lowest NF point for the NF and IC response.	at the low current range (several mA)
High-Gain	Select the highest gain for gain and IC response.	at the large current range (20 to 40 mA)
Low distortion	Select the lowest distortion point for the distortion and IC response, and suppress the transistor output power.	at the large current range (30 to 50 mA) Inter-stage gain distribution and gain for each transistor should be optimized.

Fig. 21 and 22 show the input-output response of the 2SC3355. At the point of P_{out} = −7 dBmW/50 Ω (100 dBμV), IM_3 is 75 dB when I_C is 40 mA. The NF and collector current shown in Fig. 1 shows that the noise figure of the 2SC3355 is minimized at a collector current of 7 mA. Fig. 22 provides the input-output response for a collector current of 7 mA, whereas IM_3 is 45 dB that is at the point of P_{OUT} = −7 dBmW/50 Ω (100 dBμV). If the output power of the final stage of a three-stage amplifier is assumed to be −7 dBmW/50 Ω (100 dBμV), and the gain in the second and third stages is 10 dB, then the output power of the first stage is −27 dBmW/50 Ω (80 dBμV). At this point, IM_3 at the first stage becomes 85 dB that is remarkable improvement at the value of 40 dB. This result is also calculated by equation 3.

We have looked at the importance of adequate interstage gain distribution. The noise figure for the first stage may be minimized for a low noise, low distortion amplifier.

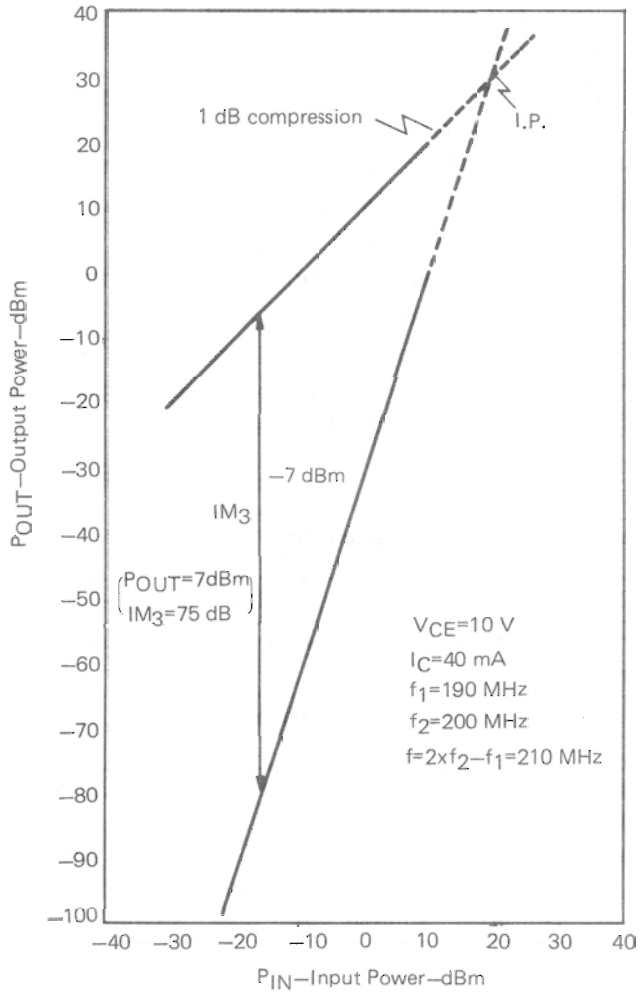


Fig. 21 P_{IN} vs. P_{OUT} (1) (2SC3355)

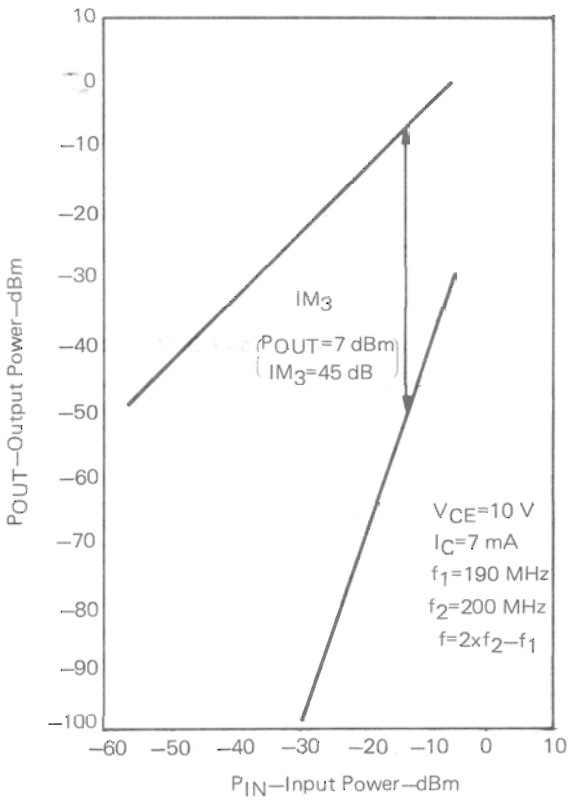


Fig. 22 P_{IN} vs. P_{OUT} (2) (2SC3355)

Figs. 23 and 24 show the characteristics of three-stage, wide band amplifier using the 2SC3355.

When supply voltage is V_{CC} = 12 V and the current bias setting is I_{CC} = 50 mA, the following performance is obtained from 40 to 900 MHz:

G_V = 28 dB, NF = 2.5 dB or less

Also IM_2 = 50 dB and IM_3 = 65 dB are obtained when P_{OUT} = 100 dBμV.

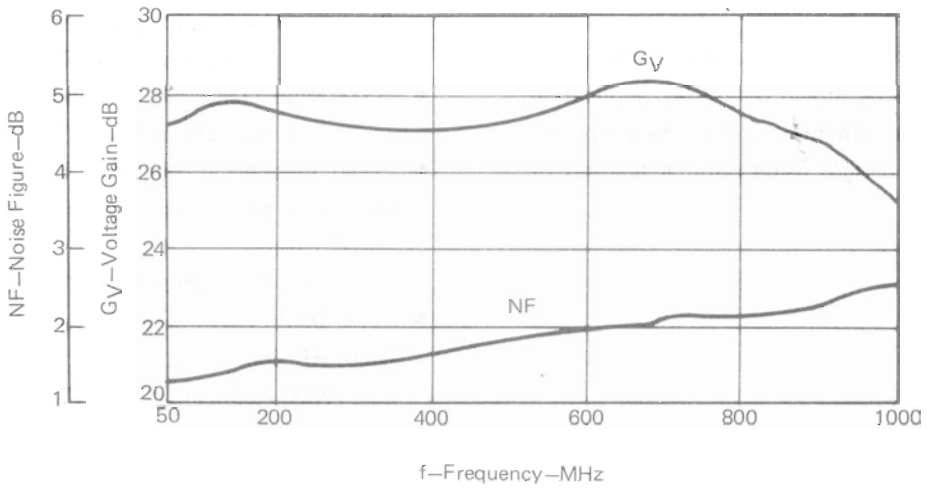


Fig. 23 A three-stage, wide band amplifier characteristics (1) using the 2SC3355 (NF, G_V vs. f)

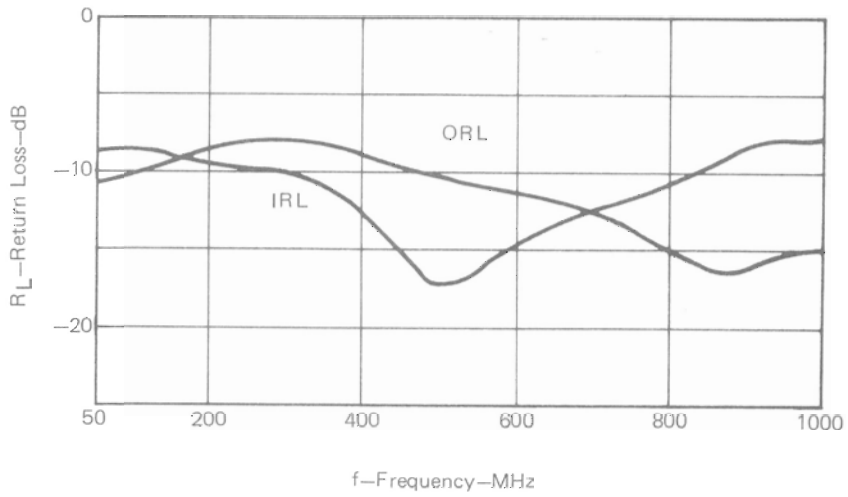


Fig. 24 A three-stage, wide band amplifier characteristics (2) using the 2SC3355 (IRL, ORL vs. f)

5. CONCLUSION

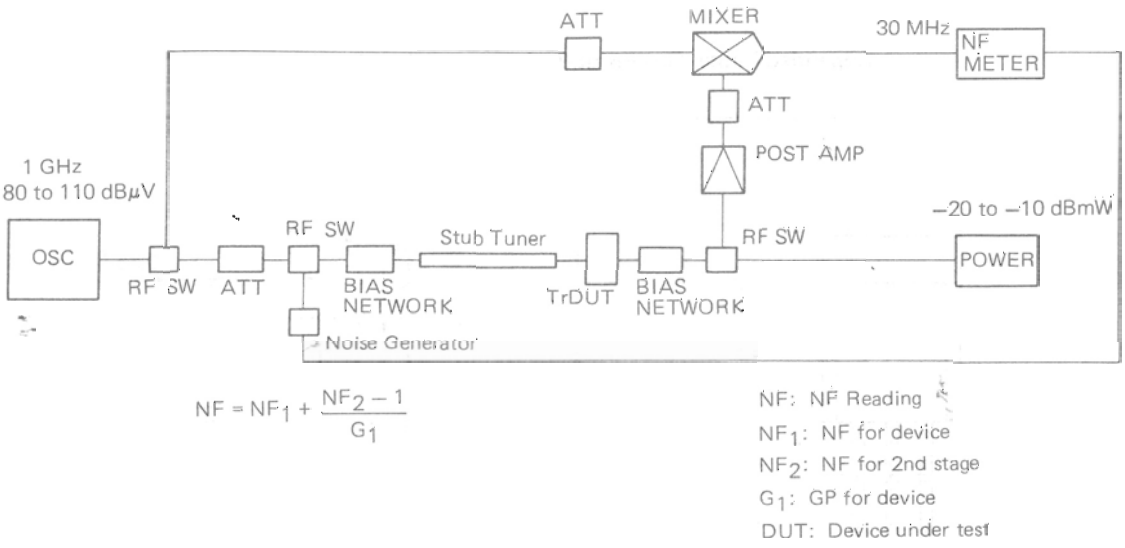
The features of 2SC3355 series (f_T = 7.0 GHz) fabricated using the DNP Process were described for each package. And also, design approaches for RF amplifiers using 2SC3355 series devices were discussed and application examples were given.

Transistor applications in the RF field include a wide application range, and we shown only a few application examples in this note. We hope circuit designers will make suitable circuit designs using optimal features of the 2SC3355 series.

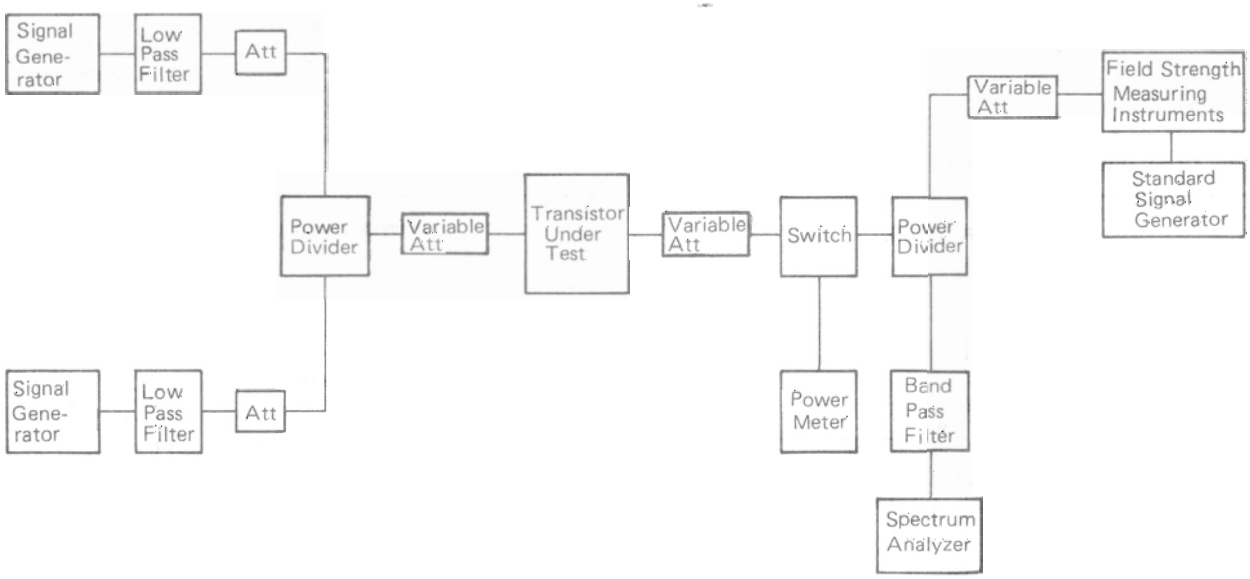
6. APPENDIX

Below materials with more detailed descriptions are listed together with those already mentioned in this note.

- "Transistor Selection Guide for Non-Industrial and Consumer Use Small-Signal Devices."
  : NEC Application Note (TEM-3004)
- "Disk Mold Transistor, FET and Diode Quad."
  : NEC Application Note (TS-1007)
- "High Frequency Low Noise Transistors for VHF and UHF Band Applications — Application of 2SC2570A —."
  : NEC Application Note (TEA-1027)
- "The DNP PROCESS and Its Application to Low Noise RF Transistors."
  : NEC Application Note (TEA-1030)



Appended Fig. 1 Measurement Network of G_S and NF for Wide Band and Low Noise Amplifier Transistors

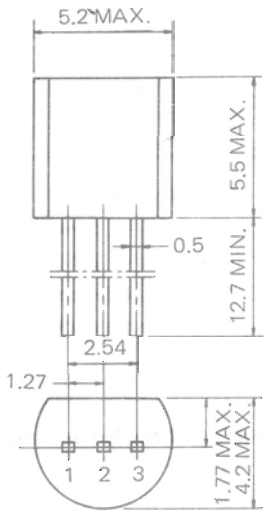


Appended Fig. 2 Measurement Network of the Distortion

Appended Table Groups of Packages and their Outlines

Unit: mm

TO-92

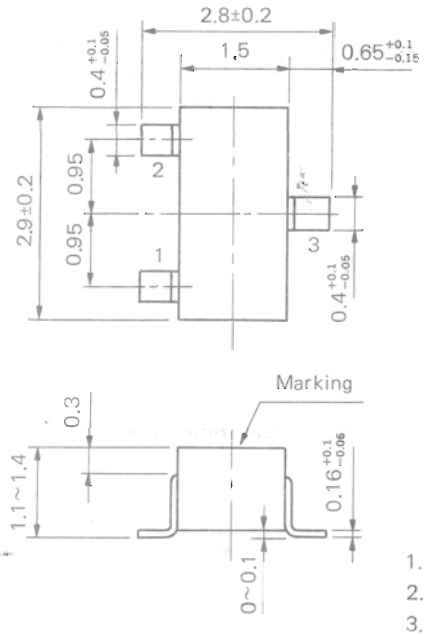


1. Base
2. Emitter
3. Collector

EIAJ: SC-43B
JEDEC: TO-92
IEC: PA-33

* Low cost, good compatibility

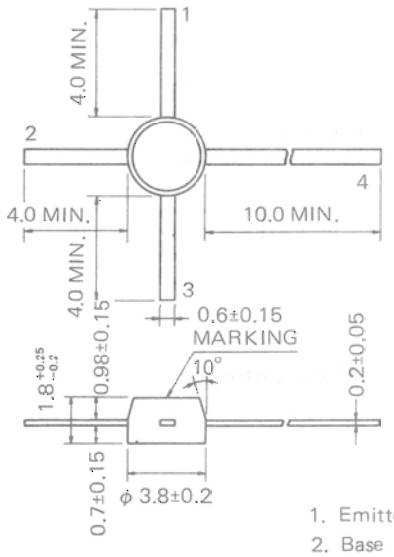
MINI MOLD



1. Emitter
2. Base
3. Collector

* Most suitable for automatic mounting and miniaturization

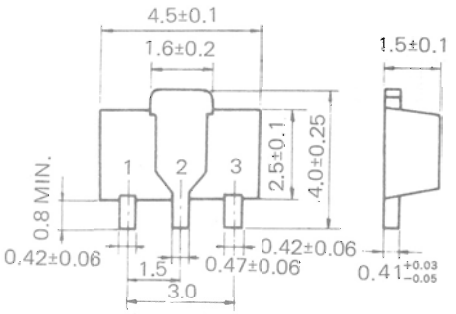
DISK MOLD



1. Emitter
2. Base
3. Emitter
4. Collector

* Automatic mounting and high frequency characteristic emphasized

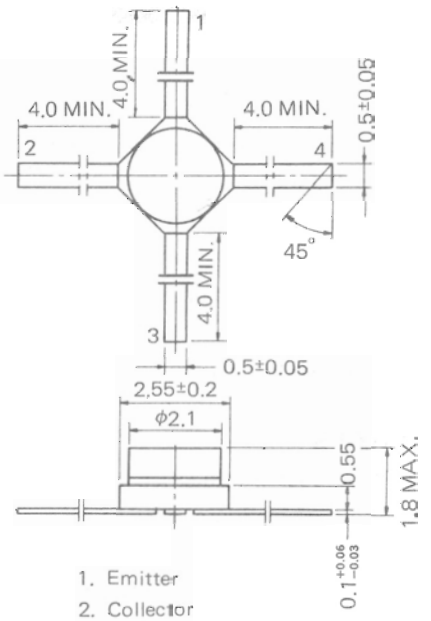
POWER MINI MOLD



1. Emitter
2. Collector
3. Base

* Most suitale for automatic mounting and miniaturization
* Good heat dissipation

MICRO-X



1. Emitter
2. Collector
3. Emitter
4. Base

* For micro wave low-noise amplifier

NEC PIN DIODES AND APPLICATIONS

Recently the use of PIN diodes has been spread in a very wide range from kHz bands to millimeter wave bands. A variety of PIN diodes are required in diversified fields of application.

NEC's PIN diodes are produced, in accordance with those requirements, to cover all the fields of applications from kHz bands to millimeter wave bands with their well-defined types and specifications.

Today, the PIN diodes may be classified into five types described below according to their usages. They are:

(1) Variable resistance elements which are controlled with low distortion by forward current, such as AGC circuit.

(2) Radio-frequency switching elements with low insertion loss and high isolation, such as microwave switching circuit. (controlled by zero or reverse bias vs. forward bias)

(3) Ultra-high-frequency switching elements with very high speed and very low transmission and reflection losses, such as PCM phase modulating PIN diodes.

(4) AM modulaing elements for frequencies of microwave or higher. (which may be regarded as high speed switching)

(5) High-power pulse controlling elements, such as PIN diode limiter which is a solid-state version of TR tube in radar system.

This document introduces NEC's PIN diodes and describes their adaptability, use and characteristics.

1. GENERALS

NEC's PIN diodes are classified as described below according to their semicoductor structures.

(1) N-base PIN diodes

The diodes are divided into two types according to the thickness and resistivity of the I-layer.

(a) Middle speed (about 100 ns) type

PIN diodes for radio fequency (VHF or beyond) ---Mainly used in microwave-band AGC circuit and switching circuit, they will be the main products in switching elements for phased-array radars because they have the most suitable characteristics for these purposes.

Table 1 List of NEC's PIN Diode

Classification		Type	Package	Outline	Characteristics	Use
N-base PIN diode	Middle Speed	1SV27	Ceramic	Fig. 1	V_R(10μA)≧100V, Ct(−6V)≦0.35pF, ISO (7GHz, 0V)≧25dB, Li (7GHz, 20mA)≦0.2dB	Wave-guide ATT, AGC, SW
		1SV26		Fig. 2	V_R(10μA)≧100V, Ct(−6V)≦0.35pF, r_{ds} (10mA)=1.6~3.6Ω, r_{dp} (10μA)=300~500Ω	μ-wave IC ATT, AGC, SW
		1SV28		Fig. 3	V_R(10μA)≧100V, Ct(−6V)≦0.25pF, r_{ds} (10mA)=1.6~3.6Ω, r_{dp} (10μA)=300~500Ω	Same as above
	High Speed	1SV46	Ceramic	Fig. 3	V_R(10μA)≧ 60V, Cj(−10V)=0.1~0.2pF, Li (20GHz, 25dBm)≦0.7dB	μ-wave IC, SW, AM
		1SV47		Fig. 1	V_R(10μA)≧ 60V, Cj(−10V)=0.1~0.2pF, Li (20GHz, 25dBm)≦0.7dB	Wave-guide, SW, AM
		1SV48		Fig. 1	V_R(10μA)≧ 30V, Cj(−10V)=0.18~0.36pF, Li (20GHz, 25dBm)≦1.0dB	Wave-guide, SW, AM
		1SV65		Fig. 4	V_R(10μA)≧ 30V, Cj(−10V)=0.09~0.18pF, Li (20GHz, 25dBm)≦0.9dB	Phase modulation for quasi-millimeter wave PCM
		1SV66		Fig. 4	V_R(10μA)≧ 30V, Cj(−10V)=0.09~0.18pF, Li (20GHz, 25dBm)≦0.9dB	Phase modulation for quasi-millimeter wave PCM
P-base PIN diode	Low Speed	1SV37	Ceramic	Fig. 1	V_R(10μA)≧100V, Ct(−50V)≦0.6pF, r_{ds}(10mA)=6~10Ω, r_{dp}(10μA)≧2kΩ	Wave-guide ATT, AGC, SW
		1SV36		Fig. 2	V_R(10μA)≧100V, Ct(−50V)≦0.6pF, r_{ds}(10mA)=6~10Ω, r_{dp}(10μA)≧2kΩ	μ-wave IC ATT, AGC, SW
		1SV35	Glass	Fig. 5	V_R(10μA)≧100V, Ct(−50V)≦0.5pF, r_{ds} (10mA)=6~10Ω, r_{dp}(10μA)≧2kΩ	V-UHF ATT, AGC, SW
		1SV34		Fig. 5	V_R(10μA)≧100V, Ct(−50V)≦0.5pF, r_{ds} (10mA)=6~10Ω, r_{dp}(10μA)≧2kΩ	Consumer V-UHF ATT, AGC, SW
		1SV80		Fig. 5	V_R(10μA)≧ 30V, Ct(−15V)≦0.5pF, r_{ds}(10mA)≦15Ω, r_{dp}(10μA)≧1kΩ	Consumer V-UHF ATT, AGC, SW
High Speed Pulse		ND702B	Module	Fig. 24	Li(9.4GHz, 0.1mW)≦1.2dB, P_i(9375MHz, 0~2kW, 1.0μs, 1kHz)≦200mW	Diode limiter for marine rader

(b) High speed (0.5–20 ns) type

PIN diodes for ultra-high frequency (microwave band or beyond)———They are principally used as phase modulators. They are now attracting attention in every frequency band from microwave to millimeter wave and are begining to use. Other new usages such as high-speed AM modulator and high-speed passive limiter are expected.

(2) P-base PIN diodes

Those PIN diodes with thick I-layer and high resistivity are now peoduced. They can be classified into various usages according to thier package structures and their design concepts. Details of the types are described in Table 1. These PIN diodes in used in every field where specially high-speed response is not required. Namely, they are used in any AGC and switching circuit or high-power active limiter around 1 MHz or higher.

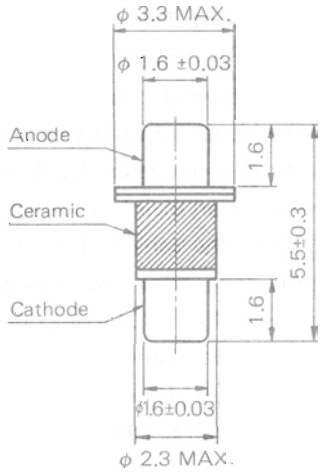


Fig. 1 Prong Package (Unit: mm)
(1SV27, 1SV37, 1SV47, 1SV48)

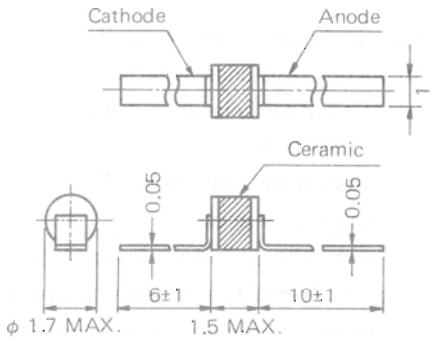


Fig. 2 Ribbon Package (Unit: mm)
(1SV26, 1SV36)

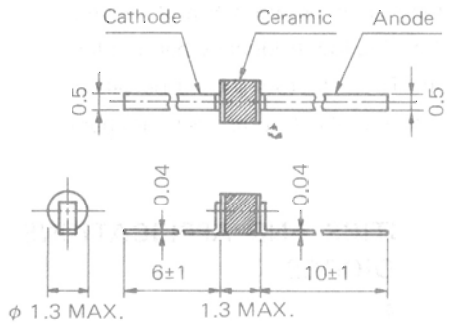


Fig. 3 Small Ribbon Package (Unit: mm)
(1SV28)

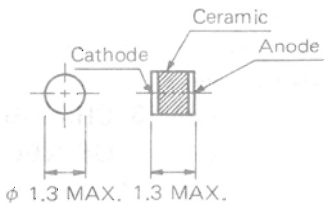


Fig. 4 Ribbon less Package
(Unit: mm)
(1SV65, 1SV66)

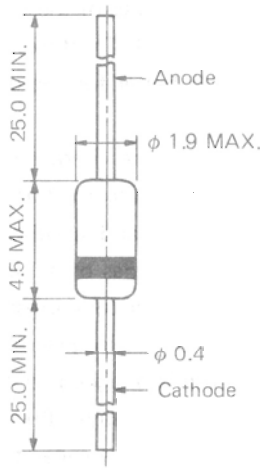


Fig. 5 JEDEC: DO-35 Glass Package
(Unit: mm)
(1SV34, 1SV35, 1SV80)

2. PERFORMANCE PRINCIPLE OF PIN DIODE

Fig. 6 shows the basic structure of PIN diode.

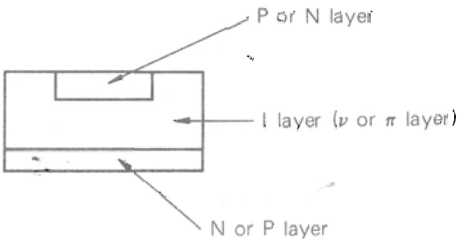


Fig. 6 Structure of NEC's PIN Diode

(In N-base PIN diode, say P-I-N junctions from the top, whereas for P-base PIN diode, read the figure as N-I-P from the top.)

(1) By supplying of the forward current, the radio-frequency resistance linearly varies with amplitude variation at fairly large amplitudes.

(2) For a reverse bias of for a small forward bias, the capacitance for radio frequency is inherently constant and every small.

(3) For a middle or a large forward bias, the radio-frequency resistance is much smaller than its parallel reactance component and, conseqiently, its reactance component can be neglected.

The above characteristics are the reasons for PIN diodes being good variable resistors at radio frequencies. The rigorous analysis of these important characteristics is too complicated. Therfore, the following qualitative description is better for the understanding of the performance.

Summarizing the characteristics (1) through (3), a PIN diode can be regarded as a capacitor with an electrode of N-layer and another electrode of P-layer, formed of both sides of an insulating "I" layer, respectively. This model corresponds to zero or reverse-biased state. Since, in general, a PIN diode for radio-frequency use is designed to make a smaller area (facing area) than its I-layer thickness and to have a very small capacitance, the capacitance of the diode in this state is far smaller than that of other diode. In addition, the capacitance is determined by I-layer thickness only and it is independent of reverse bias voltage. Now, when the PIN diode is supplied the forward bias (viewed as a simple PN junction diode), this PIN structure shows an action that the holes injects from the P-layer to the I-layer and the electrons injects from the N-layer to the I-layer. The amount of injected electrons and holes are proportional to the forward current and to the carrier lifetimes of electrons and holes. Here, the forward current replenishes carriers which are destroyed in the I-layer or pushed out of the layer, and the carrier lifetimes are factors inverse to the speed of carrier annihilation in the I-layer.

As the lifetimes are longer, the carrier is stored easy in the I-layer.

When the carriers are stored in the I-layer, the specific resisitivity of the I-layer is decreased proportionally to the stored amount. This means that the insulating I-layer is converted to a resistance which varies proportionally with the forward current. P-and N-layers on both sides of the I-layer, which have low resistivity, act as electrodes in radio-frequency band, leaving no noticeable nonlinearity on their boundaries to the I-layer. Furthermore, when the carrier lifetimes in the I-layer are satisfactorily long compared with the period of radio-frequency signal, only DC component is effective for the carrier replenishment and radio-frequency component is almost in effective. Therefore the radio-frequency current is transported by a mechanism called "phase current" which is similare to the transport in metals. This property also indicates that the phase shift in current is not expected with respect to supplied radio-frequency voltage. In other words, the reactance is not observed.

The above expanation is based on the first order model of PIN diode performance.

Sometimes it is necessary to consider the presence of the intermediate layer between P and I-layers and the problem of limiting low frequency band in low-frequency operation. These factors should be taken into account in respective application as peculiar characteristics of each type of product.

3. CHARACTERISTICS AND APPLICATIONS OF NEC'S PIN DIODES

1. N-base PIN Diodes

(1) Middle-speed, radio-frequency use PIN diodes

These PIN diodes are the most generally used ones for microwave band and they have been used the most. Following five features are found in this type of PIN diodes.

① The variation of resistance is relatively large and it has very small distortion in microwave band.

② The response speed is relatively quick and they

can be used for amplitude modulation also.

③ The driving current is relatively small.

④ The electrostatic capacitance is very small in radio-frequency region.

⑤ These PIN diodes are produced in super-high reliable structure.

There are four kinds of packaging as shown in Figs. 1 through 4, to each of which certain type names are specified. The representative characteristic curves are shown in Fig. 7.

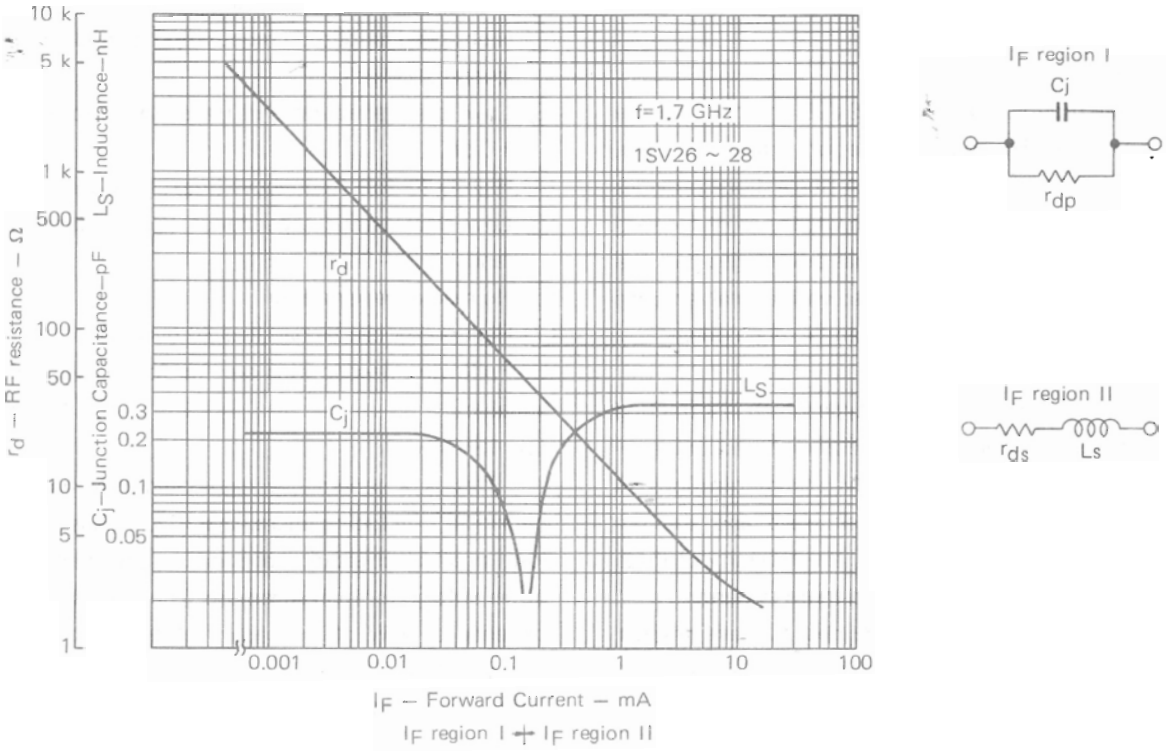


Fig. 7 RF Impedance Characteristics of PIN Diode (Ta = 25 °C)

Type names, characteristics specifications, packagings, and major usages are shown in Table 1. The points to be noted for each are described below.

(a) 1SV28

This is a general use PIN diode for hybrid IC including microwave IC. It is completely hermetic seal in a case with ceramic. It is formed very compact into an element which can be handled like a beam lead. The lead is made of hard material thickly plated with gold using either soldering of TC-bonding. It takes the advantage of package type with respect to sealing and handling as well as the merit of beam lead with respect to circuit mounting and circuit characteristics.

Since this package is designed to minimize the electrostatic capacitance and the impedance product in package also this PIN diode without lead can be used within a waveguide for guasi-millimeter or millimeter wave band. There are examples of this PIN diodes used for AGC and switching with good results. The major use of this type is found in attenuators with lumped constants such as bridged T composed of microwave IC's. An example is shown in Fig. 8.

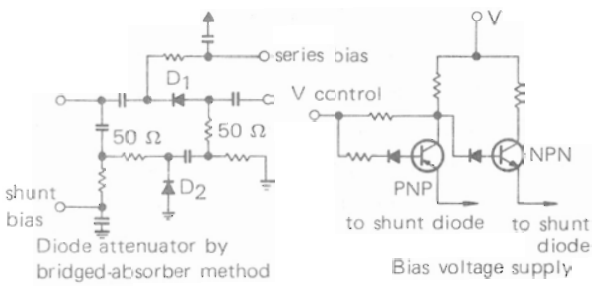


Fig. 8 Application of PIN Diode (1SV26, 1SV28, 1SV34, 1SV35, 1SV36)

(b) 1SV26

This is the high-reliability version of 1SV28. It is produced by super-high-reliability processes and the failure rate of this diode is conformed 10Fit or less presently. Concurrently its package is larger in size and its package capacitance is larger by 0.1 pF than 1SV28. The other characteristics of 1SV26 are all the same as 1SV28.

(c) 1SV27

This type is a version of 1SV28, intended for use in waveguide. The main application is line switching, different from that of 1SV28. A single diode provides an isolation of 30–40 dB when switched from forward to reverse biasing. The diode has advantages that the perfect ON-state can be provided with a small amount of forward current and it can handle much power.

(2) High-speed PIN Diodes

These diodes constitute a type which is attracting a growing attention recently. Especially accompanying with the progress of PCM communications in quasi-millimeter and millimeter wave and the demands for higher output signal, the necessity of these PIN diodes are getting more and more evident.

This type of diode is designed to have thinner I-layer for getting a satisfactorily small I-layer resistance even when the stored charge is less. The increase of the reverde capacitance due to the thinning of the layer is compensated by the reduction of junction area.

The fact that a satisfactory ON-state is maintained with small amount of stored charge means that the times of transitions OFF→ON and ON→Off are short. In addition, this nature results in a fast response speed of radio-frequency resistance to the variation of biasing current. Futhermore, this type of diode is designed to have smaller reflection and transmission lossed in ON and OFF actions, namely, a smaller radio-frequency loss component. The switching action of this diode can be rapidly actuated from ON-state in forward biasing to OFF state in reverse biasing only by momentarily supplying reverse current. This action is utilized in PCM communications that specially high-speed switching is demanded. Therfore, when PIN diodes of this type were first developed, the switching times were measured under the test conditions determined on the assumption of uses in a PCM system, and their ratings were so specified that they could be easily converted to the actual switching times. NEC's PIN diodes are now used as protectors of fine pulses surge and as passive limiters by virtue of their high-speed response speed, high cutoff frequency, and small electrostatic capacitance.

The festures of NEC's PIN diodes are:

① High-speed switching is capable (up to 0.5 ns).
② High-speed amplitude modulation is capable (up to several 10 MHz).
③ Low loss (reflection and transmission losses 0.3–1.0 dB)
④ High f_C (cutoff frequency) (max. 800 GHz)
⑤ Low electrostatic capacitance (Cj: junction capatance) 0.05–0.2 pF
⑥ No reactance variation.
⑦ High power can be handled. (0.5–4 W)

Following descriptions are for four types now available.

(a) 1SV46

This is a general-use high-speed PIN diode for hybrid IC's including microwave IC's. This is very low loss, small electrastatic capacitance, and high breakdown voltage for high-speed use. The diode has an experience of 4 W of workable high-frequency power. The switching time is longer than that of 1SV48. Its ratings and standard characteristics are shown in Table 1.

(b) 1SV47

This type is a version of 1SV46 to be mounted in waveguide.

(c) 1SV48

This PIN diode has been developed for direct phase modulation in PCM with particularly large bit numbers (400 Mbit or less). Because the use for large bundle lines is main use, its reliability is severly checked. The characteristic features of this type include, (1) a very fast response speed (2) a small driving power, and (3) the capability of switching up to the power level of transmission output. These features serve for an extreme simplification of transmission system and for a compactness of diode driving circuit, resultion in the economy of the system. Its ratings and standard characteristics are shown in Table 1. Its switching and impedance characteristics are shown in Fig. 9 and 10, respectively.

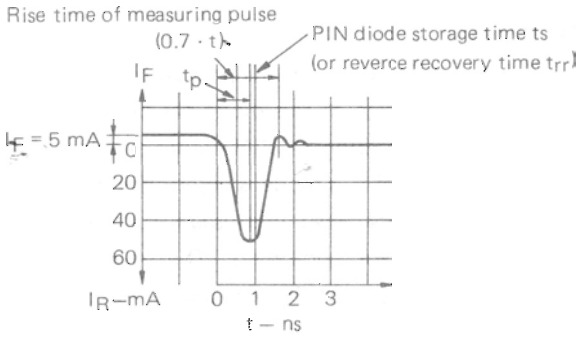
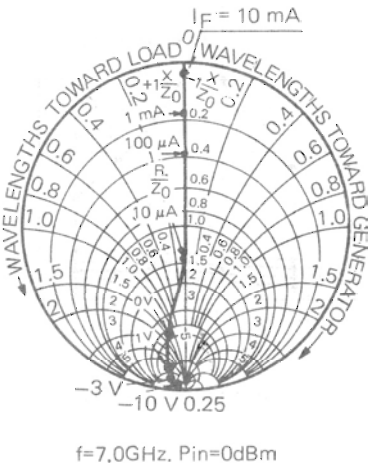


Fig. 9 Switching Characteristic of High-Speed PIN Diode 1SV48



f=7.0GHz, Pin=0dBm

Fig. 10 Impedance – Biasing Characteristic of High Speed PIN Diode 1SV48

(d) 1SV65

Contrasted to 1SV48 used as a high-speed PIN diode for quasi-millimeter wave, 1SV65 is used as high-speed PIN diode from quasi-millimeter to millimeter waves (20–40 GHz). The electrostatic capacitance is very much reduced concurrently. (Cj = 0.18 pF MAX)

(e) 1SV66

The bonding wire of this diode is reduced inductance for the use at higher frequencies than in 1SV65. (Ls = 0.1 nH)

2. P-base PIN Diodes

These diodes, are not classified by design principle. Unlike N-base PIN diodes, however, each of them is designed according to its purpose of use.

Since they have common structural natures of thick and highly resistivity I-layer , the following characteristic natures are resulted.

① Works with low distortion to low frequencies.
② High frequency electrostatic capacitance is small.
③ Special high power design is possible.
④ Resistance variation is very large.
⑤ Switches of high isolation can be formed with these PIN diodes.
⑥ Compared with N-base products, RF resistance is high in the same forward current.
⑦ Compared with N-base products, response speed is slow.

NEC's P-base PIN diodes are designed tc be fully utilized in a variety of usages.

The following descriptions will explain each type in detail.

(1) 1SV36

This diode is used super-wideband AGC curcuit from 500 kHz to microwave band. It is packaged in hermetic seal of ceramic. This is chiefly used for the mounting on hybrid IC, but, at the same time, it can be used as a general type with high reliability. In spite of its slow response speed, it will be PIN diode for AGC curcuit of communication and industry uses in the future, because it has features such as small parasitism capacitance, inductance, and junction capacitance, compact package, low distortion, and super-wide-band adaptability. The detailed description of characteristics is shown in Table. 1.

(2) 1SV37

This type is used for microwave line switching with high isolation and low insertion loss. As an element, it demonstrates simler characteristics to 1SV36. However, it is packaged for uses in waveguide. The standard specification of this PIN diode includes test conditions in microwave band, and its impedance against microwave is controlled, too. Furthermore, because heat dissipation from the package is good and the height of ceramic body is high, this PIN diode can withstand high power and high voltage and it can be used as a PIN diode for high voltage use. Fig. 11 shows the typical isolation and insertion loss of this diode mounting in waveguide.

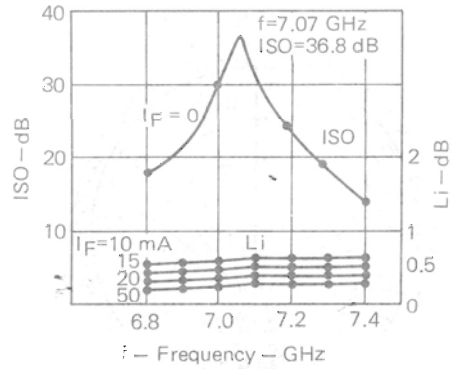


Fig. 11 Frequency Responce of ISO and Li of PIN Diode 1SV37

(3) 1SV35

This is a PIN diode for AGC curcuit from to 1 GHz. Its dimension is shown in Fig. 5. It is packaged in glass according to JEDEC: DO-35. The diode is principally used on printed curcuit board. The high reliability process is applied to make this diode and it is designed for the communication industry use under the specifications of the communication industry grade.

(4) 1SV34

This is a PIN diode for AGC curcuit from 1 MHz to 1 GHz. The design of this diode has been intended for the mass production of PIN diodes at a low cost. The specification of this diode is determined in accordance with the mass-consuming usages such at CATV and TV boosters for consumers. The frequency and biasing characteristics of RF resistance are shown in Figs. 12 and 13, respectively. A typical application to an attenuator and its characteristic curves are described in Figs. 14 and 15, respectively. Fig. 16–19 show typical applications to RF switches and their characteristics.

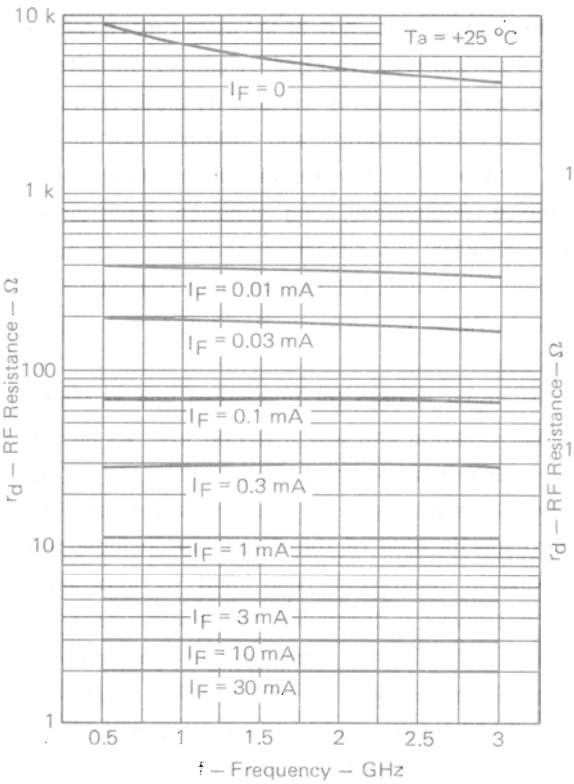


Fig. 12 r_d–f characteristic of PIN Diode 1SV34

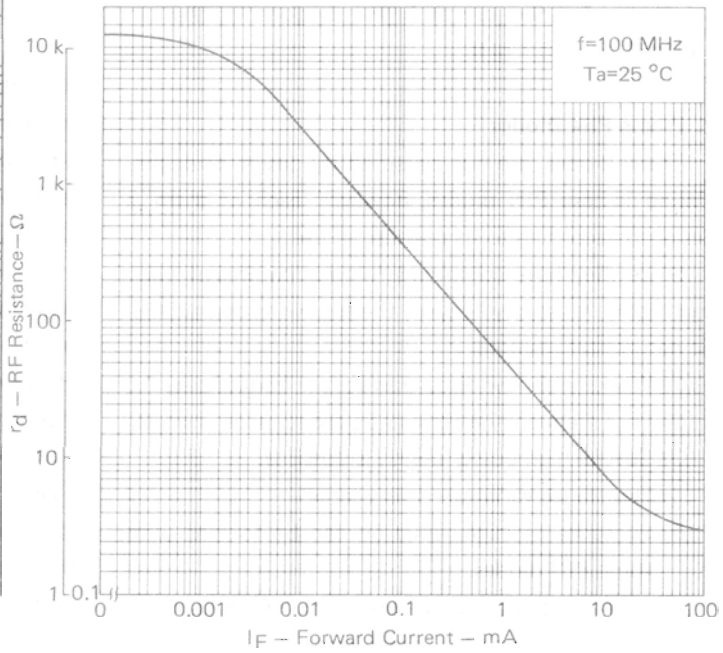


Fig. 13 r_d–I_F Characteristic of PIN Diode 1SV34

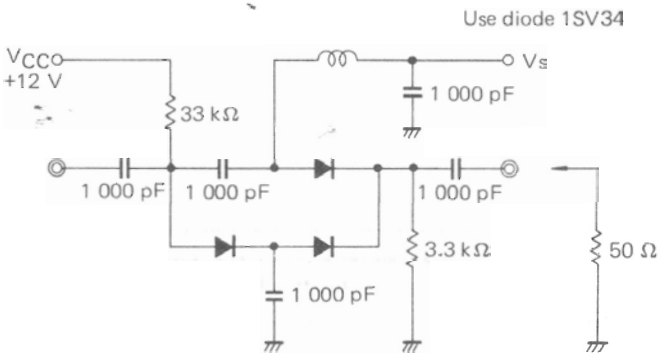


Fig. 14 Characteristic Circuit of π-type Diode Attenuator Using PIN Diodes 1SV34.

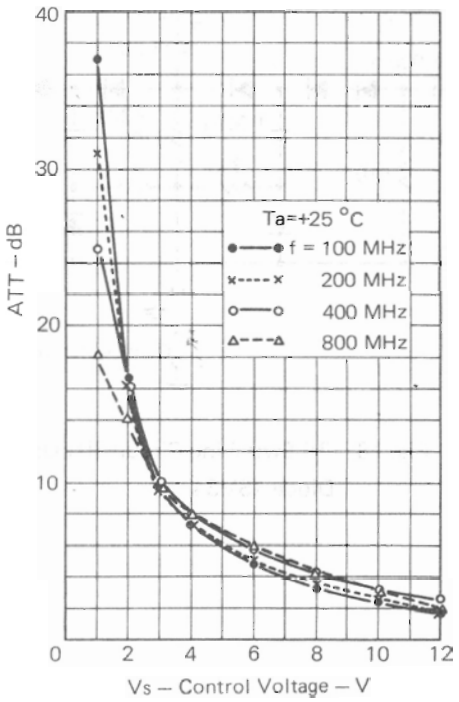


Fig. 15 Attenuation Characteristics of π-type Diode Attenuator

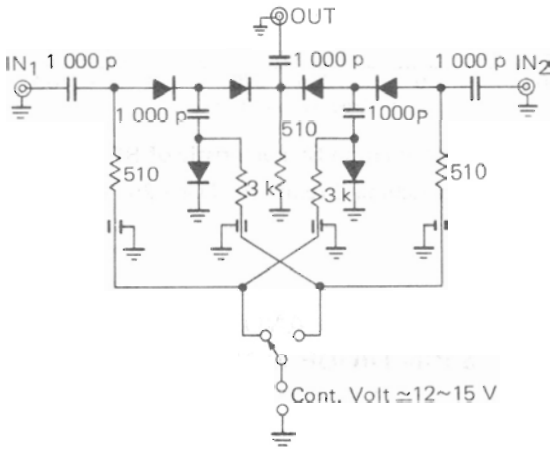


Fig. 16 RF Switching Circuit (I) Using PIN Diode 1SV34

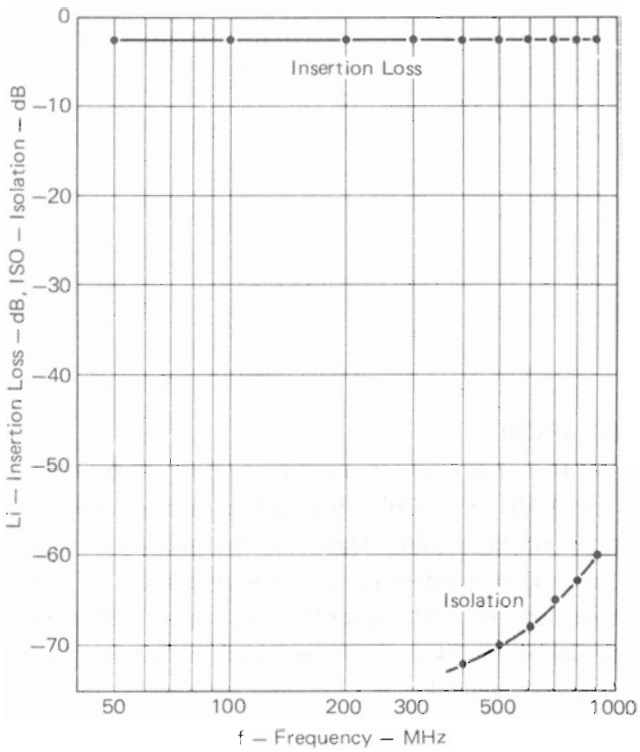


Fig. 17 Attenuation Characteristic of RF Switching Circuit (I) (Ta = 25 °C)

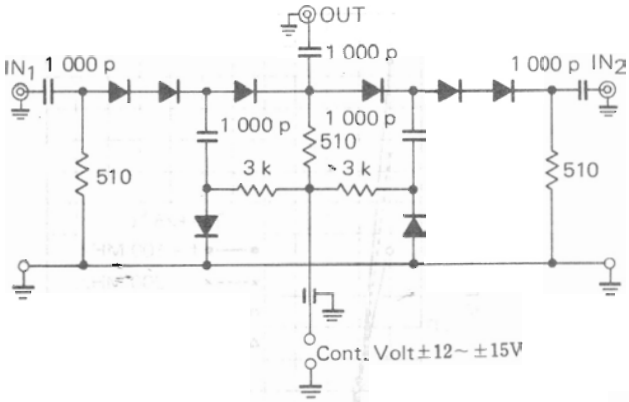


Fig. 18 RF Switching Circuit (II) Using PIN Diode 1SV34

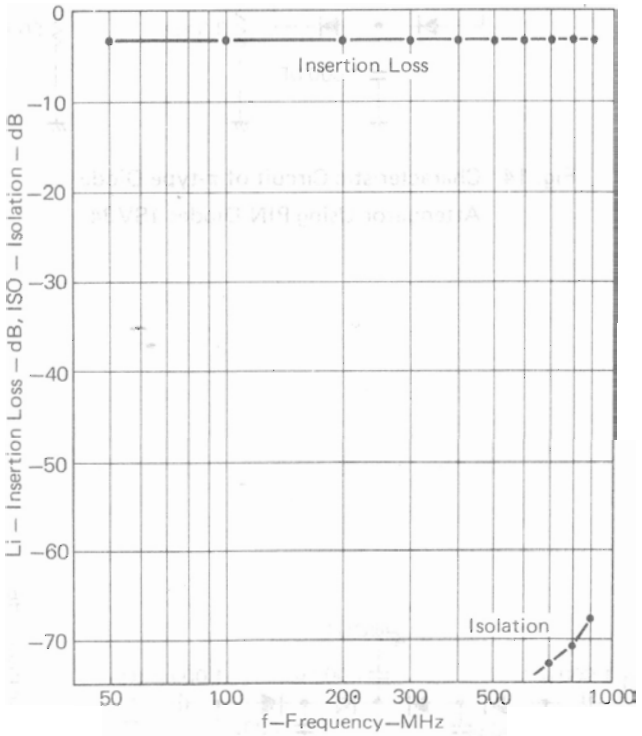


Fig. 19 Attenuation Characteristic of RF Switching Circuit (II) (Ta = 25 °C)

(5) 1SV80

This is a low-cost general-use diode to be used from 1 MHz to 1 GHz. This diode is used for applications which require diodes in the mass-consuming usages such as attenuators for consumers' CATV, TV tuners and RF switches for VTR. Its characteristics are similar to 1SV34 and it is packaged in DO–35 glass type as shown in Fig. 5.

4. CHARACTERISTICS AND APPLICATIONS OF NEC'S PIN DIODE MODULES

This is a solid-state version of TR tube which has been used for protector of ship radar system receiving mixer diode from high input power. The presently available product is ND702B for input power of 2 kW (pulse width 1.0 μs and repetition frequency 1 kHz) which is shown below. Fig. 20 shows the outline dimension of the unit which can be connected to X-Band waveguide. Figs. 21 and 22 show its frequency characteristics of its input-output and insertion loss, respectively.

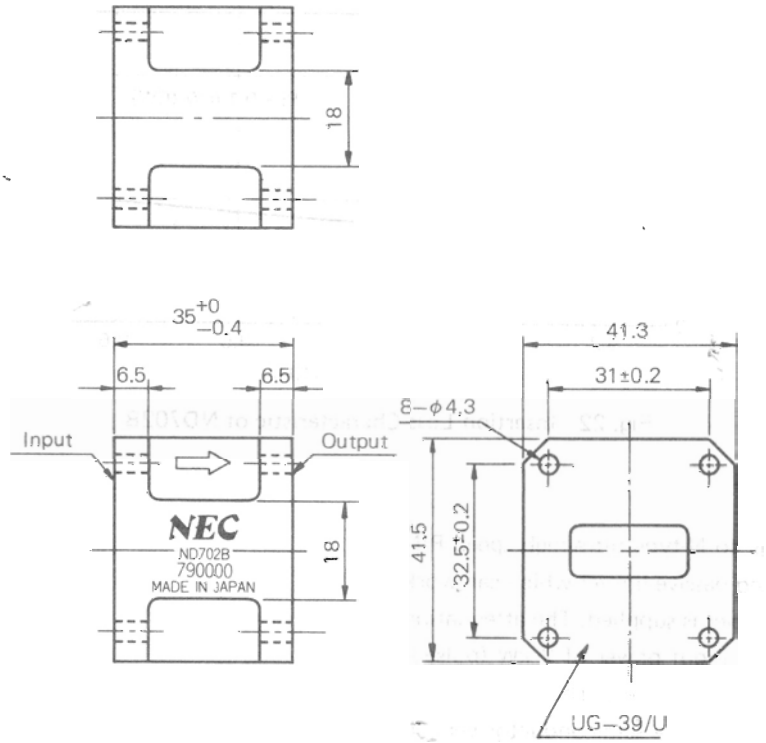


Fig. 20 Outline of PIN Diode Limiter ND702B (Unit: mm)

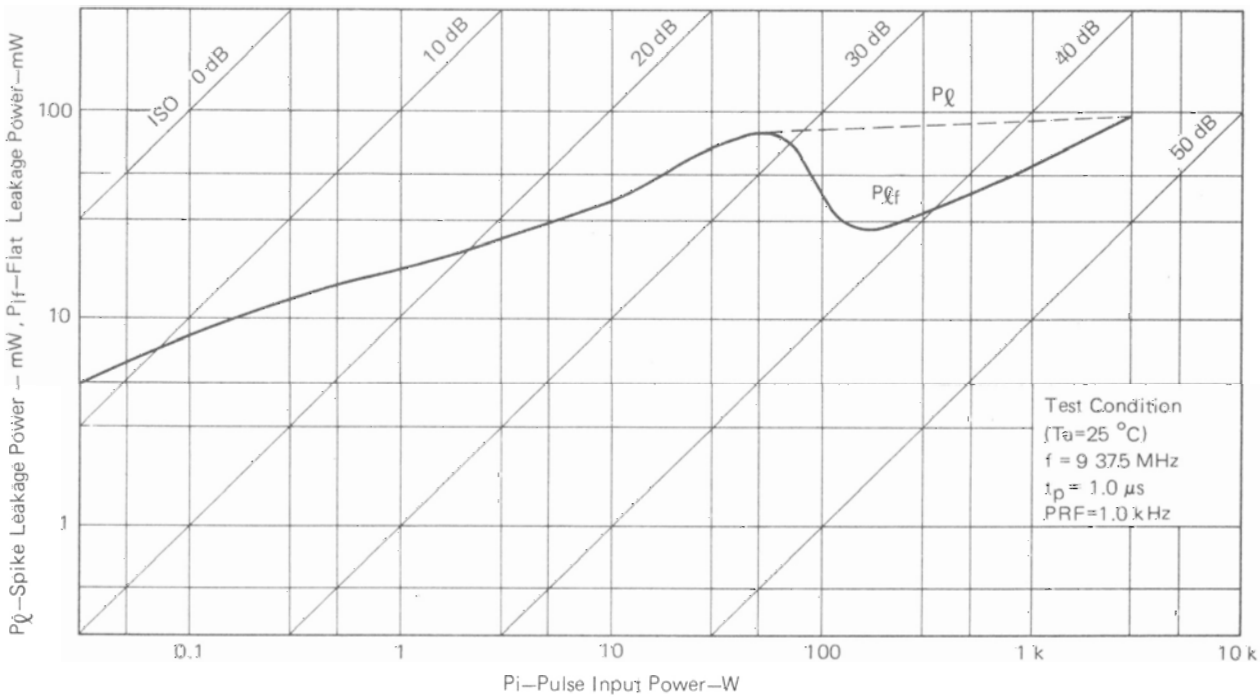


Fig. 21 Input-Output Characteristic of ND702B

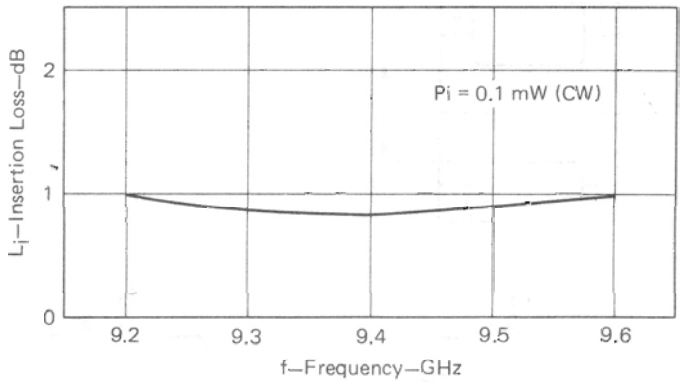


Fig. 22 Insertion Loss Characteristic of ND702B

The element belongs to N-type ultra-high speed PIN diodes. It is a zero-biased passive limiter which can work only when high input power is supplied. The attenuation is 40 dB or more for an input power of 2 kW (pulsed) and the insertion loss is 1.2 dB or less. Therfore this unit is attracting much attention as a semiconductor version of TR tube.

DOUBLE BALANCED MIXER USING NEC'S SCHOTTKY BARRIER DIODE 1SS97 OR 1SS99

1. GENERAL

Double balanced modules (DBM) using schottky barrier diodes are classified as described below according to their usages.

(1) Balanced mixer
(2) Phase detector
(3) RF modulator

Mixers using schottky barrier diodes are classified as described below according to their structures.

(1) Single mixer operating with a single diode.
(2) Single balanced mixer (SBM) operating with a pair of balanced diodes.
(3) Double balanced mixer (DBM))operating with four balanced diodes.

With a single mixer, the mixing of signal frequency f_R and local oscillation frequency f_L appears frequency of $f_R - f_L$ and $f_R + f_L$ on the IF terminal. In addition, f_R and f_L themselves appear on the IF terminal.

With a single balanced mixer, f_L does not appear on the IF terminal because the mixer is balanced against the local oscillation frequency.

Double balanced mixer is balanced not only for local oscillation frequency but also for signal frequency. Consequently, no signal except $f_R - f_L$ and $f_R + f_L$ appears on the IF terminal.

Since the mixer which not appear unnecessary components on the IF terminal is advantageous, the double balanced mixer is, of necessity, the most advantageous one.

Furthermore it has the following features.

(1) Conversion loss (L_C) is small and frequency characteristics is good (providing wide band characteristics).
(2) Isolation between signal, local oscillation and IF terminals is good.
(3) Intercept point is high.

Usually a double balanced mixer needs a relatively large local oscillation input power (3 mW – 10 mW conventionally). The feeding of large local oscillation power tends to the improvement of intermodulation distortion (IMD) characteristics. This means the raising of the intercept point which is frequently referred today. For the standard local oscillation input power of +10 dBm (10 mW), the intercept point is approximately +20 dBm (100 mW). The next paragraph describes the intercept points of NEC's schottky barrier diodes 1SS97 and 1SS99.

2. PERFORMANCE OF DOUBLE BALANCED MIXER

As shown in Figs. 1 and 2 illustrating the action of double balanced mixer, when a signal is fed to the local oscillation terminal of a circuit composition of symmetrically arranged two matching transformers and four diodes, the phase difference across the secondary of T_2 becomes 180° and the rectified current flows through D_1 and D_2. The potential of A will be equal to the potential of the central GND tap of T_2, namely, the ground potential.

Similarly, the potential of B between D_3 and D_4 is equal to GND and the relation A = B = GND = 0 holds. That means that the potential difference between A and B is zero and no voltage is induced in T_1.

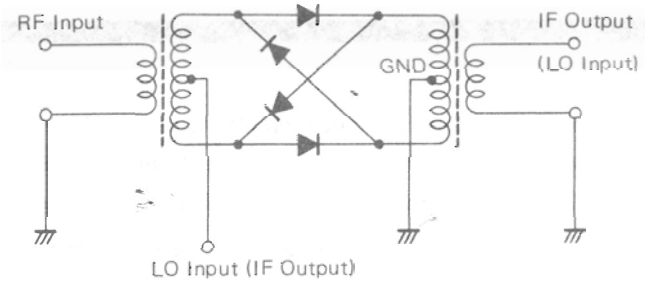


Fig. 1 Basic DBM Circuit

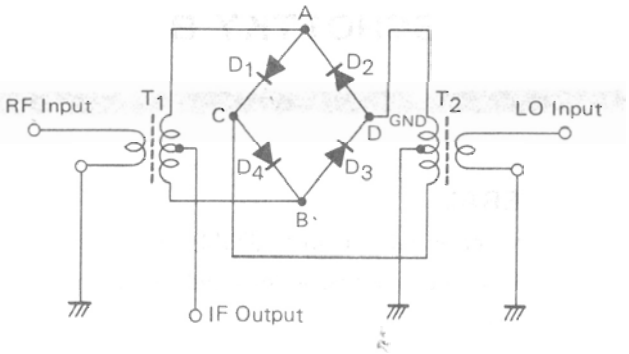


Fig. 2 DBM with Crossed over Transformers

Therefore, the local oscillation input terminal can be considered as isolated between the IF port and RF signal input port, resulting in a good isolation. When a voltage is applied to the IF port, a potential is generated at C and D point which is equal to the IF port potential due to the action of D_1, D_4 and D_2, D_3. Since no potential difference exists between A and B, no voltage is induced in T_1. This is the reason for the good isolation between the IF port and the RF port.

3. DOUBLE BALANCED MIXER USING SCHOTTKY BARRIER DIODES (1SS97 or 1SS99)

Fig. 3 shows the equivalent circuit of a double balanced mixer using NEC's schottky barrier diodes 1SS97 or 1SS99.

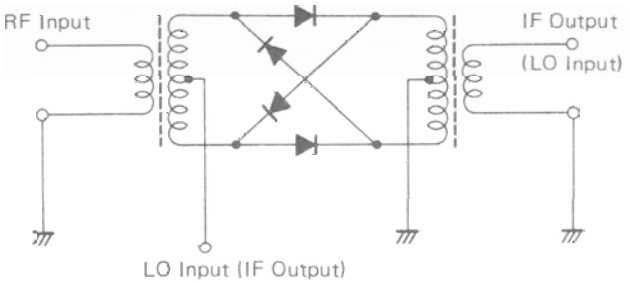


Fig. 3 Equivalent Circuit of DBM Using Double-hole Core

Figs. 4 and 5 show the conversion loss to local oscillation input power characteristics, Figs. 6 and 7 show the intermodulation distortion (intercept point) characteristics, Fig. 8 show the used double-hole care, and Figs. 9 and 10 show the insertion loss and isolation characteristics.

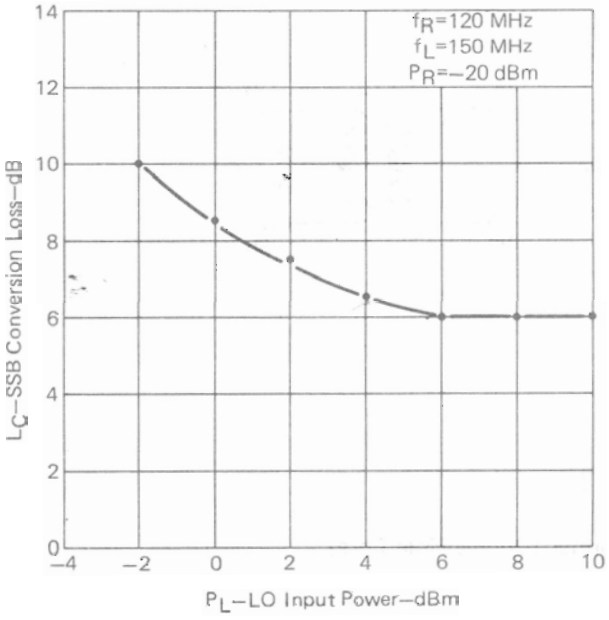


Fig. 4 L_C vs. P_L of 1SS97

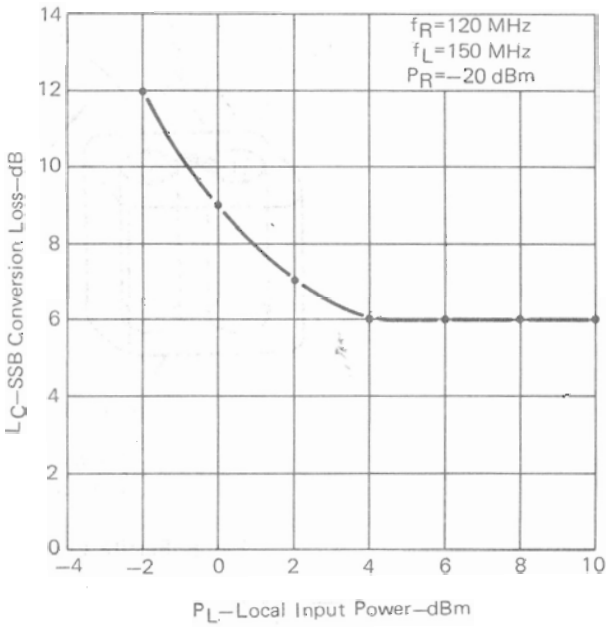


Fig. 5 L_C vs. P_L of 1SS99

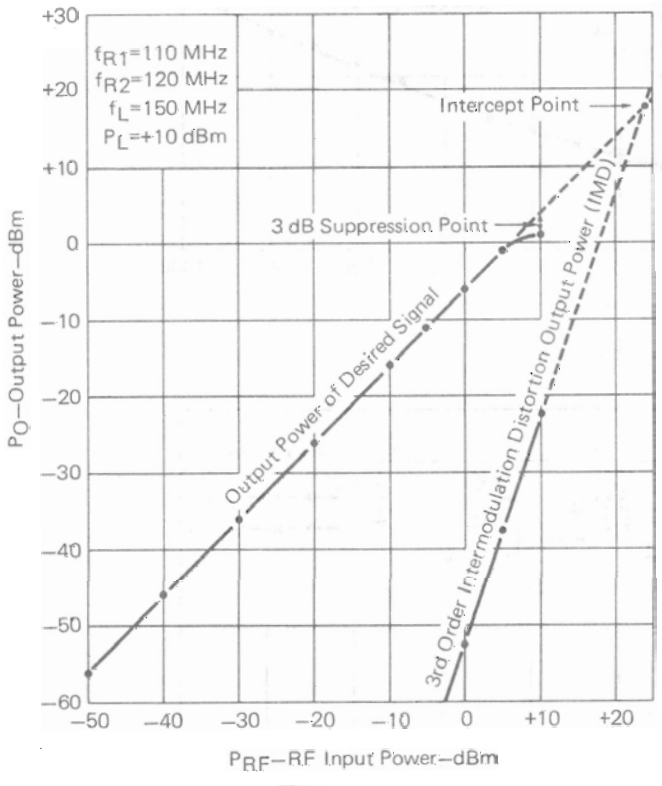


Fig. 6 Intercept Point of 1SS97

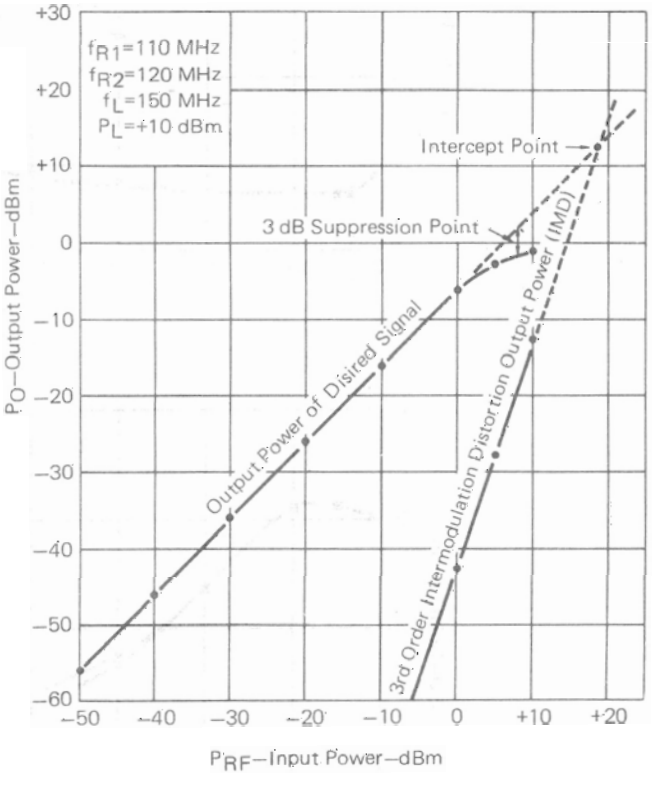


Fig. 7 Intercept Point of 1SS99

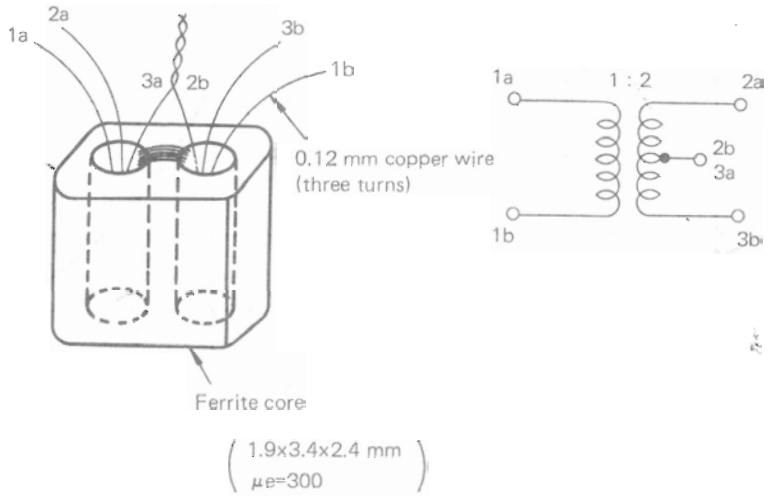


Fig. 8 Ferrite Core Transformer (Double-Hole Core)

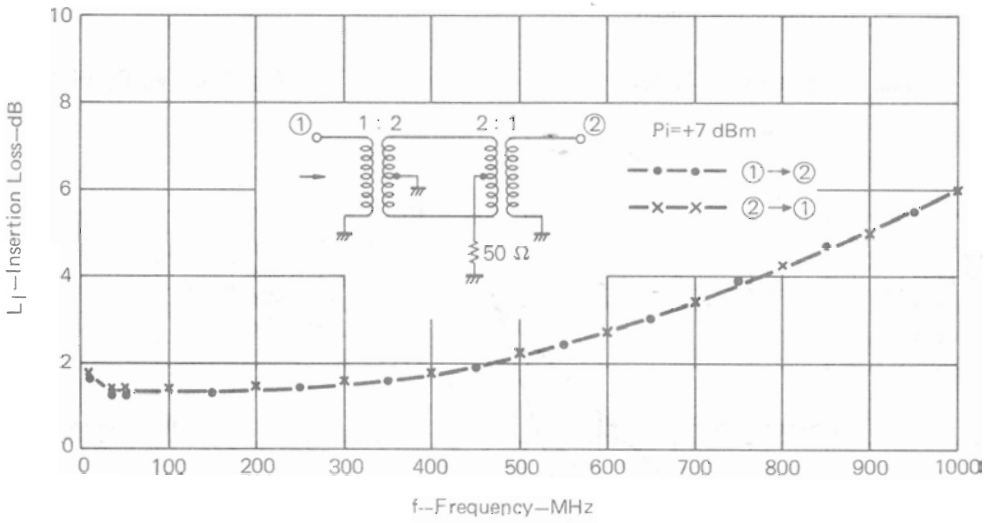


Fig. 9 Li vs. f

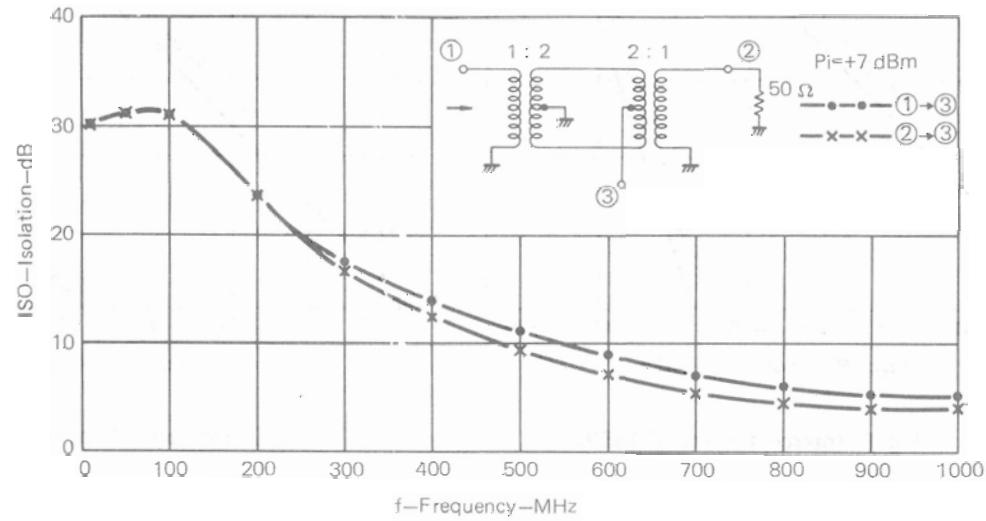
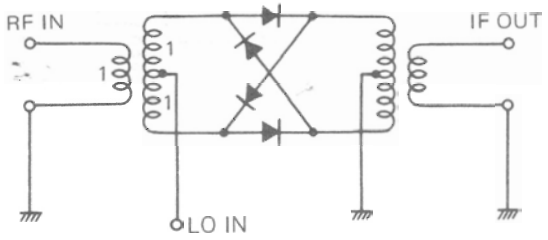


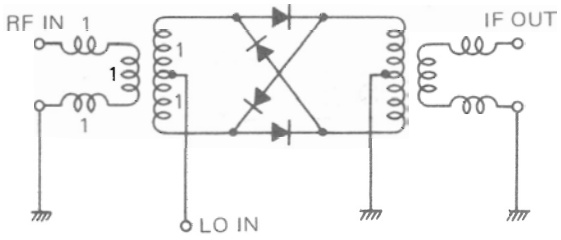
Fig. 10 ISO vs. f

4. TRANSFORMERS

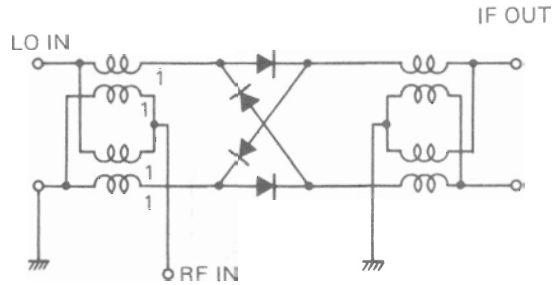
Figs. 11 and 12 show the basic circuit of various double balanced modules and the winding of transformers for double balanced modules, respectively.



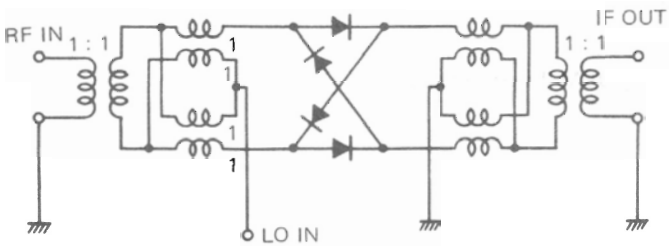
(a) The most basic circuit



(b) Isolation is good but too many transformers required



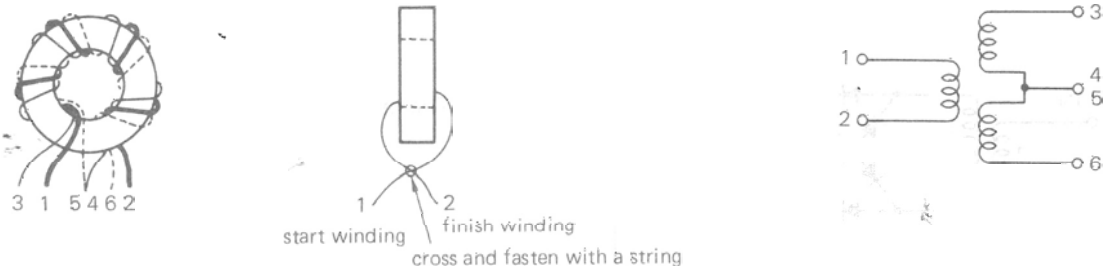
(c) Double-hole balun used for transformer, no DC voltage application allowed on signal IN, and good characteristics obtained in spite of incomplete DBM operation.



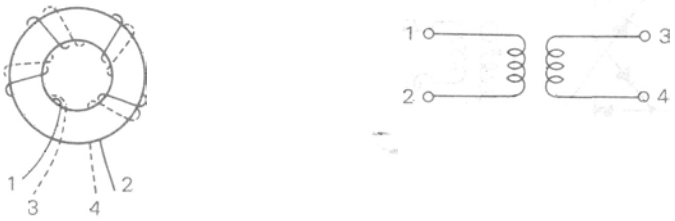
(d) Improvement of type (c), 1:1 transformer is used in front of the complete DBM double-hole balun for the use with DC voltage.

Fig. 11 Basic Circuit of Double Balanced Modules

(a) 1 : 1 : 1 Transformer to be used in Fig. 1 (a) and (b). Three ulemet wires of ϕ0.2–0.5 mm are wound in alignment on a ferrite toroidal core.



(b) 1 : 1 transformer to be used in Fig. 1 (b) and (c). Two ulemet wires of ϕ0.2–0.5 are wound in alignment on a ferrite toroidal core.



(c) Double-hole balun for UHF TV receivers or the like, to be used in Fig. 1 (c) and (d).

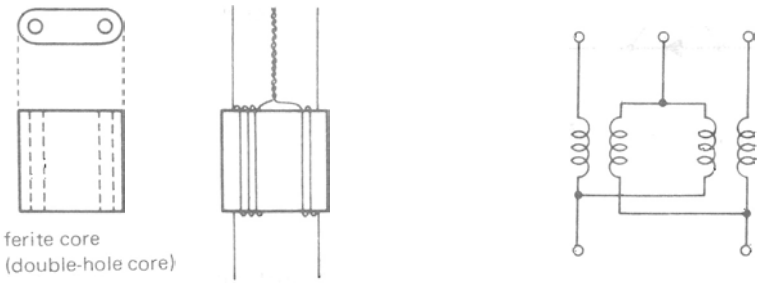


Fig. 12 Winding DBM Transformers

NEC'S SCHOTTKY BARRIER DIODE QUAD AND APPLICATION (ND487 Series)

1. GENERAL

Schottky barrier diodes formed by the contact of metal-to semiconductor are used in a very wide range from consumers applications such as TV tuners, CATV converters, and VTR modulators to industrial ones such as microwave communication systems and measuring instruments. They are rarely used as individual diodes, but in most cases, used in group as matched pair or matched quad. This document describes the introduction and the typical applications of Schottky barrier diode quads ND487 series recently developed and sold by NEC.

2. WHAT IS A SCHOTTKY BARRIER DIODE?

Schottky-barrier diode is a type of diode provided with a rectifying capability through a Schottky barrier formed on the contact of a metal and a semiconductor. Since a amount of stored carriers are little, this diode has an advantage of very short times of turn-on and turn-off.

Consequently it is used as a detector, a mixer, or a modulator for VHF/UHF through microwave band (up to 100 GHz), and, also as a switching diode for ultra-high speed gating, clamping or sampling.

Fig. 1 shows a typical structure of Schottky diode. When a forward voltage is applied to this diode which is formed by a combination of N-type epitaxial silicon layer and a metal, electrons in silicon are injected to the metal layer with much higher energy than that of free electrons in the metal, and, consequently, a forward current flows. Hence, as contrasted to PN-junction diodes whose rectifying actions are caused by the injection, of minority carriers, the rectification of Schottky barrier diode is resulted by the injection of majority carriers.

When a reverse voltage is applied, the Schottky barrier prevents the transfer of electrons from metal to semiconductor, causing no reverse current flow. Then due to the minority carrier flow is not absent, the reverse recovery time, which PN-junction diodes generally have, is not defined in Schottky barrier diode.

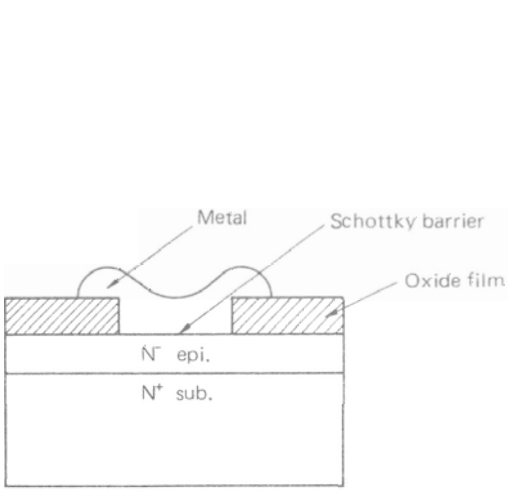


Fig. 1 Element Structure of Schottky Diode

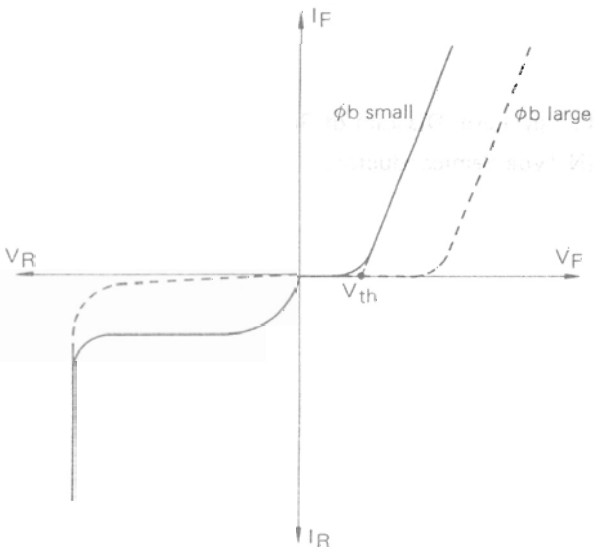


Fig. 2 Static Characteristic of Schottky Barrier Diode

The selection of the metal for a Schottky barrier diode which is formed by the contact of metal to semiconductor depends on the barrier potential (height of barrier) ϕ_b desired for the intended electrical characteristics.

The electrical characteristics related to ϕ_b are, as shown in Fig. 2, the forward threshold voltage V_{th} and the reverse current I_R in V-I characteristics.

When ϕ_b is raised too high, the hole injection is caused because a P-type inverted layer is produced in the semiconductor contacted to the metal, and the advantage of the Schottky barrier is lost. Practically, metals with ϕ_b of 0.5–0.85 eV are used. The reason of P-type layer production is understood as a phenomenon that, when the electronic potential in the N-type domain is raised too high by the space-charge layer, the Fermi level at the semiconductor surface contacted to the metal is depressed below the center of the forbidden band.

The energy level diagram of Schottky barrier diode is illustrated in Fig. 3.

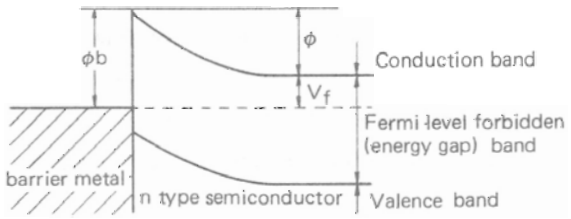


Fig. 3 Energy Level Diagram of Schottky Barrier Diode (N-Type Semiconductor)

Following the above description on the general structure of Schottky barrier diode, this document will explain a Schottky barrier diode quad recently developed and completed as a product by NEC for double balanced modulator.

3. SCHOTTKY BARRIER DIODE QUAD

As described previously, Schottky barrier diodes are widely used for detector, mixer and phase modulator in a frequency range from VHF to microwave bands. Since they are hardly used as single element but in most cases used as a matched pair (two units matched in characteristics) or a matched quad (four units matched in characteristics), the integration of the units has been demanded. The product which has been integrated as a monolithic IC on this demand is Schottky barrier diode quads ND487 series.

Table 1. List of NEC's Schottky Barrier Diode Quad

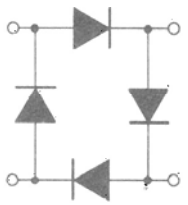
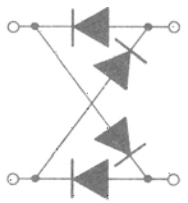
Type No.	Outline	Internal Connection	Electrical Characteristics (Ta=25°C)	Remarks
ND487C1-3R	Disk mold type	Cross	V_{F1}=0.7 VMAX. @ I_F=50 mA V_{F2}=0.3 VMAX. @ I_F=1 mA $\triangle V_{F2}$=20 mVMAX. @ I_F=1 mA C_t=1.2 pFMAX. @ f=1 MHz, V_R=0 $\triangle C_T$=0.2 pFMAX. @ f=1 MHz, V_R=0	* Internal connection  (1) Cross  (2) Ring
ND487R1-3R		Ring		
ND487C2-3R		Cross	V_{F1}=1.0 VMAX. @ I_F=50 mA V_{F2}=0.5 VMAX. @ I_F=1 mA $\triangle V_{F2}$=20 mVMAX. @ I_F=1 mA C_t=1.2 pFMAX. @ f=1 MHz, V_R=0 $\triangle C_t$=0.2 pFMAX. @ f=1 MHz, V_R=0	
ND487R2-3R		Ring		
ND487C1-3P	Micro-X type	Cross	V_{F1}=0.7 VMAX. @ I_F=50 mA V_{F2}=0.3 VMAX. @ I_F=1 mA $\triangle V_{F2}$=20 mVMAX. @ I_F=1 mA C_t=1.0 pFMAX. @ f=1 MHz, V_R=0 $\triangle C_t$=0.1 pFMAX. @ f=1 MHz, V_R=0	
ND487R1-3P		Ring		
ND487C2-3P		Cross	V_{F1}=1.0 VMAX. @ I_F=50 mA V_{F2}=0.5 VMAX. @ I_F=1 mA $\triangle V_{F2}$=20 mVMAX. @ I_F=1 mA C_t=1.0 pFMAX. @ f=1 MHz, V_R=0 $\triangle C_t$=0.1 pFMAX. @ f=1 MHz, V_R=0	
ND487R2-3P		Ring		

Table 1 shows the series of products, ND487 series. The following merits can be attributed to ND487 series.

(1) Being a one-chip double balanced module, well balanced characteristics can be expected between four electrodes.

(2) Since diodes are interconnected in cross configuration, the circuit configuration can be simplified.

(3) Since the quad can be used as a double balanced mixer of diodes, a wideband characteristic and a large dynamic range can be obtained.

(4) Being packed in a small package, it can be densely mounted and, consequently, it is suitably used for portable and mobile sets.

4. STRUCTURE OF SCHOTTKY BARRIER DIODE QUAD

4-1 External Structure

The external view of ND487 series is shown in Fig. 4 and its outline dimensions in Fig. 5 and 6.

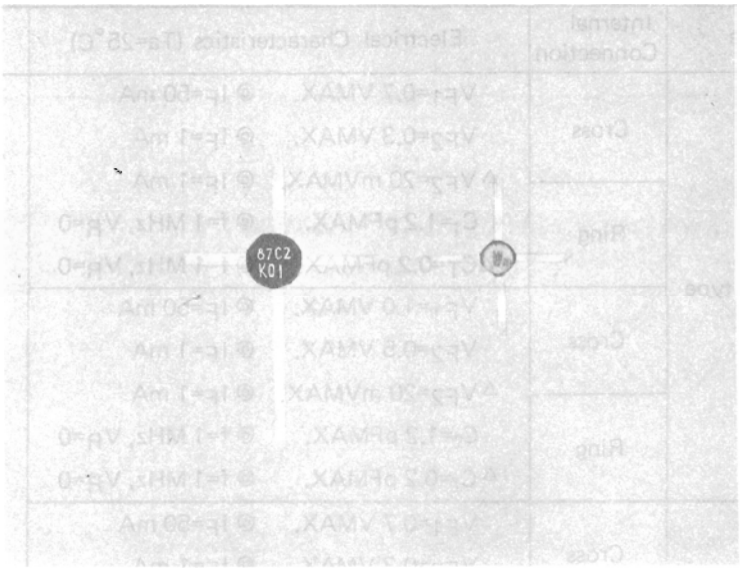


Fig. 4 External View of ND487 Series (disk mold and micro-X type)

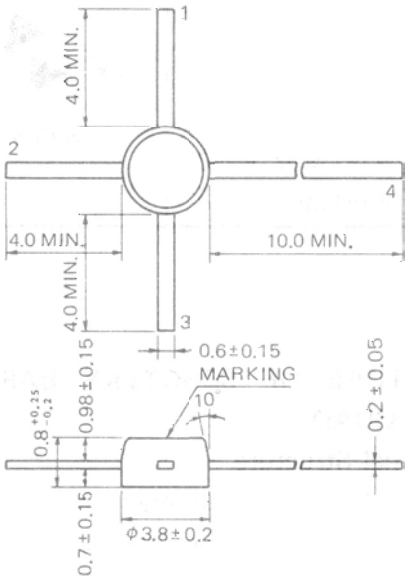


Fig. 5 Outline Dimensions of Disk Mold Type
(Unit: mm)

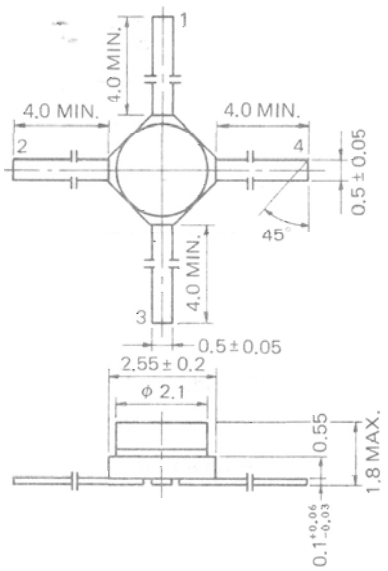


Fig. 6 Outline Dimensions of Micro-X Type
(Unit: mm)

Two types are available, disk-mold type of a structure effective for costdown and micro-X type hermetically sealed with ceramic. Either of the both occupies a much smaller space than any arrangement of four elements of usual glass-sealed Schottky barrier diodes.

4-2 Diode Pellet Structure

Usual Schottky barrier diode has a structure shown in Fig. 1, and when a voltage supply between metal and silicon, the diode operate with a diode characteristics. However, in a diode quad, four diode elements must be formed on a chip and each diodes must be connected in

series on a chip.

The series resistance and capacitance should be reduced because they determine the quality of Schottky barrier diode.

These points have been taken into account as shown in Figs. 7 and 8 by adapting striped diode element structures and by shortening the distances between the ohmic electrodes and the Schottky barrier electrodes to an extent where no problem is generated during usual processings.

There are two types of wiring between diode elements. They are the cross type where the wires are crossed over on the pellet to facilitate the construction of double balanced modulator and the ring type where the distance from a diode element to the corresponding bonding pad is equalized to have freedom from the phase defferences.

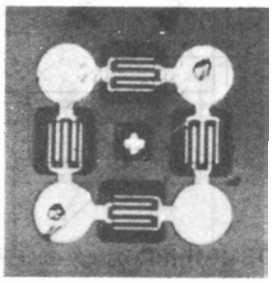


Fig. 7 External View of Ring Type Pellet

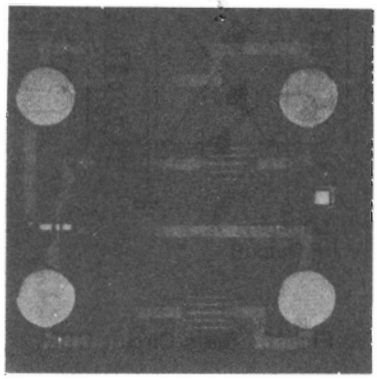


Fig. 8 External View of Cross Type Pellet

5. CHARACTERISTICS OF SCHOTTKY BARRIER DIODE

5-1 V-I Characteristics

The V-I characteristics of single diode element in ND487 series can be classified into two types, as shown in Fig. 9, dependent on the combination of silicon and metal composing the Schottky barrier.

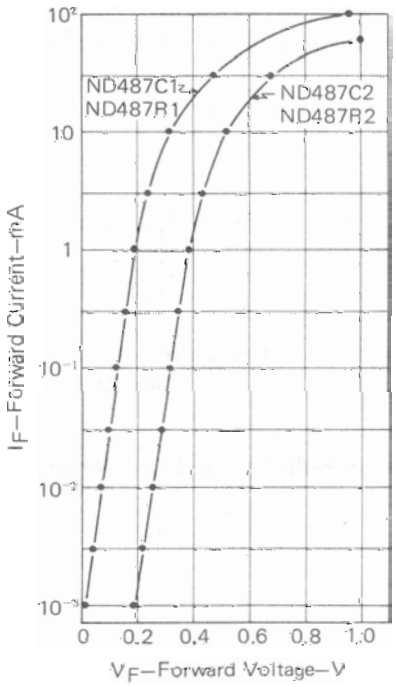


Fig. 9 Single Diode Element Characteristics of ND487 Series

5-2 Circuit Configuration and Characteristics of Double Balanced Mixer

As an example of application of a Schottky barrier diode quad, the characteristics of a double balanced mixer circuit is described.

In general, there are two types of double balanced mixer, the one that arranges diodes crossed-over on each other as shown in Fig. 10 and the other one that arranges transformers partly crossed over as shown in Fig. 11. When a quad diode is fermed on a chip and the diode's characteristics are equalized to each other, this diode quad constitutes ND487 series.

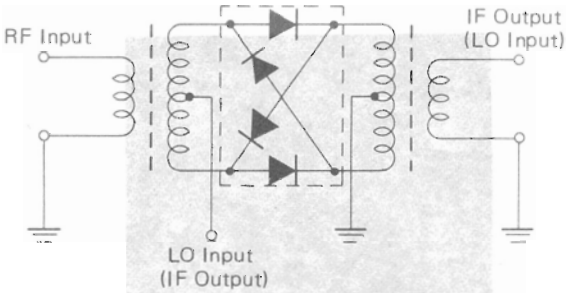


Fig. 10 Basic Circuit DBM

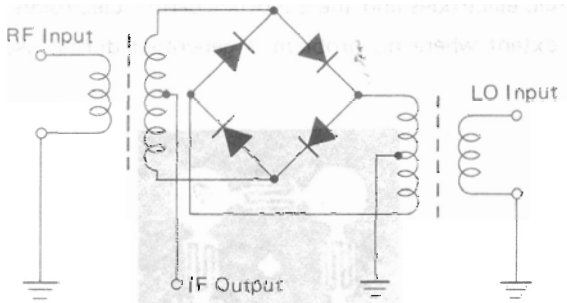


Fig. 11 DBM with Crossed over Transformers

The advantages of the double balanced mixers are:

(1) Good isolations are obtained between terminals signal, local oscillation, and IF.

(2) High intercept point can be reached.

(3) Wide-band and large dynamic range are obtained.

The characteristics of a double balanced mixer using ND487 series are described.

The transformer has been prepared using a taiyo-yuden's core (μe=300) with double holes and the coils have been wade of three enamel coated wires gathered in a bundle and wound two turns around the core illustrated in Fig. 12.

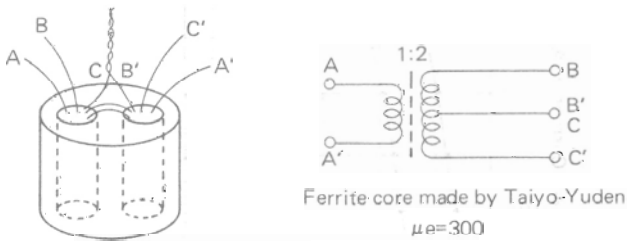


Fig. 12 Double-Hole Core and Coil Winding

Because conversion loss, isolation, and frequency band-width of double balanced mixer largely depends on the matching transformer, it is important to make it in low loss and well-balanced.

The measured characteristics of the double balanced mixers shown in Figs. 10 and 11 prepared with ND487 series will be described below.

Fig. 13 shows the conversion loss to local oscillation input power characteristics. With ND487C1 and R1, a conversion loss (L_C) of 5.5 dB is experienced at local oscillation input power (P_L) of +3 dBm (2 mW). With ND487C2 and R_2, L_C is 5.5 dB at P_L of +7 dBm (5 mW).

Fig. 14 shows the frequency characteristics demonstrating conversion loss and isolation for varied signal and local oscillation frequencies with IF (Intermediate Frequency) held constant at 30 MHz. Both characteristics are satisfactorily wide-band up to 500 MHz. According to the isolation characteristic, the local oscillation input appearing at the IF terminals is −20 dB or less (1/100 or less) which is negligible (The frequency characteristic of the transformer rolls off beyond 500 MHz.).

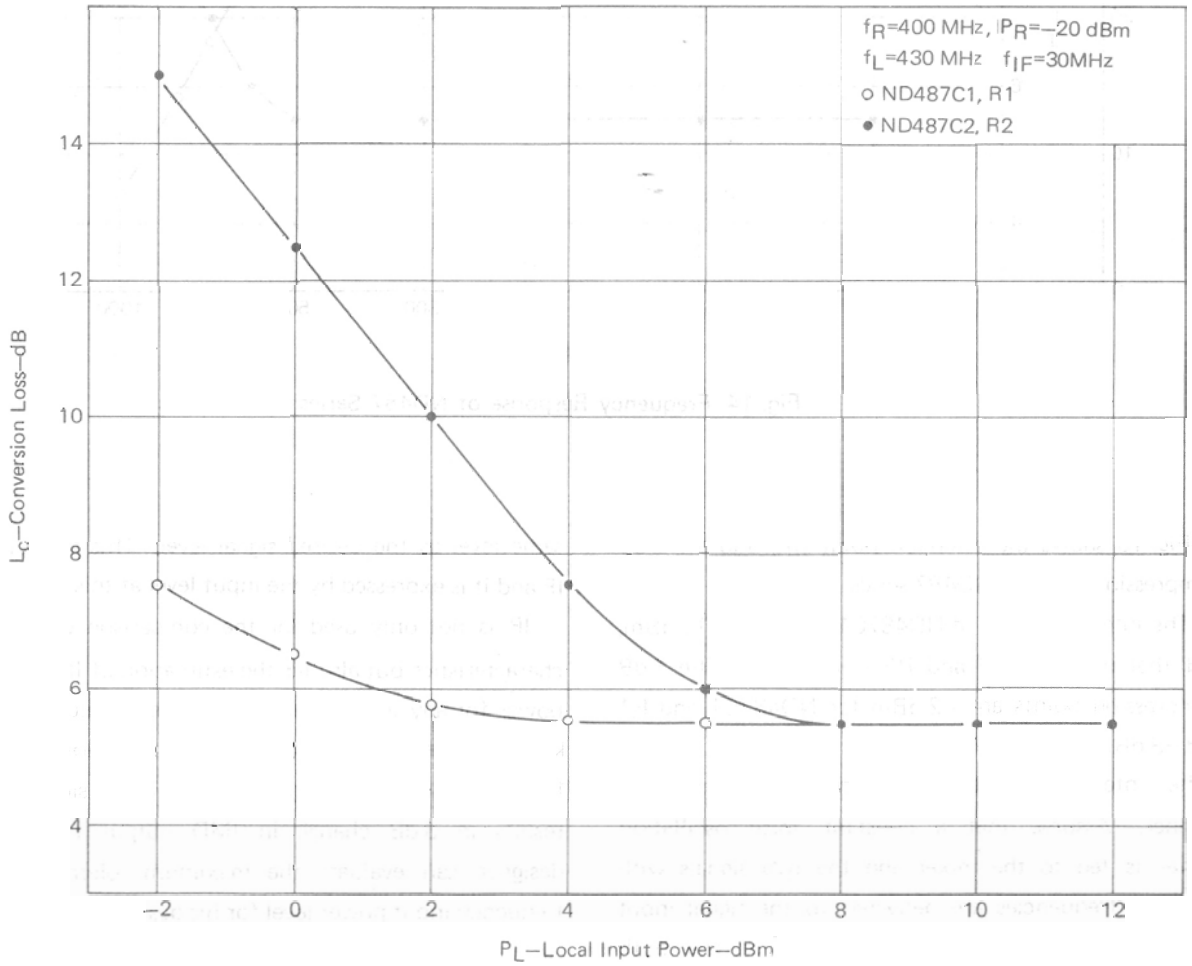


Fig. 13 Conversion Loss Characteristic of ND487 Series

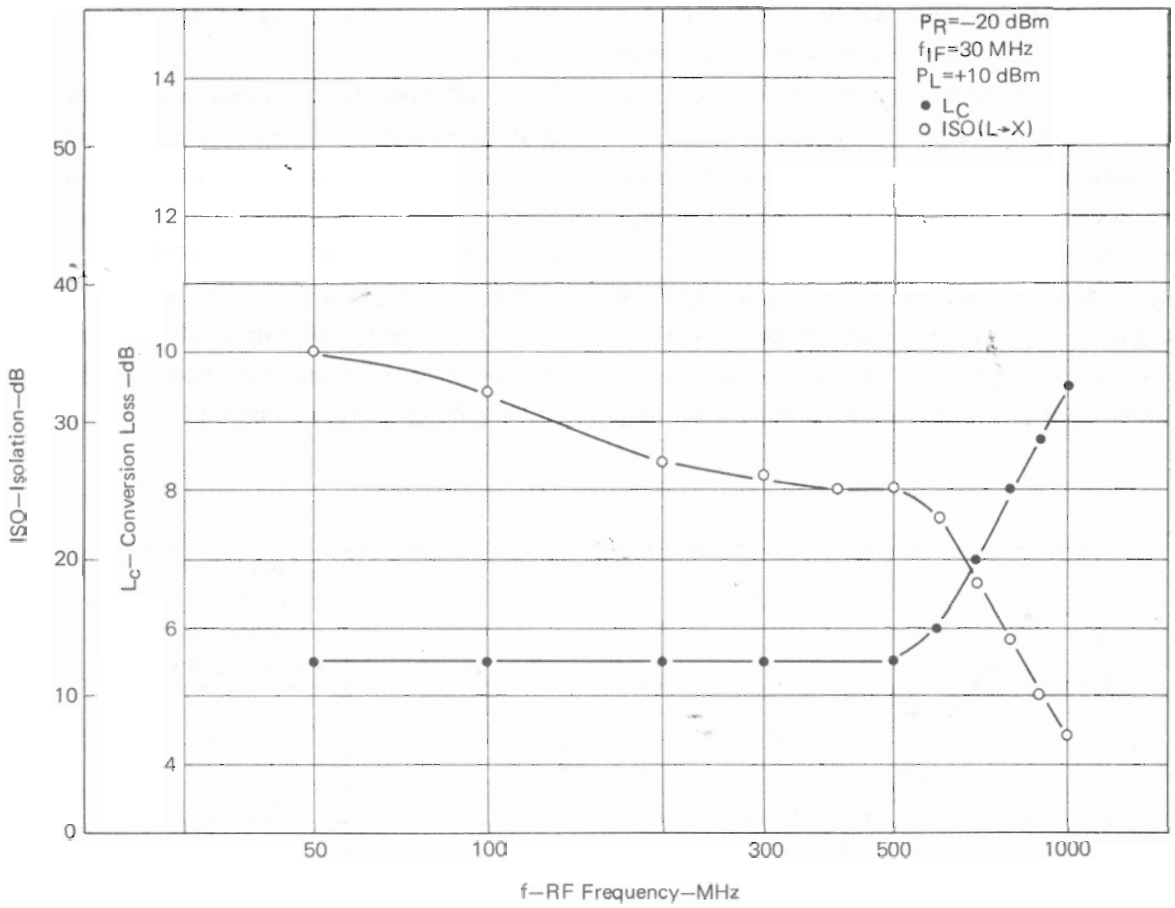


Fig. 14 Frequency Response of ND487 Series

Fig. 15 shows the intercept point (IP) and the 1 dB compression point of ND487 series.

The intercept point of ND487C1 and R1 is +13 dBm, and that of ND487C2 and R2 is +18 dBm. The 1 dB compression points are −2 dBm for ND487C1 and R1 and +3 dBm for ND487C2 and R2.

The intercept point is defined in the following manner. Assume that a constant local oscillation power is fed to the mixer and the two signals with different frequencies are delivered to the signal input terminal. As far as the input levels of the both signals are low, the third order intermodulaiton distortion power (IMD) remains very small and its curve must be located around the bottom of the graph. However, the increase in the input signal levels will bring about a rapid increase of the IMD output power reaching the same level as the desired signal level. This point is the IP and it is expressed by the input level at this point.

IP is not only used for the comparison of element characteristics but also for the estimation of IMD output power for any input signal level if the IP value has been known once. That is, by using the relationship that 1 dB change in each of the both input signal levels results in 3 dB change in IMD output power, the designer can evaluate the maximum tolerable radio-frequency input power level for his design.

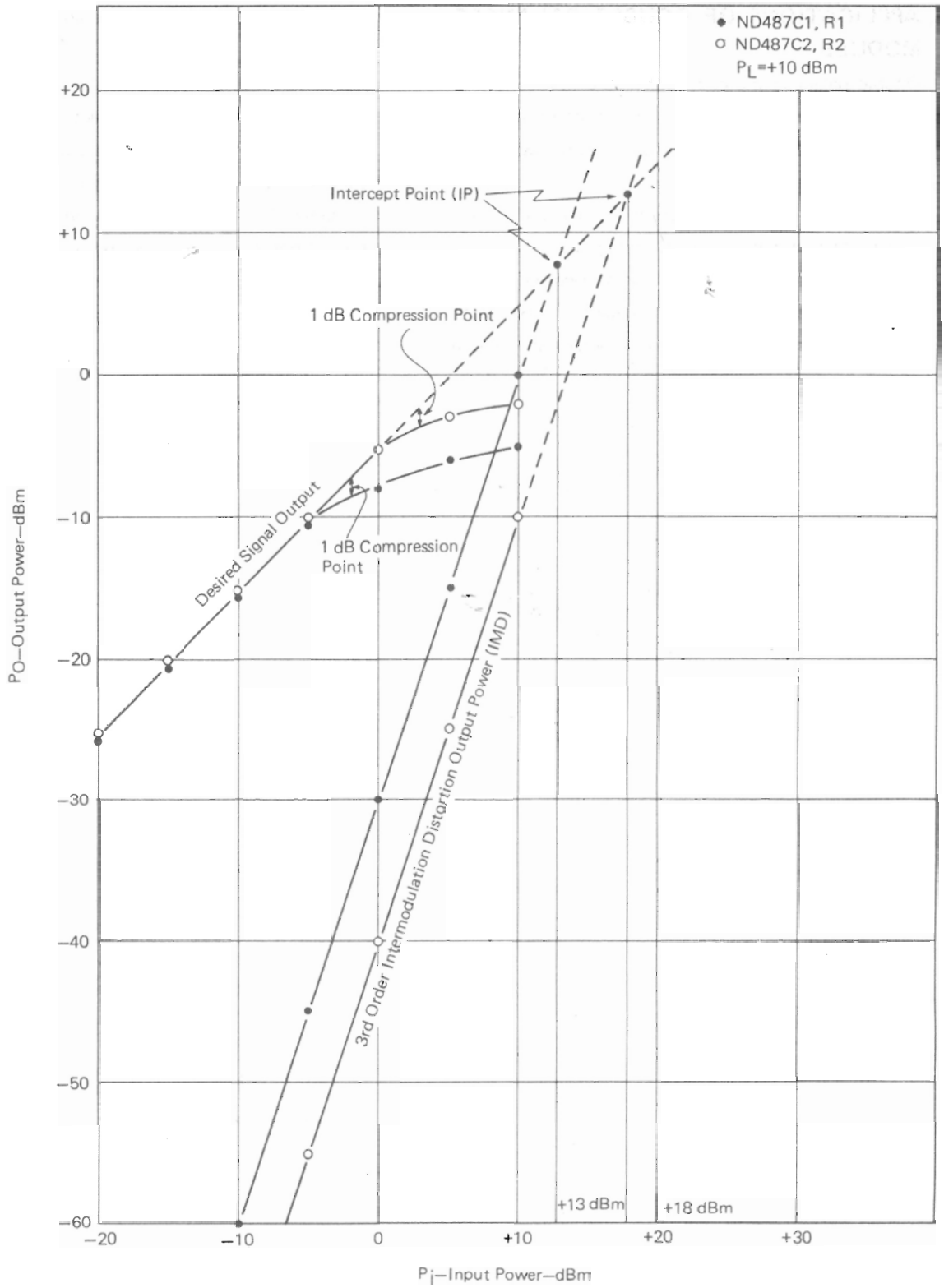


Fig. 15 P_i vs. P_O of ND487 Series

6. APPLICATIONS OF DOUBLE BALANCED MODULE

Double balanced module can be used in a variety of applications other than simple transmission or reception mixers. Typical applications are described below.

(1)Pulse modulator

For example, a circuit shown in Fig. 10 can be used as a pulse modulator if a DC voltage can be applied to its IF terminal and when constant-current pulses are fed as input. The bouble balanced mixer with wide band characteristics has an advantage that a wide range of pulse duty cycle and pulse width can be handled.

(2)Phase modulator

This modulator utilizes the fact that, when input powers of the identical frequency are fed to the local oscillation terminal and the signal input terminal at the same time, a DC output corresponding to the phase difference of the two input signals is obtained on the IF output terminal. This mcdulator is used for phase locking and phase detection.

CHARACTERISTICS OF 2 GHz BAND MIXER USING 1SS97, 1SS98 AND 1SS99

The 1SS97, 1SS98, and 1SS99 are Si Schottky barrier diodes developed for VHF–UHF bands mixer, switch, or detector. This document describes their characteristics when they are used in a 2 GHz band mixer.

1. ELECTRICAL CHARACTERISTICS OF 1SS97, 1SS98, and 1SS99

Tables 1 and 2 show the absolute maximum ratings and electrical characteristics of 1SS97, 1SS98, and 1SS99. Their outline dimensions are shown in Fig. 1.

Table 1. Absolute Maximum Ratings

Item	Rating (Ta=25 °C)			Unit
	1SS97	1SS98	1SS99	
V_R	10	5.0	5.0 note 1	V
I_F	35	50	30	mA
Pd	150	150	150	mW
Tj	175	175	175	°C
Tstg	−65~+175	−65~+175	−65~+175	°C
Bo Note 2	2.0	2.0	2.0	erg

Note 1. Peak Reverse Voltage (VRM)
Note 2. Cp=25 pF

Table 2. Electrical Characteristics

Type No.	Electrical Characteristics (Ta=25 °C)					
	Symbol	Conditions	MIN.	TYP.	MAX.	UNIT
1SS97	V_R	I_R=10 μA	10			V
	V_F	I_F=10 mA	0.46		0.55	V
	C_t	V_R=0, f=1 MHz			1.0	pF
	$\triangle V_F$	I_F=10 mA			10	mV
	$\triangle C_t$	V_R=0, f=1 MHz			0.2	pF
1SS98	V_R	I_R=100 μA	5.0			V
	I_R	V_R=1 V			500	nA
	V_{F1}	I_F=1 mA			0.34	V
	V_{F2}	I_F=10 mA			0.45	V
	C_t	V_R=0, f=1 MHz			1.0	pF
1SS99	I_R	V_R=0.5 V			25	μA
	V_F	I_F=1 mA			0.23	V
	I_F	V_F=0.5 V	30			mA
	C_t	V_R=0.2 V, f=1 MHz			0.9	pF

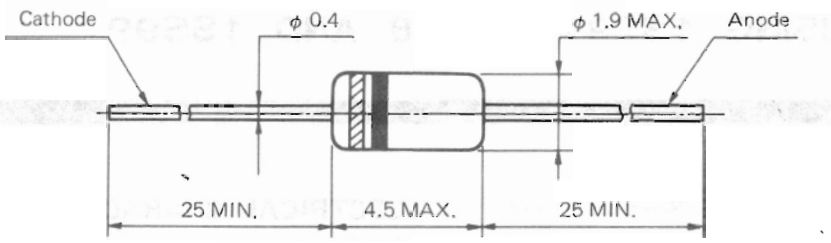
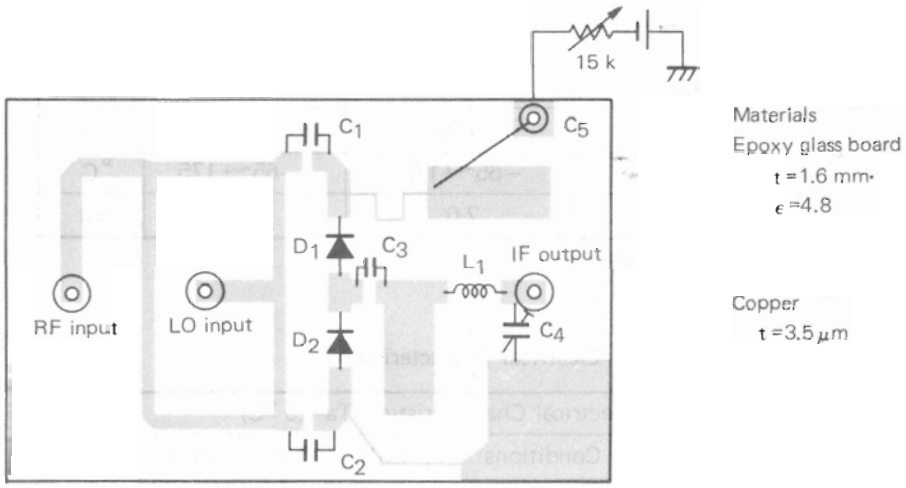


Fig. 1 Package Dimensions (Unit: mm)

2. 2 GHz BAND MIXER CIRCUIT

Fig. 2 shows the circuit of 2 GHz–band mixer.



C_1, C_2, C_3	:	1 000 pF chip capacitor
D_1, D_2	:	Schottky diode
L_1	:	5 turns of ϕ 0,6 mm tin-plated wire wound to 4.5 mm inner dia.
C_4	:	20 pF ceramic trimmer capacitor
C_5	:	1 000 pF feed-through capacitor

Fig. 2 2 GHz Band Mixer Circuit

3. CONVERSION LOSS TO LOCAL OSCILLATION INPUT POWER CHARACTERISTICS

The conversion loss versus local oscillation input power characteristics of 1SS97, 1SS98, and 1SS99 at zero bias are shown in Figs. 3, 4, and 5, respectively.

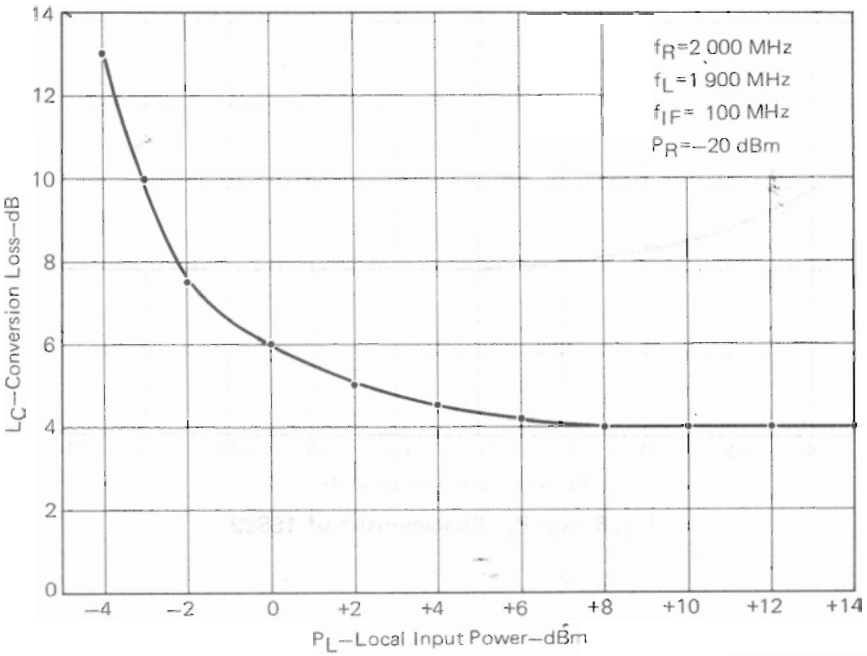


Fig. 3 L_C–P_L Characteristic of 1SS97

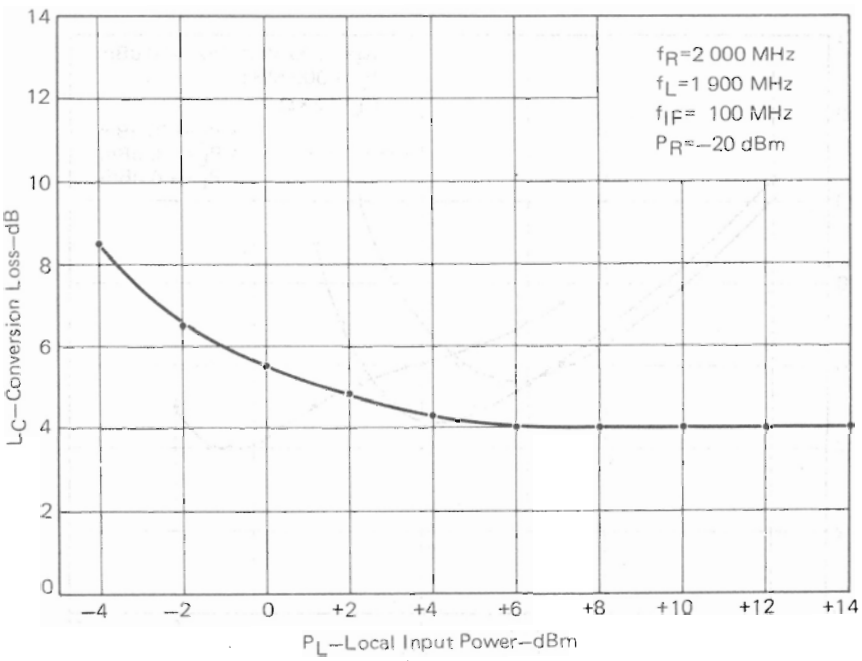


Fig. 4 L_C–P_L Characteristic of 1SS98

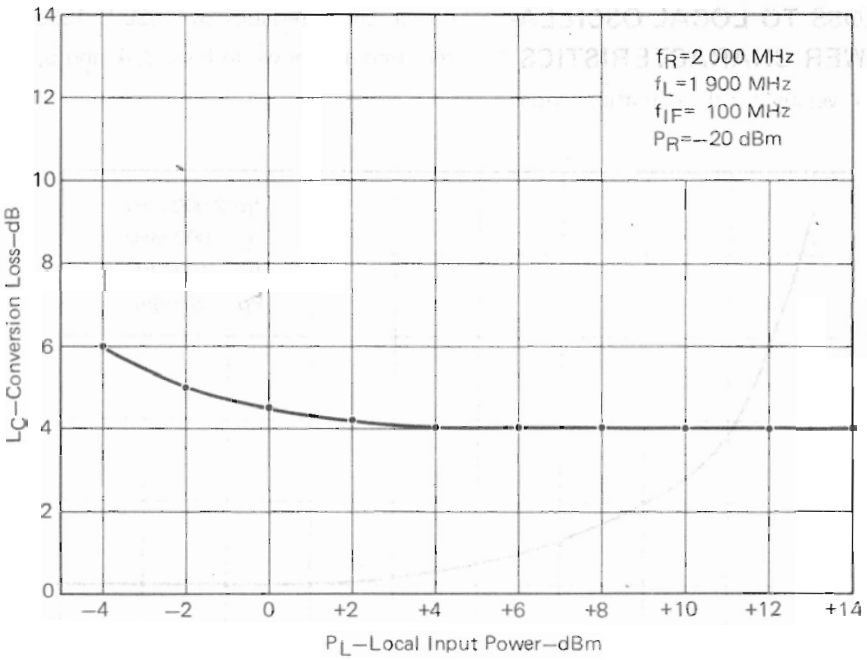


Fig. 5 L_C–P_L Characteristic of 1SS99

4. BIASING CHARACTERISTICS

Figs. 6, 7, and 8 show the biasing characteristics of 1SS97, 1SS98, and 1SS99, respectively, for externally applied DC bias voltage.

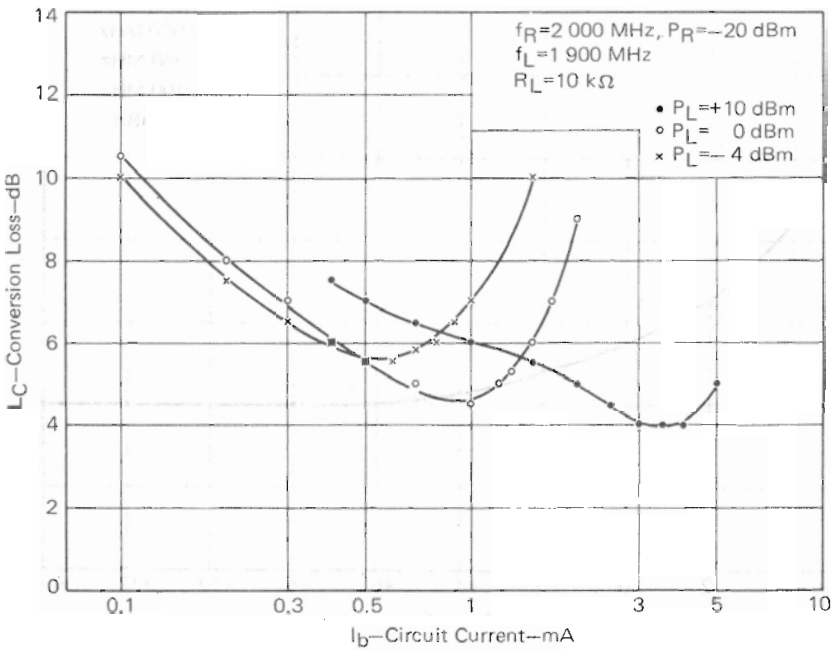


Fig. 6 L_C–I_b Characteristic of 1SS97

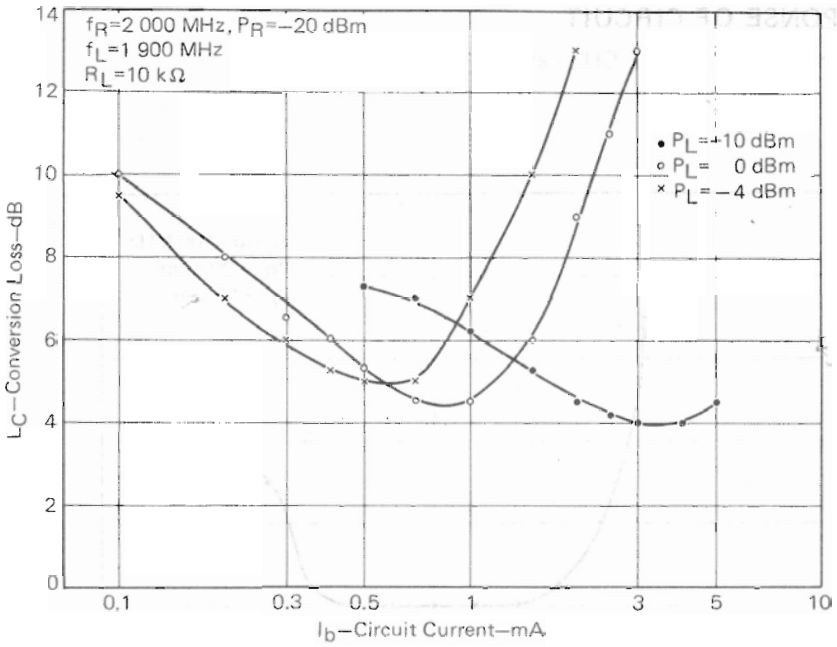


Fig. 7 L_C—I_b Characteristic of 1SS98

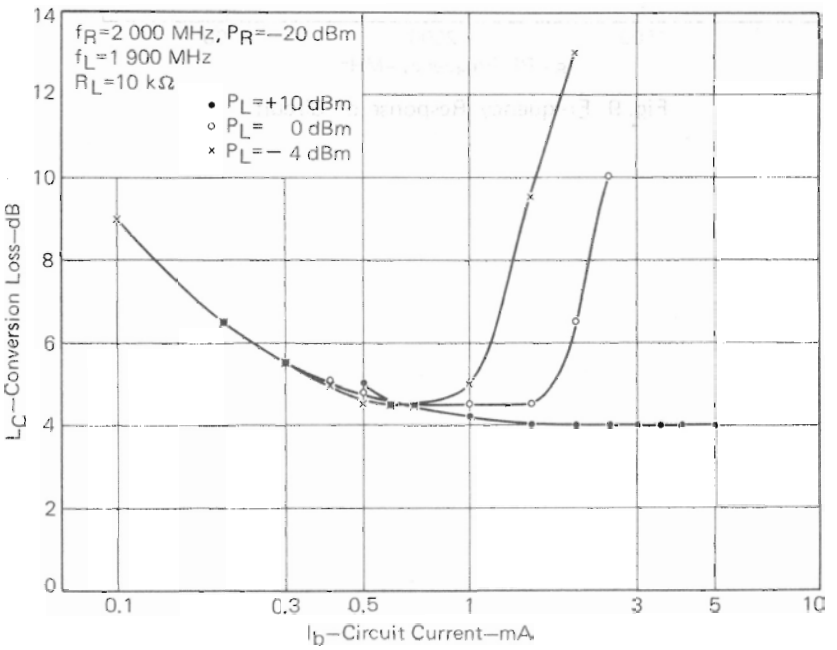


Fig. 8 L_C—I_b Characteristic of 1SS99

5. FREQUENCY RESPONSE OF CIRCUIT

Fig. 9 shows the frequency response of 2 GHz band mixer circuit.

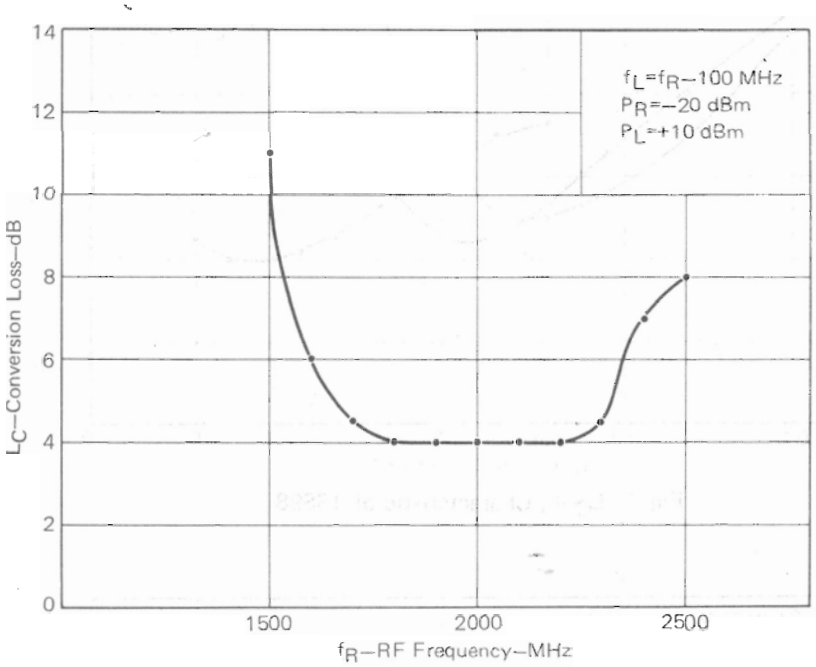


Fig. 9 Frequency Response of Circuit

NEC Corporation
INTERNATIONAL ELECTRON DEVICES D
SUMITOMO MITA Building, 37-8
Minato-ku, Tokyo 108, Japan
Tel: Tokyo 454—1111
Telex Address: NECTOK J22686
Cable Address: MICROPHONE TOKYO

NEC HONG KONG Limited, Taipei Branch
5Fl., No148, Sung Chiang Rd.
Taipei
Taiwan
Tel: 02-522-4192, 522-4258
Telex: 22372 HK NEC TP

NEC HONG KONG Limited Head Office
6th & 7th Floor,
Chuan Hing Industrial Building
14 Wang Tai Road, Kowloon Bay
Kowloon, Hong Kong
Tel: 3-7559008
Telex: 54561 HK NEC HX

NEC SINGAPORE PTE. LTD.
38 Ang Mo Kio Industrial Park 2
Singapore 2056
Tel: 4819881/9
Telex: NECSIN RS 39726

MS—3001E December 1986P Printed in Japan